Chapter 1

Definition:

- Computer architecture p2
- instruction set architecture (ISA)
- Computer organization
- A hierarchical system p3
- Structure
  - four main structural components (traditional single-processor computer) p4
  - four major structural components of CPU
- Function 定义总述
  - four basic functions that a computer can perform

Central processing unit (CPU)

Core

Processor

Chapter 4

method of accessing 4个方式的定义p122

performance: 3 definition

physical characteristics: 两对定义

relationship between access time, capacity and cost perbit

memory hierarchy 分为3层，每层是什么，以及实例?

As one goes down the hierarchy, the following occur (4)

principle of locality

cache address (2)

methods of mapping (3)

replacement algorithm (4)

write policy (2)

阐述这幅图的理解

首先给出这幅图的主题（自变量，因变量）

4点

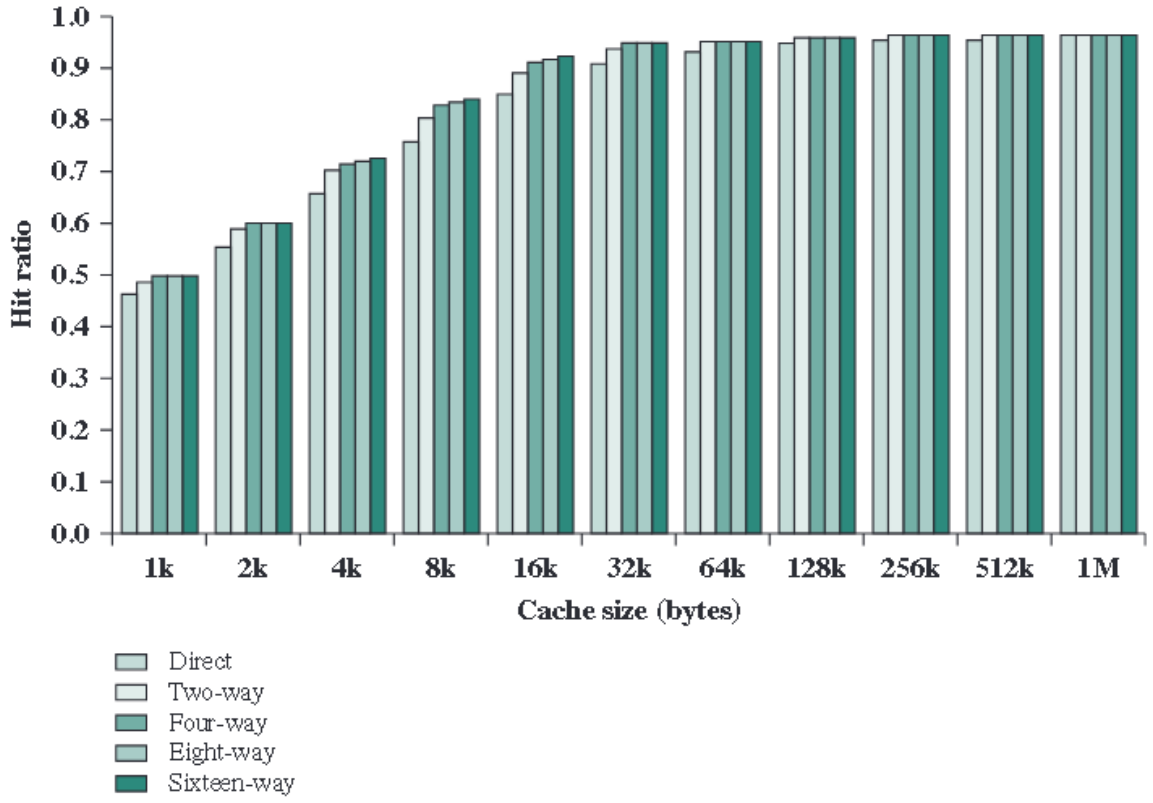


Figure 4.16 Varying Associativity over Cache Size

阐述下面这幅图，先介绍主题，然后insight1点，阐述可能的解释

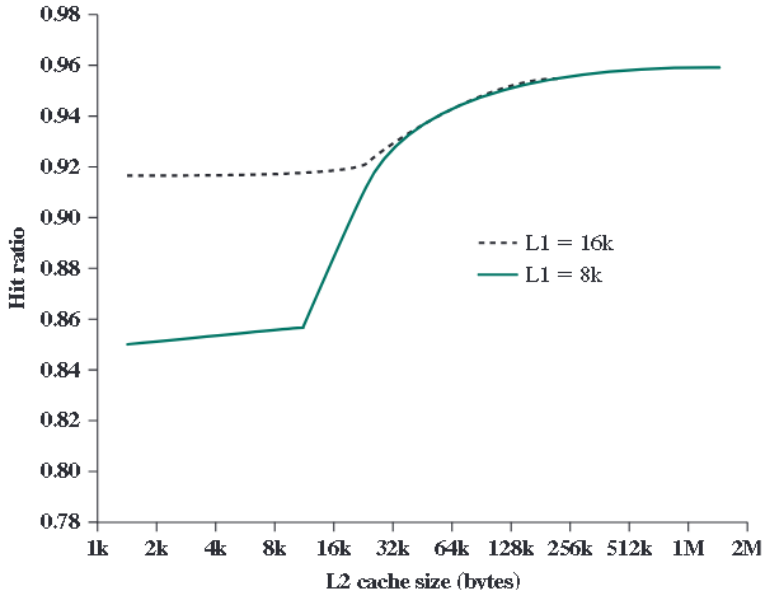


Figure 4.17 Total Hit Ratio (L1 and L2) for 8-kB and 16-kB L1

Chapter 12

Elements of a Machine Instruction, 4个

操作数的来源和去向4个 p414

指令的4个类型 p416

操作数类型 4个

Chapter 13

寻址方式7种，优缺点

instruction format 的设计因素两条

allocation of bits影响因素6条

Chapter 14

两种reg在处理器中扮演的角色

user-visible reg 4种

control and status reg 4个实例

解释图

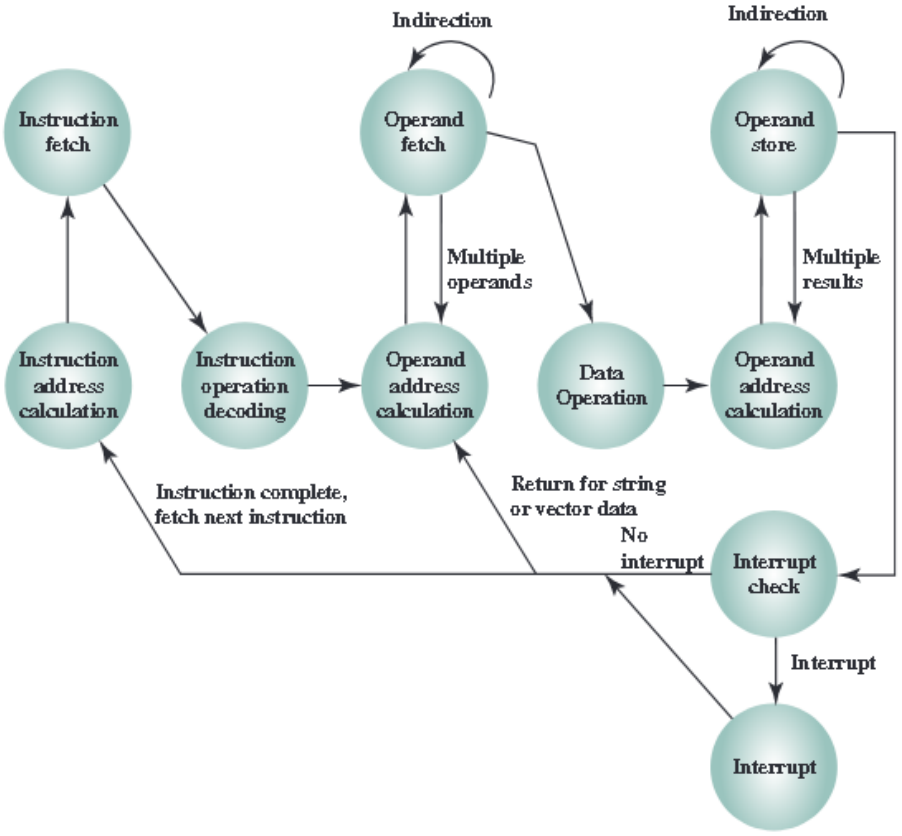
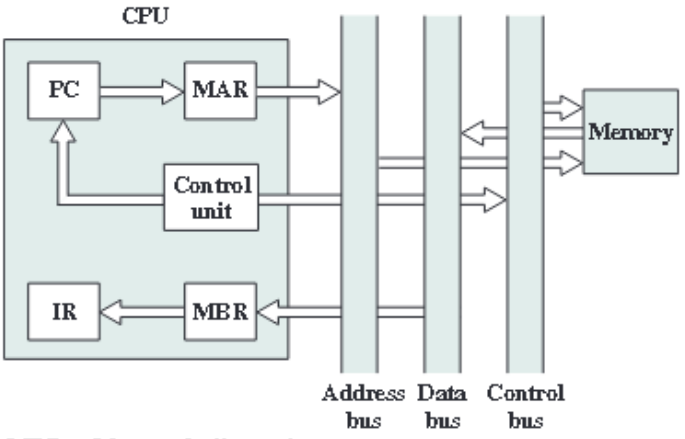


Figure 14.5 Instruction Cycle State Diagram



MBR = Memory buffer register
MAR = Memory address register
IR = Instruction register
PC = Program counter

Figure 14.6 Data Flow, Fetch Cycle

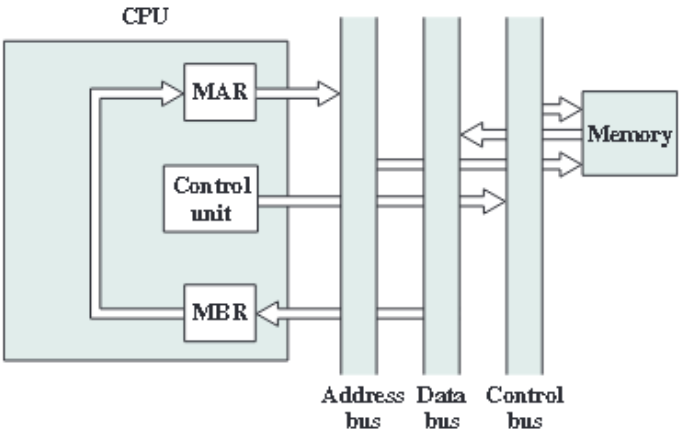


Figure 14.7 Data Flow, Indirect Cycle

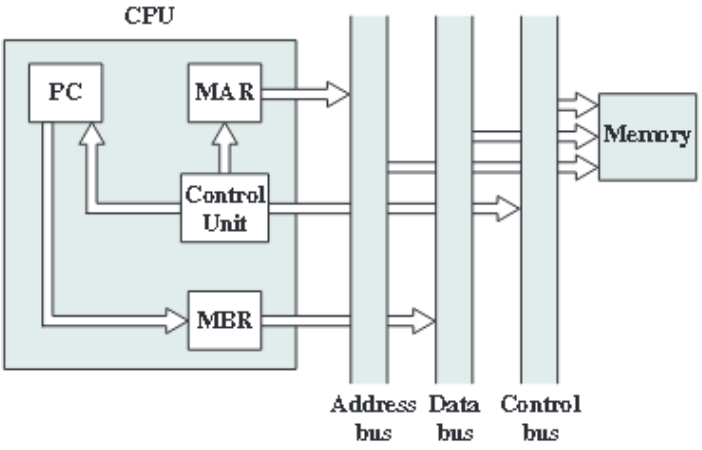


Figure 14.8 Data Flow, Interrupt Cycle

解释下面这幅图

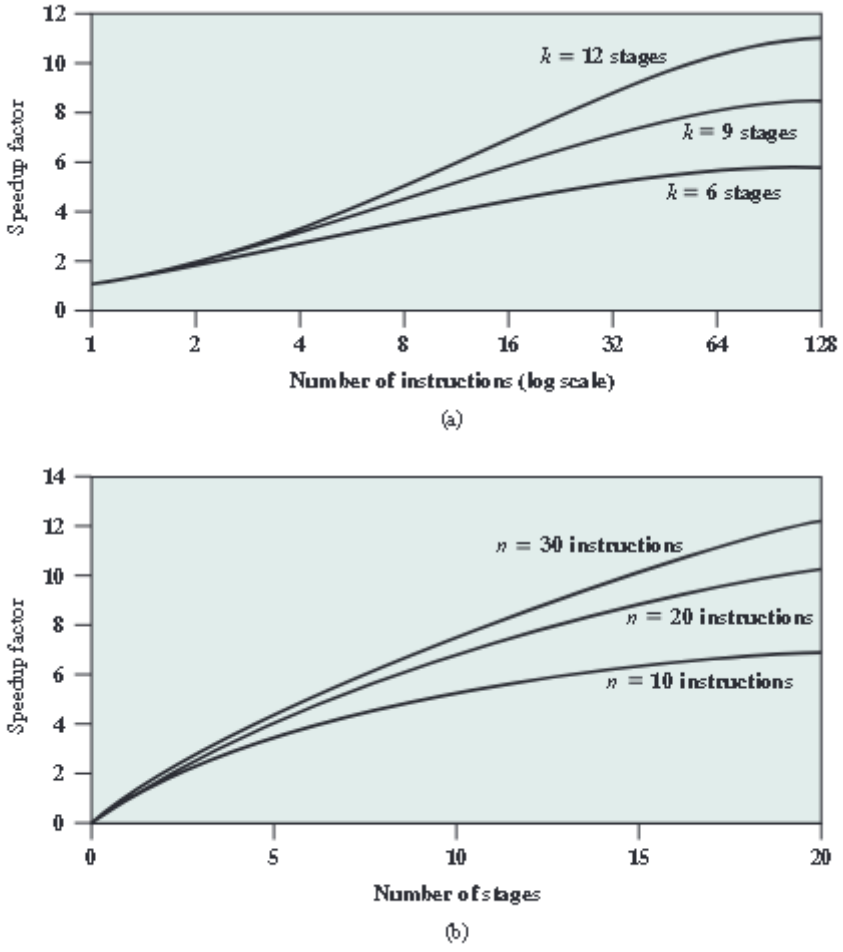


Figure 14.14 Speedup Factors with Instruction Pipelining

branch prediction 5种

解释图

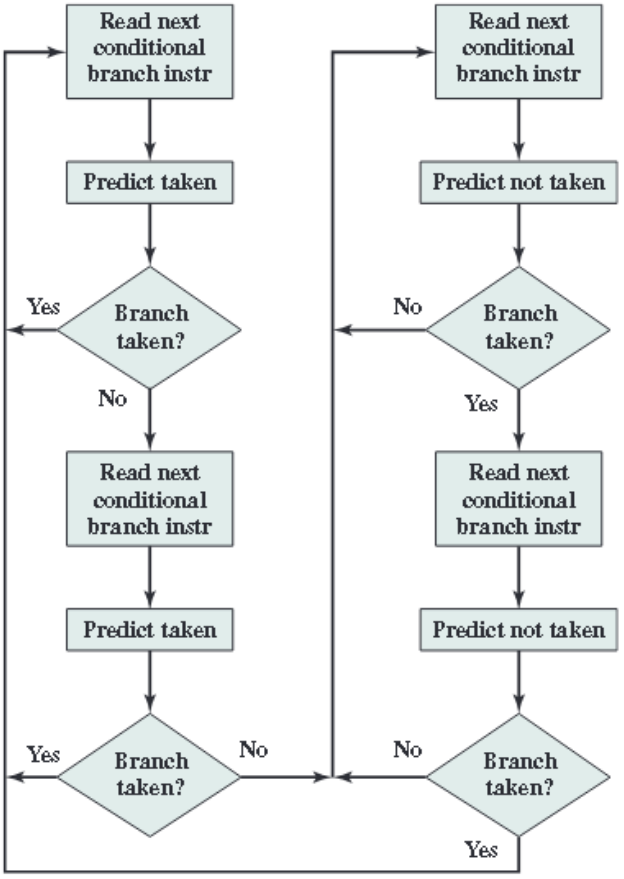


Figure 14.18 Branch Prediction Flowchart

delayed branch

Chapter 15

key elements shared by most RISC design (3) p537

解释图

环形buffer种有几个windows，现在的指针指在哪里，如果call一个，怎么变化，再call一个，如果重叠怎么变化（N-window register file can hold only N - 1 procedure activations.）

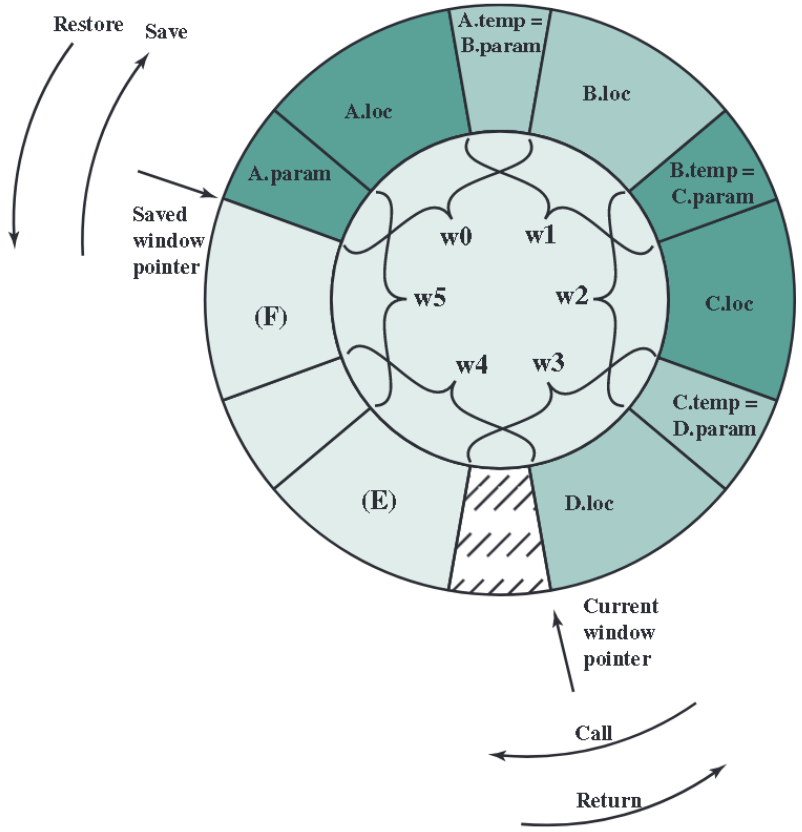


Figure 15.2 Circular-Buffer Organization of Overlapped Windows

Characteristics of Reduced Instruction Set Architectures 4点

Delayed branch 定义概念 p557

Loop unrolling 概念

Chapter 16

ILP 概念 p579

限制ILP的5个因素

fig16.4 填图

reg renaming 定义 p587

为什么延迟分支在超标量计算机出来之后失宠?

Chapter 20

micro-operation 定义

取指阶段的3个时隙，4步微操作，注意PC自增在第二个阶段发生

间址阶段的3个时隙，3步微操作

中断周期的3个时隙，4个微操作

fig20.2 可能考填图

input (4) & output (2)

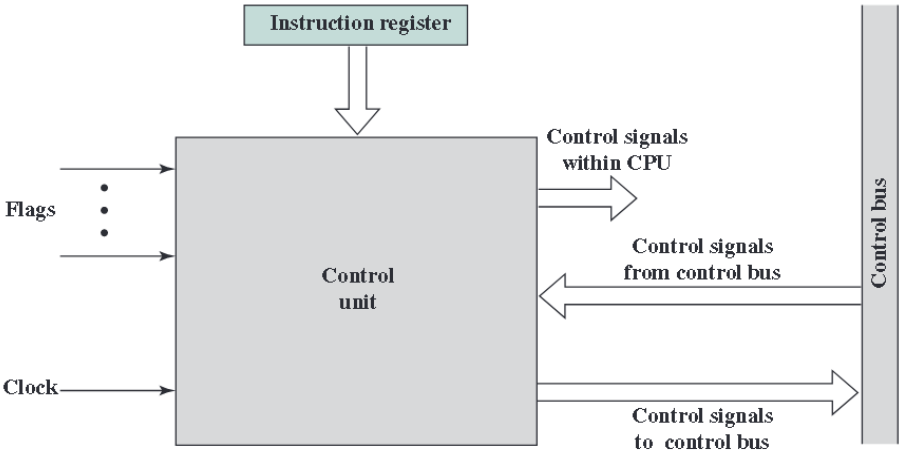


Figure 20.4 Block Diagram of the Control Unit

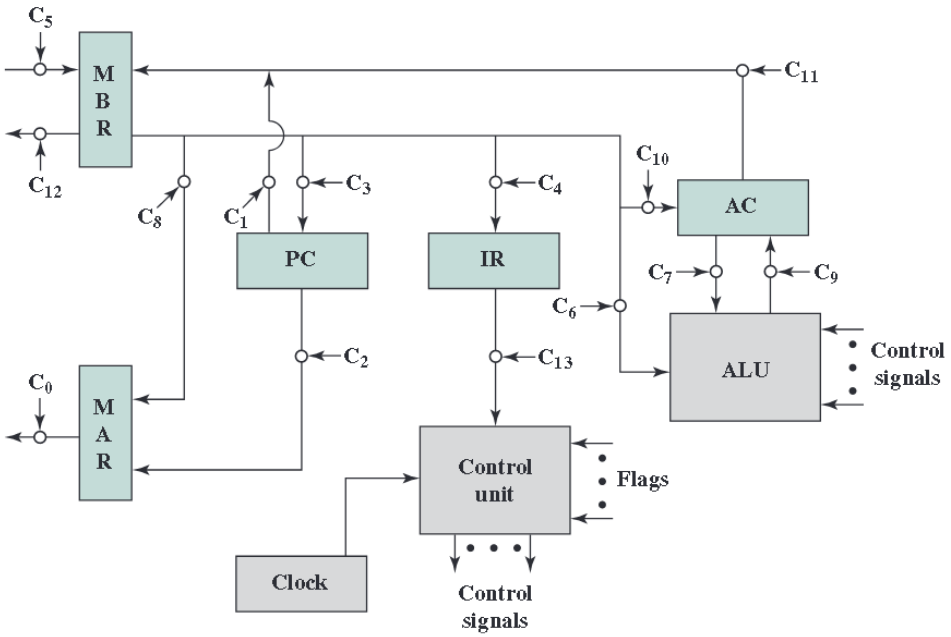


Figure 20.5 Data Paths and Control Signals

间址时，IR到MAR没有直接的通路，用的是MBR

内部总线结构为什么需要引入Y和Z寄存器：Y是输入时若有两个操作数，用Y更加灵活；Z是不能直接把ALU计算结果输出到总线上

Chapter 21

水平/垂直微指令特点与差别

下图的执行流程4步

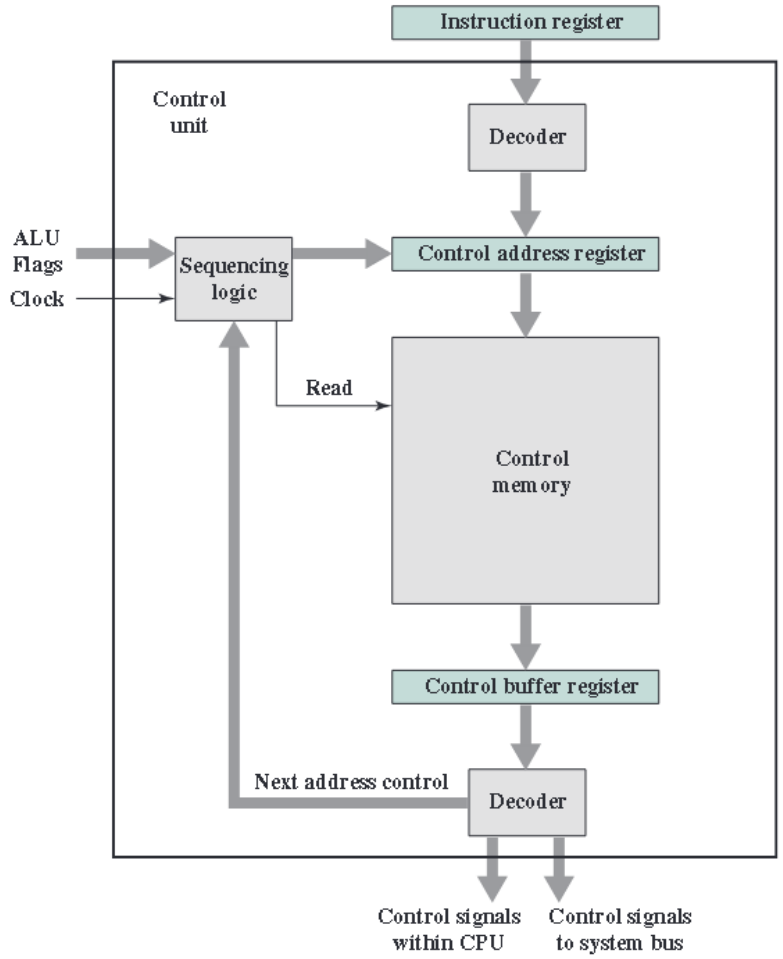


Figure 21.4 Functioning of Microprogrammed Control Unit

两个decoder的区别

sequencing 设计时要考虑的2点因素

3种不同的排序方式（按照地址数划分）尤其是变长地址格式的概念以及优点

packing/unpack 概念

horizontal/vertical 概念

hard/ soft 概念

encoding techniques 两种