1. **Counter.v**

**module Counter( dout, clk, rst, en, up ) ;**

**parameter WIDTH = 8 ;**

**input clk, rst, en, up ;**

**output reg[WIDTH-1:0] dout ;**

**always@( posedge clk )begin**

**if ( rst == 0 )begin**

**dout <= 8'd0 ;**

**end**

**else if ( en == 1 )begin**

**if ( up == 1 )begin**

**if ( dout != 8'hff ) dout <= dout + 1 ;**

**end**

**else begin**

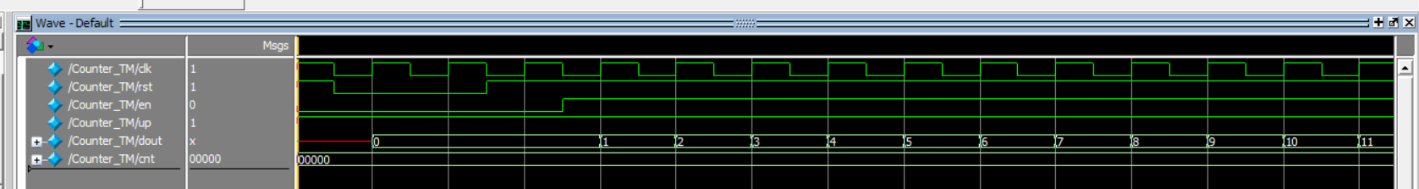
**if ( dout != 8'd0 ) dout <= dout - 1 ;**

**end**

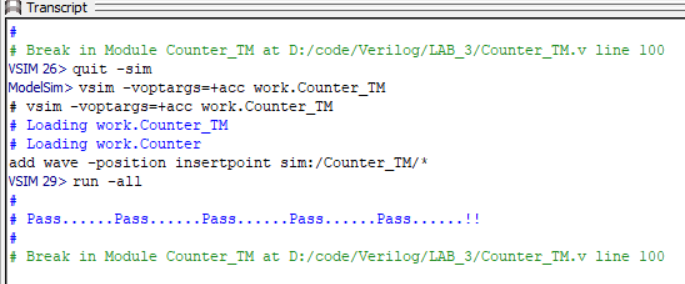
**end**

**end**

**endmodule**

**WaveForm:**

看dout那條，在一開始rst=0時 會等到clk=1時才同步設0



**心得:本次實驗讓我對於verilog的同步語法有更深的了解，也讓我知道同步與非同步的差別。**