National Yang Ming Chiao Tung University
Department of Electrical Engineering
Physical Design Automation, Fall 2023

November 29, 2023
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Programming Assignment #3

Euler Path in Standard Cells

1 Problem Description

In advanced nanometer technology nodes, standard cells are designed with FinFETs, which have a promising substitute compared with the traditional planar MOSFETs, due to its extraordinary properties such as improved channel controllability, high ON/OFF current ratio, reduced short-channel effects, and relative immunity to gate line-edge roughness. In this programming assignment, you are asked to find a common optimal Euler path for both PMOS and NMOS networks in a CMOS digital logic gate which maximize sdiffusion sharing for standard cell layout generation while minimizing total half-perimeter wire length (HPWL) in each standard cell.

2 Input Format

The input of your program is the SPICE netlist describing the CMOS FinFET network of a digital logic gate. An example SPICE format is given below.

- **Explanation of the Input:**
  - **The first line gives the circuit name and the inputs/outputs**
  - **The rest lines describe the instance name of each NMOS/PMOS and its interconnections, which starts with the instance name, followed by the net names connected to the drain, gate, source, and substrate of the transistor, MOS type (PMOS or NMOS), channel width, channel length, and fin number.**

- **Design Rules:**
  - **GATE.W.1: The horizontal GATE width must be 20nm.**
  - **GATE.W.2: The vertical GATE width must be larger than 40nm.**
  - **GATE.S.1: The horizontal GATE pitch must be 54nm.**
  - **GATE.S.2: The GATE spacing must be 34nm.**
  - **GATE.ACTIVE.EX.1: The vertical extension of GATE past ACTIVE must be larger than 4nm.**
  - **GATE.ACTIVE.EX.2: The horizontal extension of ACTIVE interacting with GATE past GATE must be 25nm.**

```
.SUBCKT NOR2 A B VDD VSS Y
MM2  Y A VSS VSS nmos_rvt w=81.0n l=20n nfin=3
MM1  Y B VSS VSS nmos_rvt w=81.0n l=20n nfin=3
MM4  Y B net1 VDD pmos_rvt w=162.00n l=20n nfin=6
MM3  net1 A VDD VDD pmos_rvt w=162.00n l=20n nfin=6
.ENDS
```

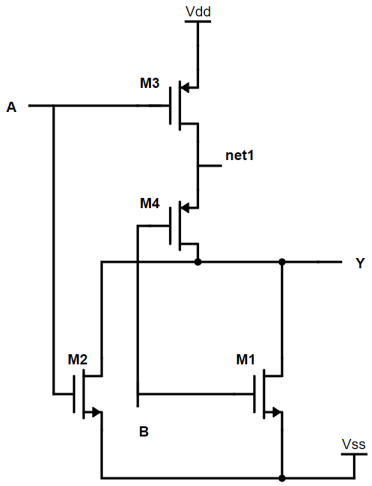


Figure 1: The SPICE netlist of a 2-input NOR gate, and its corresponding schematic.

- **GATE.ACTIVE.AUX.3: ACTIVE layer vertical edge may not lie inside, or coincide with, the GATE layer.**
- **ACTIVE.W.1: The vertical width of ACTIVE must be larger than 27nm.**
- **ACTIVE.W.2: ACTIVE layer vertical width increment is an integer multiple of 27nm.**
- **ACTIVE.W.3: The horizontal width of ACTIVE must larger than 16nm.**
- **ACTIVE.S.1: The vertical spacing of ACTIVE must be 27nm.**

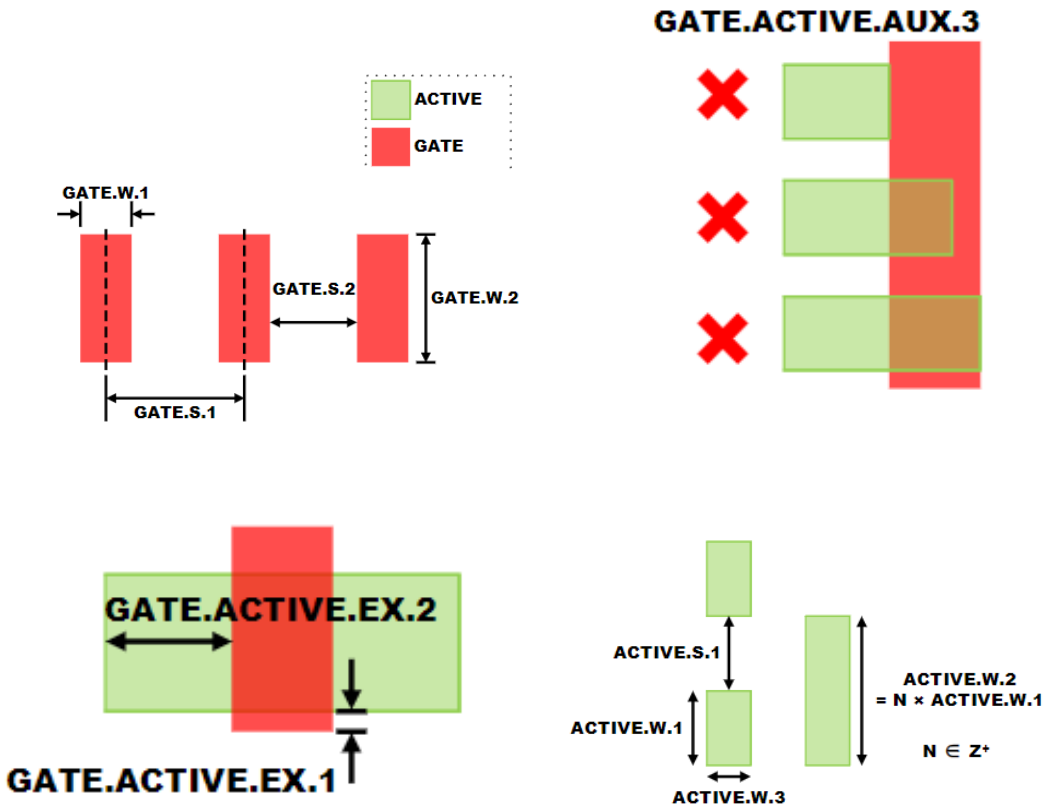
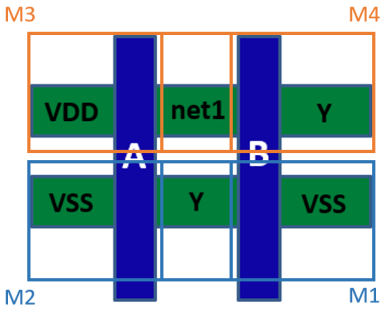


Figure 2: Illustration of design rules

3 Output Format

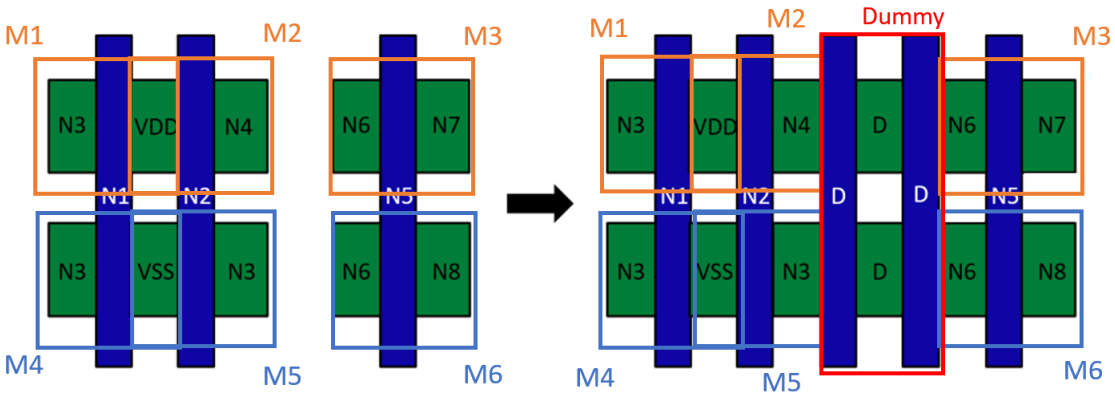



```
297                 //HPWL
M3 M4               //pmos instances
VDD A net1 B Y      //pmos pins
M2 M1               //nmos instances
VSS A Y B VSS       //nmos pins
```

Figure 3: The resulting stick diagram with the Euler paths VDD–A–net1–B–Y and VSS–A–Y–B–VSS, in PMOS and NMOS networks, respectively, and the corresponding output.

- **Explanation of the Output:**
  - **The first line gives the total HPWL of all nets in the SPICE netlist.**
  - **The second and third lines shows the Euler path of the PMOS network in terms of instance names and net names, respectively.**
  - **The fourth and fifth lines shows the Euler path of the NMOS network in terms of instance names and net names, respectively.**

- **You may add extra dummy transistors if you cannot find any Euler path in the original netlist or if adding dummy transistors can help reduce total HPWL. The figure below gives an example with dummy transistors.**
- **Active can only be separated vertically, not horizontally. ACTIVE.S.1 refers to the distance between vertically separated Active. Only one PMOS/NMOS Euler path is allowed.**




```
3210                                    //HPWL
M1 M2 Dummy M3                          //pmos instances
N3 N1 VDD N2 N4 Dummy N6 N5 N7          //pmos pins
M4 M5 Dummy M6                          //nmos instances
N3 N1 VSS N2 N3 Dummy N6 N5 N8          //nmos pins
```

Figure 4: An example output with dummy transistors in the Euler paths.

4 Grading Policy

We will use HPWL and runtime to evaluate and rank your results.

- Calculation of HPWL:
  - Take NOR2 as an example, $HPWL = VDD_w + VDD_h + VSS_w + VSS_h + Y_w + Y_h + net1_w + net1_h$
  - For the layout on the left side of the figure below and the NOR2 netlist, $HPWL = (0)_{VDD_w} + (0)_{VDD_h} + (25 \cdot 0.5 + 20 + 34 + 20 + 25 \cdot 0.5)_{Vss_w} + (0)_{Vss_h} + (34 \cdot 0.5 + 20 + 25 \cdot 0.5)_{Y_w} + (162 \cdot 0.5 + 27 + 81 \cdot 0.5)_{Y_h} + (0)_{net1_w} + (0)_{net1_h} = 297$
  - For the layout on the right side of the figure below and the NOR2 netlist, $HPWL = (0)_{VDD_w} + (0)_{VDD_h} + (25 \cdot 0.5 + 20 + 34 + 20 + 34 + 20 + 34 + 20 + 25 \cdot 0.5)_{Vss_w} + (0)_{Vss_h} + (34 \cdot 0.5 + 20 + 34 + 20 + 34 + 20 + 34 + 20 + 25 \cdot 0.5)_{Y_w} + (162 \cdot 0.5 + 27 + 81 \cdot 0.5)_{Y_h} + ((34 \cdot 0.5 + 20 + 34 + 20 + 34 \cdot 0.5)_{net1_w} + (0)_{net1_h} = 621$

$$CostFuntion = HPWL * Runtime$$

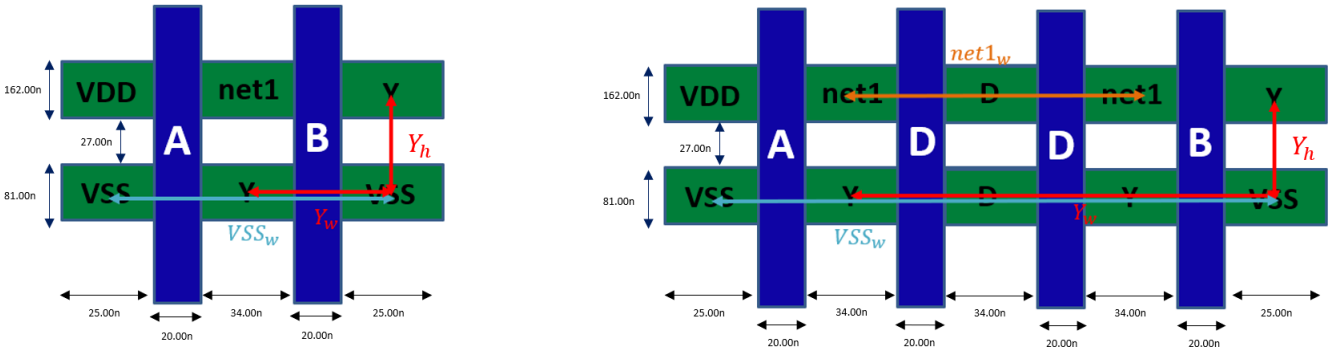


Figure 5: HPWL calculation.

5 Submission

You need to submit the following in a "tar" file to E3 (https://e3.nycu.edu.tw/) by the deadline. Please put all required files in a folder: (1) source codes, (2) Makefile, (3) a text readme file (readme.txt) stating how to build and use your program. The folder name must be your student ID. Be sure to compress the folder in the linux environment with the following command.

tar cvf Student_ID.tar Student_ID

In order to test your program, you are asked to add the following command-line parameters to your program :

./Lab3 [input file name] [output file name]

This programming assignment will be graded based on (1) the correctness, (2) solution quality, and (3) running time. For each case, the runtime limit is 1 hours. It will be regarded as "failed" for the case if it takes more than 1 hours. During the program execution process, do not print any messages or text; otherwise, there will be a penalty. There will be 25% penalty per day for late submission.