Introduction to CMOS VLSI Design

Lecture 4: DC & Transient Response

Outline

- ❑ DC Response
- ❑ Logic Levels and Noise Margins
- ❑ Transient Response
- ❑ Delay Estimation

Activity

1) If the width of a transistor increases, the current will

increase   decrease   not change

2) If the length of a transistor increases, the current will

increase   decrease   not change

3) If the supply voltage of a chip increases, the maximum transistor current will

increase   decrease   not change

4) If the width of a transistor increases, its gate capacitance will

increase   decrease   not change

5) If the length of a transistor increases, its gate capacitance will

increase   decrease   not change

6) If the supply voltage of a chip increases, the gate capacitance of each transistor will

increase   decrease   not change

Activity

1) If the width of a transistor increases, the current will

increase   decrease   not change

2) If the length of a transistor increases, the current will

increase   **decrease**   not change

3) If the supply voltage of a chip increases, the maximum transistor current will

increase   decrease   not change

4) If the width of a transistor increases, its gate capacitance will

increase   decrease   not change

5) If the length of a transistor increases, its gate capacitance will

increase   decrease   not change

6) If the supply voltage of a chip increases, the gate capacitance of each transistor will

increase   decrease   **not change**

2長度越長 電阻越大 電流越小
3供給電壓
4電晶體越長 越寬 電容也就越長 越大

DC Response

- ❑ DC Response: V_{out} vs. V_{in} for a gate
- ❑ Ex: Inverter
  - When $V_{in} = 0$ -> $V_{out} = V_{DD}$
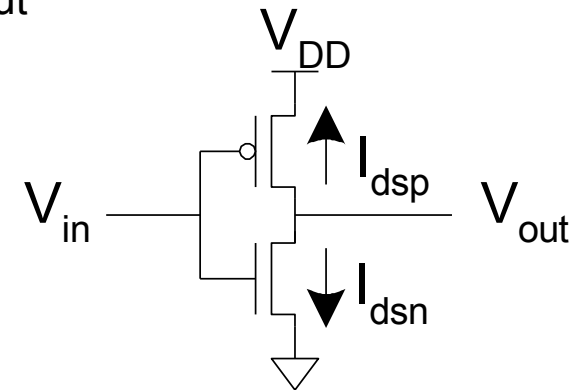 - When $V_{in} = V_{DD}$ -> $V_{out} = 0$
  - In between, V_{out} depends on transistor size and current
  - By KCL, must settle such that $I_{dsn} = |I_{dsp}|$
  - We could solve equations
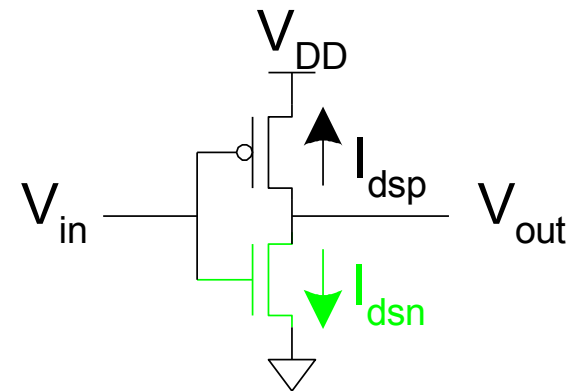 - But graphical solution gives more insight

輸出 取決於
電晶體的大小 和 電流

Transistor Operation

❑ Current depends on region of transistor behavior

❑ For what V_{in} and V_{out} are nMOS and pMOS in

- Cutoff?

- Linear?

- Saturation?

nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} <$	$V_{gsn} >$ $V_{dsn} <$	$V_{gsn} >$ $V_{dsn} >$

nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
這裡是要走下面的狀況 1導通	$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$

nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$

$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$
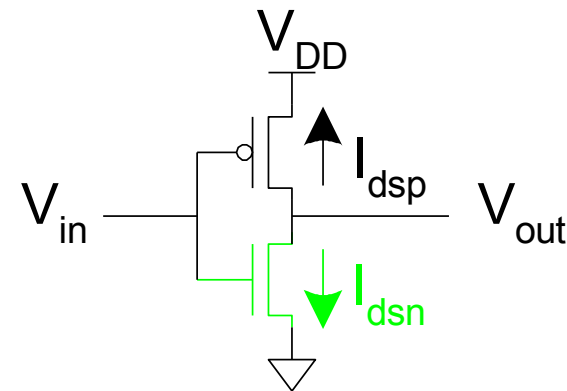
nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$

$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$
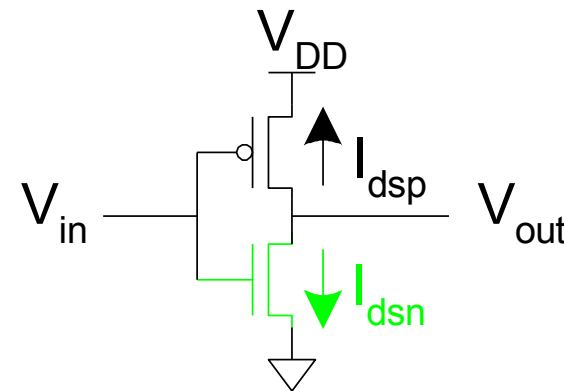
pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} >$	$V_{gsp} <$ $V_{dsp} >$	$V_{gsp} <$ $V_{dsp} <$
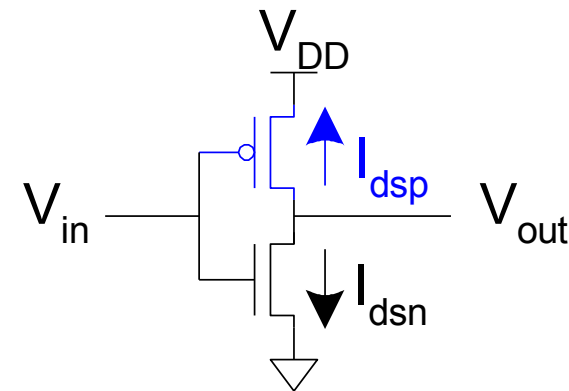
pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$
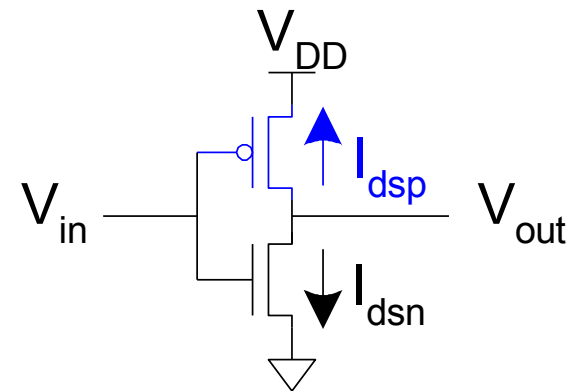
pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
	$V_{dsp} > V_{gsp} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$

$V_{gsp} = V_{in} - V_{DD}$ $V_{tp} < 0$

$V_{dsp} = V_{out} - V_{DD}$

pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
$V_{in} > V_{DD} + V_{tp}$	$V_{in} < V_{DD} + V_{tp}$	$V_{in} < V_{DD} + V_{tp}$
這裡是要走上面的狀況 Pmos 0導通	$V_{dsp} > V_{gsp} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$
	$V_{out} > V_{in} - V_{tp}$	$V_{out} < V_{in} - V_{tp}$

$V_{gsp} = V_{in} - V_{DD}$

$V_{dsp} = V_{out} - V_{DD}$

$V_{tp} < 0$
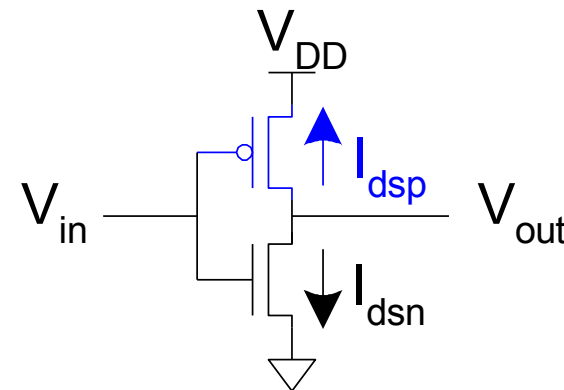
I-V Characteristics

❑ Make pMOS is wider than nMOS such that $\beta_n = \beta_p$

會希望 電流的放電 充電 斜率是一樣的

可以把這裡想像成電阻

可以把這裡想像成電容

$\beta = \mu C_{ox} \dfrac{W}{L}$

$\beta_n = \mu_n C_{ox} \dfrac{W}{L}$

$\beta_p = \mu_p C_{ox} \dfrac{W}{L}$

VDD

W/L

I/O

$\beta = \mu C_{ox} \dfrac{W}{L}$

$\mu_n = 2\sim 3\ \mu_p$ (2)

$\beta_n = \mu_n C_{ox} \dfrac{W}{L}$

$\beta_p = \mu_p C_{ox} \dfrac{②W}{L}$
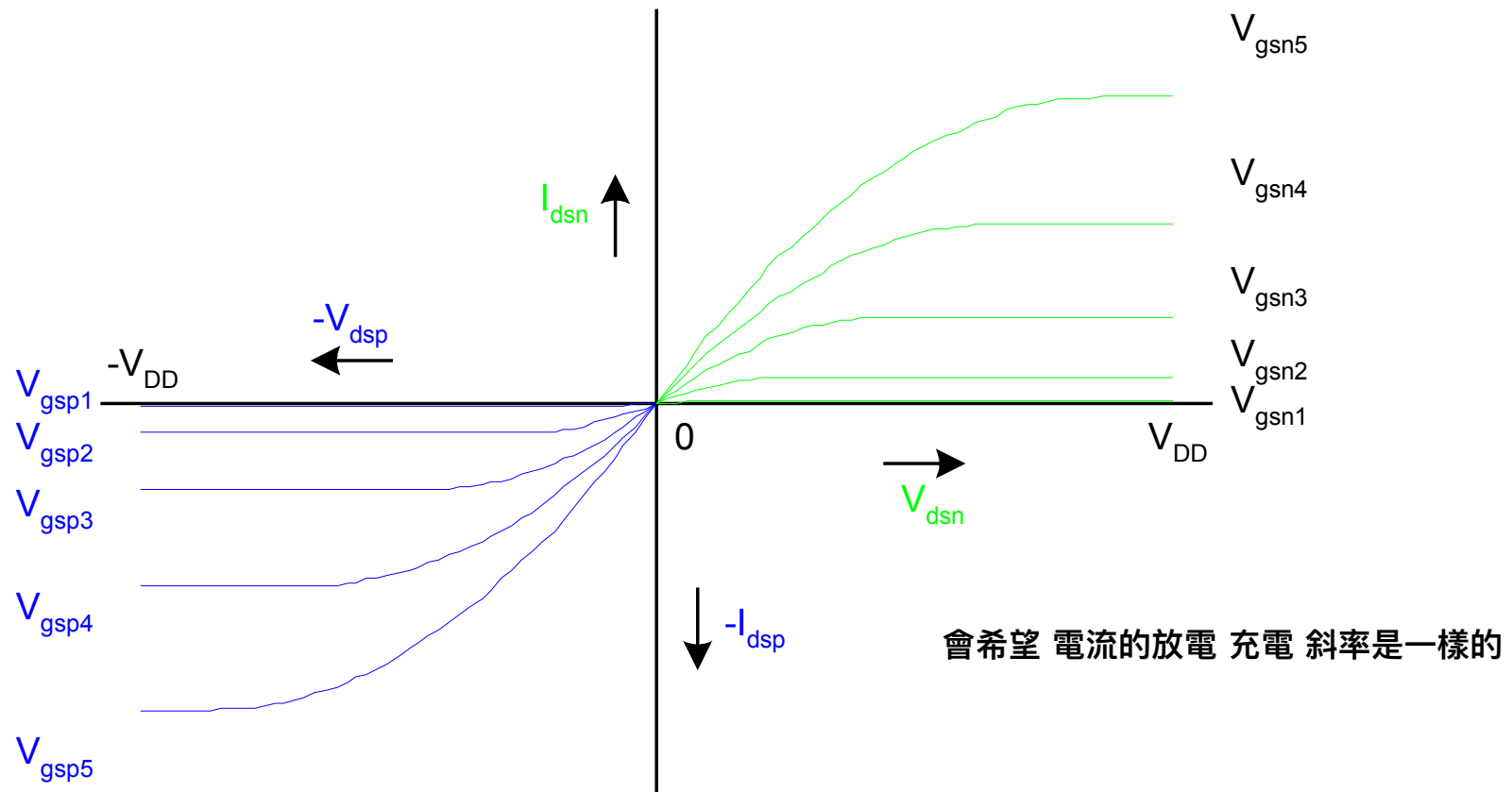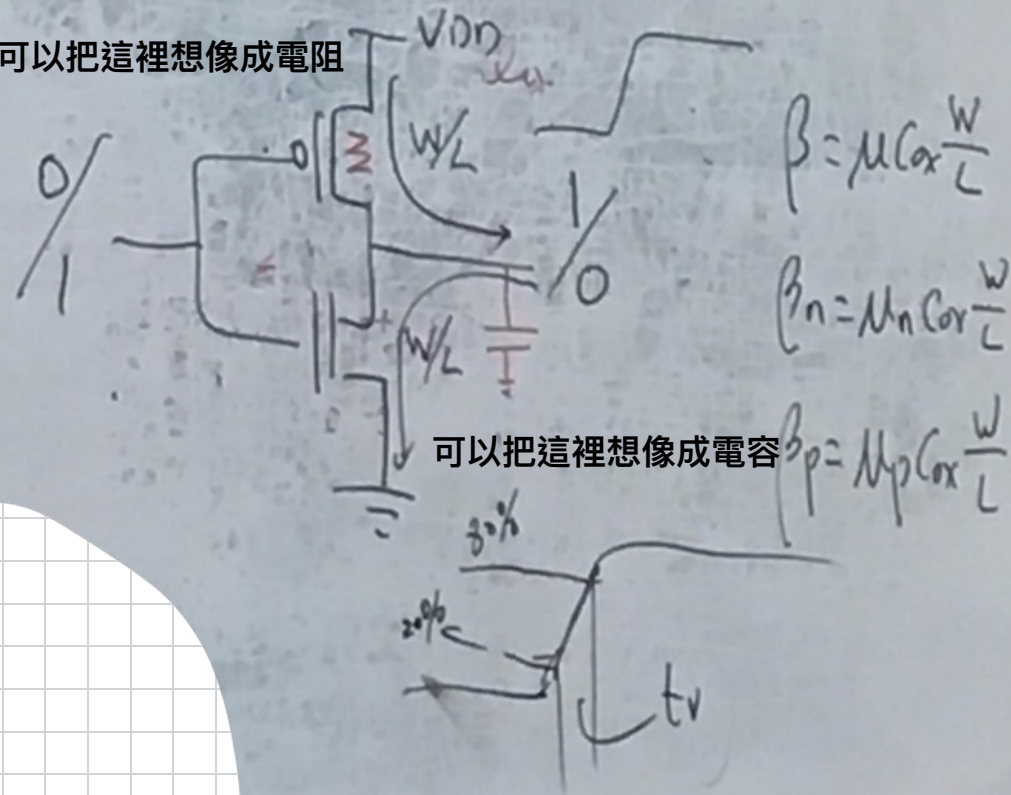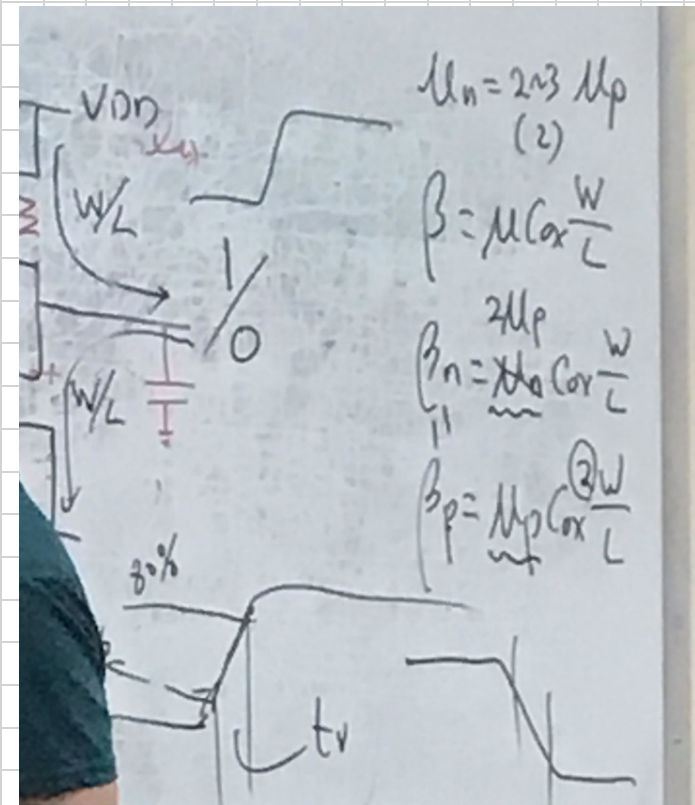
Beta 當作 導電係數

如果斜率不一樣 就會有延遲 會不好決定收取時間
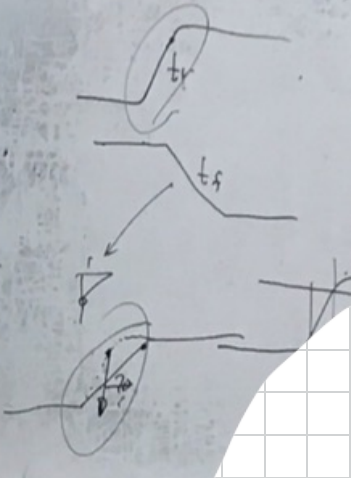
Current vs. V_{out}, V_{in}
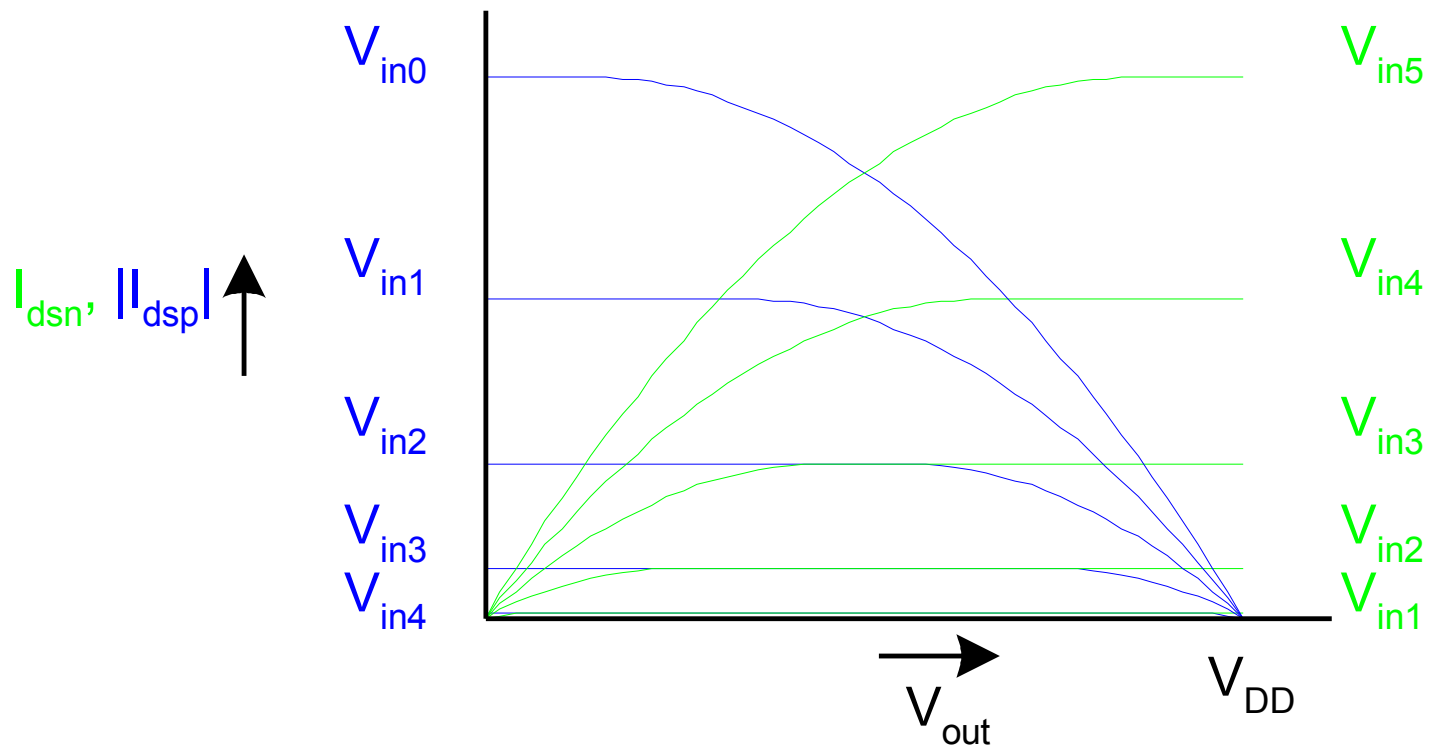
Load Line Analysis

❑ For a given V_{in}:
  – Plot I_{dsn}, I_{dsp} vs. V_{out}
  – V_{out} must be where |currents| are equal in

要藍綠 兩線
相同值的時候
就是輸出的電壓
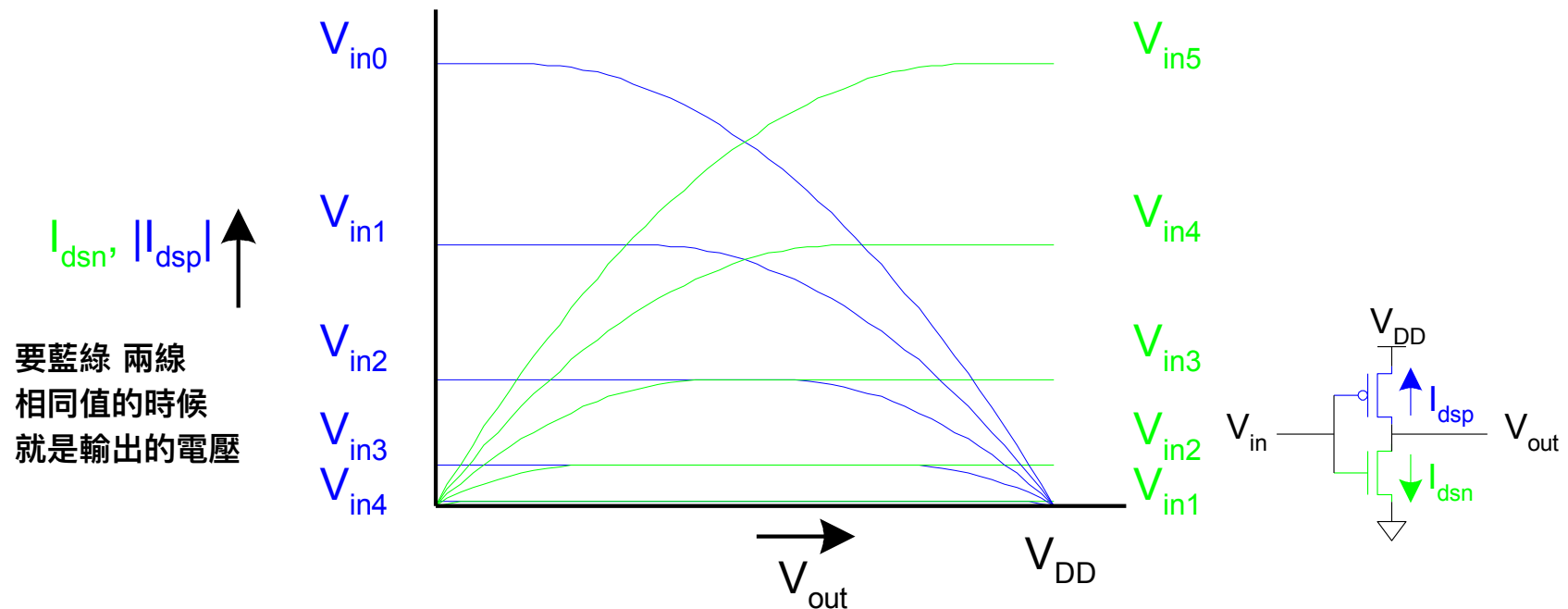
Load Line Analysis
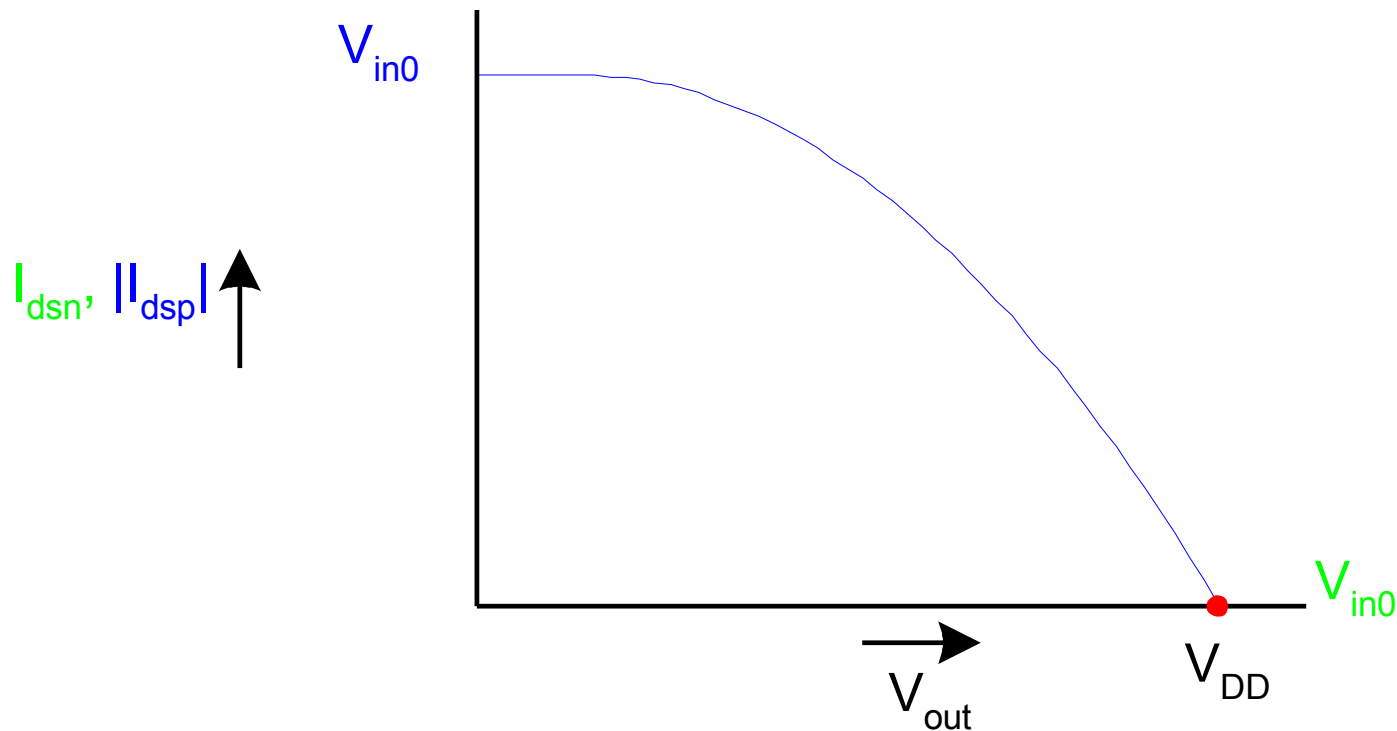
❏ $V_{in} = 0$

Load Line Analysis
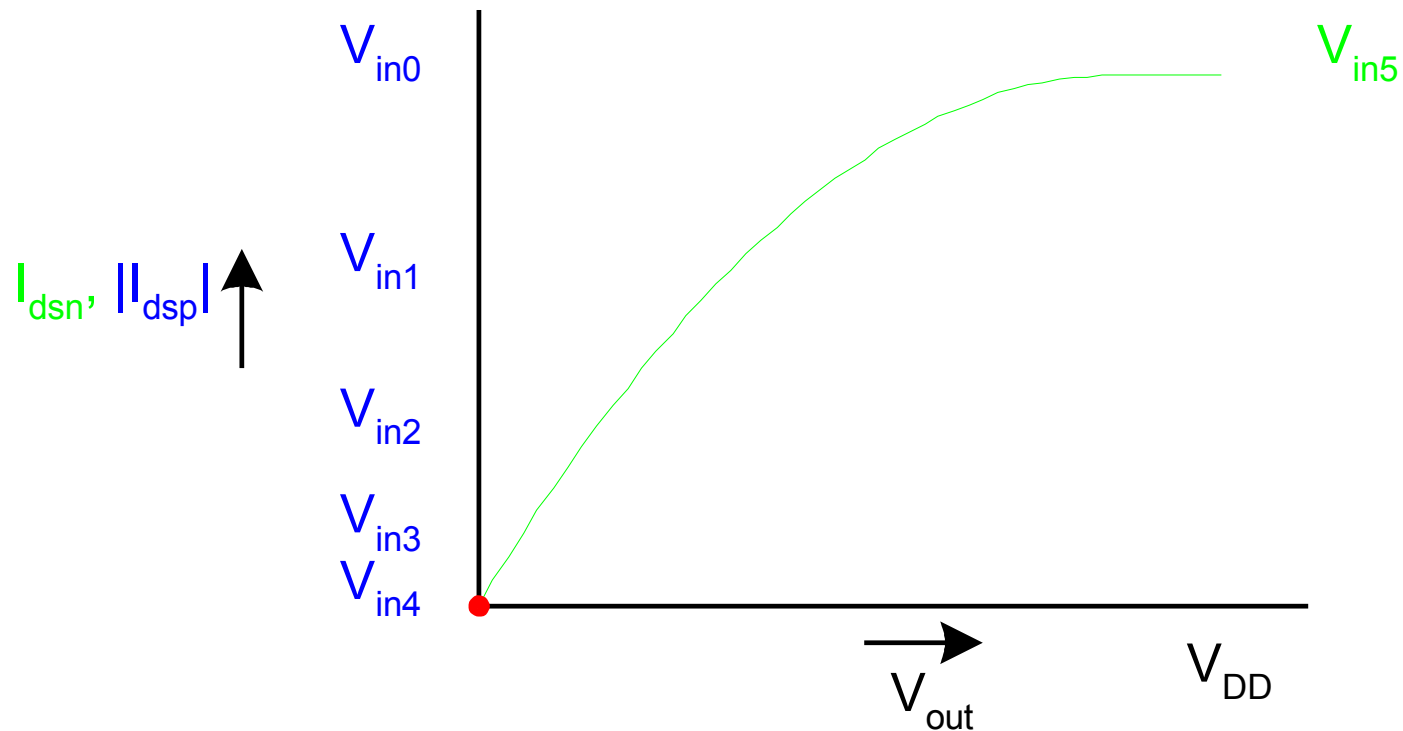
- $V_{in} = 0.2 V_{DD}$
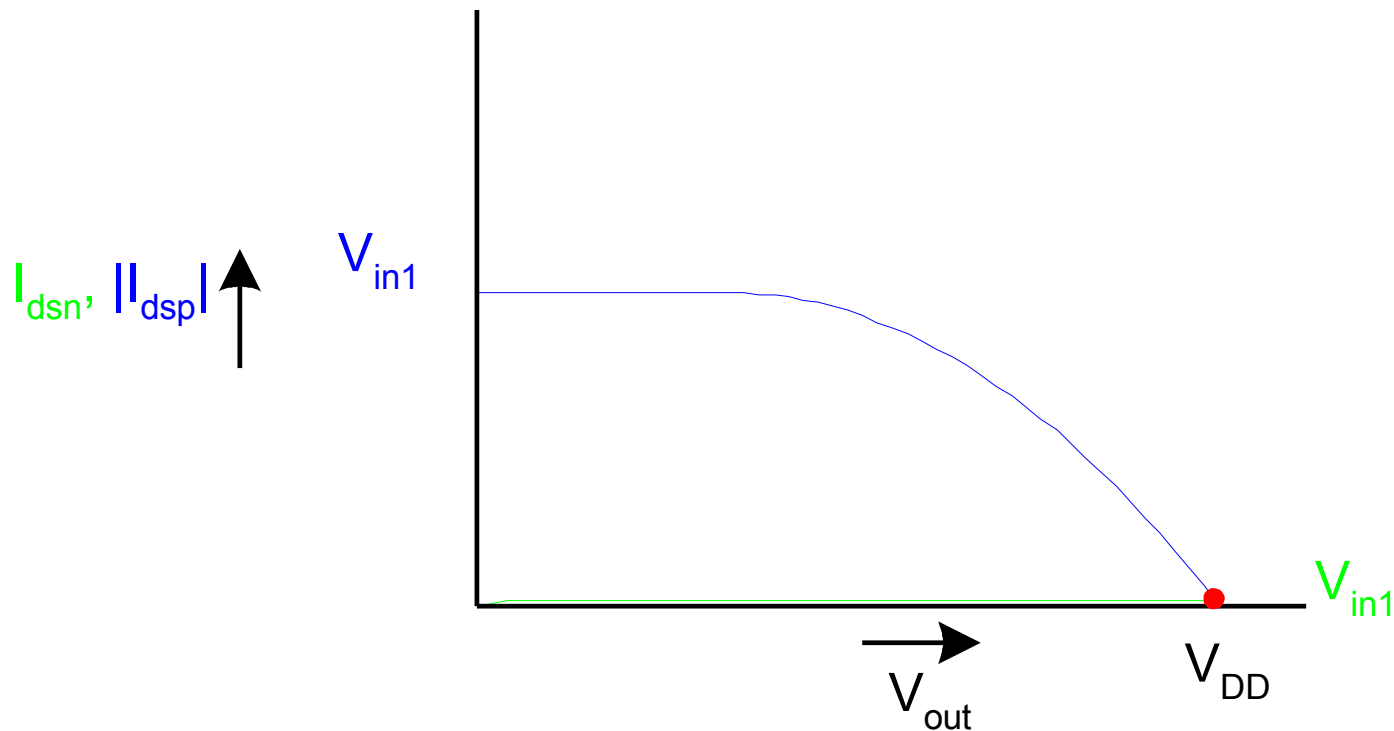
Load Line Analysis

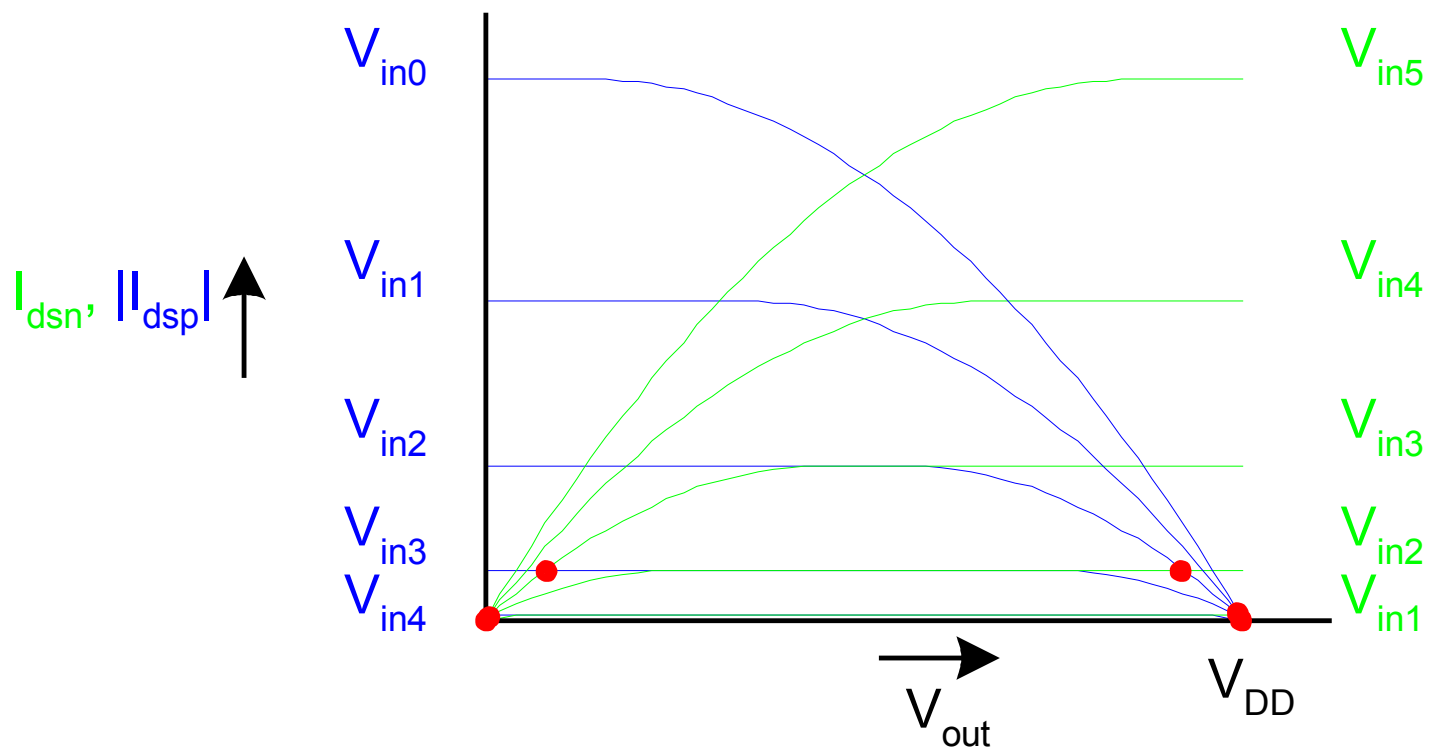❑ $V_{in} = 0.4V_{DD}$
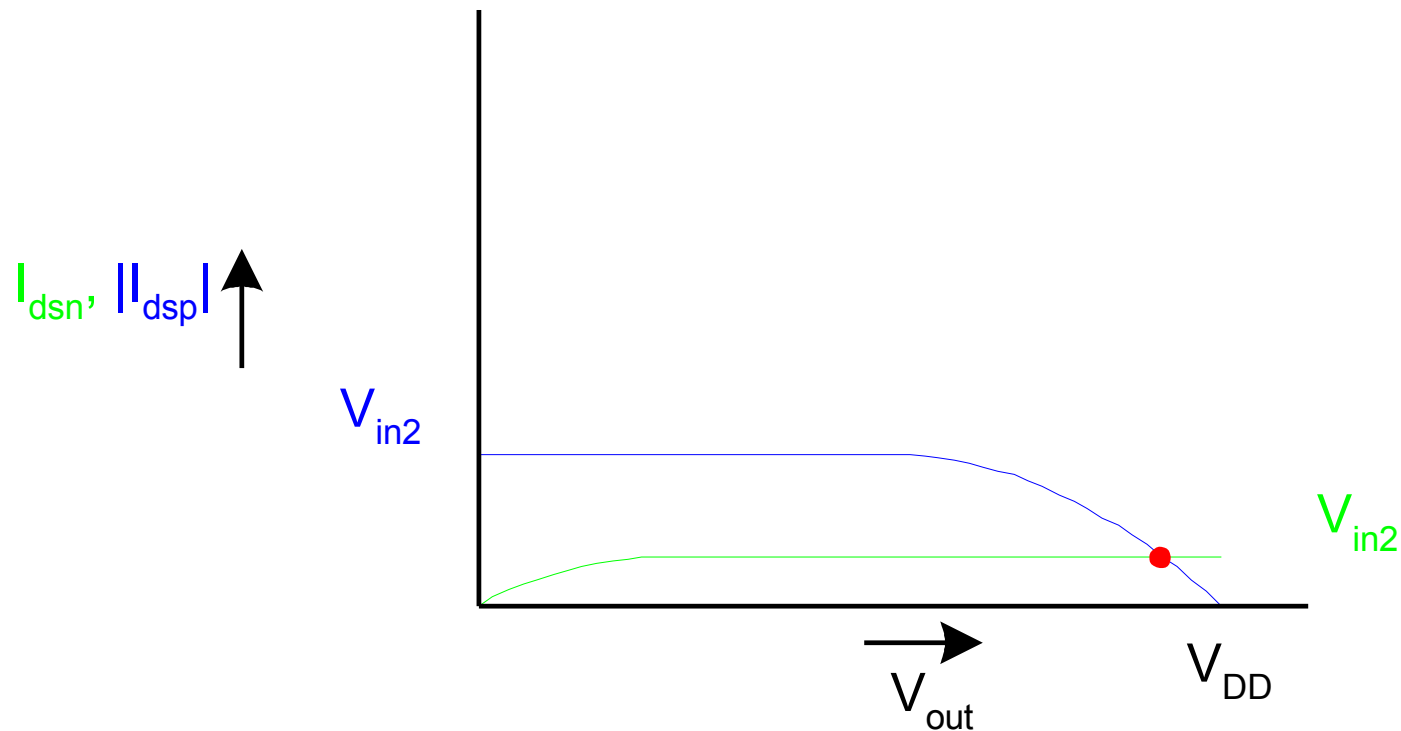
Load Line Analysis

❑ $V_{in} = 0.6V_{DD}$
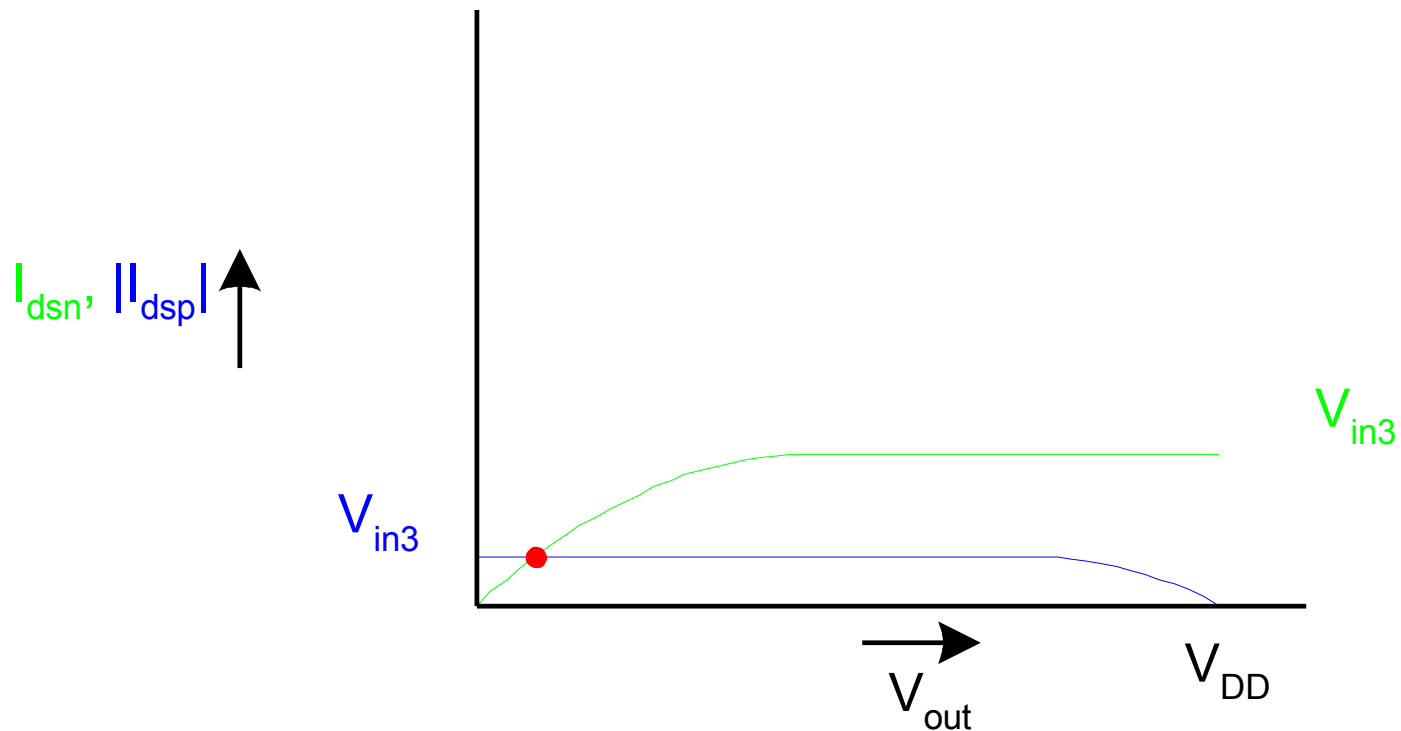
Load Line Analysis

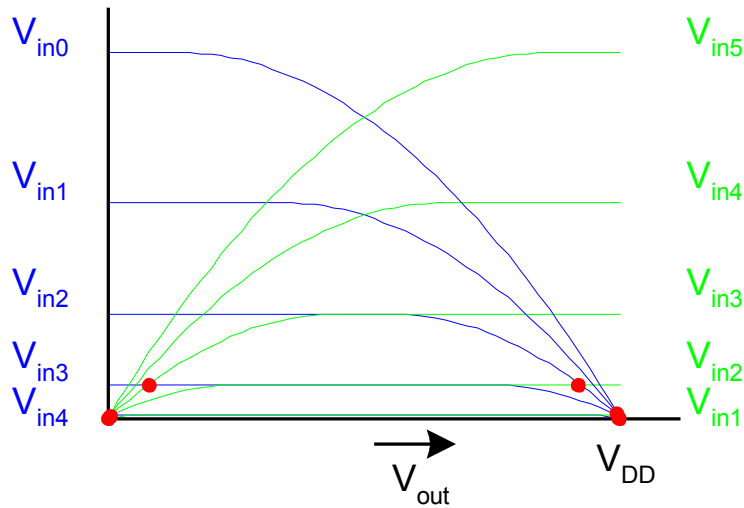- $V_{in} = 0.8V_{DD}$
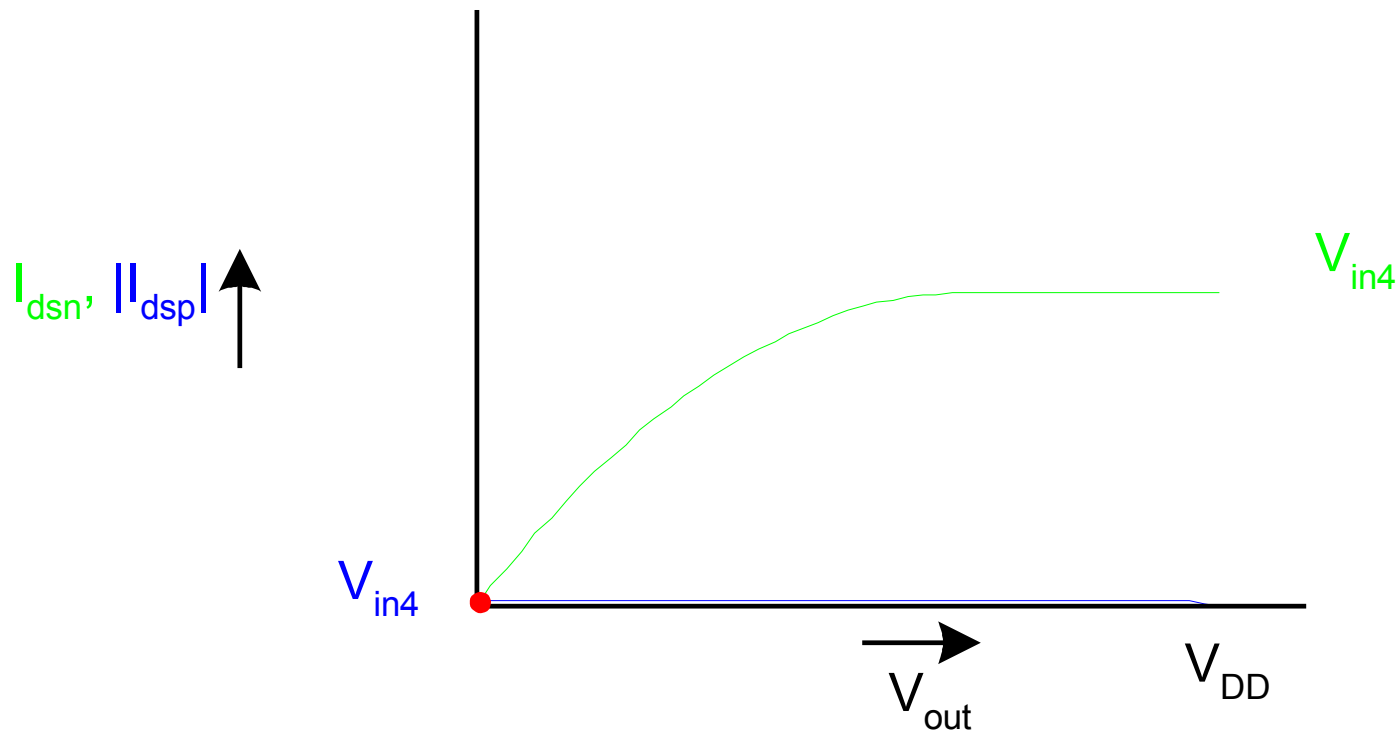
Load Line Analysis

□ $V_{in} = V_{DD}$

Load Line Summary

DC Transfer Curve
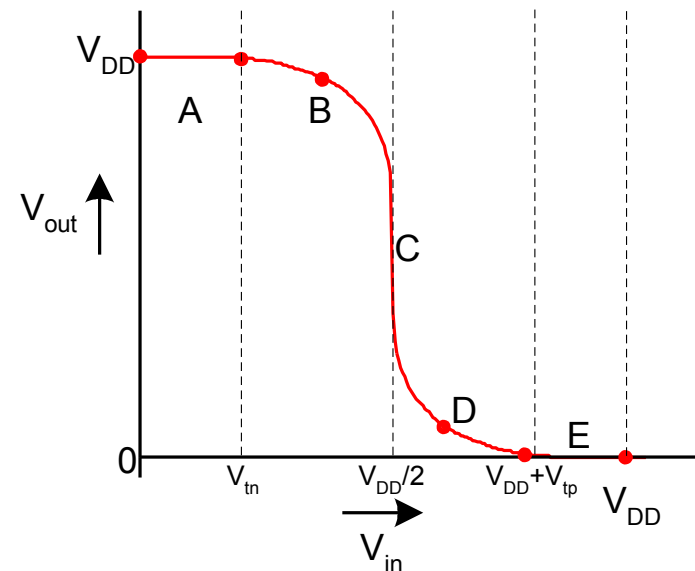
❑ Transcribe points onto V_{in} vs. V_{out} plot
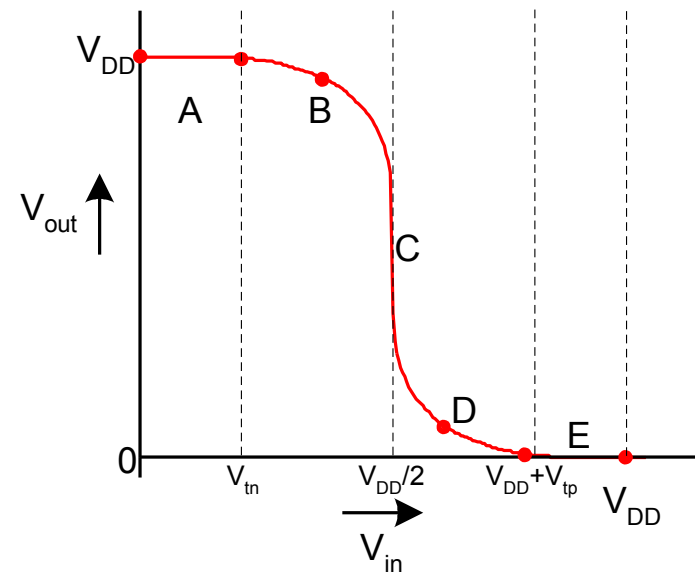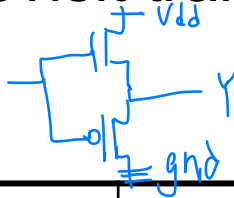

因為這是一個not 所以輸出越高 就會越接近0

Operating Regions

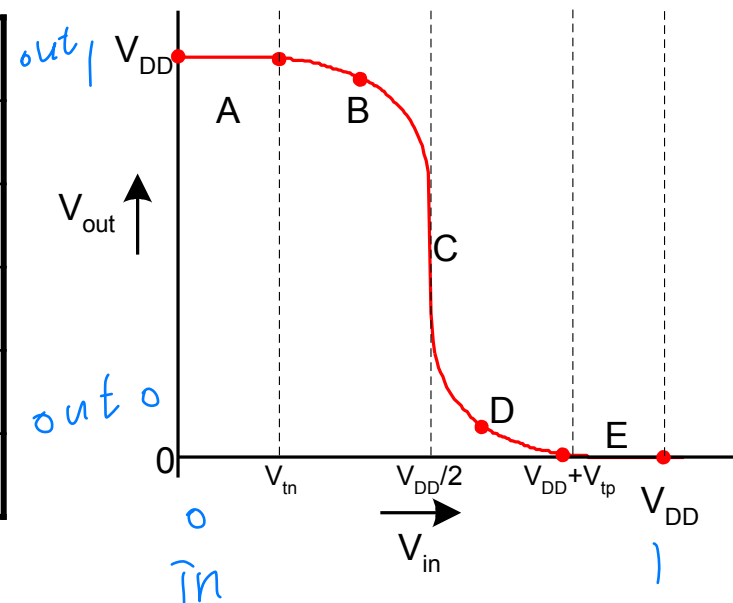❑ Revisit transistor operating regions

Region	nMOS	pMOS
A		
B		
C		
D		
E		

Operating Regions

❑ Revisit transistor operating regions

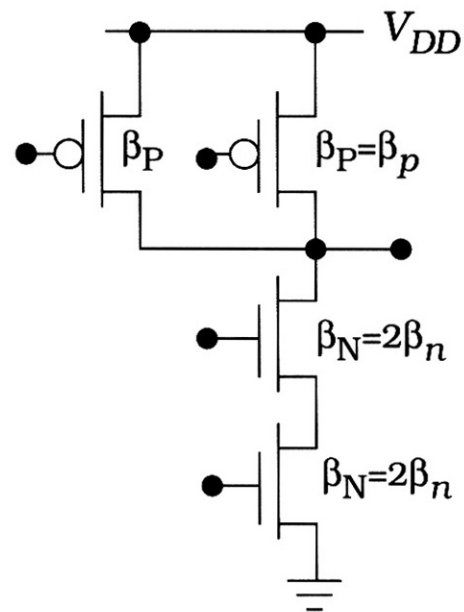| Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff

Beta Ratio

❑ If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$

❑ Called *skewed* gate
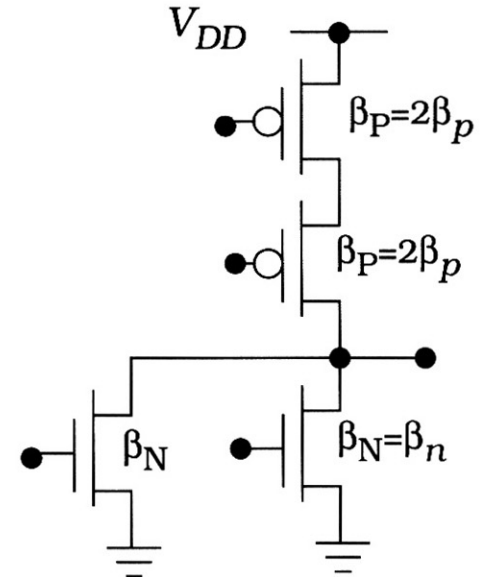
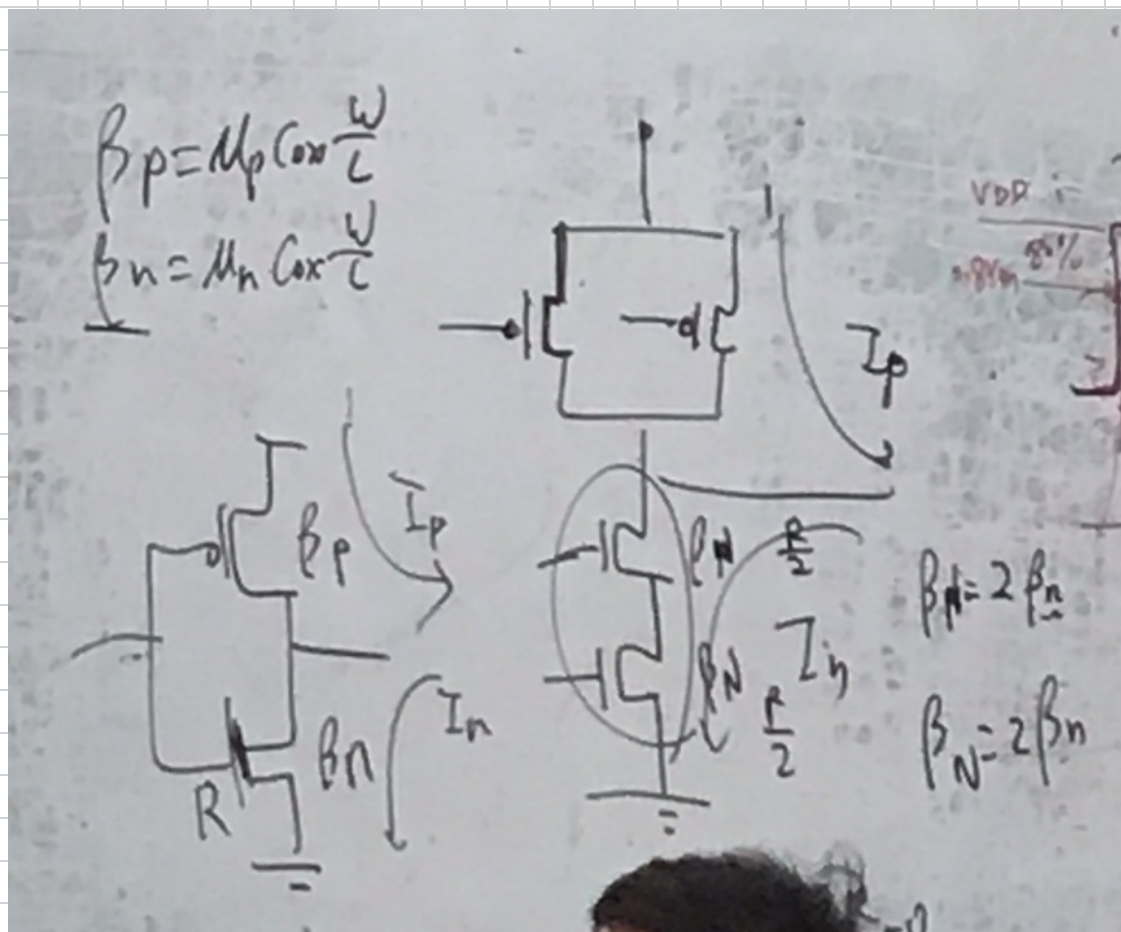❑ Other gates: collapse into equivalent inverter
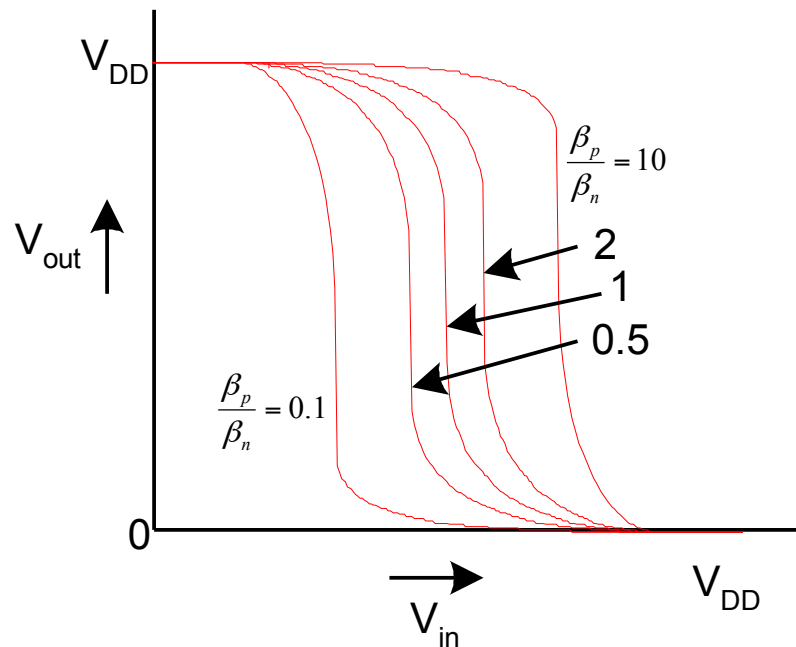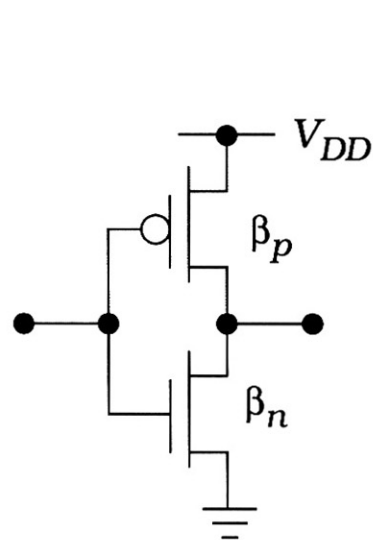
(a) Inverter   (b) NAND2   (c) NOR2
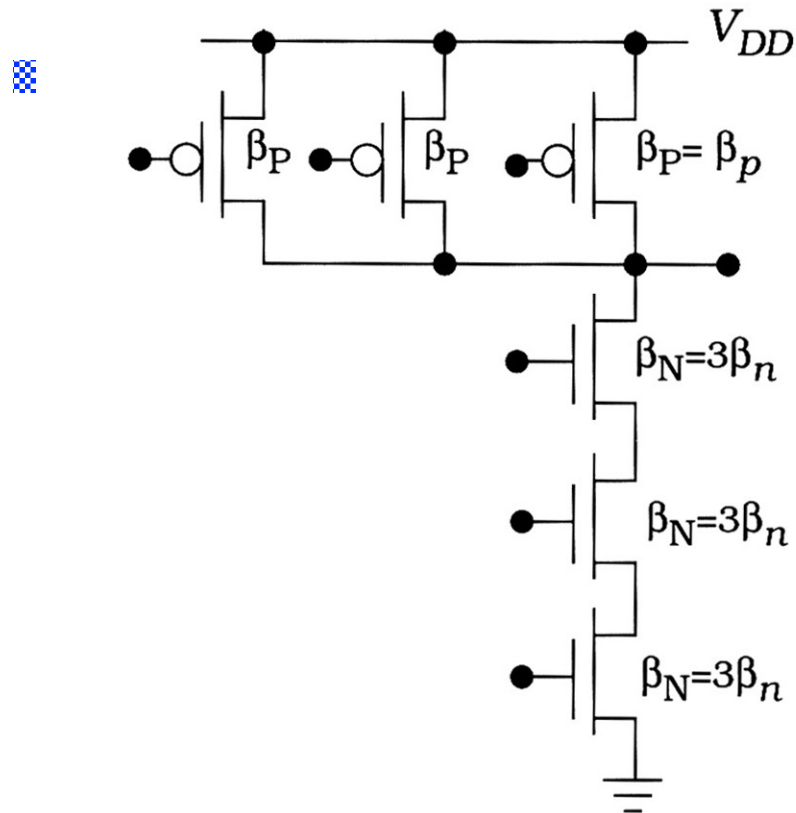
Figure 7.34 Relative FET sizing

$$\beta_p = \mu_p C_{ox} \frac{W}{L}$$

$$\beta_n = \mu_n C_{ox} \frac{W}{L}$$

$$\beta_N = 2\beta_n$$
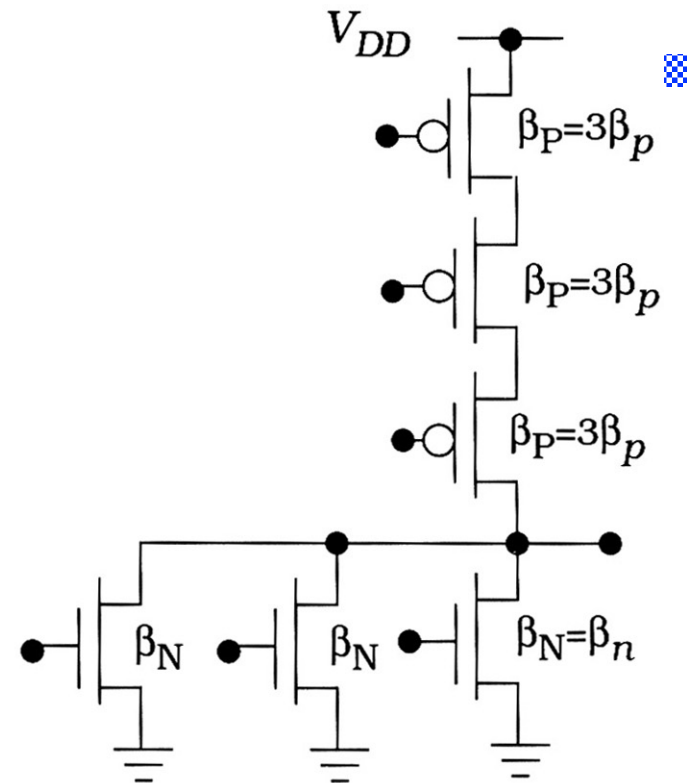
$$\beta_N = 2\beta_n$$

這裡是調整w 寬度 來 控制電阻

因為電阻 都要和原本的 not 的 電阻 一樣

因為 串連 電阻會加起來
所以串連的電阻 都要變成 R/2

$$\beta = \mu C_{ox} \frac{W}{L} \quad \Leftarrow W \text{ 在串需增寬}$$

(a) NAND3

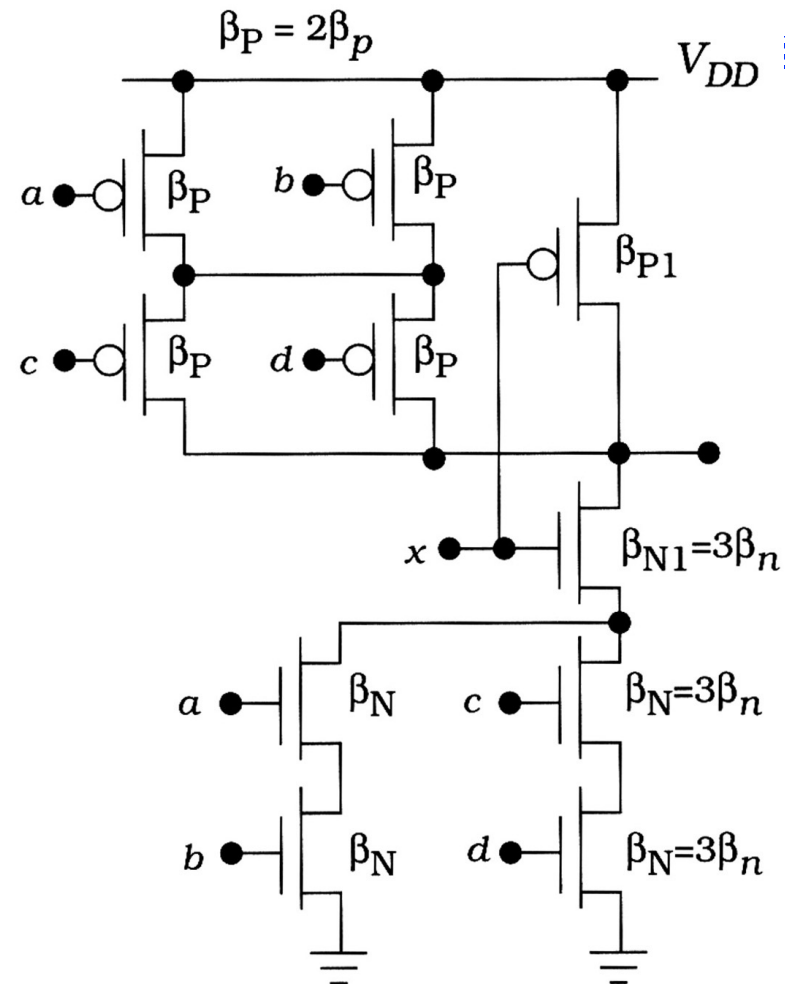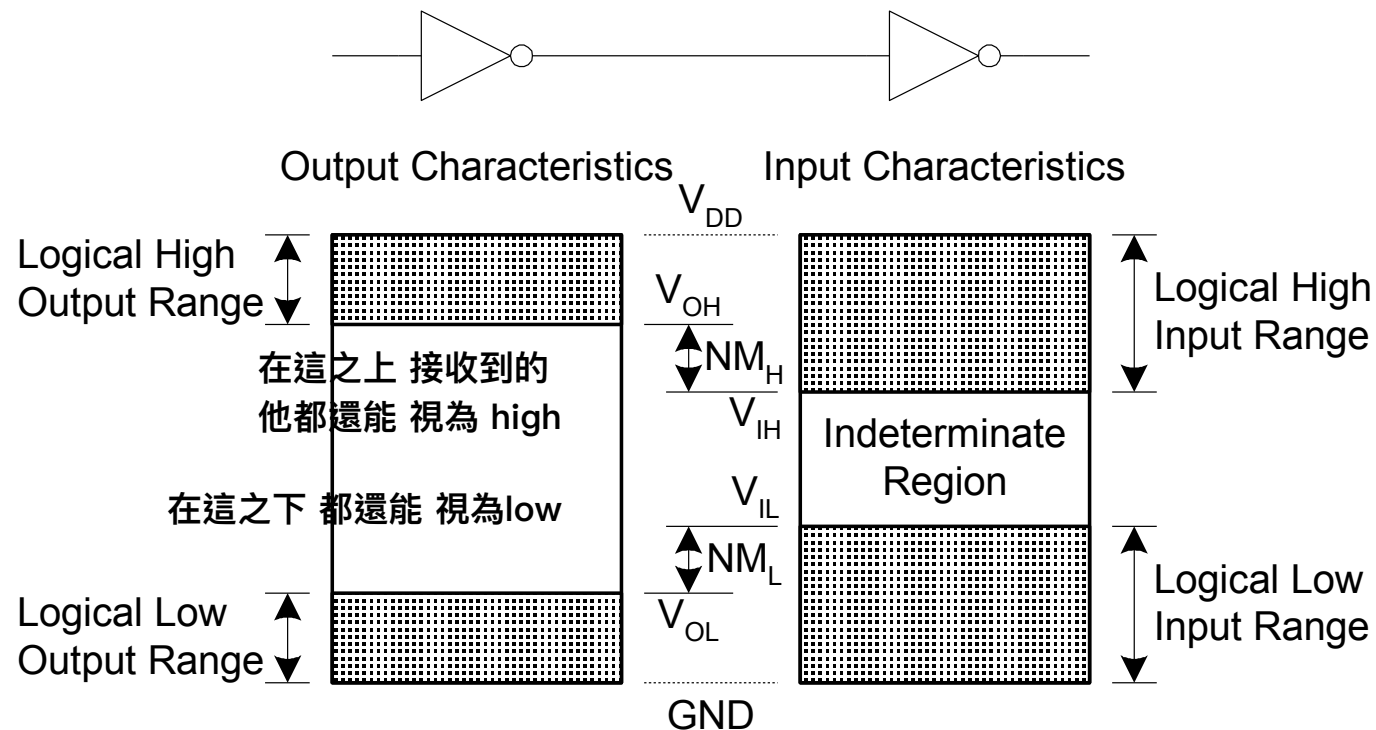(b) NOR3

Figure 7.35 Sizing for 3-input gates

Figure 7.36 Sizing of a complex logic gate

Noise Margins

❑ How much noise can a gate input see before it does not recognize the input?

Output Characteristics | Input Characteristics

Logical High Output Range

在這之上 接收到的

他都還能 視為 high

在這之下 都還能 視為low

Logical Low Output Range

V_{DD}

V_{OH}

NM_H

V_{IH}

V_{IL}

NM_L

V_{OL}

GND

Logical High Input Range
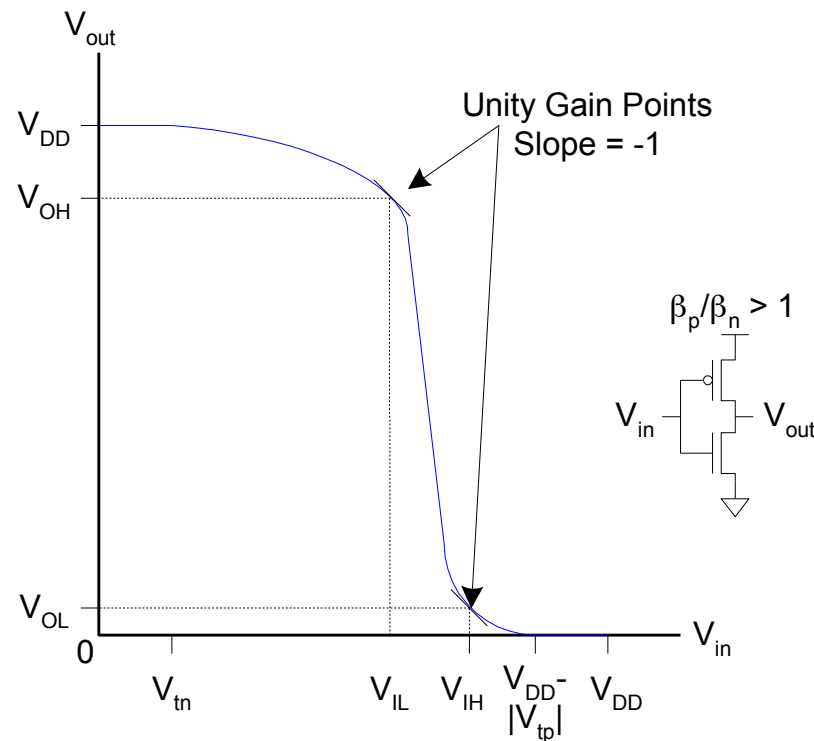
Indeterminate Region

Logical Low Input Range

Logic Levels

❑ To maximize noise margins, select logic levels at
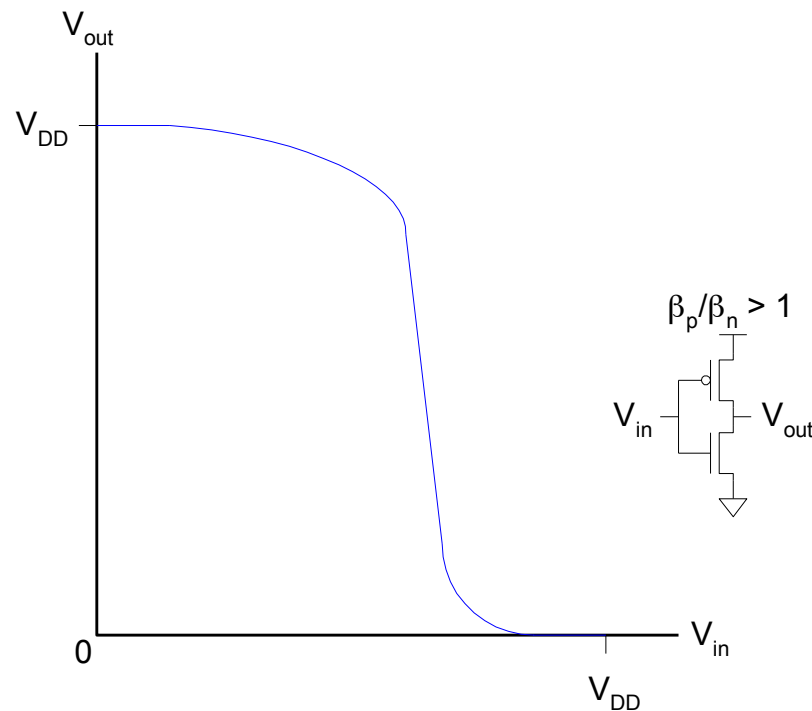
Logic Levels

❑ To maximize noise margins, select logic levels at
  – unity gain point of DC transfer characteristic

Transient Response

- *DC analysis* tells us V_{out} if V_{in} is constant
- *Transient analysis* tells us $V_{out}(t)$ if $V_{in}(t)$ changes
  - Requires solving differential equations
- Input is usually considered to be a step or ramp
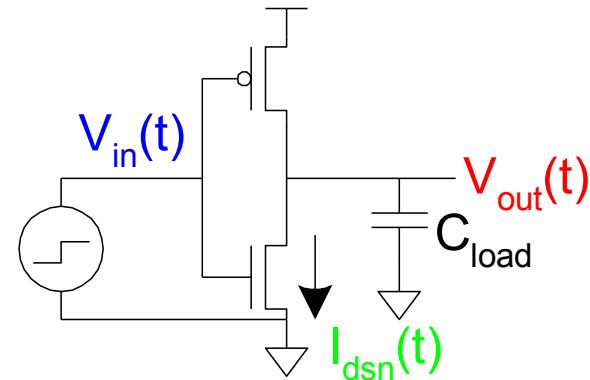 - From 0 to V_{DD} or vice versa

Inverter Step Response

❑ Ex: find step response of inverter driving load cap

$$V_{in}(t) =$$

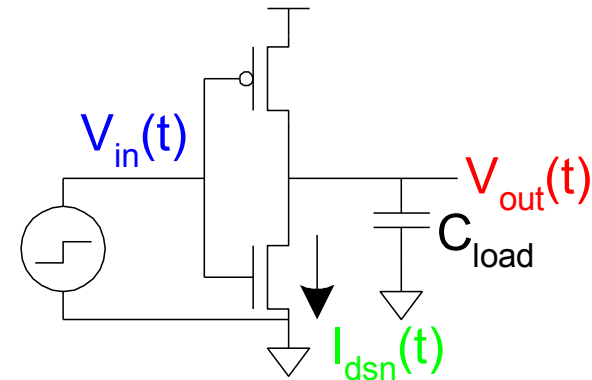$$V_{out}(t < t_0) =$$

$$\frac{dV_{out}(t)}{dt} =$$

$V_{in}(t)$

$V_{out}(t)$

C_{load}

$I_{dsn}(t)$

Inverter Step Response

❑ Ex: find step response of inverter driving load cap

$$V_{in}(t) = u(t - t_0)V_{DD}$$

$$V_{out}(t < t_0) =$$
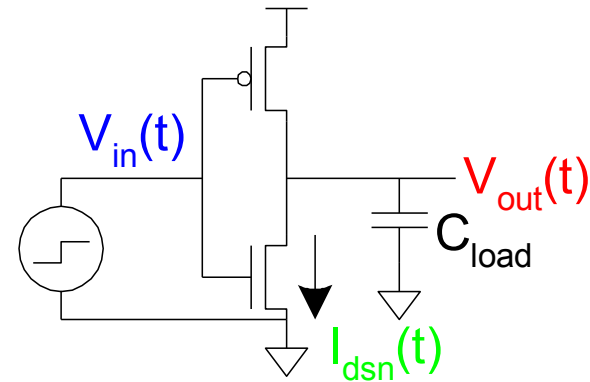
$$\frac{dV_{out}(t)}{dt} =$$

Inverter Step Response

❑ Ex: find step response of inverter driving load cap

$$V_{in}(t) = u(t - t_0)V_{DD}$$

$$V_{out}(t < t_0) = V_{DD}$$

$$\frac{dV_{out}(t)}{dt} =$$

$V_{in}(t)$

$V_{out}(t)$

C_{load}

$I_{dsn}(t)$

Inverter Step Response

❑ Ex: find step response of inverter driving load cap

$$V_{in}(t) = u(t - t_0)V_{DD}$$

$$V_{out}(t < t_0) = V_{DD}$$

$$\frac{dV_{out}(t)}{dt} = -\frac{I_{dsn}(t)}{C_{load}}$$

$$I_{dsn}(t) = \begin{cases} & t \leq t_0 \\ & V_{out} > V_{DD} - V_t \\ & V_{out} < V_{DD} - V_t \end{cases}$$
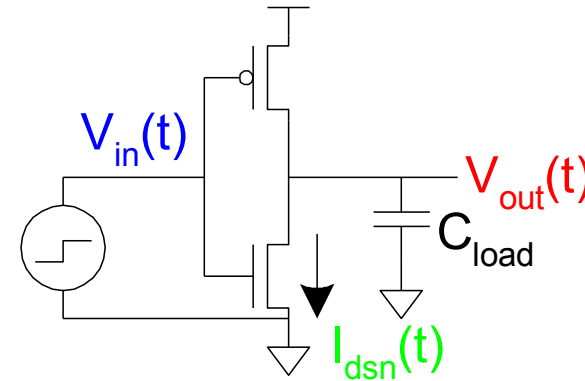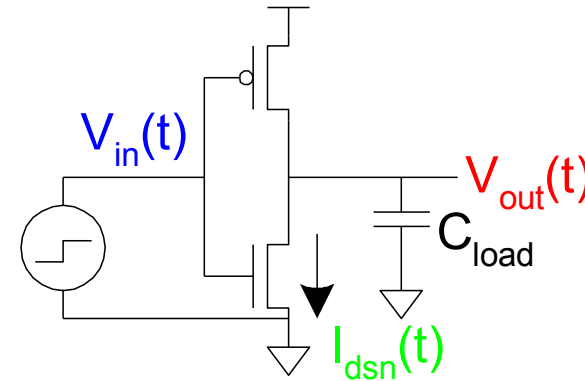
Inverter Step Response

❑ Ex: find step response of inverter driving load cap

$$V_{in}(t) = u(t - t_0)V_{DD}$$

$$V_{out}(t < t_0) = V_{DD}$$

$$\frac{dV_{out}(t)}{dt} = -\frac{I_{dsn}(t)}{C_{load}}$$

$$I_{dsn}(t) = \begin{cases} 0 & t \le t_0 \\ \frac{\beta}{2}(V_{DD} - V)^2 & V_{out} > V_{DD} - V_t \\ \beta\left(V_{DD} - V_t - \frac{V_{out}(t)}{2}\right)V_{out}(t) & V_{out} < V_{DD} - V_t \end{cases}$$
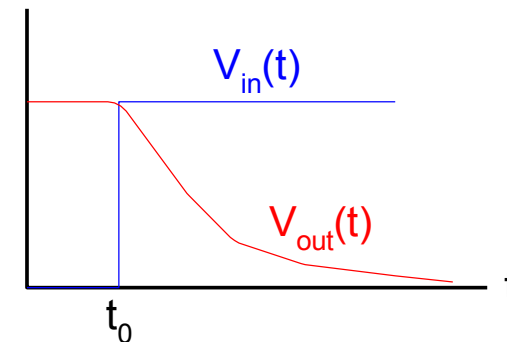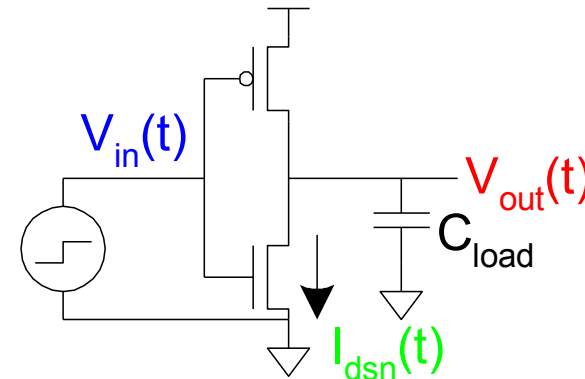
Inverter Step Response

❑ Ex: find step response of inverter driving load cap

$$V_{in}(t) = u(t - t_0)V_{DD}$$

$$V_{out}(t < t_0) = V_{DD}$$

$$\frac{dV_{out}(t)}{dt} = -\frac{I_{dsn}(t)}{C_{load}}$$

$$I_{dsn}(t) = \begin{cases} 0 & t \le t_0 \\ \frac{\beta}{2}(V_{DD} - V)^2 & V_{out} > V_{DD} - V_t \\ \beta\left(V_{DD} - V_t - \frac{V_{out}(t)}{2}\right)V_{out}(t) & V_{out} < V_{DD} - V_t \end{cases}$$

Delay Definitions

- t_{pdr}:

- t_{pdf}:

- t_{pd}:

- t_r:

- t_f: *fall time*

Delay Definitions

❑ **t_pdr**: *rising propagation delay* 充電 傳遞延遲 只有到 $\frac{Vdd}{2}$ 的時間
  – From input to rising output crossing $V_{DD}/2$

❑ **t_pdf**: *falling propagation delay* 放電 t_{pdf}
  – From input to falling output crossing $V_{DD}/2$

❑ **t_pd**: *average propagation delay*
  – $t_{pd} = (t_{pdr} + t_{pdf})/2$

❑ **t_r**: *rise time*

  – From output crossing $0.2\ V_{DD}$ to $0.8\ V_{DD}$

❑ **t_f**: *fall time*

  – From output crossing $0.8\ V_{DD}$ to $0.2\ V_{DD}$

Delay Definitions

- **t_{cdr}**: *rising contamination delay*
  - From input to rising output crossing $V_{DD}/2$
- **t_{cdf}**: *falling contamination delay*
  - From input to falling output crossing $V_{DD}/2$
- **t_{cd}**: *average contamination delay*
  - $t_{pd} = (t_{cdr} + t_{cdf})/2$

Simulated Inverter Delay

❑ Solving differential equations by hand is too hard

❑ SPICE simulator solves the equations numerically

– Uses more accurate I-V models too!

❑ But simulations take time to write
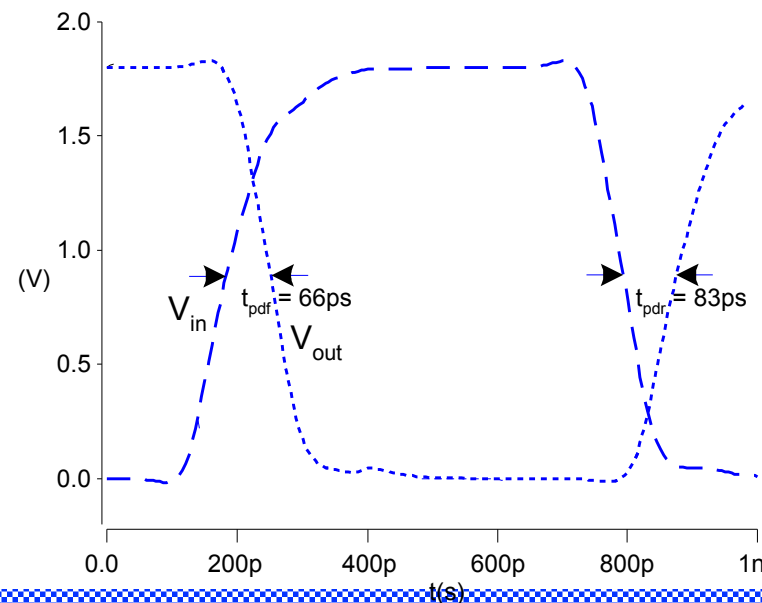
Delay Estimation

❑ We would like to be able to easily estimate delay
  – Not as accurate as simulation
  – But easier to ask   "What if?"
❑ The step response usually looks like a 1st order RC response with a decaying exponential.
❑ Use RC delay models to estimate delay
  – C = total capacitance on output node
  – Use *effective resistance* R
  – So that t_{pd} = RC
❑ Characterize transistors by finding their effective R
  – Depends on average current as gate switches

RC Delay Models

- ❑ Use equivalent circuits for MOS transistors
  - – Ideal switch + capacitance and ON resistance
  - – Unit nMOS has resistance R, capacitance C
  - – Unit pMOS has resistance 2R, capacitance C
- ❑ Capacitance proportional to width
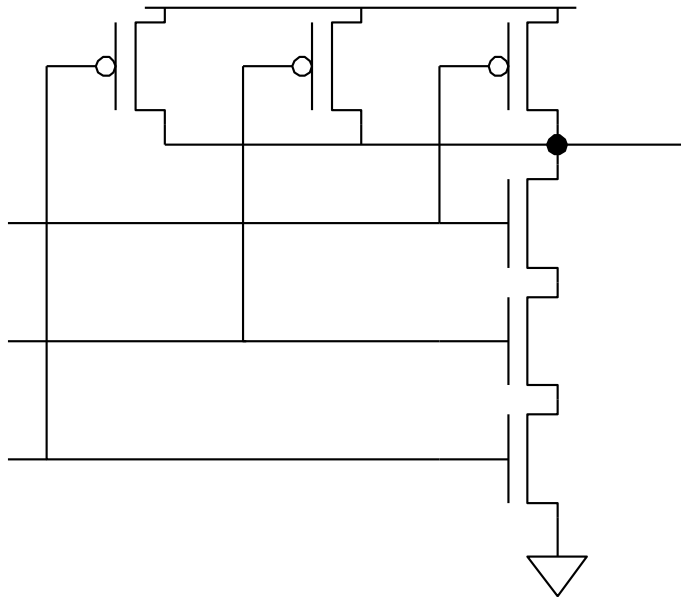- ❑ Resistance inversely proportional to width
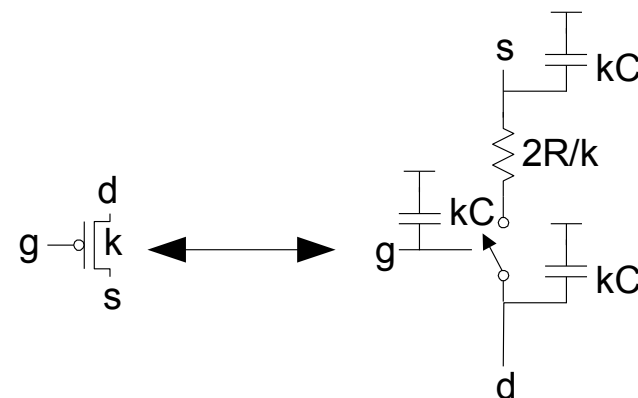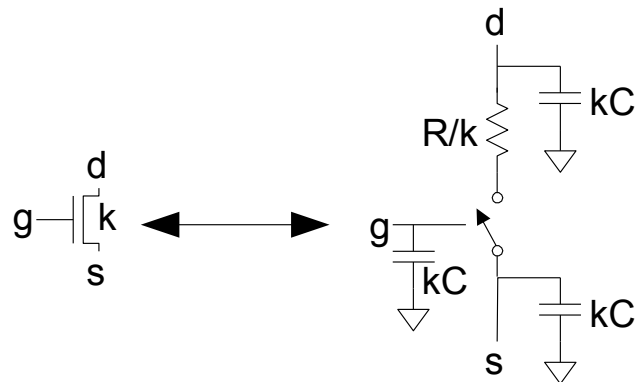
這裡是在算基本的擴散電容
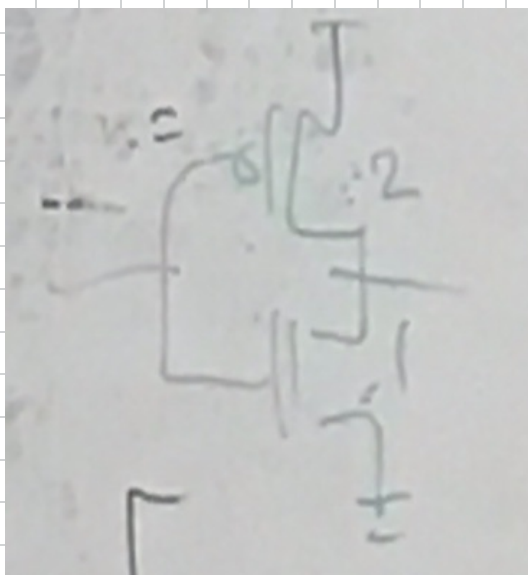
Example: 3-input NAND

❑ Sketch a 3-input NAND with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (R).

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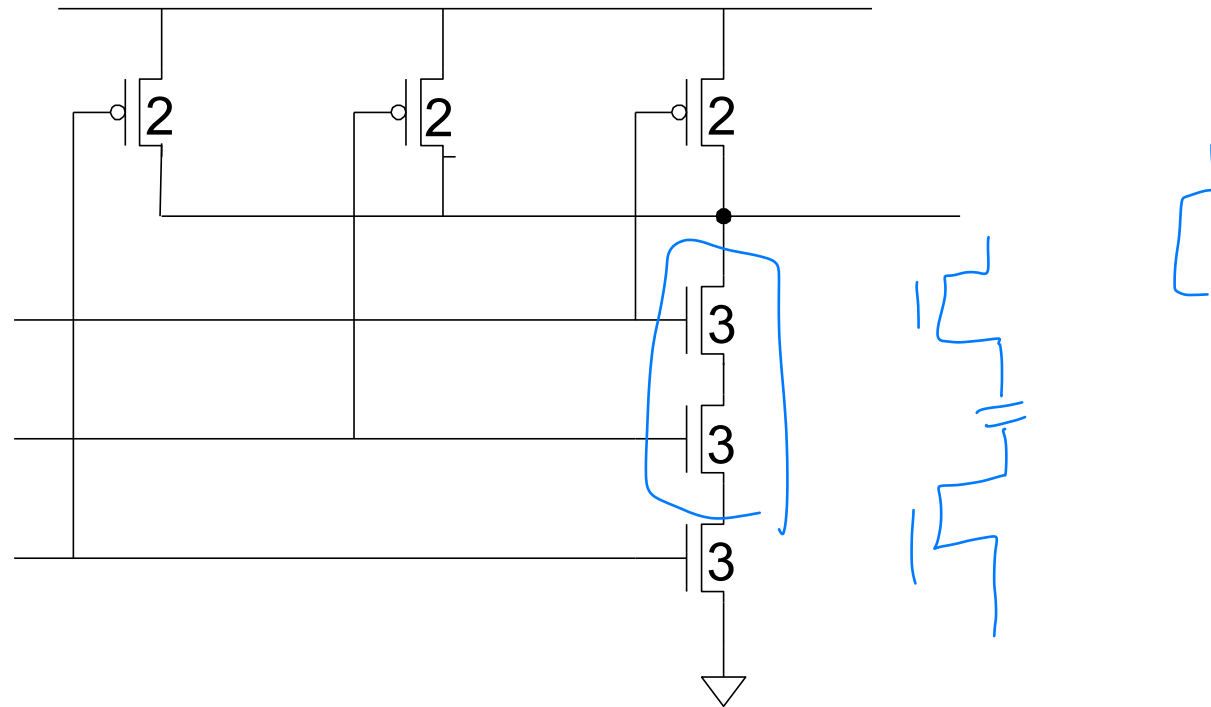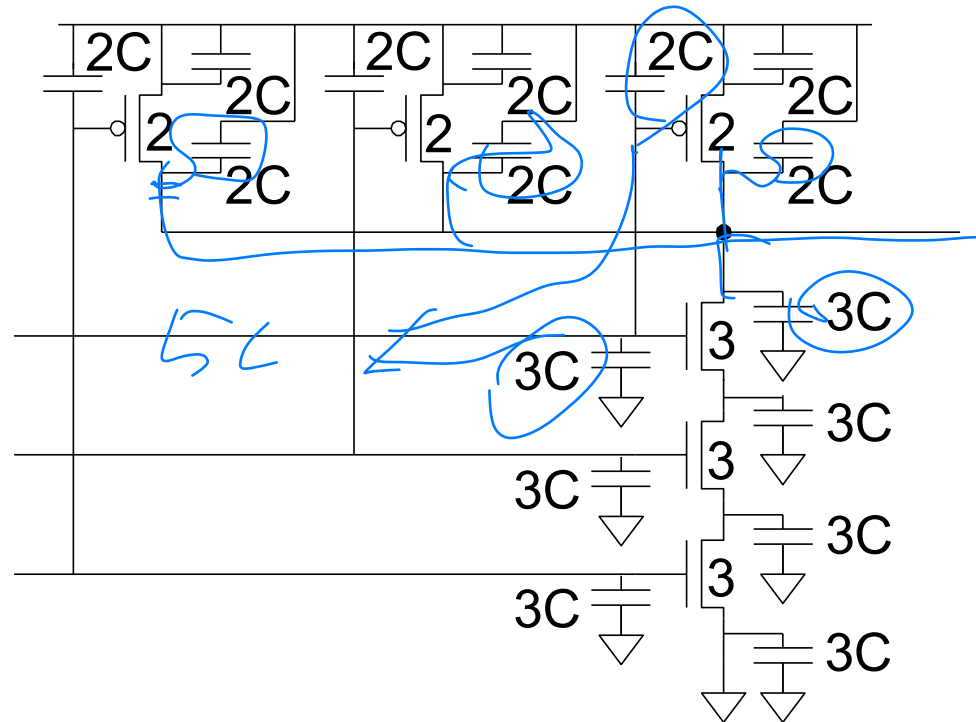
他為了把電阻變小
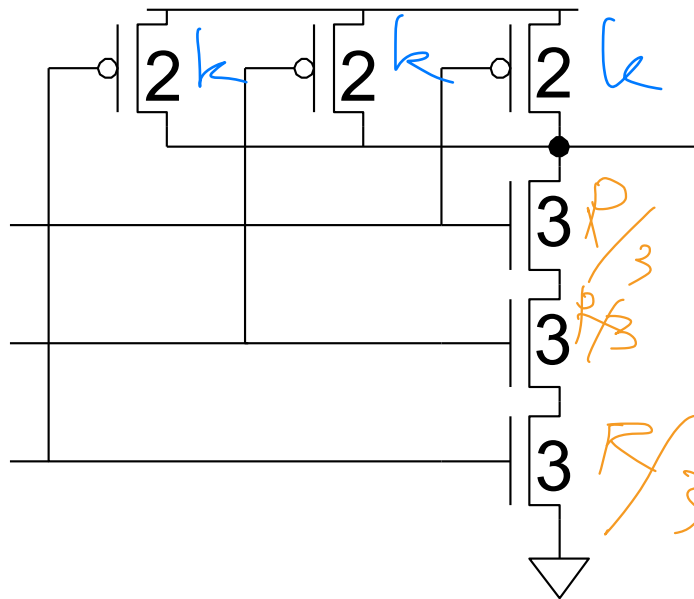
因為串連 電阻變三倍
把

3-input NAND Caps

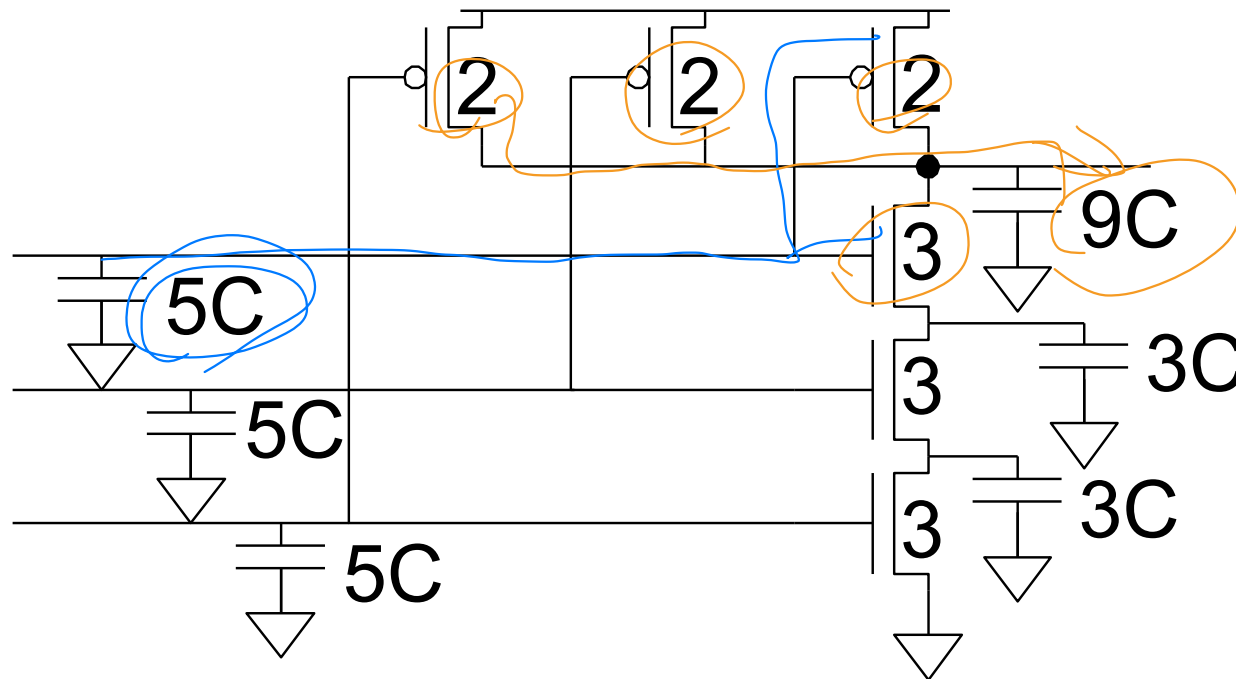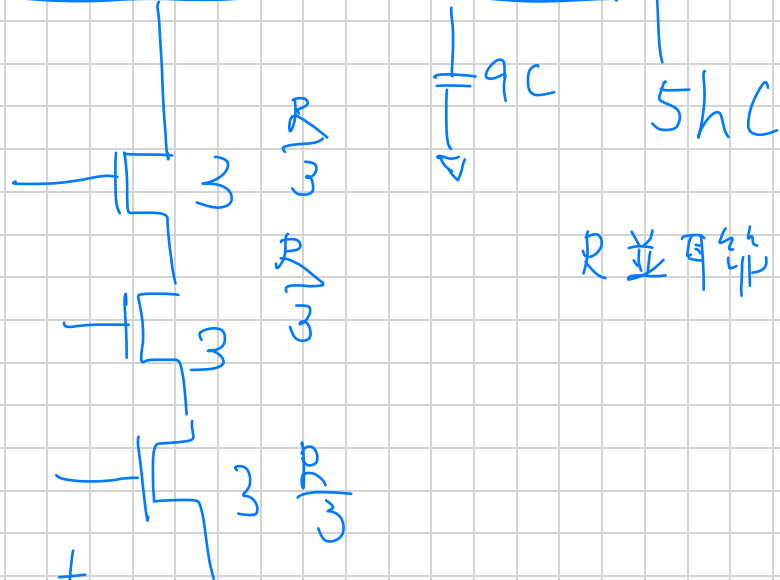❑ Annotate the 3-input NAND gate with gate and diffusion capacitance.

3-input NAND Caps

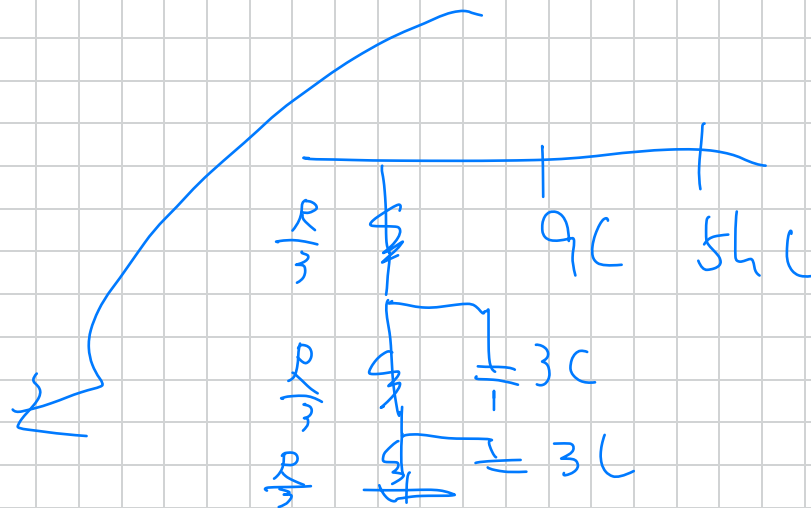❑ Annotate the 3-input NAND gate with gate and diffusion capacitance.

3-input NAND Caps

❑ Annotate the 3-input NAND gate with gate and diffusion capacitance.

Vdd

$\overline{(A * B * C)}$

A ─o[R/2]   B ─o[R/2]   C ─o[R/2]   R

─|[3 R/3]

─|[3 R/3]

─|[3 R/3]

$\frac{1}{9}C \quad 5hC$

R 並列 : $\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} + \dots$

$9RC + 5RhC + 2RC + RC$

$= 12RC + 5RhC$

C	B	A	t_r	t_f
0	0	0	$\frac{R}{3}(9+5h)$	x
0	0	1	$\frac{R}{2}(9+5h)$	x
0	1	0	$\frac{R}{2}(\ ,\ )$	x
0	1	1	$R(\ ,\ )$	x
1	0	0	$\frac{R}{2}(\ ,\ )$	x
1	0	1	$R(\ ,\ )$	x
1	1	0	$R(\ ,\ )$	x
1	1	1		x

$\frac{R}{3}$ 9C   5hC

$\frac{R}{3}$

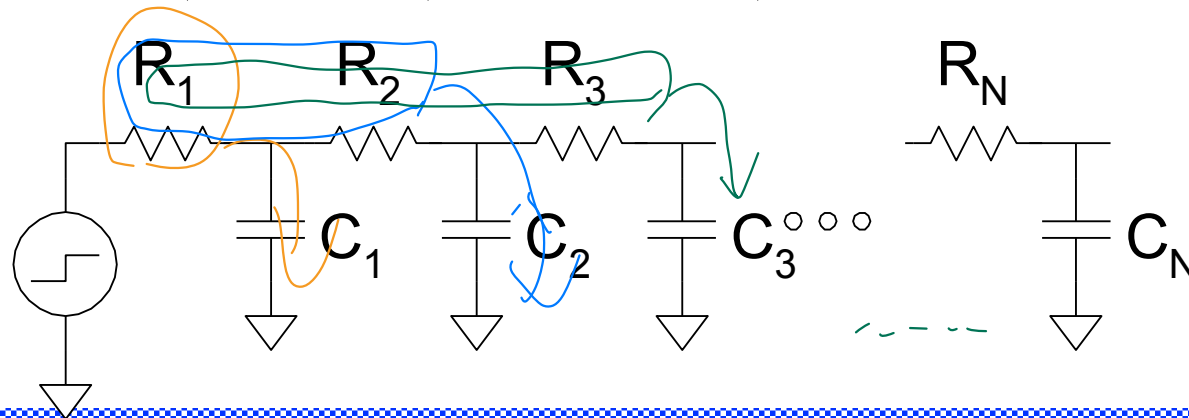$\frac{R}{3}$ 3C

$\frac{R}{3}$ 3C

Elmore Delay

- ❑ ON transistors look like resistors
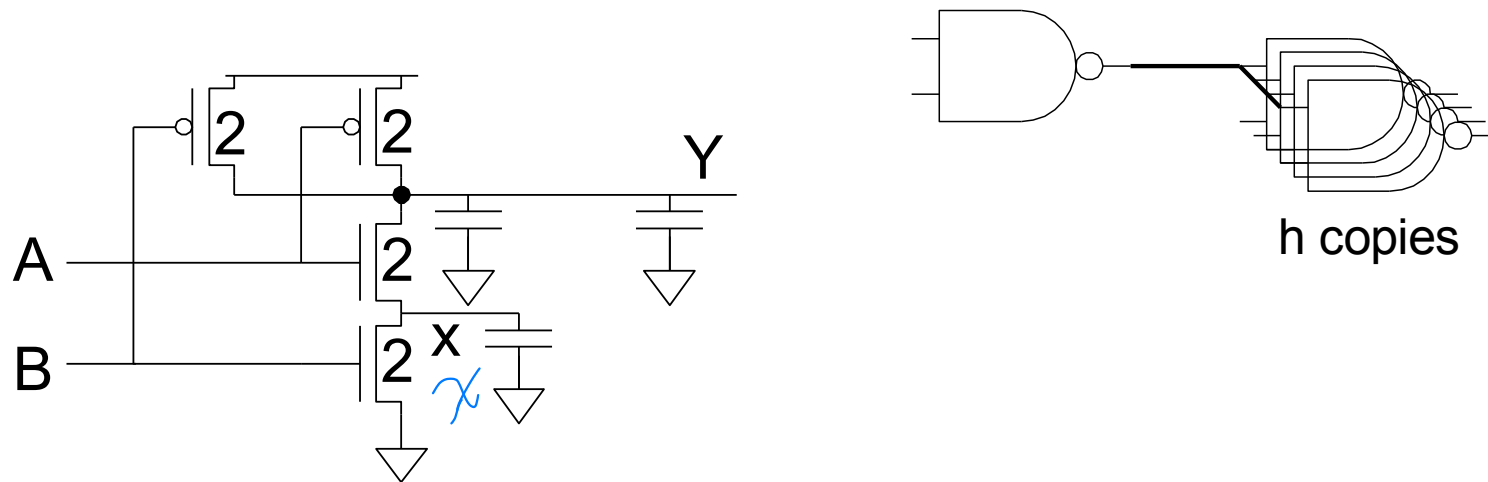- ❑ Pullup or pulldown network modeled as *RC ladder*
- ❑ Elmore delay of RC ladder

$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$

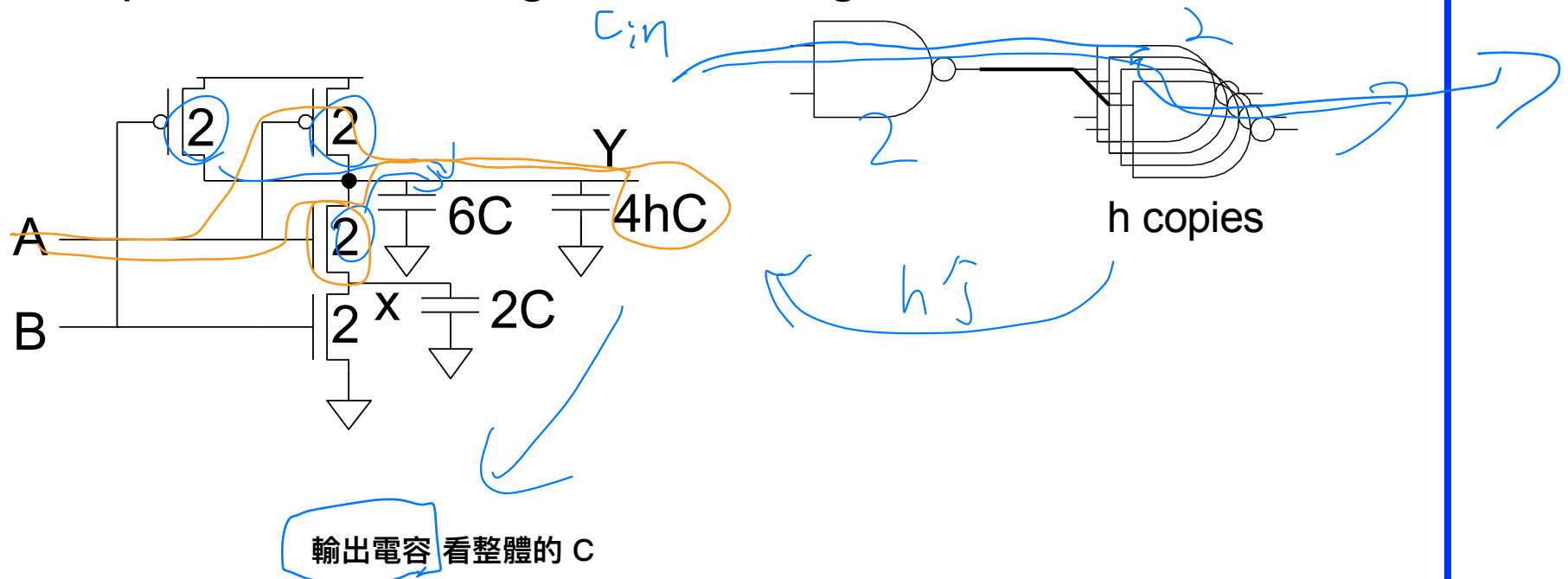$$= R_1 C_1 + (R_1 + R_2) C_2 + ... + (R_1 + R_2 + ... + R_N) C_N$$

Example: 2-input NAND

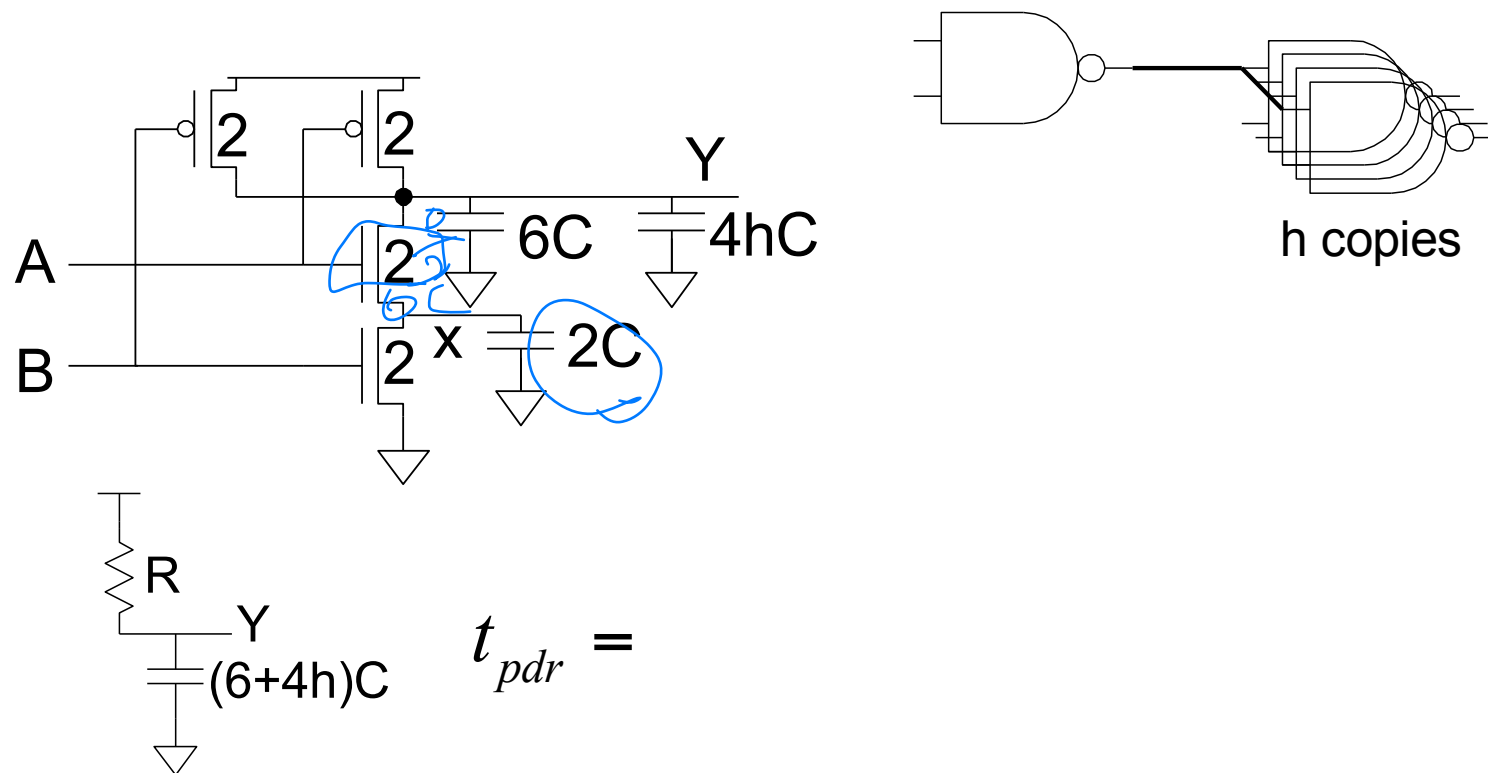❑ Estimate worst-case rising and falling delay of 2-input NAND driving *h* identical gates.

h copies

Example: 2-input NAND

❑ Estimate rising and falling propagation delays of a 2-input NAND driving *h* identical gates.

輸出電容 看整體的 C

Example: 2-input NAND

❑ Estimate *rising* and falling propagation delays of a 2-input NAND driving *h* identical gates.

h copies

$$t_{pdr} =$$

Example: 2-input NAND

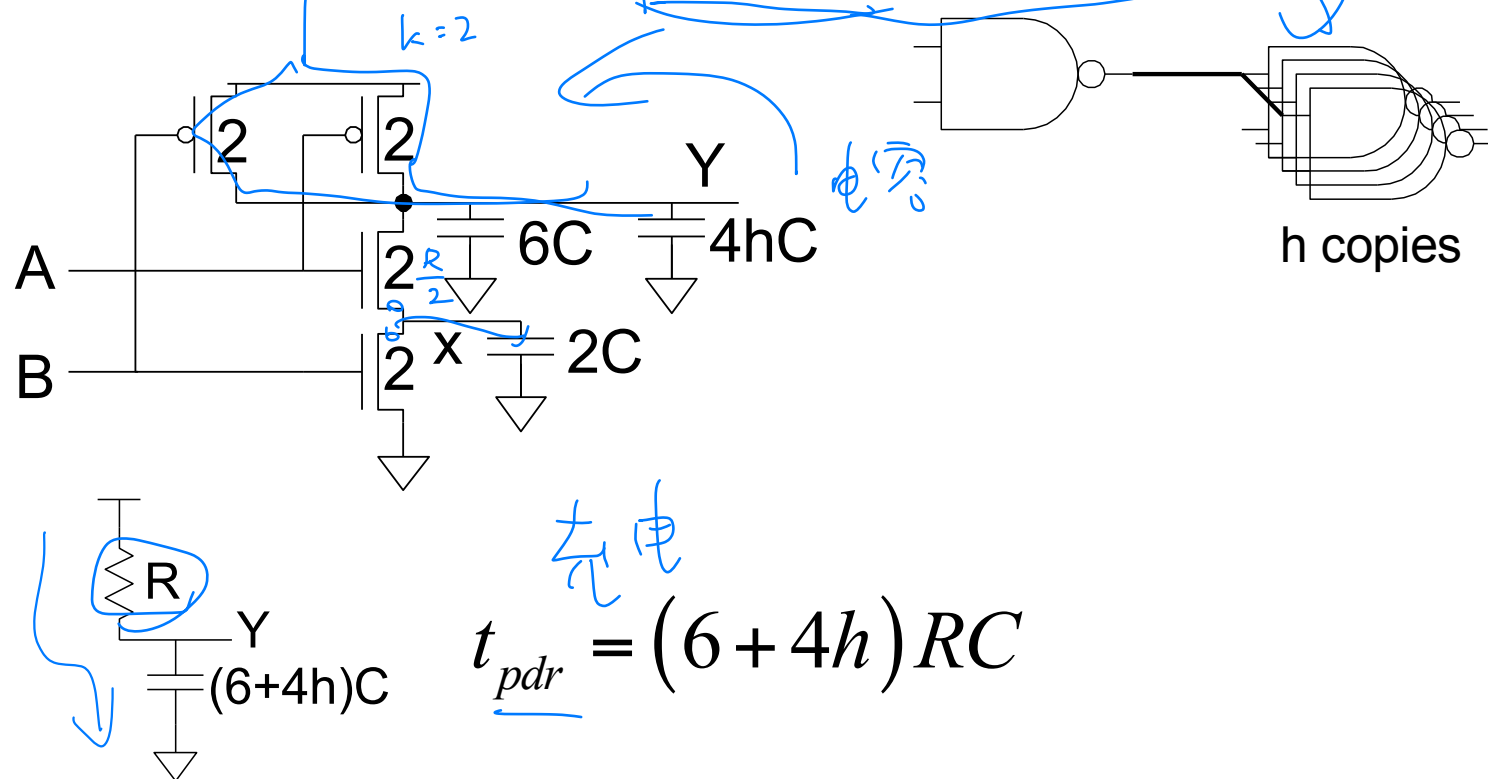❑ Estimate *rising* and falling propagation delays of a 2-input NAND driving *h* identical gates.
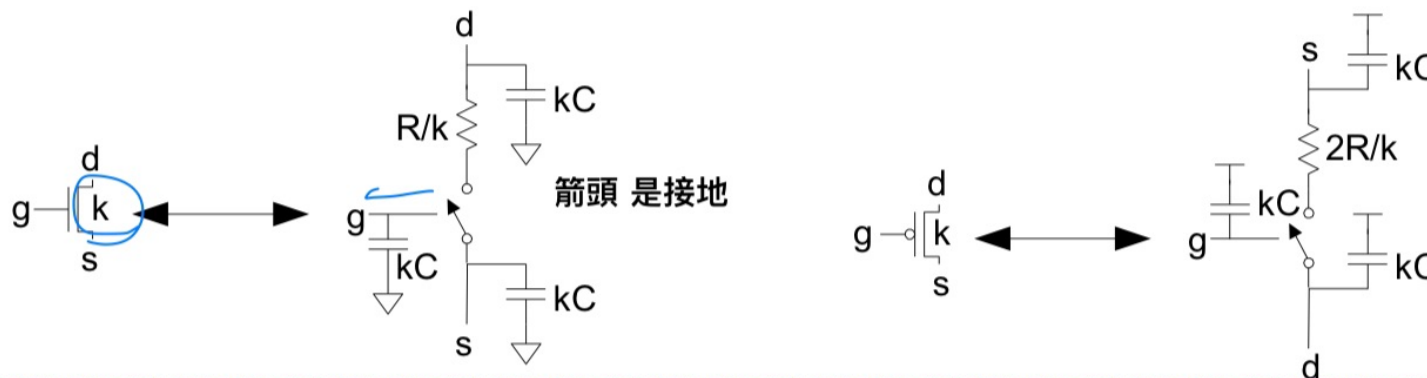


h copies

$$t_{pdr} = (6 + 4h)RC$$

RC Delay Model

❑ Use equivalent circuits for MOS transistors
  – Ideal switch + capacitance and ON resistance
  – Unit nMOS has resistance R, capacitance C
  – Unit pMOS has resistance 2R, capacitance C
❑ Capacitance proportional to width
❑ Resistance inversely proportional to width

箭頭 是接地

原本是2R 的Pmos 但為了要兩邊兩邊電流一樣 ids一樣 所以 pmos 要做寬
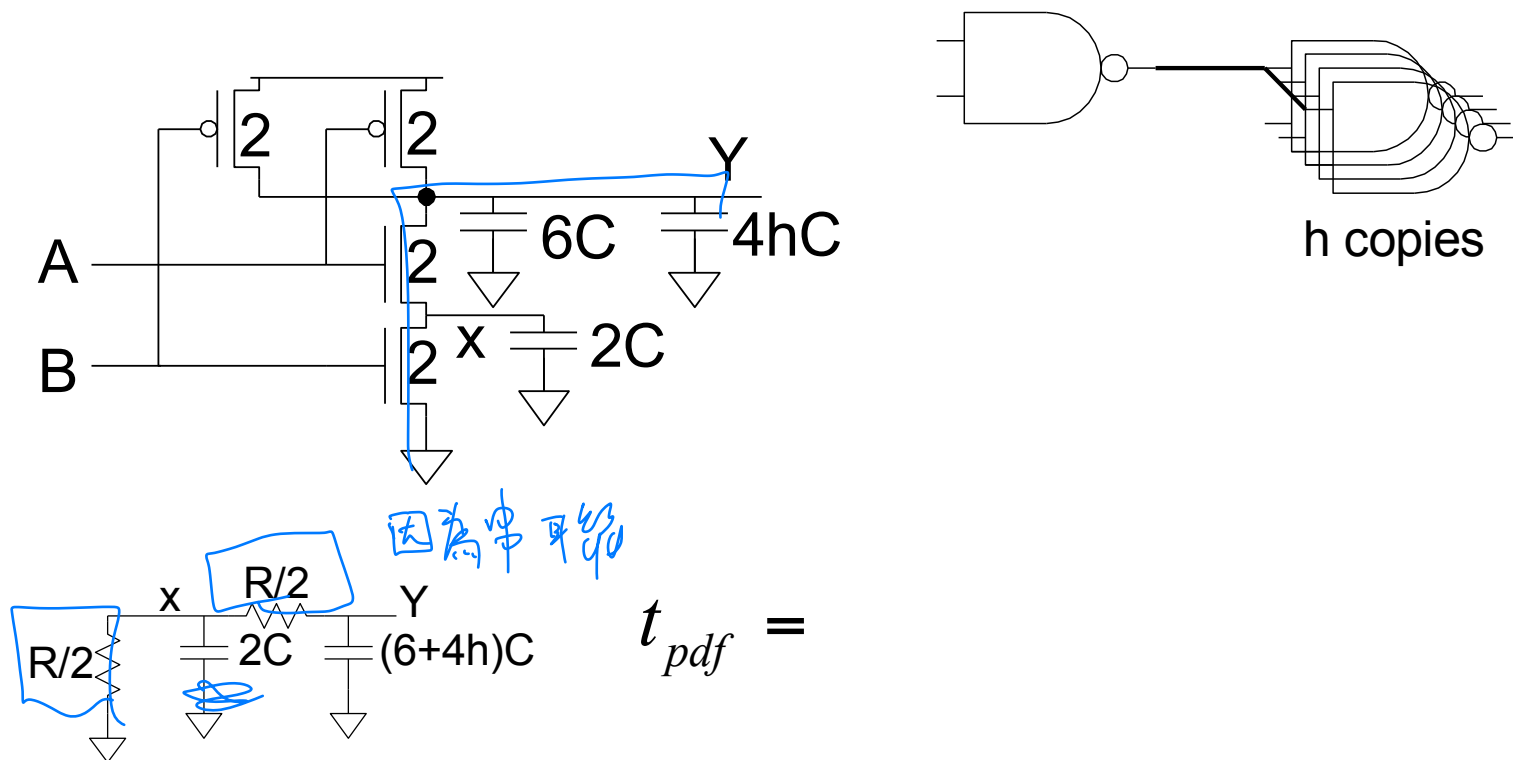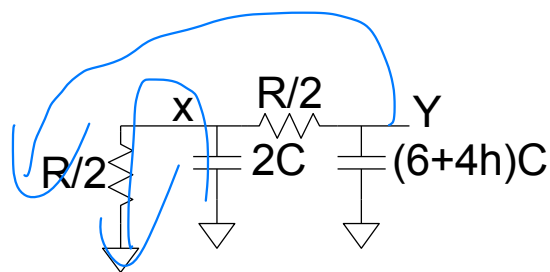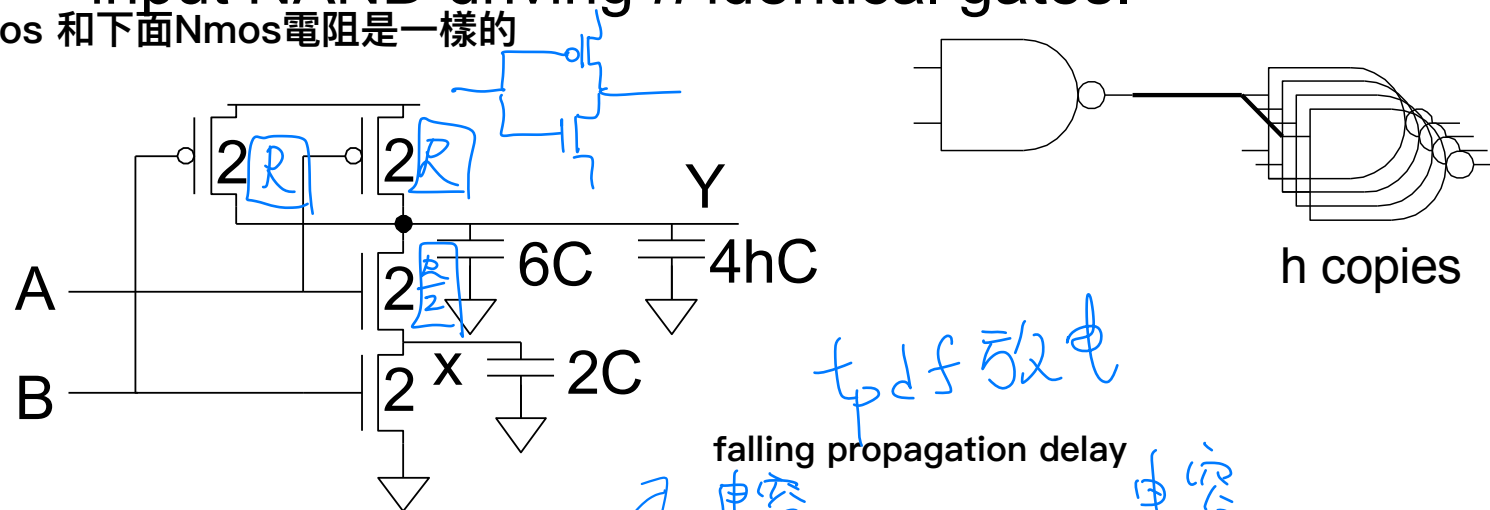也就是nmos 的兩倍寬　最終兩邊都是R

Example: 2-input NAND
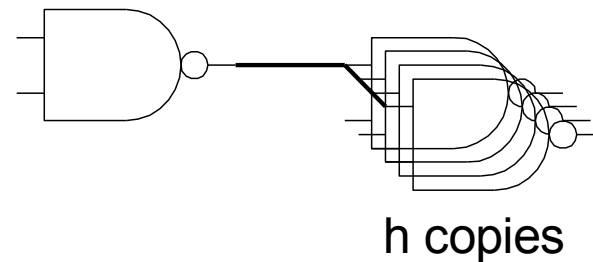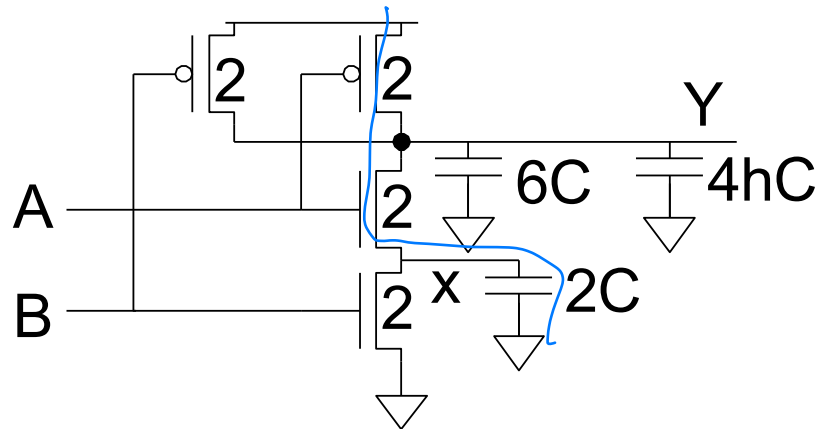
❑ Estimate rising and falling propagation delays of a 2-input NAND driving h identical gates.

Example: 2-input NAND

❑ Estimate rising and *falling* propagation delays of a 2-input NAND driving *h* identical gates.

h copies

$$t_{pdf} =$$

Example: 2-input NAND

❑ Estimate rising and falling propagation delays of a 2-input NAND driving h identical gates.

主要為了上面pmos 和下面Nmos電阻是一樣的

從電容

這樣
放電

Y

$2R$ $2R$

A

$2\frac{R}{2}$ 6C   4hC

B

2 X   2C

h copies

t_{pdf} 放电

falling propagation delay

电容   电容

X   R/2   Y

R/2   2C   (6+4h)C

$$t_{pdf} = (2C)\left(\frac{R}{2}\right) + \left[(6+4h)C\right]\left(\frac{R}{2} + \frac{R}{2}\right)$$
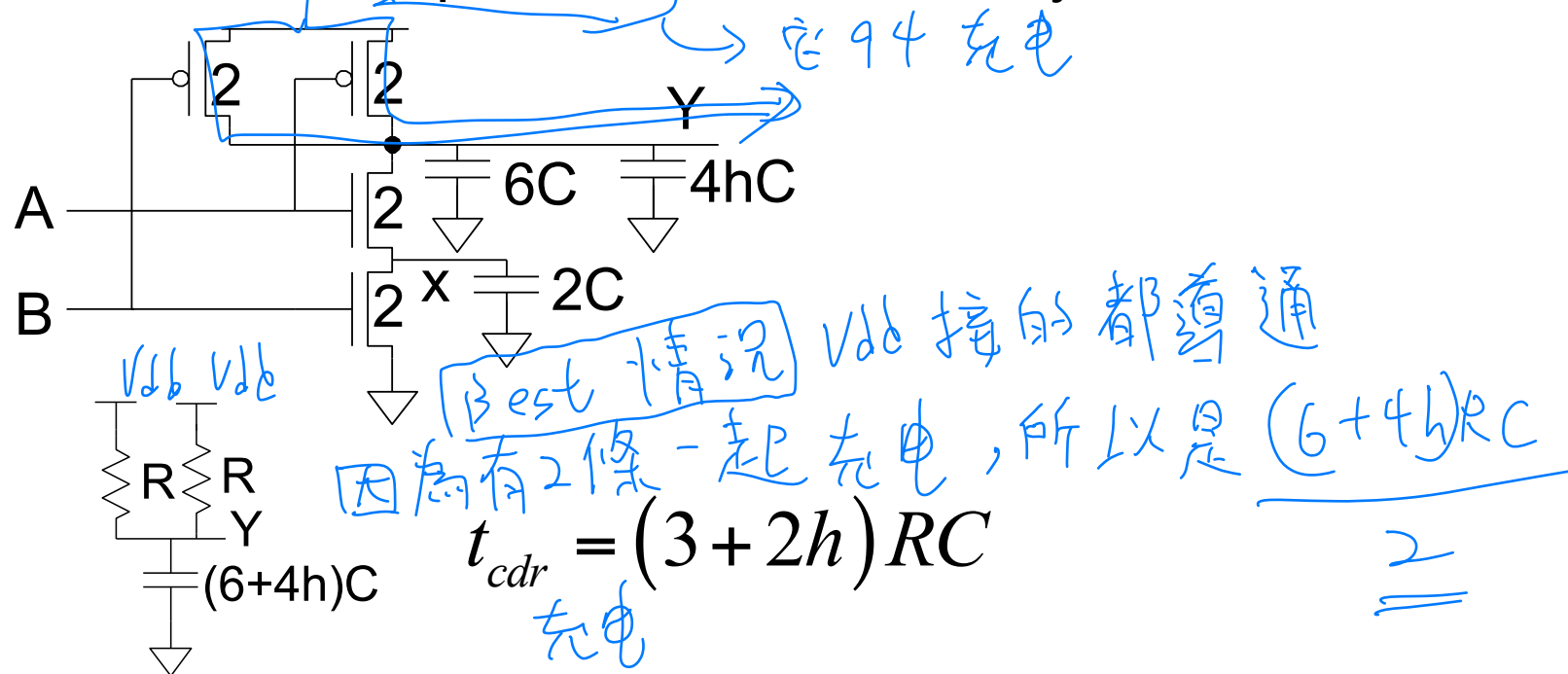
$$= (7+4h)RC$$

Delay Components

❑ Delay has two parts
  – *Parasitic delay* 寄生 延遲？
    • 6 or 7 RC
    • Independent of load
  – *Effort delay*
   • 4h RC
    • Proportional to load capacitance

Contamination Delay

- Best-case (contamination) delay can be substantially less than propagation delay.

- Ex: If both inputs fall simultaneously

在94充电

Best 情況 Vdd 接的都導通

因為有2條一起充電，所以是 $(6+4h)RC$

$$t_{cdr} = (3+2h)RC$$

充電

Diffusion Capacitance

- ❑ we assumed contacted diffusion on every s / d.
- ❑ Good layout minimizes diffusion area
- ❑ Ex: NAND3 layout shares one diffusion contact
  - – Reduces output capacitance by 2C
  - – Merged uncontacted diffusion might help too

左邊比較好
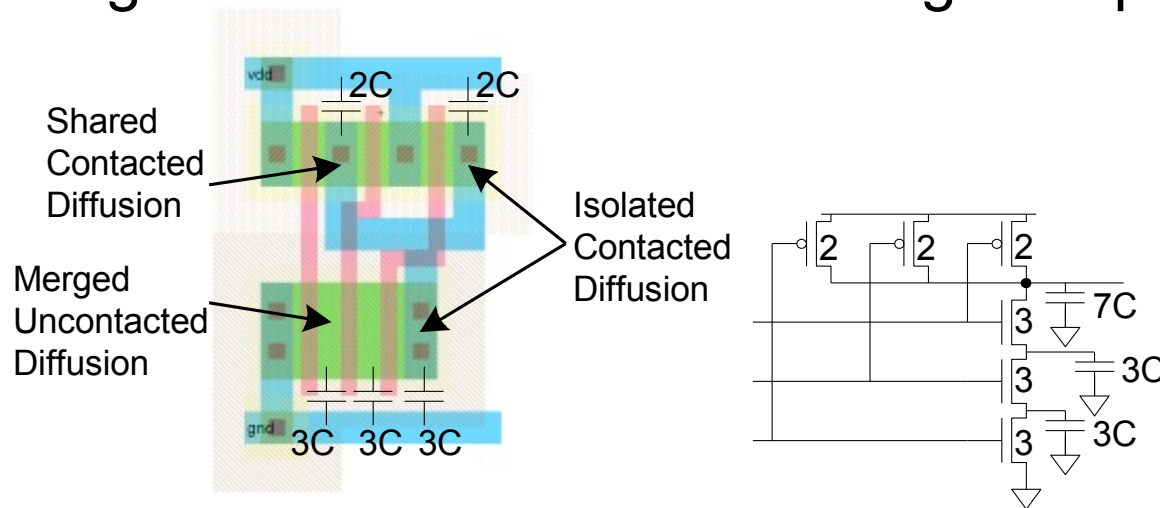
Layout Comparison

❑ Which layout is better?