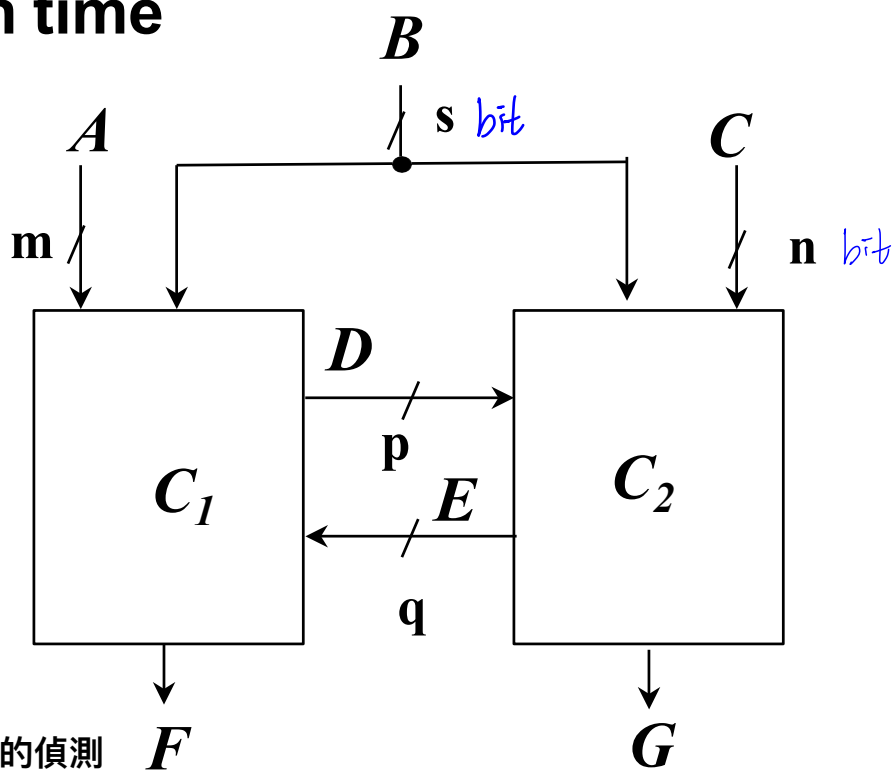
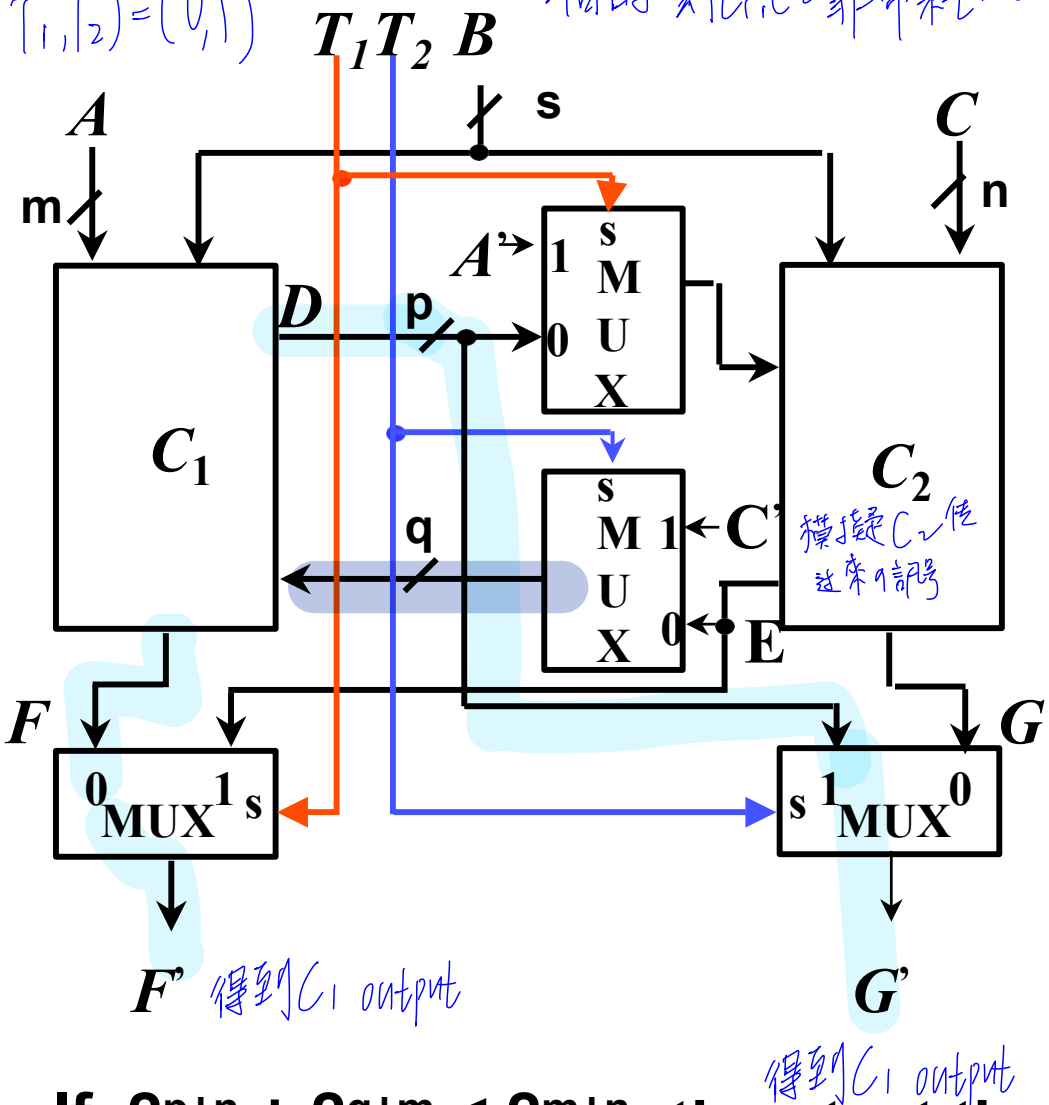
Partition of Large Combinational Circuits

- **Rule : To reduce test generation costs and/or test application time**



這裡針對的是 組合邏輯 的偵測
因為 續向邏輯 可以用scan暫存器來知道



T_1	T_2	Mode
0	0	normal
0	1	test C_1
1	0	test C_2

If $2^{p+n} + 2^{q+m} < 2^{m+n}$ then test time can be reduced

邏輯冗余

Logic Redundancy

Rule: Avoid or eliminate redundancy ckt.

- **Design errors**
- **Undetectable faults**
- **Invalidation of some tests** 有些test是无效的
- **Bias fault coverage** fault coverage会变低

Example

原本多功器的電路在轉態時可能會有 A=1, B=1, S=1, 但Z卻=0 (例如為了解決這個問題, 多加了這個gate來避免問題

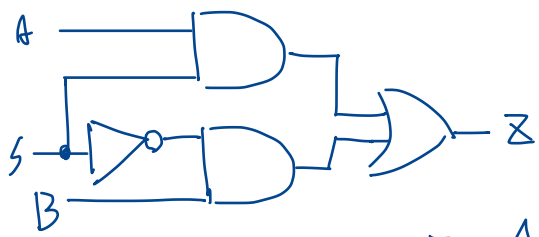
⇒但卻變成了undetectable fault

⇒∵假設SA0而A,B,S仍為1時, 無法觀察到這個錯誤

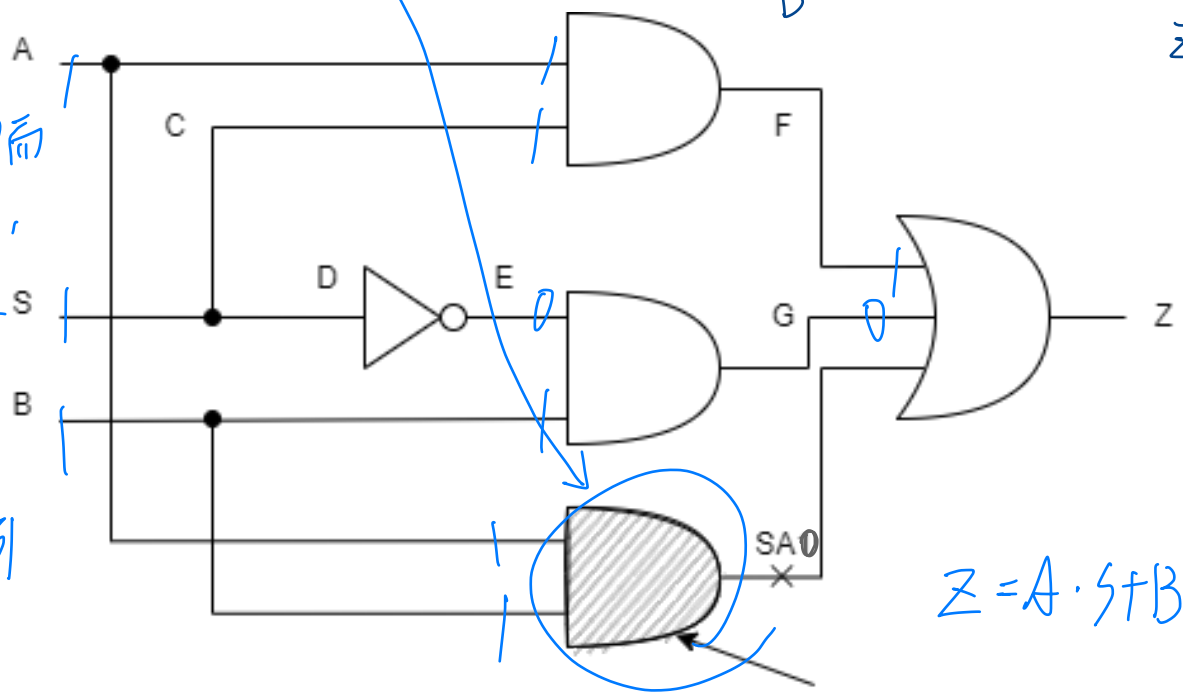
⇒用了redundancy gate來解決一個問題, 卻又引發另一個問題

多工器的電路

原本:



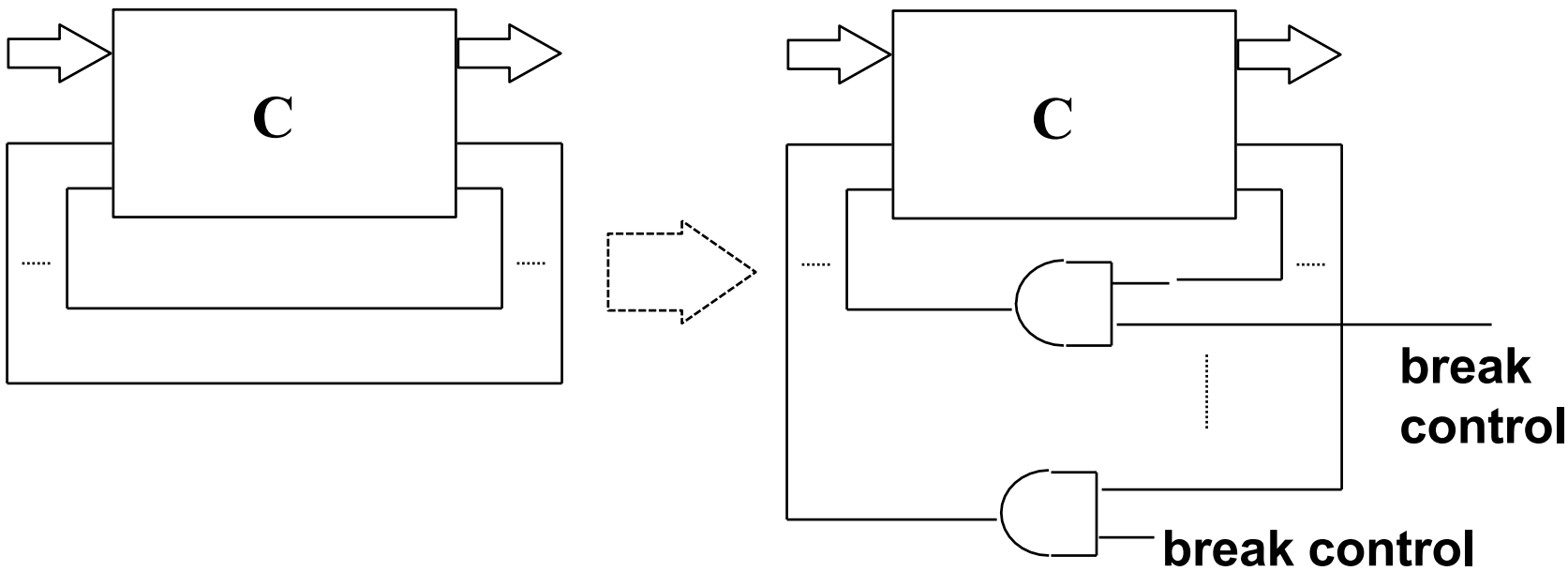
$Z = A \cdot S + B \cdot \bar{S}$



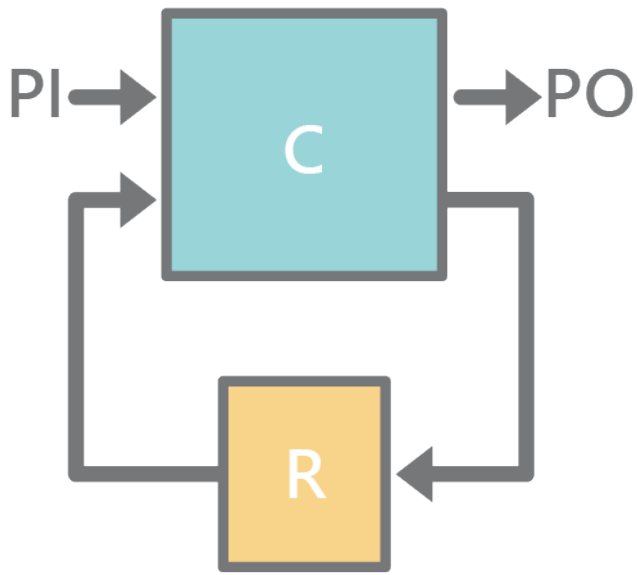
$Z = A \cdot S + B \cdot \bar{S} + AB$

Global Feedback Paths

Rule: break global feedback

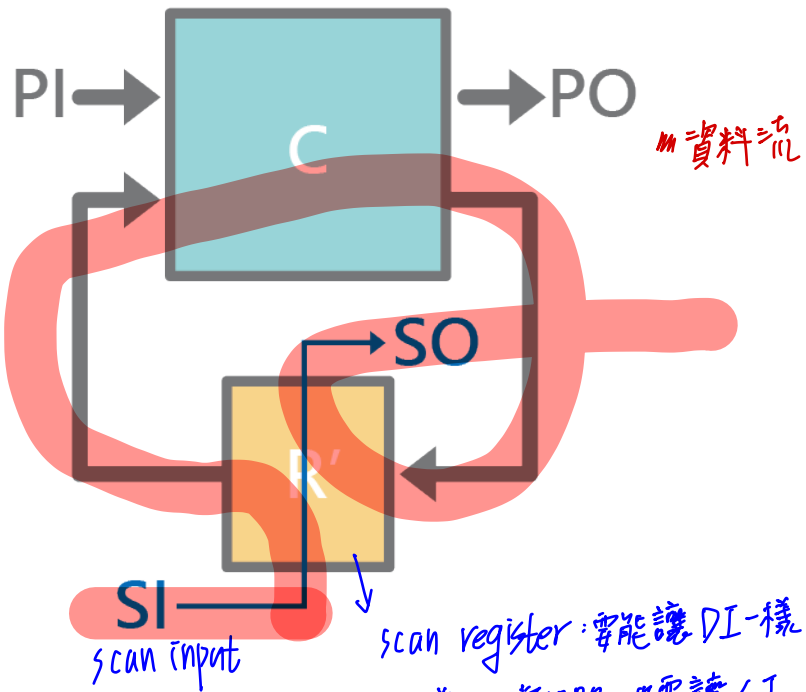


Scan System



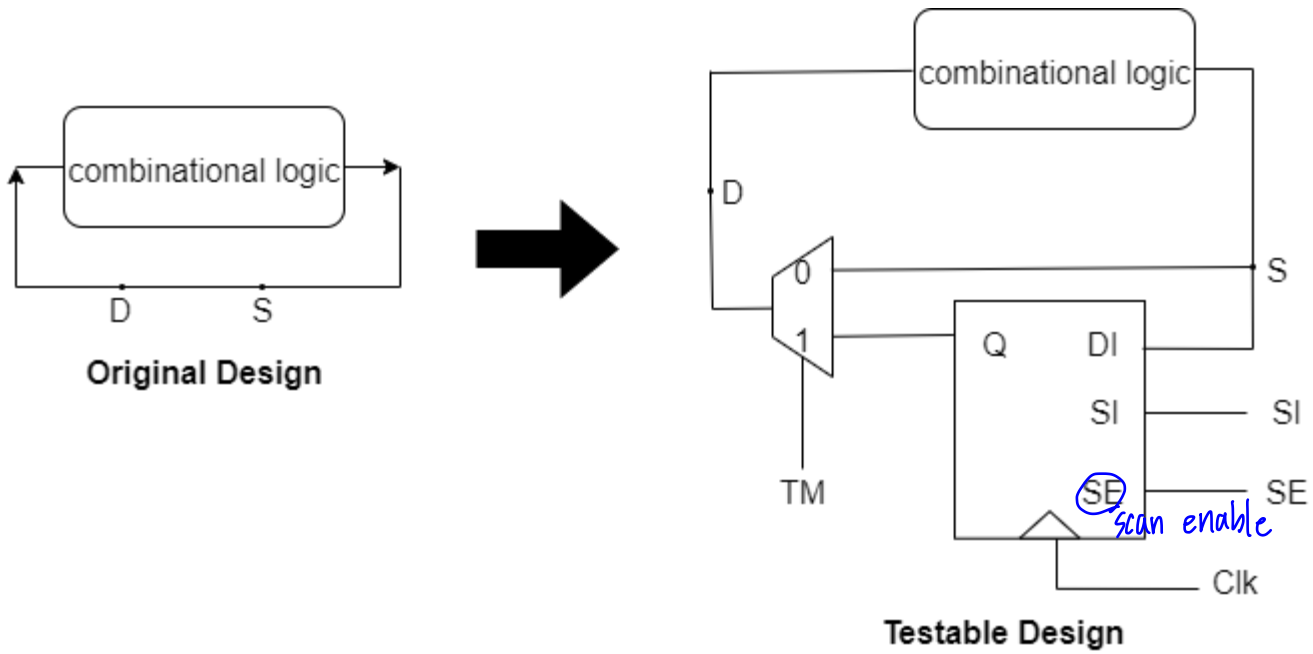
Original design

Pass mode
Scan mode



Modified circuit

Scan System



Original design

Modified circuit

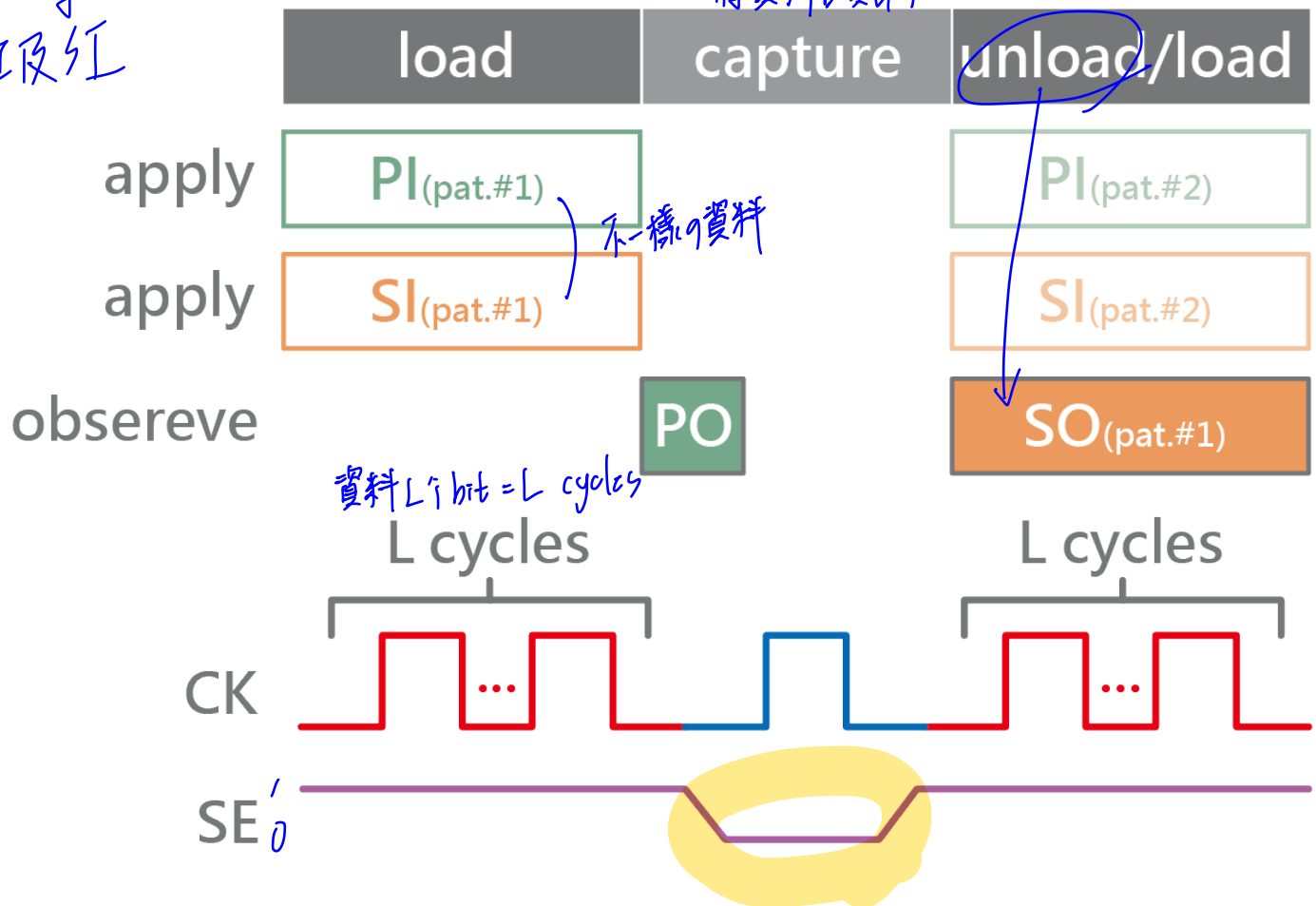
Scan System

- Long test time ∵它是串联
- Large test data
- Too much overhead
- How to test DFT circuit itself

Scan Operation

testing 时会有2种訊号
:PI及SI

將資料讀出來



Scan System Performance

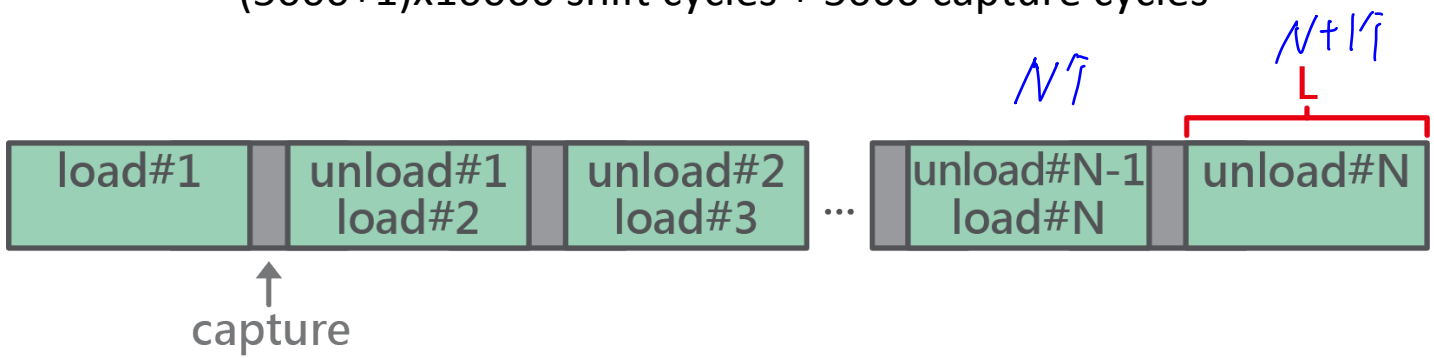
- How to calculate the test cycle:
  - L: Length of scan chain, Npattern: Number of test patterns

$$(N_{pattern}+1) \times L + N_{pattern}$$

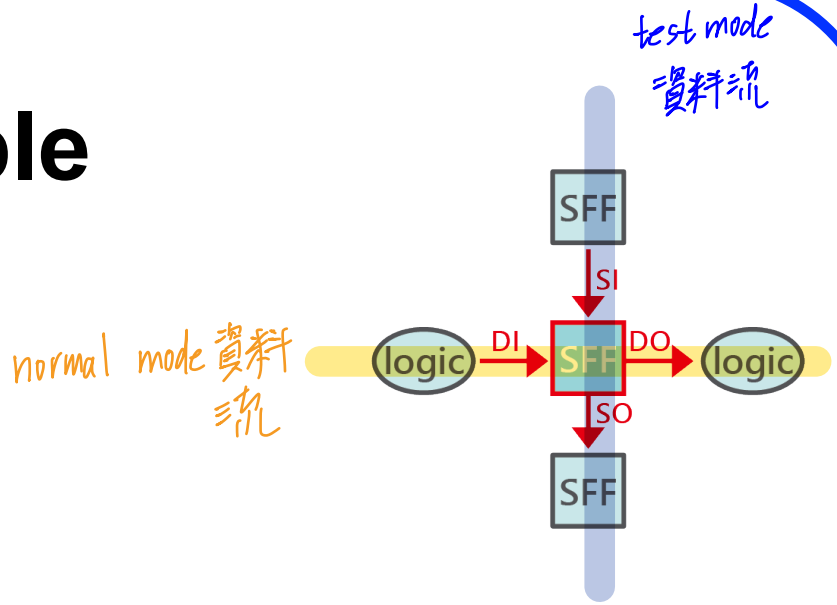
shift capture

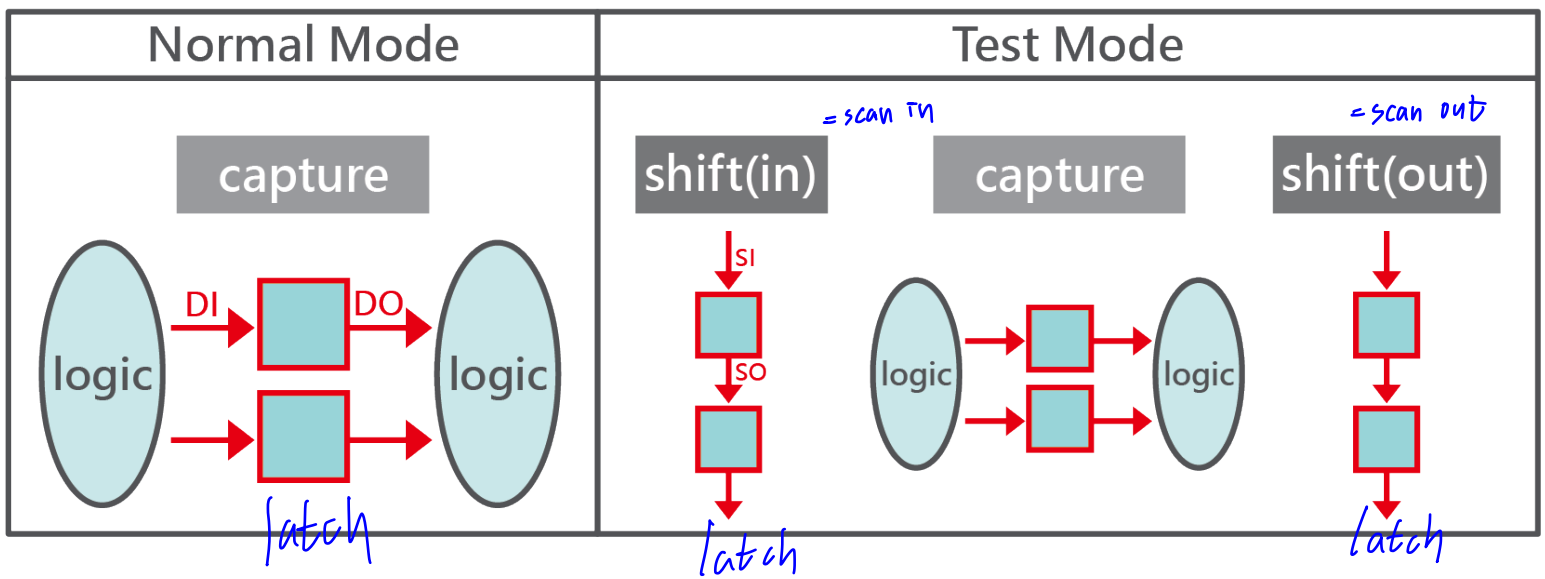
SI PI

- Example: Apply 5000 test patterns to a CUT with 10000 SFF
  - Total cycles = 50015000 cycles
    (5000+1)x10000 shift cycles + 5000 capture cycles

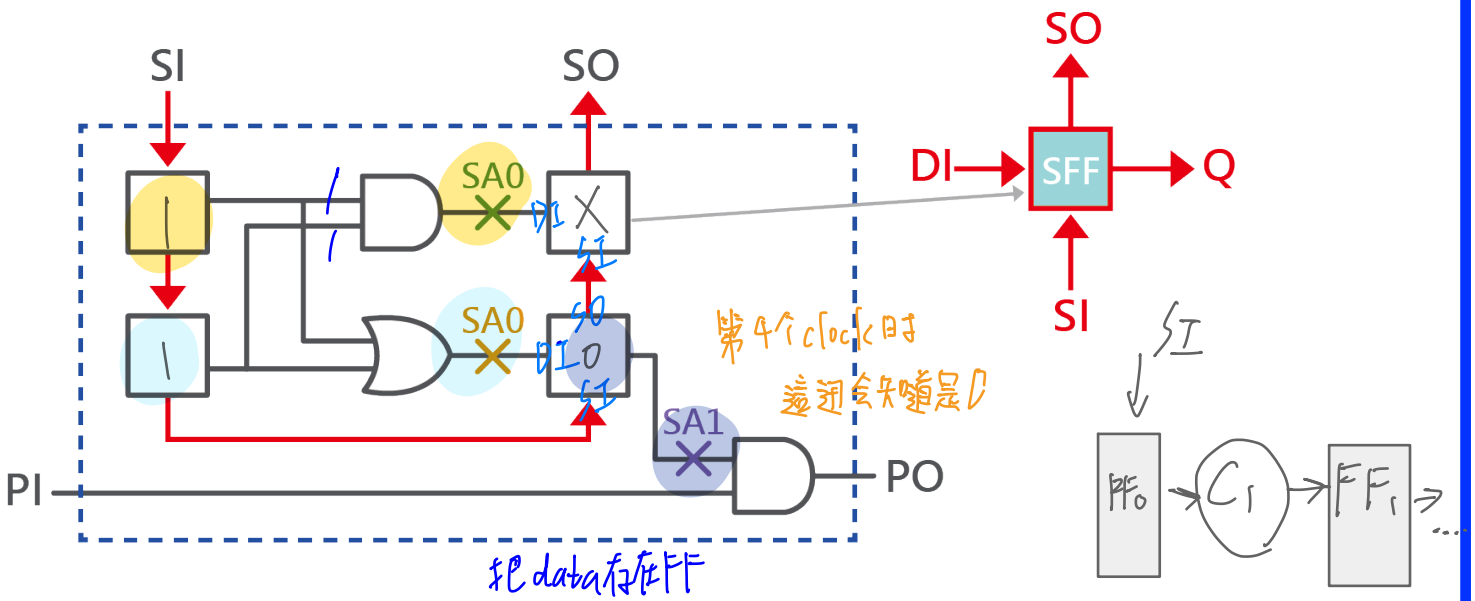


Example


test mode
資料流
SFF
SI
normal mode 資料流
logic
DI
SFF
DO
logic
SO
SFF


Normal Mode
Test Mode
capture
shift(in)
capture
shift(out)
scan in
scan out
logic
DI
DO
logic
SI
SO
logic
logic
latch
latch
latch

Example

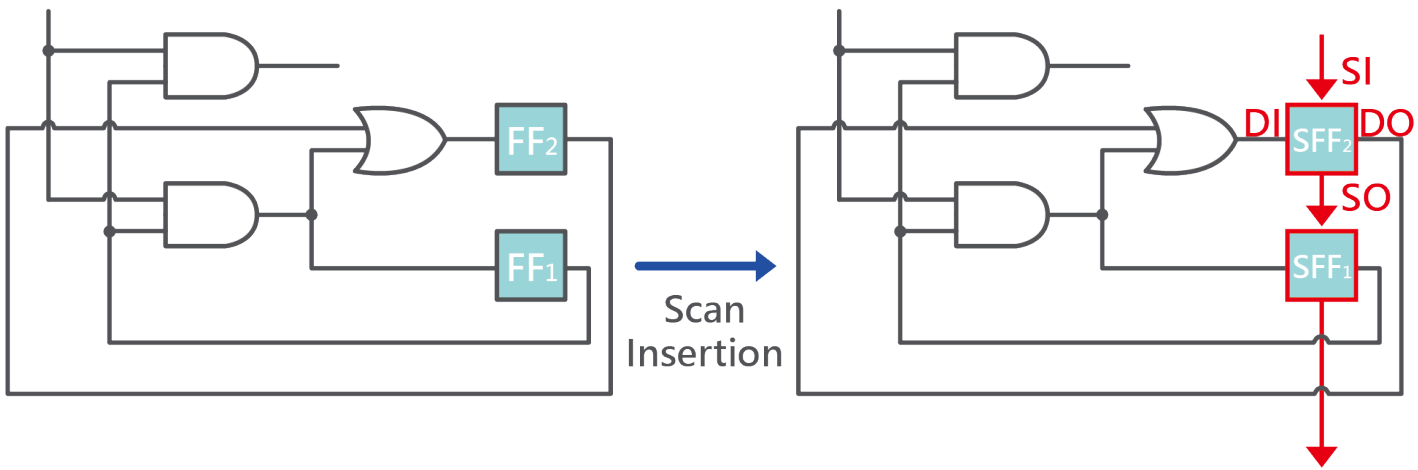


load		capture		unload
CK=PPPP	SE 1→0	CK=P	SE 0→1	CK=PPPP
SE=1111		SE=0		SE=1111
SI=X011				SO=HHXX
PI=1	PO=Low=0			

Design for Testability 48

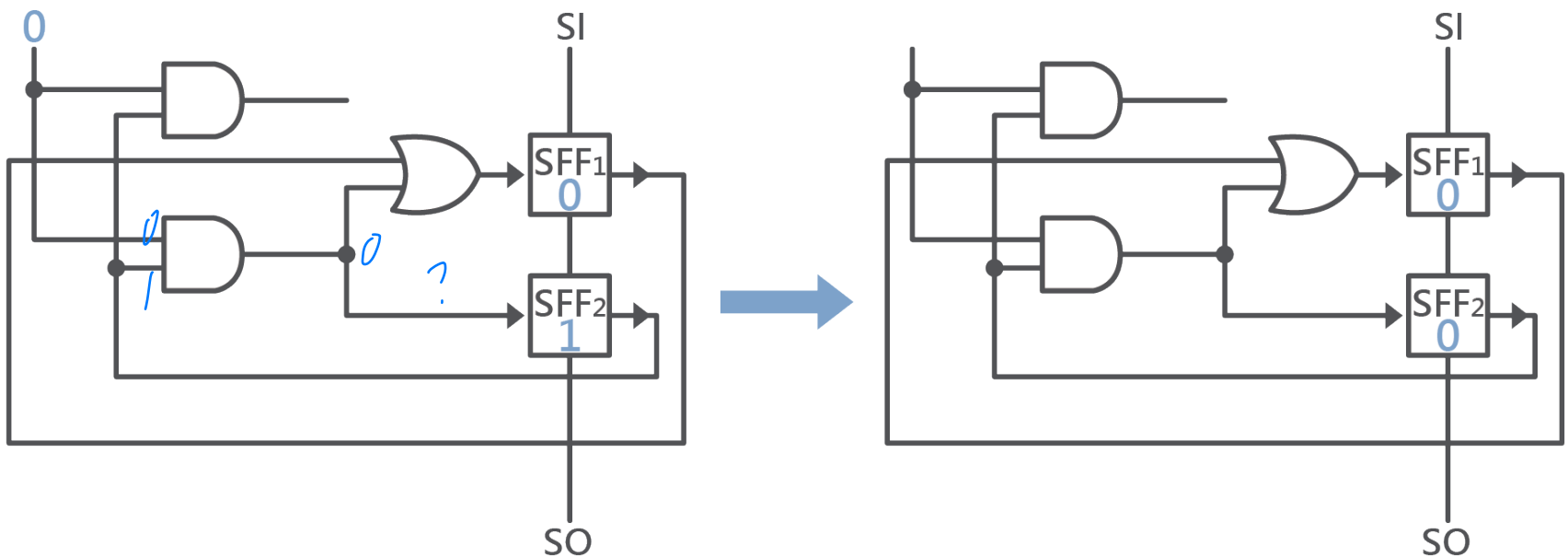
Scan DFT Overhead

- Performance Degradation
- Design overhead
- Hardware overhead
- Yield loss
- Power overhead

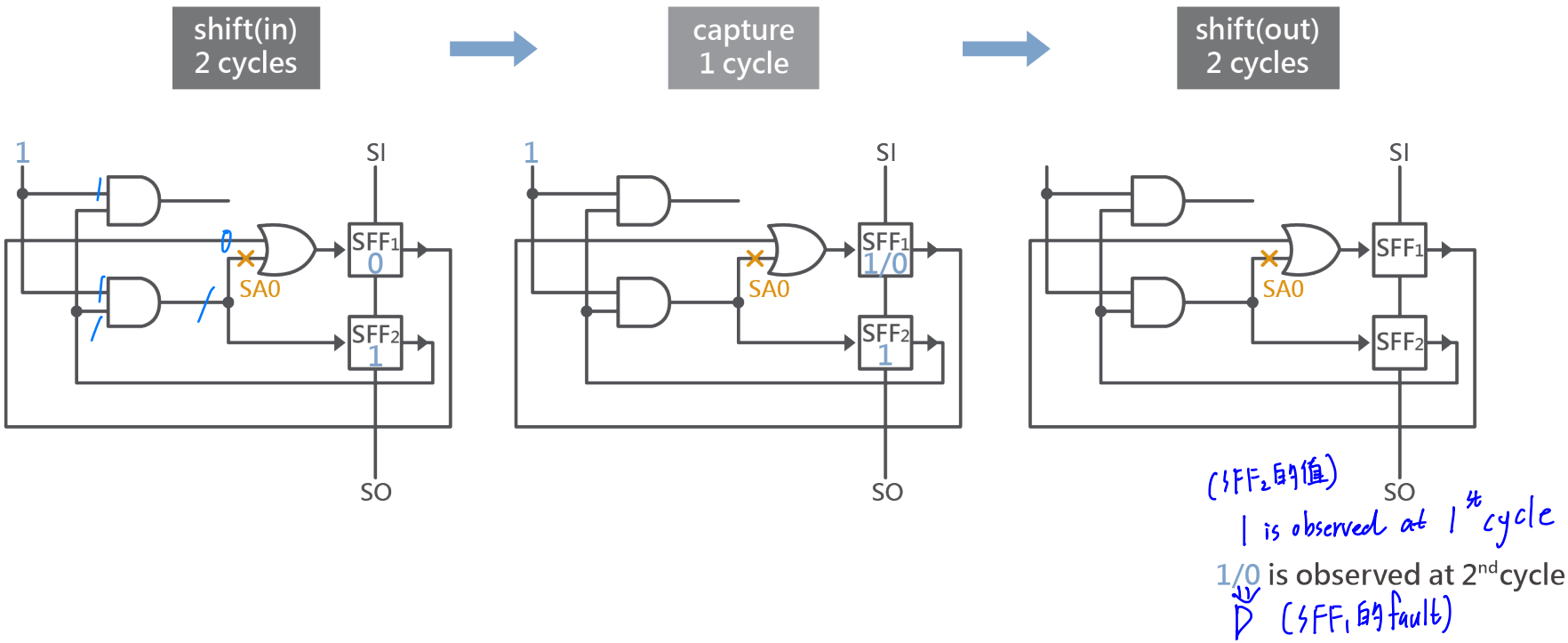


Example-Normal Mode

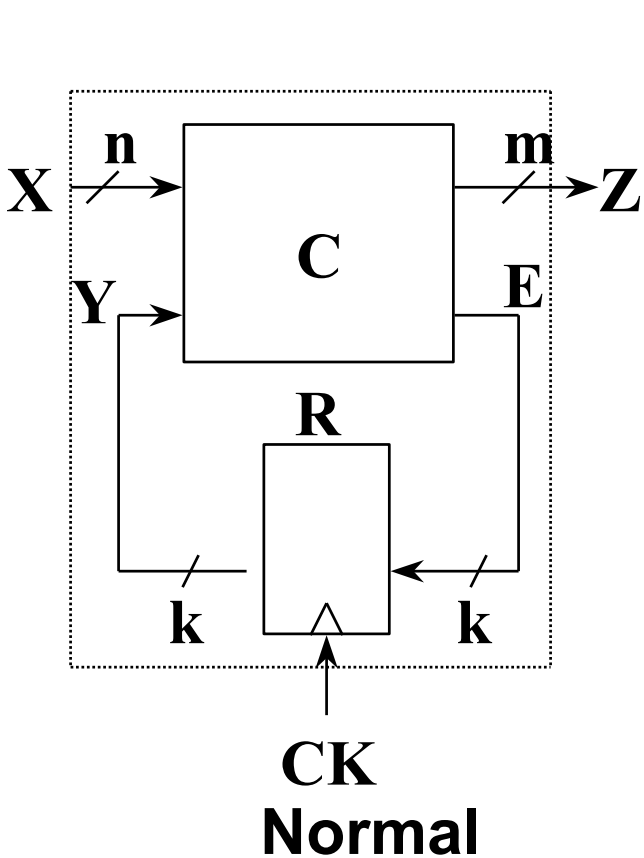
?有問題的地方

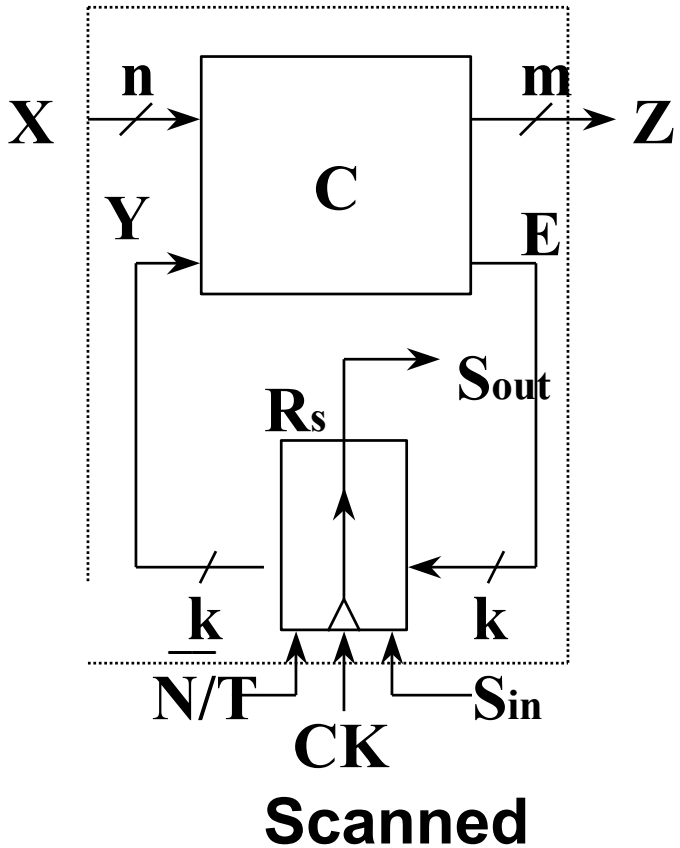


Example-Test Mode



Full Serial Integrated Scan

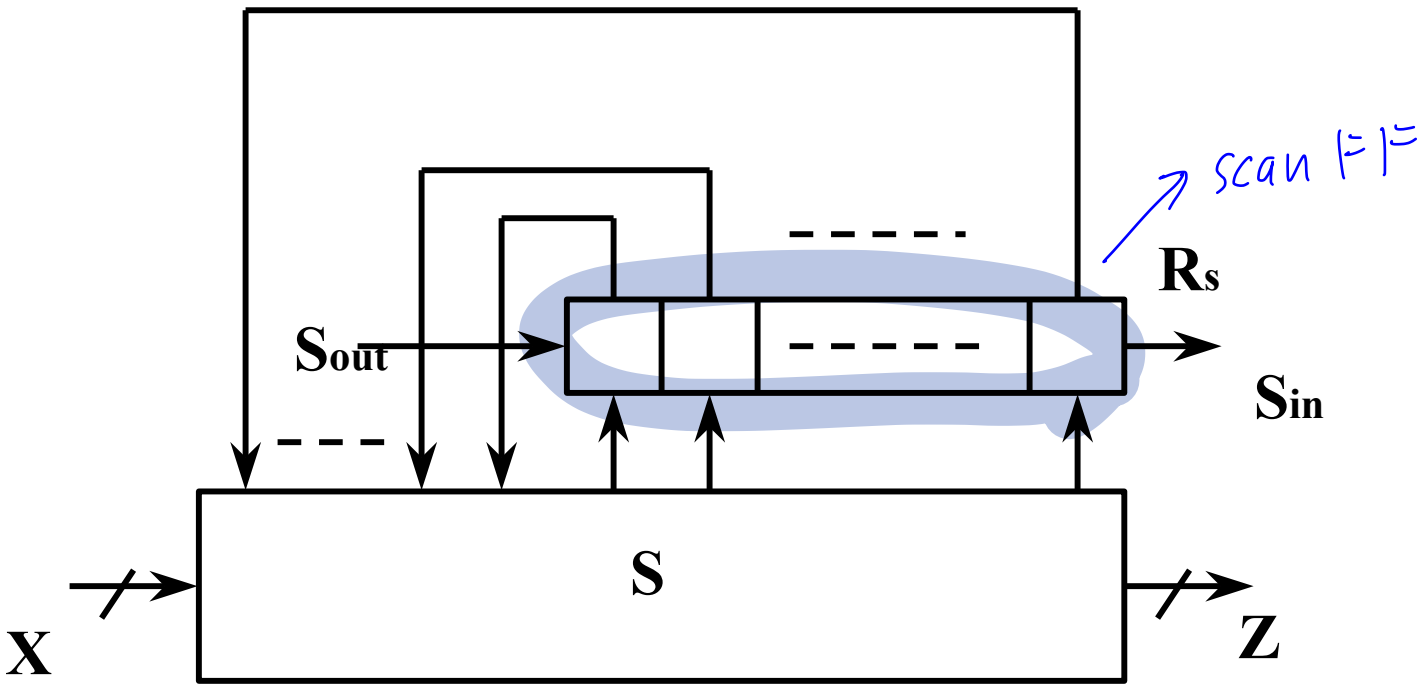




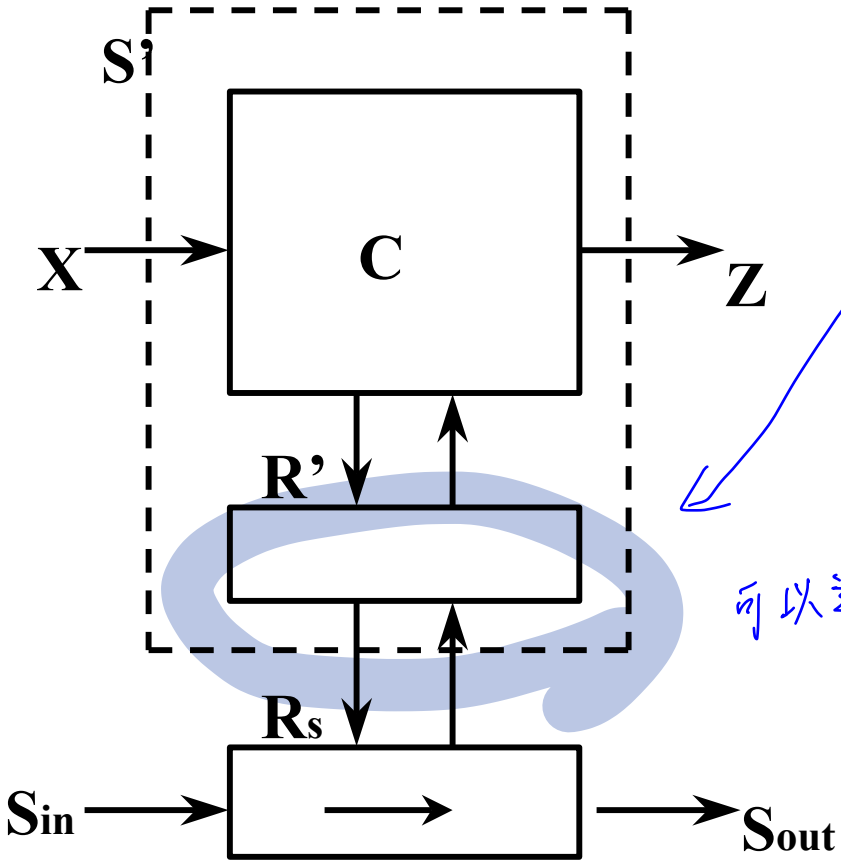
Sequential ATPG → Combinational ATPG

Isolated Serial Scan (Scan/set)

∵ Sin 及 Sout 共用 Scan FF ∴ 要將輸出都送完，才能接下次輸入



Full Isolated Scan (Structured)

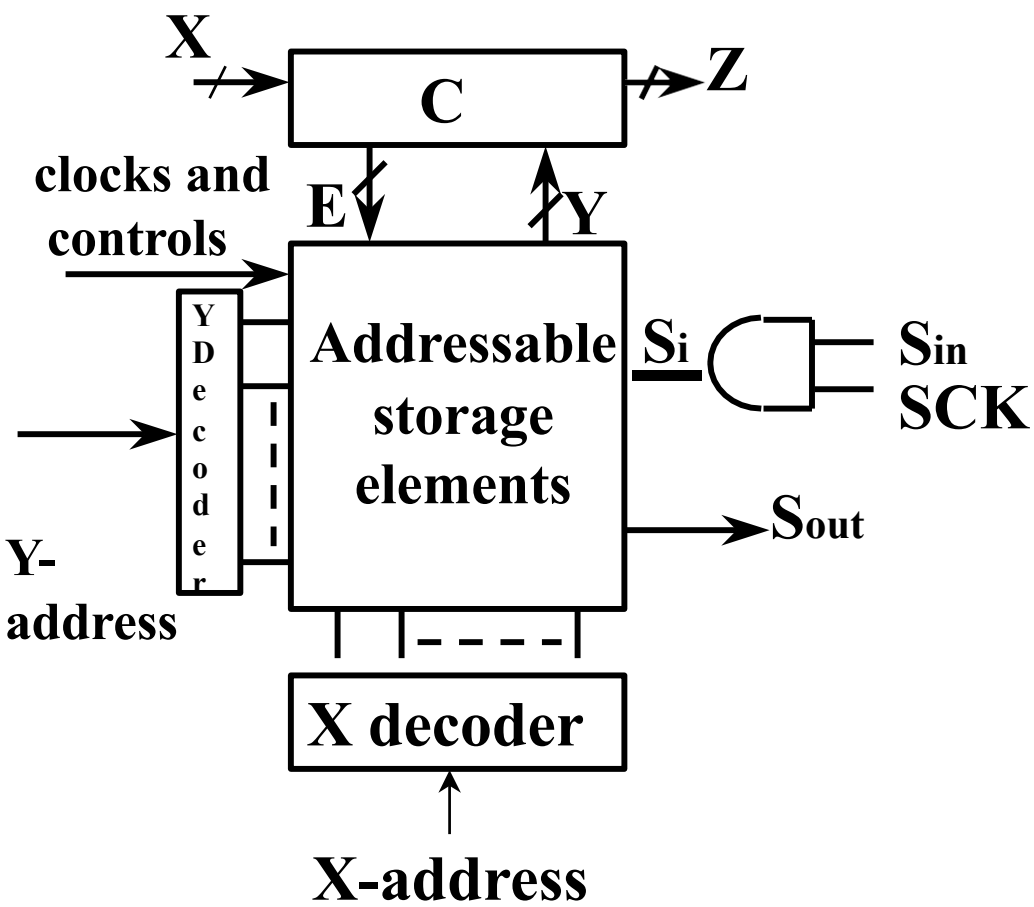


- Shadow register
- Real-time test support
- snapshot

可以進input進去，進output

→讓test time縮短

Random-Access Scan (Non serial-structured)

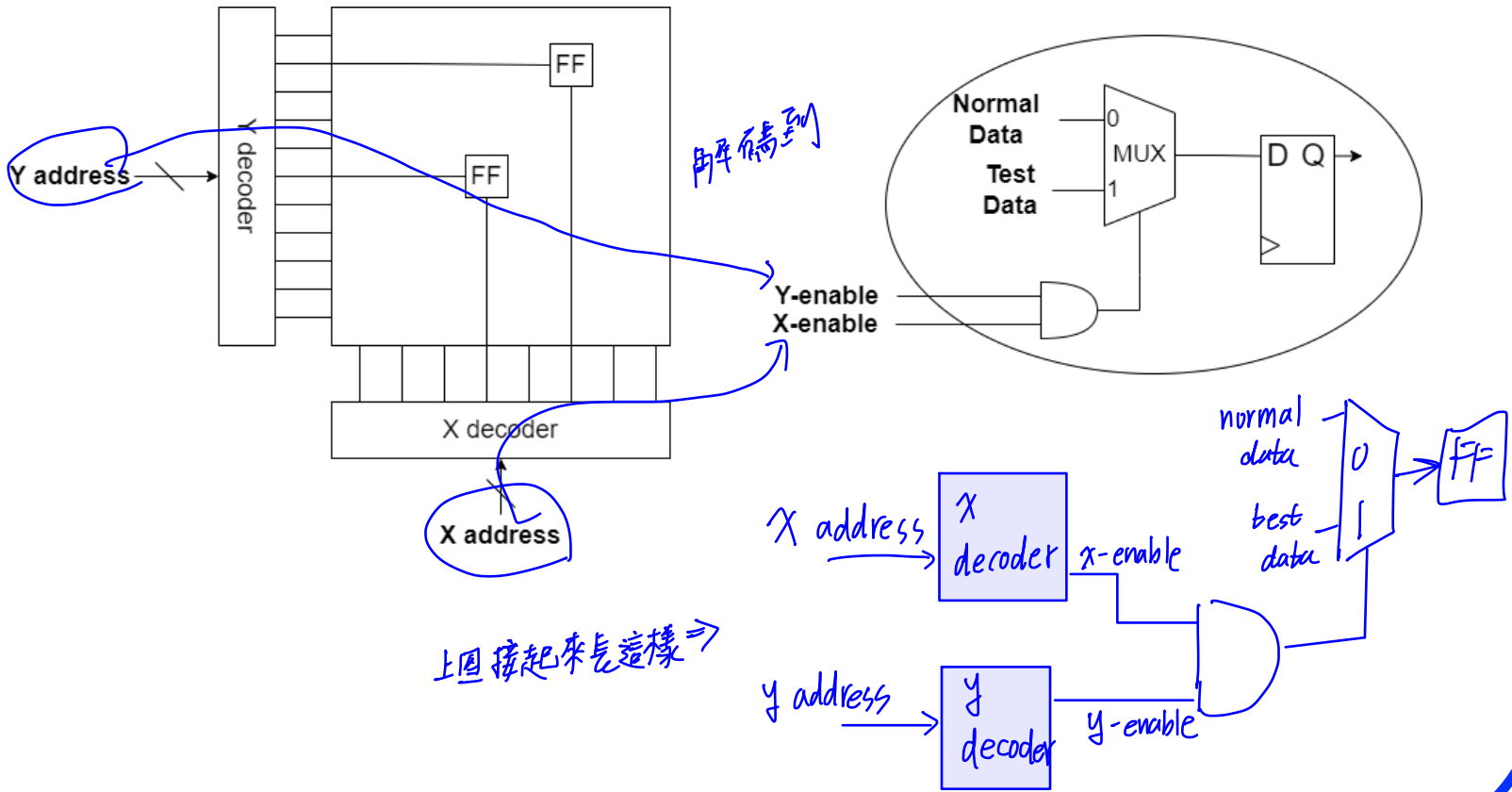


不用照順序存data

直接定址

- High area overhead
- Faster test application: only bit change
- Concept of crosscheck

Random-Access Scan (Non serial-structured)



Scan Cell Design

- Static / Dynamic
- Single / Double stages
- Latch / Flip-flop (Clocking Scheme)

Usually Two Operation Modes

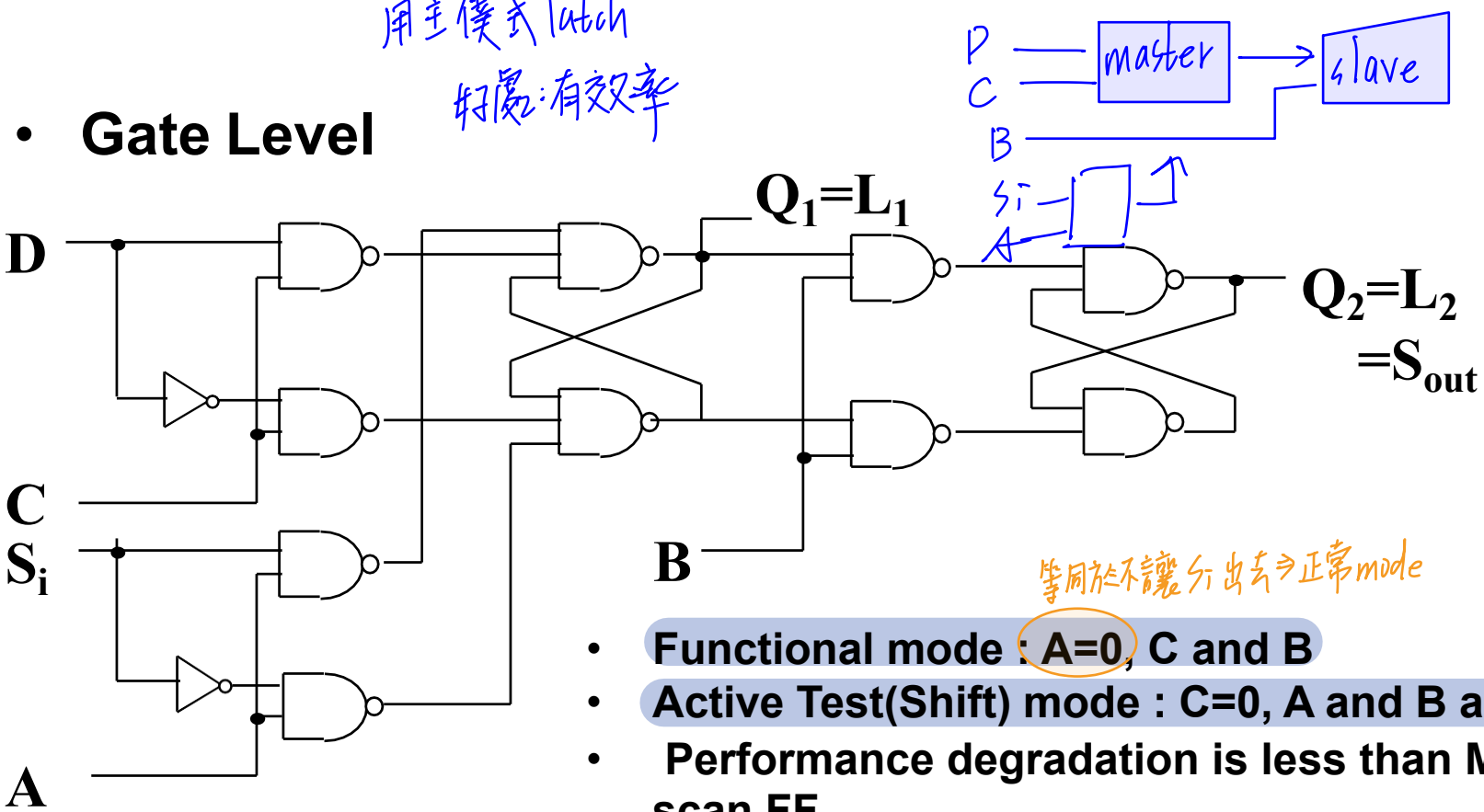
- Functional mode
- Shift mode

IBM LSSD Scan Cell

用主僕式 latch

好處：有效率

- Gate Level



等同於不讓 S_i 出去 ⇒ 正常 mode

- Functional mode : A=0, C and B
- Active Test(Shift) mode : C=0, A and B active
- Performance degradation is less than Mux-scan FF
- Non-overlap clock scheme

IBM LSSD Scan Cell

Advantages

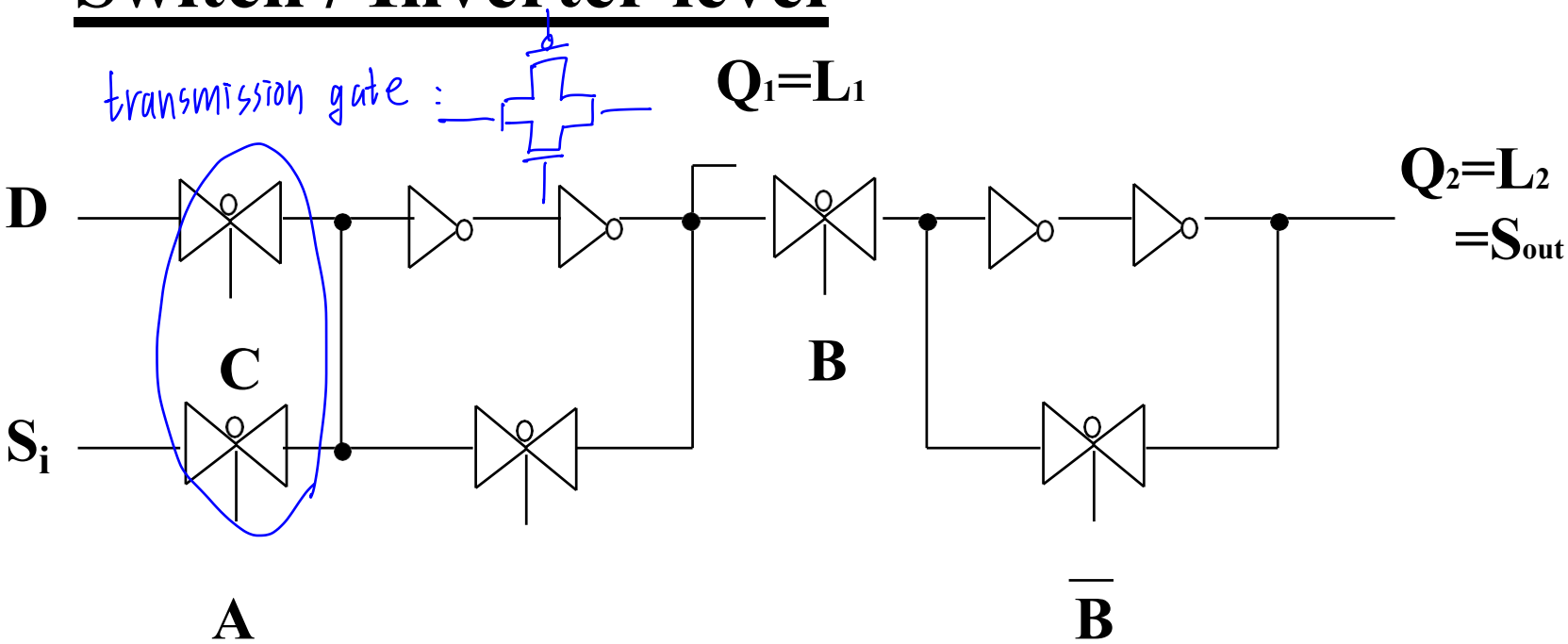
- It allows us to insert scan into a latch-based design.
- LSSD is guaranteed to be race free, which not case for the Muxed-D and Clocked-scan design.

Disadvantages

- It requires routing for the additional clocks, which increases routing complexity.

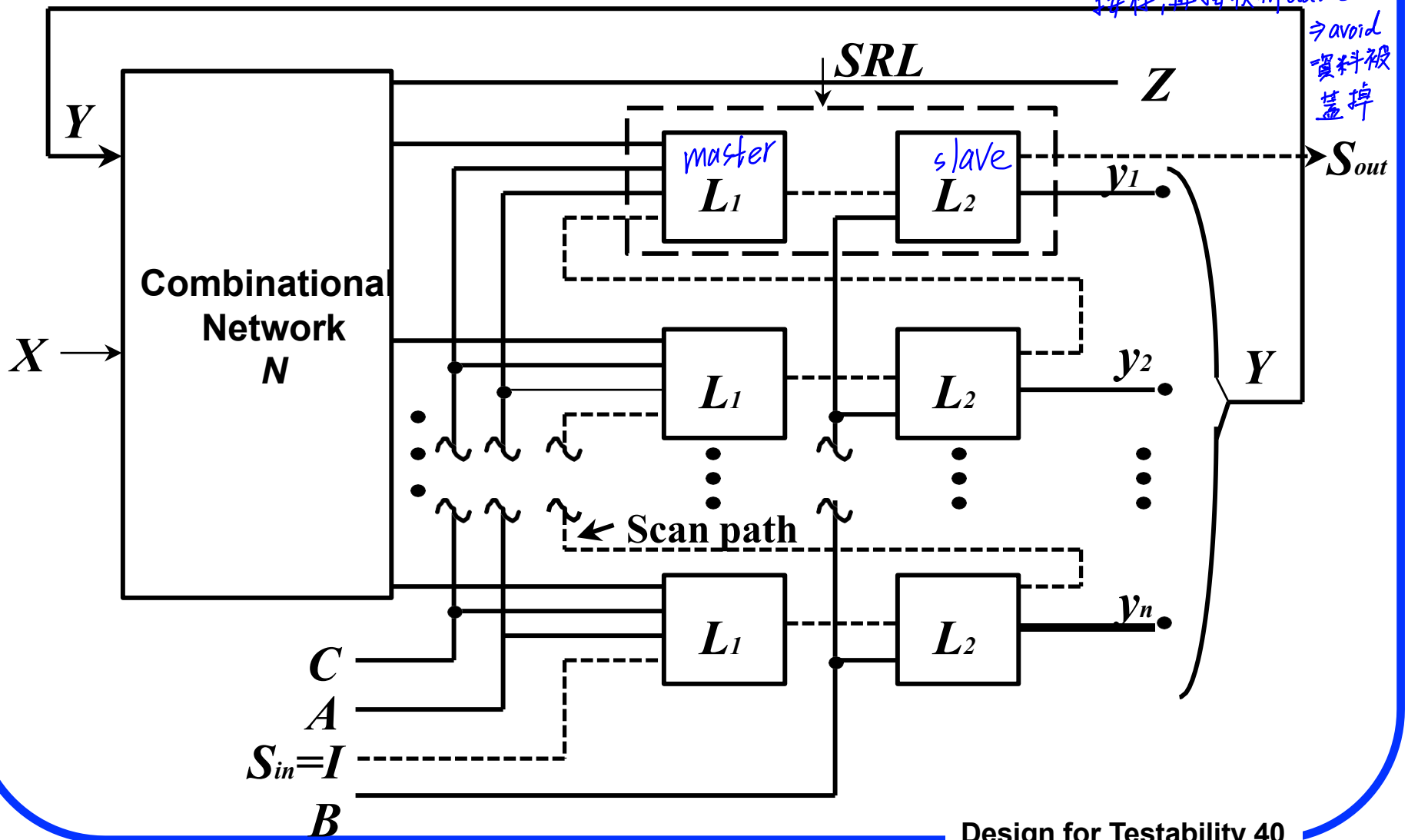
IBM LSSD Scan Cell (Cont.)

- **Switch / Inverter level**



LSSD Double-Latch Design

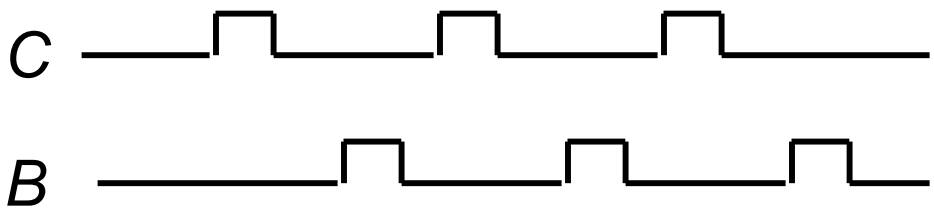
目的：讓速度变快，data送进来可以讓下个latch直接存，再接收新data
⇒avoid 資料被蓋掉



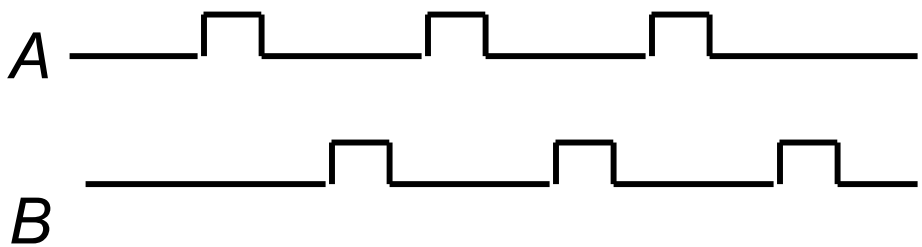
Clocking Scheme of LSSD Double-Latch

non-overlapping: avoid skew

Normal mode:

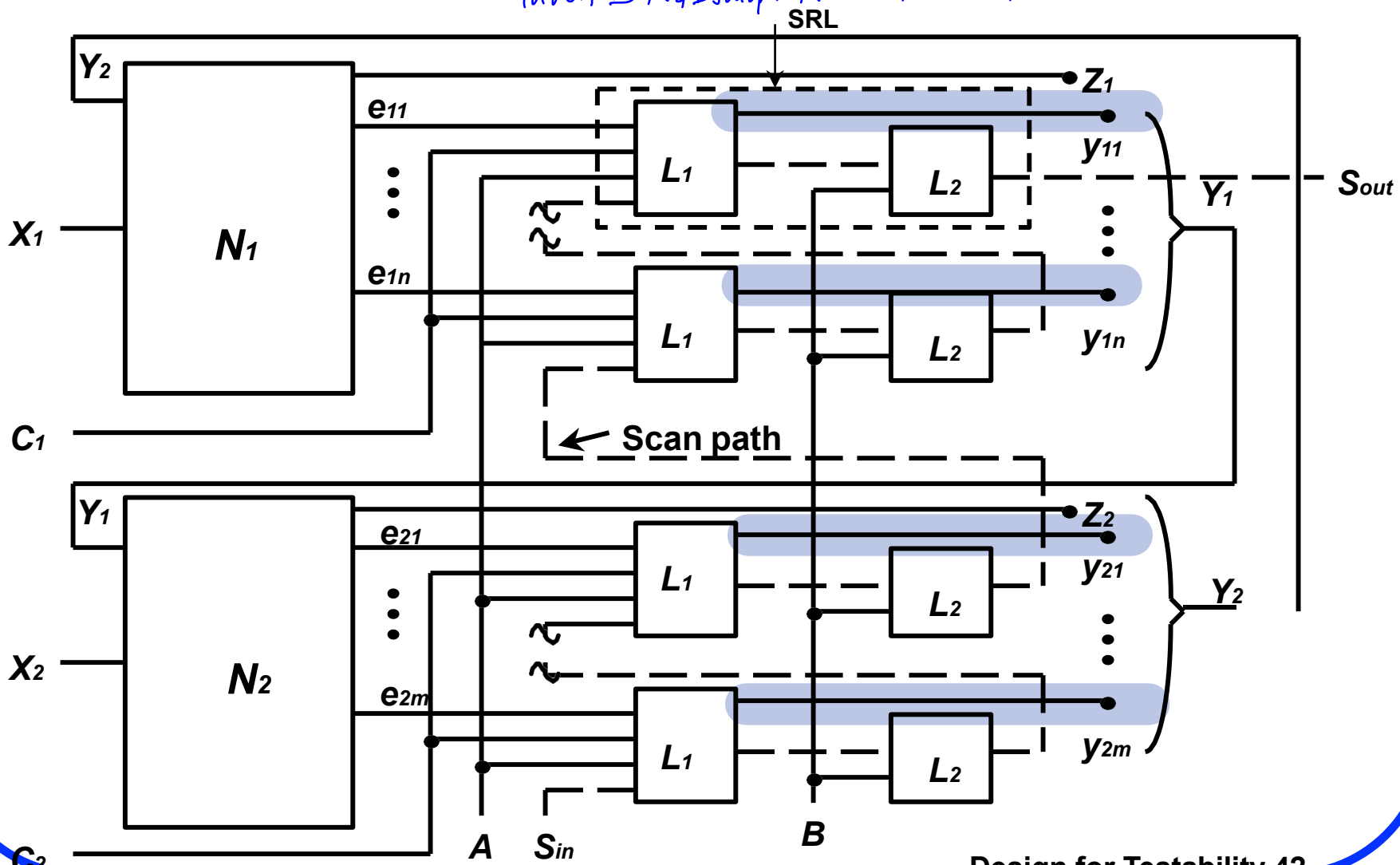


Test mode:

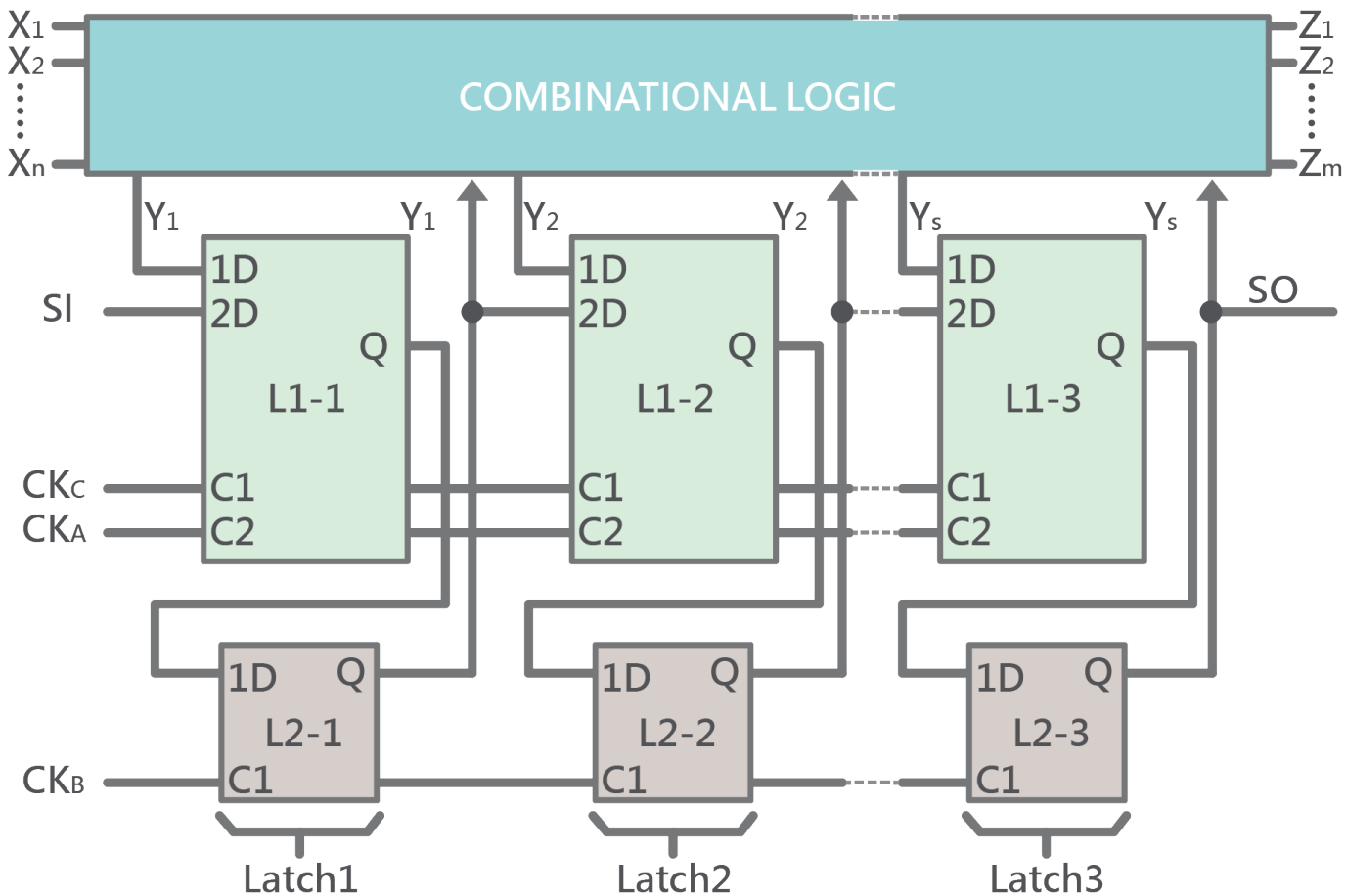


LSSD Single-Latch Design

latch 直接接到output，讓資料快速送出



Example

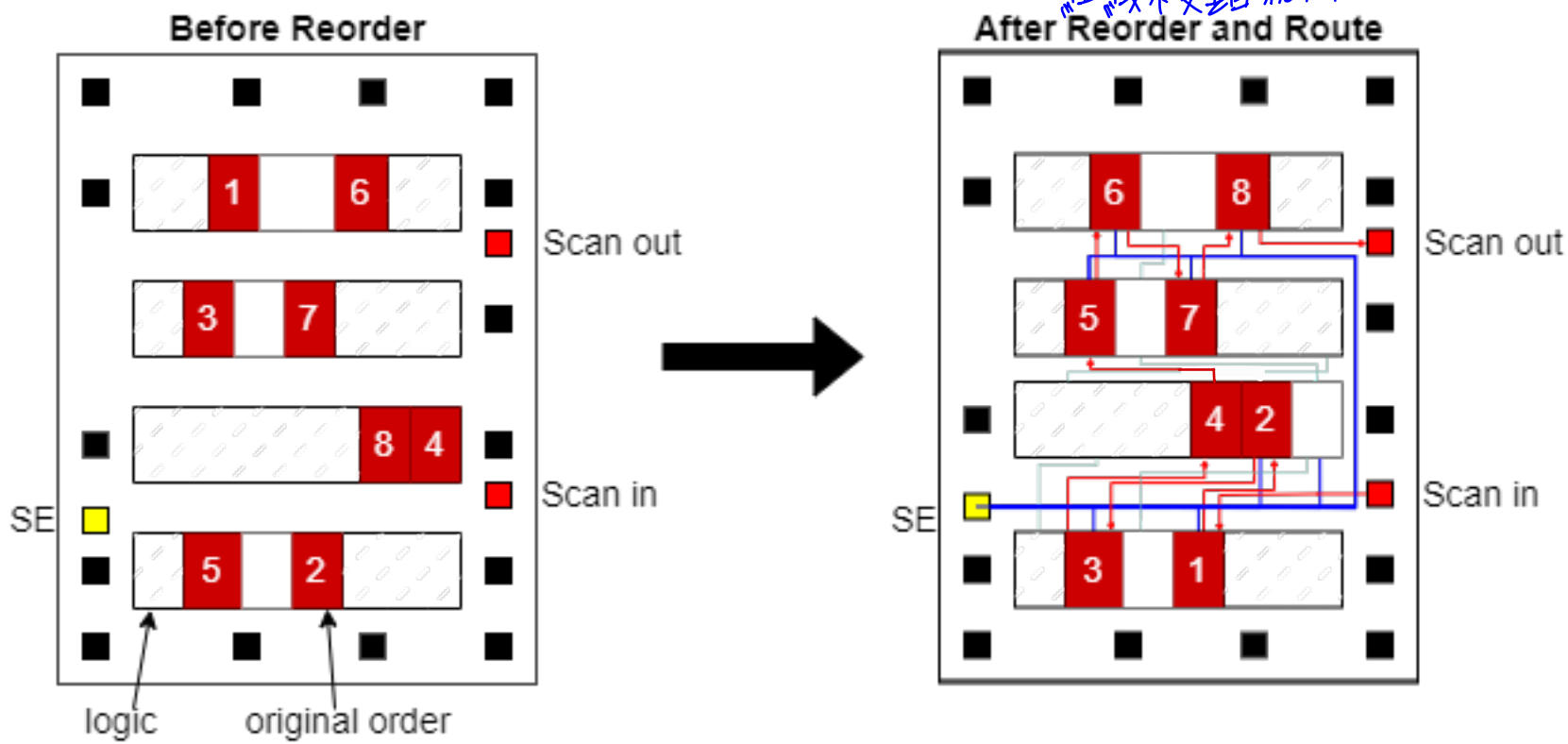

X1
X2
Xn
COMBINATIONAL LOGIC
Z1
Z2
Zm
Y1
Y1
Y2
Y2
Ys
Ys
SI
SO
1D
2D
Q
L1-1
L1-2
L1-3
CKC
CKA
C1
C2
1D
Q
L2-1
L2-2
L2-3
CKB
C1
Latch1
Latch2
Latch3

Scan Design Costs

- Area overhead
- Possible performance degradation
- Extra pins
- High test time
- Extra clock control

More Area OverHead

重新編排 register 位子，
紅線不交錯 就不用做多平面 → 省空間



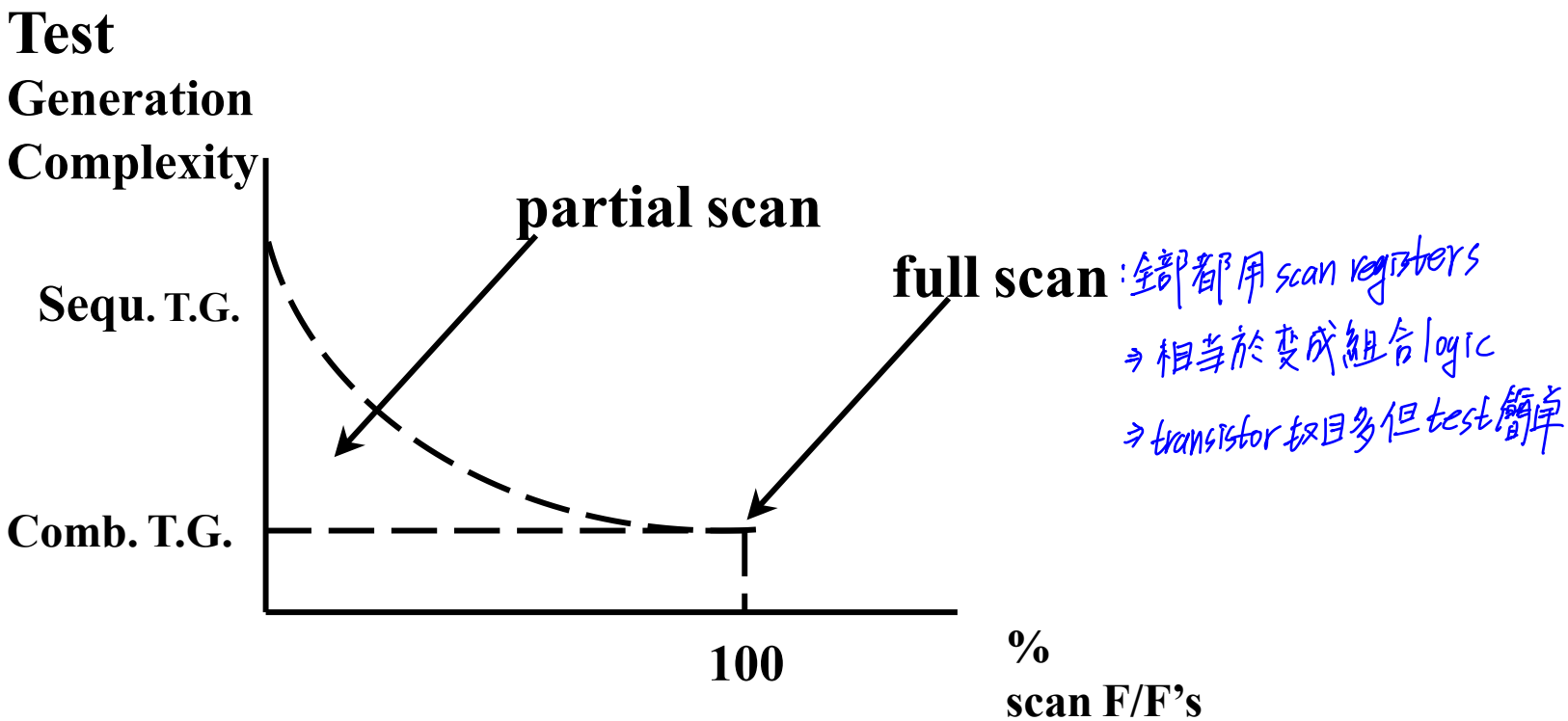
這種排序：混亂，面積變大

Advanced Scan Concepts

- **Partial scan (P.S.)**：有些变 scan register，有些不用
- **Multiple test session (M.T.S.)**：一个 scan chain 分成多段
- **Multiple scan chains (M.S.C.)** 各别 input
- **Broadcast scan chains (B.S.C)** 同一

Method	P.S.	M.T.S.	M.S.C.	B.S.C.
Area overhead	↓	same	same or ↑	same
Performance Degradation	↓	same	same	same
Extra pins	same	same	same or ↑	↓
Extra clock control	same	same	same	same
Test application time	↓	or ↑	↓	↓

Partial Scan: Only a subset of all flip-flops are scanned



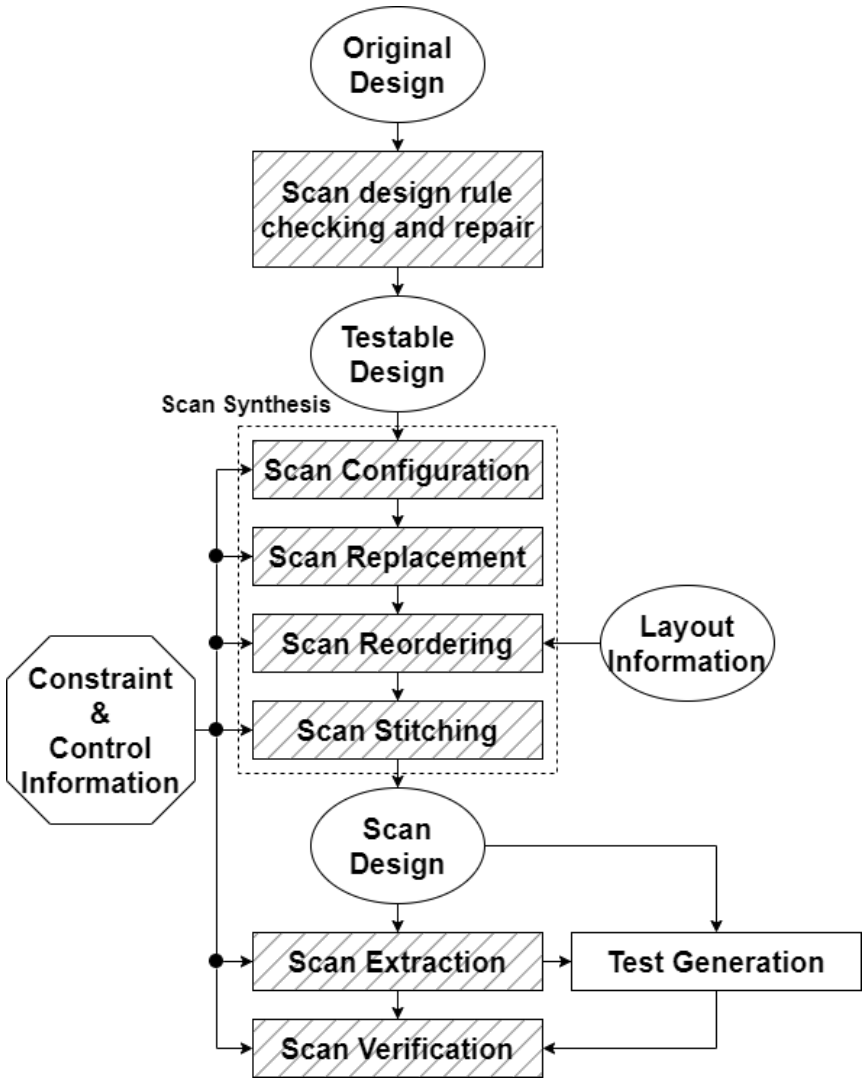
全部都用 scan registers
⇒ 相当於变成組合 logic
⇒ transistor 数目多但 test 簡单

- Trade-off between
  - –Area overhead
  - –Test generation complexity

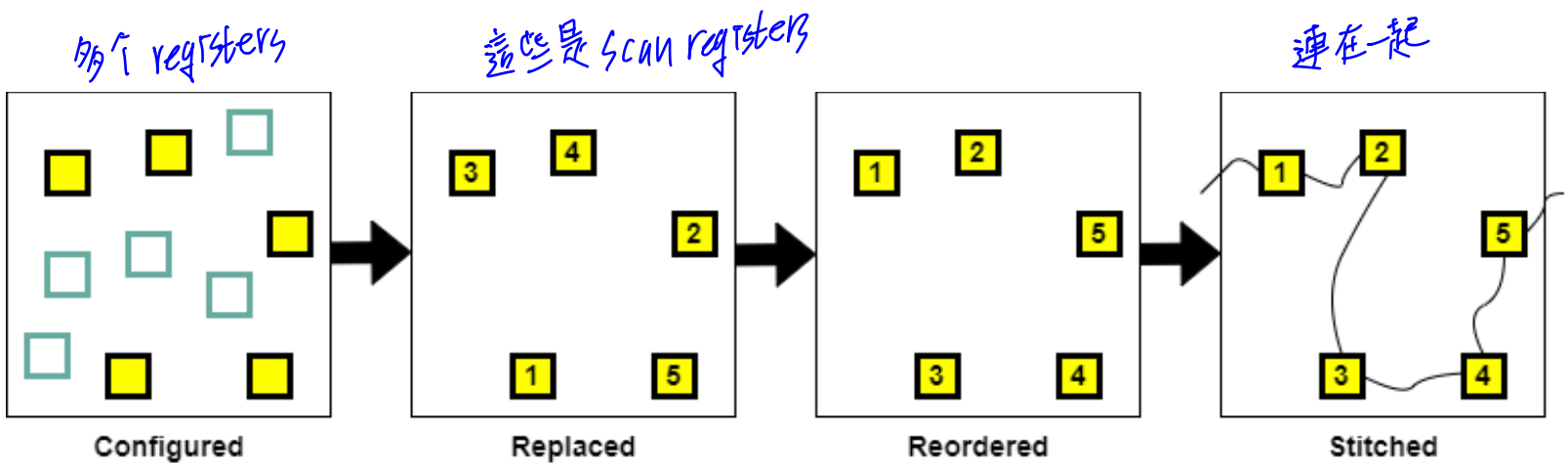
Partial Scan and Full Scan

- Full scan
  - -- Every flip-flop is scanable
  - -- More hardware overhead
  - -- Higher fault coverage
  - -- Longer test time ∵所有电路都串身关
  - -- Shorter ATPG time required ∵容易测
- Partial scan
  - -- Not every flip-flop is scanable
  - -- Less hardware overhead
  - -- Less fault coverage
  - -- Shorter test time
  - -- Longer ATPG time required

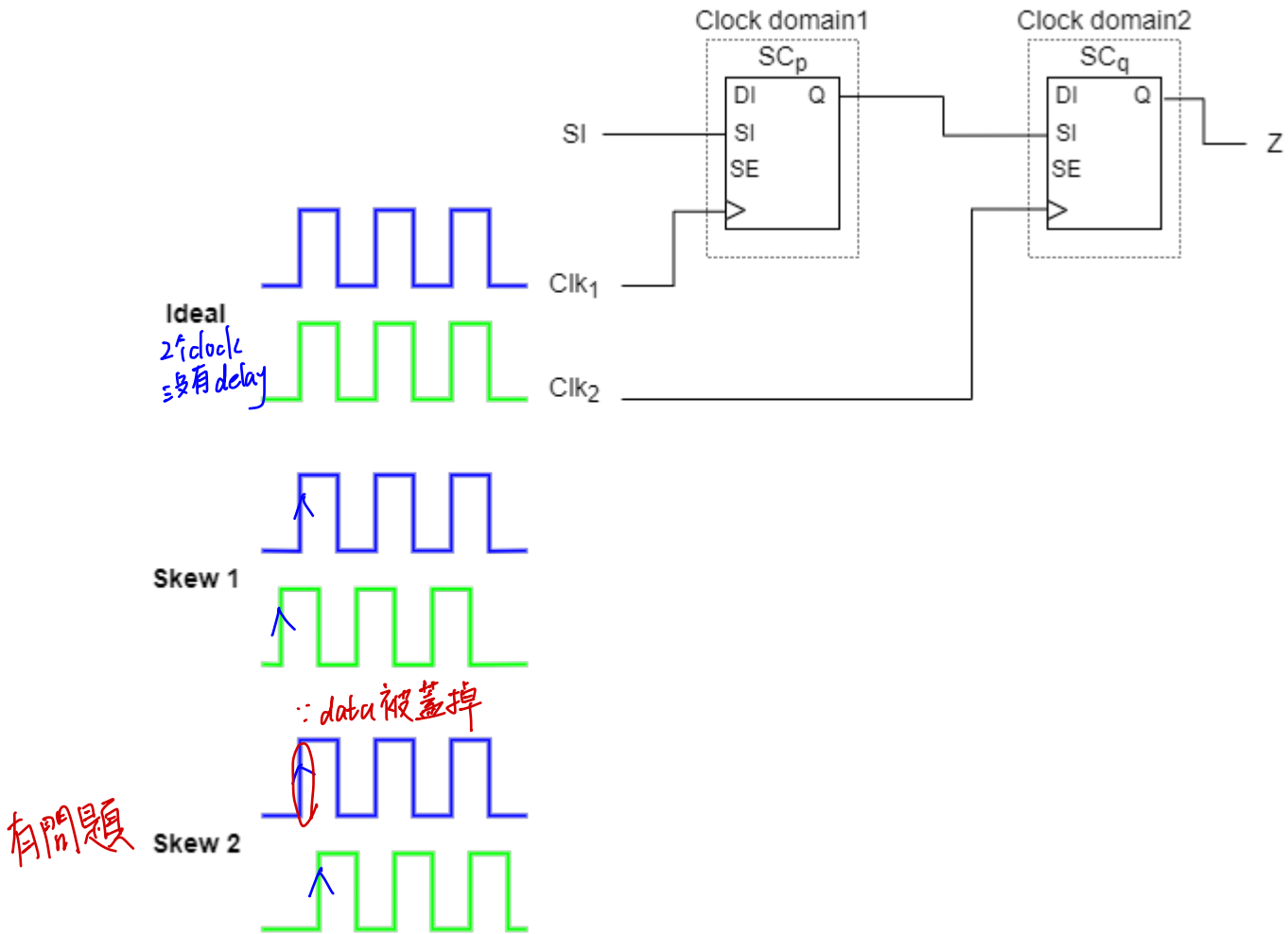
Scan Design Flow



Scan Register Selection



Clock Skew Between Two Clock Domains



Lock-up Latch