Instructions for ADS simulations:

With regard to the ADS simulations, consider the following issues in mind while designing the LNA.

1. Using the S-parameter file, you can design the matching networks at both the input as well as output. In case of designing the final layout, remember that you have to design the bias network for the transistor. When simulating the performance of the transistor with the bias network, you have to use the non-linear model of the transistor and not the S parameter file.
2. The transistor pad dimensions to be used in the layout are available in the transistor data sheet. You can design the pad and additional transmission lines for the purpose of designing the layout and then convert to schematic and work interchangeably. The S-parameters for the biased non-linear model and the transistor S2P file should be more or less the same.
3. For the DC block and bypass capacitors, use MURATA GQM / GRM series. Contact me for values and I can check the availability of the capacitors.
4. Once the layout is designed, see to that the amplifier is designed keeping in mind the overall dimensions of the board (85*70 mm) and that necessary holes are provided as given in the ground plate document to connect the amplifier board to the ground plate.
5. Once the final layout is generated, save it as a new file and delete the components, i.e. capacitors, resistors, etc. (Only the transmission lines should be remaining). Then merge the connected components and flatten them. Keep in mind that transmission lines should be in the same layer (cond). Mark the edges of the design using small metal lines to indicate the boundary.

Note: Before generating the final layout for manufacturing (i.e. step 6), contact me to show the results, and further instructions will be provided on generating the layout.

The deadline for the layout is postponed to 23/04/2014. I am out of office from 14/04/2014 13:00 – 17/04/2014 but I can answer your queries by email.