Low Noise Amplifiers for 1600 MHz and 1900 MHz Low Current, Self-biased Applications using the ATF-35143 Low Noise PHEMT

Application Note 1174

Introduction

Avago Technologies' ATF-35143 is a low noise PHEMT designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. The ATF-35143 is housed in a 4-lead SC-70 (SOT-343) surface mount plastic package. The 400-micron gate width ATF-35143 provides very high stable gain in the L band frequency range with the added benefit of being able to be self biased. This allows the use of a single polarity power supply making it ideal for low current battery applications.

The ATF-35143 is described in two low noise amplifiers. The first amplifier is designed for 1600 MHz for use in Iridium low noise amplifiers or other similar applications. The 1900 MHz amplifier is designed for use in PCS and other related markets. Both amplifiers were designed for a V_{ds} of 2 V and I_d of 10 mA. They are characterized at both 10 and 5 mA. The circuits are designed for use with 0.032-inch thickn FR-4 printed circuit board material. The amplifiers make use of low cost miniature wirewound and multilayer chip inductors for small size. When biased at a V_{ds} of 2 V and and I_{ds} of 10 mA, the 1600 MHz ATF-35143 amplifier will provide 18 dB gain, 1 dB noise figure and an output intercept point (IP3) of +20 dBm.

Biasing Options and Source Grounding

Passive biasing schemes are generally preferred for their simplicity. One method of passive biasing requires the source leads be direct DC grounded. A negative voltage is applied to the gate through a bias de-coupling network. The gate voltage is then adjusted for the desired value of drain current. The gate voltage required to support a desired drain current, I_d, is dependent on the device's pinchoff voltage, V_p, and the saturated drain current, I_{dss}. I_d is calculated with the following equation.

$$V_{gs} = V_p \left(1 - \sqrt{I_d / I_{dss}}\right)$$

As an example, for the ATF-35143 for a I_d of 10 mA, I_{dss} of 60 mA and a V_p of -0.5 V, the required V_{gs} is -0.296 V.

Another option for passive biasing is to raise the source above ground with a resistor and DC ground the gate. This configuration forces the gate negative with respect to the source, thereby allowing the drain current to be set with the source resistor. The source resistor, R_s, is equal to $-V_{gs}/I_d = 29.6\ \Omega$. The source resistor is then AC bypassed with a capacitor with a low impedance at the desired operating frequency. Both the DC grounded and bypassed source resistor technique of AC grounding the source have some inductance associated with the connection. Each source bypass capacitor can have up to 0.7 to 1 nH of associated lead inductance which can be used to an advantage in the RF design. Even the DC grounded source leads have some finite length associated with the trace which correlates to some equivalent inductance.

The use of a controlled amount of source inductance can often be used to enhance LNA performance. Usually only a few tenths of a nanohenry or at most a few nanohenrys of inductance is required. This is effectively equivalent to increasing the source leads by only 0.050 inch or so. The effect can be easily modeled using one of the Avago/EESOF microwave circuit simulators. The amount of source inductance that can be safely added depends on the device. Very short gate width devices such as the 200-micron gate width ATF-36163 can tolerate very little source inductance. Usually the inductance associated with just two plated through holes through 0.031-inch thick printed circuit board is all that the device can tolerate. Hence the smaller gate width devices such as the ATF-36163 are typically used as low noise amplifiers for C and Ku band applications such as TVRO and DBS.

The usual side effect of excessive source inductance is very high frequency gain peaking and resultant oscillations. The larger gate width devices have less high frequency gain and therefore the high frequency performance is not as sensitive to source inductance as a smaller device would be. The ability of the 400-micron gate width ATF-35143 to tolerate greater source inductance allows the designer to take advantage of self biasing thereby only necessitating a single positive power supply.

LNA Design

The amplifiers were designed for a V_{ds} of 2 V and an I_{ds} of 10 mA. Typical power supply voltage, V_{dd}, would be in the 2.25 to 2.7 V range. The generic demonstration board shown in Figure 1 is used for both designs. The board gives the designer several design options for both the RF circuitry and biasing options.

The demonstration board was designed such that the input and output impedance matching networks can be either lumped element networks or etched microstrip networks for lower cost. Either low-pass or high-pass structures can be generated based on system requirements. The demonstration board also allows the FET to be either self biased or with grounded sources the FET can be biased with a negative voltage applied to the gate terminal.

The demonstration board is etched on 0.031" thick FR-4 material for cost considerations.

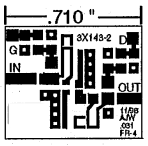

Figure 1. 1X Artwork for the ATF-35143 low noise amplifier.

Table 1. Component Parts List for the 1600 MHz ATF-35143 Amplifier.

Number	Description
C1	1.3 pF chip capacitor
C2, C6	8.2 pF chip capacitor
C3, C4	30 pF chip capacitor
C5	4.7 pF chip capacitor
C7	10000 pF chip capacitor
L1	3.9 nH inductor (Toko LL1608-F3N9K)
L2, L3	Use minimal inductance for L2 and L3. Capacitors C3 and C4 are placed as close as possible to the device source leads.
L4	4.7 nH inductor (Toko LL1608-F4N7K)
Q1	Avago Technologies ATF-35143 PHEMT
R1	50 Ω chip resistor
R2	R2 consists of two resistors in parallel, one on each source lead. Set for desired drain current. See text.
R3	12 Ω chip resistor
R4	24 Ω chip resistor
Zo	50 Ω Microstrip line

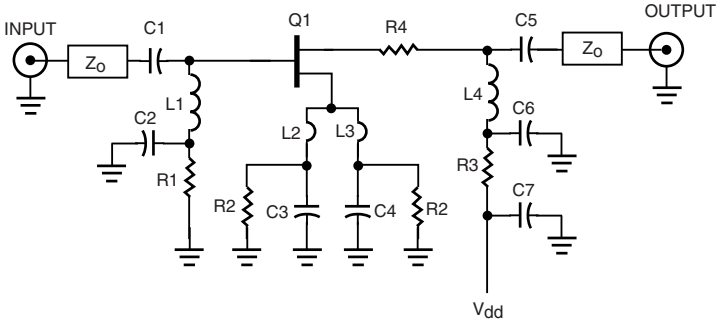

Figure 2. Schematic diagram of the self biased 1600 MHz ATF-35143 amplifier.

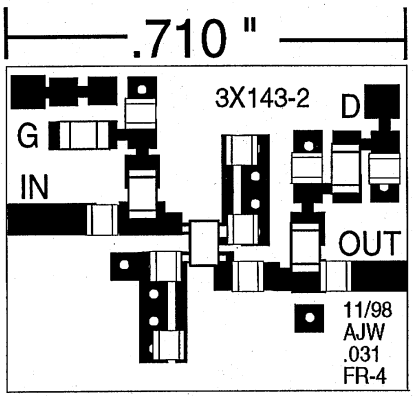

Figure 3. Component placement drawing for the 1600 MHz ATF-35143 low noise amplifier.

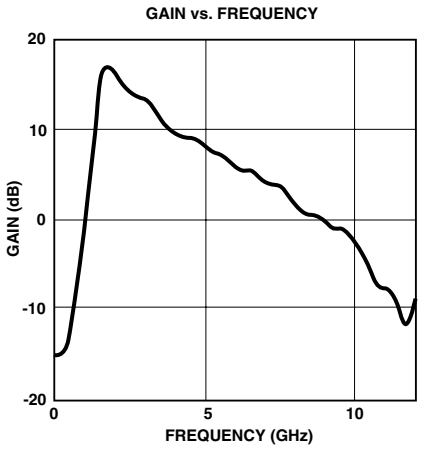

Figure 4. Wide-band gain plot of ATF-35143 amplifier using minimal source inductance.

Design of the 1600 MHz ATF-35143 Amplifier

The schematic diagram describing the 1600 MHz self biased amplifier is shown in Figure 2. The parts list for the first amplifier is shown in Table 1. The demonstration board as modified is shown in Figure 3. The modifications are discussed in the next section.

The amplifier uses a high-pass impedance matching network for the noise match. The high-pass network consists of a series capacitor (C1) and a shunt inductor (L1). The high-pass topology is especially advantageous in rejecting signals below the frequency of interest. L1 also doubles as a DC return for the gate lead of the PHEMT. R1 is inserted in series with inductor L1 to provide some resistive loading of the device at low frequencies, i.e. 500 MHz and lower. Elimination of resistor R1 can have a significant effect on low frequency stability. Capacitor C2 provides an effective RF bypass at the frequency of operation across resistor R1. C1 also doubles as a DC block. The Q of L1 is extremely important from the standpoint of circuit loss which will directly relate to noise figure. The Toko LL1608-F3N9K is a small multilayer chip inductor with a rated Q of 32 at 800 MHz. Lower element Qs may increase circuit noise figure and should be considered carefully. Conversely, higher Q airwound coils could lower the amplifier noise figure by several tenths of a dB. This network has been optimized primarily for noise figure with secondary emphasis on input return loss.

The amplifier uses a similar high-pass structure for the output impedance matching network. L4 and C5 provide the proper match for best output return loss and power output. L4 also doubles as a means of inserting voltage to the drain. Resistor R4 has been added to improve in-band stability by reducing gain about a dB. Another side effect of resistor R4 is a reduction in IP3 of about a dB. Resistor R3 and capacitor C7 provide a low frequency termination for the device.

The original demonstration board incorporates additional series microstriplines in both the input and output impedance matching networks. They are not required for this amplifier design and can be removed from the demonstration board. They should be replaced with a small 0.040" wide piece of etch.

Source inductance at L2 and L3 is commonly used to optimize amplifier performance. The inductance can be in the form of very short transmission lines or the inductance associated with a source bypass capacitor. The equivalent inductance acts as series feedback. The amount of series feedback has a dramatic effect on in-band and out-of-band gain, stability and input and output return loss. The amplifier demonstration board is designed such that the amount of source inductance is variable. For the case of DC grounding the source leads, each source lead is connected to a microstrip line which can be connected to a ground pad at any point along the line. For minimal inductance, the source lead pad is connected to the ground pad with a very short piece of etch at the point closest to the device source lead. For the self biased amplifier, the sources must be bypassed to ground with capacitors C3 and C4. The capacitors should be placed as close as possible to the device, thereby minimizing any additional source inductance. The two resistors each designated as R2 are used in parallel to set the drain current. Position one resistor on each end of the source lead pad. This provides some de-Qing of the additional source lead etch which is not being used for RF purposes. If there is any remaining unused source lead pad, it should be removed by cutting off the unused etch. On occasion, the unused etch which looks like an open circuited stub has caused high frequency oscillations.

For 10 mA drain current, each R2 should be approximately 47 Ω so that the equivalent parallel resistance is approximately 24 Ω. For 5 mA drain current each resistor should be approximately 270 Ω.

Determining the Optimum Amount of Source Inductance

Adding additional source inductance has the positive effect of improving input return loss and low frequency stability. A potential downside is reduced low frequency gain, however, decreased gain also correlates to higher input intercept point. The question then becomes how much source inductance can one add before one has gone to far?

For an amplifier operating in the 2 GHz frequency range, excessive source inductance will generally manifest itself in the form of a gain peak in the 6 to 13 GHz frequency range. Normally the high frequency gain rolloff will be gradual and smooth. Adding source inductance begins to add bumps to the once smooth gain roll-off. The source inductance, while having a degenerative effect at low frequencies, is having a regenerative effect at higher frequencies. This shows up as a gain peak in S21 and also shows up as input return loss S11 becoming more positive. Some shift in upper frequency performance is OK as long as the amount of source inductance is fixed and has some margin in the design so as to account for S21 variations in the device. A wide-band plot of S21 for an amplifier using the 400-micron ATF-35143 amplifier using DC grounded source leads is shown in Figure 4. The plot shown in Figure 4 represents an amplifier that uses minimal source inductance and has a relatively smooth gain roll-off at the higher frequencies.

The wideband gain plot shown in Figure 5 is for the same amplifier that uses additional source inductance to improve low frequency stability and input return loss. Its effect can be seen as some gain peaking in the 6 GHz frequency range. This is not a concern unless additional source inductance is added. Excessive source inductance will cause gain to peak at the higher frequencies and may even cause the input and output return loss to be positive. Adding excessive source inductance will most likely generate a gain peak at about 6 GHz and sometimes in the 12 to 13 GHz frequency range. Gain peaks could approach 20 to 30 dB. Its effect can be seen in Figure 6. The end result is poor amplifier stability especially when the amplifier is placed in a housing with walls and a cover. The wide-band gain plot does give the designer a good overall picture as to what to look for when analyzing the effect of excessive source inductance. Keep in mind that source inductance can be in the form of additional source lead length or the inductance associated with the source bypass capacitor. Most high quality chip capacitors have between 0.3 and 1.5 nH of equivalent lead inductance. A nanohenry of source inductance can have a major effect on device operation and its effect should be modeled accurately.

1600 MHz ATF-35143 Amplifier Performance

The amplifier is tested at a V_{ds} of 2 V and at both 5 and 10 mA I_{ds}. The noise figure of the amplifier is shown in Figure 7. Noise figure is slightly under 1 dB at 1600 MHz at 10 mA I_{ds}. Noise figure increases to 1.1 dB at I_{ds} = 5 mA. Gain versus I_{ds} is shown in Figure 8. At I_{ds} = 10 mA, the gain peaks at 18 dB at 1600 MHz. Decreasing I_{ds} = 5 mA reduces gain to 16 dB.

Measured input return loss is shown in Figure 9. The input return loss at 1.6 GHz is 8.3 dB with I_{ds} = 10 mA. Decreasing the value of the input capacitor C1 from 1.3 pF to 1.0 pF improves the input return loss from 8.3 dB to 12 dB with a 0.4 dB degradation in noise figure at 1600 MHz. Decreasing I_{ds} to 5 mA results in the input return loss decreasing to about 6 dB.

Output return loss versus I_{ds} is shown in Figure 10. At 10 mA I_{ds} the output return loss measures 18.4 dB. Reducing the I_{ds} to 5 mA reduces the output return loss to about 10 dB.

The amplifier output intercept point OIP3 was measured at +20 dBm at a DC bias point of 2 V V_{ds} and an I_d of 10 mA. Output IP3 was measured at +14 to +15 dBm at I_d = 5 mA.

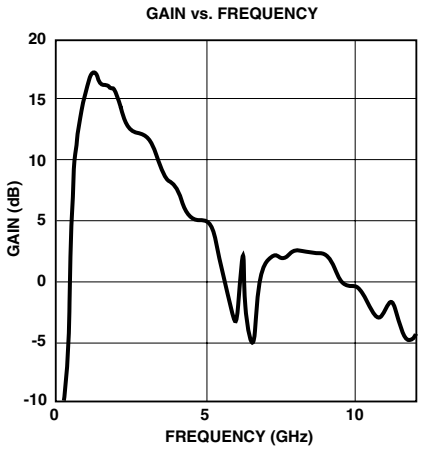

Figure 5. Wide-band gain plot of the ATF-35143 amplifier with an acceptable amount of source inductance.

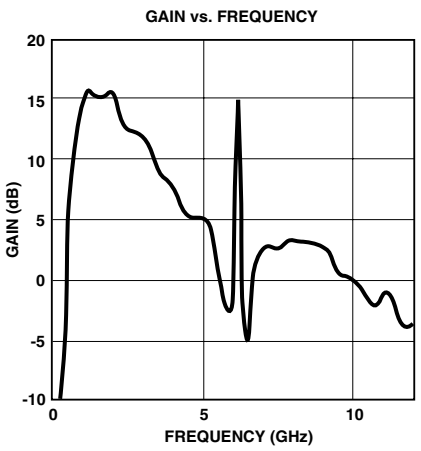

Figure 6. Wide-band gain plot of the ATF-35143 amplifier with an unacceptable amount of source inductance producing undesirable gain peaking.

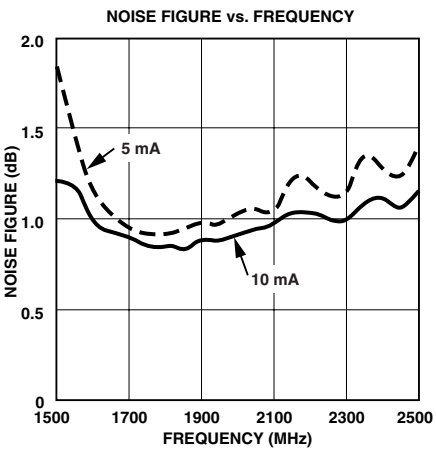

Figure 7. 1600 MHz amplifier noise figure vs. frequency.

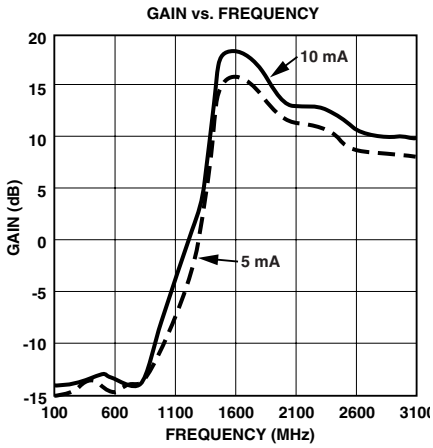

Figure 8. 1600 MHz amplifier gain vs. frequency.

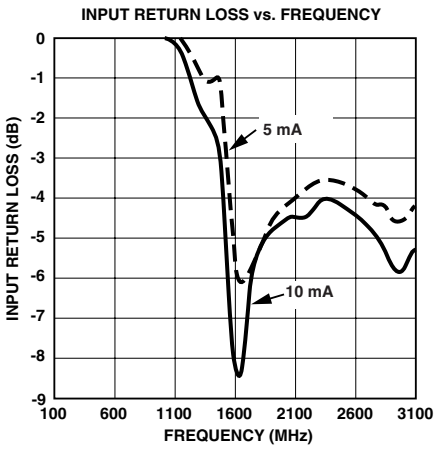

Figure 9. 1600 MHz amplifier input return loss vs. frequency.

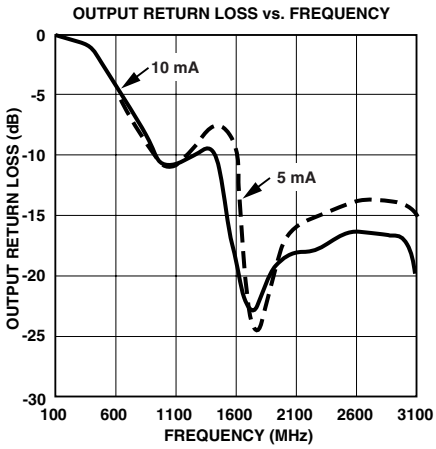

Figure 10. 1600 MHz amplifier output return loss vs. frequency.

Design of the 1900 MHz ATF-35143 Amplifier

The 1900 MHz amplifier uses the same circuit diagram as the 1600 MHz amplifier with slight changes in component values. The revised parts list is shown in Table 2. Component placement is similar to the 1600 MHz amplifier as shown in Figure 3.

The circuit topology for the 1900 MHz amplifier is similar to the 1600 MHz amplifier discussed in the previous section. Please refer to that section for a complete description of the circuit and modifications required to the demonstration board.

Performance of the 1900 MHz ATF-35143 Amplifier

The amplifier is tested at a V_{ds} of 2 V and at both 5 and 10 mA I_{ds}. The measured noise figure and gain of the completed amplifier is shown in Figures 11 and 12. Noise figure varies from 0.9 to 1 dB from 1700 MHz through 2500 at a I_{ds} of 10 mA. At an I_{ds} of 5 mA, the same amplifier has a nominal 1.1 dB noise figure over the same frequency range. At 10 mA I_{ds} the gain at 1900 MHz is 15 dB decreasing to 13.8 dB at a I_{ds} of 5 mA. Input and output return loss versus current is shown in Figures 13 and 14. At 2 GHz the input return loss measured 7.7 dB at 10 mA I_{ds} and slightly under 6 dB at I_{ds} = 5 mA. The output return loss at 2 GHz measured 14 dB at 10 mA I_{ds} and 11 dB at 5 mA I_{ds}. The amplifier was designed around the 10 mA I_{ds} bias point and therefore the performance at 5 mA I_{ds} could be improved with slight re-tuning of the matching networks. Improvement in both input and output return loss will also show up as an increase in gain.

The ATF-35143 amplifier was measured for IP3 by subjecting the amplifier input to two test signals at 2 GHz with a 1.25 MHz spacing. The 1.25 MHz spacing was used to simulate a CDMA application. The results of the IP3 measurements are shown in Table 3.

Amplifier IP3 will improve 0.5 to 1 dB with the removal of the drain resistor R4.

Conclusion

Two amplifier designs have been presented using the Avago Technologies ATF-35143 low noise PHEMT. Self biasing has been used to allow operation from a single +3 V power source. Both amplifiers provide a nominal 1 dB noise figure, reasonable gain and high intercept point at both 5 and 10 mA drain current.

Table 2. Component Parts List for the 1900 MHz ATF-35143 Amplifier.

Number	Description
C1	4.3 pF chip capacitor
C2, C6	8.2 pF chip capacitor
C3, C4	30 pF chip capacitor
C5	2.7 pF chip capacitor
C7	10,000 pF chip capacitor
L1	3.3 nH inductor (Coilcraft 0805CS-030XMBC or Toko LL1608-F3N3K)
L2, L3	Use minimal inductance for L2 and L3. Capacitors C3 and C4 are placed as close as possible to the device source leads.
L4	3.3 nH inductor (Coilcraft 0805CS-030XMBC) or (Toko LL1608-F3N3K)
Q1	Avago Technologies ATF-35143 PHEMT
R1	50 Ω chip resistor
R2	R2 consists of two resistors in parallel, one on each source lead. Set for desired drain current. See text.
R3	12 Ω chip resistor
R4	24 Ω chip resistor
Zo	50 Ω Microstrip line

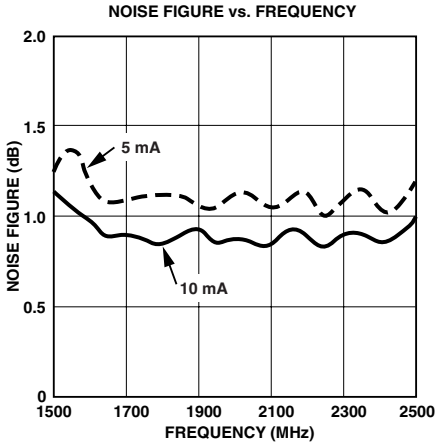

Figure 11. 1900 MHz amplifier noise figure vs. frequency.

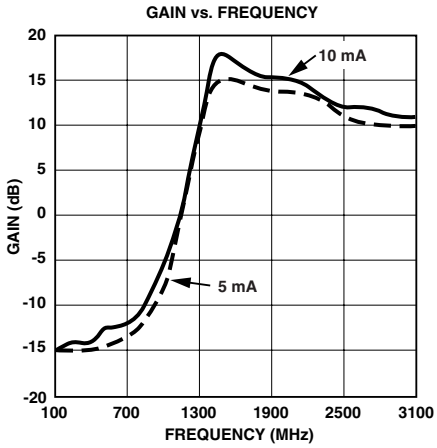

Figure 12. 1900 MHz amplifier gain vs. frequency.

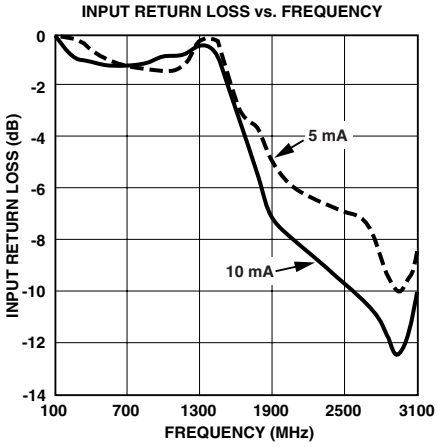

Figure 13. 1900 MHz amplifier input return loss vs. frequency.

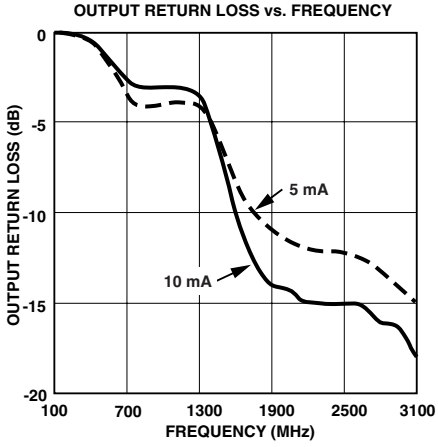

Figure 14. 1900 MHz amplifier output return loss vs. frequency.

Table 3. IP3 versus Bias Point.

Bias Point	OIP3	IIP3
2 V, 5 mA	+14.5 dBm	+0.7 dBm
2 V, 10 mA	+20 dBm	+5 dBm
2 V, 20 mA	+23 dBm	+7 dBm

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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