S-26.3120 Radio Engineering, laboratory course

Lab 4: Amplifier

Final Report

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Abstract

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Contents

Symbols and abbreviations

Symbols

R	resistance [Ω]
C	capacitance [F]
L	inductance [H]
f	frequnecy [Hz]
Z	impedance [Ω]
Y	admittance [S]
z	normalized impedance
y	normalized admittance
λ	wavelength [m]
F	noise figure [dB]
G	two-port gain equal to $\|S_{21}\|$ [dB]
L	attenuation [dB]
S_{ij}	scattering parameter from port i to port j
BW	bandwidth [Hz]
IIP_n	nth order input-referred intermodulation intercept point [dBm]
IM_n	nth order intermodulation product [dBm]
ICP	1 dB input compression point [dBm]
P	signal power [dBm]
N	noise power [dBm]
T	temperature [K]
w	transmission line width [m]
h	substrate height [m]
$\tan\delta$	"tangent delta", a merit of substrate quality (attenuation)
ϵ_r	relative permittivity of the substrate
V	voltage [V]
I	current [I]
U	unilateral figure of merit [U]
Δ	determinant of a scattering matrix
K	Rollet's stability factor
μ	stability factor
ρ	reflection coefficient
RL	return loss [dB]
l	transmission line length

Abbreviations

LNA	low-noise amplifier
SMA	SubMiniature version A, a type of coaxial connector
pHEMT	pseudomophic high electron mobility transistor, a type of field-effect transistor
RF	radio frequency
DC	direct current
CS	common source, a type of field-effect transistor configuration
IDCS	inductively degenerated common source
PTH	plated-through hole, a via
PCB	printed circuit board

1 Introduction

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2 Theoretical background

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3 Preliminary design

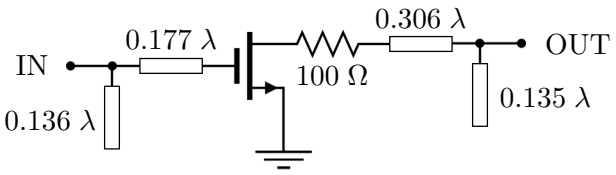

Figure 1: Amplifier pre-design ($Z_0 = 50\ \Omega$).

4 Design

After obtaining a preliminary starting point for the design it was time to pursue the actual design with ADS simulations. In ADS, the final balancing resistor, biasing networks and matching networks were to be designed and optimized. For the simulations, the used PCB material was assigned as RT-Duroid 5870 (Cu 1.0 oz/ft^2) with $\epsilon_r = 2.33 \pm 0.02$, $h = 0.787 \pm 0.003$ mm, $t = 35$ um, and $\tan\delta = 0.0012$. The dimensions of the circuit board were 70×85 mm^2. Fig. 2 presents the final amplifier layout. The layout comprises of five individual sections, namely, the transistor section (a), input and output biasing networks (a,b) and input and output matching networks (d,e).

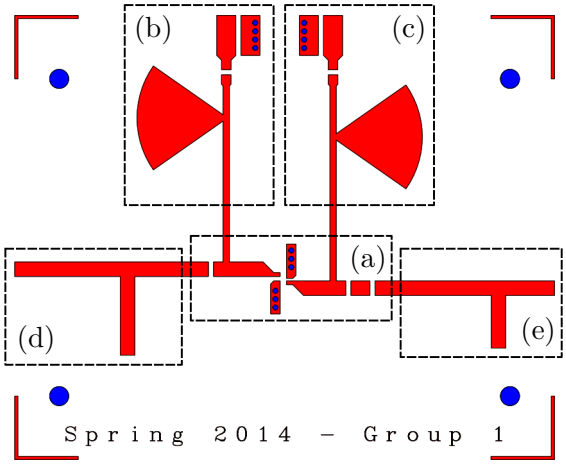

Figure 2: The final amplifier layout comprising of: (a) Transistor section, (b) Input biasing, (c) Output biasing, (d) Input matching and (e) Output matching.

The transistor section includes the transistor followed by the stabilizing resistor. The two gaps at the input and output are for the DC blocking capacitors (10 pF, MURATA GQM series). The capacitors prevent the DC power from flowing to the input and output of the amplifier. The lines pointing vertically from the transistor are for the source. The three blue dots on the source lines are the via-grounding holes. Using multiple via-holes lowers the inductance to the ground. An initial value for the balancing resistor was obtained from the preliminary design. The validity of the preliminary design was quickly checked with a S-parameter model of the transistor. The S-parameter model contains the S-parameters of a certainly biased transistor and thus does not require biasing networks. As the preliminary 100 Ω stabilizing resistor seemed valid it was time to replace the transistor with its non-linear model and continue with the design of the biasing networks.

The biasing networks were designed separately and their operation was verified before attaching them to the actual amplifier model. The main purpose of a biasing networks is to provide DC voltage to empower the transistor. The DC power should not couple to the input and output of the amplifier nor should the RF signal flow to the DC source. Coupling can be avoided by, for instance, using DC blocks, radial stubs, signal absorbing resistors and shorting capacitors. A radial stub, placed at a distance of quarter wavelength from the original signal path, creates a virtual open circuit for the RF signal at a certain frequency. Thus the RF

signal does not propagate to the DC source. The absorbing resistor and shorting capacitors are placed to account for the possible non-desired RF signals. The resistor after the radial stub absorbs the possible reflections whereas the capacitors short the RF signals directly to the ground. 15 Ω absorbing resistors were found to be adequate. Three capacitors (1 pF, 10 pF and 100 pF, MURATA GQM series) were used for the shorting. Due to the non-ideality of the capacitors they provide an enhanced shorting to the ground. The grounding was made using four via-holes. The correct biasing gate to source voltage, V_{GS} was derived with an DC analysis in which the V_{GS} was swept to result in the required biasing current I_{DS}. The result of the DC analysis is presented in Fig. 3. Thus the correct biasing was achieved with $V_{\mathrm{GS}} = -0.39\,\mathrm{V}$. The voltage drop due to the absorbing resistor should be accounted by increasing the source DC voltage by the equivalent amount. In the input biasing network the voltage drop is insignificant due to the low current whereas at the output it is significant, namely, $15\,\Omega * 30\,\mathrm{mA} = 0.45\,\mathrm{V}$.

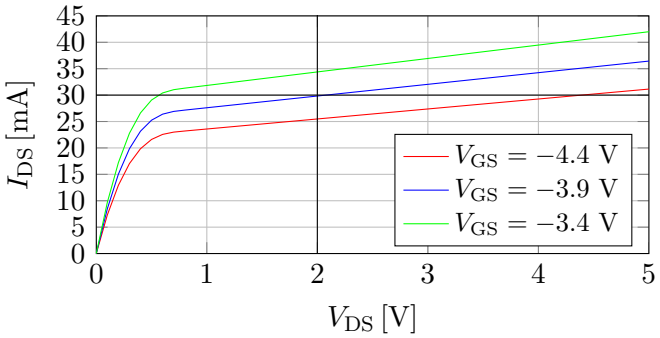

Figure 3: Bias point DC analysis.

After designing the biasing networks they were attached to the amplifier. Correctly designed biasing networks should provide similar simulation results as the S-parameter model of the transistor.

The input and output matching was done using a single open stub. The lengths of the transmission lines were tuned carefully using the Smith chart to meet the design criteria on the amplifier center frequency. At this point, the amplifier did not meet the set gain criteria and thus the value of the balancing resistor had to be decreased. A suitable compromise was found with a balancing resistor value of 50 Ω.

Fig. 4 presents the final simulation results for the input and output return losses RL, stability factor K, gain G and noise figure F. The simulation results depict the amplifier to satisfy all of the set design specifications. The final results at the design frequency of 2.5 GHz are: $RL_{\mathrm{in}} = 22.5$ dB, $RL_{\mathrm{out}} = 29.5$ dB, $K = 1.50$, $G = 13.86$ dB and $F = 0.53$ dB.

Fig. 5 illustrates the 1 dB gain compression and third order intercept (TOI) point for the amplifier. The second and third order intermodulation terms (IM_2 and IM_3) are also plotted in addition to the desired signal frequency. The 1-dB gain compression and TOI occur at input power levels of −1.3 dB and 6.7 dB, respectively.

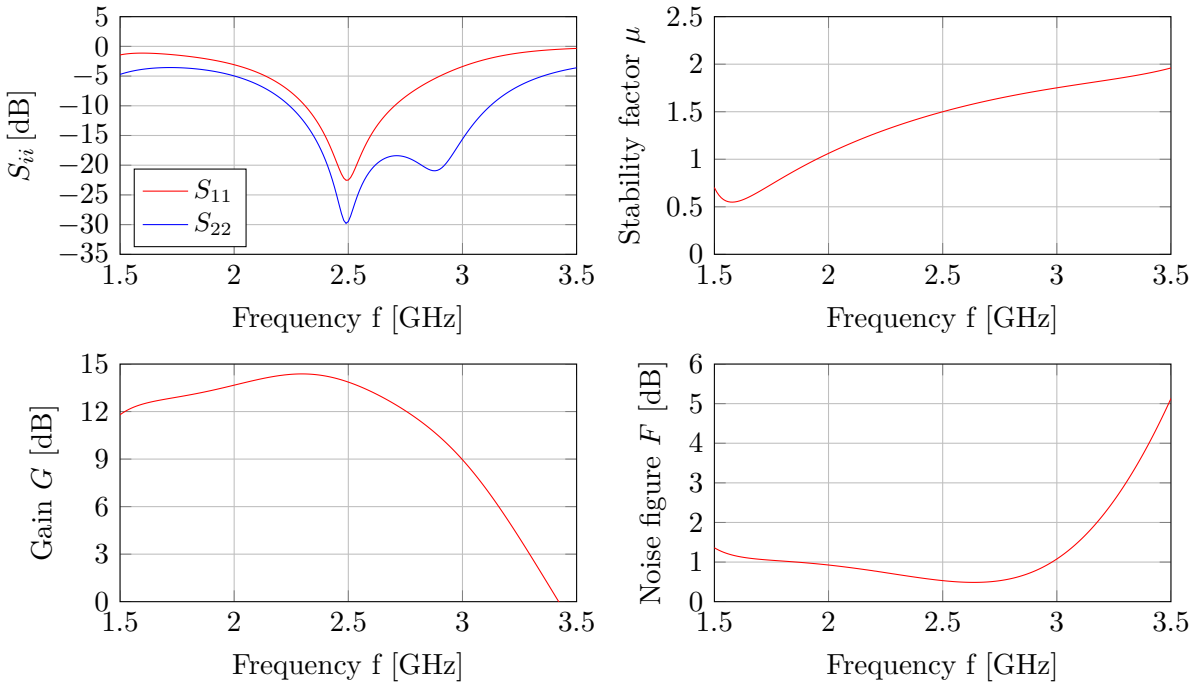

Figure 4: Simulation results for input and output return losses, stability factor, gain and noise.

5 Measurements

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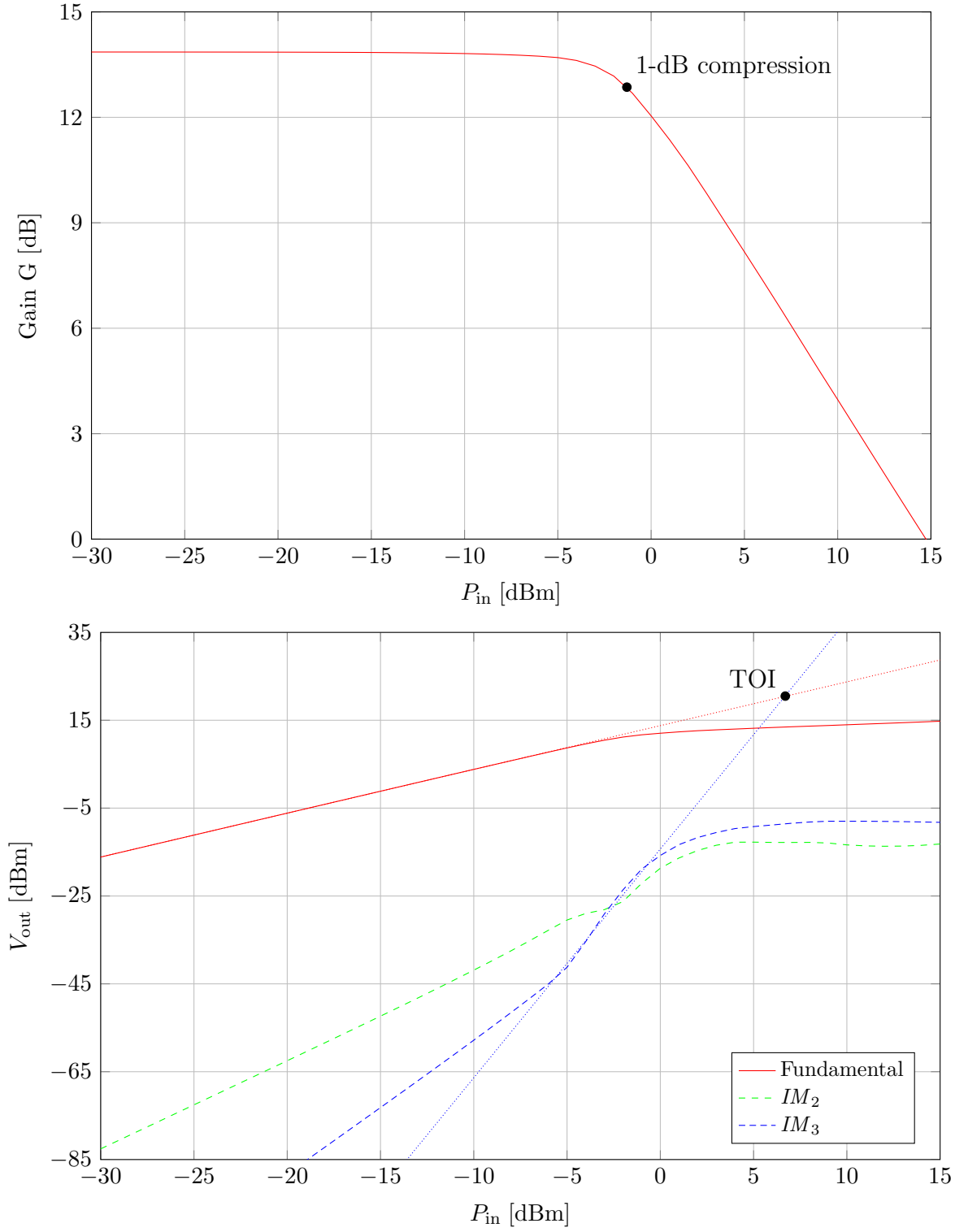

Figure 5: Simulation results for gain saturation and TOI.

6 Results

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7 Conclusions

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8 Feedback

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References

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