S-26.3120 Radio Engineering, laboratory course

Lab 4: Amplifier

Final Report

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Abstract

Text

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Symbols and abbreviations

Symbols

R	resistance [Ω]
C	capacitance [F]
L	inductance [H]
f	frequnecy [Hz]
Z	impedance [Ω]
Y	admittance [S]
z	normalized impedance
y	normalized admittance
λ	wavelength [m]
F	noise figure [dB]
G_0	power gain, equal to $\|S_{21}\|$ [dB]
G_A	available power gain [dB]
G_T	transducer power gain [dB]
G_P	operating power gain [dB]
L	attenuation [dB]
S_{ij}	scattering parameter from port i to port j
BW	bandwidth [Hz]
IIP_n	nth order input-referred intermodulation intercept point [dBm]
IM_n	nth order intermodulation product [dBm]
ICP	1 dB input compression point [dBm]
P	signal power [dBm]
N	noise power [dBm]
T	temperature [K]
w	transmission line width [m]
h	substrate height [m]
$\tan\delta$	"tangent delta", a merit of substrate quality (attenuation)
ϵ_r	relative permittivity of the substrate
V	voltage [V]
I	current [I]
U	unilateral figure of merit [U]
Δ	determinant of a scattering matrix
K	Rollet's stability factor
μ	stability factor
ρ	reflection coefficient
RL	return loss [dB]
l	transmission line length

Abbreviations

LNA	low-noise amplifier
SMA	SubMiniature version A, a type of coaxial connector
pHEMT	pseudomophic high electron mobility transistor, a type of field-effect transistor
RF	radio frequency
DC	direct current
CS	common source, a type of field-effect transistor configuration
IDCS	inductively degenerated common source
PTH	plated-through hole, a via
PCB	printed circuit board
CAD	computer-aided design
ADS	Agilent Advanced Design System, a CAD software

1 Introduction

Topic/Field – overview (one paragraph)

Topic/Field – a closer look (one paragraph)

In the fourth lab exercise during the *S-26.3120 Radio Engineering, laboratory course* a low-noise amplifier (LNA) is to be designed, fabricated and measured. The lab was divided into checkpoints as follows. First there was a individually completed pre-study, based on which the actual amplifier was to be designed in groups using computer-aided design (CAD) tools. For this purpose, Agilent Advanced Design System (ADS) was used.

Using ADS, we created a suitable microstrip layout for our amplifier. Next, a third-party manufacturer fabricated a printed circuit board (PCB) according to our specifications. The amplifier was then fabricated using this board, given transistor and miscellaneous components. The amplifier was then tested and measured rigorously. All of this was to be documented in a detailed lab report.

This document is the final report of this lab exercise and is organized ad follows. In the section following the introduction, theoretical background governing LNA design is presented briefly. In the third section, the preliminary design used as a the starting point of the group work is shown. Section 4 gives explains the final amplifier designed with ADS in detail. In the two sections following this explanation, measurements and obtained results are presented. The second to last section draws the conclusion. Finally, in the last section, feedback and suggestions to improve this course are given.

2 Theoretical background

Text

3 Preliminary design

In this section, the preliminary design used as a starting point for the group work is presented. This presentation is intentionally rather short, presenting only the main points of the manual design procedure and the crude pre-design. For a more complete depiction of the derivation of the amplifier circuit shown in this section, the reader is advised to get acquanted with the pre-study reports.

The preliminary design is based solely on linear (and also otherwise "ideal") scattering parameter analysis; a process with a direct connection to the theory shown in the previous chapter and in textbooks like [1–3]. The process is manual in the sense that no purpose-built CAD tools were used. Thus it is indeed possible to obtain same results with a "back-of-the-envelope" approach albeit extremely cumbersome. To help with this, a completely self-made Matlab-script was used.

A cicruit schematic of the pre-design is shown in Fig. 1. In the three tables following the figure, the key characteristics of the preliminary design are shown. Table 1 presents the reflection coefficients used for matching. These reflection coffecients are realized single shunt-stub matching with transmission line lengths given in Table 2. In Table 3, the obtained key performance metrics are compared with design goals. All design goals are met simultaneously.

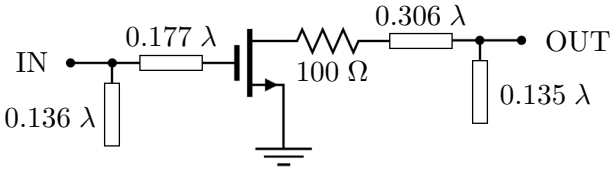

Figure 1: Amplifier pre-design ($Z_0 = 50\ \Omega$).

Table 1: Reflection coefficients of the preliminary design.

Reflection coefficient		Cartesian	Polar
Source	ρ_{S}	$-0.191 + \mathrm{j}0.461$	$0.499\angle{+}112.6\,^\circ$
Input	ρ_{in}	$-0.307 - \mathrm{j}0.503$	$0.589\angle{-}121.5\,^\circ$
Load	ρ_{L}	$+0.461 + \mathrm{j}0.171$	$0.492\angle{+}20.4\,^\circ$
Output	ρ_{out}	$+0.461 - \mathrm{j}0.171$	$0.492\angle{-}20.4\,^\circ$

Table 2: Matching circuits of the pre-design ($Z_0 = 50\ \Omega$).

Port	Distance from transistor l_1 [λ]	Stub length l_2 [λ]
Input	0.177	0.136
Output	0.306	0.135

Table 3: Properties of the pre-design.

Parameter	Value [dB]	Design goal [dB]	Margin [dB]
RL_{in}	15.22	≥ 15	0.22
RL_{out}	∞	≥ 15	∞
G_{A}	13.35	≥ 13	0.35
G_{T}	13.35	≥ 13	0.35
G_{P}	13.49	≥ 13	0.49
F	0.737	≤ 0.8	0.062

4 Design

After obtaining a preliminary starting point for the design it was time to pursue the actual design with ADS simulations. In ADS, the final balancing resistor, biasing networks and matching networks were to be designed and optimized. For the simulations, the used PCB material was assigned as RT-Duroid 5870 (Cu 1.0 oz/ft^2) with $\epsilon_r = 2.33 \pm 0.02$, $h = 0.787 \pm 0.003$ mm, $t = 35$ um, and $\tan\delta = 0.0012$. The dimensions of the circuit board were 70×85 mm^2. Fig. 2 presents the final amplifier layout. The layout consists of five individual sections, namely, the transistor section (a), input and output biasing networks (a,b) and input and output matching networks (d,e).

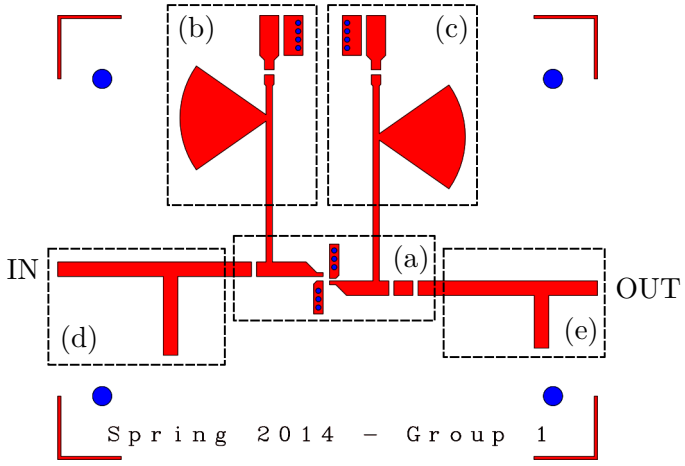

Figure 2: The final amplifier layout comprising (a) transistor section, (b) input biasing, (c) output biasing, (d) input matching and (e) output matching.

The transistor section includes the transistor followed by the stabilizing resistor. The two gaps at the input and output are for the DC blocking capacitors (10 pF, MURATA GQM series). The capacitors prevent the DC power from flowing to the input and output of the amplifier. The lines pointing vertically from the transistor are for the source. The three blue dots on the source lines are the via-grounding holes. Using multiple via-holes lowers the inductance to the ground. An initial value for the balancing resistor was obtained from the preliminary design. The validity of the preliminary design was quickly checked with a S-parameter model of the transistor. The S-parameter model contains the S-parameters of a certainly biased transistor and thus does not require biasing networks. As the preliminary 100 Ω stabilizing resistor seemed valid it was time to replace the transistor with its non-linear model and continue with the design of the biasing networks.

The biasing networks were designed separately and their operation was verified before attaching them to the actual amplifier model. The main purpose of a biasing networks is to provide DC voltage to empower the transistor. The DC power should not couple to the input and output of the amplifier nor should the RF signal flow to the DC source. Coupling can be avoided by, for instance, using DC blocks, radial stubs, signal absorbing resistors and shorting capacitors. A radial stub, placed at a distance of quarter wavelength from the original signal path, creates a virtual open circuit for the RF signal at a certain frequency. Thus the RF signal does not propagate to the DC source. The absorbing resistor and shorting capacitors

are placed to account for the possible non-desired RF signals. The resistor after the radial stub absorbs the possible reflections whereas the capacitors short the RF signals directly to the ground. 15 Ω absorbing resistors were found to be adequate. Three capacitors (1 pF, 10 pF and 100 pF, MURATA GQM series) were used for the shorting. Due to the non-ideality of the capacitors they provide an enhanced shorting to the ground. The grounding was made using four via-holes. The correct biasing gate to source voltage, V_{GS} was derived with an DC analysis in which the V_{GS} was swept to result in the required biasing current I_{DS}. The result of the DC analysis is presented in Fig. 3. Thus the correct biasing was achieved with $V_{\mathrm{GS}} = -0.39$ V. The voltage drop due to the absorbing resistor should be accounted by increasing the source DC voltage by the equivalent amount. In the input biasing network the voltage drop is insignificant due to the low current whereas at the output it is significant, namely, $15\ \Omega \cdot 30\ \mathrm{mA} = 0.45$ V.

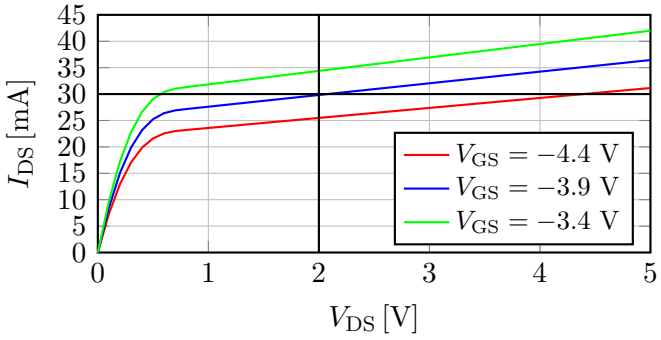

Figure 3: Bias point DC analysis.

After designing the biasing networks they were attached to the amplifier. Correctly designed biasing networks should provide similar simulation results as the S-parameter model of the transistor.

The input and output matching was done using a single open stub. The lengths of the transmission lines were tuned carefully using the Smith chart to meet the design criteria on the amplifier center frequency. At this point, the amplifier did not meet the set gain criteria and thus the value of the balancing resistor had to be decreased. A suitable compromise was found with a balancing resistor value of 50 Ω.

Fig. 4 presents the final simulation results for the input and output return losses RL, stability factor K, gain G and noise figure F. The simulation results depict the amplifier to satisfy all of the set design specifications. The final simulation results at the design frequency at 2.5 GHz are summarized in Table 4.

Table 4: Simulation results at 2.5 GHz

Parameter	Value
RL_{in} [dB]	22.5
RL_{out} [dB]	29.5
K	1.5
G [dB]	13.86
F [dB]	0.53

Fig. 5 and 6 illustrate the 1-dB gain compression and third order intercept (TOI) point

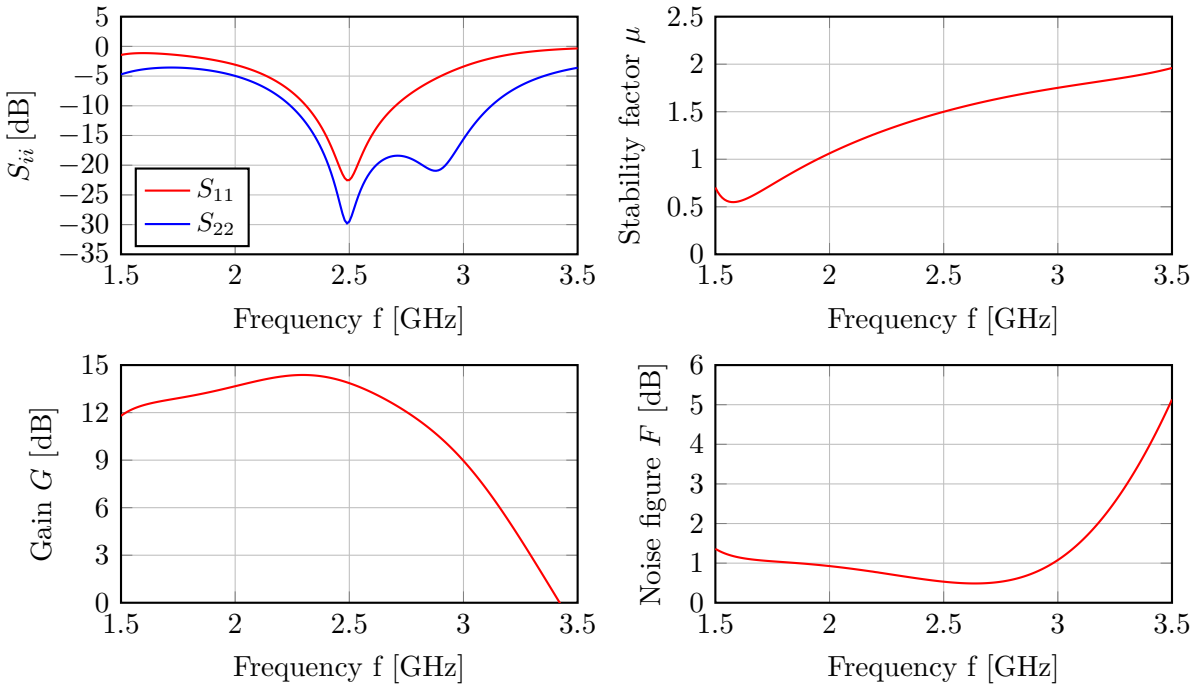

Figure 4: Simulation results for input and output return losses, stability factor, gain and noise.

for the amplifier. The second and third order intermodulation terms (IM_2 and IM_3) are also plotted in addition to the desired signal frequency. The 1-dB gain compression and TOI occur at input power levels of −1.3 dB and 6.7 dB, respectively.

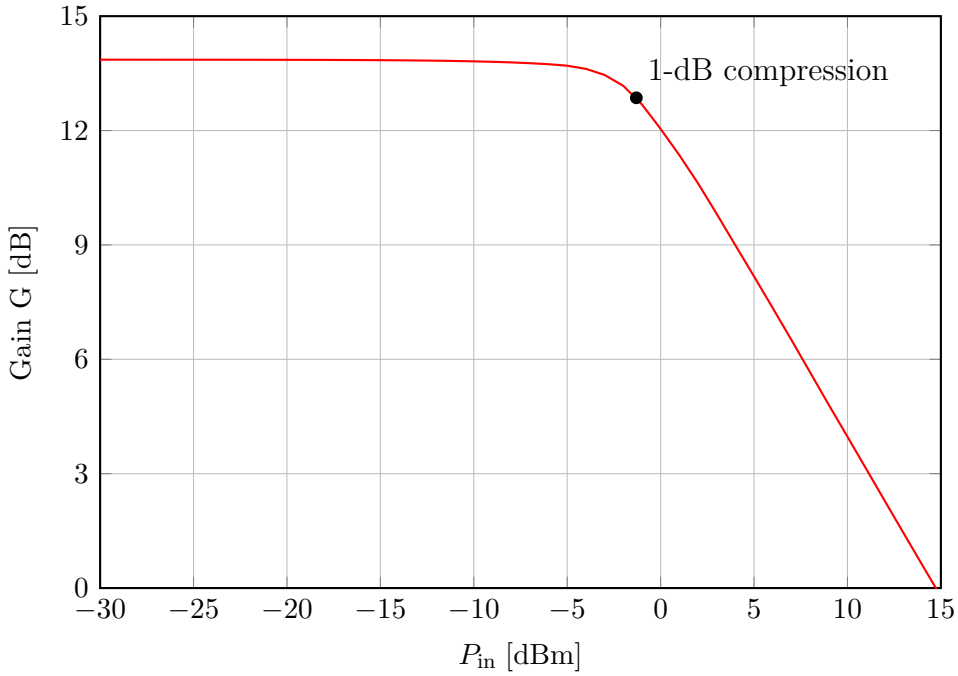

Figure 5: Simulation results for gain compression and the 1-dB compression point.

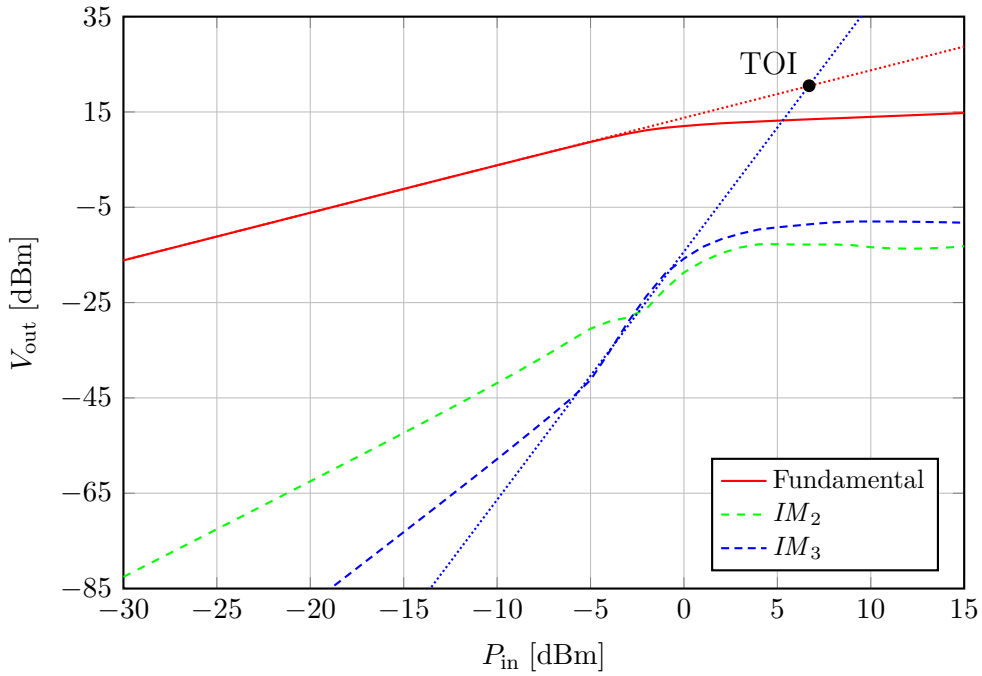

Figure 6: Simulation results for intermodulation terms and TOI.

Fig. 7 presents the final manufactured amplifier with the surface mounted components and connectors soldered in place.

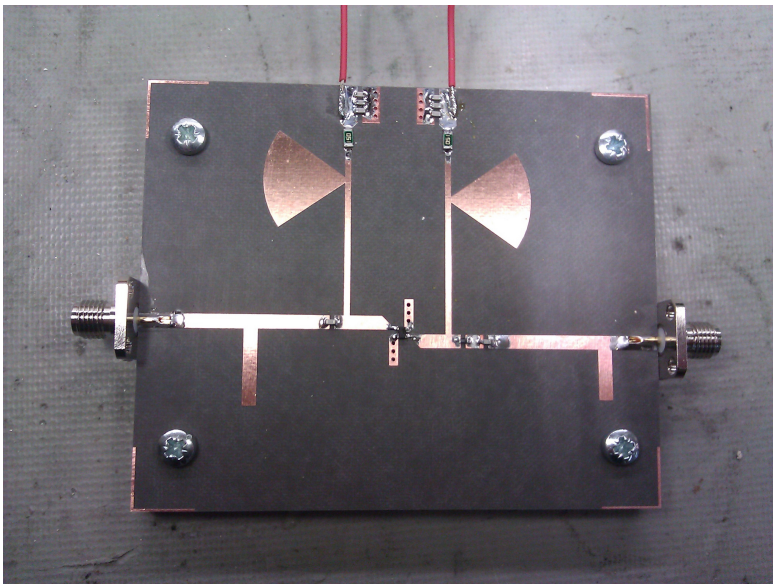

Figure 7: The final manufactured proto amplifier.

5 Measurements

The measurements began by determining the S-parameters of the amplifier. A VNA was used for this purpose which was first calibrated with a SOLT calibration kit. The amplifier was biased using two power sources. First, the simulated voltage gate of approximately -0.39 V was applied to the gate and then the drain voltage was increased slowly. It was soon realized that the previously simulated and calculated biasing point could not be reached. To reach the required $I_{\mathrm{DS}} = 30$ mA the V_{DS} had to be increased to 4.2 V. This difference could partly result from the inaccurate adjustability of the power sources. After biasing the amplifier the s-parameters were measured. The measured S-parameters are presented in Fig. 8. The S-parameter results depict a shift of the amplifier center frequency to lower frequencies.

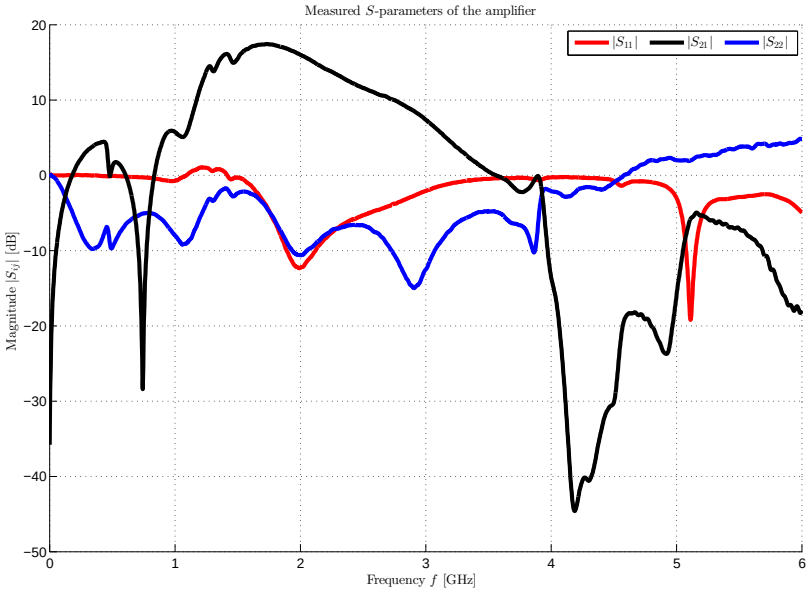

Figure 8: The measured S-paramaters S_{11}, S_{22} and S_{21}.

The gain performance is mostly set by the biasing point and is still quite acceptable at the original design frequency. On the contrary, the input and output matching are clearly shifted to lower frequencies, namely to 2 GHz. The input and output reflection coefficients can be inspected on the Smith chart to get a hint of this frequency shifting. The input and output reflection coefficients are plotted in Fig. 9 at frequencies 1.5 GHz to 3.5 GHz. The information on the Smith chart does not propose any reasonable method for improving the input matching. In contrast, the output matching seems to be rotated by a possibly unaccounted additional parallel capacitance. Series inductance would rotate the matching similarly. The output matching could possibly be improved by disabling some of the via-grounds which would increase the parallel inductance thus rotating the matching point towards the center of the Smith chart. The measurements presented later on are conducted at 2 GHz as the built amplifier's performance would be really poor on the desired 2.5 GHz.

Fig. 10 presents the gain saturation and the 1-dB compression point of the amplifier at 2

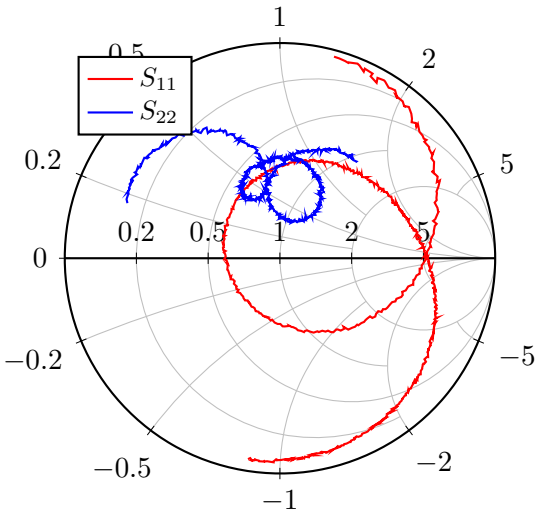

Figure 9: Input and output reflection coefficients at frequencies 1.5 GHz to 3.5 GHz.

GHz. The unsaturated gain is 14.1 dB and the 1-dB compression occurs at an input power of approximately -2.9 dB.

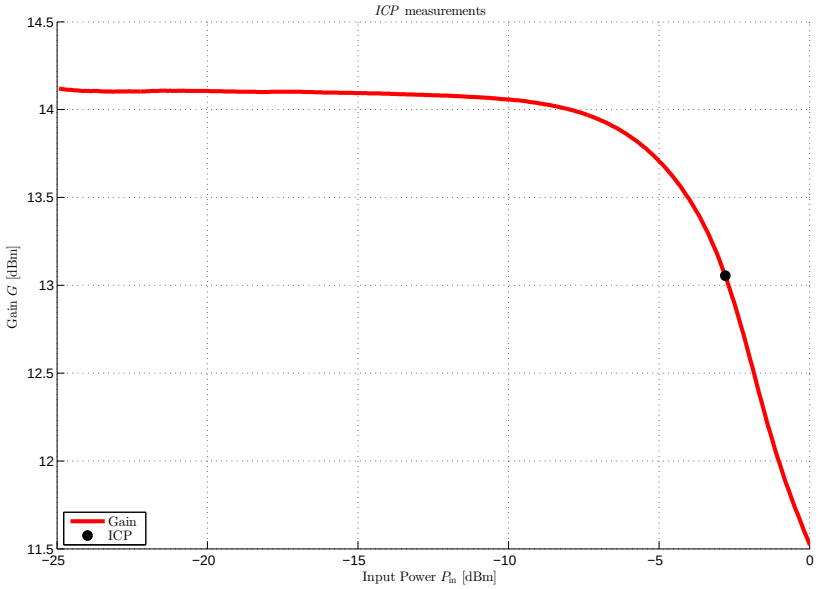

Figure 10: The measured gain saturation and 1-dB compression point.

Intermodulation of the amplifier was inspected by applying two closely separated signal frequencies to the input of the amplifier and setting their power intensity to the same level. The signal frequencies were chosen as 1.999 GHz and 2.001 GHz. Thus the inspected third order intermodulation term would occur at 2.003 GHz. The intermodulation term was measured as the original signal frequency power levels were increased. The resulting plot is presented in

Fig. 11. The TOI is approximately at an input power level of 3 dB.

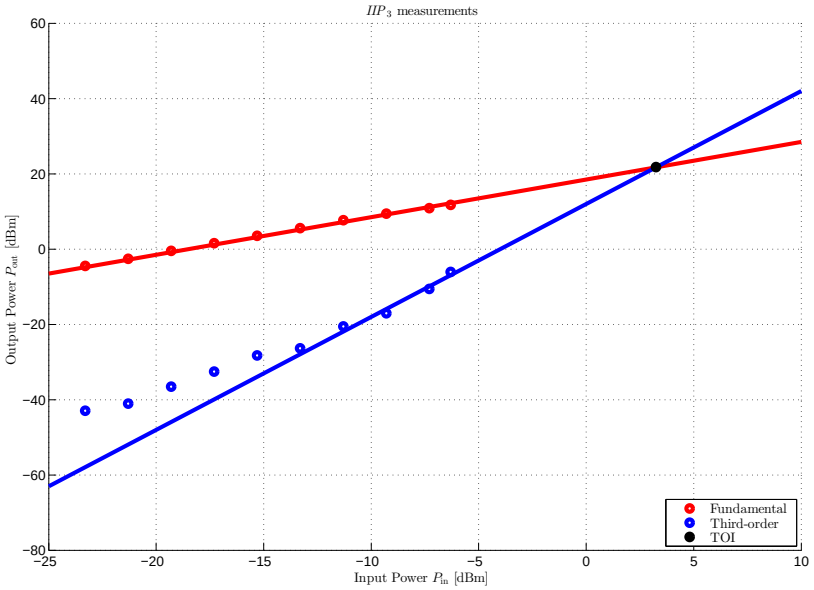

Figure 11: Result of the intermodulation measurement.

An important occurrence was observed when conducting the intermodulation measurement originally. The spectrum analyzer displayed 10 MHz harmonics around the original signal frequencies. This indicated that the amplifier input either had some disturbing signal present or that the transistor was damaged. The situation was fixed by replacing the transistor and adding an additional 1 uF capacitor to the output biasing ground. Most likely the transistor was broken. Transistors are most likely broken by the excessive heat during soldering and de-soldering. Applying the biasing drain voltage before the gate voltage or exceeding the maximum allowed current of the transistor may also damage it (even burn it, as was noticed).

Noise figure of the amplifier was measured by using the Y-factor method. In the Y-factor method a noise source is connected to the input of the amplifier. The noise source is used as a hot and cold source by applying a biasing voltage and the output power from the amplifier is measured. In this case the output noise power is too low and requires an additional pre-amplifier. Thus the Y-factor method has to be applied twice by first measuring the hot and cold source only with the pre-amplifier applied. When the DUT (built amplifier) is in conjunction with the pre-amplifier the DUT noise figure can be calculated from the cascaded system.

6 Results

Text

7 Conclusions

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8 Feedback

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References

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