VGA

The image bellow shows each module created and connected through buses.

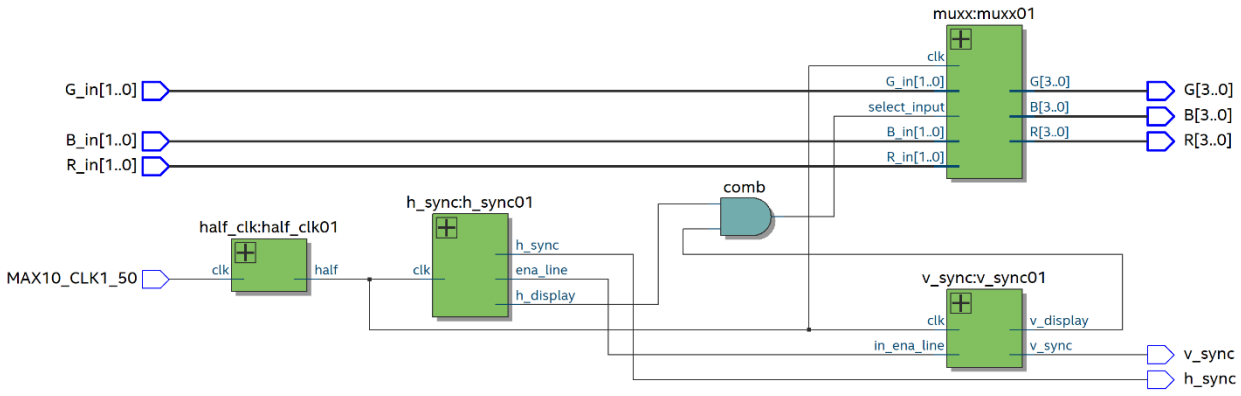

Image 1

Muxx: This module is where the input of the user is taken. Then 4-bit value is routed to the output, only if h_display and v_display is 1.

Half_clk: In this module is very straight forward, the internal clock signal is taken then at each whole period a new signal is generated slowing down the initial clock by ½.

H_sync: Here is where some magic starts to happen. A counter is created and specific numbers some signals go high or low. To be more specific see Image 2 and it will make more sense.

V_sync: Same here, refer to Image 2 to have a better understanding of what happens here.

The rest is just buses and connections to route one module to another.

Counters for h_sync and v_sync

Using the 25Mhz clock the counter for h_sync goes from 0-95 and HSYNC=0 and from 96-800 HSYNC = 1.

Display interval or display time occurs from 144-784 then Display_Interval = 1.

The same concept is applied to VSYNC and the Display_Interval

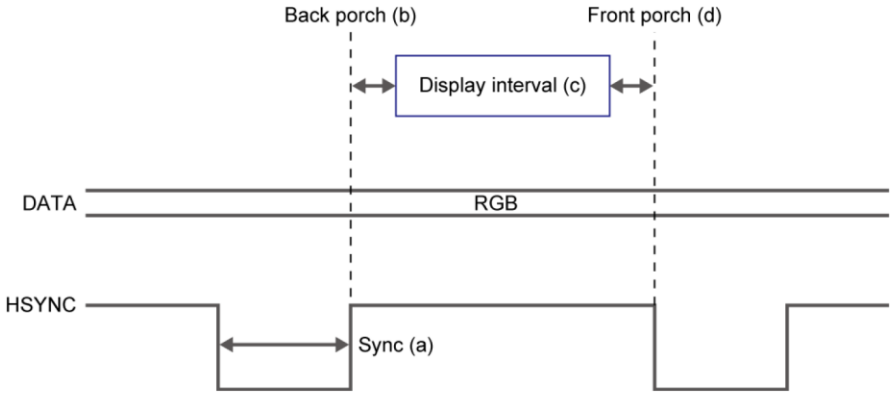

Figure 3-22 VGA horizontal timing specification

Table 3-9 VGA Horizontal Timing Specification

VGA mode		*Horizontal Timing Spec*				
Configuration	*Resolution(HxV)*	*a(pixel clock cycle)*	*b(pixel clock cycle)*	*c(pixel clock cycle)*	*d(pixel clock cycle)*	*Pixel clock(MHz)*
VGA(60Hz)	640x480	96	48	640	16	25

Table 3-10 VGA Vertical Timing Specification

VGA mode		*Vertical Timing Spec*				
Configuration	*Resolution(HxV)*	*a(lines)*	*b(lines)*	*c(lines)*	*d(lines)*	*Pixel clock(MHz)*
VGA(60Hz)	640x480	2	33	480	10	25

Image 2

The following images are some images of different colors changing the position of the switches of the board

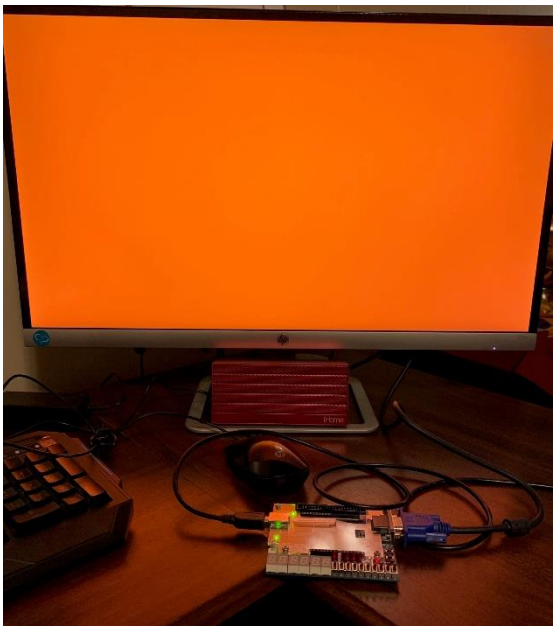

Image 3

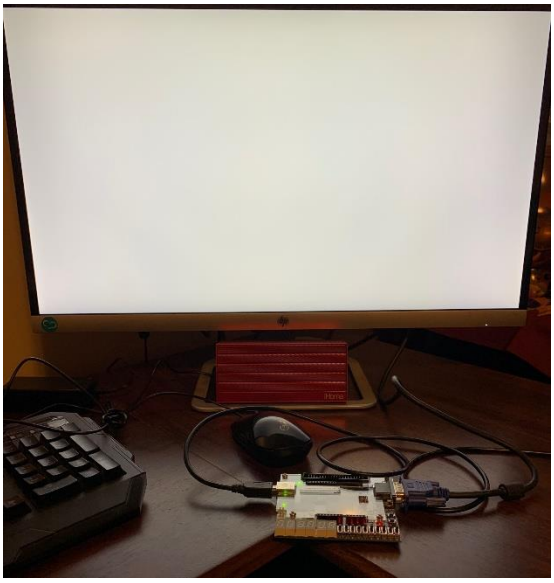

Image 4