

2023 Digital IC Design Homework 4

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| NAME | 劉承軒 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Simulation Result | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Functional simulation | 100 | Gate-level simulation | 100 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <pre> # Layer 0 output is correct ! # Layer 1 output is correct! # # ----- S U M M A R Y ----- # # Congratulations! Layer 0 data have been generated successfully! The result is PASS! # Congratulations! Layer 1 data have been generated successfully! The result is PASS! # terminate at 70662 cycle # # ** Note: \$finish : C:/Users/liuch/Desktop/Code/DIC_Assignment/HW4/testfixture.v # Time: 3533108315 ps Iteration: 0 Instance: /testfixture # </pre> | | <pre> # Layer 0 output is correct ! # Layer 1 output is correct! # # ----- S U M M A R Y ----- # # Congratulations! Layer 0 data have been generated successfully! The result is PASS! # Congratulations! Layer 1 data have been generated successfully! The result is PASS! # terminate at 70662 cycle # # ** Note: \$finish : C:/Users/liuch/Desktop/Code/DIC_Assignment/HW4/testfixture.v # Time: 3533108315 ps Iteration: 0 Instance: /testfixture # </pre> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Synthesis Result | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Total logic elements | 451 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Total memory bits | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Embedded multiplier 9-bit elements | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Total cycle used | 70662 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <div style="border: 1px solid #ccc; padding: 5px;"> <div style="display: flex; justify-content: space-between; align-items: center;"> Filter <<Filter>> </div> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Flow Status</td><td>Successful - Sun May 21 14:21:05 2023</td></tr> <tr> <td>Quartus Prime Version</td><td>20.1.1 Build 720 11/11/2020 SJ Lite Edition</td></tr> <tr> <td>Revision Name</td><td>ATCONV</td></tr> <tr> <td>Top-level Entity Name</td><td>ATCONV</td></tr> <tr> <td>Family</td><td>Cyclone IV E</td></tr> <tr> <td>Device</td><td>EP4CE55F23A7</td></tr> <tr> <td>Timing Models</td><td>Final</td></tr> <tr> <td>Total logic elements</td><td>451 / 55,856 (< 1 %)</td></tr> <tr> <td>Total registers</td><td>152</td></tr> <tr> <td>Total pins</td><td>82 / 325 (25 %)</td></tr> <tr> <td>Total virtual pins</td><td>0</td></tr> <tr> <td>Total memory bits</td><td>0 / 2,396,160 (0 %)</td></tr> <tr> <td>Embedded Multiplier 9-bit elements</td><td>2 / 308 (< 1 %)</td></tr> <tr> <td>Total PLLs</td><td>0 / 4 (0 %)</td></tr> </table> </div> | | | | Flow Status | Successful - Sun May 21 14:21:05 2023 | Quartus Prime Version | 20.1.1 Build 720 11/11/2020 SJ Lite Edition | Revision Name | ATCONV | Top-level Entity Name | ATCONV | Family | Cyclone IV E | Device | EP4CE55F23A7 | Timing Models | Final | Total logic elements | 451 / 55,856 (< 1 %) | Total registers | 152 | Total pins | 82 / 325 (25 %) | Total virtual pins | 0 | Total memory bits | 0 / 2,396,160 (0 %) | Embedded Multiplier 9-bit elements | 2 / 308 (< 1 %) | Total PLLs | 0 / 4 (0 %) |
| Flow Status | Successful - Sun May 21 14:21:05 2023 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Quartus Prime Version | 20.1.1 Build 720 11/11/2020 SJ Lite Edition | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Revision Name | ATCONV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Top-level Entity Name | ATCONV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Family | Cyclone IV E | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Device | EP4CE55F23A7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Timing Models | Final | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Total logic elements | 451 / 55,856 (< 1 %) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Total registers | 152 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Total pins | 82 / 325 (25 %) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Total virtual pins | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Total memory bits | 0 / 2,396,160 (0 %) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Embedded Multiplier 9-bit elements | 2 / 308 (< 1 %) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Total PLLs | 0 / 4 (0 %) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Description of your design | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

I use a [8:0] array to store target address of peripheral address of current pixel. This may spend some area but is easy to use. It use 10 cycles to get all 3*3 pixels and calculate the temp multiplication results simultaneously. After all 3*3 pixels are done then store the relu result to layer 0 memory and move to the next pixels. Th maxpooling stage is simply loading 4 pixels in layer 0 and do the comparison.

*Scoring = (Total logic elements + Total memory bits + 9*Embedded multipliers 9-bit elements) X Total cycle used*

*** Total logic elements must not exceed 1000.**