2023 Digital IC Design Homework 4

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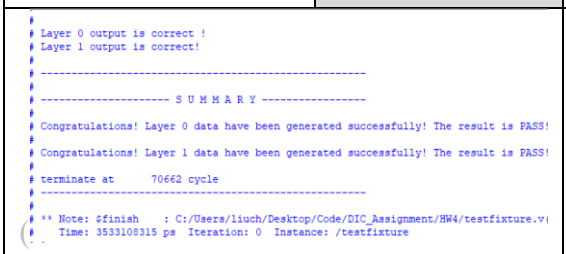
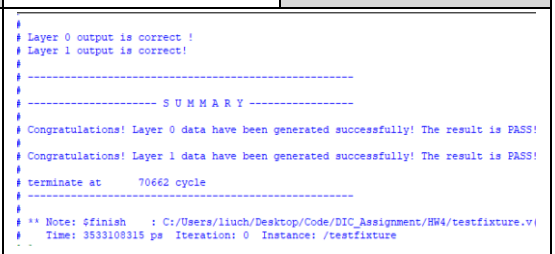
Simulation Result

Functional simulation	100	Gate-level simulation	100





Synthesis Result

Total logic elements	451
Total memory bits	0
Embedded multiplier 9-bit elements	2
Total cycle used	70662

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Flow Status	Successful - Sun May 21 14:21:05 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	ATCONV
Top-level Entity Name	ATCONV
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	451 / 55,856 (< 1 %)
Total registers	152
Total pins	82 / 325 (25 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	2 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

Description of your design

I use a [8:0] array to store target address of peripheral address of current pixel.
This may spend some area but is easy to use. It use 10 cycles to get all 3*3 pixels and calculate the temp multiplication results simultaneously. After all 3*3 pixels are done then store the relu result to layer 0 memory and move to the next pixels.
Th maxpooling stage is simply loading 4 pixels in layer 0 and do the comparison.

*Scoring = (Total logic elements + Total memory bits + 9*Embedded multipliers 9-bit elements) X Total cycle used*

*** Total logic elements must not exceed 1000.**