2023 Digital IC Design Homework 2

|  |  |  |
| --- | --- | --- |
| NAME | 劉承軒 | |
| Student ID | P77111079 | |
| **Functional Simulation Result** | | |
| **Score** | | **100** |
|  | | |
| **Description of your design** | | |
| I declared a size 11 of register stack[10:0] for each element has 4 bits to store the temporary number which range from 1~10. The logic state has 6 steps which defines as below:  *INIT*: Initial all data.  *LOAD\_SEQ* : Loading the target number station B need to match with.  *READ\_NUM*: read the top number in stack.  *PUSH:* Push the number in station A into the stack.  *POP*: Pop the top of number stores in stack to station B.  *DONE*: output the result if the match is all paired or not match, then return negative result.  Methodology:  I firstly read the target number in station B, and then in READ\_NUMS step, compares the target number to top number stores in stack. If the target number is less than top stack number then go to the push step and push the number to top of the stack, until it match the target number then pop out the number to station B and read the next target. Until all target is read then output the result true, or once if the target number is larger than the top number in stack in POP state, then return false instead. | | |