2023 Digital IC Design Homework 4

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| **Simulation Result** | | | | | |
| Functional simulation | | 100 | | Gate-level simulation | 100 |
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| **Synthesis Result** | | | | | |
| Total logic elements | | | 451 | | |
| Total memory bits | | | 0 | | |
| Embedded multiplier 9-bit elements | | | 2 | | |
| Total cycle used | | | 70662 | | |
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| **Description of your design** | | | | | |
| I use a [8:0] array to store target address of peripheral address of current pixel.  This may spend some area but is easy to use. It use 10 cycles to get all 3\*3 pixels and calculate the temp multiplication results simultaneously. After all 3\*3 pixels are done then store the relu result to layer 0 memory and move to the next pixels.  Th maxpooling stage is simply loading 4 pixels in layer 0 and do the comparison. | | | | | |

*Scoring = (Total logic elements + Total memory bits + 9\*Embedded multipliers 9-bit elements) X Total cycle used*

**\* Total logic elements must not exceed 1000.**