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Understanding Delta-Sigma Modulators

Specific equations can help designers quantify the various improvements that delta-sigma modulators can provide.

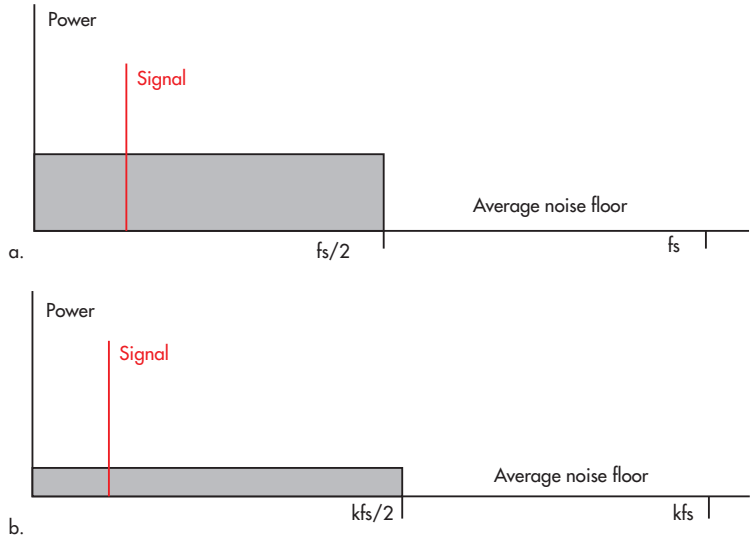
Delta-sigma analog-to-digital converters (ADCs) are fascinating—almost mythical in their ability to support low- to medium-speed and high-resolution applications. They take advantage of the speed of analog circuits, along with the robustness of digital circuits. They also reduce the amount of analog circuitry used in the converter. More importantly, the analog parts of the circuit don't need to be very accurate. Of course, the digital blocks then must work at higher sampling clocks and, thus, consume more power.

DELTA-SIGMA MODULATORS

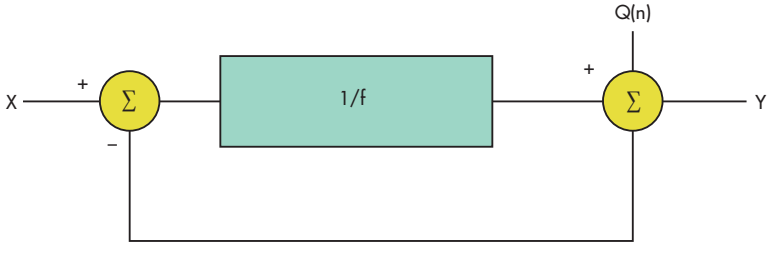
A delta-sigma ADC generally comprises a delta-sigma modulator, followed by a decimation filter. Delta-sigma modulation is one of the most effective forms of conversion in the data converter world. Its applications include communication systems, professional audio, and precision measurements.

The goal of delta-sigma modulation is to achieve higher transmission efficiency by transmitting only the changes (delta) in value between consecutive samples, rather than the actual samples themselves. ADCs and digital-to-analog converters (DACs) both can use delta-sigma modulation.

Oversampling reduces the effect of noise within the signal bandwidth of interest, benefitting the delta-sigma ADC's analog operation. Next, noise shaping pushes the noise out of signal bandwidth. Digital operation then filters out the noise that's out of the band of interest. Finally, this digital filter decimates or down-samples the data. Before considering the modulator



1. A hypothetical delta-sigma spectrum of signal components in a delta-sigma converter includes what its average noise floor looks like when it is sampled at an arbitrary sampling frequency: fs (where fs > $2f_O$, i.e., greater than Nyquist) (a). With the sampling frequency increased by a factor, k, the noise energy is distributed over a wider range of frequencies (b).



2. To achieve noise shaping, the output signal, Y, is fed back and summed with the input signal, X. The result is then fed to an amplifier block with gain of 1/f, the output of which summed with the signal Q(n).

itself, though, it's necessary to become familiar with a few concepts that play a significant role in converters: quantization noise, oversampling, and noise shaping.

QUANTIZATION NOISE

In an ADC, the quantized signal can be described as the input signal plus quantization noise:

$$V_{Quantized} = V_{In} + \varepsilon \qquad (1)$$

$V_{Quantized}$ and V_{In} are, respectively, the quantized signal and the input signal; ε is the error associated with this process, or the difference between the input and output of the quantizer.

The converter's full range divided by the number of its quantization levels defines its least significant bit (LSB). An N-bit converter has 2N levels of quantization. Therefore, the width of any of these quantization levels is FS/(2N – 1). For an ADC with a quantization width of Δ, the quantization noise has equal probability of falling anywhere between –Δ/2 and +Δ/2 and a probability density function that is uniform over the range of quantization error. The quantization noise power can be calculated by integrating the error over this range as in:

$$\varepsilon_{rms}^2 = \frac{1}{\Delta}\int_{\frac{-\Delta}{2}}^{\frac{\Delta}{2}} \varepsilon^2\, d\varepsilon = \frac{1}{\Delta}\frac{\varepsilon^3}{3}\Bigg|_{\frac{-\Delta}{2}}^{+\frac{\Delta}{2}} = \frac{\Delta^2}{12} \qquad (2)$$

which describes the noise power in terms of LSB width. However, it can be rewritten to express it in terms of number of bits and full scale:

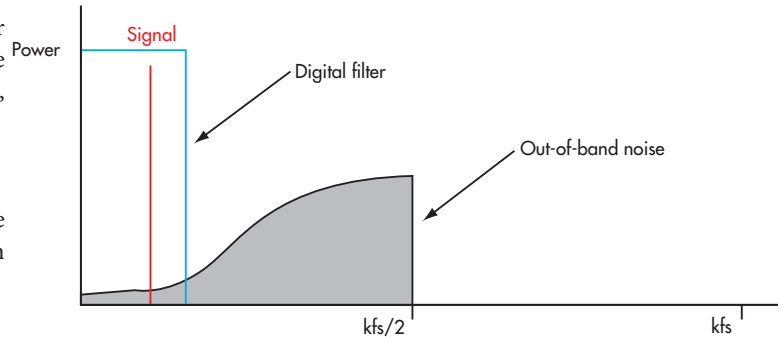
$$\varepsilon_{rms}^2 = \frac{\Delta^2}{12} \approx \frac{FS^2}{3 \bullet 2^{2N}} \qquad (3)$$

OVERSAMPLING

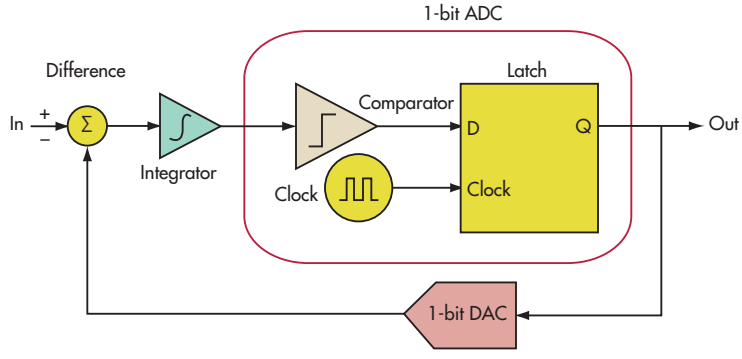
In general, the signals can be sampled with a frequency that is much greater than the Nyquist frequency. The ratio of sampling frequency (fs) to Nyquist frequency ($2f_O$) is called an oversampling ratio (OSR), where f_O is the frequency of the input signal. So, OSR can be written as:

$$OSR = \frac{f_{OS}}{2f_O} \qquad (4)$$

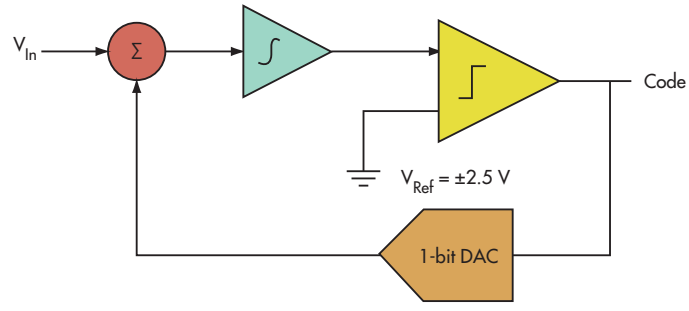
Under oversampled conditions, the noise power that falls within the signal bandwidth (0



3. Following noise shaping, a digital filter removes most of the noise. Filtering can be performed in the digital or analog domain. In this case, the modulator is emitting a bit stream, so a digital filter is appropriate. Because the oversampling factor was k, noise is pushed out to higher frequencies. By filtering at fs/2, most of the noise will be out of band.



4. In a typical first-order modulator, the input signal is sent to a difference block where the feedback signal is being subtracted from it. The resulting signal is sent to an integrator and the comparator acts on the integrator's output. The comparator compares a reference voltage with the integrator's output and generates a "high" or "low," accordingly. In turn, the sub-DAC uses the output of the sub-ADC and generates one of the two available reference voltages. This reference voltage is passed to the difference block to be subtracted from the input again. This feedback forces the DAC's output average to be equal to the input signal. The DAC's output is an analog representation of its input, which is the modulator's output.



5. In a conceptual diagram for a first-order modulator, the input voltage to the modulator is 1 V, and the DAC V_{Ref}s are ±2.5 V. The table shows how the voltages are calculated and passed around within the modulator to create the resulting bit stream.

to f_O) is given by:

$$n^2 = \int_0^{f_O} \varepsilon^2(f)df = \varepsilon_{rms}^2\left(\frac{2f_O}{f_{OS}}\right) = \frac{\varepsilon_{rms}^2}{OSR} \quad (5)$$

As the equation illustrates, oversampling reduces the in-band rms noise by the square root of the oversampling ratio *(Fig. 1)*. The reduction is quantified in:

$$n^2 = \int_0^{f_O} \varepsilon^2(f)df = \varepsilon_{rms}^2\left(\frac{2f_O}{f_{OS}}\right) = \frac{\varepsilon_{rms}^2}{OSR} \quad (6)$$

OVERSAMPLING'S EFFECT ON NOISE

While oversampling the input to the converter reduces noise, this reduction is even greater for delta-sigma modulators. In fact, higher-order modulators can further decrease noise.[1] The general formula for calculating the noise of a modulator with an order of L and OSR of M is given by:

$$n = \varepsilon_{rms}\left(\frac{\pi^L}{\sqrt{2L+1}}\right)\left(\frac{1}{M}\right)^{L+\frac{1}{2}} \quad (7)$$

Note that Equation 6 could be obtained from Equation 7 for the case in which no delta-sigma modulation is used. In that case, the order of modulation would be considered zero.

NOISE SHAPING

By oversampling, the noise spectrum is distributed over a wider frequency range. The next step in a sigma-delta is shaping the noise and pushing most of the noise spectrum to higher frequencies so the in-band noise is reduced significantly. This concept is called noise shaping *(Fig. 2)*. This simple feedback system can be represented by:

$$Y = (X - Y) * \frac{1}{f} + Q(n) \quad (8)$$

$$Y = \frac{X}{1+f} + \frac{Q(n) * f}{1+f} \quad (9)$$

Note that in Equation 9, as frequency approaches zero, Y approaches input component X. As the frequency increases, the first term (with the input signal component) approaches zero, and the output approaches Q(n). In other words, at high frequencies, the output consists mostly of quantization noise. Overall, it seems as if a low-pass filter is acting on the signal in the forward path and a high-pass filter is acting on noise in the feedback path. Noise shaping has been achieved! After that, all that needs to be done is to filter out the noise at high frequencies *(Fig. 3)*.

HOW THE MODULATOR WORKS

A first-order delta-sigma modulator comprises an integrator, a comparator that acts as a sub-ADC, and a sub-DAC *(Fig. 4)*. The sub-DAC can be as simple as a multiplexer that switches between two reference voltages. Latch operation is usually embedded in the comparator.

OVERSAMPLING'S EFFECT ON SNR

Oversampling improves signal-to-noise ratio (SNR). When noise power is reduced, an increase in SNR is expected. From a quantitative point of view, starting with the quantization noise for non-oversampled converters obtained by Equation 2, the theoretical SNR value for quantized noise is expressed by the ratio of input signal to noise signal:

$$SNR = 20\log\left(\frac{V_{In}(rms)}{V_{Noise}(rms)}\right) = 20\log\left(\frac{V_{Ref}\,(2\sqrt{2})}{\Delta/\sqrt{12}}\right) \quad (10)$$

$$SNR = 20\log\left(\sqrt{\frac{3}{2}} * 2^N\right) = 6.02N + 1.76\ dB \quad (11)$$

where N is the number of bits in the converter. Equation 6 expresses the noise power for an oversampled converter. Using Equations 6 and 10, the SNR for a converter with an oversampling ratio of OSR could be calculated as:

$$\begin{aligned} &SNR = 10\log\left(\sqrt{\frac{3}{2}} * 2^{2N}\right) + 10\log(OSR) \\ &SNR = 6.02N + 1.76\ dB + 10\log(OSR) \\ &lets \\ &OSR = 2^M \\ &M = 1,2,3... \\ &SNR = 6.02N + 1.76\ dB + 10\log 2^M \\ &SNR = 6.02N + 1.76\ dB + m \bullet 3\ dB \end{aligned} \quad (12)$$

SNR improves by 3 dB, or 0.5 bit, each time the sampling frequency is doubled. For example, a 16-bit converter has a theoretical value for SNR of about 98 dB. But with an oversampling ratio of 8, the SNR is increased to 107 dB for an increase of 3 dB/octave, or 9 dB in total.

EFFECT OF HIGHER-ORDER MODULATORS ON SNR

Using higher-order modules, delta-sigma will further improve SNR. A second-order modulator improves SNR by 15 dB for each doubling of oversampling ratio. The improvement that is achieved for each doubling of oversampling ratio generally can be calculated from:

$$3(2L + 1)\text{dB} \quad (13)$$

VOLTAGE CALCULATIONS				
V_{In} = 1	Summing node	Integrator V_O	Comparator	DAC
	1	1	H	2.5
	1 – (2.5) = –1.5	1+ (– 1.5)= –0.5	L	–2.5
	1 – (–2.5) = 3.5	(–0.5) + 3.5 = 3	H	2.5
	1 – (2.5) = –1.5	3 + (–1.5) = 1.5	H	2.5
	1 – (2.5) = –1.5	1.5 + (–1.5) = 0	H	2.5
	1 – (2.5) = –1.5	0 + (–1.5) = –1.5	L	–2.5
	1– (–2.5) = 3.5	(–1.5) + 3.5 = 2	H	2.5
	1 – (2.5) = –1.5	2 + (–1.5) = 0.5	H	2.5

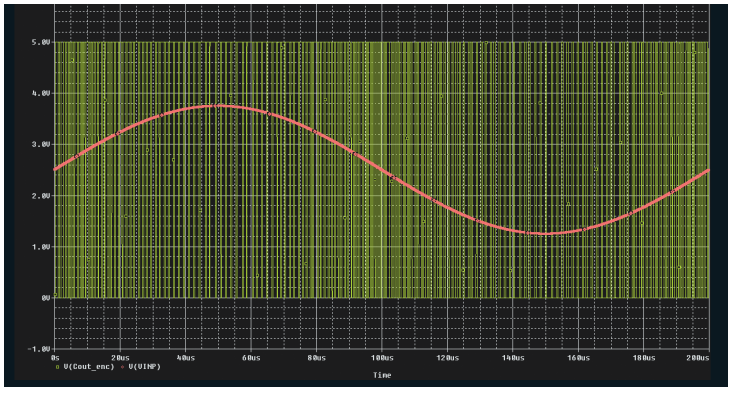
for each doubling of OSR. Equation 13 also shows that for a first-order modulator (where L = 1), there is a 9-dB improvement for every oversampling ratio of two. For a second-order modulator (L = 2) with the same OSR, this improvement increases to 15 dB—that is, there is a 6-dB improvement for each additional order of modulator.

HIGHER-ORDER MODULATORS

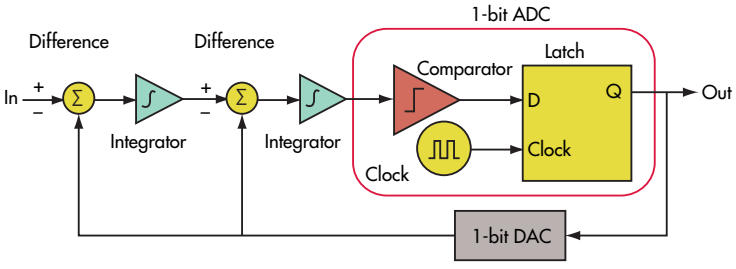
Since the modulator's output is a digital bit stream, it is hard to visualize and check the correctness of the digitized input signal at its output *(Fig. 5 and table)*. For example, code 10111011 is obtained by reading the comparator's output for each comparison. The full scale in this example is (2.5 – (–2 .5)) = 5 V.

On a 5-V scale, since the lower reference is sitting at –2.5 V, a 1-V signal will be 3.5 V above the lower reference. This is 0.7 of the full scale (3.5/5 = 0.7). The resulting code (HLHHHLHH or 10111011) has six highs and two lows, so six out of eight of the bit-stream codes are high. Thus, the average value is 6/8 = 0.75. This average value is close to the actual value of the input (0.7).

If one continues the operation and obtains more bits for the table, the average value gets closer and closer to 0.7. For this type of modulator, it is understood that for values that are closer to $+V_{Ref}$, the modulator generates more highs. For input values that are closer to $-V_{Ref}$, the modulator generates more lows. A typical sine-wave input generates a code that has more highs or lows at its two peaks. As the input gets closer to



6. The A sine wave and the resulting bit-stream out of the first-order modulator show the various density of ones and zeros.



the mid-range, on average, the resulting number of ones and zeros becomes comparable *(Fig. 6)*. Typically, the modulator takes an order that is greater than one *(Fig. 7)*.

The bit stream output by the model of a sixth-order modulator is followed by a decimation filter to form a 24-bit delta-sigma ADC, resulting in this output. Again, as the input amplitude is increased, the modulator generates more ones and, moving toward the lowest voltage of the input, more zeros *(Fig. 8)*. ed

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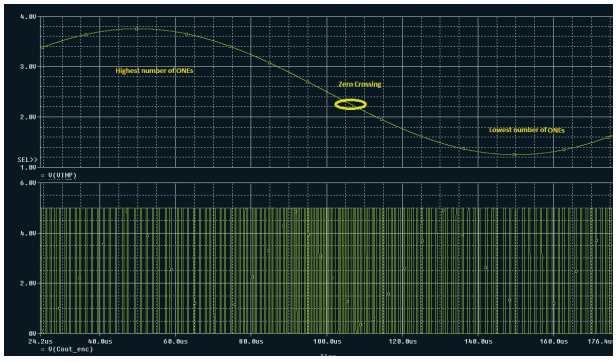
7. The order of modulator dictates the order of filter that follows. Generally, the order of the filter is equal to the order of modulator, plus one.



8. The bit stream output by the model of a sixth-order modulator is followed by a decimation filter to form a 24-bit delta-sigma ADC, resulting in this output. Again, as the input amplitude is increased, the modulator generates more ones, and, moving toward the lowest voltage of the input, more zeros.

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9. For more information on data converters, visit www.ti.com/dataconverters-ca.

ARASH LOLOEE is a Member of TI's Group Technical Staff. As Senior IC Design Engineer, he is responsible for designing transistor- to system-level projects. He received his PhD in EE and MSEE from Southern Methodist University and his BS in physics from the University of North Texas. He also was a lecturer at the University of Texas at Dallas from 2005 to 2011, where he taught various analog-related topics. He has three patents, with one pending.

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