Politecnico di Torino
III Facoltà di Ingegneria

Lab 1 Report
Integrated Systems Architecture

Master degree in Computer Engineering

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CHAPTER 1

Introduction

Our assignment was to implement a 2nd order IIR filter on 12 bits. For this architecture we have implemented, as required, first a Matlab model, then a C model and finally the actual VHDL model. A note on the filter order: to obtain its value we have considered the space character in "Dai Prà".

As required, we have also created a GitHub repository, available at the following link: `https://github.com/leoizzi/isa_labs/tree/main/lab1`.

CHAPTER 2

IIR

2.1 Matlab model

2.2 C model

2.3 VHDL model

CHAPTER 3

IIR Lookahead