Digital Integrated Circuits

#Homework 2 2024.10.11 (Due: 10.18 15:30 ED520)

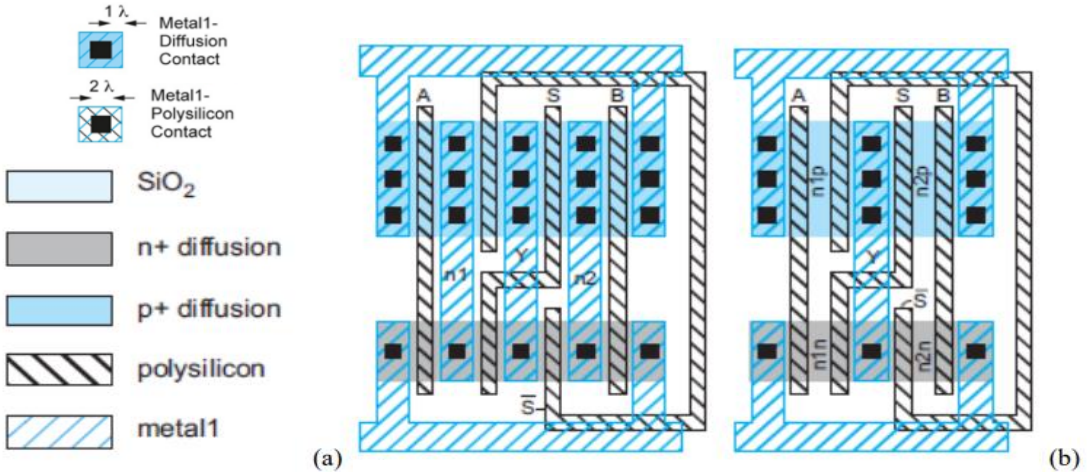
Given VDD=0.8V, W_{min}=64nm, L_{min}=32nm with resolution of 1nm; Use Low V_t CMOS in this homework. Please submit your SPICE to E3.

(1) Layout (40%)

A. Draw the circuit schematic of the attached layout (a) and (b). The signal name each node shall be marked at the schematic. **Explain** which circuit has higher speed. (20%)

B. Indicate the W/L ratio of each transistors in both (a) and (b) and AD, AS in terms of λ. (10%)

C. Mark the design rules in (a) and (b) that determine the width of this layout. (10%)



(2) Timing and Power Analysis (60%)

A. Design a two inputs NAND logic gate as shown in the following figure such that it has the logic threshold of 0.45*VDD (when two inputs have the same voltage). Indicate the W/L of PMOS and NMOS and show the SPICE simulation results of VTC. (15%)

B. Run SPICE to get the followings: (25%)

i. output capacitances and input capacitance of the NAND circuit.

ii. Leakage power dissipation when V_{in} = logic 1, and V_{out} = logic 0.

iii. Leakage power dissipation when V_{in} = logic 0, and V_{out} = logic 1.

C. Do the timing analysis of the NAND circuit which has a fanout of two NANDs. Input signal is a pulse waveform with duration of 2ns (with $t_r = t_f =$ 0.4ns defined as 0%-100%, duty = 0.5) Run two cases by using SPICE (5ns) to get the timing (t_{df} and t_{dr}) and power waveform: (20%)

i. A=1 and B changes from 0 to 1.

ii. B=1 and A changes from 0 to 1

List in table form with the t_{df}, t_{dr}, average power and peak power of the NAND circuits.

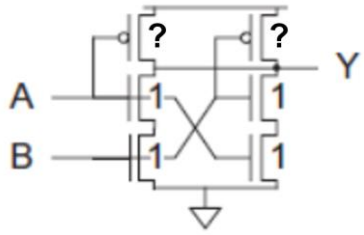


Fig. 2: Perfectly Symmetric 2-input NAND gate