DIC HW1

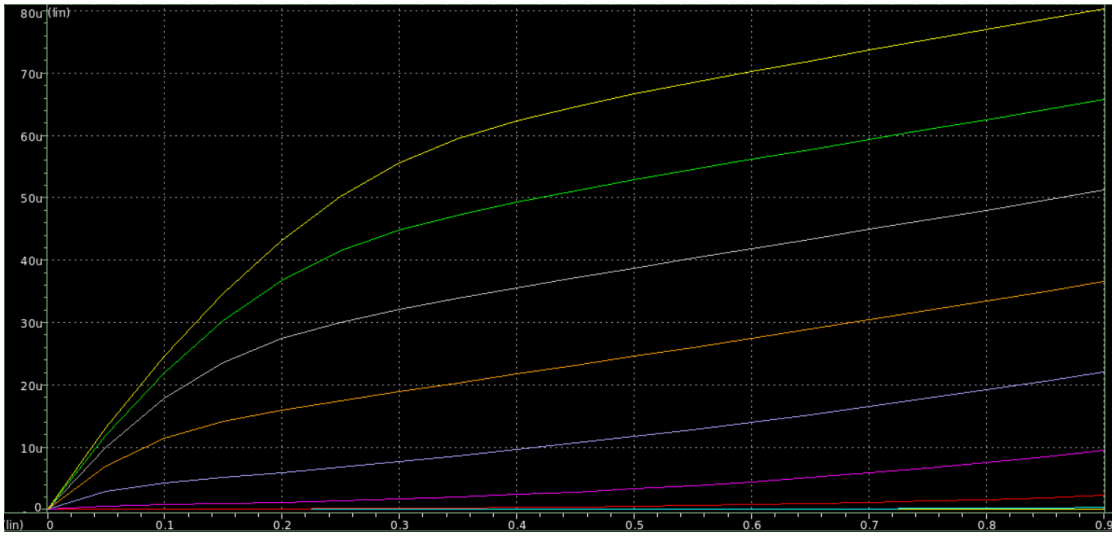
313580059 李元睿

Given VDD=0.9V, Wmin=64nm, Lmin=32nm with resolution of 1nm; there are three kinds of Vt: High Vt, Medium Vt and Low Vt CMOS

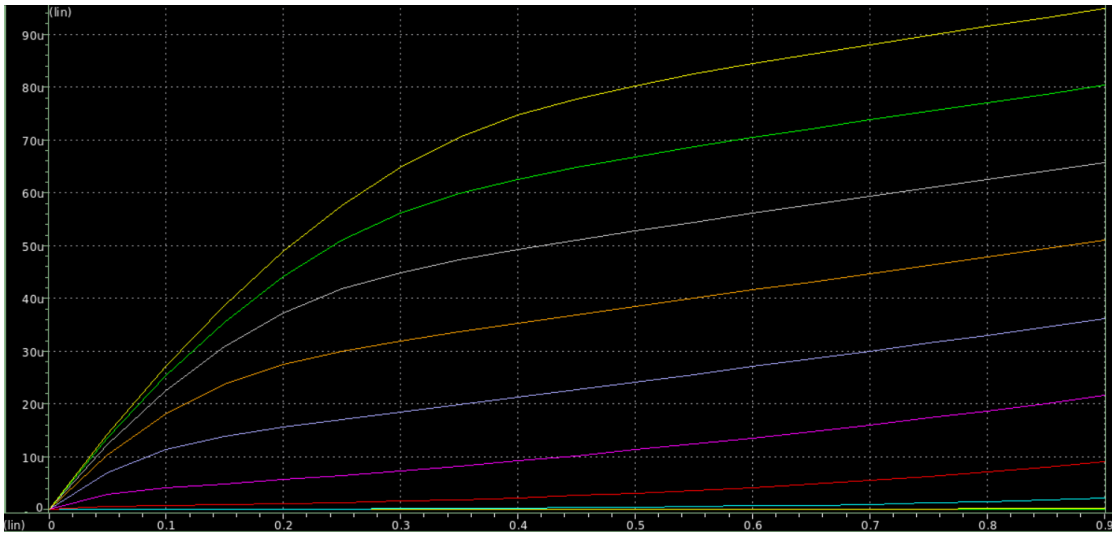
(1) MOS and Inverter with medium threshold voltages (30%)

A. Run SPICE to draw the I-V DC curves for PMOS and NMOS with minimum feature size using High Vt, Medium Vt, and Low Vt respectively. (24%)

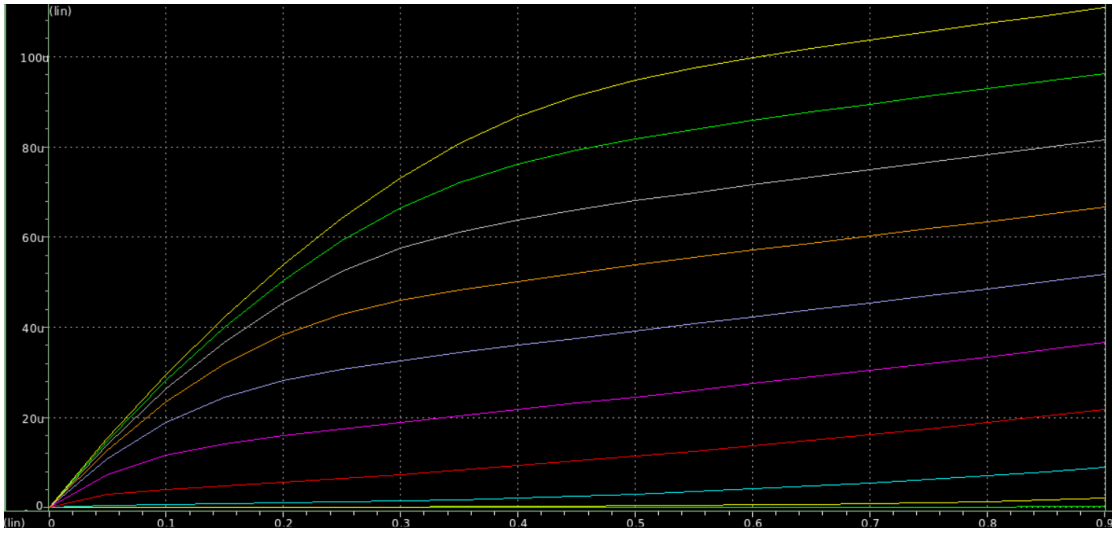
1.NMOS with High Vt:



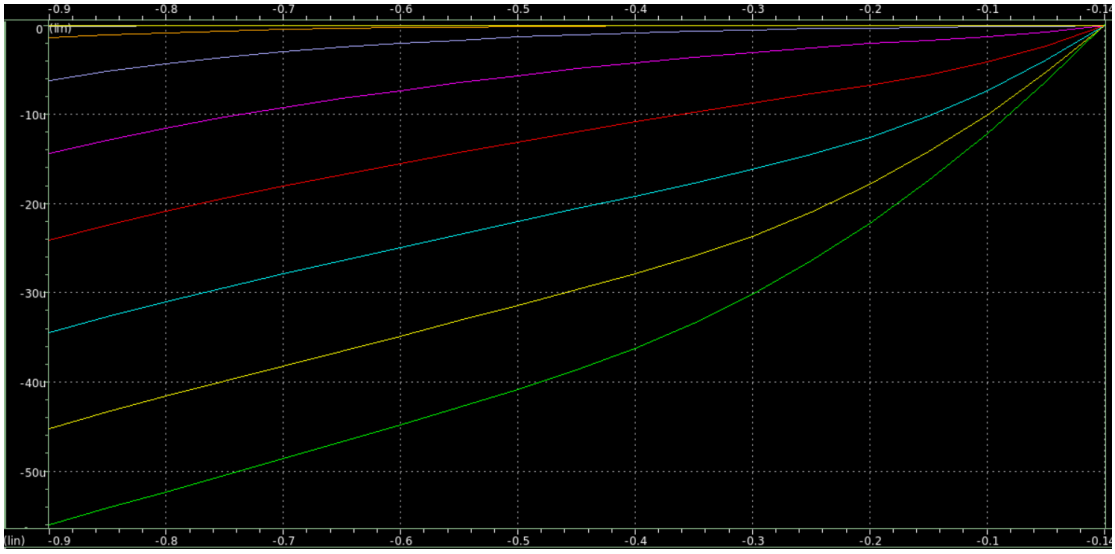
2.NMOS with Medium Vt:



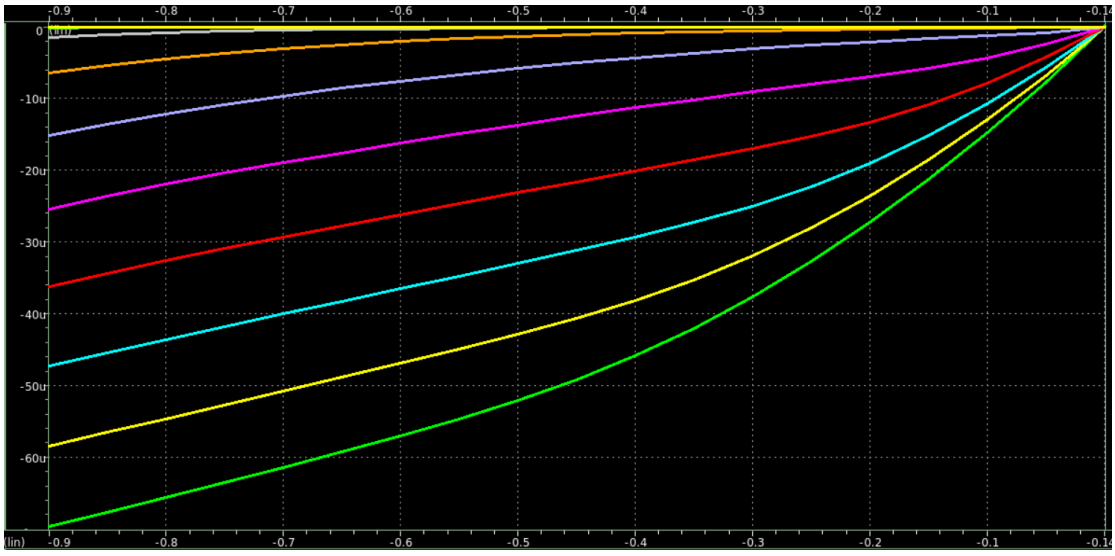
3.NMOS with Low Vt:



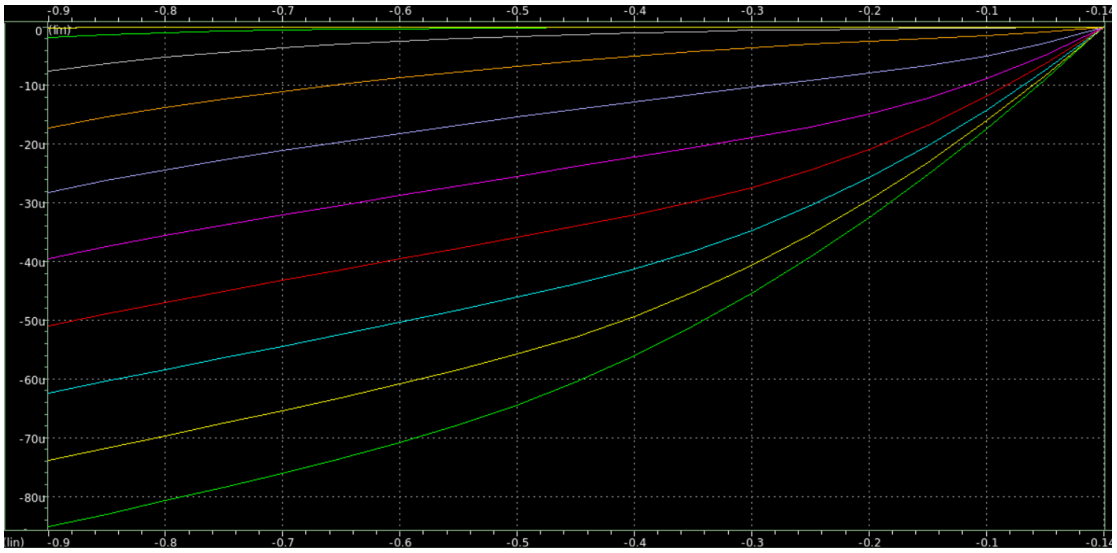
4.PMOS with High Vt:



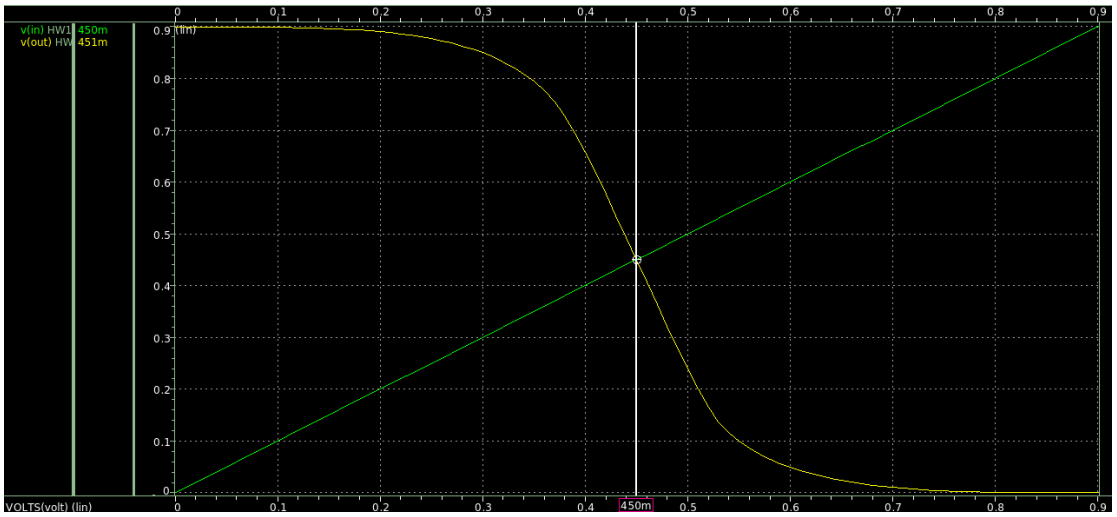
5.PMOS with Medium Vt:



6.PMOS with Low Vt:



B. Keep L equals to Lmin, design the W of each transistor using medium Vt such that the logic threshold of inverter is at 0.5VDD. Discuss your design procedures and the way you choose your MOS dimensions. Run SPICE to verify your results. (6%)



```
14    MN out in 0 0 nmos_svt W=64n L=32n
15    MP out in vdd vdd pmos_svt W=114n L=32n
```

根據題目規定，L 設定在 32nm。然後為了達到 logic threshold 為 0.5VDD，也就是 0.45V，我固定住 nmos 的 W=64nm，開始調整 pmos 的 W，最終經過微調多次，我發現在 W=114nm 的時候可以達到 logic threshold 為 0.5VDD。

(2) Design a CMOS schmitt trigger shown at Fig. 1(b) such that V+ = 0.54-0.57V and V - = 0.36-0.33V with CT=VDD (70%)

A. Discuss the difference between Fig. 1(a) and (b). Give the W/L of each device (in table form) of Fig. 1(b) with CT=VDD and discuss your design procedures to determine the size of each transistor using medium Vt. (30%)

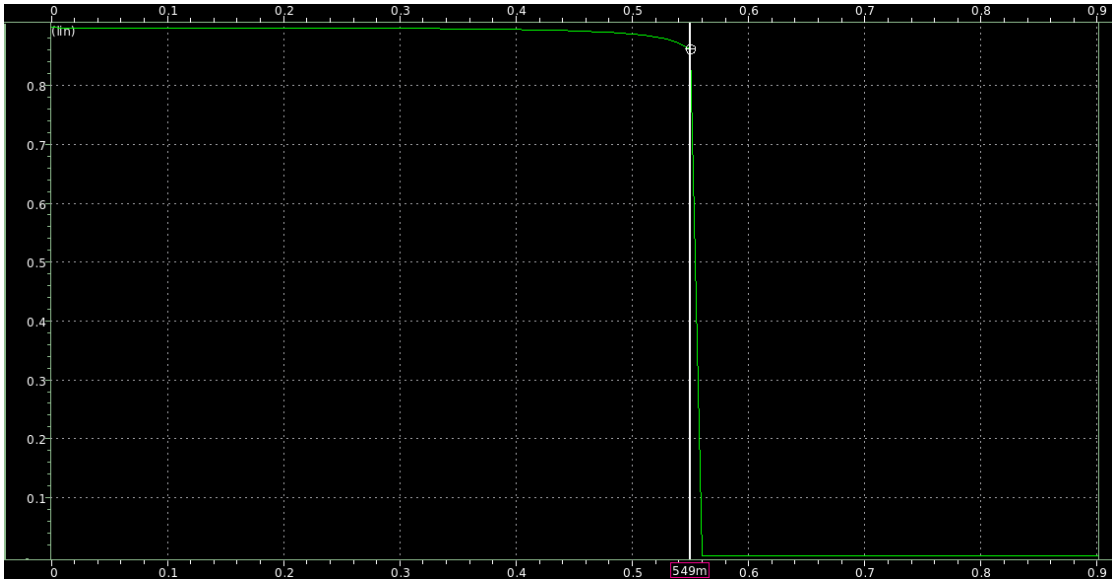
Schmitt Trigger with Controllable Hysteresis 與普通的施密特觸發器主要區別在

於回滯的範圍（即 V+和 V−的差距）是可調的。在普通的施密特觸發器中，回滯範圍是固定的，設計完成後無法靈活調整；而具有可控回滯的施密特觸發器能夠根據外部控制信號(V_{CT})來改變這個範圍。

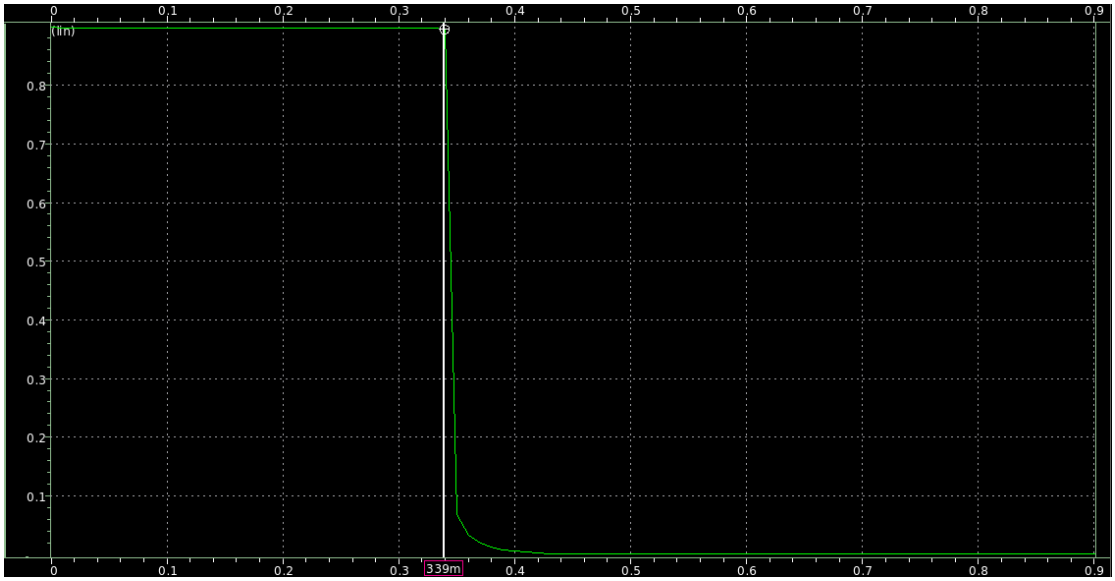
```
14  MN1 n1 in 0 0 nmos_svt W=70n L=32n
15  MN2 out in n1 n1 nmos_svt W=64n L=32n
16  MN3 n3 out n1 n1 nmos_svt W=300n L=32n
17  MN4 vdd vdd n3 n3 nmos_svt W=300n L=32n
18  MP1 p1 in vdd vdd pmos_svt W=90n L=32n
19  MP2 out in p1 p1 pmos_svt W=80n L=32n
20  MP3 p1 out p3 p3 pmos_svt W=300n L=32n
21  MP4 p3 vdd 0 0 pmos_svt W=300n L=32n
```

附圖則為 8 個 MOS 的 W/L，而根據老師上課所說的以及網路資源，可以知道在 NMOS 中$(W/L)_1$要大於$(W/L)_2$，且 V+會隨著$\frac{(W/L)_1}{(W/L)_3}$的下降而上升。同理，PMOS 對 V−的影響也是一樣。因此根據這個原則我先固定住 MN2 以及 MP2 的 W，然後開始調整 MN1 對 MN3、MN4 以及 MP1 對 MP3、MP4 的比值，最後調整出附圖的數據，V+能達到 0.549V，V-能達到 0.339V。

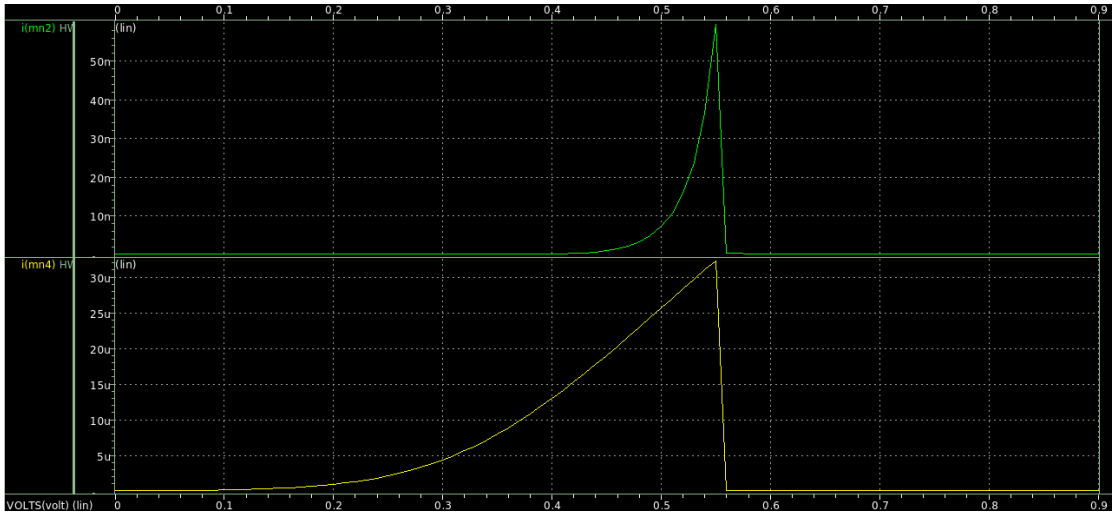
B. Run SPICE to verify your results. Your report must have the figures of VTC, IN2 vs Vin, and IN4 vs Vin (20%)



此圖顯示出 V+能達到 0.549V

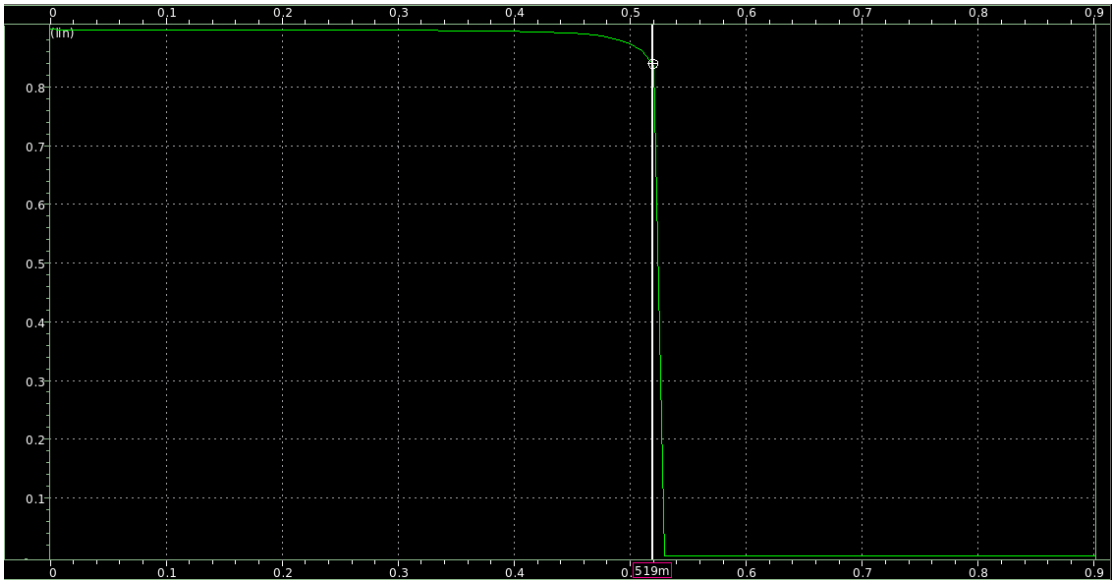


此圖顯示出 V-能達到 0.339V

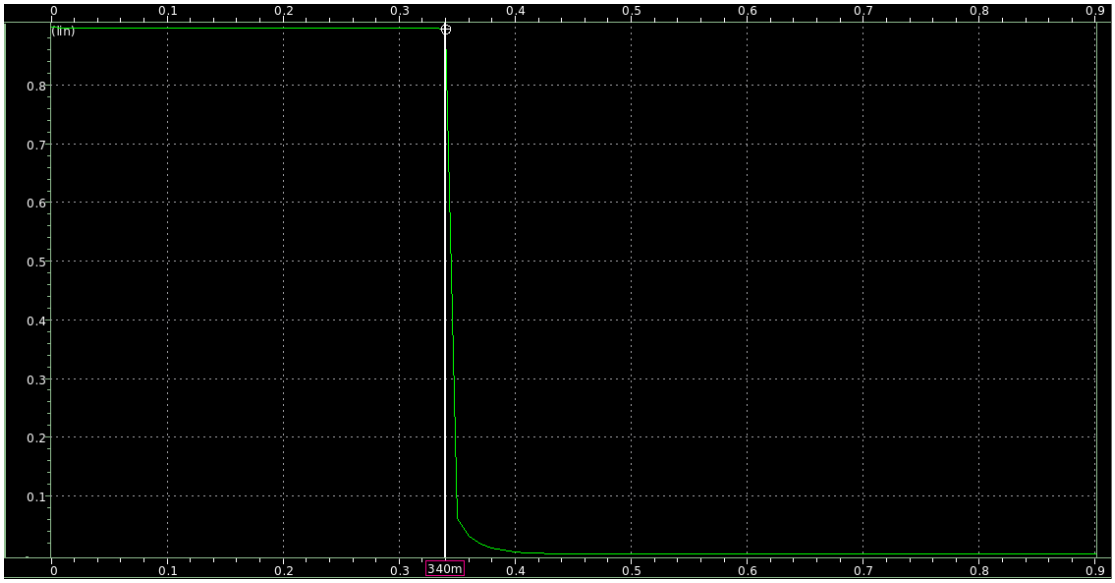


在此圖中，綠色的圖是I_{N2} vs V_{in}的圖。黃色的圖則是I_{N4} vs V_{in}的圖。

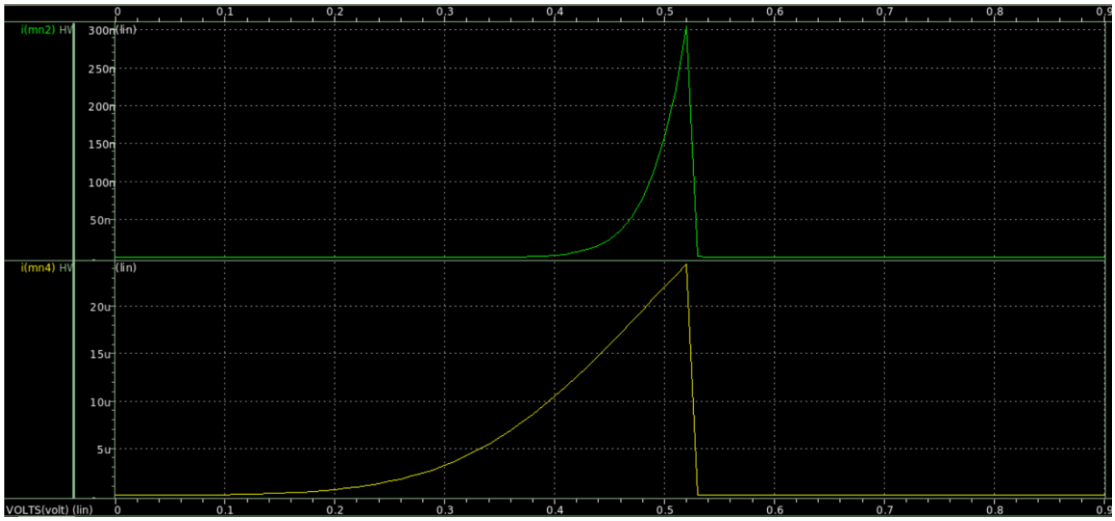
C. Use the same size as in part A, and modify CT to 0.8VDD. Repeat part B to have figures to indicate the new V- and V+ (20%)



此圖顯示出經過調整 CT 到 0.8VDD 後的 V+降低到 0.519V



此圖顯示出經過調整 CT 到 0.8VDD 後的 V-升高到 0.340V



在此圖中，綠色的圖是I_{N2} vs V_{in}的圖。黃色的圖則是I_{N4} vs V_{in}的圖。