Digital Integrated Circuits

Homework#5 2024.11.20 (Due: 11.27 17:30 ED520)

Using 32nm technology with VDD = 0.9V, L = 32nm, medium V_t CMOS process.

Rise time and fall time of input signals are 0.02ns (0V-0.9V)

32nm tech. path: /RAID2/COURSE/dic/dicTA01/DIC_2024_Fall/bulk_32nm.l

(1) A 6T SRAM is shown in Fig. 1. Design the transistor widths for the SRAM to ensure proper functionality during both read and write operations. (20%) Generate the read and write operation curves for your SRAM cell, similar to those shown in Fig.2. (20%)

(2) Determine the butterfly curve and the quiescent Static Noise Margin (SVM_{hold}) of your SRAM cell in TT corners. (20%) Determine the butterfly curve and the read Static Noise Margin (SVM_{read}) of your SRAM cell TT corners. (20%)

(3) Design a 6T SRAM cell array under TT corner as shown in Fig. 3. Set the initial value of A=0 and A_b=1 in $SRAM_0$. Set the initial value of A=1 and A_b=0 in $SRAM_1$~$SRAM_{64}$. Perform a proper read operation (W_0~W_{63}=0, phi=0 → phi=1 → W_0=1) for $SRAM_0$. Generate the read operation curve and discuss the result to that of (1). What makes the difference? (20%)

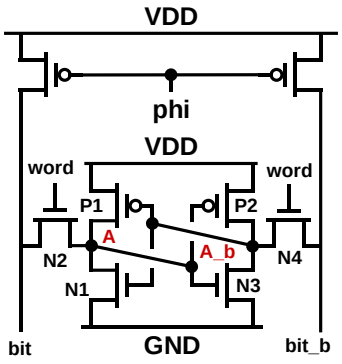

Fig. 1. 6T SRAM Cell

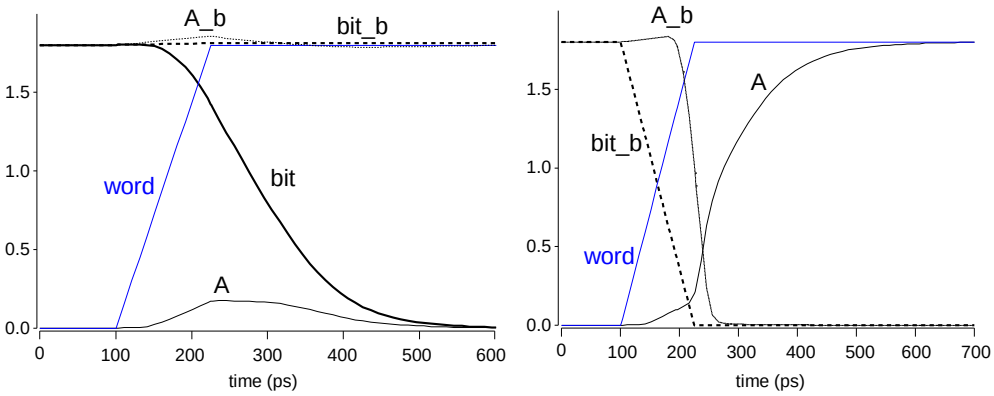

Fig. 2. Read and Write operation of the SRAM cell

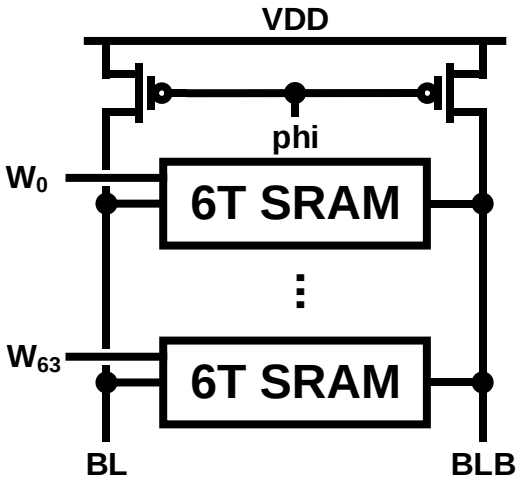

Fig. 3 6T SRAM cell array