Digital Integrated Circuits

Homework#3 2024.10.30 (Due: 11.06 17:30 ED520)

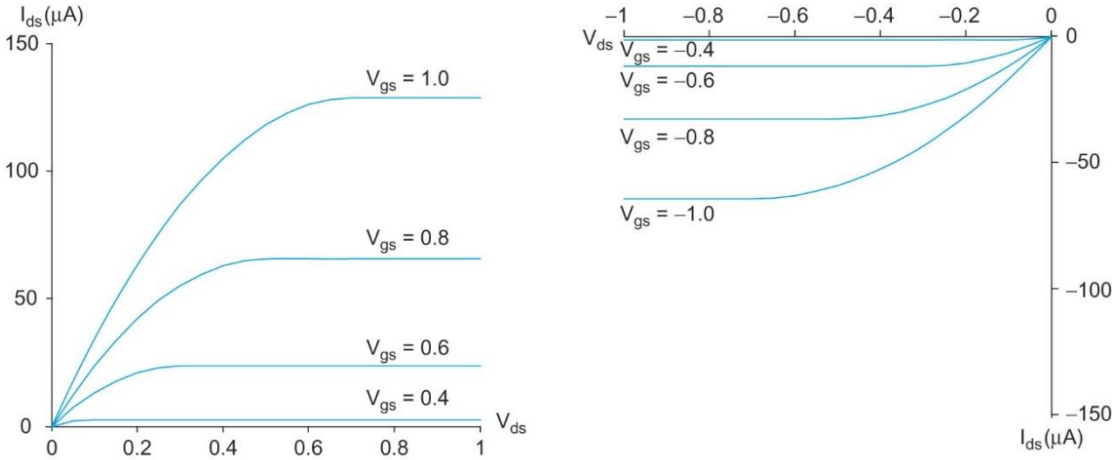
Using 7nm FinFET devices with VDD = 0.8V, FF process corner and medium V_t CMOS process. Rise time and fall time of input signals and clock are 0.02ns (0V-0.8V)

7nm tech. path: /RAID2/COURSE/dic/dicTA01/DIC_2024_Fall/7nm_files

(1) MOS and Inverter (30%)

A. Run SPICE to draw I-V DC curve (like the figure below with Vgs = 0.8, 0.6, 0.35) for PMOS and NMOS with Fin n=1. Mark maximum I_{DS} (Vgs=Vds=VDD) in table form. **Discuss the results.**

B. Keep a unit size inverter with NMOS n=1 and choose the n of PMOS for n=1 and 2 to show the logic threshold voltage. Run SPICE to verify your results by showing simulated waveforms.



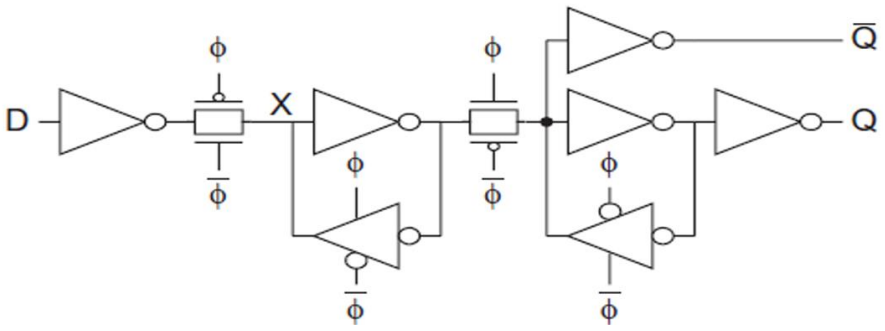
(2) Ring Oscillator (20%)

According to the results of (1)B, design a 3-stage inverter-based ring oscillator with unit size inverter. Set the initial voltage of each node so that it can oscillate. Show the SPICE simulation results of oscillation frequency and power consumption in table form.

(3) Assume both ϕ and ϕ^- are available, design a static D register as shown in the figure below with proposed size of NMOS and PMOS to have better t_{setup}, t_{pcq}, t_{pdq}, and t_{hold}. The loading of Q and Q^- have 4 unit size inverters as loading. Both D and CLK has rise time and fall time of 0.1ns (0V-0.8V). (50%)

A. **Explain your sizing principle** of each MOS to have least t_{setup}, t_{pcq}, t_{pdq}, and t_{hold} for logic 1 and 0. (Explain that by changing which transistors would affect each timing respectively)

B. Run SPICE to verify your results and list the results (size of each transistor and four kinds of timing) in table form for part A.


D
X
Q
Q
ϕ
ϕ
ϕ
ϕ
ϕ
ϕ
ϕ
ϕ