# Digital Integrated Circuits

## Homework#4 2024.11.06 (Due: 11.13 17:30 ED520)

**Using 7nm FinFET devices with VDD = 0.8V, FF process corner and medium $V_t$ CMOS process. Rise time and fall time of input signals and clock are 0.02ns (0V-0.8V)**

**7nm tech. path: /RAID2/COURSE/dic/dicTA01/DIC_2024_Fall/7nm_files**

A 4-bit ripple carry adder shown in Fig. 1 is designed with fully complementary static logic gate of full adder (FA). Input signals are A[3:0], B[3:0], and $C_{in}$. Outputs are SUM[3:0] and $C_{out}$.

(1) Try to design the fastest adder when each input signal is driven by one unit size inverter. For the output loads, 5 unit size inverters are used for each output signal. First, show your block diagrams in terms of the 1-bit FA. Second, show the circuit schematic of the FA. Use logic effort concepts (do not have to write down the procedure) to design **transistor widths. Describe your design concept.** (40%)

(2) Based on the design of (1), run SPICE to find the propagation delay (As shown in Fig. 2, with pattern from **IA [3:0] = 4'b1111, IB[3:0] = 4'b0000, $IC_{in}$ = 1'b1** to **IA[3:0] = 4'b1111, IB[3:0] = 4'b0000, $IC_{in}$ = 1'b0**). Determine the maximum propagation delay of the Ripple Carry Adder (exclude the load inverters). (20%)

(3) Run SPICE of the ripple carry adder with each output load equals to 4 unit size inverter. Determine the **average, peak, and leakage** power dissipation and energy per bit, respectively when simulating at the working frequency in (2). (20%)

(4) Add pipelining stages as shown in Fig. 4 into the 4-bit ripple carry adder, with the D register given in Fig. 3. Run SPICE to find the propagation delay time (with pattern from **IA [3:0] = 4'b0000, IB[3:0] = 4'b1111, $IC_{in}$ = 1'b0** to **IA[3:0] = 4'b0000, IB[3:0] = 4'b1111, $IC_{in}$ = 1'b1**) between pipelining stages to determine the **maximum working frequency** of the clock.

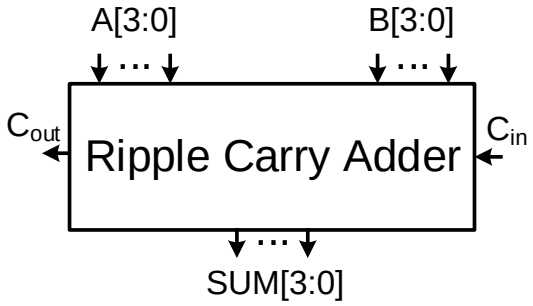


Fig. 1. Ripple Carry Adder

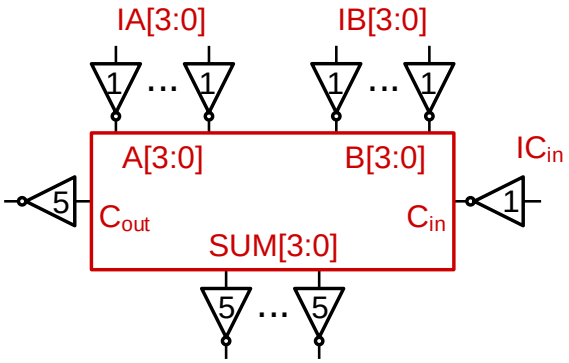


Fig. 2. Ripple Carry Adder

**Table I. Input Pattern for (3)**

| Average and Peak Power | Leakage Power |
|---|---|
| A[3:0] = 0000, 0001, … 1111 | A[3:0] = 0000 |
| B[3:0] = 1111, 1110, … 0000 | B[3:0] = 1111 |
| $C_{in}$ is 0/1 by turns | $C_{in}$ = 0 |

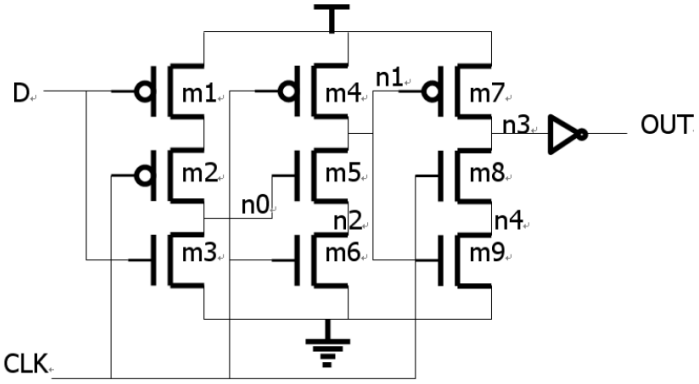


Fig. 3. Schematic of TSPC Register

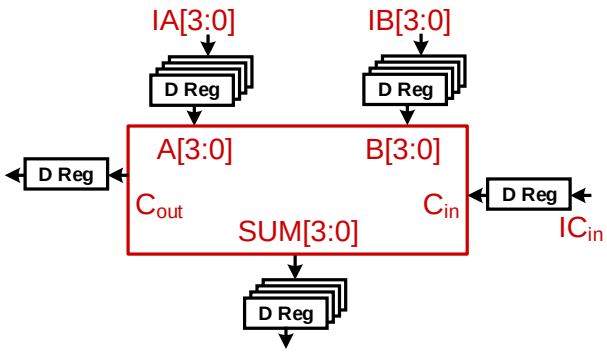


Fig. 4.