# **Digital Integrated Circuits**

## Homework#6 2024.12.12 (Due: 2025.01.08 23:59 ADFP Cloud 2.0)

- Using ADFP standard  $V_T$  technology with VDD = 0.8V
- Tutorial File:

/RAID2/COURSE/2024\_Fall/DIC/DICTA01/DIC\_Document/DIC2024\_A DFP-Layout-Tutorial.pdf

- **Design Rules:** ~/ADFP\_PDF/ADFP039\_N16ADFP\_DRM\_V1.1\_1.pdf
  - (1) Design an inverter with arbitrary number of fin in Virtuoso using:
    - i. Schematic with Pre-Sim Simulation. (Input Waveform  $0 \rightarrow 1 \rightarrow 0$  with rise time  $0 \times 0.8 \times 0.8 \times 0.8 \times 0.8 \times 0.8 \times 0.8 \times 0.9 \times 0.9$
    - ii. Layout with 0 DRC error (except dummy and density issues), 0 LVS error, and Post-Sim Simulation. (20%)
  - (2) Design a 4-bit **Ripple Carry Adder** in Virtuoso using:
    - i. Schematic with Pre-Sim Simulation. (rise time and fall time = 10ps with following input signals) (20%)

Pattern	time	A[3:0]	B[3:0]	Cin	Out[4:0]
0	0ps	4'b0000	4'b0000	1'b0	5'b00000
1	10ps	4'b1010	4'b0101	1'b1	5'b10000
2	10ps + 2T	4'b1100	4'b0011	1'b0	5'b01111
3	10ps + 3T	4'b1111	4'b1111	1'b1	5'b11111

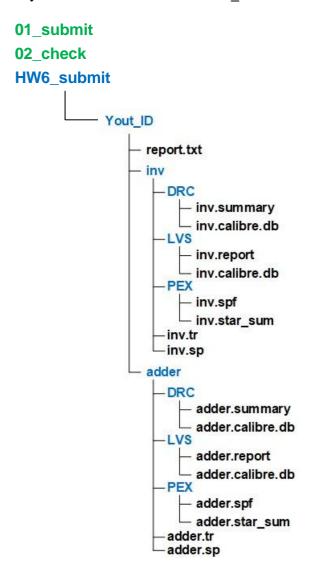
(Note: T = maximum propagation delay of your adder)

- ii. Layout with 0 DRC error (except dummy and density issues), 0 LVS error, and Post-Sim Simulation. (30%)
- (3) Performance Ranking (Area \* Propagation Delay) (20%)
  - i. Area of Chip Boundary (µm²)
  - ii. Propagation Delay (ps): (Delay of [Pattern1] + [Pattern2] + [Pattern3])

#### **Submission:**

- 1. Make a directory using Your\_ID
- Create inv directory, adder directory, and copy report.txt in Your\_ID
   Template file of report.txt:
  - /RAID2/COURSE/2024\_Fall/DIC/DICTA01/DIC\_Final\_Submission/report.txt
- 3. create **DRC**, **LVS**, **PEX** directories and organize them as the hierarchy below.

- 4. Edit **report.txt** and make sure you have submitted all the files.
- 5. Link submission scripts: In -s ~DICTA03/01\_submit
  In -s ~DICTA03/02\_check
- 6. Create a "HW6\_submit" folder: mkdir HW6\_submit"HW6 submit" should be created in the same directory as the scripts.
- 7. Put your submission files in "HW6\_submit".



8. Run 01\_submit: ./01\_submit

```
[Info] Now start tar zcvf HW6_submit_course.tar.gz
HW6_submit/
HW6_submit/Tutorial.jpg
[Success] HW6_submit_course.tar.gz
[Info] Deadline check OK ...
[Info] File check OK ...
[Info] Your file will be submitted to: HW6
[Info] Are you sure you want to submit your design file?(y/n):
```

### 9. Type "y" to continue.

Please make sure there are no errors, such as "file not found", after running ./01\_submit.

```
[Info] Now start tar zcvf HW6_submit_course.tar.gz
HW6_submit/
HW6_submit/Tutorial.jpg
[Success] HW6_submit_course.tar.gz
[Info] Deadline check OK ...
[Info] File check OK ...
[Info] Your file will be submitted to: HW6
[Info] Are you sure you want to submit your design file?(y/n):y
[Info] Now submit HW6_submit_course.tar.gz file to system.
[Success] Copying Sucessfully.
               Submit Report
Make sure there
Result
      : HW6 has been submitted.
Submission time: Mon Dec 16 04:31:28 PM CST 2024
                                                      are no any error
------
      -- Congratulations !!
_____
course@icssl-4090:~/Project/312510232/File_Submission$
```

#### 10. Run 02\_check: **./02\_check**

The submission file will be downloaded in the "HW6\_submit\_[your server account]\_check" folder.

Please make sure there are no errors, such as "file not found", after running ./02\_check.

```
HW6_submit_course.tar.gz has been downloaded!

It was put in the HW6_submit_course_check folder!!
```