SOC Design Laboratory

Lab4-1 Execute Code in User Memory

311651055_林柏宇
交大電物碩二

Github：https://github.com/leolin0501/soclab.github.io/tree/main/Lab4
HackMD：https://hackmd.io/gzN6anM4SDKoXhKOAAJzDA

一、電路設計：

1. FIR 演算法：

   第一步：為了使 combination 時，要累加的 outputsignal[]，因為讀到沒有初始化記憶體空間的未知值而出錯，先設置一個迴圈將 outputsignal[]所有值歸零。

   第二步：設置一個雙迴圈，執行 convolution 運算。

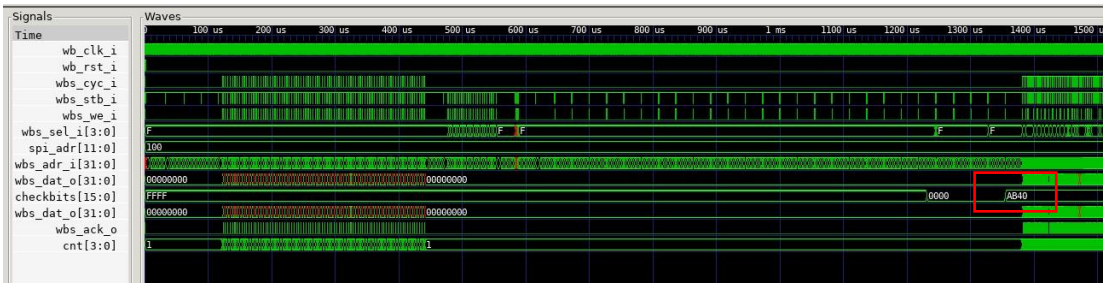
   $$(inputSignal * taps)[n] = \sum_{k=-\infty}^{\infty} inputSignal[k] \cdot taps[n-k]$$

2. BRAM：為滿足 32KB，N 設置 10。

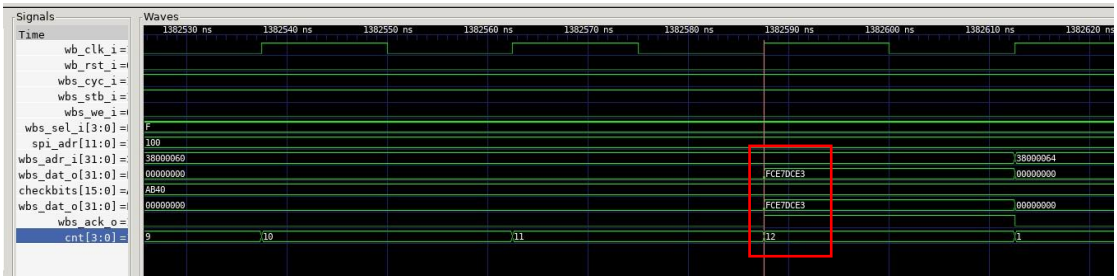
二、波型呈現：

```
ubuntu@ubuntu2004:~/course-lab_4/test/testbench/counter_la_fir$ source run_clean
ubuntu@ubuntu2004:~/course-lab_4/test/testbench/counter_la_fir$ source run_sim
Reading counter_la_fir.hex
counter_la_fir.hex loaded into memory
Memory 5 bytes = 0x6f 0x00 0x00 0x0b 0x13
VCD info: dumpfile counter_la_fir.vcd opened for output.
LA Test 1 started
LA Test 2 passed
ubuntu@ubuntu2004:~/course-lab_4/test/testbench/counter_la_fir$
```

跑模擬的結果，通過。



波型呈現，確定有讀取到 AB40(十進制：43840)



Counter 數到 12 的同時，wbs_ack_o 會升起，接收 BRAM 讀出的值。

三、Synthesis Report：

Utilization：

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	37	0	0	53200	0.07
LUT as Logic	37	0	0	53200	0.07
LUT as Memory	0	0	0	17400	0.00
Slice Registers	4	0	0	106400	<0.01
Register as Flip Flop	4	0	0	106400	<0.01
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

Timing report: (Frequency:100MHZ)：

Max Delay Paths

```
Slack:                   inf
  Source:                cnt_reg[1]/C
                           (rising edge-triggered cell FDCE)
  Destination:           wbs_dat_o[0]
                           (output port)
  Path Group:            (none)
  Path Type:             Max at Slow Process Corner
  Data Path Delay:       5.088ns  (logic 3.407ns (66.968%)  route 1.681ns (33.032%))
  Logic Levels:          3  (FDCE=1 LUT5=1 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------    -------------------       --------  --------    -------------------
                         FDCE                         0.000     0.000 r  cnt_reg[1]/C
                         FDCE (Prop_fdce_C_Q)         0.478     0.478 f  cnt_reg[1]/Q
                         net (fo=37, unplaced)        0.881     1.359    user_bram/Q[1]
                                                                 f  user_bram/wbs_dat_o_OBUF[0]_inst_i_1/I0
                         LUT5 (Prop_lut5_I0_O)        0.295     1.654 r  user_bram/wbs_dat_o_OBUF[0]_inst_i_1/O
                         net (fo=1, unplaced)         0.800     2.454    wbs_dat_o_OBUF[0]
                                                                 r  wbs_dat_o_OBUF[0]_inst/I
                         OBUF (Prop_obuf_I_O)         2.634     5.088 r  wbs_dat_o_OBUF[0]_inst/O
                         net (fo=0)                   0.000     5.088    wbs_dat_o[0]
                                                                 r  wbs_dat_o[0] (OUT)
  -------------------------------------------------------------------    -------------------

Slack:                   inf
  Source:                cnt_reg[1]/C
                           (rising edge-triggered cell FDCE)
  Destination:           wbs_dat_o[10]
                           (output port)
  Path Group:            (none)
  Path Type:             Max at Slow Process Corner
  Data Path Delay:       5.088ns  (logic 3.407ns (66.968%)  route 1.681ns (33.032%))
  Logic Levels:          3  (FDCE=1 LUT5=1 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------    -------------------       --------  --------    -------------------
                         FDCE                         0.000     0.000 r  cnt_reg[1]/C
                         FDCE (Prop_fdce_C_Q)         0.478     0.478 f  cnt_reg[1]/Q
                         net (fo=37, unplaced)        0.881     1.359    user_bram/Q[1]
                                                                 f  user_bram/wbs_dat_o_OBUF[10]_inst_i_1/I0
                         LUT5 (Prop_lut5_I0_O)        0.295     1.654 r  user_bram/wbs_dat_o_OBUF[10]_inst_i_1/O
                         net (fo=1, unplaced)         0.800     2.454    wbs_dat_o_OBUF[10]
                                                                 r  wbs_dat_o_OBUF[10]_inst/I
                         OBUF (Prop_obuf_I_O)         2.634     5.088 r  wbs_dat_o_OBUF[10]_inst/O
                         net (fo=0)                   0.000     5.088    wbs_dat_o[10]
                                                                 r  wbs_dat_o[10] (OUT)
  -------------------------------------------------------------------    -------------------
```

```
Slack:                    inf
  Source:                 cnt_reg[1]/C
                            (rising edge-triggered cell FDCE)
  Destination:            wbs_dat_o[11]
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        5.088ns  (logic 3.407ns (66.968%)  route 1.681ns (33.032%))
  Logic Levels:           3  (FDCE=1 LUT5=1 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         FDCE                         0.000     0.000 r  cnt_reg[1]/C
                         FDCE (Prop_fdce_C_Q)         0.478     0.478 f  cnt_reg[1]/Q
                         net (fo=37, unplaced)        0.881     1.359    user_bram/Q[1]
                                                                     f  user_bram/wbs_dat_o_OBUF[11]_inst_i_1/I0
                         LUT5 (Prop_lut5_I0_O)        0.295     1.654 r  user_bram/wbs_dat_o_OBUF[11]_inst_i_1/O
                         net (fo=1, unplaced)         0.800     2.454    wbs_dat_o_OBUF[11]
                                                                     r  wbs_dat_o_OBUF[11]_inst/I
                         OBUF (Prop_obuf_I_O)         2.634     5.088 r  wbs_dat_o_OBUF[11]_inst/O
                         net (fo=0)                   0.000     5.088    wbs_dat_o[11]
                                                                     r  wbs_dat_o[11] (OUT)
  -------------------------------------------------------------------    -------------------

Slack:                    inf
  Source:                 cnt_reg[1]/C
                            (rising edge-triggered cell FDCE)
  Destination:            wbs_dat_o[12]
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        5.088ns  (logic 3.407ns (66.968%)  route 1.681ns (33.032%))
  Logic Levels:           3  (FDCE=1 LUT5=1 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         FDCE                         0.000     0.000 r  cnt_reg[1]/C
                         FDCE (Prop_fdce_C_Q)         0.478     0.478 f  cnt_reg[1]/Q
                         net (fo=37, unplaced)        0.881     1.359    user_bram/Q[1]
                                                                     f  user_bram/wbs_dat_o_OBUF[12]_inst_i_1/I0
                         LUT5 (Prop_lut5_I0_O)        0.295     1.654 r  user_bram/wbs_dat_o_OBUF[12]_inst_i_1/O
                         net (fo=1, unplaced)         0.800     2.454    wbs_dat_o_OBUF[12]
                                                                     r  wbs_dat_o_OBUF[12]_inst/I
                         OBUF (Prop_obuf_I_O)         2.634     5.088 r  wbs_dat_o_OBUF[12]_inst/O
                         net (fo=0)                   0.000     5.088    wbs_dat_o[12]
                                                                     r  wbs_dat_o[12] (OUT)
  -------------------------------------------------------------------    -------------------


Slack:                    inf
  Source:                 cnt_reg[1]/C
                            (rising edge-triggered cell FDCE)
  Destination:            wbs_dat_o[13]
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        5.088ns  (logic 3.407ns (66.968%)  route 1.681ns (33.032%))
  Logic Levels:           3  (FDCE=1 LUT5=1 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         FDCE                         0.000     0.000 r  cnt_reg[1]/C
                         FDCE (Prop_fdce_C_Q)         0.478     0.478 f  cnt_reg[1]/Q
                         net (fo=37, unplaced)        0.881     1.359    user_bram/Q[1]
                                                                     f  user_bram/wbs_dat_o_OBUF[13]_inst_i_1/I0
                         LUT5 (Prop_lut5_I0_O)        0.295     1.654 r  user_bram/wbs_dat_o_OBUF[13]_inst_i_1/O
                         net (fo=1, unplaced)         0.800     2.454    wbs_dat_o_OBUF[13]
                                                                     r  wbs_dat_o_OBUF[13]_inst/I
                         OBUF (Prop_obuf_I_O)         2.634     5.088 r  wbs_dat_o_OBUF[13]_inst/O
                         net (fo=0)                   0.000     5.088    wbs_dat_o[13]
                                                                     r  wbs_dat_o[13] (OUT)
  -------------------------------------------------------------------    -------------------

Slack:                    inf
  Source:                 cnt_reg[1]/C
                            (rising edge-triggered cell FDCE)
  Destination:            wbs_dat_o[14]
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        5.088ns  (logic 3.407ns (66.968%)  route 1.681ns (33.032%))
  Logic Levels:           3  (FDCE=1 LUT5=1 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         FDCE                         0.000     0.000 r  cnt_reg[1]/C
                         FDCE (Prop_fdce_C_Q)         0.478     0.478 f  cnt_reg[1]/Q
                         net (fo=37, unplaced)        0.881     1.359    user_bram/Q[1]
                                                                     f  user_bram/wbs_dat_o_OBUF[14]_inst_i_1/I0
                         LUT5 (Prop_lut5_I0_O)        0.295     1.654 r  user_bram/wbs_dat_o_OBUF[14]_inst_i_1/O
                         net (fo=1, unplaced)         0.800     2.454    wbs_dat_o_OBUF[14]
                                                                     r  wbs_dat_o_OBUF[14]_inst/I
                         OBUF (Prop_obuf_I_O)         2.634     5.088 r  wbs_dat_o_OBUF[14]_inst/O
                         net (fo=0)                   0.000     5.088    wbs_dat_o[14]
                                                                     r  wbs_dat_o[14] (OUT)
  -------------------------------------------------------------------    -------------------

Slack:                    inf
```

```
Slack:                   inf
  Source:                cnt_reg[1]/C
                           (rising edge-triggered cell FDCE)
  Destination:           wbs_dat_o[17]
                           (output port)
  Path Group:            (none)
  Path Type:             Max at Slow Process Corner
  Data Path Delay:       5.088ns  (logic 3.407ns (66.968%)  route 1.681ns (33.032%))
  Logic Levels:          3  (FDCE=1 LUT5=1 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         FDCE                         0.000     0.000 r  cnt_reg[1]/C
                         FDCE (Prop_fdce_C_Q)         0.478     0.478 f  cnt_reg[1]/Q
                         net (fo=37, unplaced)        0.881     1.359    user_bram/Q[1]
                                                                       f  user_bram/wbs_dat_o_OBUF[17]_inst_i_1/I0
                         LUT5 (Prop_lut5_I0_O)        0.295     1.654 r  user_bram/wbs_dat_o_OBUF[17]_inst_i_1/O
                         net (fo=1, unplaced)         0.800     2.454    wbs_dat_o_OBUF[17]
                                                                       r  wbs_dat_o_OBUF[17]_inst/I
                         OBUF (Prop_obuf_I_O)         2.634     5.088 r  wbs_dat_o_OBUF[17]_inst/O
                         net (fo=0)                   0.000     5.088    wbs_dat_o[17]
                                                                       r  wbs_dat_o[17] (OUT)
  -------------------------------------------------------------------    -------------------

Slack:                   inf
  Source:                cnt_reg[1]/C
                           (rising edge-triggered cell FDCE)
  Destination:           wbs_dat_o[18]
                           (output port)
  Path Group:            (none)
  Path Type:             Max at Slow Process Corner
  Data Path Delay:       5.088ns  (logic 3.407ns (66.968%)  route 1.681ns (33.032%))
  Logic Levels:          3  (FDCE=1 LUT5=1 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         FDCE                         0.000     0.000 r  cnt_reg[1]/C
                         FDCE (Prop_fdce_C_Q)         0.478     0.478 f  cnt_reg[1]/Q
                         net (fo=37, unplaced)        0.881     1.359    user_bram/Q[1]
                                                                       f  user_bram/wbs_dat_o_OBUF[18]_inst_i_1/I0
                         LUT5 (Prop_lut5_I0_O)        0.295     1.654 r  user_bram/wbs_dat_o_OBUF[18]_inst_i_1/O
                         net (fo=1, unplaced)         0.800     2.454    wbs_dat_o_OBUF[18]
                                                                       r  wbs_dat_o_OBUF[18]_inst/I
                         OBUF (Prop_obuf_I_O)         2.634     5.088 r  wbs_dat_o_OBUF[18]_inst/O
                         net (fo=0)                   0.000     5.088    wbs_dat_o[18]
                                                                       r  wbs_dat_o[18] (OUT)
  -------------------------------------------------------------------    -------------------

S
```

四、發現：

只有在”wbs_cyc_i、wbs_we_i 兩者皆為 1”且” counter 為 10”，才會啟動 we（寫入 BRAM），否則寫入的值不會正確。