SOC Design Laboratory Lab6

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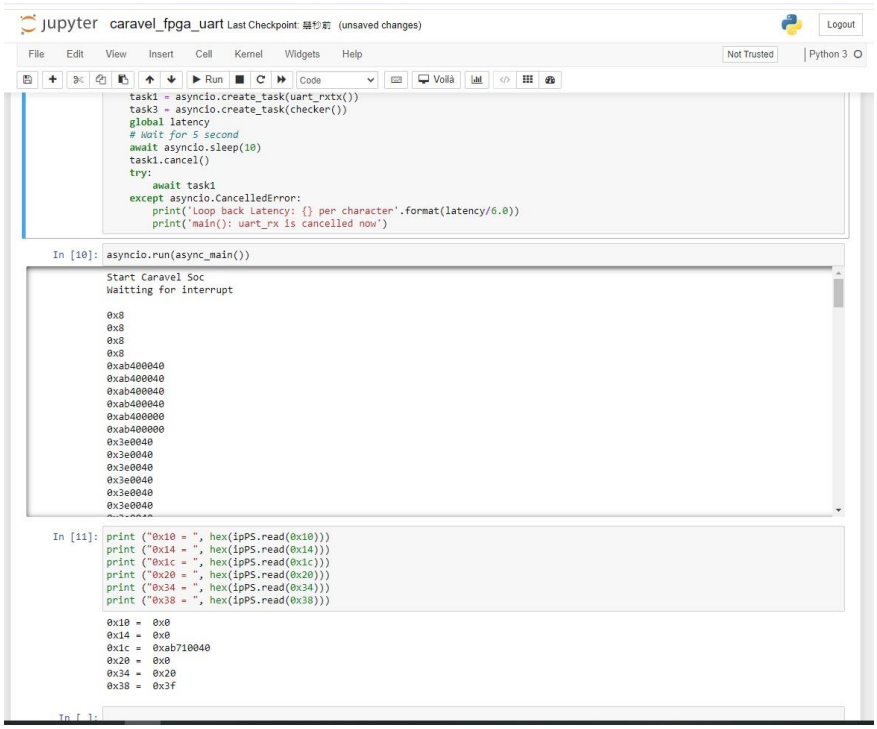
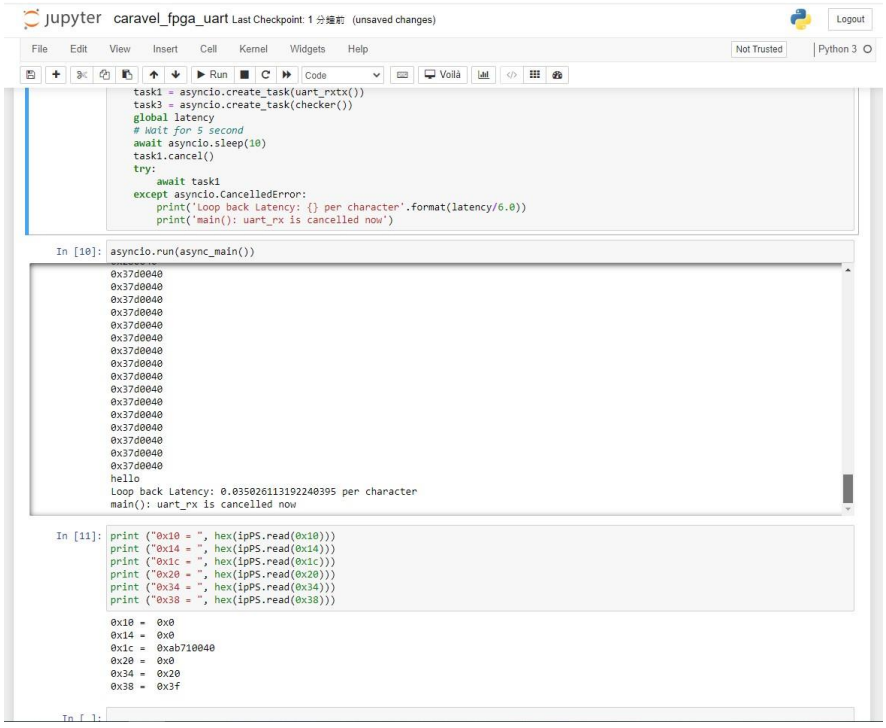
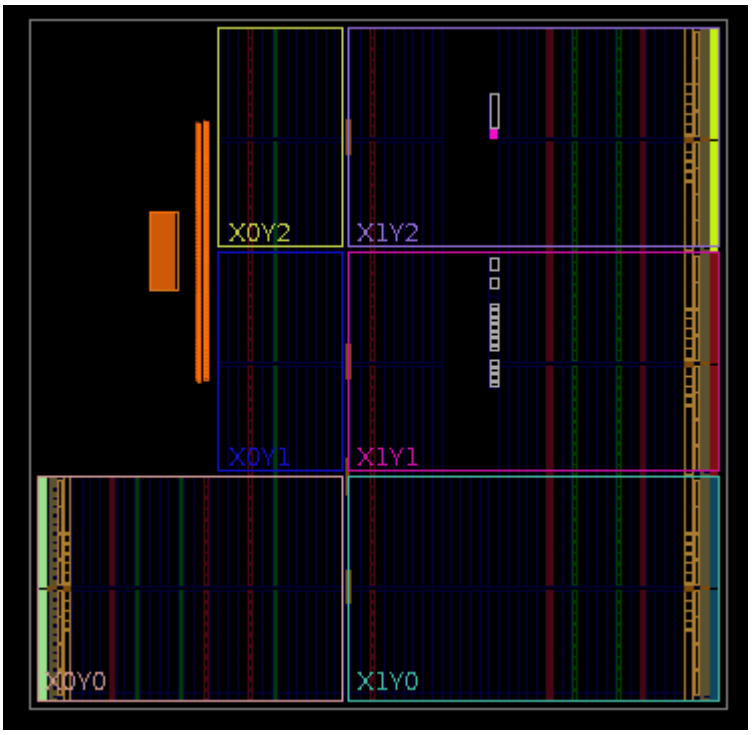
交大電物碩二

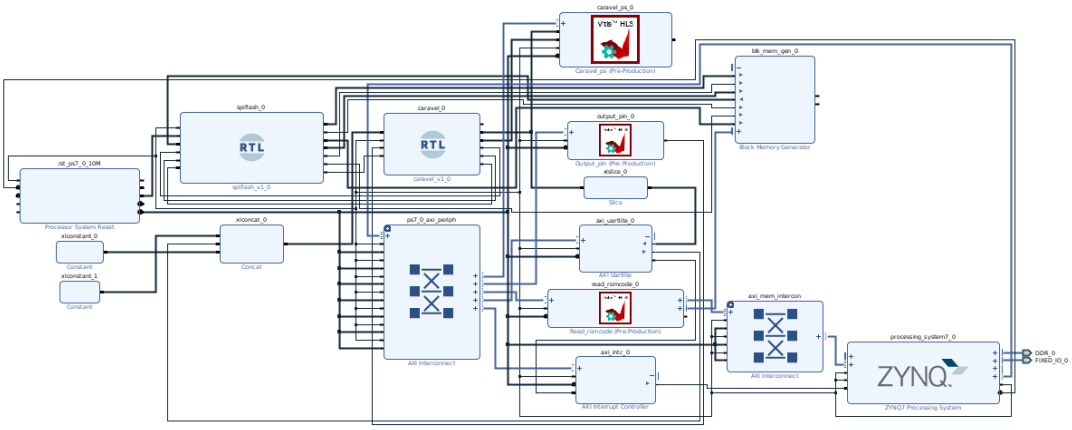
1.FPGA：





2. Block Design：





3. Report：Report 檔案我有放在”report”路徑內

(a)Synthesis Timing Report

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Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             11.848ns  (required time - arrival time)
  Source:                 design_1_i/processing_system7_0/inst/PS7_i/FCLKCLK[0]
                            (clock source 'clk_fpga_0'  {rise@0.000ns fall@12.500ns period=25.000ns})
  Destination:            design_1_i/caravel_ps_0/inst/control_s_axi_U/int_ps_mprj_out_reg[14]/D
                            (rising edge-triggered cell FDRE clocked by clk_fpga_0  {rise@0.000ns fall@12.500ns period=25.000ns})
  Path Group:             clk_fpga_0
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            12.500ns  (clk_fpga_0 rise@25.000ns - clk_fpga_0 fall@12.500ns)
  Data Path Delay:        1.824ns  (logic 0.225ns (12.333%)  route 1.599ns (87.667%))
  Logic Levels:           2  (BUFG=1 LUT6=1)
  Clock Path Skew:        1.505ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    1.505ns = ( 26.505 - 25.000 )
    Source Clock Delay      (SCD):    0.000ns = ( 12.500 - 12.500 )
    Clock Pessimism Removal (CPR):    0.000ns
  Clock Uncertainty:      0.377ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.750ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock clk_fpga_0 fall edge)
                                                   12.500    12.500 f
    PS7_X0Y0             PS7                          0.000    12.500 f  design_1_i/processing_system7_0/inst/PS7_i/FCLKCLK[0]
                         net (fo=1, unplaced)         0.800    13.300    design_1_i/processing_system7_0/inst/FCLK_CLK_unbuffered[0]
                                                                  f  design_1_i/processing_system7_0/inst/buffer_fclk_clk_0.FCLK_CLK_0_BUFG/I
                         BUFG (Prop_bufg_I_O)         0.101    13.401 f  design_1_i/processing_system7_0/inst/buffer_fclk_clk_0.FCLK_CLK_0_BUFG/O
                         net (fo=5692, unplaced)      0.800    14.200    design_1_i/caravel_0/inst/gpio_control_in_1[6]/clock
                                                                  f  design_1_i/caravel_0/inst/gpio_control_in_1[6]/mprj_o[14]_INST_0/I3
                         LUT6 (Prop_lut6_I3_O)        0.124    14.324 f  design_1_i/caravel_0/inst/gpio_control_in_1[6]/mprj_o[14]_INST_0/O
                         net (fo=2, unplaced)         0.000    14.324    design_1_i/caravel_ps_0/inst/control_s_axi_U/mprj_out[14]
                         FDRE                                       f  design_1_i/caravel_ps_0/inst/control_s_axi_U/int_ps_mprj_out_reg[14]/D
  -------------------------------------------------------------------    -------------------

                         (clock clk_fpga_0 rise edge)
                                                   25.000    25.000 r
    PS7_X0Y0             PS7                          0.000    25.000 r  design_1_i/processing_system7_0/inst/PS7_i/FCLKCLK[0]
                         net (fo=1, unplaced)         0.760    25.760    design_1_i/processing_system7_0/inst/FCLK_CLK_unbuffered[0]
                                                                  r  design_1_i/processing_system7_0/inst/buffer_fclk_clk_0.FCLK_CLK_0_BUFG/I
                         BUFG (Prop_bufg_I_O)         0.091    25.851 r  design_1_i/processing_system7_0/inst/buffer_fclk_clk_0.FCLK_CLK_0_BUFG/O
                         net (fo=5692, unplaced)      0.655    26.505    design_1_i/caravel_ps_0/inst/control_s_axi_U/ap_clk
                         FDRE                                       r  design_1_i/caravel_ps_0/inst/control_s_axi_U/int_ps_mprj_out_reg[14]/C
                         clock pessimism              0.000    26.505
                         clock uncertainty           -0.377    26.129
                         FDRE (Setup_fdre_C_D)        0.044    26.173    design_1_i/caravel_ps_0/inst/control_s_axi_U/int_ps_mprj_out_reg[14]
  -------------------------------------------------------------------
                         required time                         26.173
                         arrival time                         -14.324
  -------------------------------------------------------------------
                         slack                                 11.848
```

(b) Synthesis Utilization Report

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	5957	0	0	53200	11.20
LUT as Logic	5716	0	0	53200	10.74
LUT as Memory	241	0	0	17400	1.39
LUT as Distributed RAM	18	0			
LUT as Shift Register	223	0			
Slice Registers	6786	0	0	106400	6.38
Register as Flip Flop	6711	0	0	106400	6.31
Register as Latch	75	0	0	106400	0.07
F7 Muxes	171	0	0	26600	0.64
F8 Muxes	47	0	0	13300	0.35

(c)Implement Timing Report

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             8.557ns  (required time - arrival time)
  Source:                 design_1_i/processing_system7_0/inst/PS7_i/FCLKCLK[0]
                            (clock source 'clk_fpga_0'  {rise@0.000ns fall@12.500ns period=25.000ns})
  Destination:            design_1_i/caravel_ps_0/inst/control_s_axi_U/int_ps_mprj_out_reg[15]/D
                            (rising edge-triggered cell FDRE clocked by clk_fpga_0  {rise@0.000ns fall@12.500ns period=25.000ns})
  Path Group:             clk_fpga_0
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            12.500ns  (clk_fpga_0 rise@25.000ns - clk_fpga_0 fall@12.500ns)
  Data Path Delay:        6.046ns  (logic 0.342ns (5.656%)  route 5.704ns (94.344%))
  Logic Levels:           3  (BUFG=1 LUT1=1 LUT6=1)
  Clock Path Skew:        2.716ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.716ns = ( 27.716 - 25.000 )
    Source Clock Delay      (SCD):    0.000ns = ( 12.500 - 12.500 )
    Clock Pessimism Removal (CPR):    0.000ns
  Clock Uncertainty:      0.377ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.750ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock clk_fpga_0 fall edge)
                                                     12.500    12.500 f
    PS7_X0Y0             PS7                          0.000    12.500 f  design_1_i/processing_system7_0/inst/PS7_i/FCLKCLK[0]
                         net (fo=1, routed)           1.193    13.693    design_1_i/processing_system7_0/inst/FCLK_CLK_unbuffered[0]
    BUFGCTRL_X0Y20                                                   f  design_1_i/processing_system7_0/inst/buffer_fclk_clk_0.FCLK_CLK_0_BUFG/I
    BUFGCTRL_X0Y20       BUFG (Prop_bufg_I_O)         0.101    13.794 f  design_1_i/processing_system7_0/inst/buffer_fclk_clk_0.FCLK_CLK_0_BUFG/O
                         net (fo=5264, routed)        2.171    15.965    design_1_i/caravel_0/inst/gpio_control_in_1[7]/clock
    SLICE_X54Y98                                                     f  design_1_i/caravel_0/inst/gpio_control_in_1[7]/mprj_o[15]_INST_0/I3
    SLICE_X54Y98         LUT6 (Prop_lut6_I3_O)        0.124    16.089 f  design_1_i/caravel_0/inst/gpio_control_in_1[7]/mprj_o[15]_INST_0/O
                         net (fo=1, routed)           1.177    17.266    design_1_i/caravel_0/inst/gpio_control_in_1[7]/mprj_o[0]
    SLICE_X33Y98                                                     f  design_1_i/caravel_0/inst/gpio_control_in_1[7]/mprj_o[0]_hold_fix/I0
    SLICE_X33Y98         LUT1 (Prop_lut1_I0_O)        0.117    17.383 f  design_1_i/caravel_0/inst/gpio_control_in_1[7]/mprj_o[0]_hold_fix/O
                         net (fo=1, routed)           1.164    18.546    design_1_i/caravel_ps_0/inst/control_s_axi_U/mprj_o[0]_hold_fix_1_alias
    SLICE_X54Y98         FDRE                                        f  design_1_i/caravel_ps_0/inst/control_s_axi_U/int_ps_mprj_out_reg[15]/D
  -------------------------------------------------------------------    -------------------

                         (clock clk_fpga_0 rise edge)
                                                     25.000    25.000 r
    PS7_X0Y0             PS7                          0.000    25.000 r  design_1_i/processing_system7_0/inst/PS7_i/FCLKCLK[0]
                         net (fo=1, routed)           1.088    26.088    design_1_i/processing_system7_0/inst/FCLK_CLK_unbuffered[0]
    BUFGCTRL_X0Y20                                                   r  design_1_i/processing_system7_0/inst/buffer_fclk_clk_0.FCLK_CLK_0_BUFG/I
    BUFGCTRL_X0Y20       BUFG (Prop_bufg_I_O)         0.091    26.179 r  design_1_i/processing_system7_0/inst/buffer_fclk_clk_0.FCLK_CLK_0_BUFG/O
                         net (fo=5264, routed)        1.537    27.716    design_1_i/caravel_ps_0/inst/control_s_axi_U/ap_clk
    SLICE_X54Y98         FDRE                                        r  design_1_i/caravel_ps_0/inst/control_s_axi_U/int_ps_mprj_out_reg[15]/C
                         clock pessimism              0.000    27.716
                         clock uncertainty           -0.377    27.339
    SLICE_X54Y98         FDRE (Setup_fdre_C_D)       -0.236    27.103    design_1_i/caravel_ps_0/inst/control_s_axi_U/int_ps_mprj_out_reg[15]
  -------------------------------------------------------------------    -------------------
                         required time                         27.103
                         arrival time                         -18.546
  -------------------------------------------------------------------
                         slack                                 8.557
```

(d)Implement Utilization Report

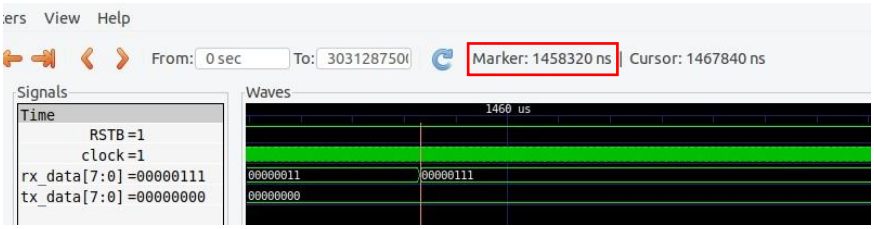
1. Slice Logic

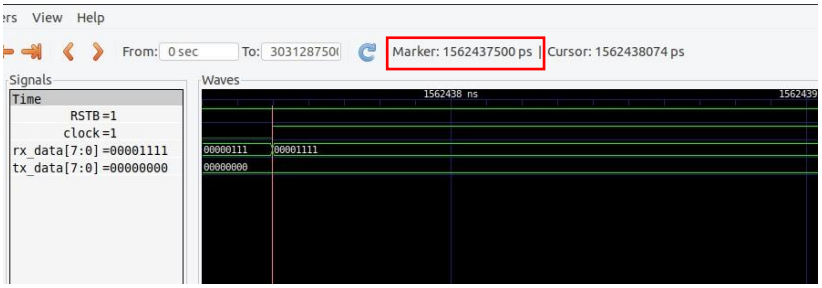
Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	5332	0	0	53200	10.02
LUT as Logic	5144	0	0	53200	9.67
LUT as Memory	188	0	0	17400	1.08
LUT as Distributed RAM	18	0			
LUT as Shift Register	170	0			
Slice Registers	6159	0	0	106400	5.79
Register as Flip Flop	6159	0	0	106400	5.79
Register as Latch	0	0	0	106400	0.00
F7 Muxes	170	0	0	26600	0.64
F8 Muxes	47	0	0	13300	0.35

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
283	Yes	-	Set
1031	Yes	-	Reset
130	Yes	Set	-
4715	Yes	Reset	-

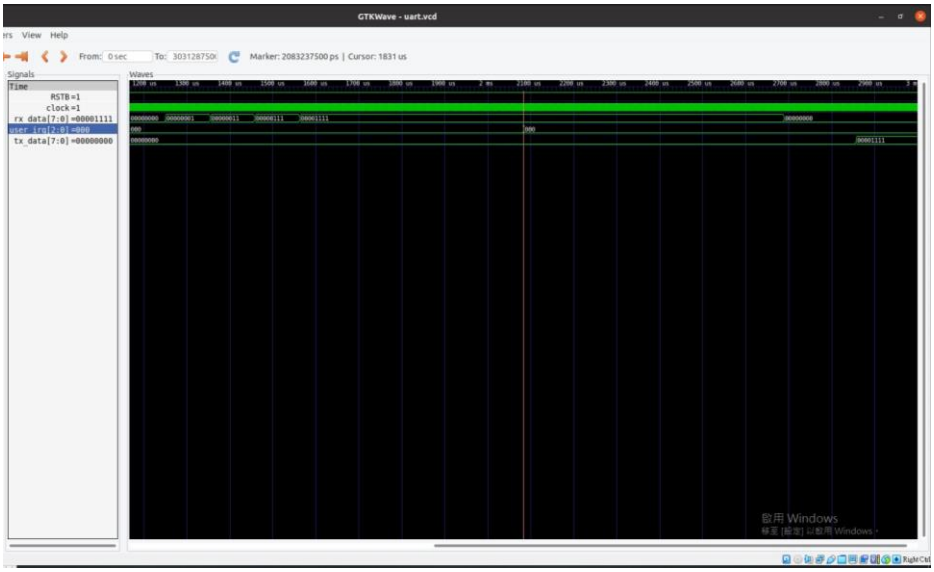
4. Latency for a character loop back using UART





T = 1562437500 - 1458320 = 1560979180 ps

Interrupt 波形圖：



5. What else do you observe

Testbench 不能把 UART 和 CPU 的 code serialize，否則如果 Interrupt 在這中間要進來會出問題。