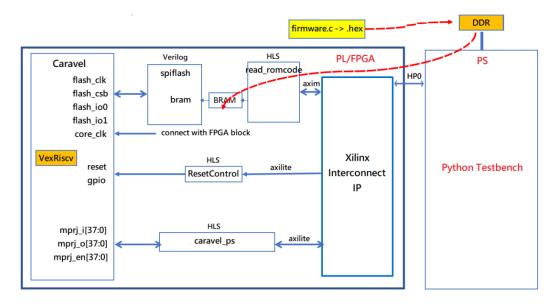
\report\311651055_林柏宇\Report\10MSOC Design

Laboratory Lab5

311651055_林柏宇 交大電物碩二

1. Block diagram:



2. 50M Utilization:

(1)BRAM Synthesis:

1. Slice Logic

+	+			+	++
Site Type	l Used	Fixed	Prohibited	l Available	Util% i
+	+	F		t <u></u>	++
Slice LUTs*	1 10	0	0	l 53200	I 0.02 I
LUT as Logic	1 8	l 0	0	l 53200	I 0.02 I
l LUT as Memory	1 2	0	0	l 17400	I 0.01 I
I LUT as Distributed RAM	1 0	l 0			l l
I LUT as Shift Register	1 2	l 0			I I
Slice Registers	1 12	0	0	l 106400	0.01 I
l Register as Flip Flop	1 12	l 0	0	l 106400	I 0.01 I
l Register as Latch	1 0	0	0	l 106400	I 0.00 I
F7 Muxes	1 0	l 0	0	l 26600	I 0.00 I
l F8 Muxes	1 0	0	0	l 13300	I 0.00 I
+	+			+	++

1.1 Summary of Registers by Type

Total Clock Enable Synchronous Asynchronou	_
	3 I
0	t - - t

2. Memory

+	+	+	+		+
Site Type			Prohibited		
Block RAM Tile RAMB36/FIFO* RAMB36E1 only RAMB18	i 2 I 2	i 0 I 0	0 0	140	i 1.43 i

3. DSP

4. IO and GT Specific

Site Type | Used | Fixed | Prohibited | Available | Util% | Bonded IOB
Bonded IPADs
Bonded IOPADs
PHY_CONTROL
PHASER_REF
OUT_FIFO
IN_FIFO
IDELAYCTRL
IBHEDS 125 | 2 | 130 | 0 0.00 0.00 0.00 0.00 0.00 0.00 Ö Ö 0 0 i 0 i 0 i 0 i 4 I 4 I ŏ Ŏ Ŏ Ŏ Ŏ 16 İ 0 | 0 | 0 | 0 | Ö 16 I 0.00 4 | 121 | 16 | 16 | 0.00 0.00 0.00 0.00 0 0 IBUFDS
PHASER_OUT/PHASER_OUT_PHY
PHASER_IN/PHASER_IN_PHY
IDELAYE2/IDELAYE2_FINEDELAY Õ οi 0.00 ILOGIC OLOGIC 125 i 0 1 0 1 0 1 0.00

5. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	0	0	0	32	0.00
BUF10	0	0	0	16	0.00
MMCME2_ADV	0	0	0	4	0.00
PLLE2_ADV	0	0	0	4	0.00
BUFMCE	0	0	0	8	0.00
BUFHCE	0	0	0	72	0.00
BUFR	0	0	0	16	0.00

6. Specific Feature

+	+	+	+	+	++
Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2 CAPTUREE2 DNA_PORT EFUSE_USR FRAME_ECCE2 I CAPE2 STARTUPE2 XADC	+ 0 0 0 0 0 0	+	0 0 0 0 0 0 0	+	

7. Primitives

+	H	+ -
Ref Name	Used	Functional Category
FDRE LUT2 SRL16E RAMB36E1 LUT4	12 6 2 2	Flop & Latch LUT

(2) Caravel Synthesis:

1. Slice Logic

L		т.	ь .			
i	Site Type	Used	Fixed	Prohibited	Available	Util%
	Slice LUTs* LUT as Logic LUT as Memory LUT as Distributed RAM LUT as Shift Register Slice Registers Register as Flip Flop Register as Latch F7 Muxes F8 Muxes	3842 3788 54 16 38 3945 3870 75 169 47	0 0 0 0 0 0 0 0 0	0 0 0 0 0	53200 53200 17400 106400 106400 106400 26600 13300	0.31
+		+	+	+	+	++

1.1 Summary of Registers by Type

+-----+ | Total | Clock Enable | Synchronous | Asynchronous |

Total	Clock Enable	Synchronous	Asynchronous
0 0 0 0 0 0 0 271 964 87 2623		Set Reset - - - Set Reset	- Set Reset - Set Reset -
+	+		++

2. Memory

+	+	+	+	+	++
Site Type		Fixed	Prohibited	Available	l Util% l
Block RAM Tile RAMB36/FIFO* RAMB18 RAMB18E1 only	i 3 I 0 I 6	i 0 I 0 I 0	į o	i 140 I 140	i 2.14 i

3. DSP

 i Used	. i Fixed	Prohibited	l Available	Util% i
i 0	ıi o	i o	i 220	i 0.00 i

4. IO and GT Specific

+	+			+	+
i Site Type	Used	Fixed	Prohibited	Available	Util%
+	+			+	++
Bonded IOB	I 0	0 1	0	l 125	0.00
l Bonded IPADs	I 0	0 1	0	1 2	0.00
Bonded IOPADs	1 0	0 1	0	l 130	0.00
PHY CONTROL	1 0	0 1	0	1 4	0.00
I PHASER REF	I 0	0 1	0	1 4	0.00
I OUT_FIFO	I 0	0 1	0	l 16	0.00
I IN_FIFO	I 0	0 1	0	l 16	0.00
I IDĒLAYCTRL	I 0	0 1	0	1 4	0.00
I IBUFDS	I 0	0 1	0	l 121	0.00
I PHASER OUT/PHASER OUT PHY	I 0	0 1	0	l 16	0.00
I PHASER IN/PHASER IN PHY	I 0	0 1	0	l 16	0.00
IDELAYE2/IDELAYE2	I 0	0 1	0	I 200	0.00
ILOGIC	I 0	0 1	0	l 125	0.00
OLOGIC	I 0	0 1	0	l 125	0.00
4	+			-	

5. Clocking

4	+	+	4	-	
Site Type	Used	Fixed	Prohibited		Util%
+	+	+	+	+	++
BUFGCTRL	1 0	1 0	I 0	l 32	I 0.00 I
BUFIO	1 0	1 0	1 0	l 16	I 0.00 I
I MMCME2 ADV	1 0	1 0	1 0	1 4	I 0.00 I
I PLLE2 ADV	1 0	1 0	1 0	1 4	I 0.00 I
BUFMRŒE	1 0	1 0	1 0	l 8	I 0.00 I
BUFHCE	1 0	1 0	1 0	l 72	I 0.00 I
I BUFR	1 0	1 0	1 0	l 16	0.00 I
1	т.	ь.	ь.	L .	ь д

6. Specific Feature

+	+	+	+	+	++
Site Type	j Used ∸	Fixed	Prohibited	Available	Util%
BSCANE2 CAPTUREE2	1 0	0	0	4	0.00
I DNA_PORT	0	0	į 0		0.00
EFUSE_USR FRAME_ECCE2	I 0	I 0 I 0	I 0 I 0	l 1 l 1	0.00 0.00
ICAPE2 STARTUPE2	1 0	1 0	0	1 2	0.00
XADC	iŏ	i ő	i ő	i 1	0.00
+	.+	+	+	+	++

7. Primitives

+		
Ref Name	Used	Functional Category
FDRE LUT6	2623 1753	Flop & Latch
I FDCE	889	LUT Flop & Latch
LUT5 LUT4	876 814	LUT I LUT I
LUT3 FDPE	291 271	LUT Flop & Latch
I LUT2	262 I	LUT I
MUXF7	169	MuxFx
CARRY4 FDSE	134 87	CarryLogic Flop & Latch
LDCE MUXF8	75 47	Flop & Latch MuxFx
SRL16E RAMD32	38 i 24 i	Distributed Memory Distributed Memory
RAMS32	8	Distributed Memory
RAMB18E1	6	Block Memory I

(3) Caravel_PS Synthesis:

1. Slice Logic

+	+		·		++
Site Type	l Used	Fixed	Prohibited	Available	Util% i
Slice LUTs* LUT as Logic LUT as Memory Slice Registers Register as Flip Flop Register as Latch F7 Muxes	119 119 0 158 158 0		Ŏ 0	53200 53200 17400 106400 106400 106400 26600	0.22 0.22 0.00 0.15 0.15 0.00
F8 Muxes	İŌ	i Õi	Ŏ	13300	0.00

1.1 Summary of Registers by Type

++ Total	Clock Enable	Synchronous	
0	- - - Yes Yes Yes Yes	Set Reset - - Set Reset	Set Reset - - Set Reset

2. Memory

l Site Type	l Used	Fixed	Prohibited	++ Available Util% +
Block RAM Tile RAMB36/FIFO* RAMB18	i 0	j 0	i 0	140 0.00 140 0.00

3. DSP

Site Type	i Used i	Fixed İ	Prohibited i	Available	Util% i
DSPs	i oi	0 i	0 i	220	i 0.00 i

4. IO and GT Specific

Site Type	+ Used	Fixed	Prohibited	+ Available	+ Util%
Bonded IOB Bonded IPADs Bonded IPADs Bonded IPADs Bonded IPADs PHASER REF OUT FIFO IN FIFO IDELAYCTRL IBUPDS PHASER OUT /PHASER OUT PHY PHASER IN /PHASER IN _PHY IDELAYEZ/IDELAYEZ_FINEDELAY ILOGIC ILOGIC			0 0 0 0 0 0 0 0 0	1 125 1 130 1 4 1 16 1 16 1 121 1 16 1 16 1 16 1 16	0.00 0.00 0.00 0.00 0.00 0.00 0.00 0.00 0.00 0.00
OLOGIC	0	0 1	0	125	0.00

5. Clocking

+	+		+	·	+	++
Site Type	i Use	ed	Fixed	Prohibited	Available	Util% i
+	+		+	+	+	++
BUFGCTRL	1	0	l 0	I 0	I 32	I 0.00 I
BUFIO	1	0	l 0	I 0	I 16	I 0.00 I
I MMCME2_ADV	1	0	0	I 0	1 4	I 0.00 I
PLLE2_ADV	1	0	l 0	I 0	1 4	I 0.00 I
BUFMRCE		0	l 0	I 0	l 8	I 0.00 I
BUFHCE	1	0	l 0	I 0	l 72	I 0.00 I
I BUFR	1	0	l 0	I 0	l 16	l 0.00 l
+	+		+	+	+	++

6. Specific Feature

+		+-	4		+	+	++
į	Site Type	į	Used i	Fixed	Prohibited	Available	Util%
Ţ	BSCANE2	-	0	0	0	4	0.00
	CAPTUREE2 DNA PORT		U I	U 0	I U	I I I 1	0.00 0.00
Ţ	EFUSE_USR_	ļ	0	0	ļ 0	! !	0.00
i	FRAME_ECCE2 ICAPE2	ŀ	U I N I	U	I U	l l l 2	0.00 0.00
į	STARTUPE2	į	ŏį	Ŏ	i ŏ	i î	i 0.00 i
!	XADC	!	0 [0	l 0	1	0.00

7. Primitives

+		b
Ref Name	Used	Functional Category
+	+	h
I FDRE	l 158	Flop & Latch
I LUT3	l 79	LUT I
I LUT6	l 46	LUT
I LUT2	l 8	LUT
I LUT4	1 4	LUT
I LUT5	1	LUT
I LUT1	1	LUT
+	+	

(4) Output Pin Synthesis:

1. Slice Logic

4	+			+	++
Site Type	Used	Fixed	Prohibited	Available	Util% i
Slice LUTs* LUT as Logic LUT as Memory Slice Registers Register as Flip Flop Register as Latch F7 Muxes F8 Muxes F8 Muxes	10 10 0 12 12 0 0	i ŏ	0 0 0	53200 53200 17400 106400 106400 106400 26600 13300	0.02 0.02 0.00 0.01 0.01 0.00 0.00
L	4		L .	L .	4 4

1.1 Summary of Registers by Type

Total	+	Synchronous	++ Asynchronous
0 0 0 0 0 0 0 0 0 1 12		Set Reset - - - Set Reset	Set Reset - - Set Reset -

2. Memory

Site Type	l Used	Fixed	Prohibited	I Available	Util% i
Block RAM Tile	i 0	i 0	0	140	0.00
RAMB36/FIFO*	I 0	I 0	0	140	0.00
RAMB18	I 0	I 0	0	280	0.00

3. DSP

Site Type	l Used	Fixed i	Prohibited	Available	Util% i
DSPs	i 0 i	0 i	0	i 220	i 0.00 i

4. IO and GT Specific

	4			+	
Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB Bonded IPADs Bonded IPADs Bonded IOPADs PHY_CONTROL PHASER REF OUT_FIFO IN_FIFO IDELAYCTRL IBUPDS PHASER_OUT_PHY PHASER_OUT_PHY IDELAYE2/IDELAYE2_FINEDELAY ILLGIC	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	125 2 130 4 4 16 16 121 16 16 16 200 125	0.00 0.00 0.00 0.00 0.00 0.00 0.00 0.00 0.00 0.00
OLOGIC I	0 1	0 1	0	l 125	0.00

5. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL BUF10 MMCME2_ADV PLLE2_ADV BUFMRCE BUFMRCE BUFHCE	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	32 16 4 4 8 72	0.00 0.00 0.00 0.00 0.00 0.00

6. Specific Feature

+		+	+				++
i	Site Type	i U	sed İ	Fixed	Prohibited	Available	Util% i
+		+	+		+		++
	BSCANE2		0.1	0	0	4	I 0.00 I
	CAPTUREE2		0 1	0	0	1	I 0.00 I
	DNA_PORT		0 1	0	0	1	I 0.00 I
	EFUSE_USR		0 1	0	0	1	I 0.00 I
	FRAME ECCE2		0 1	0	0	1	I 0.00 I
	ICAPE2		0 1	0	0	1 2	I 0.00 I
	STARTUPE2		0 1	0	0	1	I 0.00 I
	XADC		0 1	0	0	1	I 0.00 I
- 1							

7. Primitives

+		+
Ref Name	Used	Functional Category
FDRE LUT5 LUT4 LUT6 LUT2 LUT1	12 4 4 1 1	Flop & Latch LUT LUT LUT LUT LUT

(5) Processing System Synthesis:

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	1 24	l 0	i 0	53200	0.05
LUT as Logic	1 24	l 0	I 0	I 53200	0.05
LUT as Memory	1 0	I 0	I 0	I 17400	0.00
Slice Registers	1 0	I 0	I 0	I 106400	0.00
Register as Flip Flop	1 0	0	I 0	I 106400	0.00
Register as Latch	1 0	0	I 0	I 106400	0.00
F7 Muxes	1 0	0	I 0	l 26600	0.00
F8 Muxes	1 0	0	I 0	l 13300	0.00

1.1 Summary of Registers by Type

0	+ Total	 Clock Enable	Synchronous	Asynchronous
	0 0 0 0 0 0 0 0 0 0	l Yes Yes Yes	Reset - - - Set	Reset

2. Memory

				++ Available Util%
Block RAM Tile	i 0	i 0 i	0	140 0.00
RAMB36/FIFO*	I 0	I 0 i	0	
RAMB18	I 0	I 0 i	0	

3. DSP

Site Type	l Used	Fixed	+ Prohibited +	l Available	Util%
i DSPs	i 0	i 0	0	i 220	i 0.00 i

4. IO and GT Specific

.....

+	+		+	+	++
Site Type	Used	Fixed	Prohibited	Available	Util% i
Bonded IOB Bonded IPADs Bonded IPADs Bonded IOPADs PHY_CONTROL PHASER REF OUT_FIFO IN_FIFO IDELAYCTRL	0 0 0 0 0 0 0 0 0 0		+	125 2 130 4 1 4 1 16 1 16	0.00 0.00
IBUPDS PHASER_OUT/PHASER_OUT_PHY PHASER_IN/PHASER_IN_PHY IDELAYE2/IDELAYE2_FINEDELAY ILOGIC OLOGIC		0 0 0 0 0	0 0 0 0 0	121 16 16 200 125	0.00 0.00 0.00 0.00 0.00

5. Clocking

Site Type	+ Used		Prohibited		+ Util%
BUFGCTRL BUFIO MMCME2_ADV PLLE2_ADV BUFMRCE BUFHCE BUFHCE	1 0 0 0 0 0	0 1 0 1 0	Ŏ	32	3.13 0.00 0.00 0.00 0.00 0.00

6. Specific Feature

Site Type	+ Used +	Fixed	Prohibited	Available	 Util%
I BSCANE2 I CAPTUREE2 I DNA PORT I EFUSE_USR I FRAME ECCE2 I ICAPE2 I STARTUPE2 I XADC	0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	4 1 1 1 1 2 1 1	0.00 0.00 0.00 0.00 0.00 0.00 0.00

7. Primitives

+		
Ref Name	Used	Functional Category
BIBUF LUT1 PS7 BUFG	130 24 1 1 1 1	IO LUT Specialized Resource Clock

(6)Read Romcode Synthesis:

1. Slice Logic

4		4	4	4	4	44
	Site Type	Used	Fixed	Prohibited	Available	Util%
	Logic Memory	739 664 75	0 0 0	0 0 0	53200 53200 17400	
LUT a	as Distributed RAM as Shift Register	i 75	I 0			
	gisters er as Flip Flop er as Latch	1100 1100	I U I 0 I n	I U I 0	I 106400 I 106400 I 106400	1.03 1.03 0.00
F7 Muxes F8 Muxes	or as batter	i ŏ	i ŏ	j ŏ	26600 1 13300	0.00

1.1 Summary of Registers by Type

L	+		++
Total	l Clock Enable i	Synchronous	Asynchronous
0 0 0 0 0 0 0 0 0 0		Set Reset - - - Set Reset	Set Set Reset - Set Reset -
H	+		++

2. Memory

+	+		+		++
l Site Type	l Used	Fixed	Prohibited	Available	Util% i
I DIOCK KIIM IIIC	1	0	0	140	0.71 i
RAMB36/FIFO* RAMB36E1 only	l 1 I 1		l 0 I	l 140 I	0.71
RAMB18	l 0	l 0 	l 0 +	l 280 +	0.00 ++

3. DSP

Site Type	i Used i	Fixed I	Prohibited	Available	Util% i
DSPs	i oi	0 i	0 i	i 220	i 0.00 i

4. IO and GT Specific

Site Type	 Used	Fixed	Prohibited	Available	++ Util%
		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	125 2 130 4 4 16 16 121 16 16 200	++ 0.00 0.00
OLOGIC	i ői	ő	ŏ	125	0.00

5. Clocking

Site Type	Used	Fixed	Prohibited		 Util%
BUFGCTRL BUF10 MMCME2_ADV PLLE2_ADV BUFMRCE BUFMCE BUFHCE BUFR	0 0 0 0 0 0	0 0 0	0 0 0 0 0 0 0	16 4 1 4 1 8 1 72	0.00 0.00 0.00 0.00 0.00 0.00

6. Specific Feature

+	+	+	+	+	++
Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2	0	0	0	4	0.00
CAPTUREE2 DNA_PORT	1 0	I 0	I 0	I I I 1	0.00 0.00
EFUSE_USR FRAME ECCE2	I 0	l 0 I 0	l 0 I 0	l 1 l 1	0.00 0.00
I ICAPEZ I Startupez	1 0	I 0	I 0	1 2	0.00
XADC	į ŏ	i ŏ	į ŏ	į į	0.00

7. Primitives

+		
Ref Name	Used	Functional Category
FDRE	1 1097 1 261 1 212 1 158 1 132 1 75 1 68 1 63 1 22 1 3 1 1	Flop & Latch LUT LUT LUT LUT Distributed Memory LUT CarryLogic LUT Flop & Latch Block Memory
+	+	++

(7) Reset Control Synthesis:

1. Slice Logic

ļ	+	+	+		+	++
	Site Type	l Used	Fixed	Prohibited	Available	Util% i
	Slice LUTs* LUT as Logic LUT as Memory LUT as Distributed RAM LUT as Shift Register Slice Registers Register as Flip Flop Feg Muxes	19 18 1 18 1 0 1 1 1 40 1 40 1 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0	53200 53200 17400 17400 106400 106400 106400 26600	<0.01 0.04
	F8 Muxes	1 0 1		U	l 13300	1 0.00 1

1.1 Summary of Registers by Type

L	+	-	+
Total	Clock Enable	Synchronous	Asynchronous
0		Set Reset - - Set Reset	- Set Reset - - Set Reset

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	i 0 i	0	140	0.00 i
RAMB36/FIFO*	0	0 i	0	140	0.00 i
RAMB18	0	0 l	0	280	0.00 l

3. DSP

Site Type	i Used	Fixed	Prohibited	I Available	Util% i
DSPs	i 0	i oi	0	i 220	i 0.00 i

4. IO and GT Specific

+	+	+		+	++
Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB Bonded IPADs Bonded IPADs Bonded IPADs Bonded IOPADs PHY CONTROL PHASER REF OUT_FIFO IN FIFO IDELAYCTRL IBUFDS PHASER OUT/PHASER OUT_PHY PHASER IN/PHASER IN PHY IDELAYEZ/IDELAYEZ_FINEDELAY ILOGIC	+		0 0 0 0 0 0 0 0 0	125 1 22 1 130 1 4 1 4 1 16 1 16 1 121 1 16 1 16 1 16	0.00 0 0 0 0 0 0 0 0
OLOGIC	1 U +	U	·	l 125	0.00 ++

5. Clocking

+	+	-	+	-	
Site Type	Used	Fixed	Prohibited	I Available	
BUFGCTRL	0	0	l 0	j 32	i 0.00 i
BUFIO	0		0	16	0.00 0.00
MMCME2_ADV PLLE2 ADV	I 0 I 0		i ü	1 4 1 4	0.00 0.00
I BUFMRĒE	i ŏ		i ŏ	i 8	0.00
BUFHCE	1 0	l 0	1 0	1 72	0.00
BUFR		. 0	ı v	l 16	0.00

6. Specific Feature

Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2 CAPTUREE2	0	I 0	0	4 1	0.00
DNA PORT	0		0	1	0.00
EFUSE_USR FRAME_ECCE2	0	I 0	0	1 1	0.00
ICAPE2 STARTUPE2	1 0	l 0 I 0	0 0	l 2 I 1	0.00 0.00
XADC	l 0	l 0 +	0 	l 1	0.00

7. Primitives

Ref Name	Used	Functional Category
FDRE	36 9 6 5 4 3 1	Flop & Latch LUT LUT LUT Flop & Latch LUT Distributed Memory LUT LUT
+		

(8) Spiflash Synthesis:

1. Slice Logic

L	4	L	L .	L	
Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs* LUT as Logic LUT as Memory Slice Registers Register as Flip Flop Register as Latch F7 Muxes F8 Muxes	44 44 0 63 63 0 0	i ŏ	0 0 0 0 0 0 0 0	53200 53200 17400 106400 106400 106400 26600 13300	0.08 0.08 0.00 0.06 0.06 0.00 0.00
	T	r		r	г

1.1 Summary of Registers by Type

4		-		L4	+
į	Total	Clock Enable	Synchronous	Asynchronous	i
*	0 0 0 0 0 0 0 0 0 0	- - - Yes Yes Yes Yes Yes	Set Reset - - Set Reset	Set Reset - - - Set Reset -	
+				+	٠

2. Memory

İ	Site Type	İ	Used	İ	Fixed	Prohibited	İ	Available İ	Util%	İ
	Block RAM Tile			•		0	:		0.00	٠.
	RAMB36/FIFO*		0		0	0		140 l	0.00	l
	RAMB18	1	0		0	0		280 I	0.00	l

3. DSP

Site Type	i Used i	Fixed i	Prohibited i	Available İ	Util% İ
DSPs	i oi	0 i	0 i	i 220 i	0.00 i

4. IO and GT Specific

Site Type	+ Used	Fixed	Prohibited	Available	Util%
Bonded IOB	1 0	0	0	125	0.00
Bonded IPADs	1 0	0	0	2	0.00
Bonded IOPADs	j 0	0	0	130	0.00
PHY_CONTROL	i ŏ	I 0 1	0 1	4 1	0.00
PHASER_REF	1 0	. U	Ŭ	4 1	0.00
OUT_FIFO IN FIFO	1 0	I U I	U	16 16	0.00 l 0.00 l
I IDELAYCTRL	1 0	I 0 1	U 1	10 1	0.00 1
I IBIIFDS	i ň	i	i	121	0.00
PHASER OUT/PHASER OUT PHY	i ŏ	i ŏi	ĭŏi	16 1	0.00 i
I PHASER_IN/PHASER_IN_PHY	i ŏ	i ŏi	Ď	i 16 i	0.00 i
IDELAYE2/IDELAYE2_FINEDELAY	i 0	0	0 1	200 l	0.00
ILOGIC	1 0	0 1	0 1	l 125 I	0.00
I OLOGIC	1 0	0 1	0 1	l 125 l	0.00 l
+	+	+	h	++	+

5. Clocking

Site Type	++ Used	Fixed I	Prohibited	++ Available Util%
BUFGCTRL BUFIO MMCME2_ADV PLLE2_ADV BUFMRCE BUFMCE BUFMCE BUFFCE	0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	32 0.00

6. Specific Feature

o. Specific reacure

Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2 CAPTUREE2 DNA_PORT EFUSE_USR FRAME_ECCE2 ICAPE2 STARTUPE2 XADC		0 0 0 0 0	0 0 0 0 0 0	4 1 1 1 1 2 1	0.00 0.00 0.00 0.00 0.00 0.00 0.00

7. Primitives

Ref Name Used Functional Category	+	+	·
FDCE	Ref Name	Used	Functional Category
+	FDCE LUT3 LUT6 CARRY4 LUT4 LUT5 LUT1	31 1 26 1 21 1 10 1 5 1 4	Flop & Latch LUT LUT

(9) Wrapper Synthesis:

1. Slice Logic

Slice LUTs	Site Type	Used	Fixed	Prohibited	H Available	++ Util%
1 TO MUXES 1 01 01 15500 1 0.00	LUT as Logic LUT as Memory Slice Registers Register as Flip Flop Register as Latch	0 0 0 0 0 0 0		0 0 0 0 0 0 0 0	53200 53200 17400 106400 106400 106400	0.00 0.00 0.00 0.00

1.1 Summary of Registers by Type

0	+	++ Clock Enable	Synchronous I	Asynchronous
0	+	l Yes Yes Yes	Reset - - - Set	Reset - - Set

2. Slice Logic Distribution

Site Type	+ Used	+ Fixed	+ Prohibited	H Available	++ Util%
Slice SLICEL	i 0	i 0	i 0	13300	0.00
SLICEM LUT as Logic	I 0	l 0	l I 0	l 53200	 0.00
LUT as Memory LUT as Distributed RAM	i Ŏ	i Ö	j Ö	17400	0.00
LUT as Shift Register Slice Registers	i ŏ	i ŏ	 	i 106400	i 0.00 i
Register driven from within the Slice Register driven from outside the Slice	i ŏ	i i	i i	100,100 	
Unique Control Sets	i ŏ +	; +	0 +	13300	0.00 i

3. Memory

. - - - - - - -

+	+	+	-	+	-
Site Type	l Used	Fixed	Prohibited	I Available	Util%
Block RAM Tile RAMB36/FIFO* RAMB18	i 0 I 0	i 0 I 0	0 1 0	i 140 I 140	0.00
+					

4. DSP

.

Site Type	l Used	Fixed İ	Prohibited	I Available	Util% i
i DSPs i	i 0 i	0 i	0	i 220	i 0.00 i
+	+	+		+	+

5. IO and GT Specific

.....

Site Type	Used	Fixed	Prohibited	Available	Util% i
Bonded IOB	l 0	0	0	125	0.00
Bonded IPADs	I 0	0	0	1 2	I 0.00 I
Bonded IOPADs	I 0	0	0	l 130	I 0.00 I
PHY_CONTROL	I 0	0	0 1	1 4	I 0.00 I
PHASER_REF	I 0	0	0	1 4	I 0.00 I
OUT_FIFO	1 0	0	I 0 I	l 16	I 0.00 I
IN_FIFO	I 0	0	0	l 16	I 0.00 I
IDĒLAYCTRL	I 0	0	0	1 4	I 0.00 I
IBUFDS	1 0	0	0	l 121	I 0.00 I
PHASER_OUT/PHASER_OUT_PHY	I 0	0	0	l 16	l 0.00 l
PHASER_IN/PHASER_IN_PHY	1 0	0	0	16	0.00
IDELAYE2/IDELAYE2_FINEDELAY	1 0	0	0	200	0.00 [
ILOGIC	1 0	0	0	125	0.00
OLOGIC	I 0	0	0	l 125	l 0.00 l

6. Clocking

+	+	+	·	+	++
l Site Type	l Used	Fixed	Prohibited	Available	Util%
+	+	+		+	++
I BUFGCTRL	1 0	I 0	0	I 32	I 0.00 I
l BUFIO	1 0	I 0	l 0	l 16	I 0.00 I
I MMCME2 ADV	1 0	I 0	l 0	l 4	I 0.00 I
PLLE2_ADV	1 0	I 0	l 0	1 4	I 0.00 I
I BUFMRĒE	1 0	I 0	1 0	l 8	I 0.00 I
I BUFHCE	i 0	1 0	i Ó	l 72	0.00
I BUFR	1 0	I 0	l 0	l 16	I 0.00 I
+	+	+		+	++

7. Specific Feature

Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2	1 0	0	0	4	0.00
CAPTUREE2	1 0	l 0 1	0	1	l 0.00 l
DNA_PORT	1 0	l 0 1	0	1	I 0.00 I
EFUSE USR	1 0	l 0 1	0	1	I 0.00 I
FRAME_ECCE2	1 0	l 0 1	0	1	0.00 l
ICAPE2	1 0	l 0 1	0	2	0.00 I
STARTUPE2	1 0	l 0 l	0	1	0.00 I
XADC	1 0	0 1	0	1	0.00

(10) Wrapper Place Synthesis:

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util% I
I Slice LUTs LUT as Logic LUT as Memory LUT as Distributed RAM LUT as Shift Register Slice Registers	5327 5149 178 18 160 6051	0 0 0 0 0	0 0 0	53200 53200 17400	10.01 9.68 1.02 5.69
Register as Flip Flop Register as Latch F7 Muxes F8 Muxes	6051 0 169 47	0 I 0 I 0 I	0 0 0 0	106400 106400 26600 13300	5.69 I 0.00 I 0.64 I 0.35 I

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 282 1 943 1 111 1 4715		Set Reset - - Set Reset	Set Reset - - Set Reset

2. Slice Logic Distribution

†	+			·	++
Site Type	Used	Fixed	Prohibited	Available	I Util% I
I Slice	2303	0	0	13300	17.32
I SLICEL	1625	0 1			
I SLICEM	678	0		52200	
LUT as Logic	5149	0	0	53200	9.68
I using O5 output only I using O6 output only	1 4205				
I using 05 and 06	944				i i
LUT as Memory	178	0 1	0	17400	i 1.02 i
I LUT as Distributed RAM	18	0 1		l	1 1
using 05 output only	1 0				!!
using 06 output only	2				!!
using 05 and 06 LUT as Shift Register	l 16 l 160	0			
using 05 output only	I 100	U			
using 06 output only	81				i i
l using 05 and 06	38				i i
I Slice Registers	I 6051 I	0 1	0	106400	5.69 1
Register driven from within the Slice	2815				
Register driven from outside the Slice	1 3236				!!
LUT in front of the register is unused LUT in front of the register is used	I 1978 I I 1258 I				
I Unique Control Sets	1 312		0	13300	2.35
+	+				++

3. Memory

+		+			++
Site Type			Prohibited	Available	Util%
Block RAM Tile RAMB36/FIFO* RAMB36E1 only RAMB18 RAMB18E1 only	6	Ŏ	0 0	i 140	4.29 2.14 2.14 2.14
1	_	L	L J	L .	L L

4. DSP

Site Type	İ	Used	i	Fixed	İ	Prohibited	İ	Available	i	Util% İ
DSPs	İ	0	İ	0	İ	0	İ	220	İ	0.00 i

5. IO and GT Specific

Site Type	Used	Fixed	+ Prohibited	Harailable	++ Util%
Bonded IOB Bonded IPADs Bonded IPADs Bonded IOPADs PHY CONTROL PHASER_REF OUT_FIFO IN FIFO IDELAYCTRL IBUFDS PHASER_OUT/PHASER_OUT_PHY PHASER_IN_PHY IDELAYER_IN_PHY	0	0 130 0 0 0 0 0 0 0 0		125 2 130 4 16 16 121 121 16 200 125	
OLOGIC	. 0	. 0	I 0	l 125	I 0.00 I

6. Clocking

+		+		L	-4		L	4
į	Site Type	įυ	sed	Fixed	. į	Prohibited	Available	Util%
Ţ	BUFGCTRL	Ţ	7	0	Ţ	0	32	21.88
-	BUFIO		U	l U		U	l 16	I 0.00 I
-	MMCME2_ADV		0	10		0	1 4	I 0.00 I
	PLLE2_ADV	1	0	1 0		0	1 4	I 0.00 I
- 1	BUFMRCE		0	1 0		0	l 8	I 0.00 I
-	BUFHCE		0	1 0		0	l 72	I 0.00 I
-	BUFR	1	0	I 0		0	l 16	I 0.00 I

7. Specific Feature

Site Type Used Fixed Prohibited	Available Util%
BSCANE2	4 0.00 1 0.00 1 0.00 1 0.00 1 0.00 2 0.00
I XADC I OI OI	î i ő.őő i

(11) Xbar Synthesis:

1. Slice Logic

Site Type	+ Used	Fixed	Prohibited	Available	++ Util%
I Slice LUTs* I LUT as Logic LUT as Memory Slice Registers Register as Flip Flop Register as Latch F7 Muxes F8 Muxes	140 140 0 131 131 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	106400	0.26 0.26 0.00 0.12 0.12 0.00 0.00
+	+	+			++

1.1 Summary of Registers by Type

Total	Clock Enable i	Synchronous	Asynchronous
			+
0		-	-
0	_	-	l Set
0	_	-	l Reset
0	_	Set	-
0	_	Reset	-
0	Yes I	-	-
0	Yes	-	l Set
0	Yes	_	l Reset
0	Yes	Set	-
131	Yes	Reset	-

2. Memory

Site Type	l Used	Fixed	Prohibited	l Available	Util% i
Block RAM Tile	i 0	i 0	0	140	0.00
RAMB36/FIFO*	I 0	i 0	0	140	0.00
RAMB18	I 0	I 0	0	280	0.00

3. DSP

Site Type	Used	Fixed	Prohibited	I Available İ	Util% İ
DSPs +	0	i 0	0	i 220 i	0.00 i

4. IO and GT Specific

+	+ Used	+	 Prohibited	+	++ Util%
Site Type	ı usea	ı rixed	rionibilea -	i avaliadie	r
Bonded IOB	i 0	0	0	125	0.00
Bonded IPADs	i ŏ	i ŏ	Ŏ	i 2	i 0.00 i
l Bonded IOPADs	1 0	l 0	0	l 130	I 0.00 I
PHY_CONTROL	1 0	0	0	l 4	0.00
PHASER_REF	1 0	. 0	0	. 4	0.00
OUT_FIFO	1 0	0	0	16	0.00
I IN_FIFO	0	l Ü	Ü	l 16	0.00
I IDELAYCTRL I IBUFDS	1 0	I 0	U	l 4 l 121	0.00 0.00
PHASER OUT/PHASER OUT PHY	1 0	I 0	Ü	1 121 1 16	1 0.00 I
PHASER IN/PHASER IN PHY	iň	iň	Ň	l 16	0.00
IDELAYE2/IDELAYE2 FINEDELAY	i ŏ	i ŏ	Ŏ	i 200	i ŏ.ŏŏ i
I ILOGIC	i ŏ	i ŏ	Ŏ	i 125	i 0.00 i
OLOGIC	1 0	I 0	0	l 125	0.00
+	+	+		+	++

5. Clocking

Site Type	-+ Us:	+ ed +	Fixed	Prohibited	+ Available	++ Util%
BUFGCTRL BUF10 MMCME2_ADV PLLE2_ADV BUFMRCE BUFHCE BUFF	 	0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 0 0	16 1 4 1 4 1 8 1 72	0.00 0.00 0.00 0.00 0.00 0.00

6. Specific Feature

+	+	+		·	++
Site Type	l Used	Fixed	Prohibited	Available	Util%
+	+	+	H		++
I BSCANE2	1 0	I 0 I	0 1	l 4	I 0.00 I
I CAPTUREE2	1 0	0	0 1	l 1	I 0.00 I
I DNA_PORT	1 0	0	0 1	l 1	I 0.00 I
I EFUSE USR	1 0	0 1	0 1	l 1	I 0.00 I
FRAME_ECCE2	1 0	0 1	0 1	l 1	I 0.00 I
I ICAPE∑	1 0	0 1	0 1	1 2	I 0.00 I
I STARTUPE2	1 0	0 1	0 1	1	I 0.00 I
I XADC	1 0	0 1	0 1	l 1	I 0.00 I
+	+	+		L	++

7. Primitives

++	+	+
l Ref Name i	Used i	Functional Category
++	+	+
I FDRE I	131 I	Flop & Latch
I LUT4 I	49 I	LUT I
I LUT6 I	42 I	LUT I
I LUT3 I	39 I	LUT I
I LUT5 I	33 I	LUT I
I LUT2 I	8 I	LUT I
I LUT1	1 1	LUT I
++	+	+

(12)為了不讓報告太冗長,10M 的 Utilization.rpt 與其他.bit、.hwh 等,我有放到上傳作業壓縮檔:

[&]quot;\report\311651055_林柏宇\Report\10M"的路徑內。

3. Explain the function of IP in this design:

```
(1) Caravel Ps:
#include "ap_int.h"
#define NUM_IO 38
 void caravel_ps (
    ap_uint<NUM_IO> ps_mprj_in, //表示 PS 端的輸入信號。
    ap_uint<NUM_IO>& ps_mprj_out, //表示 PS 端的輸出信號,使用引用,意味著函數可以修改它。
    ap_uint<NVM_IO>& ps_mprj_en, //表示 PS 端的使能信號,同樣使用引用。
// Caravel flash interface
    ap_uint<NUM_IO>& mprj_in,//表示 Caravel Flash 端的輸入信號。
    ap_uint<NUM_IO> mprj_out,//表示 Caravel Flash 端的輸出信號。
    ap_uint<NUM_IO> mprj_en) {//表示 Caravel Flash 端的使能信號。
┴#pragma HLS PIPELINE //指示在函數中使用流水線化,以優化時鐘周期。
 /*#pragma HLS INTERFACE指示 Vivado HLS 如何對待函數的接口,
例如's axilite 表示對標準 AXI Lite 接口進行簡化的支持。*/
 #pragma HLS INTERFACE s_axilite port=ps_mprj_in
 #pragma HLS INTERFACE s_axilite port=ps_mprj_out
 #pragma HLS INTERFACE s_axilite port=ps_mprj_en
 #pragma HLS INTERFACE ap_ctrl_none port=return
#pragma HLS INTERFACE ap_none port=mprj_in //
 #pragma HLS INTERFACE ap_none port=mprj_out //
#pragma HLS INTERFACE ap_none port=mprj_en //
    ps_mprj_out = mprj_out;//將 Caravel Flash 的輸出信號複製給 PS 端的輸出信號。
    ps_mprj_en = mprj_en;//將 Caravel Flash 的使能信號複製給 PS 端的使能信號。
    for(i = 0; i < NUM_IO; i++) {</pre>
       #pragma HLS UMROLL//指示迴圈的展開,以實現更好的性能。
       /*mprj_in[i] = mprj_en[i] ? mprj_out[i] : ps_mprj_in[i];根據 Caravel Flash
的使能信號,選擇性地從 Caravel Flash的輸出信號或 PS 端的輸入信號中選擇數據,
       然後存儲在 Caravel Flash 的輸入信號中。*/
       mprj_in[i] = mprj_en[i] ? mprj_out[i] : ps_mprj_in[i];
(2) read romcode:
#define CODE_SIZE 2048*4 //定義了一個常數 CODE_SIZE,表示 ROM 代碼的大小,這裡設置為 2048*4,即 8KB。
void read_romcode(
// PS side interace
    /*以下表示 ROM 代碼的數組,使用整數數據類型,其大小為 CODE_SIZE 字節。*/
    int romcode[CODE_SIZE/sizeof(int)],
    /*以下表示 BRAM 的數組,用於存儲讀取的 ROM 代碼,同樣使用整數數據類型,其大小為 CODE_SIZE 字節。*/
    int internal_bram[CODE_SIZE/sizeof(int)],
int length)//表示要讀取的 ROM 代碼的長度,以整數表示。
   /*指示這是一個 AXI Lite 接口,並且沒有任何輸入或輸出,只有一個返回值。*/
    #pragma HLS INTERFACE s_axilite port=return
    /*以下表示指示這是一個 AXI Master 接口,用於讀取 romcode,並指定了一些相關的參數,
    如地址偏移、最大讀取突發長度等。*/
    #pragma HLS INTERFACE m_axi port=romcode offset=slave max_read_burst_length=64 bundle=BUSO
    #pragma HLS INTERFACE bram port=internal_bram //指示這是一個 BRAM 接口,用於存儲讀取的 ROM 代碼。
    #pragma HLS INTERFACE s_axilite port=length //指示這是一個 AXI Lite 接口,用於設置 ROM 代碼的讀取長度。
    // Check length parameter can't over than CODE SIZE/4
    /*以下檢查 length 參數,確保它不超過 CODE_SIZE 的大小,如果超過,則將其設置為 CODE_SIZE*/
    if(length > (CODE_SIZE/sizeof(int))) o
       length = CODE_SIZE/sizeof(int);
    // load ROMCODE
    for(i = 0; i < length; i++) {//用一個循環遍歷 romcode 中的元素,length 決定了循環的次數。
       #pragma HLS PIPELINE
       internal_bram[i] = romcode[i];//將讀取的 ROM 代碼從 romcode 數組複製到 internal_bram 數組中。
```

(3) spiflash:

(a)輸入/出如下:

input ap_clk:FPGA 的時鐘信號。

input ap_rst:FPGA 的重置信號。

output [31:0] romcode_Addr_A: BRAM 的地址。

output romcode_EN_A:使能 BRAM 的信號。

output [3:0] romcode_WEN_A: BRAM 的寫使能信號。

output [31:0] romcode_Din_A: 寫入 BRAM 的數據。

input [31:0] romcode_Dout_A:從 BRAM 讀取的數據。

output romcode_Clk_A:BRAM 的時鐘信號。

output romcode_Rst_A:BRAM 的重置信號。

input csb: SPI Flash 的片選信號。

input spiclk: SPI Flash 的時鐘信號。

input [0:0] io0:SPI Flash 的輸入信號。

output iol:SPI Flash 的輸出信號。

(b) 內部變數:

reg [7:0] buffer:緩衝器,用於暫存輸入的 SPI 數據。

reg [3:0] bitcount:位計數,用於跟蹤 SPI 數據的位。

reg [12:0] bytecount:字節計數,用於跟蹤 SPI 數據的字節。

reg [7:0] outbuf:輸出緩衝器,在 spiclk 下降沿更新。

(c) BRAM 接口:

assign romcode_Addr_A = {8' b0, spi_addr}; : 將 SPI 地址的低 8 位添加到 BRAM 地址的高 8 位。

assign romcode_Din_A = 32'b0; : 將 32 位的 BRAM 寫入數據設置 為零。

assign romcode_EN_A = (bytecount >= 4); : 使能 BRAM 的信號, 當字節計數大於等於 4 時為真。

assign romcode_WEN_A = 4'b0; : BRAM 的寫使能信號設置為零。 assign romcode_C1k_A = ap_c1k; : BRAM 的時鐘信號使用 FPGA 的時鐘信號。

assign romcode_Rst_A = ap_rst;: BRAM 的重置信號使用 FPGA 的重置信號。

(d) SPI 動作任務:定義了一個名為 spi_action 的任務,其中包含了 SPI 讀取動作的邏輯,主要是根據字節計數和 SPI 命令更新 SPI 地址和緩衝器。

- (e) 輸出 IO1: assign io1 = outbuf[7]; : 將 outbuf 的最高位賦 值給 io1,即作為 SPI Flash 的輸出。
- (f) SPI Flash 操作邏輯:在 always @(negedge spiclk or posedge csb)區塊中,根據 SPI 時鐘和片選信號的變化,更新緩衝器、位計數、字節計數和 SPI 地址等內部狀態,同時執行 SPI 讀取動作。
- (g) SPI Flash 輸出邏輯:在 always @(negedge spiclk or posedge csb)區塊中,使用另一個緩衝器 outbuf 來暫存輸出,並在 SPI 時鐘下降沿時更新。
- 4. Screenshot of Execution result on all workload:

```
INFO: [Common 17-206] Exiting Vivado at Wed Nov 22 06:51:10 2023...
INFO: [HLS 200-802] Generated output file hls_caravel_ps.prj/solution1/imp
INFO: [HLS 200-111] Finished Command export_design CPU user time: 9.75 sec
INFO: [HLS 200-112] Total CPU user time: 18.91 seconds. Total CPU system t
INFO: [Common 17-206] Exiting vitis_hls at Wed Nov 22 06:51:13 2023...

vitis_hls complete

//course-lab_5/labi
ubuntu@ubuntu2004:~/course-lab_5/labi$
```

Vitis Done

Vivado 10M Done

```
open_run: Time (s): cpu = 00:00:15 ; elapsed = 00:00:16 . Memory (MB): peak = 3189
# report_timing_summary -file timingreport.txt
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max.
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of
# exit
INFO: [Common 17-206] Exiting Vivado at Wed Nov 22 04:43:32 2023...

vivado complete

ubuntu@ubuntu2004:~/course-lab_5/labi$ ■
```

Vivado 50M Done

```
print ("0x10 = ", hex(ipPS.read(0x10)))
print ("0x14 = ", hex(ipPS.read(0x14)))
print ("0x1c = ", hex(ipPS.read(0x1c)))
print ("0x20 = ", hex(ipPS.read(0x20)))
print ("0x34 = ", hex(ipPS.read(0x34)))
print ("0x38 = ", hex(ipPS.read(0x38)))

0x10 = 0x0
0x14 = 0x0
0x1c = 0xab510041
0x20 = 0x0
0x34 = 0x0
0x38 = 0x3f
```

10M Case Result

50M Case Result

5. caravel_fpga.ipynb :

```
from __future__ import print_function
import sys
import numpy as np
import matplotlib.pyplot as plt
sys.path.append('/home/xilinx')
from pyng import Overlay
from pyng import allocate
ROM_SIZE = 0x2000 #8K
                                                                                    Python
ol = Overlay("/home/xilinx/jupyter_notebooks/ipy_fpga/caravel_fpga.bit")
                                                                                    Python
ipOUTPIN = ol.output_pin_0
ipPS = ol.caravel_ps_0
ipReadROMCODE = ol.read_romcode_0
                                                                                    Python
```

分別在定義參數、Instance IP、Download Bitstream 到 FPGA

```
# Create np with 8K/4 (4 bytes per index) size and be initiled to 0
rom_size_final = 0
npROM = allocate(shape=(ROM_SIZE >> 2,), dtype=np.uint32)
for index in range (ROM_SIZE >> 2):
    npROM[index] = 0
npROM\_index = 0
npROM offset = 0
fiROM = open("counter_wb.hex", "r+")
#fiROM = open("counter_la.hex", "r+")
#fiROM = open("gcd_la.hex", "r+")
for line in fiROM:
    if line.startswith('@'):
        # Ignore first char @
        npROM_offset = int(line[1:].strip(b'\x00'.decode()), base = 16)
        npROM_offset = npROM_offset >> 2 # 4byte per offset
        #print (npROM_offset)
        npROM_index = 0
    buffer = 0
    bytecount = 0
    for line byte in line.strip(b'\x00'.decode()).split():
        buffer += int(line_byte, base = 16) << (8 * bytecount)</pre>
    bytecount = 0
    for line_byte in line.strip(b'\x00'.decode()).split():
        buffer += int(line_byte, base = 16) << (8 * bytecount)</pre>
        bytecount += 1
        if(bytecount == 4):
            npROM[npROM_offset + npROM_index] = buffer
            buffer = 0
            bytecount = 0
            npROM_index += 1
```

上面那段是 /4 之後放入 BRAM(因為 BRAM 以 4byte 為單位存放),下面 那段是每 4 個 byte 為單位存到 buffer 裡面。

npROM[npROM_offset + npROM_index] = buffer

if (bytecount != 0):

npROM_index += 1

```
# 0x00 : Control signals

# bit 0 - ap_start (Read/Write/COH)

# bit 1 - ap_done (Read/COR)

# bit 2 - ap_idle (Read)

# bit 3 - ap_ready (Read)

# bit 7 - auto_restart (Read/Write)

# others - reserved

# 0x10 : Data signal of romcode

# bit 31~0 - romcode[31:0] (Read/Write)

# 0x14 : Data signal of romcode

# bit 31~0 - romcode[63:32] (Read/Write)

# 0x12 : Data signal of length_r

# bit 31~0 - length_r[31:0] (Read/Write)

# Program physical address for the romcode base address

ipReadROMCODE.write(0x10, npROM.device_address)

ipReadROMCODE.write(0x10, npROM.device_address)

ipReadROMCODE.write(0x10, rom_size_final)

# ipReadROMCODE.write(0x10, rom_size_final)

# ipReadROMCODE start to move the data from rom_buffer to bram

ipReadROMCODE.write(0x00, 1) # IP Start

while (ipReadROMCODE.read(0x00) & 0x04) == 0x00: # wait for done

continue

print("Write to bram done")

Python
```

這裡有 buffer address、buffer size,確定正確後開始搬資料到 BRAM, 之後判斷是否搬完了。

```
# Release Caravel reset
# 0x10 : Data signal of outpin_ctrl
# bit 0 - outpin_ctrl[0] (Read/Write)
# others - reserved
print (ipOUTPIN.read(0x10))
ipOUTPIN.write(0x10, 1)
print (ipOUTPIN.read(0x10))
```

Data 都準備好了,先 read 確定 reset PIN 是 assert,去 deassert 它

```
while (1) {
    if (reg_la0_data_in > 0x1F4) {
        reg_mprj_datal = 0xAB410000;
        break;
    }
}
//print("\n");
//print("Monitor: Test 1 Passed\n\n"); // Makes simulation very long!
reg_mprj_datal = 0xAB510000;
```

這個 IP 用來讀相關的 register map,包含 mprj 的 $i \cdot o \cdot en$,這次要看的是 o(17 & 20),但我們只要 $16 \sim 31$ bits (17)。若 output 值與 reg_mprj_datal 是穩和,表示 firmware 跑完且 design 正確。