A high-performance ZVS full-bridge DC-DC 0-50-V/0-10-A power supply with phase-shift control

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A High-Performance ZVS Full-Bridge DC–DC 0–50-V/0–10-A Power Supply with Phase-Shift Control

Marcelo Brunoro and José Luiz F. Vieira

***Abstract*— This paper presents a high-performance dc–dc switching mode power supply designed to deliver a regulated 0–50-V/0–10-A output. The proposed power supply is based on a modified version of the zero-voltage switching (ZVS) full-bridge (FB) phase-shift dc–dc converter, which incorporates commutation auxiliary inductors to provide ZVS for the entire load range as well as a commutation aid circuit to clamp the output diode voltage. The control strategy is based on two control loops operating in cascade mode. The inner loop maintains a regulated output current, whereas the external voltage loop regulates the output voltage, independently of load and input-voltage changes. In order to obtain a high-reliability converter, the control circuit has been implemented using just two integrated circuits (IC's). The phase-shift regulator UC3875 IC generates the gate drive signal to the MOSFET's. The control loop regulators are implemented using the TL074 IC. A theoretical analysis was conducted, and experimental results were obtained for a 0–50-V/0–10-A power supply operating at 100 kHz.**

***Index Terms*— Adjustable power supply, high-performance dc–dc converter, ZVS converter.**

I. Introduction

EFFORTS HAVE been made to replace the conventional power supply by a switching mode power supply (SMPS). High-frequency operation results in SMPS with small weight and size. However, at high frequency, soft-commutation techniques must be employed. The zero-voltage switching (ZVS) technique can be used to increase the converter efficiency [1].

At high-power levels, the full-bridge (FB) ZVS phase-shift dc–dc converter has been an attractive choice, since it provides high-power density with high efficiency and low-electromagnetic interference [2]–[6]. Besides the constant frequency operation with linear output characteristics, it integrates the stray elements (junction capacitances and leakage inductance). Also, this converter incorporates the advantages of low-conduction losses present in hard-switching technology, as well as small-switching losses provided by soft-switching technology [5]–[7].

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Some strategies have been proposed in the literature to overcome the converter drawbacks. The ringing and overshoot across the output rectifier diodes can be reduced by using a dissipative clamp [3], a low-loss active clamp, which requires an additional power switch with its control circuit [9], a clamping circuit based on a transformer tertiary and four clamping diodes [8], and a clamping circuit which employs just two clamping diodes [6], [7].

The load range in which ZVS occurs can be extended by using the techniques proposed in [4], [7], and [10]–[13]. A saturable inductor can be used to increase the ZVS load range, but it does not ensure ZVS in the entire load range [10], [13]. By incorporating two additional power switches in the power stage, the converter can perform ZVS in almost full-load range. However, the converter reliability is reduced due to additional switches and their control circuits [12]. The transformer magnetizing current can be used to extend the ZVS load range. However, this technique does not perform ZVS in the full range of an adjustable SMPS, mainly when the output voltage and the output current are close to zero. Also, it increases the reactive circulating energy as well as the conduction losses [4], [7]. Two commutation auxiliary inductors can assure ZVS in the entire load and input-voltage range [11]. In spite of increasing the reactive circulating energy and the conduction losses, this strategy allows the dual-thyristor circuit to be incorporated [14], which protects the converter legs against short circuit, increasing the reliability.

This paper presents an adjustable SMPS based on the FB ZVS dc–dc power supply with phase-shift control, which yields an adjustable output voltage of 0–50 V with an adjustable output current of 0–10 A. In order to obtain a simple SMPS that results in low cost, high reliability, and high efficiency, a clamping circuit with two additional diodes and two small commutation auxiliary inductors to perform ZVS in all load and input-voltage range have been incorporated.

II. Power Stage Diagram

The power stage diagram of the adjustable SMPS is shown in Fig. 1. It is a high-performance dc–dc converter, based on the FB-ZVS pulsewidth modulation (PWM) converter [2]–[5].

To reduce the ringing and the overshoot across the output rectifier diodes, this converter incorporates the commutation aid circuit presented in [6] and [7]. In addition, to provide ZVS for the entire load and input range, with low-magnetizing current, commutation auxiliary inductors are included [11].

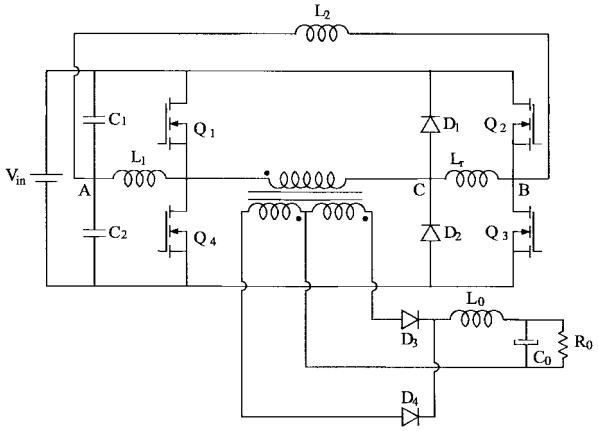


Fig. 1. Power stage diagram of the adjustable SMPS.

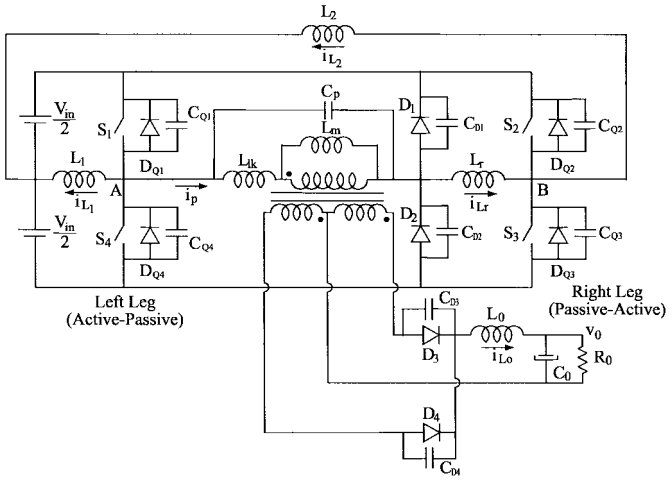


Fig. 2. Power stage circuit model.

The gate drive circuit used in this converter incorporates the dual-thyristor concept [14], shown in dashed lines in Fig. 14. This method prevents a switch from turning on before its voltage falls to nearly zero. Therefore, the dual-thyristor circuit adapts the delay time of each leg in order to perform ZVS. However, it requires enough energy stored in the magnetic elements to discharge the intrinsic capacitances of the switches. Also, the converter legs are intrinsically protected against short circuit, increasing the reliability [11].

A. Principle of Operation

This converter utilizes the phase-shift PWM control. This control method provides three voltage levels between the center points of the converter legs. The leg commutations occur under different conditions, which are described below.

The left-leg commutation leads the converter from the power transfer stage (active stage) to a freewheeling stage (passive stage). The output current source reflected to the transformer primary I_0' assures linear discharge of the switch intrinsic capacitances. The auxiliary inductor L_1 has been included to ensure ZVS mainly at no-load conditions.

The right-leg commutation is achieved with the output current source short circuited by the output diodes. This commutation leads the converter from the passive stage to the active stage. Thus, the available energy to perform this commutation is that stored in L_r and in the auxiliary inductor L_2. By introducing the auxiliary inductor L_2, ZVS is achieved from no load to full load, with low L_r values. For large L_r values, the rising and falling edge slopes of the primary current reduce the duty cycle available in the transformer primary [5], [11].

B. Stages of Operation

In order to simplify the analysis the following assumptions are made.

1) The MOSFET model is formed by an ideal switch S with a low on-state voltage drop, an ideal diode D_Q, and a constant capacitance C_Q.
2) The diode model is an ideal diode D with a low on-state voltage drop and a constant capacitance C_D.
3) The transformer model is represented by an ideal transformer with a leakage inductance L_{lk} and a parasitic capacitance C_P. The magnetizing inductance L_m is large enough such that its current is negligible.
4) The leakage inductance L_{lk} presents a low value, which is smaller than the resonant inductance L_r.
5) The voltage across L_{lk}, which is a result of the switch on-state voltage drop, reduces the transformer primary current in the freewheeling stages.
6) The commutation auxiliary inductors are considered as current sources, of values I_{L_1} and I_{L_2}, during the commutations since their inductances are greater than L_r and L_{lk}.
7) The capacitances C_1 and C_2 are large enough to be considered voltage sources at the switching frequency.

Based on the above assumptions, a half cycle of the converter operation can be described by seven stages. The equivalent circuits of each stage are shown in Fig. 3.

Just before t_0, the output current I_0 was freewheeling through output diodes D_3 and D_4, with D_4 current greater than D_3 current. Also, the transformer primary current was freewheeling through S_1, D_{Q1}, S_2, and D_1. The clamping diode D_1 was conducting the difference between the L_r current (i_{L_r}) and the transformer primary current (i_P).

1) **First Stage** (t_0, t_1)**—Right-Leg Resonant Commutation:** At instant t_0, S_2 is turned off, $v_{C_{Q3}} = V_{in}$, and $i_{L_r} = I_0'$. During this stage, $v_{C_{Q2}}$, $v_{C_{Q3}}$, and i_{L_r} change in a resonant fashion. As I_0 is freewheeling through D_3 and D_4, the commutation is ensured by the energy stored in L_r and L_2 (considered as a current source). This stage ends at instant t_1 when $v_{C_{Q3}}$ reaches zero, i_{L_r} becomes equal to i_P, and D_1 is turned off.
2) **Second Stage** (t_1, t_2)**—Linear Decreasing of** i_{L_r} **and** i_P**:** At instant t_1, D_{Q3} starts to conduct, and just after this, S_3 is turned on at zero voltage. During this stage, i_{L_r} and i_P decrease linearly, I_0 is kept freewheeling through D_3 and D_4, and there is a small resonance between C_{D1}, C_{D2}, C_P, and L_{lk}, which can be neglected. At the end of this stage, i_{L_r} and i_P reach zero, and the currents through D_3 and D_4 reach the same value.

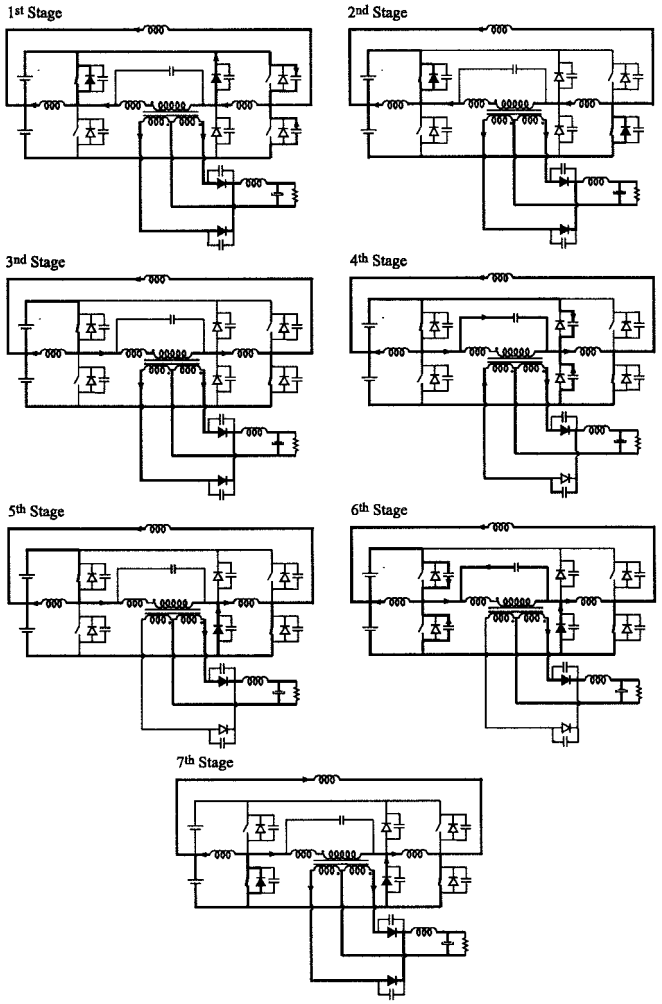


Fig. 3. Stages of operations.

3) **Third Stage** (t_2, t_3)—**Linear Increasing of** i_{L_r} **and** i_P**:** During this stage i_{L_r} and i_P rise linearly through S_1 and S_3 and I_0 is still kept freewheeling through D_3 and D_4. The small resonance mentioned in the second stage can be neglected too. However, $V_{C_{D2}}$ can be considered equal to V_{in}. At the end of this stage, i_{L_r} and i_P become equal to I_0', and the D_4 current reaches zero.
4) **Fourth Stage** (t_3, t_4)—**Resonant Increasing of** v_{Cp} **and** $v_{C_{D1}}$**:** During this stage v_{Cp}, $v_{C_{D1}}$, $v_{C_{D2}}$, and i_{L_r} change in a resonant way. Due to this resonance, i_{L_r} rises beyond $i_P = I_0'$. Power starts to be transferred from V_{in} to the load, through S_1, S_3, and D_3. The reverse recovery process of D_4 is initiated, and its voltage rises toward the total secondary voltage. This stage ends at t_4, when $v_{Cp} = V_{\text{in}}$ and $v_{C_{D2}}$ reaches zero.
5) **Fifth Stage** (t_4, t_5)—**Power Transfer:** During this stage, power is transferred from source V_{in} to the load through S_1, S_3, and D_3. The clamping diode D_2 conducts the difference between i_{L_r} and i_P. Due to D_4 reverse recovery process, its voltage presents an oscillation caused by C_{D4} and L_{lk}. As the transformer primary voltage is clamped to V_{in}, $v_{C_{D4}}$ is clamped to the total secondary voltage.

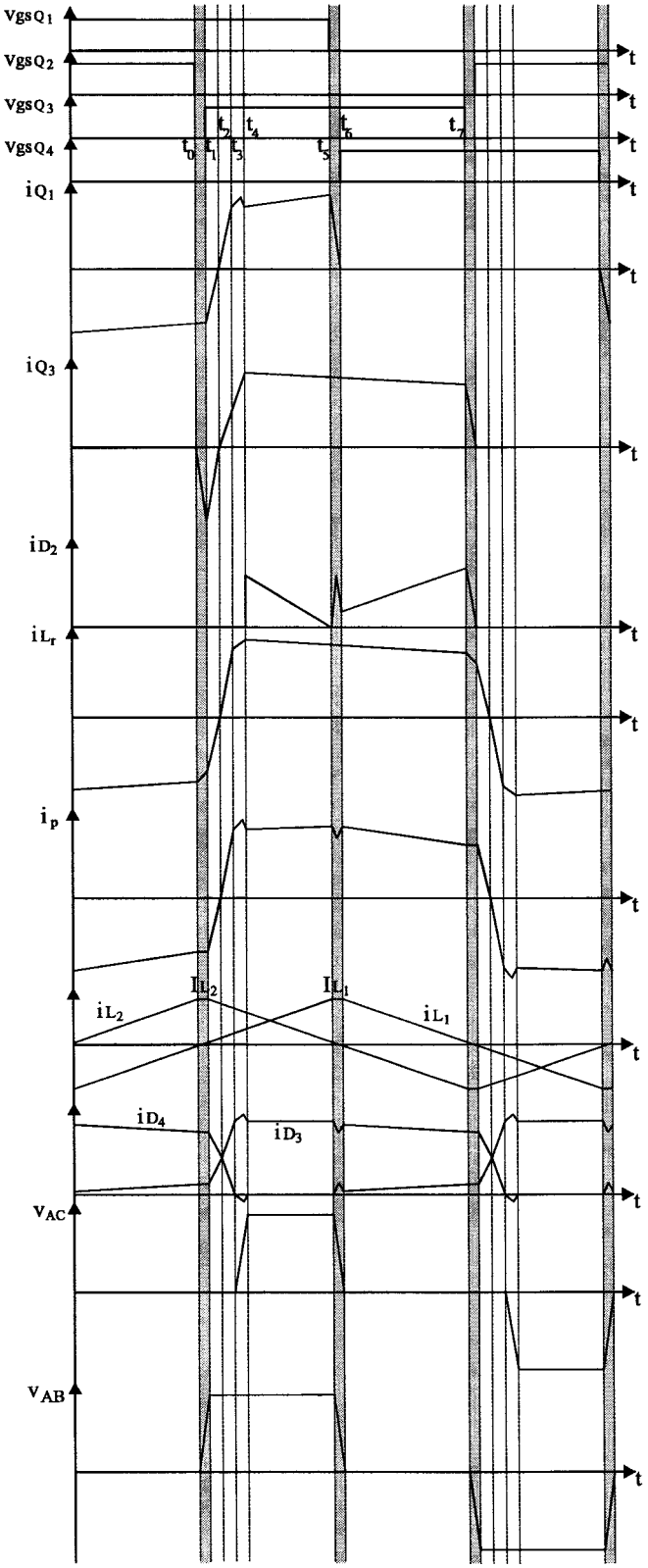


Fig. 4. Main waveforms of the converter.

6) **Sixth Stage** (t_5, t_6)—**Left-Leg Linear Commutation:** At instant t_5, S_1 is turned off. During this stage, $v_{C_{Q1}}$, $v_{C_{Q4}}$, and v_{Cp} change linearly due to I_0' and i_{L_1} (L_1 is considered as a current source). The current i_{L_r} is kept freewheeling through S_3 and D_2. The voltage $v_{C_{D4}}$ and

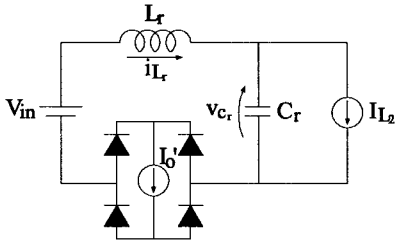


Fig. 5. Simplified circuit of the right-leg commutation.

the current i_P change in a resonant fashion due to C_{D4} and $L_{\rm lk}$. At the end of this stage, $v_{C_{Q4}}$ and $v_{C_{D4}}$ reach zero.

7) **Seventh Stage** (t_6, t_7)—**Freewheeling Stage:** At instant t_6, D_{Q4} starts to conduct and, just after this, S_4 is turned on at zero voltage. During this stage, I_0 is freewheeling through D_3 and D_4, with D_3 current greater than D_4 current. Also, i_P is freewheeling through S_4, D_{Q4}, S_3, and D_2. The clamping diode D_2 is conducting the difference between i_{L_r} and i_P.

The main waveforms, along with the gate drive signals, are shown in Fig. 4.

C. Commutation Analysis

1) Right-Leg Resonant Commutation: This commutation always takes place when the output current source is freewheeling through the output diodes. Thus, the available energy to perform the commutation is stored in L_r and L_2. Its analysis can be made based on the simplified circuit shown in Fig. 5, in which I_0' is freewheeling through the equivalent diode bridge, and L_2 is considered as a current source.

Initially, $v_{C_r} = V_{\rm in}$ and $i_{L_r} = -I_0'$. During this commutation, v_{C_r} and i_{L_r} change in a resonant way until v_{C_r} reaches zero. The relevant equations, valid for $|i_{L_r}(t)| \le I_0'$, are

$$v_{C_r}(t) = V_{\rm in} - \sqrt{\frac{L_r}{C_r}}\left(I_0' + I_{L_2}\right)\sin\omega_0 t \tag{1}$$

$$i_{L_r}(t) = I_{L_2} - \left(I_0' + I_{L_2}\right)\cos\omega_0 t \tag{2}$$

where $\omega_0 = 1/\sqrt{L_r \cdot C_r}$ and $C_r = C_{Q1} + C_{Q4} = C_{Q2} + C_{Q3}$.

As can be noticed in Fig. 5, while i_{L_r} is negative, it adds to I_{L_2} in discharging of C_r. Hence, to determine the I_{L_2} value, which ensures ZVS for entire load range, the following conditions must be considered.

1) $I_0' < I_{L_2}$: As the maximum value that i_{L_r} reaches is I_0', which is lower than I_{L_2}, there is always sufficient current to discharge C_r.
2) $I_0' \ge I_{L_2}$: In this case, it must be ensured that v_{C_r} becomes zero before i_{L_r} reaches I_{L_2} because after this moment, there is no net current to continue discharging C_r.

The second condition can be verified by the waveforms shown in Fig. 6 for $i_{L_r}(t) = I_0'$ and $I_{L_2} = I_0'$, and from (2) we have $\omega_0 t = \pi/2$. From (1) for $v_{C_r}(t) = 0$, one obtains the I_{L_2} value, which assures ZVS for the entire load and input

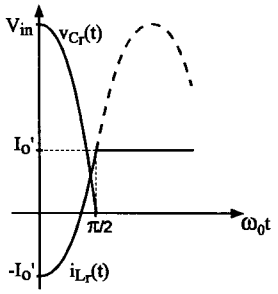


Fig. 6. Waveforms of right-leg commutation for $I_0' = I_{L_2}$.

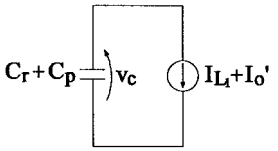


Fig. 7. Simplified circuit of the left-leg commutation.

range, as

$$I_{L_2} \ge \frac{V_{\rm in}}{2 \cdot \sqrt{\frac{L_r}{C_r}}}. \tag{3}$$

2) Left-Leg Linear Commutation: This commutation always occurs when I_0' is active, which provides a linear increasing of v_C. The current source I_{L_1} ensures the C_r discharges mainly for $I_0' = 0$. Its analysis can be made based on the simplified circuit of Fig. 7. The I_{L_1} value is established in order to charge $C_r + C_p$ in a specified time interval Δt_1 as

$$I_{L_1} \ge \frac{(C_r + C_p) \cdot V_{\rm in}}{\Delta t_1}. \tag{4}$$

III. Control Stage

The control stage shown in the block diagram of Fig. 8, allows the phase-shift dc–dc converter to function in one of the following modes: voltage source or current source. By using this control strategy, the output voltage and the output current can be adjusted individually.

When the output filter inductor current is lower than the value defined by the current limiter (corresponding to the voltage $v_{I\rm lim}$), the phase-shift dc–dc converter operates as a voltage source. In this condition, the two control loops operate in cascade mode, and the voltage regulator defines the current reference (corresponding to the voltage v_{VA}) to the current regulator. Also, the phase-shift dc–dc converter can operate as a current source for values of the output filter inductor current greater than the current limit. In this case, just the inner current loop is active.

A. Current Loop

The control strategy uses a fast inner current loop to maintain a regulated output current at the reference value (corresponding to the voltage $v_{I\rm ref}$). The current limiter circuit assures the converter operation as an adjustable current source. Consequently, the output current follows the value defined by the current limiter circuit $(v_{I\rm lim})$.

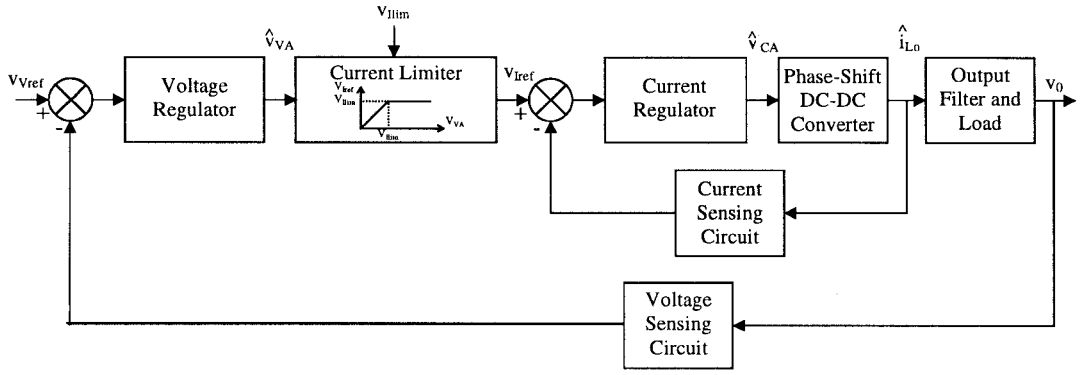


Fig. 8. Block diagram of the control stage.

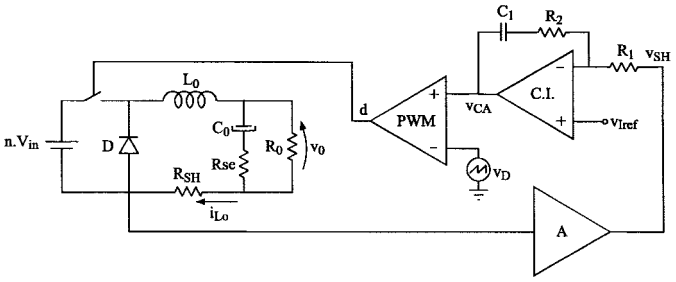


Fig. 9. Current loop equivalent circuit.

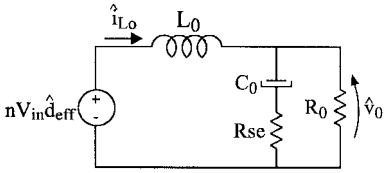


Fig. 10. Simplified small-signal circuit model.

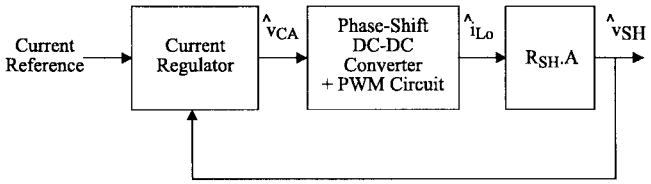


Fig. 11. Block diagram of the current loop.

The power stage of the phase-shift dc–dc converter can be considered as a buck-derived topology for control analysis. Hence, the current loop can be represented by the equivalent circuit shown in Fig. 9. However, the finite slope of i_{L_r} reduces the duty cycle of the secondary voltage modifying the dynamic characteristics of the phase-shift dc–dc converter.

The effective duty cycle of the secondary voltage can be expressed as [15]

$$D_{\text{eff}} = D - \Delta D \tag{5}$$

$$\Delta D = \frac{4nf_sL_r}{V_{\text{in}}}\left(I_{L_0} - \frac{V_0}{4f_sL_0}(1-D)\right) \tag{6}$$

where D is the duty cycle of the primary voltage set by the control circuit, ΔD is the loss of duty cycle due to the finite slope of the rising and falling edges of the primary current,

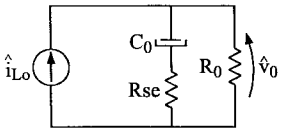


Fig. 12. Equivalent circuit model for the voltage control loop.

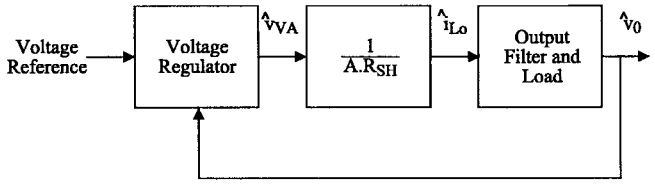


Fig. 13. Block diagram of the voltage loop.

$n = N_s/N_p$ is the transformer turns ratio, V_{in} and V_0 are the input and output voltages, f_s is the switching frequency, I_{L_0} is the output filter inductor current, and L_0 is the output filter inductance.

The small-signal analysis is performed considering a small ac perturbation component around the steady-state value of the converter variables. However, the effective duty cycle can be written as

$$d_{\text{eff}} = D_{\text{eff}} - \hat{d}_{\text{eff}} \tag{7}$$

where d_{eff} is the effective duty cycle of the secondary voltage, D_{eff} is the steady-state dc operating point of d_{eff}, and $\hat{d}_{\text{eff}}$ is the small ac perturbation.

Based on the analysis and from the averaged circuit model presented in [15] one can obtain, for V_{in} constant, the simplified small-signal circuit model of the phase-shift dc–dc converter operating in continuous conduction mode, shown in Fig. 10. This simplified circuit was developed assuming that the total change of d_{eff} is given by

$$\hat{d}_{\text{eff}} = \hat{d} - \hat{d}_i \tag{8}$$

where

$$\hat{d}_i = -\frac{R_d}{nV_{\text{in}}}\hat{i}_{L_0} \tag{9}$$

$$R_d = 4n^2 f_s L_r \tag{10}$$

where $\hat{d}$ is a small ac perturbation of the duty cycle D, $\hat{d}_i$ is the effect of the duty cycle modulation of d_{eff} due to the change

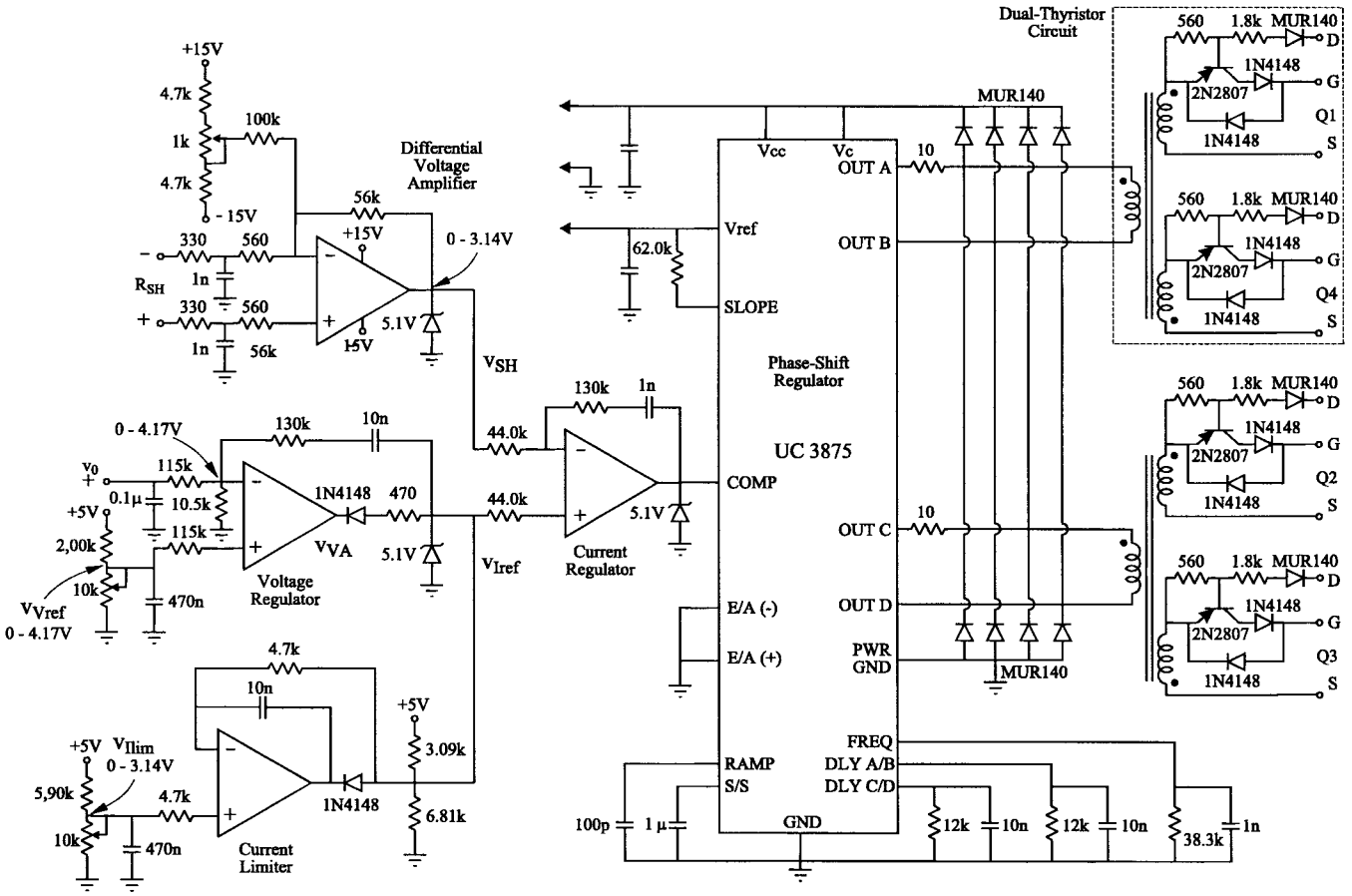


Fig. 14. Complete control stage diagram.

of the output filter inductor current, and R_d is an equivalent reactance.

The small-signal transfer function obtained from Fig. 10 is

$$\frac{\hat{i}_{L_0}(s)}{\hat{d}_{\text{eff}}(s)} = \frac{nV_{\text{in}}}{R_0} \cdot \frac{1 + sC_0(R_0 + R_{\text{se}})}{s^2 L_0 C_0\left(1 + \frac{R_{\text{se}}}{R_0}\right) + s \cdot \left[\frac{L_0}{R_0} + R_{\text{se}}C_0\right] + 1}. \tag{11}$$

Using (8) and (9) in (11) results in (12), given at the bottom of the page.

In the direct duty-cycle pulse-width modulator of the Fig. 9, the small-signal transfer function $\hat{d}(s)/\hat{v}_{CA}(s)$ is given by [16]

$$\frac{\hat{d}(s)}{\hat{v}_{CA}(s)} = \frac{1}{V_D} \tag{13}$$

where the control voltage v_{CA} is the output of the current regulator, which consists of a dc component and a small ac perturbation $\hat{v}_{CA}(s)$, and V_D is the maximum value of the sawtooth waveform v_D.

Therefore, the current loop can be represented by the block diagram shown in Fig. 11, from which the following transfer function can be obtained:

$$\frac{\hat{v}_{\text{SH}}(s)}{\hat{v}_{CA}(s)} = \frac{A \cdot R_{\text{SH}}}{V_D} \cdot \frac{\hat{i}_{L_0}(s)}{\hat{d}(s)} \tag{14}$$

where

$$\hat{v}_{\text{SH}}(s) = A \cdot R_{\text{SH}} \cdot \hat{i}_{L_0}(s) \tag{15}$$

is a small ac perturbation of the amplified voltage v_{SH}, R_{SH} is the shunt resistance, and A is the gain of a voltage differential amplifier.

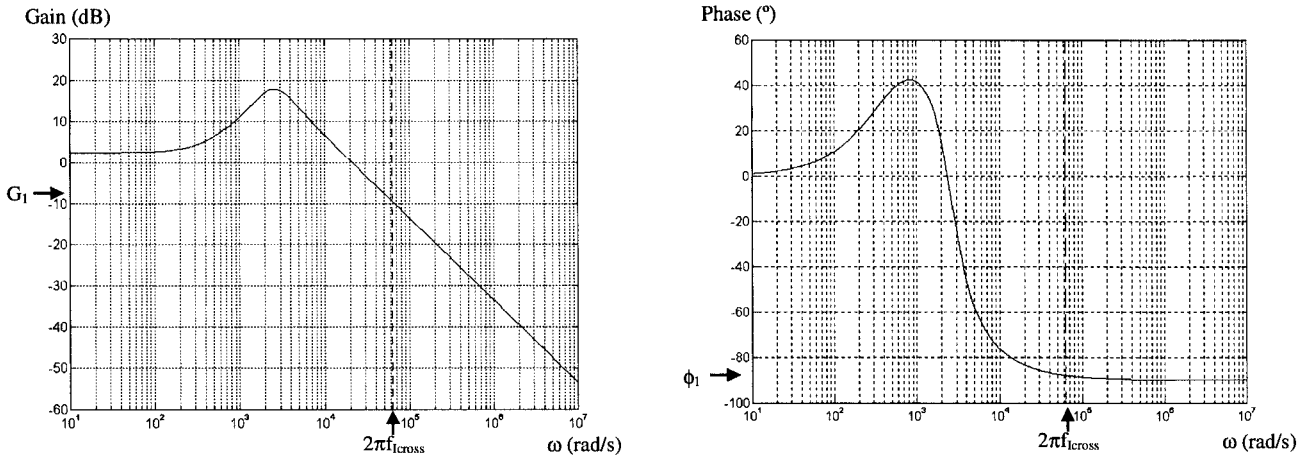
The current loop PI regulator presents the following small-signal transfer function:

$$\frac{\hat{v}_{CA}(s)}{\hat{v}_{\text{SH}}(s)} = \frac{R_2}{R_1} \cdot \frac{s + 1/R_2C_1}{s}. \tag{16}$$

Therefore, the overall open-loop current transfer function $T_{\text{OL}}(s)$ is obtained from Fig. 11 by multiplying (14) and (16).

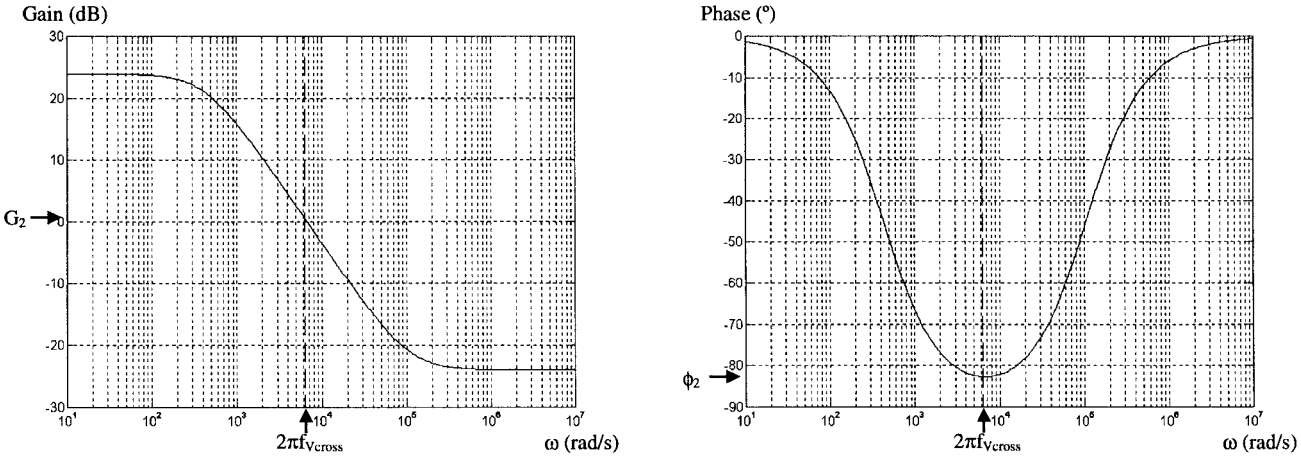
The PI parameters can be found by following the design procedure described in [16] or by altering the method presented in [17]. However, in order to use the Bode plots to determine the appropriate compensation in the feedback current loop, for

$$\frac{\hat{i}_{L_0}(s)}{\hat{d}(s)} = \frac{nV_{\text{in}}}{R_0} \cdot \frac{1 + sC_0(R_0 + R_{\text{se}})}{s^2 L_0 C_0\left(1 + \frac{R_{\text{se}}}{R_0}\right) + s \cdot \left[\frac{L_0}{R_0} + R_{\text{se}}C_0 + R_d C_0\left(1 + \frac{R_{\text{se}}}{R_0}\right)\right] + \frac{R_d}{R_0} + 1} \tag{12}$$



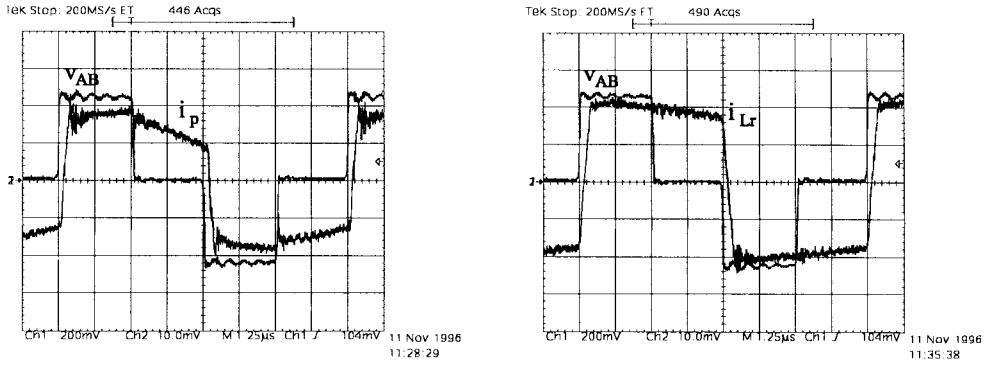
(a) (b)

Fig. 15. Current open-loop Bode plots: (a) gain and (b) phase.



(a) (b)

Fig. 16. Voltage open-loop Bode plots: (a) gain and (b) phase.



(a) (b)

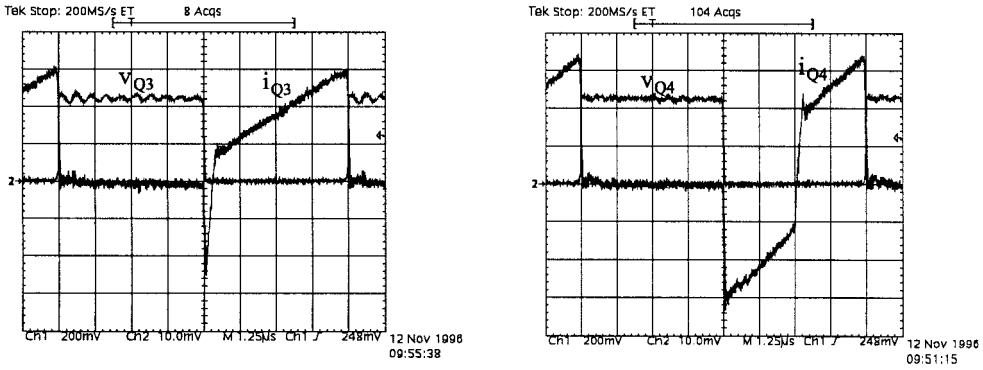
Fig. 17. Converter primary waveforms: (a) v_{AB} (100 V/div) and i_p (1 A/div) and (b) v_{AB} (100 V/div) and i_{L_r} (1 A/div); time scale: 1.25 μs/div.

the desired steady-state and transient responses, the crossover frequency of $T_{\rm OL}(s)$ must be smaller than the switching frequency. This can be assured by assuming

$$f_{I\rm cross} = \frac{f_s}{10} \tag{17}$$

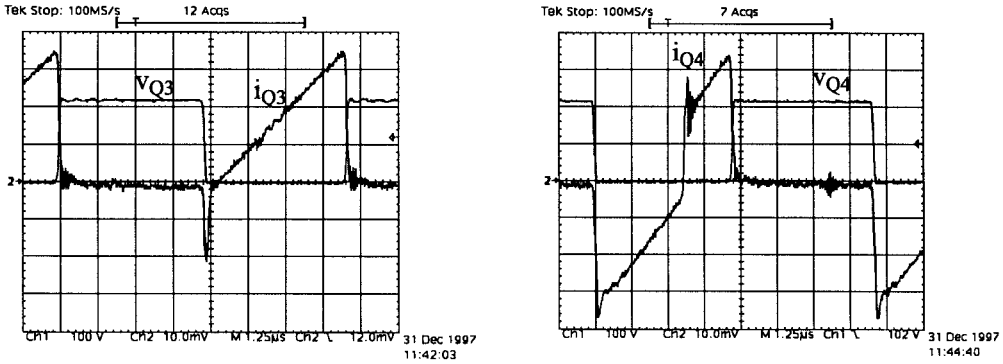
where the crossover frequency $f_{I\rm cross}$ is the frequency at which the gain of $T_{\rm OL}(s)$ falls to 1.0 (0 dB).

The phase margin of $T_{\rm OL}(s)$ at $f_{I\rm cross}$ determines the transient response of the output filter inductor current. Generally, a phase margin greater than 45° is used to meet a desired closed-loop performance.



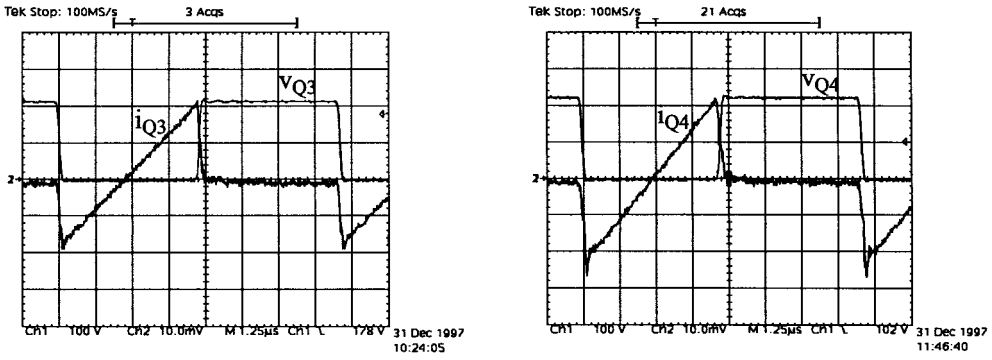
(a) (b)

Fig. 18. MOSFET's waveforms for $I_0 = 10$ A and $V_0 = 25$ V: (a) v_{Q3} (100 V/div) and i_{Q3} (1 A/div) and (b) v_{Q4} (100 V/div) and i_{Q4} (1 A/div); time scale: 1.25 μs/div.



(a) (b)

Fig. 19. MOSFET's waveforms for $I_0 = 2$ A and $V_0 = 20$ V: (a) v_{Q3} (100 V/div) and i_{Q3} (500 mA/div) and (b) v_{Q4} (100 V/div) and i_{Q4} (500 mA/div); time scale: 1.25 μs/div.



(a) (b)

Fig. 20. MOSFET's waveforms for $I_0 = 0$ and $V_0 = 0$: (a) v_{Q3} (100 V/div) and i_{Q3} (500 mA/div) and (b) v_{Q4} (100 V/div) and i_{Q4} (500 mA/div); time scale: 1.25 μs/div.

From the Bode plots of (14), which are shown in Fig. 15, one obtains the open-loop gain G_1 at low frequencies and the phase ϕ_1 at $f_{I\text{cross}}$.

The phase angle of the current loop PI regulator at $f_{I\text{cross}}$ is given by

$$\phi_c = \text{PM} - \phi_1 - 180^\circ. \tag{18}$$

The design of the current loop PI regulator requires the knowledge of the values of $f_{I\text{cross}}$, G_1, ϕ_1, and ϕ_c as well at the establishment of a phase margin (PM) and the choice of the capacitance C_1 of the PI regulator. Therefore, the PI regulator resistances can be obtained as follows:

$$R_1 = G_1 \cdot R_2 \tag{19}$$

$$R_2 = \frac{1}{2\pi f_{I\text{cross}} \cdot C_1 \cdot \text{tg}(-\phi_c)}. \tag{20}$$

B. Voltage Loop

The external voltage loop is responsible for keeping a regulated output voltage at the reference value. When the

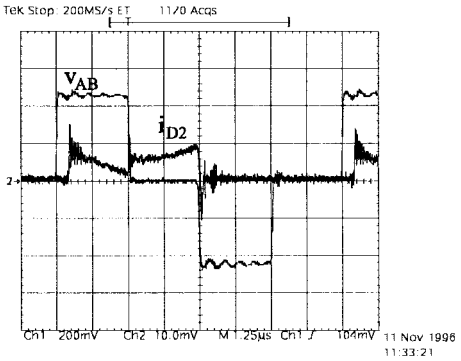


Fig. 21. Voltage v_{AB} (100 V/div) and the clamping diode current i_{D_2} (500 mA/div); time scale: 1.25 μs/div.

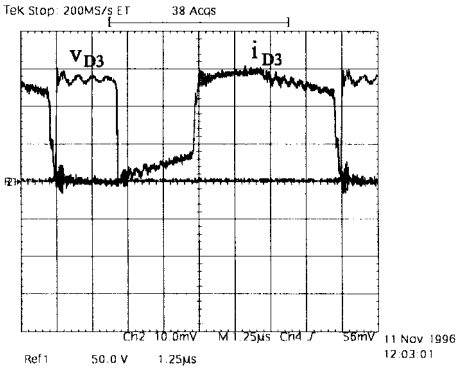


Fig. 22. Output diode waveforms: v_{D_3} (50 V/div) and i_{D3} (2 A/div); time scale: 1.25 μs/div.

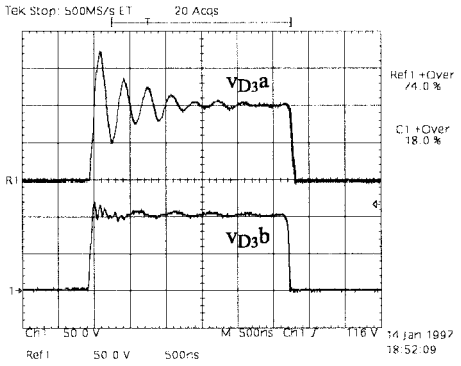


Fig. 23. Output diode voltage (50 V/div): $v_{D_3}a$ without and $v_{D_3}b$ with clamping circuit; time scale: 500 ns/div.

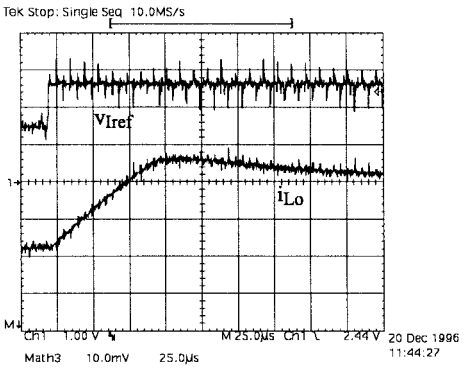


Fig. 24. Current i_{Lo} (2 A/div) for a step of 4.6–9.2 A in the current reference $v_{I\mathrm{ref}}$ (1 V/div); time scale: 25 μs/div.

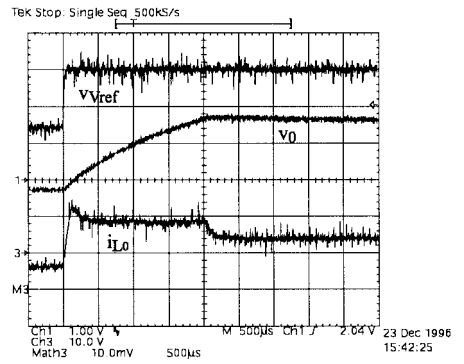


Fig. 25. Output waveforms for a step of 17.5–36 V in the voltage reference: $v_{V\mathrm{ref}}$ (1 V/div), v_0 (10 V/div), and i_{Lo} (5 A/div); time scale: 500 μs/div.

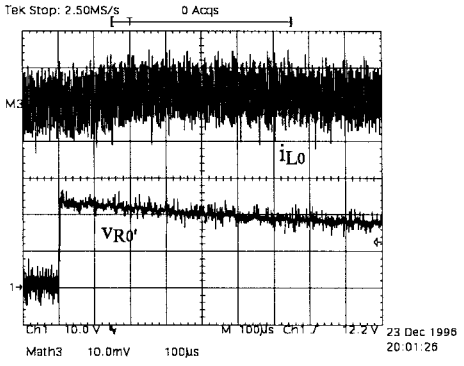


Fig. 26. Current i_{Lo} (100 mA/div) regulated in 5 A for a load step and v'_{Ro} (10 V/div); time scale: 100 μs/div.

phase-shift dc–dc converter operates as an adjustable voltage source, the output voltage follows the voltage reference $(v_{V\mathrm{ref}})$.

The voltage loop analysis and design can be performed in a straightforward way, since it has been dynamically separated from the current loop. This can be ensured making

$$f_{V\mathrm{cross}} = \frac{f_{I\mathrm{cross}}}{10} \tag{21}$$

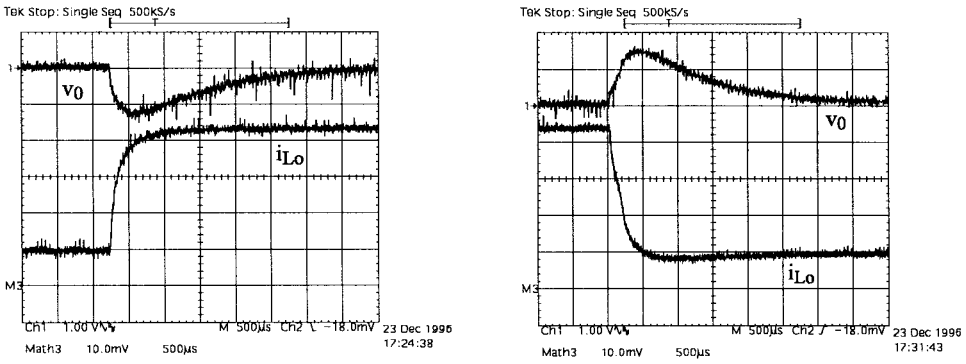
where $f_{V\mathrm{cross}}$ is the crossover frequency of the overall voltage open-loop transfer function.

Consequently, the current closed-loop transfer function can be considered as a simple gain to the voltage loop, which is given by

$$\frac{\hat{i}_{L_0}(s)}{\hat{v}_{VA}(s)} = \frac{1}{A \cdot R_{\mathrm{SH}}}. \tag{22}$$

Therefore, the power stage of the phase-shift dc–dc converter can be represented by the equivalent circuit shown in Fig. 12, from which one obtains the following transfer function:

$$\frac{\hat{v}_0(s)}{\hat{i}_{L_0}(s)} = R_0 \frac{C_0 \cdot R_{\mathrm{se}} \cdot s + 1}{C_0(R_0 + R_{\mathrm{se}})s + 1}. \tag{23}$$



(a) (b)

Fig. 27. Output waveforms for load changes, with $V_0 = 20$ V: (a) v_0 (1 V/div) and i_{Lo} (2 A/div) for a i_{Lo} step of 2–9 A and (b) v_0 (1 V/div) and i_{Lo} (2 A/div) for a i_{Lo} step of 9–2 A; time scale: 500 μs/div.

The complete voltage loop can be represented by the block diagram shown in Fig. 13, from which one can obtain

$$\frac{\hat{v}_0(s)}{\hat{v}_{VA}(s)} = \frac{R_0}{A \cdot R_{\rm SH}} \cdot \frac{C_0 \cdot R_{\rm se} \cdot s + 1}{C_0(R_0 + R_{\rm se})s + 1}. \qquad (24)$$

Following the design procedure, which has been applied to the current loop, the parameters of the PI regulator of the voltage loop can be obtained.

The control stage was implemented using just two integrated circuits (IC's). The phase-shift regulator UC3875 IC provides the gate drive signals to the MOSFET's. The control loop regulators were implemented employing the TL074 IC. The complete diagram of the control stage circuit is shown in Fig. 14.

IV. Design Example and Experimental Results

A SMPS prototype was built to meet the following requirements:

1) input voltage: 220 V $\pm$ 10% dc;
2) output voltage: 0–50-V dc;
3) output current: 0–10-A dc;
4) switching frequency: 100 kHz.

The main parameters and components of the phase-shift dc–dc converter can be obtained from the design procedure presented in [11] and [18].

The transformer turns ratio $n = 1/3$ is obtained based on the voltage specifications. By assuming $\Delta I_{L_0} = 7\%$, $I_{0\max} = 0.7$ A, and $D_{\min} = 0$, from [11] and [18] one obtains $L_0 = 364$ μH. Also, for $\Delta D = 0.1$ and $I_{L_0} = 10$ A, from (6) we have $L_r = 17$ μH .

The selected MOSFET's present $C_{DS} = 600$ pF, which results in $C_r = 1{,}2$ nF. However, from (3) one can define $I_{L_2} = 1.2$ A. Also, by assuming $\Delta t_1 = 300$ ns and $C_P = 200$ pF, from (4) one can define $I_{L_1} = 1.2$ A.

The power stage main parameters and components are:

1) switches: MOSFET IRFP360;
2) transformer: $N_p/N_s = 3$, $N_p = 24$ turns, and $N_s = 8$ turns on ferrite core EE 55/21;
3) $L_r = 17$ μH (eight turns on core EE 30/14);
4) auxiliary inductors: $L_{1,2} = 230$ μH (38 turns on ferrite core EE 30/7);
5) auxiliary capacitors: $C_1 = C_2 = 1$ μF/200 V;

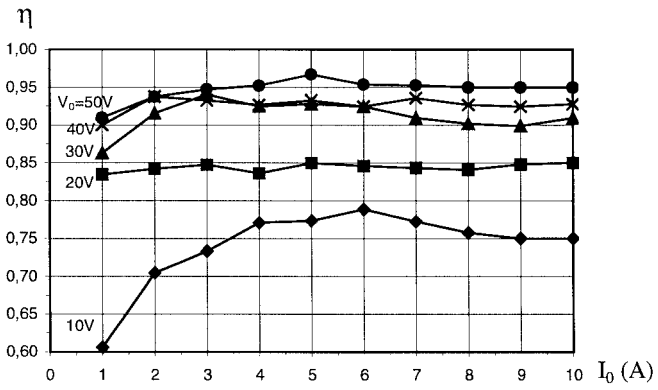


Fig. 28. Efficiency versus I_0 with V_0 as a parameter.

6) clamping diode: MUR140 and output diode: MUR620;
7) output filter: $L_0 = 360$ μH (EE 55/21) and $C_0 = 470$ μF with $R_{\rm se} = 0.02$ Ω;
8) maximum load resistance: $R_0 = 5$ Ω;
9) shunt resistance: $R_{\rm SH} = 5$ mΩ;
10) control circuit: $A = 63$ V/V and $V_D = 3$ V.

From the Bode plots shown in Fig. 15, one obtains $G_1 = 0.337$ V/V and $\phi_1 = -88°$. By assuming PM $= 85°$, $C_1 = 1$ nF, and $f_{I\rm cross} = f_s/10 = 10$ kHz, from (18), (19), and (20) we have $R_1 = 44$ kΩ and $R_2 = 130$ kΩ. By using the same procedure for the voltage loop, from the Bode plots shown in Fig. 16, one obtains $G_2 = 1.1$ V/V and $\phi_2 = -86°$. Selecting PM $= 87°$, $C_2 = 10$ nF, and $f_{\rm Vcross} = f_{I\rm cross}/10 = 1$ kHz, we have $R_3 = 115$ kΩ and $R_4 = 130$ kΩ.

The power stage waveforms at steady-state conditions with $f_s = 100$ kHz are shown in Figs. 17–23. The converter primary waveforms, obtained for $V_0 = 25$ V and $I_0 = 10$ A, are shown in Fig. 17. The MOSFET's waveforms for three different output conditions are shown in Figs. 18–20. These figures show that the converter performs ZVS even for $V_0 = 0$ and $I_0 = 0$. Figs. 21–23 have been obtained for $V_0 = 25$ V and $I_0 = 10$ A. Fig. 21 shows the voltage v_{AB} and the clamping diode current. The output diode waveforms are shown in Fig. 22. The clamping circuit operation can be verified by the waveforms of Fig. 23.

The converter waveforms at transient conditions are shown in Figs. 24–27. The output current for a step in the current reference is shown in Fig. 24. From this figure, one can verify

that the output filter inductor current presents: rise time close to 50 μs, overshoot of 15%, and 300 μs for the settling time. The output waveforms for a step in the reference voltage are shown in Fig. 25, from which one can notice the linear charging of the output capacitor in 2 ms. Fig. 26 shows the output inductor current i_{Lo}, regulated in 5 A for a load step consisting in an additional load R_0'.

The output waveforms under load changes are shown in Fig. 27. This figure shows that the converter comes back to its steady state value in 3 ms.

The converter efficiency versus I_0 with V_0 as a parameter is shown in Fig. 28. The efficiency measured for $V_0 = 50$ V and $I_{Lo} = 10$ A was 95%.

V. Conclusion

This paper introduced an adjustable SMPS which provides high efficiency and reliability. By including a commutation aid circuit, the ringing and the overshoot across the output rectifier diodes are reduced. The ZVS for the entire load range is obtained by incorporating commutation auxiliary inductors in the converter power stage. In order to provide both adjustable voltage and current, two control loops operating in cascade mode have been implemented. The inner loop regulates the output current at a reference value, whereas the external voltage loop keeps a constant output voltage, at a specified value, independently of load and input-voltage changes. The SMPS reliability is increased by using just two IC's to perform the control loops. The experimental results demonstrate the high efficiency of this SMPS and show the fast operation of the control loops, which provide a good regulation.

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