Phase-Shifted Full Bridge Converter Featuring ZVS over the Full Load Range

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***Abstract*— A new full-bridge circuit which can achieve zero voltage switching (ZVS) for all the primary side switches over the full load range and a wide input voltage range is proposed. The ZVS is achieved by the energy stored in the auxiliary inductor and the magnetizing inductance of the transformer. Because the leakage inductance is relatively small, there is no severe duty ratio loss or severe voltage ringing across the output rectifier. As the assistant current for achieving ZVS is almost the same for any duty ratio, the conduction losses at light load are reduced. The principal operation of the converter is described, and the optimal design is discussed. Finally, the operation of the converter is verified on a 1kW prototype.**

I. INTRODUCTION

The zero-voltage switching (ZVS) phase-shift full-bridge (PSFB) converter has been widely used in medium- or high-power application [1]-[3]. It has several desirable features, such as low component stresses, low EMI, constant switch frequency and soft switching for all switching devices by utilizing the parasitic capacitor of the power MOSFET and the leakage inductor. In a conventional PSFB, ZVS of the leading leg can only be achieved over a limited load range, and attention must be spent on the leakage inductance. A large leakage inductance, which can extend the ZVS range, has several drawbacks such as duty cycle loss, high voltage ringing across the rectifier diodes and large circulating current [4].

A number of techniques have been proposed to improve the performance of the ZVS PSFB converter [5]-[7]. In [8] and [9], the ZVS range of the PSFB is extended and no output inductor is needed by using series-connected two transformers. In [9], the conduction losses are reduced by adding a boost capacitor. However, the duty cycle loss is still serious. In the approaches proposed in [10]-[16], full-range ZVS of primary switches is achieved by utilizing adaptive energy stored in inductive components of an auxiliary circuit. The energy stored in the auxiliary circuit is adaptive according to the phase shift i.e. the load condition, so circulating energy is reduced. As the auxiliary inductor does not appear in the power-transfer path, it does not cause serious duty cycle loss or voltage ringing. However, at critical continuous condition, the operation duty ratio is still large while the reflected load current is nearly zero, so the inductance of the auxiliary circuit must be small enough to ensure enough assistant current to achieve ZVS. As a result, the conduction losses are large at light load.

A new full-bridge circuit is proposed, which uses the adaptive energy stored in the auxiliary inductor and the transformer magnetizing inductor to achieve ZVS over full line and load range. As the duty ratios of the auxiliary inductor and the transformer are complementary, the assistant current is almost constant. As a result, the inductance of the auxiliary circuit can be larger, and the conduction losses at light load are reduced. The circuit configuration, the operational principle and the converter performance of the presented topology are introduced in section II. Then the optimal design for achieving ZVS and high efficiency is discussed in section III. Finally, the analysis is verified on a 1kW prototype.

II. OPERATION PRINCIPLE

Fig. 1 shows the proposed circuit topology which can be divided into two independent parts: one is the standard PSFB converter with a smaller magnetizing inductance L_m; the other is the transition auxiliary circuit including a transformer TR_x and an inductor L_x.

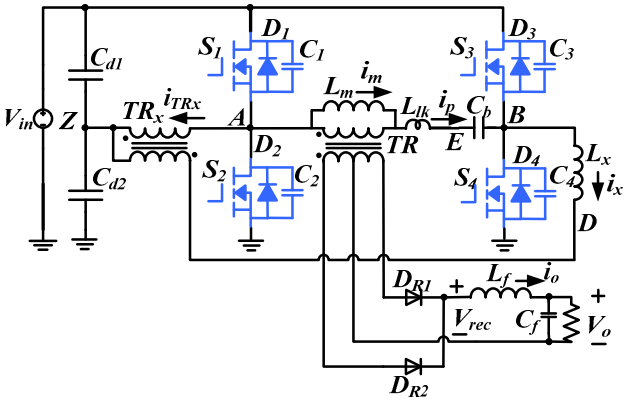

Fig. 1. Proposed ZVS full-bridge converter.

The primary side of the power transformer *TR* is connected between the leading leg output *A* and the lagging leg output *B*. A small capacitor C_b is inserted on the primary side of *TR* for blocking dc voltage unbalance. L_{lk} is the leakage inductance of *TR*, which is much smaller than that in a conventional PSFB. The secondary side of the *TR* is connected to a full-wave rectifier. Other types of rectifiers can also be used.

In order to achieve ZVS over the full load range, the primary side of an auxiliary transformer TR_x is connected between the leading switching leg output *A* and the center-tap of the a capacitive divider in the DC bus. One of the terminals

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of the secondary winding of TR_x is also connected to the capacitive center-tap. The other secondary output is connected in series with an inductor L_x, which, by its turn, is connected to the lagging leg output *B*. The inductance of L_x is designed to have a same valve with the magnetizing inductance of the transformer *TR*. A small DC blocking capacitor may need to be inserted between the terminal of L_x and the lagging leg output *B*, which is not drawn for simplicity.

To simplify the analysis, it is assumed that each switch device is ideal with a fixed output capacitor value. The auxiliary transformer is assumed to be ideal with a turn ratio of $n_{TRx} = 1$. The turn ratio of the transformer *TR* is $n_{TR} = N_p/N_s$. N_p and N_s are the numbers of primary-winding turns and secondary-winding turns of *TR,* respectively. The DC bus capacitors C_{d1} and C_{d2} are assumed to be large enough to achieve a constant voltage equal to $V_{in}/2$ across each capacitor.

Fig. 2 illustrates representative waveforms of the circuit in Fig. 1. The voltage across the auxiliary inductor L_x ($v_{BD} = v_{BZ} - v_{DZ}$) is illustrated in Fig. 2. Generally, the voltage second products of the transformer *TR* and the auxiliary inductor L_x both depend on the phase shift between the turn-on instants of the corresponding switches in the bridge legs, and the sum of them is almost constant. Therefore, the sum of the two current i_x and i_m is almost constant at the transition of leading leg for any duty ratio.

Fig.3 shows the equivalent circuits of the operation stages in half switching cycle.

Stage 1 (*t0-t1*): Before *t1*, switch S_1 and S_4 are conducting, and the voltage across the primary-winding of *TR* is almost equal to V_{in}. The magnetizing current i_m increases with the rate V_{in}/L_m. D_{R1} is off, and D_{R2} conducts the current i_o to the load. Because the voltage across the auxiliary inductor L_x is nearly zero, the current of L_x keeps at $-I_x$ during this stage, as shown in Fig. 2. The value of I_x can be expressed as follow:

$$I_x = \frac{V_{in}(1-D)}{4 f_s L_x}. \tag{2}$$

Stage 2 (t1-t2): At *t1*, *S4* is turned off, the output capacitors *C4* and *C3* are charged and discharged linearly by currents i_x and i_p until the voltage across *C4* reaches V_{in}, where i_p is the sum of reflected filter inductor current i_o/n_{TR} and the magnetizing current i_m. As the energy is from the output filter L_f, the magnetizing inductance L_m and the auxiliary inductor L_x, the charging and discharging is easily completed before dead time ends. The voltage across the primary-winding of the power transformer v_{AB} remains positive during this stage, so D_{R1} is still off, and D_{R2} conducts the output current.

Stage 3 (t2-t4): At *t2*, *C4* is fully charged to V_{in}, and the body diode *D3* conducts naturally. Then *S3* is turned on with zero voltage switching after dead time ends at *t3*. The equivalent circuit is shown in Fig. 3(c). The outputs of the two legs are shorted by switch *S1* and body diode *D3*, and the voltage across the primary-winding falls to zero. The primary current i_p decreases with the rate given by

$$\frac{di_p}{dt} = \frac{di_o}{n_{TR} dt} = -\frac{V_o}{n_{TR} L_f}. \tag{1}$$

At this stage, the voltage across the auxiliary inductor L_x is V_{in}. Therefore, current i_x increases with the slope V_{in}/L_x until it reaches its maximal value I_x at *t4*.

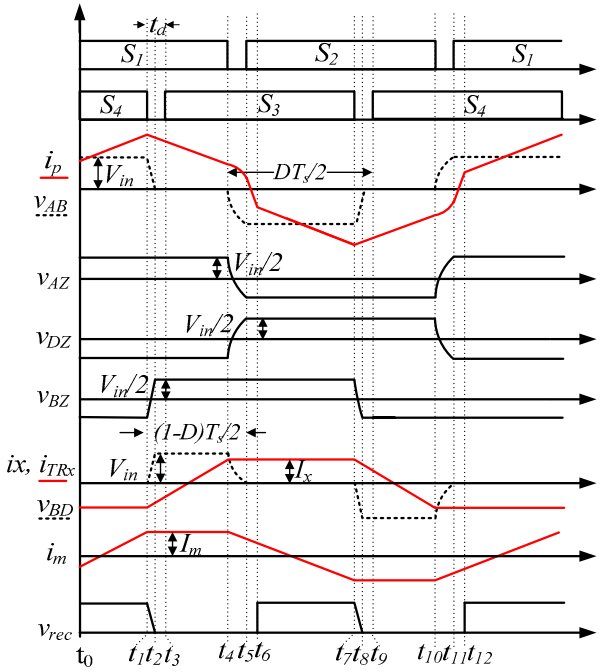

Fig. 2. Key operation waveforms of the proposed converter.

Stage 4 (t4-t5): At *t4*, after *S1* is turned off, *C1* and *C2* are charged and discharged by the currents i_p and i_x, as shown in Fig. 3(d). Because the magnetizing inductance L_m and the auxiliary inductance L_x are much larger than the leakage inductance L_{lk}, they can be treated as constant current sources during the transition time, the value of which can be expressed as (2) and (3). As L_x and L_m are designed to have the same value, the sum of the two currents I_x and I_m can be considered as one current source I_{cnst}, which can be expressed as (4). Besides, as seen from (4), I_{cnst} does not change with the duty ratio, so, with proper design, the conduction losses can be minimal for any duty ratio. The leakage inductor L_{lk} resonates with *C1* and *C2*, and the rest part of the primary current $i_{rsnt} = i_p - I_m$, which does not flow through the magnetizing inductor, decreases following a cosine wave. With the decrease of i_p, D_{R1} and D_{R2} conduct the output current i_o together. This stage ends when *C2* is discharged to zero and the body diode *D2* conducts.

$$I_m = \frac{DV_{in}}{4 f_s L_m} \tag{3}$$

$$I_{cnst} = \frac{V_{in}}{4 f_s L_x} = \frac{V_{in}}{4 f_s L_m} \tag{4}$$

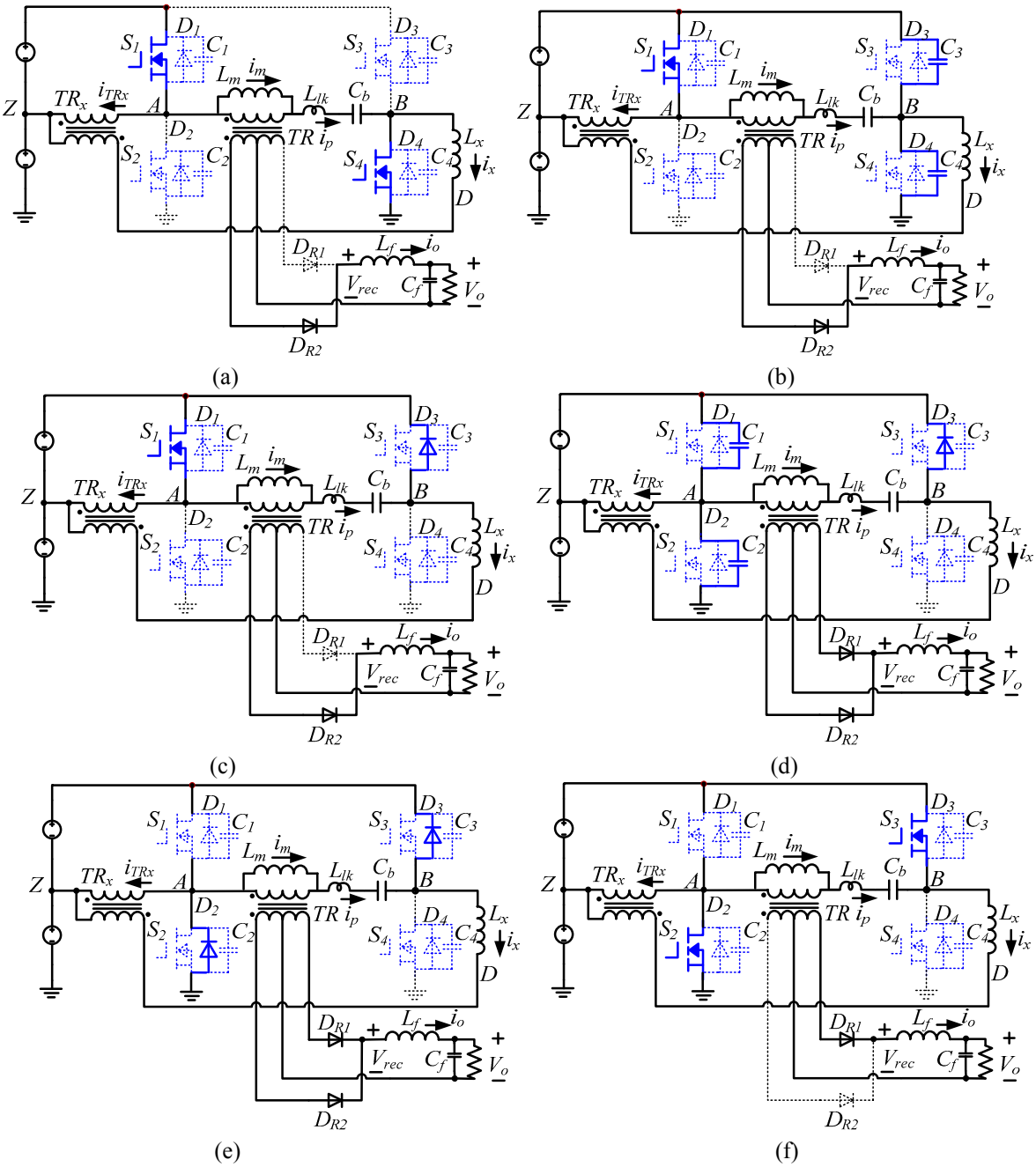

Fig. 3. Equivalent circuits of the operations stages in half switching cycle: (a) Stage 1 (t0-t1), (b) Stage 2 (t1-t2), (c) Stage 3 (t2-t4), (d) Stage 4 (t4-t5), (e) Stage 5 (t5-t6), (f) Stage 6 (t6-t7).

Stage 5 and Stage 6 (t5-t7): At *t5*, after the body diode *D2* conducts, *S2* is turned on at zero voltage, as shown in Fig. 3(f). The input voltage is applied on L_{lk}, so i_p decreases with the slope V_{in}/L_{lk} until it changes direction, and then D_{R2} turns off. The output current i_o flows through D_{R1}, and V_{in} is applied on the magnetizing inductor of *TR*. This stage ends when *S3* turns off at *t7*, and then the second half cycle starts, witch is similar to the first one.

III. DESIGN CONSIDERATION

To achieve ZVS over the full load range, the leakage and magnetizing inductance of *TR* and the auxiliary inductance should be designed properly.

A. ZVS Range for the Lagging Leg

The charging and discharging of the output capacitor *C4* and *C3* is achieved by the energy stored in output filter inductor L_f, magnetizing inductor L_m and auxiliary inductor L_x, all of which can be seen as constant current source. Further simplified equivalent circuit at this transition time is shown in Fig. 4(a). The equivalent capacitor $Cs = C1+C2$ is charged

by two current sources. From Fig. 2, the value of I_x and I_p can be described by (2) and (5).

$$I_p = \frac{I_o + \Delta I_o / 2}{n_{TR}} + \frac{DV_{in}}{4 f_s L_x} \tag{5}$$

I_o is the average output current, and ΔI_o given by (6) is the current ripple of the output filter inductor L_f. To achieve ZVS for the lagging leg, equation (7) must be satisfied, where t_d is the dead time illustrated in Fig. 2.

$$\Delta I_o = \frac{V_o(1-D)_s}{2 L_f f_s} \tag{6}$$

$$\frac{(I_x + I_p) t_d}{C_s} \geq V_{in} \tag{7}$$

B. ZVS Range for the leading leg

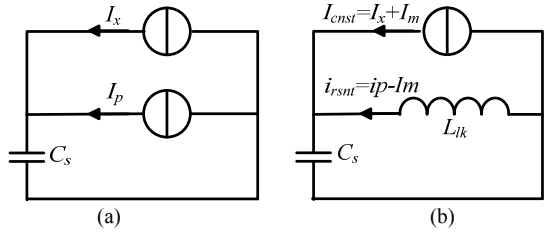

Fig. 4. Simplified transition equivalent circuits: (a) the lagging leg and (b) the leading leg

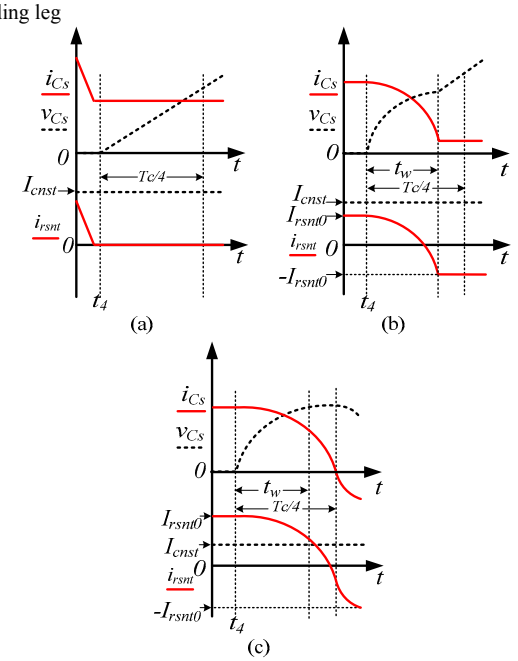

Fig. 5. Key waveforms of the leading leg during transition stage at different load. (a) $I_{rsnt0} = 0$ i.e. in DCM, Cs is charged by I_{cnst} linearly, (b) $0<I_{rsnt0}<I_{cnst}$, i_{rsnt} decreases to $-I_{rsnt0}$, and then clamped at $-I_{rsnt0}$, and (c) $I_{rsnt0}>I_{cnst}$, i_{rsnt} is not clamped and the voltage across Cs gets its maximal value at $t4 + Tc/4$.

The charging and discharging of output capacitors $C1$ and $C2$ is achieved by the energy stored in the leakage and magnetizing inductance of TR and the auxiliary inductor L_x. The further simplified equivalent circuit of the leading leg at the transition time is shown in Fig. 4(b). L_{lk} resonates with Cs during the transition period with the initial current I_{rsnt0} and resonant period Tc, which are given in (8) and (9) respectively.

$$I_{rsnt0} = (I_o - \Delta I_o / 2) / n_{TR} \tag{8}$$

$$Tc = 2\pi\sqrt{C_s L_{lk}} \tag{9}$$

There are three different cases for the transition of leading leg, according to the value relationship between I_{rsnt0} and I_{cnst} which is shown in Fig. 5 [13], [15].

Assuming the dead time to be $T_c/4$, we can get the voltage across the output capacitor Cs at the end of dead time for different leakage inductance, magnetizing inductance and auxiliary inductance. Fig. 6 and Fig. 7 show the results without considering the input voltage clamp. At the end of dead time, if voltage V_{Cs} is higher than the input voltage (V_{in} = 400V), ZVS can be achieved.

A conclusion can be drawn from Fig. 6 and Fig. 7 that if ZVS cannot be achieved, either a larger leakage inductance or a smaller auxiliary inductance should be used. Compared with the converters presented in [10] and [13], there's no large redundant assistant current at light load, so the conduction losses at light load is reduced.

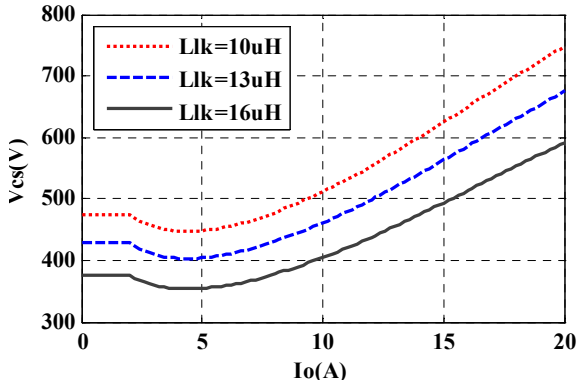

Fig. 6. Voltage across the parasitic capacitor Cs at the end of the transiting period versus load current I_o at different leakage inductance L_{lk} (L_x = 410 μ H , L_f = 26 μ H and V_{in} = 400V).

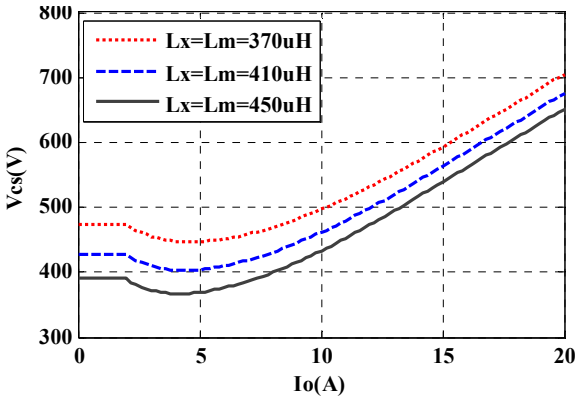

Fig. 7. Voltage across the parasitic capacitor Cs at the end of the transiting period versus load current I_o at different L_x and L_m (L_{lk} = 13 μ H, Lf = 26 μ H and V_{in} = 400V).

From the above analysis, larger leakage inductance and smaller auxiliary inductance is helpful to achieve ZVS. On the other hand, with smaller leakage inductance, duty cycle loss and voltage ringing can be reduced. So a compromise must be reached between conduction losses and duty cycle loss and voltage ringing.

IV. EXPERIMENTAL RESULTS

An lkW/100kHz (Input: 300-400 VDC; Output: 50V/20A) prototype is built to verify the operation. The main components and some key parameters are listed in Table I. To damp the ringing between the rectifier diodes and the leakage inductor, a RCD-snubber circuit is employed.

TABLE I Utilized Components and Parameters of the Prototype

Components	Parameters
Vin (Input voltage)	300 V-400V
Vout (Output voltage)	50 V
Pout (Maximum output power)	1000 W
f_s (Switching frequency)	100 kHz
L_f (output filter inductor)	26 μH
n_{TR} (Turns ratio of transformer)	19/4
L_m (magnetizing inductance)	420μH
L_x (auxiliary inductance)	381 uH
L_{lk} (Leakage inductance)	12.1 μH
S (Power MOSFETs)	IXFH24N50
D_R (Diodes)	MBR20200
t_d (dead time)	160ns
C (Output capacitor of MOSFET)	510pF
Controller	UC3895

Fig. 8 and 9 represent the voltage and current waveforms of *TR* and L_x at 50% load. It is shown that the voltage waveforms across *TR* and L_x are complementary, and the current i_x changes when i_p stays the same, which verifie the operation of the converter.

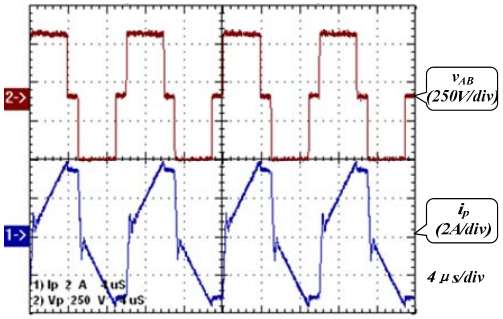

Fig. 8. Voltage and current waveforms of *TR* at 50% load.

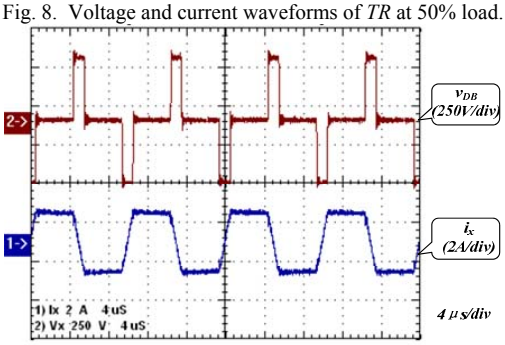

Fig. 9. Voltage and current waveforms of L_x at 50% load.

The ZVS operation waveforms of the leading leg and lagging leg at full load and 5% load are shows in the Fig. 10, respectively. As seen in all these waveforms, the drain voltage falls to zero before the rise of the corresponding gate voltage. ZVS operation is well achieved for all primary switches over the full load range.

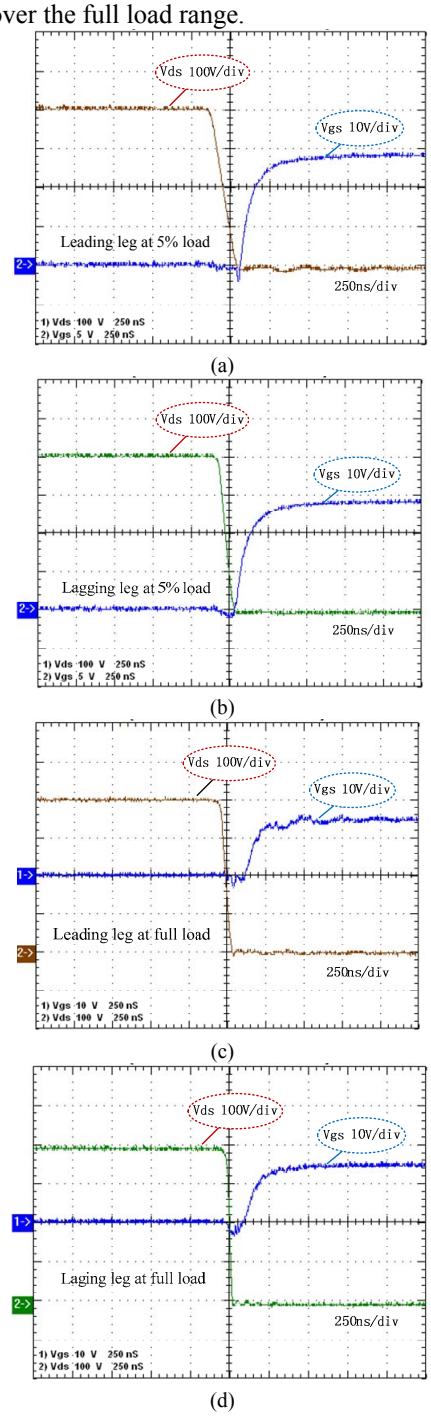

Fig. 10. Key waveforms of the leading and lagging switches at full and 5% load.

In order to illustrate the efficiency improvement, another similar converter is built, which only does not utilizing the magnetizing current. Because the magnetizing inductance of this converter is much larger than the auxiliary inductance, the auxiliary inductance must be much smaller than that in the proposed converter to ensure full load range ZVS. Fig. 11 shows the overall efficiency of the two similar converters, compared to a conventional PSFB converter utilizing a large leakage inductance. At high load the efficiencies of the two

similar converters are almost the same, and are both about 2% higher than the conventional one. However, at light load the proposed converter has a much higher efficiency than that without utilizing the magnetizing current, because the assistant current increases considerably when duty ratio is small in the converter without utilizing the magnetizing current. The efficiency higher than 90% is achieved from 20% load to full load, and the efficiency of 95% is achieved at full load for the proposed converter.

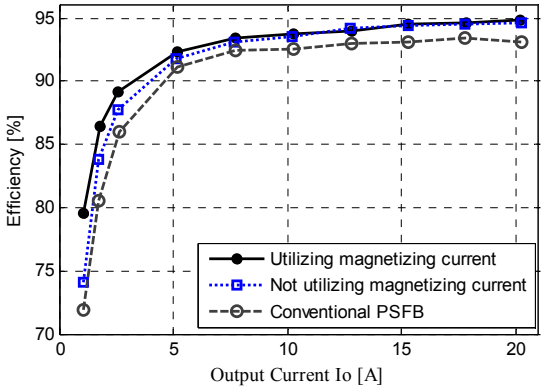

Fig. 11. Efficiency comparison.

V. CONCLUSION

A new phase-shift full-bridge circuit featuring ZVS over the full load range and a wide input voltage range is proposed in this paper. The ZVS is achieved using adaptive power stored in an auxiliary inductor and the magnetizing inductance of the power transformer. As the leakage inductance is much smaller compared to that of conventional phase-shift full-bridge converters, the duty cycle loss is reduced. Because the assistant current for achieving ZVS is almost the same for any duty ratio, there is no large redundant assistant current and the conduction losses are reduced at light load. The operation is verified on a 1kW prototype, and the overall efficiency is improved more than 2% with respect to the conventional PSFB converter.

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