DESIGN CONSIDERATIONS FOR HIGH-VOLTAGE HIGH-POWER FULL-BRIDGE ZERO-VOLTAGE-SWITCHED PWM CONVERTER

J.A. Sabaté, V. Vlatkovic, R.B. Ridley, F.C. Lee and B.H. Cho

Virginia Power Electronics Center
The Bradley Department of Electrical Engineering
Virginia Polytechnic Institute and State University
Blacksburg, Virginia 24061

ABSTRACT

The paper presents a steady-state analysis with complete characterization of the converter operation. A small-signal model of the converter is established. The design procedures based on the analysis are presented and the various losses in the circuit assessed. Critical design considerations for a high-power, high-voltage application are analyzed. The results of the analysis are verified using a high voltage, 2 kW prototype.[1]

1 INTRODUCTION

The achievement of efficient high-frequency power conversion requires reduction of switching losses. Conventional resonant converters can provide zero-current switching (ZCS) or zero-voltage switching (ZVS). They generally require a wide range of frequency control, thus making the optimization of the filter components difficult. Quasi-resonant and multi-resonant converters have been proposed for reduced frequency range [1,2], but the high component stresses make them impractical for high-power and high-voltage applications. The recently-introduced constant frequency resonant converters [3,4] can achieve ZCS or ZVS. However, it is at the expense of increased component stresses.

When conventional PWM converters are operated at higher frequencies, the circuit parasitics are shown to have detrimental effects on the converter performance. Switching losses are especially pronounced in high-power, high-voltage applications. Snubbers are normally required, thus adding significant losses in high frequency operation.

A recently proposed new operating mode of the full-bridge PWM converter permits all switching devices to operate under ZVS by using circuit parasitics to achieve resonant switching [5,6,7]. To achieve ZVS, the two legs of the bridge are operated with a phase shift. This operation allows a resonant discharge of the output capacitance of the MOSFETs, and, subsequently, forces the conduction of each MOSFET's antiparallel diode prior to the conduction of the MOSFET. Fig. 1 illustrates the waveforms in the circuit.

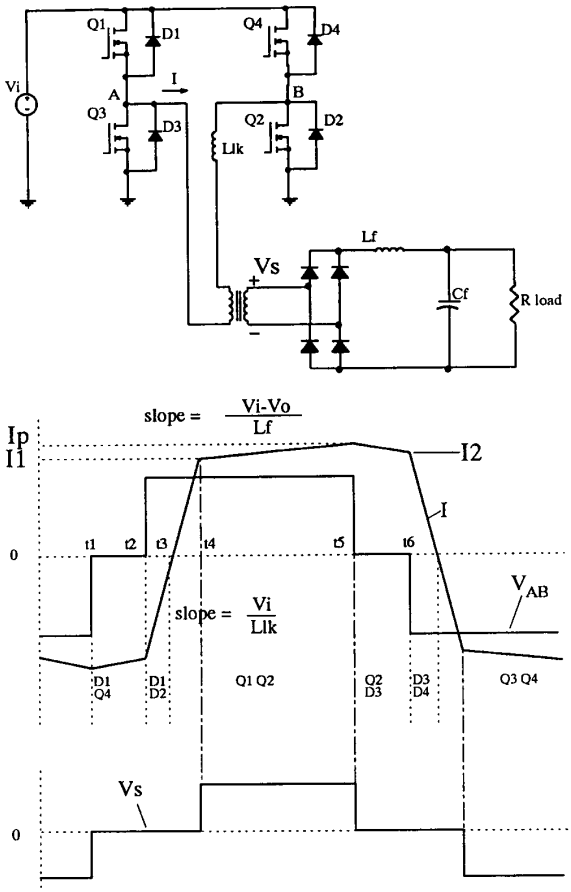

Fig. 1. : FB-ZVS-PWM converter and primary and secondary waveforms.

The zero-voltage switched PWM converter (ZVS-PWM) shown

[1] The work was supported by the International Business Machines Co., Kingston NY, and by the Virginia Center for Innovative Technology, Technology Development Center for Power Electronics.

in Fig. 1 requires no additional active devices, and utilizes leakage inductance of the power transformer to achieve ZVS. It has a somewhat higher rms current than the conventional full-bridge PWM converter, but has much lower rms currents than the resonant converters. The ZVS allows operation with much reduced switching losses and stresses, and eliminates the need for primary snubbers. It enables high switching frequency operation for improved power density and conversion efficiency. These advantages make this converter well suited for high-power, high-frequency applications.

The operation of this converter requires design considerations that differ from the conventional full-bridge PWM. The small-signal response of the ZVS converter also differs significantly from that of its PWM counterpart. The paper presents the complete steady-state analysis and the small-signal model of the ZVS-PWM converter. The paper also presents assessment of various losses in the circuit.

An analysis based design procedure is presented, and certain design considerations are discussed in the paper. A high-voltage, 2 kW prototype is built to verify the proposed design procedure. The small-signal and steady-state characteristics predicted from the analytical model are verified experimentally.

2 ANALYSIS

2.1 Principle of Operation

The full-bridge PWM converter is operated in a mode that provides zero-voltage turn-on for the active switches. The current and voltage in the transformer primary are shown in Fig. 1. The gating signals are such that, instead of turning on the diagonally opposite switches in the bridge simultaneously, a phase shift is introduced between the switches in the left leg and those in the right leg. This phase shift determines the operating duty cycle of the converter.

The zero-voltage turn-on is achieved by using the energy stored in the leakage inductance of the transformer to discharge the output capacitance of the switches before turning them on.

Q4 and D1 are conducting, and at time t_2, switch Q4 turns off and the current through the primary of the transformer charges the output capacitance of Q4 and discharges the output capacitance of Q2, turning on the diode D2. After D2 starts conducting, Q2 can be turned on with virtually no voltage applied across it. In order to achieve zero-voltage turn-on the energy stored in the leakage inductance has to be larger than the energy stored in the output capacitances. Therefore ZVS is lost for low load currents. The same is true for Q4 at t_6.

At time t_5, switch Q1 turns off and the current through the primary discharges the output capacitance of Q3 and charges the output capacitance of Q1, subsequently, diode D3 is turned on. After D3 starts conducting, Q3 can be turned on with no voltage applied across it. In this case, when Q1 turns off, the current through the primary of the transformer is the output current reflected to the primary. The energy of the large filter inductor in the secondary is used to achieve ZVS. Therefore, ZVS is achieved easily for the switches Q1 or Q3.

2.2 Steady-State Analysis

2.2.1 Required Dead Times

The mechanism by which ZVS is achieved is different for both legs of the bridge.

For transistors Q2 and Q4, the ZVS is provided by the resonance between the leakage inductance, L_{lk}, and the output capacitance of the switch. Figure 2a shows the waveform of the current through D2-Q2.

Before Q2 is turned off, the current in the primary is circulating through diode D3 and transistor Q2, and the primary voltage is clamped to zero. When Q2 is turned off, the current through the primary forces the diode D4 to turn on, and the energy remaining in the primary leakage inductance is returned to the source. In order to turn on D4, the output capacitance of Q4 has to be discharged and the output capacitance of Q2 charged to the input voltage. The energy available for charging the output capacitance of Q4 and charging the output capacitance of Q2 is the energy stored in L_{lk}, after t_2 (or t_6). Also, the transformer winding capacitance has to be charged in the process. Then the energy in L_{lk} has to be

$$E = \frac{1}{2} L_{lk} I_2^2 > \frac{4}{3} C_{MOS} V_{in}^2 + \frac{1}{2} C_{TR} V_{in}^2 \qquad (1)$$

where I_2 is the current through the primary at time t_2 (or t_6), V_{in} is the input voltage, L_{lk} is the transformer leakage inductance, C_{MOS} is the output capacitance of the switch at V_{in}, and C_{TR} is the transformer winding capacitance. The term $\frac{4}{3} C_{MOS} V_{in}^2$ corresponds to two times the energy stored in the nonlinear drain-to-source capacitor, whose capacitance is inversely proportional to the square root of the voltage.

In order to ensure that Q4 will turn on with zero voltage, a dead time is needed between the turn-off of Q2 and turn-on of Q4 to ensure that D4 conducts prior to turn on of Q4. Knowing the elements that are involved in the process, the dead time required to ensure the maximum possible load range with ZVS can be determined. The resonance between L_{lk}, C_{MOS} and C_{TR} provides a sinusoidal voltage across the capacitances that reaches a maximum at one fourth of the resonant period,

$$\delta\tau_{\max} = \frac{T}{4} = \frac{\pi}{2} \sqrt{L_{lk} C} \qquad (2)$$

where $C = C_{MOS} + C_{TR}$.

The dead time between Q2 and Q4 is set at $\delta\tau_{\max}$ to ensure that

all the energy stored in L_{lk} is available to charge/discharge the capacitances.

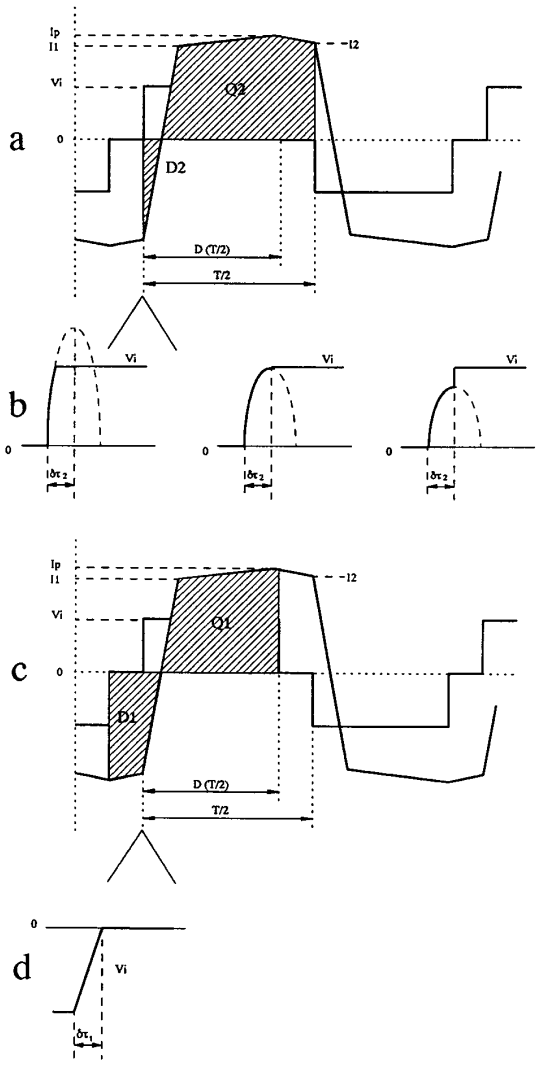

Fig. 2. : a) Voltage and current in D2 and Q2, b) Detail of the rising edge of the voltage c) Voltage and current in D1 and Q1, d) Detail of the rising edge of the voltage.

Figure 2b presents detail of the voltage across Q4 at turn-off (time t_2) for three different values of load current. The first voltage waveform corresponds to the case when the energy in L_{lk} is larger than the energy required to charge/discharge the capacitors. The switch output capacitances are charged/discharged in less than $\delta\tau_{max}$, and the voltage is clamped to the input voltage. The second voltage waveform corresponds to the limit case when the energy in L_{lk} is equal to the energy required to charge the capacitances. The last waveform corresponds to the case when the energy in L_{lk} is not sufficient to charge/discharge the output capacitances, and ZVS is lost. After $\delta\tau_{max}$, Q4 (or Q2) is turned on and the voltage V_{AB} increases sharply to V_{in}.

The ZVS for Q2 and Q4 is dependent on the load of the converter, and for light loads, the current through L_{lk} at t_2 (or t_6) may not be sufficient to charge/discharge the output capacitance of the FETs and to turn on the antiparallel diode (D2 or D4).

For switches Q1 and Q3, ZVS is provided by a different process. Before Q1 is turned off, the current in the primary is reaching its peak value (Fig. 2c). The primary current is the reflected filter inductor current. When Q1 is turned off the energy available to charge the output capacitance of Q1 and discharge the output capacitance of Q3 is the energy stored in L_{lk} plus the energy in the output filter inductor. The latter is available because the filter inductor current does not yet freewheel through the rectifier until the voltage across the secondary has fallen to zero. Since the energy in the filter inductor is large compared to that required to charge/discharge the capacitances in the primary, the capacitances of the switches can be considered charged approximately at a linear rate with a constant current (Fig. 2d).

The value of the dead time, $\delta\tau_1$, required between Q1 and Q3, can be determined from the equation

$$4C_{MOS}V_{in} + C_{TR}V_{in} = I_p\,\delta\tau_1 \tag{3}$$

where the term $4C_{MOS}V_{in}$, corresponds to twice the charge stored in the nonlinear drain-to-source capacitance of the MOSFET.

The dead time can be calculated with the peak value of the primary current, I_p, that corresponds to the peak value of the current ripple in the output filter inductor reflected to the primary.

2.2.2 Zero Voltage Switching Range

The ZVS for Q1 and Q3 can be achieved even at light loads because D1 and D3 can always be turned on by the reflected current of the output filter inductance. However, Q2 and Q4 only achieve ZVS for a load current above a critical value. The critical current required in the primary to achieve ZVS can be calculated from (1)

$$I_{crit} = \sqrt{\frac{2}{L_{lk}}\left(\frac{4}{3}C_{MOS}\,V_{in}^2 + \frac{1}{2}C_{TR}\,V_{in}^2\right)} \tag{4}$$

The available current through L_{lk},at t_2, can be calculated as,

$$I_2 = \frac{N_s}{N_p}\left(I_{load} + \frac{\Delta I}{2} - \frac{V_{out}}{L_f}(1-D)\frac{T}{2}\right) \tag{5}$$

where L_f is the filter inductance, V_{out} is the output voltage, D is the duty cycle in the primary, T is the switching period, I_{load} is the average output filter current, ΔI is the output filter inductor current ripple, and

N_p and N_s correspond to the number of turns in the primary and secondary of the transformer, respectively.

Finally, ZVS is achieved for values of load current such that

$$I_2 > Icrit \tag{6}$$

or

$$I_{load} > \frac{N_p}{N_s} \; I_{crit} - \frac{\Delta I}{2} + \frac{V_{out}}{L_f}(1-D)\frac{T}{2} \tag{7}$$

When the load current reflected to the primary is lower than the magnetizing current, the magnetizing inductance becomes part of the ZVS process. For such light loads the energy available to charge/discharge the output capacitances of the switches Q2 and Q4 at times t_2 and t_6, respectively, is the energy stored in the leakage inductance, plus the energy stored in the magnetizing inductance of the transformer. This is because the magnetizing current can not circulate through the secondary of the transformer during intervals $t_1 - t_2$ and $t_5 - t_6$, due to the low output inductor filter currents freewheeling through the rectifier. The use of the magnetizing current has been fully described in reference [9].

2.2.3 Choice of Switching Frequency, Leakage Inductance and Duty Cycle.

ZVS is achieved over a greater load range with larger values of L_{lk} . However, the finite slope in the rising and falling edges of the primary current reduces the duty cycle available in the secondary. For a desired dc-to-dc transformation, L_{lk} has to be selected together with the frequency of operation and transformer turns ratio.

The voltage gain of the ZVS-PWM converter can be expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{N_s}{N_p} \; D_{eff} \tag{8}$$

where D_{eff} is the duty cycle of the secondary voltage.

The primary duty cycle, that is set by the control of the circuit, can be expressed as:

$$D = D_{eff} + \Delta D \tag{9}$$

where ΔD is the loss of duty cycle due to the finite slope of the rising and falling edges of the primary current. Looking at Fig.3 ΔD can be expressed as:

$$\Delta D = \frac{I_1 + I_2}{\frac{V_{in}}{L_{lk}} \; \frac{T}{2}} \tag{10}$$

$$\Delta D = \frac{\frac{N_s}{N_p}}{\frac{V_{in}}{L_{lk}} \; \frac{T}{2}} \left(2I_{load} - \frac{V_{out}}{L_f}(1-D)\frac{T}{2} \right) \tag{11}$$

Putting Eq.(11) into (9) and using Eq.(8), the following expression is obtained:

$$D = \frac{1 + \frac{4L_{lk}f_s}{R'} - \frac{L_{lk}}{L'_f}}{\frac{1}{D_{eff}} - \frac{L_{lk}}{L'_f}} \tag{12}$$

where $R' = R_{load}(N_p/N_s)^2$ and $L_f' = L_f(N_p/N_s)^2$ are the load resistance and filter inductor reflected to the primary.

When the term containing $(1 - D)$ in Eq. (11) is small compared to $2I_{load}$, the Eq.(12) can be simplified to:

$$D = D_{eff}\left(1 + 4\frac{L_{lk}}{R'} f_s\right) \tag{13}$$

For a given power, input-output voltage ratio,and maximum duty cycle, the transformer turns ratio, switching frequency and leakage inductance have to be chosen to satisfy:

$$1 \geq D_{\max} \geq \frac{N_p}{N_s} \; \frac{V_{out}}{V_{in}} \left(1 + 4 \; \frac{L_{lk}}{R'} f_s\right) \tag{14}$$

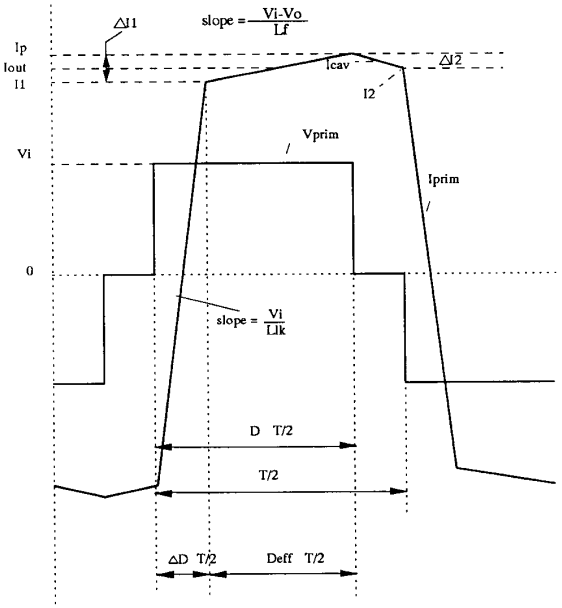

Fig. 3. : Definition of variables of the waveforms.

2.2.4 Loss Analysis

The ZVS-PWM converter provides ZVS for the devices, but it has larger rms currents in the primary than the conventional full bridge PWM converter. It is of primary interest to quantify the conduction losses and compare them with those of the conventional PWM counterpart.

The conduction losses due to channel resistance of the switches can be calculated as:

$$P_Q = R_{on}\ I_{rms}^2 \tag{15}$$

where R_{on} is the channel resistance of the switch and I_{rms} is the rms value of the current through the switch. The conduction losses for the switches are:

• Q2 or Q4

$$P_{Q_{2,4}} = R_{on}\cdot\left[\left(\frac{I_1}{\sqrt{3}}\right)^2\ \frac{\Delta D}{2} + \left(I_{out}^2 + \frac{\Delta I_1^{\ 2}}{3}\right) D_{eff} + \left(I_{cav}^2 + \frac{\Delta I_2^{\ 2}}{3}\right)(1-D)\right] \tag{16}$$

• Q1 or Q3

$$P_{Q_{1,3}} = R_{on}\cdot\left[\left(\frac{I_1}{\sqrt{3}}\right)^2\ \frac{\Delta D}{2} + \left(I_{out}^2 + \frac{\Delta I_1^{\ 2}}{3}\right) D_{eff}\right] \tag{17}$$

where the first and second terms inside the brackets correspond to the rms currents during intervals $t_3 - t_4$ and $t_4 - t_5$, respectively. The third term for losses in Q2 and Q4 corresponds to the rms current during the time the primary voltage (V_{AB}) is clamped to zero, interval $t_1 - t_2$ ($t_5 - t_6$). All the rest of the variables used are defined in Fig. 3.

Since the conventional PWM converter is always designed to minimize the leakage of the transformer, $\Delta D \simeq 0$. There is also no conduction during the interval $t_1 - t_2$ ($t_5 - t_6$).

The conduction losses on the primary bridge diodes are:

$$P_D = V_{diode}\, I_{av} \tag{18}$$

where V_{diode} is the forward voltage drop on the diodes, and I_{av} is the average current through the diodes. The conduction loss of the diodes can be written as:

• D2 or D4

$$P_{D_{2,4}} = \left(\frac{I_2}{2}\right) V_{diode}\ \frac{\Delta D}{2} \tag{19}$$

• D1 or D3

$$P_{D_{1,3}} = V_{diode}\left[I_{out}\ (1-D) + \frac{I_2}{2}\frac{\Delta D}{2}\right] \tag{20}$$

these losses are negligible in a conventional full-bridge PWM converter.

The conduction losses in the rectifier are the same for conventional PWM and ZVS-PWM.

•Rectifier

$$P_{rect} = 4\left(\frac{I_{out}}{2}\ V_f\right) \tag{21}$$

where V_f is the forward drop for the rectifier diodes, assuming that a full-bridge rectifier is used.

From the loss expressions, it can be deduced that the ZVS-PWM converter has larger conduction losses than the conventional PWM bridge, particularly when using small duty cycle and large L_{lk} which imply large $(1-D)$ and large ΔD, respectively. The main advantage in terms of efficiency for the ZVS-PWM is provided by the reduced switching losses and the elimination of the need for snubber circuits across the bridge switches. This reduction of switching losses permits efficient operation at higher frequencies and reduces stress in the devices.

The use of snubber circuits across the output rectifier, common to both conventional PWM and ZVS-PWM, adds additional losses. The losses for the rectifier snubber are dependent on the available devices, and are discussed in detail in Section 3.

2.3 Small Signal Model

The ZVS-PWM converter is a buck-derived topology. However, it can be seen from the description of operation that the duty cycle of the secondary voltage, D_{eff}, depends not only on the duty cycle of the primary voltage, D, (determined by the control), but also on the load current (I_L), leakage inductance (L_{lk}), input voltage (V_{in}), and switching frequency (f_s). This can be concluded by examining Eq. (12), and observing the relation $D_{eff} = D - \Delta D$. The small-signal transfer function of this converter, therefore, will depend on L_{lk}, f_s, and the perturbations of the filter inductor current ($\hat{i}_L$), input voltage ($\hat{v}_{in}$), and duty cycle of the primary voltage ($\hat{d}$).

To accurately model the dynamic behavior of this converter, it should be found how L_{lk}, f_s, $\hat{i}_L$, $\hat{v}_{in}$, and $\hat{d}$ contribute to the perturbation of d_{eff} ($\hat{d}_{eff}$). Knowing that, it is possible to incorporate the effects from this circuit into the small-signal circuit model of the PWM buck converter (Fig. 4) to obtain a new small-signal model of the ZVS-PWM converter.

It is shown [8] that the total change of duty cycle of the secondary voltage is:

$$\hat{d}_{eff} = \left(1 - \left(\frac{N_s}{N_p}\right)^2 D'_{eff}\ \frac{L_{lk}}{L}\right)\hat{d} - \frac{N_s}{N_p}\frac{4L_{lk}f_s}{V_{in}}\hat{i}_L + \\ + \frac{N_s}{N_p}\frac{4L_{lk}f_s}{V_{in}^2}\hat{v}_{in} \\ \triangleq K_L\hat{d} + \hat{d}_i + \hat{d}_v \qquad (22)$$

The first term represents a change in secondary duty cycle due to the change in the primary duty cycle. The second term in the Eq. (22) represents a change of d_{eff} due to the change of the filter inductor current. This term is negative and acts as a current feedback. The third term represents the change of d_{eff} due to the change in the input voltage. This term introduces the effect of the feedforward of input voltage.

When we replace $\hat{d}$ in the conventional PWM buck converter model (Fig. 4) with $\hat{d}_{eff}$, we obtain the small-signal model of the ZVS-PWM converter (Fig. 5). Figure 6 shows a prediction (dashed lines), and measurement (solid lines) of the control-to-output transfer function obtained using the model of Fig. 5.

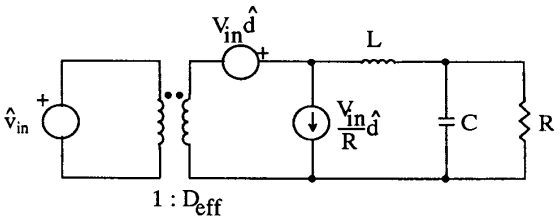

Fig. 4. : Small-signal model of the PWM buck converter.

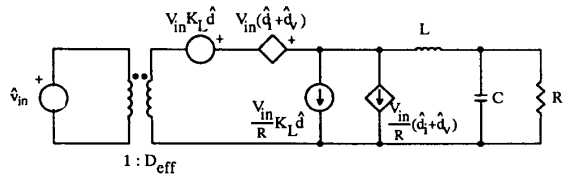

Fig. 5. : Small-signal model of the ZVS-PWM converter.

3 IMPLEMENTATION AND DESIGN GUIDELINES

3.1 Specific Considerations

The high voltage and power level of the converter require special attention to parasitics that can affect the operation.

The primary leakage inductance and output capacitance of the devices are used to achieve ZVS, as has been described in Section 2.

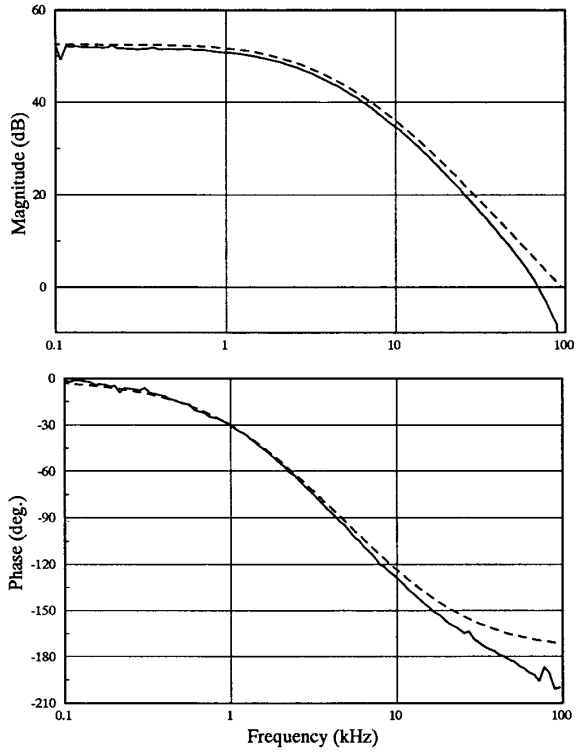

Fig. 6. : Control-to-output transfer function, measurement (solid lines), and prediction (dashed lines).

The transformer design does not need to be optimized to reduce the leakage inductance as would be the case for a conventional PWM converter. However, the parasitic capacitance of the windings has an adverse effect: it needs to be discharged at the same time as the output capacitances of the power FETs are charged/discharged. This increases the total energy required to be stored in the leakage inductance to ensure ZVS, as is presented in Eq.(4), resulting in a larger critical current required to achieve ZVS (Eq. 5). To reduce this effect, the transformer should be designed to minimize the winding parasitic capacitances.

The ringing across the rectifier is affected by the leakage inductance of the transformer, the winding capacitance and the rectifier diode characteristics. This ringing across the rectifier occurs when the voltage rises in the secondary of the transformer. In a full-bridge rectifier, when voltage is applied to the secondary, two of the rectifier diodes are reverse biased, and the leakage of the transformer rings with the diode capacitance and winding capacitances. Even though fast recovery rectifiers are employed in this application, the diode reverse recovery can produce peak voltages higher than three times the voltage applied to the secondary.

The ringing has to be snubbed, but the use of an RC snubber in parallel with the rectifier would introduce large losses since the ringing

frequency is less than 10 times the switching frequency, due to the large values of L_{lk}. This frequency is,

$$f_{rng} = \frac{1}{2\pi\sqrt{\left(\frac{N_s}{N_p}\right)^2 L_{lk} C}} \tag{23}$$

where C is the equivalent capacitance of the rectifying diodes and the transformer windings.

A scheme has been proposed [7] that clamps the maximum peak voltage of the ringing and returns part of the energy to the output. Figure 7a presents the clamping circuit used.

The design of the clamping circuit is based on balancing the charge that is transferred to the clamping capacitor, C_c, with the charge returned to the load in order to keep the voltage across C_c constant [7]. Figure 7b presents a simulation of the voltage across the rectifier and the primary current after adding the clamping circuit.

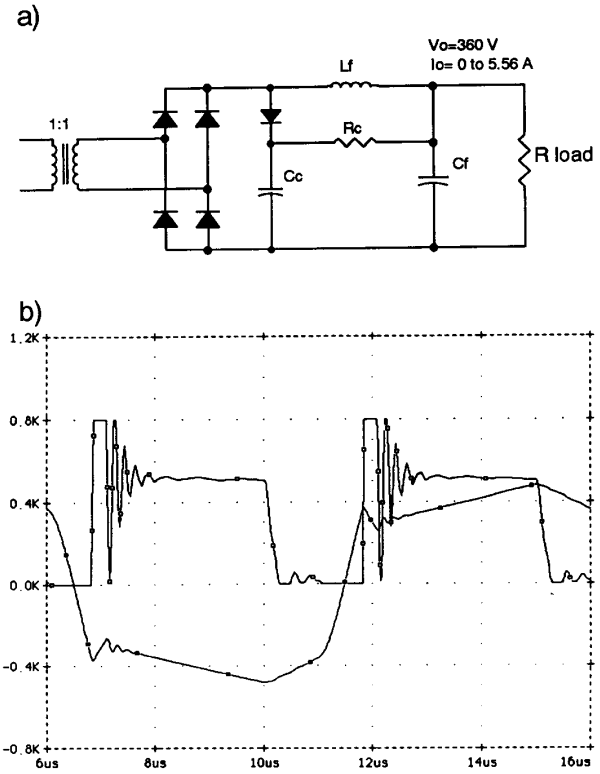

Fig. 7. : a)Clamping circuit, b) Simulated rectifier voltage with the clamping circuit.

3.2 Design Guidelines

The equations presented in Section 3 are used to design the power stage. This section outlines the design procedure for the ZVS-PWM. In the next section this procedure is used to design a prototype hardware.

Specifications needed to start the design are: V_{in}, V_{out},and $I_{load\,max}$. The design procedure can be performed in the following steps.

1. Choose D_{max}. D_{max} should be chosen as large as possible. This allows to maximize $\frac{N_p}{N_s}$ and subsequently reduce the conduction losses in the primary (Eq. 20). D_{max} is, however, limited by the time available for resetting the current-sensing transformer and by the duty cycle range allowed by the PWM controller.

2. Choose V_{sec}. V_{sec} should be chosen as low as possible to reduce the voltage stress of the rectifiers, and to maximize $\frac{N_p}{N_s}$. However, reducing V_{sec}, i.e. increasing (N_p/N_s) reduces the primary current and consequently increases the value of the L_{lk} required for achieving a desired ZVS range. For this reason the initial choice of V_{sec} is somewhat arbitrary, and the final value is obtained after several iterations through steps 2 to 5.

V_{sec} has to satisfy:

$$V_{sec} \geq \frac{V_{out}}{D_{max}} \tag{24}$$

$$\frac{N_p}{N_s} = \frac{V_{in}}{V_{sec}} \tag{25}$$

The initial choice of V_{sec} should be somewhat higher than V_{out}/D_{max}. Once V_{sec} is chosen it is straightforward to calculate (N_p/N_s), D_{eff} (Eq. 8) and ΔD (Eq. 9).

3. Chose the ZVS range. Calculate I_{crit} from Eq.(7).For this calculation it is necessary to choose the value of the output inductor current ripple, ΔI_L. Since D is not known at partial loads, it is not possible to calculate I_{crit} exactly. In the first iteration of the design it is reasonable to make the average output inductor filter reflected to the primary equal to the value of I_{crit}.

After the first iteration is completed, the values required for the exact calculation can be determined and used as initial data for the next iteration.

4. Calculate L_{lk} from Eq.(4). To perform this calculation it is necessary to choose the devices for the bridge and estimate the parasitic capacitance of the transformer.

5. Calculate the switching frequency from Eq.(11) or (12).

After completing these steps the initial design is obtained. This design, however, may not be unsatisfactory from the point of view of

circuit realization. The following cases may occur:

- Switching frequency too low (high): In this case it is possible to go to step 4 and reduce (increase) the ZVS range or to return to step 2 and increase (decrease) V_{sec}.
- L_{lk} too high (low): In this case it is possible to go to step 4 and reduce (increase) the ZVS range or to return to step 2 and increase (decrease) V_{sec}.

3.3 Power Stage Design

The converter built has the following specifications:

- Input voltage, $V_{in} = 600\ V$
- Output voltage, $V_{out} = 360\ V$
- Output power, $P_{out} = 2\ kW$ ($I_{out} = 5.56\ A$)

and the following were chosen

- Maximum duty cycle, $D_{max} = 0.8$
- Secondary voltage, $V_{sec} = 600\ V$
- Output inductor current ripple, $\Delta I_L = 2.3\ A$

The ZVS range is chosen to be from full load to 50% load, this implies a minimum load current for ZVS of 2.78 A. Using Eq.(7), the initial guess for I_{crit} is $I_{crit} = 2.78A$

Choosing the devices with $C_{MOS} = 82\ pF$, and estimating the transformer capacitance to be $C_{TR} = 100\ pF$, the Eq. (4) gives $L_{lk} = 14.8\ \mu H$.

Eq. (12) gives the switching frequency of 368.5 kHz.

At this point the value of the filter inductor required for the desired current ripple is $105\ \mu H$.

Using the results of the first iteration, $D = 0.67$ is obtained for the operation at the ZVS limit.

Recalculating all the steps with the values obtained for D, the next set of values obtained is:

$$I_{crit} = 2.1\ A\ ,\ L_{lk} = 26\ \mu H\ ,\ f_s = 212\ kHz$$

After going through the design steps several more times, the following results were obtained:

$$L_{lk} = 52\ \mu H\ ,\ f_s = 100\ kHz$$

The transformer turns ratio is set at 1:1, and using a core EE-55/55/21 of H7C4 material from TDK with $N_p = N_s = 26$ turns.

The the duty cycle required in the primary is $D = 0.79$, which is below the specified limit. The filter inductor is $L_f = 314\ \mu H$, which gives a current ripple $\Delta I = 2.3\ A$.

Fast-recovery rectifying diodes were used to minimize the ringing across the rectifier.

The clamp circuit was designed (7) to clamp the ringing voltage to a maximum voltage $V_c = 850\ V$. The values required are $R_c = 20\ k\Omega$ and $C_c = 30\ nF$. The losses associated with the clamp circuit are

$$P_{loss} = \frac{(V_c - V_{out})^2}{R_c} = 12\ W \qquad (25)$$

which is below 1% of the converter power.

The ZVS range can be calculated using Eq. (7): The minimum current to have ZVS is $I_{crit} = 1.49\ A$, for $C_{TR} = 100\ pF$ and $C_{MOS} = 82\ pF$, and the corresponding load current is 2.67 A, so ZVS is lost for loads below 48% of full load.

Fig. 8 is the circuit schematic of the power stage, specifying the components used in the prototype.

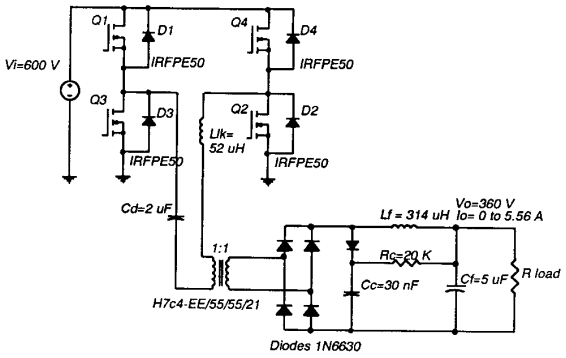

Fig. 8. : Experimental circuit.

4 EXPERIMENTAL RESULTS

4.1 Circuit Operation Waveforms

Based on the design given in Section 3.3 a breadboard has been implemented.

Figure 9 shows current and voltage in the primary (top waveforms), and the voltage across the secondary for full-load operation. The absence of ringing in the voltage waveform implies ZVS. The secondary voltage ringing is clamped to 850 V (close to the predicted value). The ringing frequency is approximately 2.3 MHz. This low ringing frequency would produce large losses in a RC snubber.

When the load current is decreased below 2.7 A, ZVS is lost as predicted by the analysis. Figure 10 shows the waveforms for a load

current of 2.1 A (top waveforms) and the detail of the rising edge. The voltage in the primary increases sinusoidally until L_{lk} has been fully discharged, then the switch is turned on with 200 V across it.

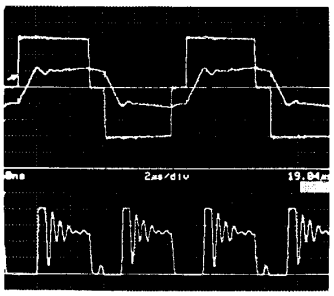

Fig. 9. : Voltage and current in the primary (top waveforms) and voltage across the rectifier (lower waveform), full-load operation. (Scales: Voltage:200 V/div., Current:5 A/div., Time:2 μsec/div.)

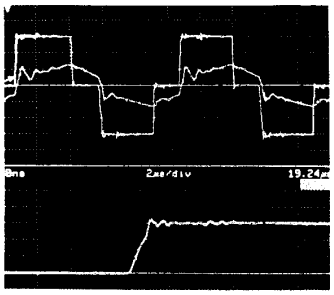

Fig. 10. : a)Voltage and current in the primary (top waveforms) and voltage across the rectifier (lower waveform), for $I_{load} = 2.1$ A,b)detail of the rising edge. (Scales: Voltage:200 V/div., Current:2 A/div., Time:2 μsec/div.)

Figure 11 shows the waveforms corresponding to 5% load. ZVS is lost but the voltage overshoot on the switches is less than 200 V, as can be seen in the primary voltage waveform. The voltage across the rectifiers (bottom waveform) has two ringing frequencies:

- The ringing between L_{lk}, capacitance of diodes and capacitances of the transformer windings, is at 2.3 MHz. This ringing is also present in the waveforms at larger loads.
- The ringing between the output filter inductor and diodes capacitance, is at a frequency of 1 MHz. This is due to the discontinuous conduction mode of operation of the filter inductor current.

4.2 Efficiency measurements

Figure 12 shows the measurements of efficiency vs load. The maximum efficiency achieved was 94.5% at full load. The efficiency remains approximately constant until ZVS is lost and the switching losses start to increase.

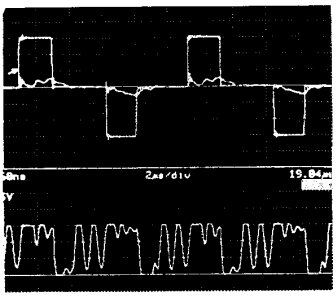

Fig. 11. : Voltage and current in the primary (top waveforms) and voltage across the rectifier (lower waveform), for $I_{load} = 0.3$ A. (Scales: Voltage:200 V/div., Current:2 A/div., Time:2 μsec/div.)

Table I presents the loss breakdown at full-load and at 1.8 A load (after losing ZVS). The equations derived in Section 2.2.4 are used to calculate the conduction losses. The magnetic core losses and the winding resistances are used to calculate transformer and inductor losses. The snubber circuit losses can be calculated based on its design [7]. Finally, switching losses in the rectifier are calculated assuming linear voltage and current transitions during the reverse recovery. The remaining difference with the measured value is assumed to be switching losses in the bridge devices.

The switching losses in the devices at full load are practically zero. ZVS provides no turn-on losses. The fast turn-off of the devices together with the large value of output capacitance also minimize the current and voltage overlap during turn-off. Therefore switching losses are negligible. Even when the ZVS is lost, the total loss associated with each switch is always below the full-load case.

The main source of loss is the voltage drop in the channel resistance of the MOSFETs. This is followed by the magnetics losses. The snubber losses (1% of output power) could be reduced by allowing a larger peak voltage across the rectifiers. However, the selections of de-

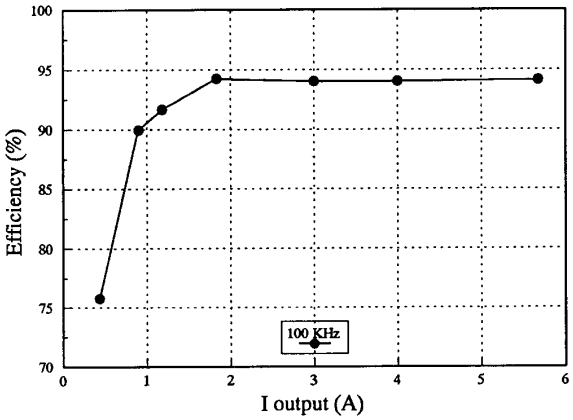

Fig. 12. : Measured efficiency vs. load.

vices with large blocking capability and small reverse recovery times is limited.

Table I: Loss breakdown

switching freq.	100	100	KHz
input voltage	600	600	volts
output voltage	360	360	volts
output current	5.56	1.84	amps
input current	3.52	1.17	amps
input power	2113	702	watts
output power	2000	662	watts
losses	113	40	watts
Q1-Q3 cond.	19.7	3.1	watts
Q2-Q4 cond.	26.6	4.86	watts
D1-D3 cond.	2.7	1.56	watts
D2-D4 cond.	1.1	0.01	watts
transformer	12	5.4	watts
filter induct.	12.6	2.5	watts
rectifier cond.	15	4.75	watts
rectifier sw.	3	0.3	watts
switching	0	5.3	watts
snubber	20	12	watts
efficiency	94.5	94.2	%

5 CONCLUSIONS

The ZVS-PWM converter provides ZVS for the switches by using the leakage inductance of the transformer and the output capacitance of the switches. No extra component is required to realize ZVS.

The steady-state operation of the ZVS-PWM converter has been analyzed to fully characterize its operation and to establish design equations. The magnitude of L_{lk} of the transformer determines the ZVS load range. Since L_{lk} limits the rising and falling times of the primary currents, the available duty cycle in the secondary is reduced. This limits the maximum L_{lk} to be used in a particular design.

An analysis based design procedure is established and verified. A breadboard was fabricated with 600 V input voltage and 360 V output voltage at 2 kW output power. The converter was operated at 200 kHz conversion frequency. The efficiency at full load was 94.5 %. ZVS operation was retained up to 48% load.

Due to ZVS operation the primary side waveforms are free from switching noise and require no snubber. The secondary voltage waveform for a high output voltage (360 V) has a substantial ringing due to the reverse recovery of the diodes. The ringing frequency is usually too close to the switching frequency which makes it difficult to snub the ringing effectively using a RC snubber. An energy recovery snubber network is employed to keep the snubber loss below 1% of the output power.

The conduction losses of the converter are somewhat larger than those of a conventional PWM bridge converter. however, this is compensated by not requiring the use of snubbers across the primary switches.

The prototype designed operates with ZVS from full load to 48% load. The loss of ZVS does not greatly affect the good operation of the converter and the waveforms are free from switching noise, even at light loads.

6 REFERENCES

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