A FULL BRIDGE SOFT SWITCHED TELECOM POWER SUPPLY WITH A CURRENT DOUBLER RECTIFIER

Nasser H. Kutkut

Soft Switching Technologies Corporation
2224 Evergreen Rd. Suite # 6, Middleton, WI 53562 USA
Tel : (608) 836-6552, Fax : (608) 836-6553
E-mail: kutkut@softswitch.com

Abstract— This paper presents a full bridge soft switched PWM TELECOM power supply with a current doubler rectifier. The full bridge PWM dc-to-dc converter offers high power handling capability, minimum VA ratings for the main devices, no additional auxiliary components and simple PWM based control strategy. Phase shift control is employed to regulate the output voltage and achieve soft switching. The transformer leakage inductance is utilized effectively to achieve zero voltage turn on for the main devices. The current doubler rectifier has only one diode conduction drop in addition to frequency doubling in the output capacitor. The transformer secondary winding current rating is one half the load current which improves the overall efficiency of the converter.

I. INTRODUCTION

Most of the DC/DC converters in use today are derived from the three basic single quadrant topologies: buck, boost and buck-boost converters. At high power levels, the full-bridge (buck-derived) DC/DC converter with isolation on the intermediate high frequency ac link is the preferred topology. The main advantages of this topology include constant frequency operation which allows optimum design of the magnetic filter components, PWM control, minimum VA stresses and good control range and controllability. However, the increase in device switching losses as the frequency increases in and the high voltage stress induced by the parasitic inductances following diode reverse recovery are major drawbacks of this topology.

Various soft switching schemes (ZVS and ZCS) have been proposed to improve the performance of hard switching converters. One topology which achieves PWM control with resonant transitions is the full-bridge ZVS PWM converter [1-5]. In this topology, the transformer leakage and magnetizing inductances in addition to the MOSFET's output capacitances are effectively utilized to achieve ZVS. The load range can be extended by properly sizing the leakage inductance of the transformer. This topology has received a great deal of attention and has been widely adopted for high power applications.

In low voltage high current applications (e.g. TELECOM power supplies), the converter efficiency is limited by the losses on the high current side. A full bridge diode rectifier has two diode drops in the current path and the transformer secondary is rated for the full load current. On the other hand, a center tapped arrangement offers one diode drop in the current path with two transformer secondary windings, each is rated for 71% load current.

II. THE FULL BRIDGE DC/DC CONVERTER WITH A CURRENT DOUBLER

A further improvement in the converter efficiency can be realized by utilizing the current doubler rectifier [6,7]. In this case, only one diode drop exists in the current path. In addition, the transformer secondary winding is rated for one half the load current with no center tapped connection required. Although two output filter inductors are required, their current rating is only one half the load current. Due to the current doubler effect, the size of the output filter inductors is rather small and they can be integrated on a single core. Figure 1 shows a proposed full bridge PWM converter with a current doubler rectifier suitable for high current and low voltage applications. Due to the reduced current ratings of the secondary side transformer winding and filter components, the converter efficiency and cooling is improved.

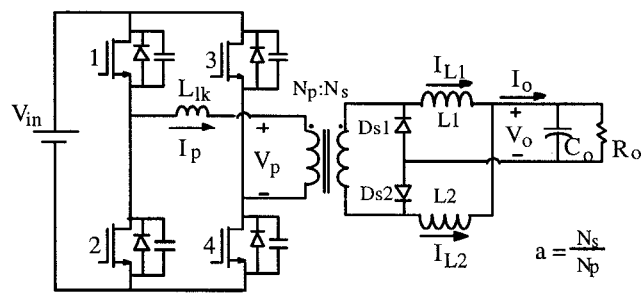

Fig. 1: The dual bridge DC-to-DC converter

The converter is operated in a mode which provides zero voltage turn-on for the main devices. This can be achieved by introducing a phase shift between the switches in the right leg (leading leg) and those in the left leg (lagging leg). In addition, the phase shift will determine the duty cycle of the converter. The typical current and voltage waveforms of the converter under continuous output current are shown in Fig. 2 while the discontinuous operation is shown in Fig. 3. It is interesting to note that with discontinuous output

0-7803-3996-7/97/$10.00©1997 IEEE

current, the output filter currents are non zero. This maintains current flow on the inverter side and extends the ZVS range to light loads.

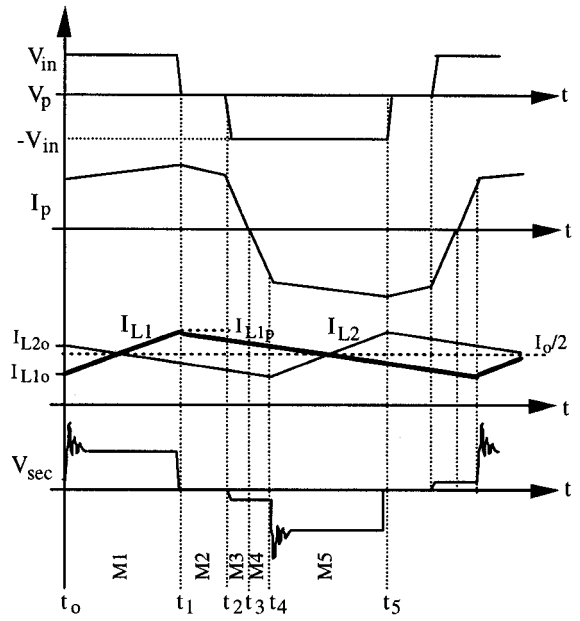

Fig. 2: Typical waveforms of the converter under continuous output current

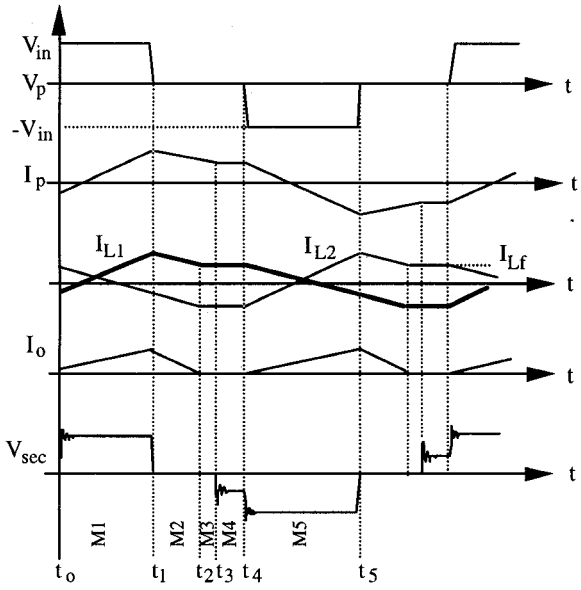

Fig. 3: Typical waveforms under discontinuous output current

III. CONVERTER OPERATION

The converter is operated in a mode that provides zero voltage turn-on for the main devices. This is made possible by introducing a phase shift between the switches in the leading (right) legs and those in the lagging (left) legs of both bridges. The phase shift sets the duty cycle of the converter and hence the output voltage.

Similar to the FB-ZVS PWM converter [2], the transformer leakage and magnetizing inductances, and the device output capacitances are utilized to achieve zero voltage switching for the main devices. Zero voltage commutation of leading leg switches uses the energy stored in the output filter inductors, while the lagging leg switches uses the energy stored in both the leakage and magnetizing inductances of the transformer.

The converter has four operating modes within half a switching cycle. The current and voltage waveforms during each of the modes are shown in Fig. 2 for continuous output current and in Fig. 3 for discontinuous output current. The equivalent topological modes are shown in Fig. 4. The devices in each leg of the converter, Q1 & Q2 in the lagging leg and Q3 & Q4 in the leading leg, are turned on and off alternately with nearly 50% duty cycle ratio such that there is a phase shift between the two inverter legs.

A) Continuous Output Current

Under continuous output current operation, four modes are identified during half a cycle. These modes are described below.

Mode 1: $t_o \le t \le t_1$

With Q1 and Q4 initially conducting, the primary voltage is $V_{p1}=+V_{in}$. with diode Ds1 off while diode Ds2 conducting. The current I_{L1} will ramp up linearly while I_{L2} will ramp down linearly. The charging and discharging rates of the output filter currents are given by,

$$I_{L1}(t) = I_{L1o} + \frac{aV_{in} - V_o}{L_1} t \qquad (1)$$

$$I_{L2}(t) = I_{L2o} - \frac{V_o}{L_2} t \qquad (2)$$

where a is the primary to secondary turns ratio. Since Ds1 is off, the primary current will also ramp up with the same rate as I_{L1}. During this mode, power is delivered to the load. The equivalent circuit during this mode is shown in Fig. 4a while the voltage and current waveforms of the converter are shown in Fig. 2 (M1).

Mode 2: $t_1 \le t \le t_2$

When transistor Q4 is turned off at t_1, the energy stored in the output filter inductor L1 charges the output capacitance of Q4 and discharges the output capacitance of Q3 causing the anti-parallel diode of Q3 to conduct. At this point, the load current free wheels through the rectifier diodes Ds1 and Ds2. The equivalent circuit during this the transition from mode 1 to mode 2 is shown in Fig. 4b.

The output filter energy is available since the output current does not free wheel in the secondary diodes until the voltage on both primary windings has fallen to zero. Once the anti-parallel diode of Q3 conducts, transistor Q3 can be turned on under ZVS. Since the energy available for achieving ZVS for the leading leg is the output filter energy, ZVS is possible over a wide load range.

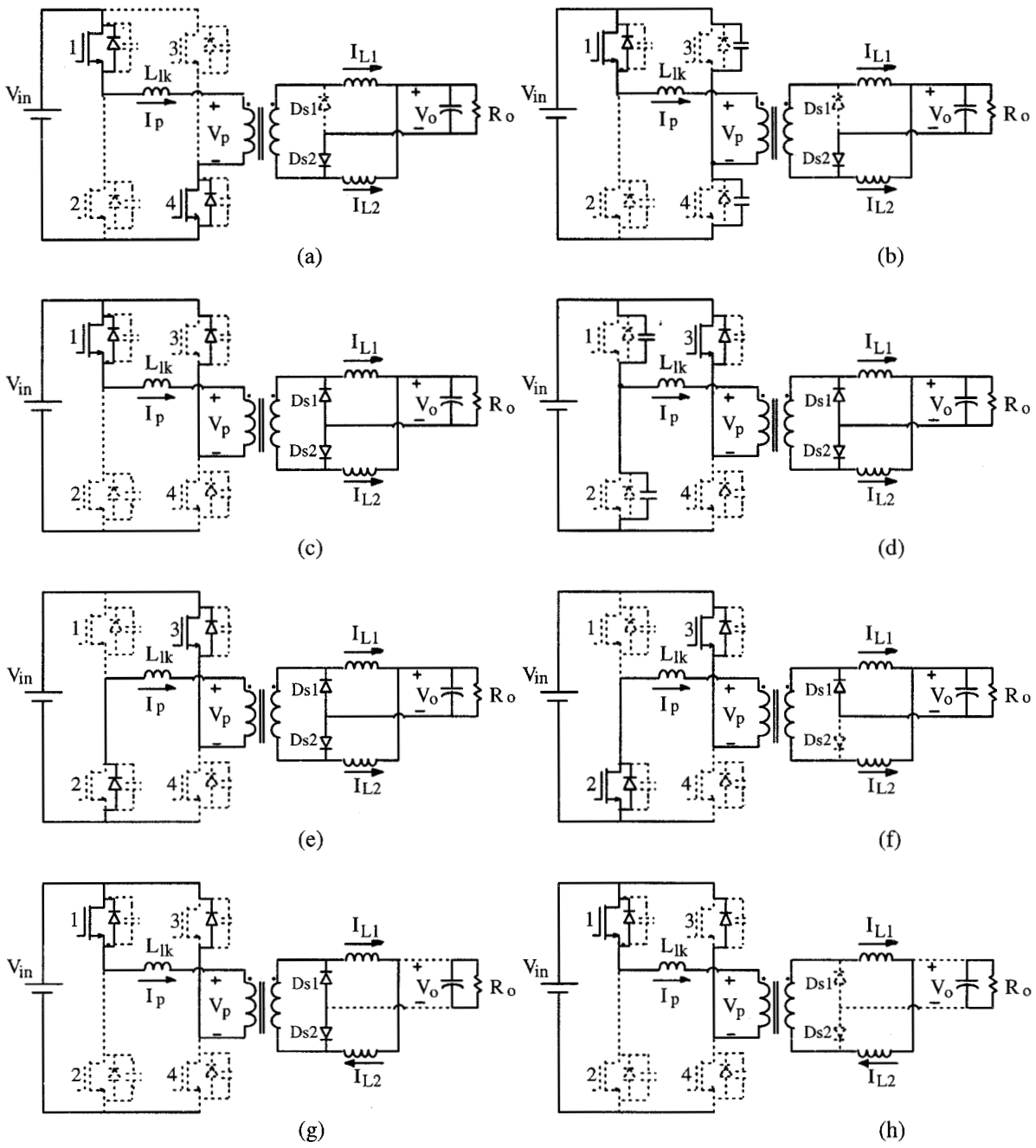

Fig. 4: Equivalent circuit modes of the converter

To insure the anti-parallel diode conducts prior to the turn on of Q3, a dead time is required between the turn-off of Q4 and the turn-on of Q3. The value of this dead time, Δt_d can be computed as,

$$a \cdot I_{L1}(t_1) \cdot \Delta t_d = 4 \cdot C_{eff} V_{in} \qquad (3)$$

where C_{eff} is the effective collector to emitter capacitance of the MOSFET. Note that the factor of 4 in (3) reflects the presence of four devices that are being commutated.

While all secondary diodes are conducting, the transformer voltage is zero and the primary current I_p free wheels through Q1, the anti-parallel diode of Q3 and the shorted primary winding. The equivalent circuit during this mode is shown in Fig. 4c, and the current and voltage waveforms are shown in Fig. 2 (M2). The secondary filter current I_{L1} starts ramping down at a rate given by,

$$I_{L1}(t) = I_{L1p} - \frac{V_o}{L_1} t \qquad (4)$$

Mode 3: $t_2 \le t \le t_3$

When Q1 is turned off at t_2, the energy stored in the leakage and magnetizing inductances charges the output capacitance of Q1 and discharges the output capacitance of Q2 causing the anti-parallel diode of Q2 to conduct. At this point, Q2 can be turned on under ZVS. The equivalent circuit during this mode is shown in Fig. 4d. Since the energy stored in the leakage and magnetizing inductances is less than output filter energy, the soft

switching range is limited. Increasing the leakage inductance or decreasing the magnetizing inductance extends the soft switching range of the converter but adversely affects the effective duty cycle. On the other hand, due to the current doubler filter arrangement, the current ripple in the output filter inductors can be made higher which extends the ZVS range compared with a full bridge or a center tapped arrangement.

With the anti-parallel diode of Q2 conducting, the equivalent circuit during this mode is shown in Fig. 4e, and the voltage and current waveforms during this mode are shown in Fig. 3 (M3). The current transition from anti-parallel diodes to the main devices occurs when I_p crosses zero. Since the main devices have already been turned on, reverse recovery of the main diodes is not an issue.

Mode 4: $t_3 \le t \le t_4$

The cycle is completed when the primary current I_p reaches the reflected secondary filter current I_{L2} at which point diode Ds1 turns off while Ds2 conducts the full load current. The equivalent circuit during this mode is shown in Fig. 4f. The negative half cycle is similar to the positive half cycle.

Under discontiuous ouput current operation, two additional modes are introduced. These modes occur during mode 2 of the continuous output current operation described above.

B) Discontinuous Output Current

Under discontinuous output current operation, four modes are identified during half a cycle. Modes 1 and 2 is similar to the continuous current operation described above. The other two modes are described below.

Mode3a: $t_2 \le t \le t_3$

Due to the light load condition, when the output current reaches zero, the secondary filter currents will be clamped at I_{Lf} while the secondary rectifier diodes carry the difference between the secondary referred primary current and I_{Lf}. The primary current continues to free wheel through the primary side devices and the shorted primary winding. The equivalent circuit during this mode is shown in Fig. 4g while the primary current and voltage waveforms are shown in Fig, 3 (M3).

Mode4a: $t_3 \le t \le t_4$

If the primary current decreases and reaches the reflected secondary filter current I_{Lf}, the secondary diodes Ds1 and Ds2 seize to conduct as shown in Fig. 4h. The voltage and current waveforms during this mode are shown in Fig. 2(M4). Note here that the primary current during the freewheeling mode decreases due to the losses on the inverter side and the driving voltage drops of the main devices.

When Q1 is turned off at t_4, the secondary filter energy due to I_{LF} is used to charge the output capacitance of Q1 and discharge the output capacitance of Q2 causing the anti-parallel diode of Q2 to conduct. Even if the energy is not enough to guarantee a ZVS condition, the turn on losses of the incoming device are minimized due to the reduced turn on voltage. At this point, diode Ds2 starts conducting and the secondary filter current I_{L2} starts ramping up linearly. Note also here that the voltage spike across the secondary winding is reduced due to the fact that the secondary diodes are commutated prior to the turn off of Q1.

Under steady state conditions, the converter output voltage is given by

$$V_o = \frac{a \cdot D_{eff} \cdot V_{in}}{2} \qquad (5)$$

where D_{eff} is the effective duty cycle of the converter. Note here that part of the duty cycle is lost due to the current commutation in Mode 3.

IV. OUTPUT FILTER RATINGS

The proposed dc-to-dc converter topology utilizes a two inductor rectifier to realize reduced ratings of the secondary side transformer winding and filter components. Although two inductive filter components are required, their current rating is only one half the load current. In addition, they can be integrated on a single magnetic core as shown in Fig. 5.

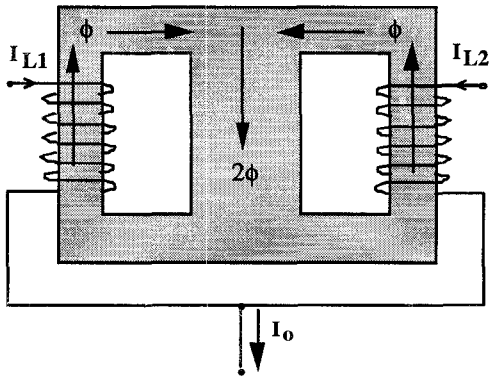

Fig. 5: An integrated two inductor filter design

For the same output current ripple, the size of the output filter inductors is less than that of a full bridge or a center tapped rectifier topology. The inductance value for a given output filter current ripple, ΔI_f, is given by,

$$L_f = \frac{(2-D) \cdot V_o}{2 \cdot f_s \cdot \Delta I_f} \qquad (6)$$

where f_s is the switching frequency. The resultant output current ripple is given by,

$$\Delta I_o = \frac{(1-D) \cdot V_o}{f_s \cdot L_f} \qquad (7)$$

The above two design equations can be used to size the output filter inductors for a given output current ripple. In addition, the ripple ratings of the output filter capacitor can be determined as well.

V. TRANSFORMER DESIGN CONSIDERATIONS

In practice it is desired to fully utilize the transformer leakage inductance to achieve soft

switching without any need for additional inductance. Controlling the leakage inductance of the transformer and limiting the leakage field from penetrating the magnetic core are key design issues especially at high currents.

The use of the co-axial winding transformer (CWT) for high power and high frequency soft switched DC-to-DC converters has been demonstrated in [8,9]. Figure 6 shows a cross sectional view of a co-axial winding transformer suitable for high current applications.

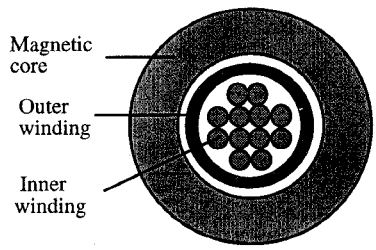

Fig. 6: Cross sectional view of the co-axial winding transformer

The outer tubular conductor forms the high current secondary winding while the inner conductors, which are completely wound inside the outer conductor, form the dual primary windings. The windings are tightly coupled via the high permeability toroidal magnetic cores shown in Fig. 6.

Since the inner winding is totally enclosed by the outer winding, all the flux produced by the outer winding will link the inner one. In addition, the leakage field can only exist in the winding space between the inner and the outer windings. As a result, none of the leakage field finds its way to the core. Consequently, the core needs to be sized to only handle the main flux thus minimizing the core size and weight. The leakage inductance can be controlled by controlling the inter-winding space between the inner winding and the outer tubular winding.

The equivalent circuit of the CWT of Fig. 6 is shown in Fig. 7. Note here that .the leakage inductance is only present on the primary side winding (inner winding) with no leakage on the secondary side winding (outer winding) since all the flux generated by the outer winding links both of the primary windings.

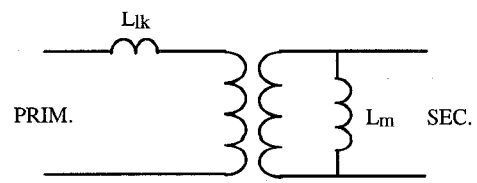

Fig. 7: Equivalent circuit of the co-axial winding transformer

Figure 8 shows a typical CWT with a single turn tubular secondary winding and a multi-turn primary winding. The primary winding can be realized using litz wire to reduce the ac winding losses.

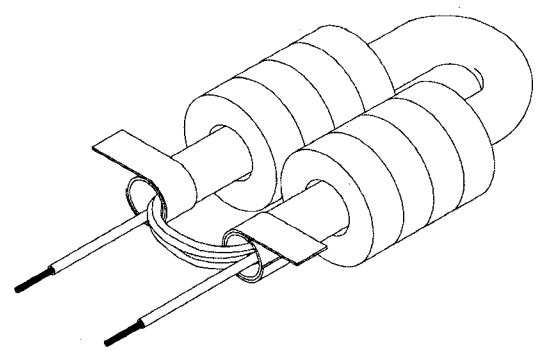

Fig. 8: A CWT with a single turn secondary and multi turn primary windings

VI. CONTROLLER IMPLEMENTATION

In order to ensure equal current sharing between the secondary filter inductor, current mode control techniques are employed. Average current mode control is preferred for accurate control of the average output current and offers higher noise immunity compared with peak current control. This is advantageous in current limited power supplies where the supply current is limited. A dc blocking capacitor is used to ensure flux balancing for the power transformer.

Since the output current is the sum of the two output filter inductor currents, the system can be reduced to two parallel connected buck converters [7,8]. Furthermore, since the output filter inductor currents are not individually regulated, the small signal model of the system can be reduced to that of a single buck converter with average current mode control where the resultant filter inductor is the parallel combination of the two output inductors. Although each inductor current is not separately regulated, any difference between the average currents will be corrected by the input dc blocking capacitor which maintains zero net dc flux within the transformer. This guarantees that the two inductor currents remain equal. Note that the effective switching frequency of the resultant system is twice the switching frequency for the two filter inductor currents are out of phase which results in frequency doubling at the output. Using the PWM switch model and assuming the transformer is ideal, the equivalent small signal model of the converter is shown in Fig. 9 [10]. Here, R_S is the sense resistor, $H_e(s)$ is the sampling gain, F_m is the modulator gain and $G_c(s)$ is the compensation transfer function. The sampling and modulator gains are defined in [11] to be

$$H_e(s) = 1 + \frac{s}{Q_z \omega_n} + \frac{s^2}{\omega_n^2} \tag{8}$$

$$F_m = \frac{1}{S_e + S_n'} \tag{9}$$

where $Q_z = -2/\pi$, $\omega_n = \pi f_s$, S_n' is the positive slope of the inductor current while S_e is the added slope.

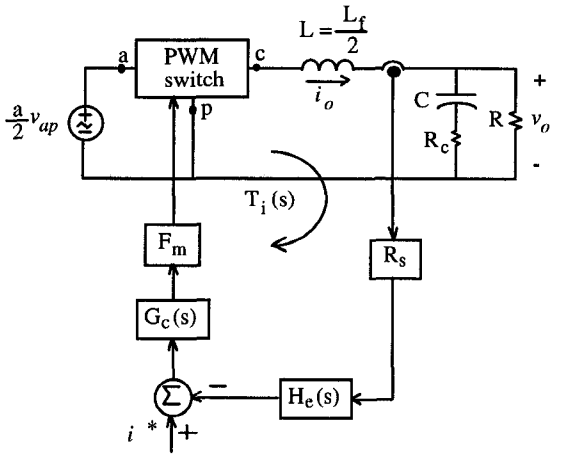

Fig. 9: Small signal model of the converter

An integrator followed by a lead-lag network can be used as a possible compensating network. To ensure stability, the zero should be placed before the power stage filter frequency of the current loop where the phase shift of the integrator is canceled by the zero at half the switching frequency. The pole is normally placed above half the switching frequency to roll off the gain and thereby eliminate high frequency noise. Furthermore, this pole placement minimizes interaction with the current loop.

The control to output current loop transfer function is given by

$$T_i(s) = R_s \cdot H_e(s) \cdot G_c(s) \cdot F_m \cdot F_i(s) \qquad (10)$$

where $F_i(s)$ is the direct (forward) gain transfer function which is given by,

$$F_i(s) = \frac{V_{ap}}{R} \cdot \frac{1 + RCs}{LCs^2 + \left(R_c C + \frac{L}{R}\right) \cdot s + 1} \qquad (11)$$

The loop transfer function for an 5kW converter were computed using MATLAB and the results are shown in Fig. 10 (see section VII).

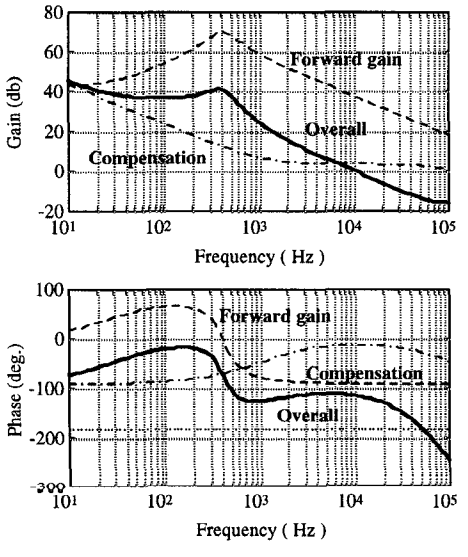

Fig. 10: Loop transfer function with average current control

It is clear from the above figure that the current loop can be stabilized with proper compensator design and without slope compensation. In fact, the compensator gain can be adjusted in a similar fashion to adding slope compensation in peak current mode systems. The gain margin of the current loop is 13.5dB and the phase margin is 67.7° while the current loop bandwidth is 10kHz. The output current step response is shown in Fig. 11. As expected, the output current overshoot is low (5%) and the system reaches steady state in 0.3ms.

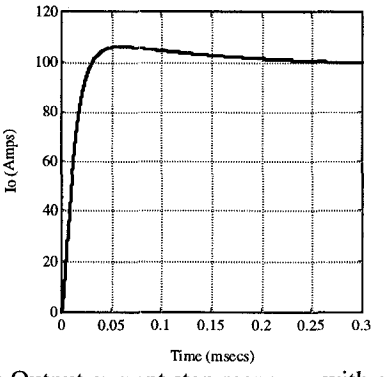

Fig. 11: Output current step response with average current control

VII. EXPERIMENTAL VERIFICATION

The experimental results for a 5kW, 48V/100A rectifier with 300VDC input voltage and 75 kHz switching frequency are shown in Figures 12 through 14. MOSFETs were used as the main switching devices. The primary voltage and current waveforms at full load are shown in Fig. 12. The characteristics of a full bridge PWM ZVS converter are clear in this figure.

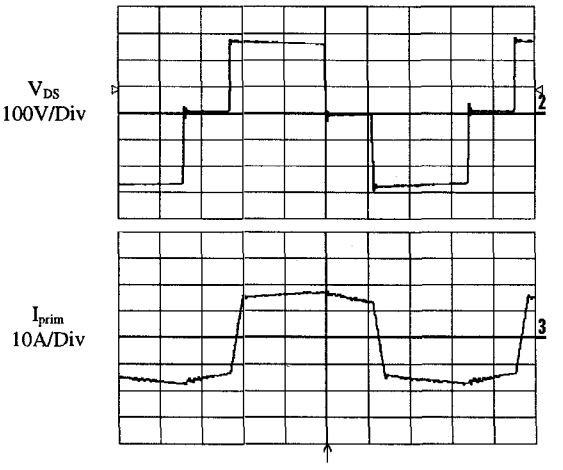

Fig. 12: Primary voltage and current waveforms at 48V/100A

In order to investigate the soft switching characteristics of the converter, the gate and drain to source voltage of the leading and lagging leg MOSFETs are shown in Figs. 13 and 14, respectively.

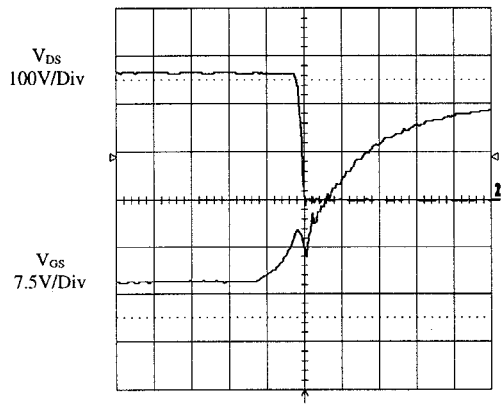

Fig. 13: ZVS of the phase shifted (leading) leg at 48V/100A

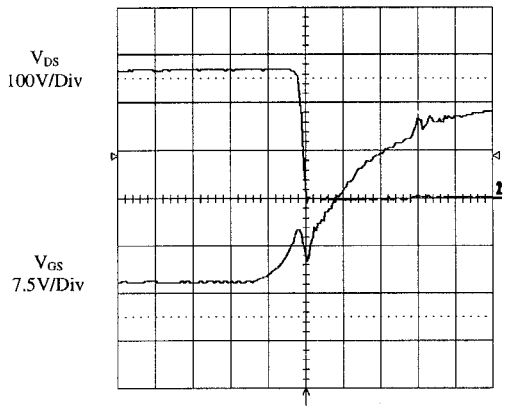

Fig. 14: ZVS of the non phase shifted (lagging) leg at 48V/100A

It is clear from the above figures that ZVS is achieved for the main devices. The drain to source voltage collapses to zero while the gate signal is still negative. As a result, the MOSFETs' anti-parallel diodes conduct prior to main device conduction. For the leading leg devices, the secondary filter energy is used to achieve ZVS. As a result, ZVS can be realized even at light loads. On the other hand, the lagging leg devices utilize the energy stored in the transformer leakage and magnetizing inductances. Hence, ZVS is lost below a certain load condition. This does not highly impact the converter design and performance since the loss of ZVS for the lagging leg devices occurs at light load conditions where the MOSFET's conduction losses are minimal.

The measured converter efficiency under full load conditions was 94%.

VIII. CONCLUSIONS

In summary, the proposed converter topology improves the performance of the full bridge ZVS PWM converter via the use of a current doubler rectifier. Due to the reduced current rating of the transformer secondary winding and output filter components, an improvement in the overall system efficiency results. In addition, the thermal performance of the converter is greatly enhanced. The size of the output filter inductors is less than that of a full bridge or a center tapped rectifier topology for a given output current ripple. The two inductor filter components can be integrated on a single magnetic core which simplifies their design and construction. Detailed analysis of the converter operation in addition to experimental verification data were presented.

ACKNOLEDGMENT

The author would like to thank Steve Norris of Soft Switching Technologies for his help in obtaining the experimental data.

REFERENCES

[1] L. Mweene, C.A. Wright and M.F. Schlecht, "A 1 kW 500 kHz Front-End Converter for a Distributed power Supply System," IEEE APEC Rec., pp. 423-432, 1989.

[2] J.A. Sabate, V. Vlatkovic, R.B. Ridley, F.C. Lee, B.H. Cho, "Design Considerations for High-Voltage High-Power Full-Bridge Zero-Voltage-Switched PWM Converter," IEEE APEC Conf. Rec., pp. 275-284, 1990.

[3] G. Hua, F.C. Lee, M. Jovanovic, "An Improved Zero-Voltage-Switched PWM Converter Using A Saturable Inductor," IEEE PESC Conf. Rec., pp. 189-194, 1991.

[4] J.A. Sabate, V. Vlatkovic, R.B. Ridley, F.C. Lee, "High-Voltage High-Power ZVS Full-Bridge PWM Converter Employing Active Snubbers," IEEE APEC Conf. Rec., pp. 158-163, 1991.

[5] G. Torvetjonn, T. Undeland, O. Schmidt, J. Bryde," A DC-DC Converter Topology with Phase Shift Control Lossless Snubbers for Use in a 200A Battery Charger Working on 400V Bus," IEEE INTELEC Conf. Rec., pp. 489-495, October 1995.

[6] Arthur Cook, Elements of Electrical Engineering, John Wiley and Sons, 1924, pp. 476-478.

[7] N.H. Kutkut, D.M. Divan, R.W. Gascoigne, "An Improved Full Bridge Zero Voltage Switching PWM Converter Using A Two Inductor Rectifier," IEEE Trans. on Industry Applications, Vol. 31, No. 1, pp. 119-126, Jan/Feb 1995.

[8] M.H. Kheraluwala, D.W. Novotny, D.M. Divan, "Design Considerations for High Frequency Transformers," IEEE PESC Conf. Rec., pp. 734-742, 1990.

[9] M.H. Kheraluwala, D.M. Divan, E. Baumann, "Design Considerations for High Power Density DC/DC Converters," HFPC Conf. Rec., pp. 324-335, May 1990.

[10] V. Vorperian, "Simplified Analysis of PWM Converters Using the Model of PWM Switch: Parts I and III," IEEE Trans. on Aerospace and Electronic Systems, vol. 26, No. 3, pp. 490-505, May 1990.

[11] W. Tang, F.C. Lee, R.B. Ridley, "Small-Signal Modeling of Average Current-Mode Control," IEEE Trans. on Power Electronics, vol. 8, No. 2, pp. 112-119, April 1993.

[12] N.H. Kutkut, G. Luckjiff, "Current Mode Control of a Full Bridge DC-to-DC Converter with a Two Inductor Rectifier," IEEE PESC Conf. Rec., pp. 203-209, June 1997.