CMPE 124 Lab 7: 4:1 multiplexer circuits

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***Abstract*—The purpose of this lab project is to implement 4:1 multiplexers with the help of our previously implemented 74LS163 counter.**

I. Introduction

This lab project is based on the implementation of a 74LS163 counter, a logical circuit that tracks time by using 8 bits.
We use this counter's output into two 4:1 multiplexers, one implemented via tri-state buffers, and another one implemented via logic gates.

II. Design Methodology

For this lab project, we use the 74LS163 4-bit counter. This 4-bits counter requires not only a voltage source—to function—and a clock—to provide it with time input—but also a binary switch, to reset it and ensure the wave functions it outputs are correct. Additionally, although we use a resistor, its value can be changed or ignored; our 1kΩ resistor is part of the circuit to demonstrate that we are not focusing on the input voltage, but on the H and L states instead.
Furthermore, create two 4:1 multiplexers, one via tri-state buffers and another one via logic gates and we input the counter's output into both multiplexers. Additionally, we set the select lines to such that they are set to the counter's LSB. Finally, we verify our 4:1 multiplexer circuits' functionality by checking one against each other, the counter's LSB, and the clock, through their waveforms.

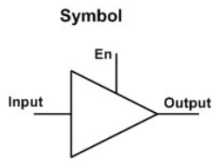
A. Parts List

- Clock
- 5V source
- A 74LS163 counters
- Binary switches
- Resistor
- AND gates
- OR gates
- NOT gates
- Tri-state buffers

B. Truth Tables

State	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
q_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
q_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
q_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
q_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Figure 1. Truth table for a 74LS163 4-bit counter.



En	Input	Output
0	X	Hi-Z
1	0	0
1	1	1

Figure 2. Truth table for a tri-state buffer.

C. Schematics

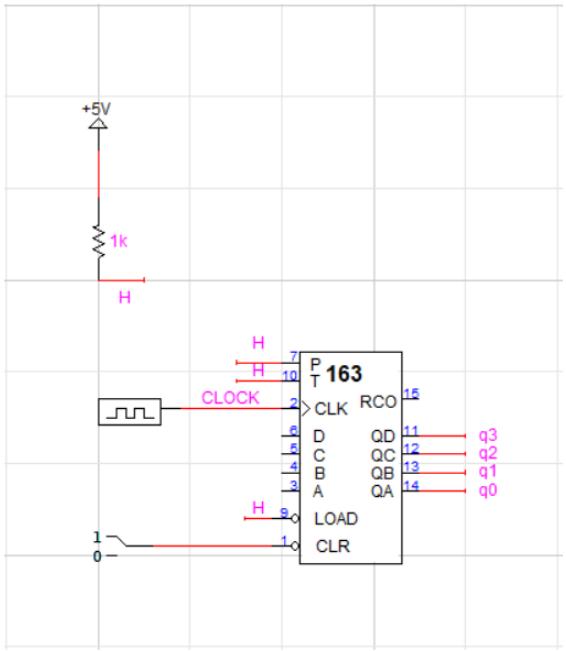


Figure 3. 74LS163 clock-counter circuit scheme.

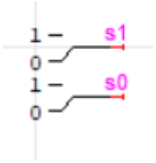


Figure 4. Setting the selection lines to the counter's LSB.

Figure 5. Components of both multiplexers, preprocessing the selection lines' output.

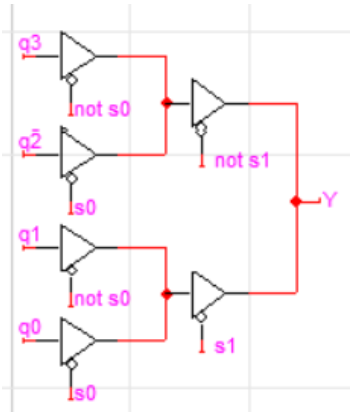


Figure 6. 4:1 multiplexer circuit implemented via tri-state buffers.

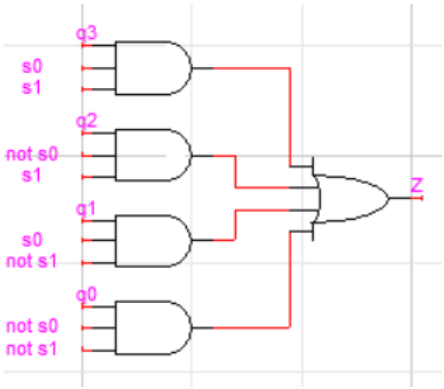


Figure 7. 4:1 multiplexer circuit implemented via logic gates.

III. TESTING PROCEDURES

1. Create a counter as pictured in Figure 3.
2. Set up the binary switches as pictured in Figure 4.
3. Set up the logic gates, tri-state buffers, and their input as pictured in Figures 5, 6, and 7.
4. Reset the counter with a switch and run the simulation.
5. Record both 4:1 multiplexer circuits' waveforms and compare them.

IV. TESTING RESULTS

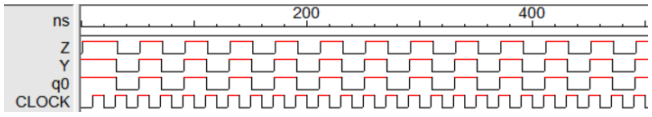


Figure 8. Both multiplexers' output, when the selection lines are set to the counters' LSB, q0.

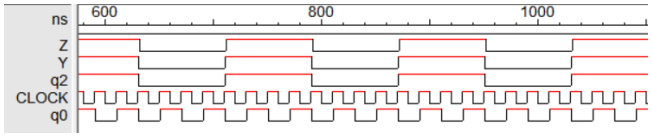


Figure 9. Both multiplexers' output, when the selection lines are set to the counters' second MSB, q2.

V. CONCLUSION

In conclusion both multiplexers—one created via tri-state buffers, and another through logic gates—seem to have been correctly implemented. This is because they have identical waveforms, which not only also match with the counters' LSB, q0, but with the clock's output as well (for every 2 ticks, the counter's LSB will alternate between on and off)—see **Figure 8**. Finally, note that something similar happens if we set the selection lines to the counter's second most significant bit, q2—See **Figure 9**.

Finally, this lab has taught us the basics behind the implementation of multiplexer circuits, which not only tests our theoretical knowledge—obtained in our lectures—but also advances our comprehension of logic circuits and how computers work.