CMPE 124 Lab 3: Counting up to 210 with two 4-bit counters

Leonardo Blas

***Abstract*—The purpose of this lab project is to detect if a theater room has reached max capacity—set at 210—through digital circuits.**

I. Introduction

This lab project is based on the implementation of the cascading of two 74LS163 counters, a logical circuit that tracks time by using 8 bits.
We use these clocks' input to count the number of people in the theater and we pause the counters as soon as we reach 210.

II. Design Methodology

For this lab project, we use the 74LS163 4-bit counter. This 4-bits counter requires not only a voltage source—to function—and a clock—to provide it with time input—but also a binary switch, to reset it and ensure the wave functions it outputs are correct. Additionally, although we use a resistor, its value can be changed or ignored; our 1kΩ resistor is part of the circuit to demonstrate that we are not focusing on the input voltage, but on the H and L states instead.
Furthermore, by cascading two of these clocks together, we use their output in an 8-input NAND gate to stop counting once we reach the maximum capacity, 210, in a theater. We do this by connecting the NAND gate's output, set to produce a negative value once we reach 210, with the P and T inputs in the first counter, the one that counts the last 4 significant bits

A. *Parts List*

- Clock
- 5V Source
- Two 74LS163 counters
- Binary switch
- Resistor
- 8-input NAND gate
- NOT gates

B. *Truth Tables*

State	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
q_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
q_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
q_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
q_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Figure 1. Truth table for a 74LS163 4-bit counter.

C. *Schematics*

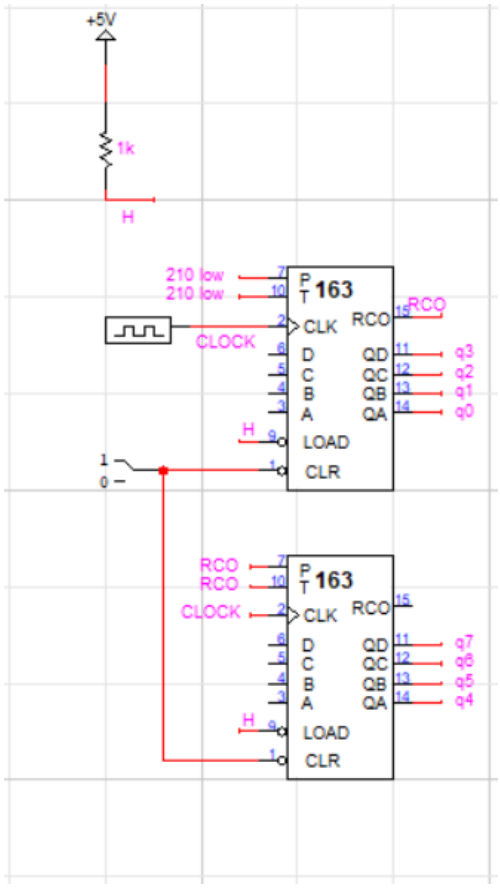

Figure 2. Two 74LS163 counters cascaded together.

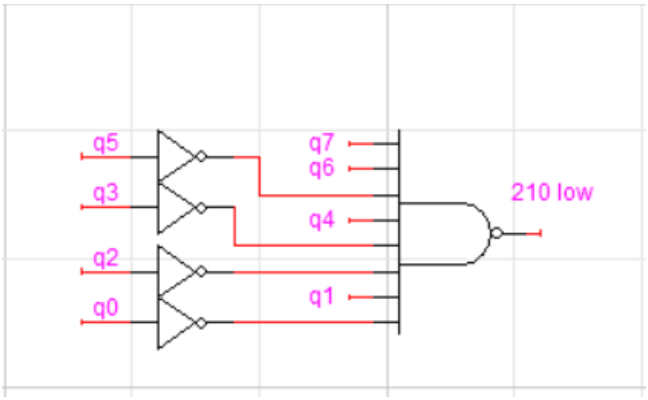

Figure 3. Gate that stops the counters once they reach 210.

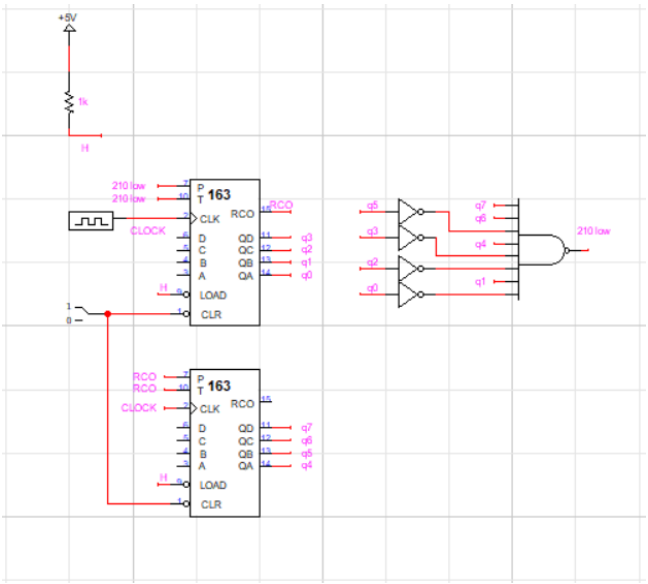

Figure 4. Complete circuit. Two counters cascaded together, and an 8-input NAND gate set to produce a low input once it reaches 210.

III. TESTING PROCEDURES

1. Create two counters as pictured in Figure 3.
2. Set up a the 8-input NAND gate as pictured in Figure 4.
3. Feed the NAND gate's output to the 4 lowest bit's counter's P and T.
4. Reset both CLRs with a switch and run the simulation.

IV. TESTING RESULTS

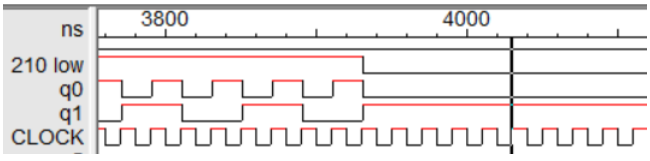

Figure 5. The complete circuit's simulation results.

V. CONCLUSION

In conclusion, an 8-bits binary number can be represented by two 74LS163 clock-counter circuit. If we use these 8-bits to encode for 210, produce a low signal once this happens, and feed this signal to the first clock's—the one feeding input to the second clock—P and T, then we can stop counting once we reach 210, as requested by the specs.