CMPE 110 Lab 4: CMOS Circuits

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***Abstract*—The purpose of this lab project is to learn about rise and fall propagation delays and times in CMOS circuits.**

I. INTRODUCTION

This lab project is based on the implementation of a CMOS inverter, NAND, and NOR circuits. To observe and record their rise and fall propagation delays and times, we vary each circuit's fan-out.

A. Parts List

- Capacitors (10 pF)
- BSS84 MOSFETs
- HAT2044R MOSFETs
- Generators (see **Figures 1-5**)

II. DESCRIPTION OF THE CIRCUITS' SCHEMATICS

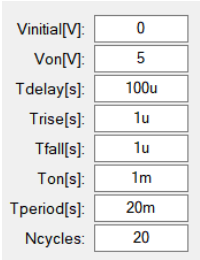

Figure 1. 0-5 V pulse generator's settings (V2).

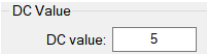

Figure 2. 5 V DC generator's settings (V1).

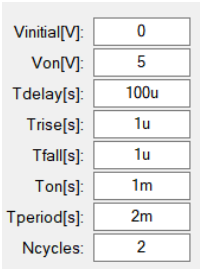

Figure 3. 0-5 V pulse generator's settings (VA, VB)

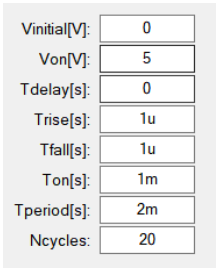

Figure 4. 0-5 V pulse generator's settings (VC, VD)

Figure 5. 0 V DC generator's settings (VE)

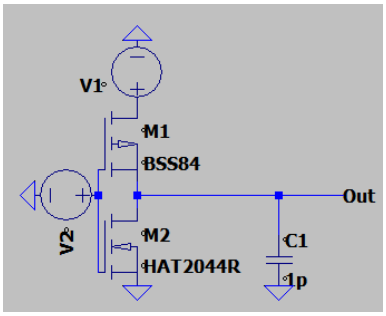

Figure 6. CMOS inverter circuit with 0 fan-out.

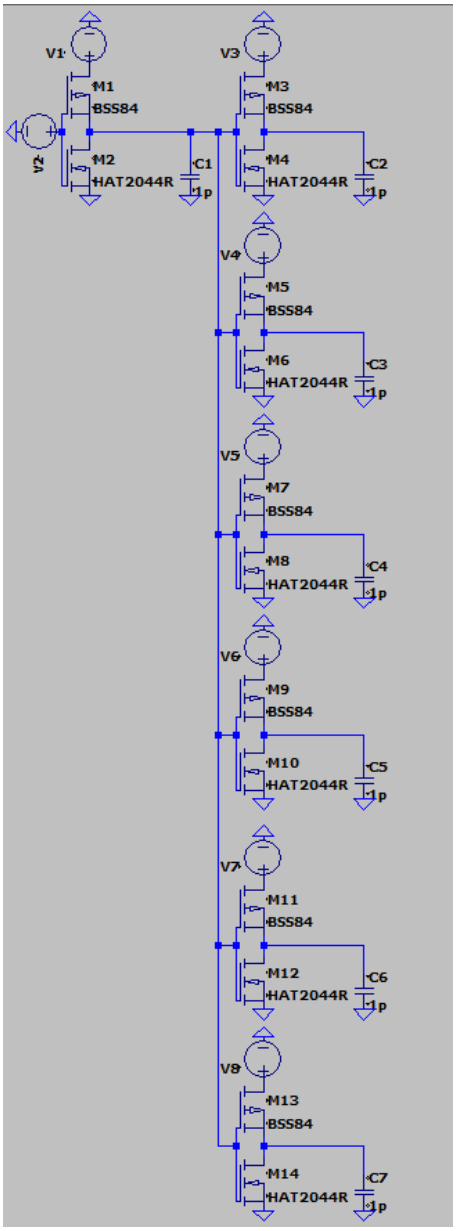

Figure 7. CMOS inverter circuit with 6 fan-out (sample of how to increase a CMOS inverter circuits' fan-out).

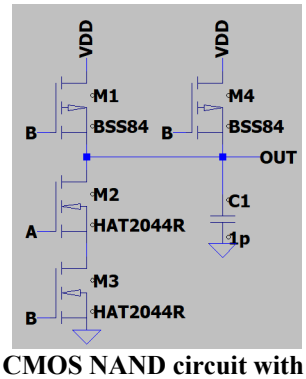

Figure 8. CMOS NAND circuit with 0 fan-out.

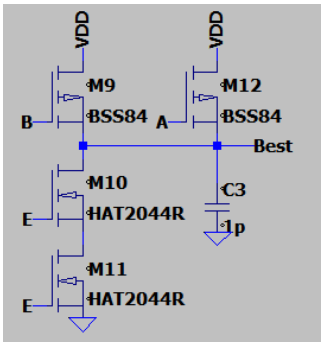

Figure 9. Best-case CMOS NAND circuit with 0 fan-out.

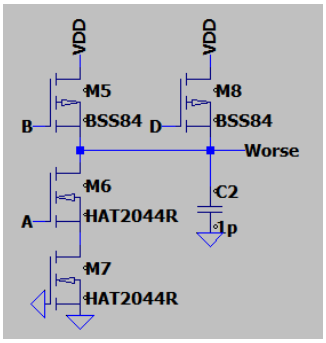

Figure 10. Worst-case CMOS NAND circuit with 0 fan-out.

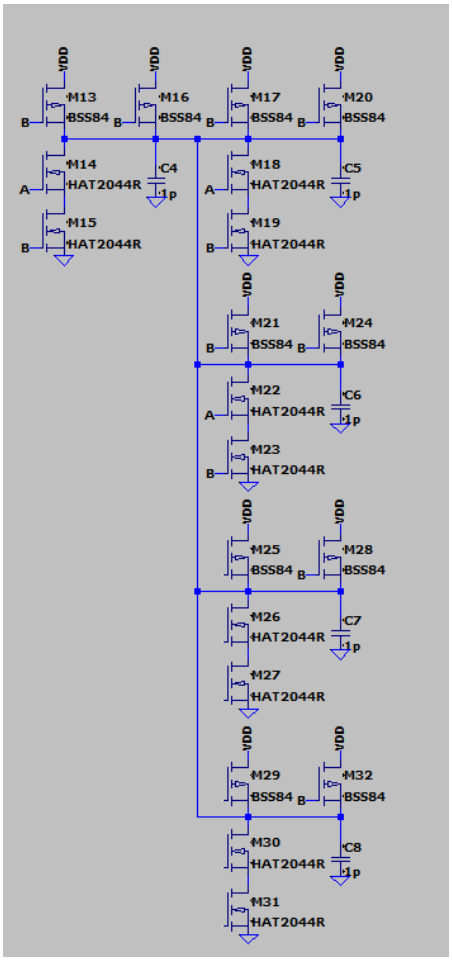

Figure 11. CMOS NAND circuit with 4 fan-out (sample of how to increase a CMOS NAND circuit's fan-out).

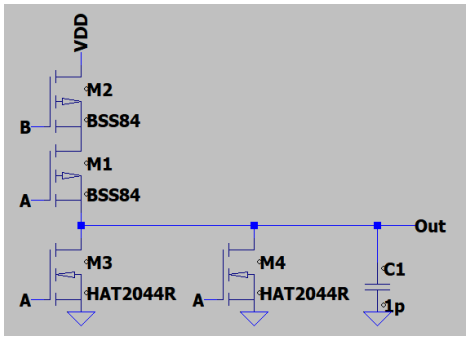

Figure 12. CMOS NOR circuit with 0 fan-out.

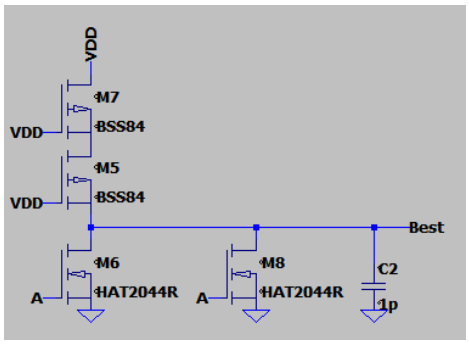

Figure 13. Best-case CMOS NOR circuit with 0 fan-out.

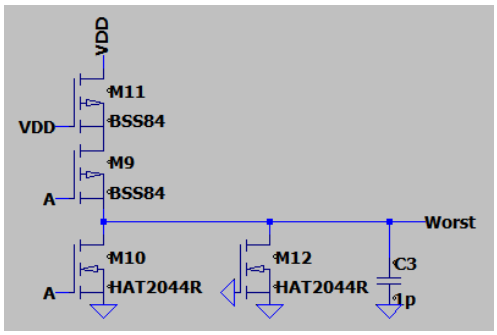

Figure 14. Worst-case CMOS NOR circuit with 0 fan-out.

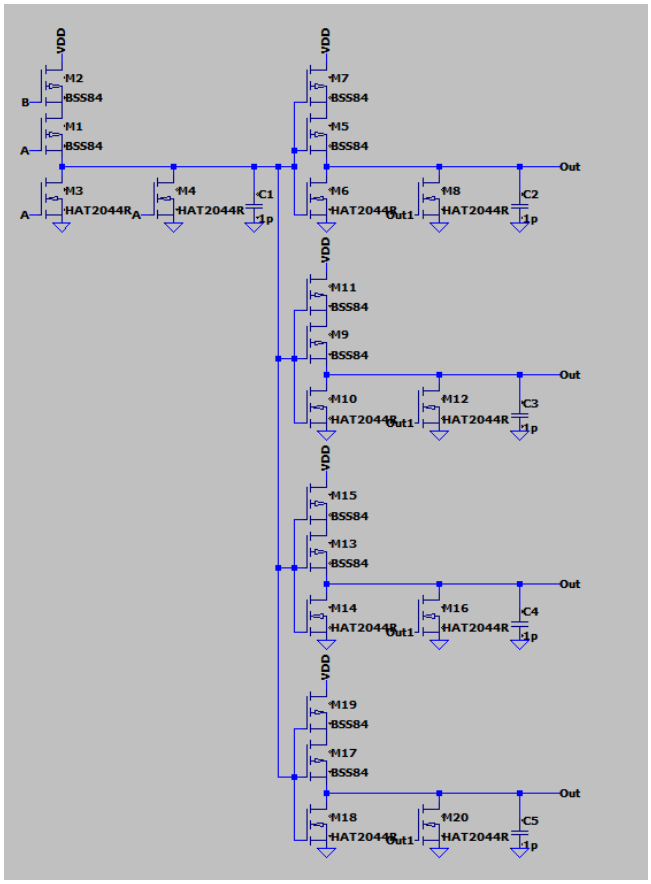

Figure 15. CMOS NOR circuit with 4 fan-out (sample of how to increase a CMOS NAND circuit's fan-out).

III. WAVEFORMS AND RESULTS

- Part 1 – CMOS inverter circuits:

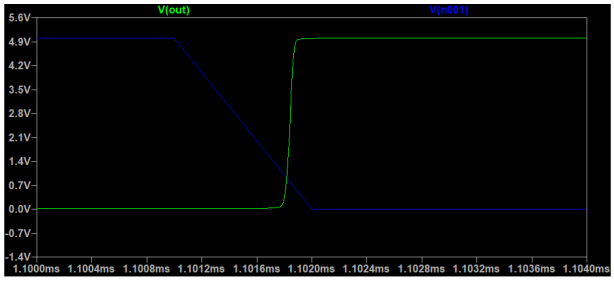

Figure 16. CMOS inverter circuits sample curves (0 fan-out)

Fan-Out	Rise Time	Rise Delay	Fall Time	Fall Delay
0	40.34 ns	343.21 ns	54.66 ns	258.83 ns
6	12.39 ns	180.42 ns	17.95 ns	352.33 ns
12	12.35 ns	169.28 ns	40.17 ns	373.79 ns
18	12.86 ns	156.44 ns	45.75 ns	386.22 ns

Table 1. Rise and fall propagation delay and times in CMOS inverter circuits.

Fan-Out	R_N	R_P
0	39042.86 Ω	28814.29 Ω
6	12821.43 Ω	8850.00 Ω
12	28692.86 Ω	8821.43 Ω
18	32678.57 Ω	9185.71 Ω

Table 2. R_N and R_P in CMOS inverter circuits. Calculated using: $R_N = \frac{Fall\ Time}{1.4*1\ pF}$ and $R_P = \frac{Rise\ Time}{1.4*1\ pF}$.

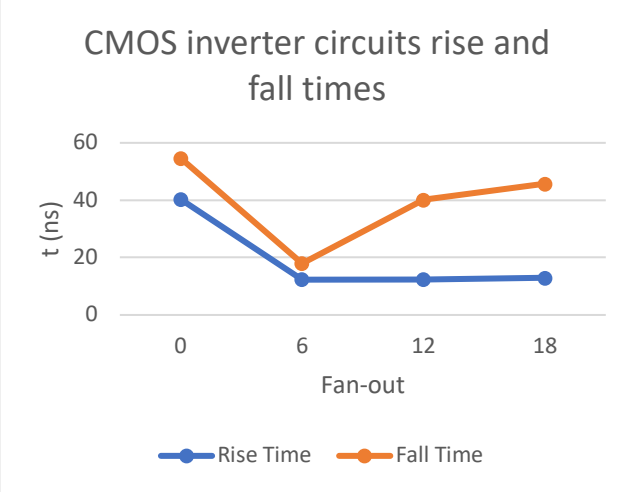

Figure 17. Rise time and fall times in function of fan-out in CMOS inverter circuits

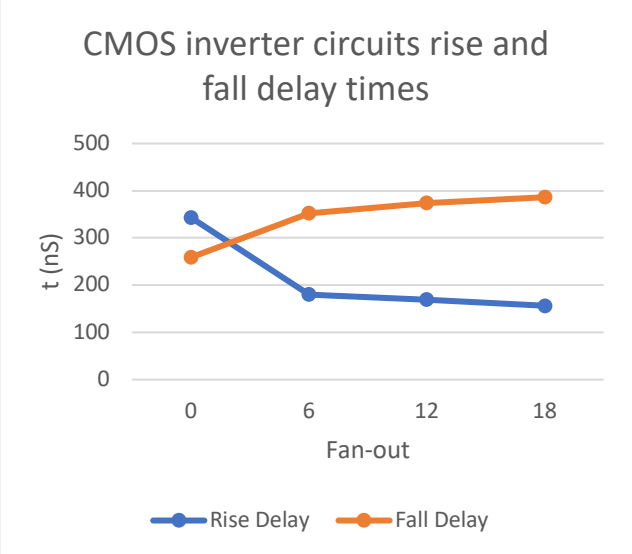

Figure 18. Rise time and fall times in function of fan-out in CMOS inverter circuits

- Part 2 – CMOS NAND:

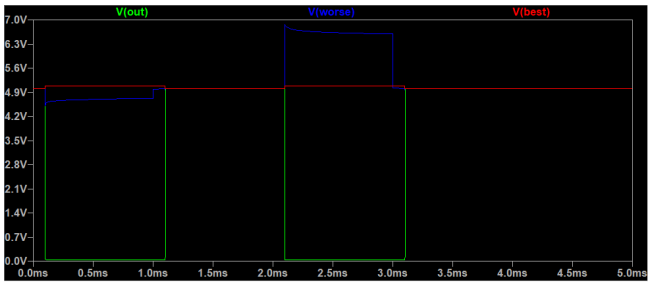

Figure 19. CMOS NAND circuits sample curves (0 fan-out)

Fan-Out	Rise Time	Fall Time
0	30.79 ns	58.26 ns
4	8.05 ns	13.51 ns
8	8.13 ns	21.09 ns
12	9.12 ns	27.34 ns

Table 3. Rise and fall times in CMOS NAND circuits.

Fan-Out	Rise Delay	Fall Delay
0	271.92 ns	230.26 ns
4	1 ms	317.34 ns
8	1 ms	336.17 ns
12	1 ms	351.44 ns

Table 4. Best-case rise and fall propagation delay in CMOS NAND circuits.

Fan-Out	Rise Delay	Fall Delay
0	279.94 ns	229.53 ns
4	3 ms	318.02 ns
8	3 ms	335.95 ns
12	3 ms	351.50 ns

Table 5. Worst-case rise and fall propagation delay in CMOS NAND circuits.

Fan-Out	R_N	R_P
0	41614.29 Ω	21992.86 Ω
4	9650.00 Ω	5750.00 Ω
8	15064.29 Ω	5807.14 Ω
12	19528.57 Ω	6154.29 Ω

Table 6. R_N and R_P in CMOS NAND circuits. Calculated using: $R_N = \frac{Fall\ Time}{1.4*1\ pF}$ and $R_P = \frac{Rise\ Time}{1.4*1\ pF}$.

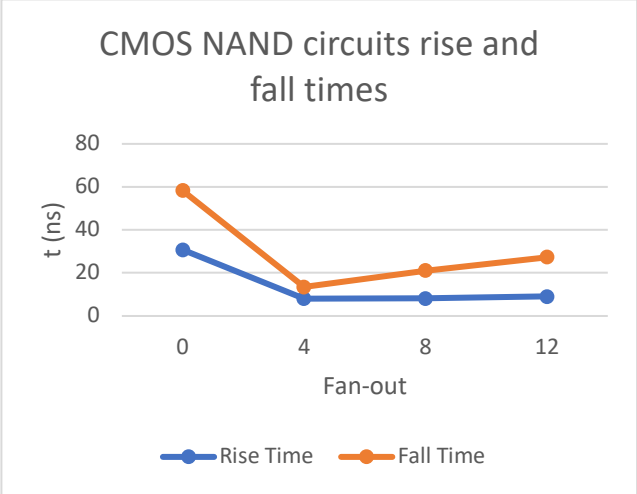

Figure 20. Rise time and fall times in function of fan-out in CMOS NAND circuits

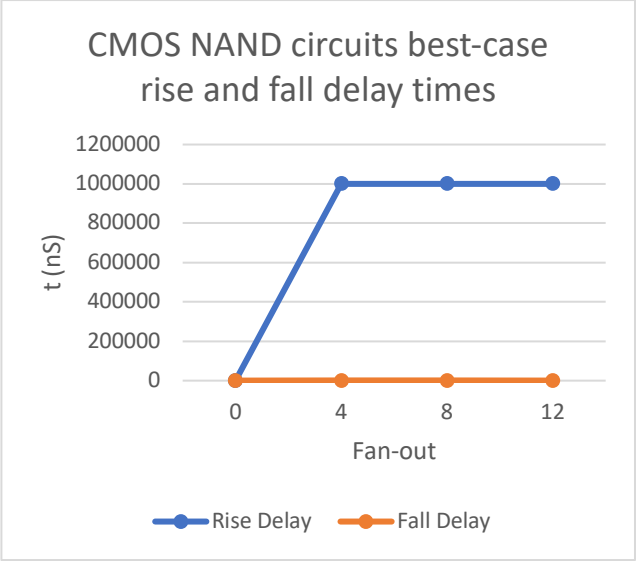

Figure 21. Rise time and fall times in function of fan-out in best-case CMOS NAND circuits

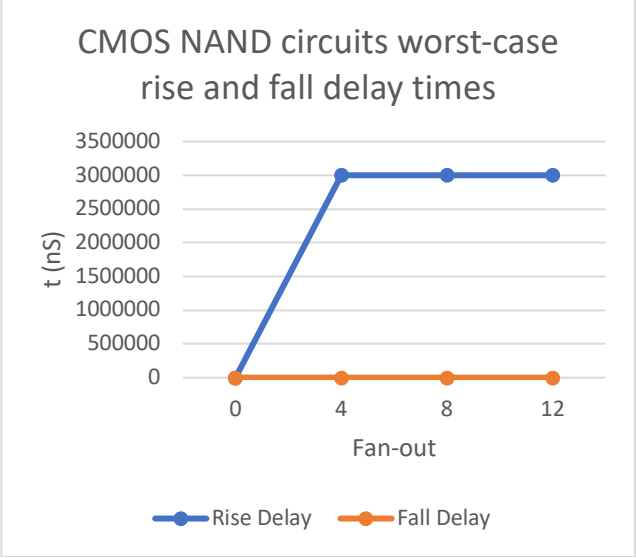

Figure 22. Rise time and fall times in function of fan-out in worst-case CMOS NAND circuits

- Part 3 – CMOS NOR:

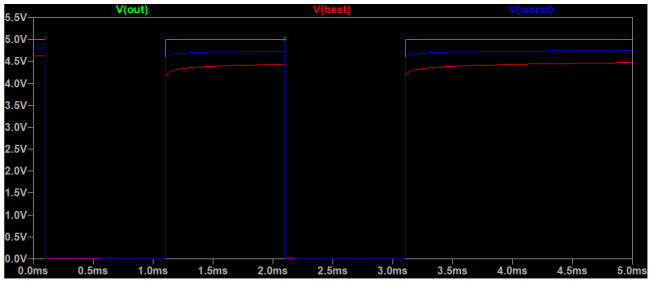

Figure 23. CMOS NOR circuits sample curves (0 fan-out)

Fan-Out	Rise Time	Fall Time
0	53.44 ns	47.27 ns
4	33.36 ns	70.03 ns
8	33.52 ns	83.11 ns
12	33.48 ns	120.89 ns

Table 7. Rise and fall times in CMOS NOR circuits.

Fan-Out	Rise Delay	Fall Delay
0	330.22 ns	270.95 ns
4	1 ms	437.71 ns
8	1 ms	518.48 ns
12	1 ms	599.74 ns

Table 1. Best-case rise and fall propagation delay in CMOS NOR circuits.

Fan-Out	Rise Delay	Fall Delay
0	330.35 ns	262.02 ns
4	1 ms	422.93 ns
8	1 ms	502.01 ns
12	1 ms	579.16 ns

Table 9. Worst-case rise and fall propagation delay in CMOS NOR circuits.

Fan-Out	R_N	R_P
0	33764.29 Ω	38171.43 Ω
4	50021.43 Ω	23828.57 Ω
8	59364.29 Ω	23942.86 Ω
12	86350.00 Ω	23914.29 Ω

Table 10. R_N and R_P in CMOS NOR circuits. Calculated using: $R_N = \frac{Fall\ Time}{1.4*1\ pF}$ and $R_P = \frac{Rise\ Time}{1.4*1\ pF}$.

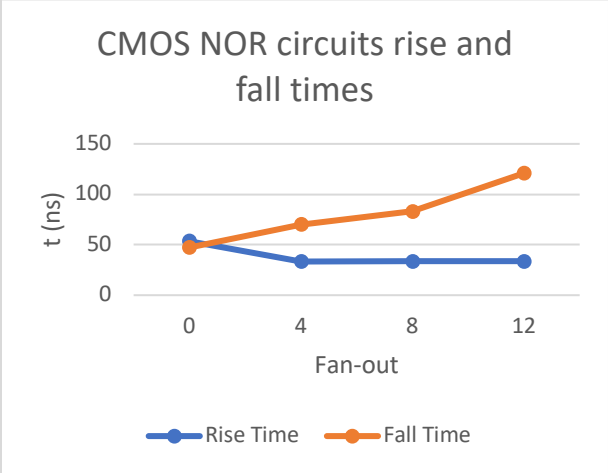

Figure 24. Rise time and fall times in function of fan-out in CMOS NOR circuits

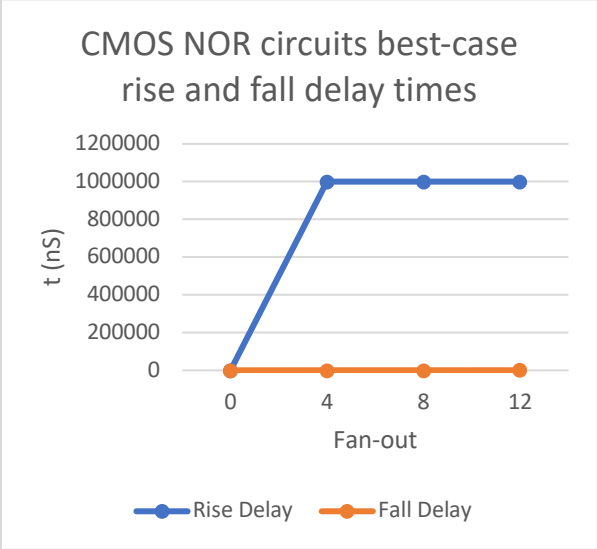

Figure 25. Rise time and fall times in function of fan-out in best-case CMOS NOR circuits

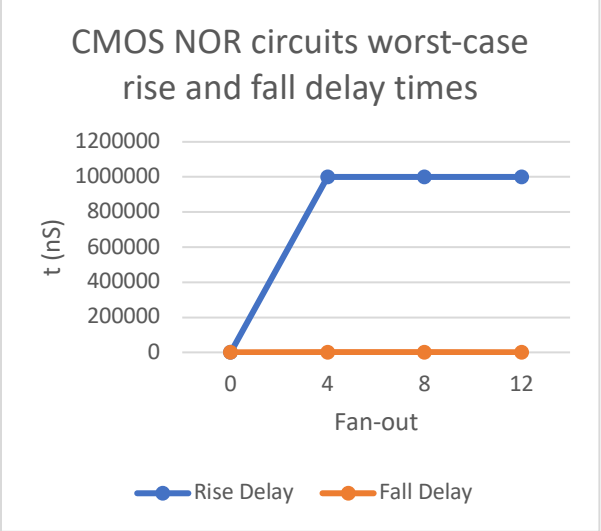

Figure 26. Rise time and fall times in function of fan-out in worst-case CMOS NOR circuits

IV. DISCUSSION

For Part 1, we assembled the CMOS inverter circuit as instructed, and then proceeded to increase its' fan-out. We recorded the rise and all delays and times and computed the R_N and R_P for each case. We notice that, in general, the rise and fall times—and R_N and R_P—and rise delay decrease when transitioning from fan-out 0 to 6, but then increase as we continue to increase the fan-out. The fall delay continues to increase in all cases.

For Part 2, we assembled the CMOS NAND circuit as instructed, and then proceeded to increase its' fan-out. We recorded the rise and all delays and times, including those for best and worst-cases, and computed the R_N and R_P for each case. We notice that, in general, the rise and fall times—and R_N and R_P—decrease when transitioning from fan-out 0 to 6, but then increase as we continue to increase the fan-out. Furthermore, we also notice that the fall delay values increase with increasing fan-out numbers, in both best and worst-cases, and that the rise delay increases when transitioning from 0 to 4 fan-out—in both best and worst-cases—but then becomes steady and at very high values, if compared with their analog fall delay values.

For Part 3, we assembled the CMOS NOR circuit as instructed, and then proceeded to increase its' fan-out. We recorded the rise and all delays and times, including those for best and worst-cases, and computed the R_N and R_P for each case. We notice that, in general, while the rise time—and R_P— decreases when transitioning from fan-out 0 to 6, but then increases as we continue the fan-out quantity increases, the fall time—and R_N—increases regardless of the fan-out. Furthermore, we also notice that the fall delay values increase with increasing fan-out numbers, in both best and worst-cases, and that the rise delay increases when transitioning from 0 to 4 fan-out—in both best and worst-cases—but then becomes steady and at very high values, if compared with their analog fall delay values.

V. DESCRIPTION OF THE LEARNING EXPERIENCE

This lab, in my opinion, required a lot of attention to detail. While increasing the fan-out of a CMOS circuit involves a lot of parts—hence exposing us to more potential errors—doing so several times, when increasing our circuits' fan-out, further increases our chances of facing bugs throughout our procedure.
Overall, I believe that this lab not only taught me about CMOS circuits and rise and fall delays and times, but more importantly, exposed me to the reality of circuits design, which involves a lot of patience, resilience, and attention to detail.

VI. CONCLUSION

In conclusion, depending on the CMOS circuit, increasing its fan-out could be used for increasing or decreasing its fall

or rise times. Furthermore, we note that while rise and fall delays are noticeably affected by the fan-out of a circuit, this is dramatically noticeably in the NAND and NOR circuits' cases, where these circuits' fanout affects the rise and fall delays such that the rise delay values are in the order of the milliseconds, while the fall delay values are in the order of the nanoseconds.

Finally, this lab experiment was a fruitful CMOS circuits learning experience. We learned not only how inverter, NAND and NOR CMOS circuits work, but also learned to better analyze, understand, and handle circuits in general. This lab was particularly helpful in conveying the idea of rise and fall delays and times within CMOS circuits.