COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE
14:332:331
Rutgers University
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Homework 1
Due: Sep. 30, 2016

1. You are on the design team for a new processor. The clock of the processor runs at 500 MHz. The following table gives instruction frequencies for Benchmark B, as well as how many cycles the instructions take, for the different classes of instructions. For this problem, we assume that (unlike many of today's computers) the processor only executes one instruction at a time.

Instruction Type	**Frequency**	**Cycles**
Loads & Stores	30%	5 cycles
Arithmetic Instructions	40%	6 cycles
All Others	30%	3 cycles

   a. Calculate the CPI for Benchmark B.
   b. The CPU execution time on the benchmark is exactly 11 seconds. What is the "MIPS" (MIPS here stands for Millions of Instructions executed Per Second)?
   c. Assume that if you double the number of registers, the cycle time must be increased by 20%. What would the new clock speed be (in MHz)?
   d. Assume that if you double the number of registers, then the compiler will generate code that requires only half the number of Loads & Stores. What would the new CPI be on the benchmark?
   e. How many CPU seconds will the benchmark take if we double the number of registers (taking into account both changes described above)?

2. Assume a program includes 3000 integer instructions (INT), 30,000 floating point (FP) instructions, 5000 Load/Store (L/S) instructions and 10000 branch instructions. The CPI for each type of instruction is 1, 1, 3 and 2, respectively. Assume that the processor has a 2.6 GHz clock rate.

   a. By how much must we improve the CPI of FP instructions if we want the program to run 50% faster?
   b. By how much must we improve the CPI of L/S instruction if we want the program to run 30% faster?
   c. By how much is the execution time of the program improved if the CPI of INT and FP instructions are reduced by 25% and the CPI of L/S and Branch is reduced by 30%?

3. Suppose you have a machine which executes a program consisting of 50% floating point multiply, 20% floating point divide, and the remaining 30% are from other instructions.

a. Management wants the machine to run 4 times faster. You can make the divide run at most 3 times faster and the multiply run at most 8 times faster. Can you meet management’s goal by making only one improvement, and which one?

b. If you make both the multiply and divide improvements, what is the speed of the improved machine relative to the original machine?

4. The base address of the array B is stored in $s2. We want to load B[16] into $t1. In the following cases, please fill the blanks with appropriate parameters to do so (Please show the values in **HEX**)

a. **lw $t1, __($s2)**

b. **addi $t0, $s2, 24**
lw $t1, __($t0)

c. **addi $t0, $s2, 96**
lw $t1, __($t0)

5. The following instructions are pseudo instructions that are not included in the MIPS ISA. Please write down the shortest sequence of MIPS instructions that perform the same operation.

a. **subi $t1, $t4, 10** #$t1=$t4-10
b. **subi $t4, $t2,** 2^{22} #$t4=$t2-2^{22}
c. **rpt $t1, L1** #if ($t1<0) $t1=$t1+1, go to L1

6. Find the shortest sequence of MIPS instruction that extracts the value shown in bits 22 down to 4 from register $t0 and compute the half of this value (the value is assumed unsigned integer) and use the new value to replace bits 24 down to 6 in register $t1 (note that other bits of $t1 will remain unchanged.)

7. Compile the assembly code for the following C codes. Assume that i, j, and k have been stored in $s0, $s1, and $s2 respectively. The base address of the array B is stored in $s4. Please only use only **TRUE** MIPS instructions.

a. **for (i=k; i>0; i=i-2)**
    j = i + 2k;

b. **for (i=0; i<k; i++)**
    for (j=1; j<i; j++)
      B[2j]=B[i-k]-4