COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE
14:332:331
Rutgers University
Fall 2016

Homework 3
Due: Oct. 28, 2016

1. Suppose A = C4 and B = 4D (both in hexadecimal). Show the step by step result multiplying A and B, using Booth's algorithm. Assume A and B are 8-bit two's complement integers, stored in hexadecimal format.

2. Suppose A = C4 and B = 4D (both in hexadecimal). Show the step by step result multiplying A and B, using the multiplier hardware shown in Fig. 1. Assume A and B are 8-bit unsigned numbers, stored in hexadecimal format.

   b) Suppose for an 8-bit number, each step of operation (either addition or shift) takes 2ns. Please calculate the worst case time necessary to perform a multiply using the approach given in Fig. 1. Assume the registers have been initialized. In hardware, please note that the shifts of the multiplicand and multiplier can be done simultaneously.

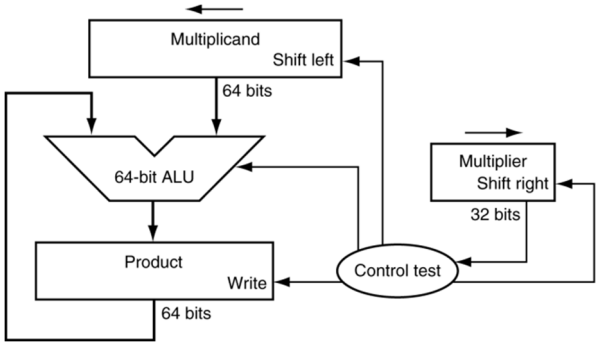

Fig. 1

3. Compile the assembly code for the following C code (using jr). Assume that s, i, j, and h are in $s0,$s1, and $s2, and $s3, respectively and that sequential words in memory starting at $s4.

```
switch(s){
    case 0: h=i+3j; break;
    case 1: h=j-4i; break;
}
```

4. Suppose A = 0111 and B = 0101. Show the step by step result computing A divide B, using the hardware hardware shown in Fig. 2. Assume A and B are 4-bit unsigned numbers. Dividend is initially loaded into the Remainder register. Please show the steps in the given table. Please expand the table if more rows needed.

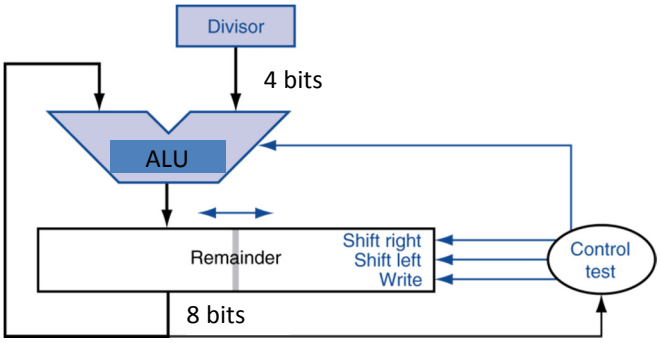

Fig. 2

Quotient	Deviser	Remainder	Description	Step
			Initial values	Step 1
				Step 2

b) Suppose that each operation (addition, subtraction or shift) takes 2ns. Please calculate the time necessary to perform **the above division** using the given hardware. Assume the registers have been initialized.

5. Assume that IEEE 754 floating point format is used and $f1 and $f2 and $f3 store the floating numbers as below:

$f1: 1010 1010 0110 1010 1001 1010 0000 0011
$f2: 1010 1010 0100 1011 0100 0010 0000 1010
$f3: 0010 0001 0011 0111 0101 0111 0110 0001

a) Please show the step by step result computing for ($f1+$f2)+$f3 (in floating point format). (first show the steps required to compute $f1+$f2 and then the steps for adding this results to $f3)

b) Please show the values of each register in decimal as well as the value of the final result ($f1+$f2+$f3) in decimal.

6. Repeat Question 5.a and show the steps required to compute ($f1*$f2)*$f3.
   b) Show the result of ($f1*$f2)*$f3 in decimal.