COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE
14:332:331
Rutgers University
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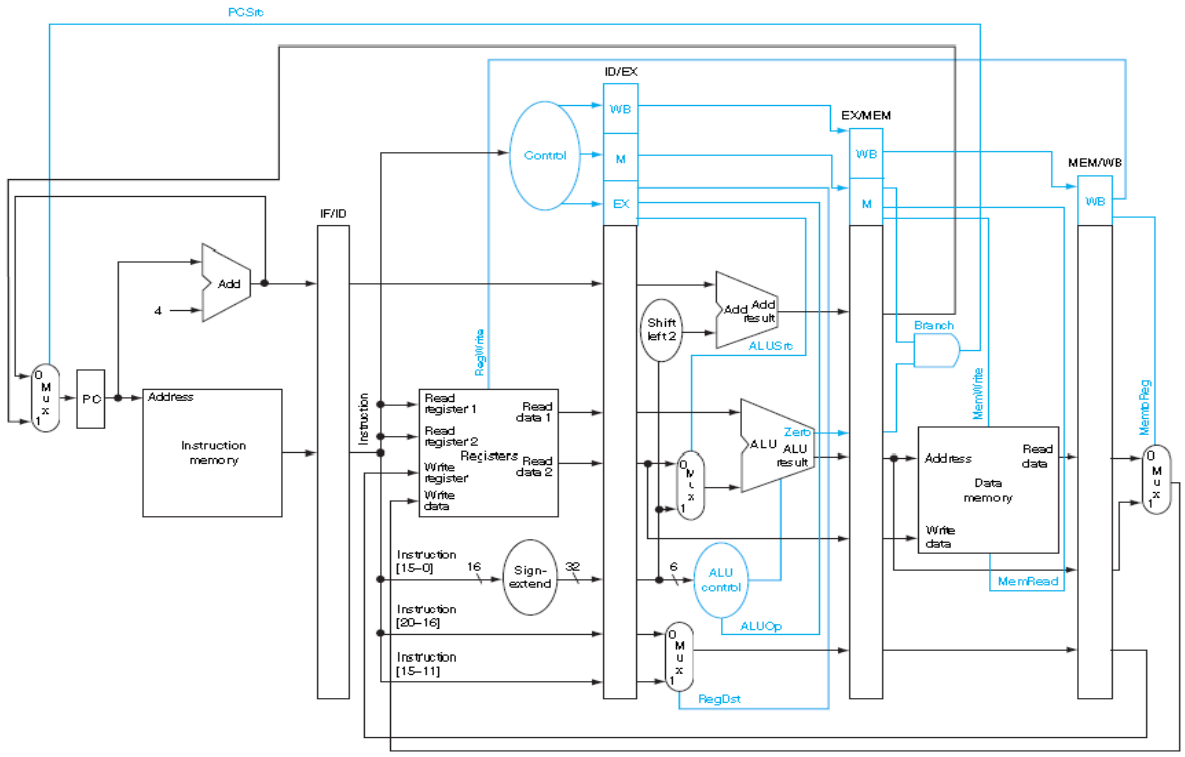
Quiz 3 Solution

Question1. Consider the following instruction sequence. We want to run this code on pipelined MIPS.

and R2, R1, R10
lw R1, 2(R2)
add R10, R2, R6
lw R6, 10(R10)
sw R6, 2(R3)
sub R15, R6, R3
lw R7, 6(R15)
or R8, R7, R6

(1.1) Show all the data hazards (assuming that there is no forwarding).
(1.2) Show the pipeline stages for each instruction in different clock cycles (assuming that there is no forwarding)
(1.3) Repeat part b but assume that there is a full forwarding mechanism.



Solution

1.1. Data Hazards in the given instructions (assuming no forwarding) are:

a) The data in R2 is **used by instruction 2 and instruction 3** before it is written back by "and" instruction (instruction 1)

b) The data in R10 is **used by instruction 4** before it is written back by "add" instruction (instruction 3)

c) Instruction 4 loads a new value into R6, and **instruction 5 and instruction 6** uses that value, but the value of R6 is not available as instruction 4 has not written the value yet.

d) Instruction 6 calculate the value of R15 which is **used by instruction 7** to load value in R7, there should be two stalls as the value of R15 will not be available for instruction 7.

e) Instruction 7 generates the value of R7 and **instruction 8** uses R7 as source before it is ready.

1.2. Below table shows the pipeline and stalls for given instructions.

Inst\Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
and R2,R1, R10	IF	ID	EX	MEM	WB																	
Stall																						
Stall																						
lw R1, 2(R2)				IF	ID	EX	MEM	WB														
add R10, R2, R6					IF	ID	EX	MEM	WB													
Stall																						
Stall																						
lw R6, 10(R10)								IF	ID	EX	MEM	WB										
Stall																						
Stall																						
sw R6, 2(R3)											IF	ID	EX	MEM	WB							
sub R15, R6, R3												IF	ID	EX	MEM	WB						
Stall																						
Stall																						
lw R7, 6(R15)															IF	ID	EX	MEM	WB			
Stall																						
Stall																						
or R8, R7, R6																		IF	ID	EX	MEM	WB

1.3. The below table shows the pipeline with forwarding.

Inst\Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14
and R2,R1, R10	IF	ID	EX	MEM	WB									
lw R1, 2(R2)		IF	ID	EX	MEM	WB								
add R10, R2, R6			IF	ID	EX	MEM	WB							
lw R6, 10(R10)				IF	ID	EX	MEM	WB						
sw R6, 2(R3)					IF	ID	EX	MEM	WB					
sub R15, R6, R3						IF	ID	EX	MEM	WB				
lw R7,6(R15)							IF	ID	EX	MEM	WB			
Stall		Stal	Stall	Stall	Stall	Stall	Stall	Stall	Stall	Stall	Stall	Stall	Stall	
or R8, R7, R6									IF	ID	EX	MEM	WB	