COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE
14:332:331
Rutgers University
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Homework 5
Due: Dec 6, 2016

Note: Question 6 is for your practice. You do not need to answer question 6.

1. Suppose that your processor has 8MB data cache and its block size is 64B. Physical address to access the memory is 54-bit wide (addr[53:0]). For each of the following cache structures, calculate TAG size and index size.
   (a) A direct-mapped cache implementation
   (b) A 4-Way set associative cache implementation
   (c) A fully associative cache implementation

2. The following **memory addresses** are used consecutively by a running program (from left to right, shown in decimal). Note that the followings are memory address not block number:

   520, 400, 380, 540, 816, 204, 1348, 200, 440, 140, 1064, 44, 196, 404, 180

   In each of the following cache structures, compute the number of hits, misses and the final values stored in each cache location (show finally which block of memory is in each cache block). Each word is 4-bytes and the memory size is 8Kbyte

   (a) Direct-mapped cache with 32-word blocks and a total size of cache is 128 words of data
   (b) 2-way set associative cache with 32-word blocks and a total size of cache is 128 words of data. (LRU replacement)

3. For each part of Question 2, find the size of the cache required to hold the data (as mentioned in 2.a and 2.b above the cache should hold 128 words of data)?

4. In each of the following three cases, calculate the CPI for a processor with these specifications:
   - Base CPI=3
   - Processor speed=2 GHz
   - Main memory access time=100ns
   - First-level cache miss rate per instruction=12%

   (a) We only have a first level (L1) cache
   (b) Along with L1 cache, we also have a second level direct-mapped cache in which
   . Second-level cache direct-mapped speed=20 cycle
   . Global miss rate with second-level cache direct-mapped=4%

   (c) Along with L1 cache, we also have a second level 4-way set associative cache in which:
   .Second-level cache 4-way set-associative speed=24 cycle
   .Global miss rate with second-level cache 4-way set-associative=3%

5.

(a) What is the average memory access time (AMAT) if a cache uses write-back strategy and 20% of the data blocks to be swapped out are dirty. Assume that the miss rate is 15%, the hit time of the cache is 1 cycle and the miss penalty is 8 cycles for the data blocks that are not dirty and 20 cycles for those blocks that are dirty.

(b) What is the speedup up if we add a "write-buffer" that eliminates 40% of the stall cycles to write back the dirty blocks?

6. As discussed, virtual memory uses a page table to track the mapping of virtual addresses to physical addresses. This exercise shows how this table must be updated as addresses are accessed. The following data constitutes a stream of virtual addresses as seen on a system. Assume 4 KB pages, a 4-entry fully associative TLB, and LRU replacement. If pages must be brought in from disk, increment the next largest page number.

Virtual addresses: 4669, 2227, 13916, 34587, 48870, 12608, 49225

TLB

Valid	Tag	Physical Page Number
1	11	12
1	7	4
1	3	6
0	4	9

Page Table

Valid	Physical Page or in Disk
1	5
0	Disk
0	Disk
1	68
1	9
1	11
0	Disk
1	4
0	Disk
0	Disk
1	3
1	12

Given the address stream shown, and initial TLB and Page Table States provided above, show if each reference is hit in the TLB, a hit in the page table, or a page fault. (To make it clear, the first two accesses have been shown below. Please continue in the same way)

Address	Virtual Page	TLB H/M	TLB		
			Valid	Tag	Physical Page
4669	1	TLB miss PT hit PF	1	11	12
			1	7	4
			1	3	6
			1 (last access 0)	1	13
2227	0	TLB miss PT hit	1 (last access 1)	0	5
			1	7	4
			1	3	6
			1 (last access 0)	1	13