COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE
14:332:331
Rutgers University
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Homework 1
Due: Feb. 13, 2017

1. Consider two different implementation of the same instruction set architecture. The instruction can be divided into four classes according to their CPI (class A, B, C and D). P1 with clock rate of 2.5 GHz and CPIs of 1, 2, 3 and 3, and P2 with a clock 3 GHz and CPIs of 2, 2, 2 and 2.
   Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C and 20% class D, which implementation is faster?

   a) What is the global CPI for each implementation?
   b) Find the clock cycle required in both cases.

2. Assume a program requires the execution of 50 x 106 FP instructions, 110 x 106 INT instructions, 80 x 106 Load/Store (L/S) instructions and 16 x 106 branch instructions. The CPI for each type of instruction is 1, 1, 4 and 2, respectively. Assume that the processor has a 2 GHz clock rate.

   a) By how much must we improve the CPI of FP instructions if we want the program to run two times faster?
   b) By how much must we improve the CPI of L/S instruction if we want the program to run two times faster?
   c) By how much is the execution time of the program improved if the CPI of INT and FP instructions are reduced by 40% and the CPI of L/S and Branch is reduced by 30%?

3. The base address of the array B is stored in $s1. We want to load B[5] into $t0. In the following cases, please fill the blanks with appropriate parameters to do so (Please show the values in **HEX**)

   a. **lw $t0, __($s0)**

   b. **addi $t1, $s0, 12**
      lw $t0, __($t1)

   c. **addi $t1, $s0, 32**
      lw $t0, __($t1)

4. The following instructions are pseudo instructions that are not included in the MIPS ISA. Please write down the shortest sequence of MIPS instructions that perform the same operation.
   a. **subi $t1, $t4, 10** #$t1=$t4-10
   b. **subi $t1, $t5, 2^{18}** #$t1=$t5-2^{18}
   c. **rpt $t2, loop** #if ($t2>0) $t2=$t2-1, go to loop

5. Compile the assembly code for the following C codes. Assume that i, j, and k have been stored in $s0, $s1, and $s2 respectively. The base address of the array B is stored in $s3. Please only use only **TRUE** MIPS instructions.

   a. **for (i=0; i<k; i++)**
      j = j + 2k;

   b. **for (i=0; i<k; i++)**
      for (j=1; j<i; j++)
      B[i-j]=B[2*j-1]+10

6. Find the shortest sequence of MIPS instruction that extracts bits 16 down to 11 from register $t0 and use the value of this field to replace bits 31 down to 26 in register $t1 without changing the other 26 bits of register $t1.

7. Translate the following loop into C. Assume that C-level integer is held in register $t1, $s2 holds the C-level integer called ***result,*** and $s0 holds the base address of the integer ***MemArray.***

```
        addi $t1, $0, $0
LOOP: lw $s1, 0($s0)
        add $s2, $s2, $s1
        addi $s0, $s0, 4
        addi $t1, St1, 1
        slti $t2, $t1, 100
        bne $t2, $s0, LOOP
```

8. Compiler scan have a profound impact on the performance of an application. Assume that for a program, compiler A results in a dynamic instruction count of 1.0E9 and has an execution time of 1.1s, while compiler B results in a dynamic instruction count of 1.2E9 and an execution time of 1.5 s.
   a. Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.
   b. Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler's A code versus the clock of the processor running compiler B's code?
   c. A new compiler is developed that uses only 6.0EB instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor?

9. One fallacy students and researchers often make is expecting to improve the overall performance of a computer just by improving only one aspect of the computer. Consider a computer running a program that requires 250 s, with 70 s spent executing FP instructions, 85 s executed L/S instructions, and 40 s spent executing branch instructions.

a. By how much is the total time reduced if the time for the FP operations is reduced by 20%?
b. By how much is the time for INT operations reduced if the total time is reduced by 20%?
c. Can the total time be reduced by 20% by reducing only the time for the branch instructions?

10. Assume a program requires the execution of 50 X 106 FP instructions, 110 X 106 INT instructions, 80 X 106 L/S instructions, and 16 X 106 branch instructions. The CPI for each type of the instructions is 1, 1, 4, and 2, respectively. Assume that a processor has a 2GHz clock rate.

a) By how much do we improve the CPI of FP instructions if we want the program to run two times faster?
b) By how much do we improve the CPI of L/S instructions if we want the program to run two times faster?
c) By how much is the execution time of the program improved if the CPI of INT and FP instructions is reduced by 40% and the CPI of L/S and Branch is reduced by 30%?