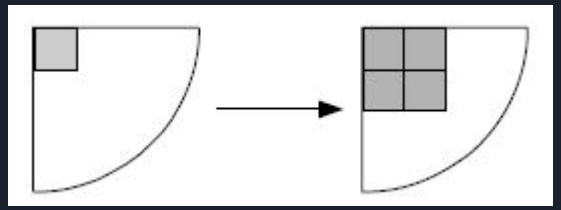
Tema 4 - Redução de Imagem

Leonardo Alves Paiva	10276911
Lucas Fernandes da Nobrega	9805320
João Pedro Doimo Torrezan	9806933

Índice

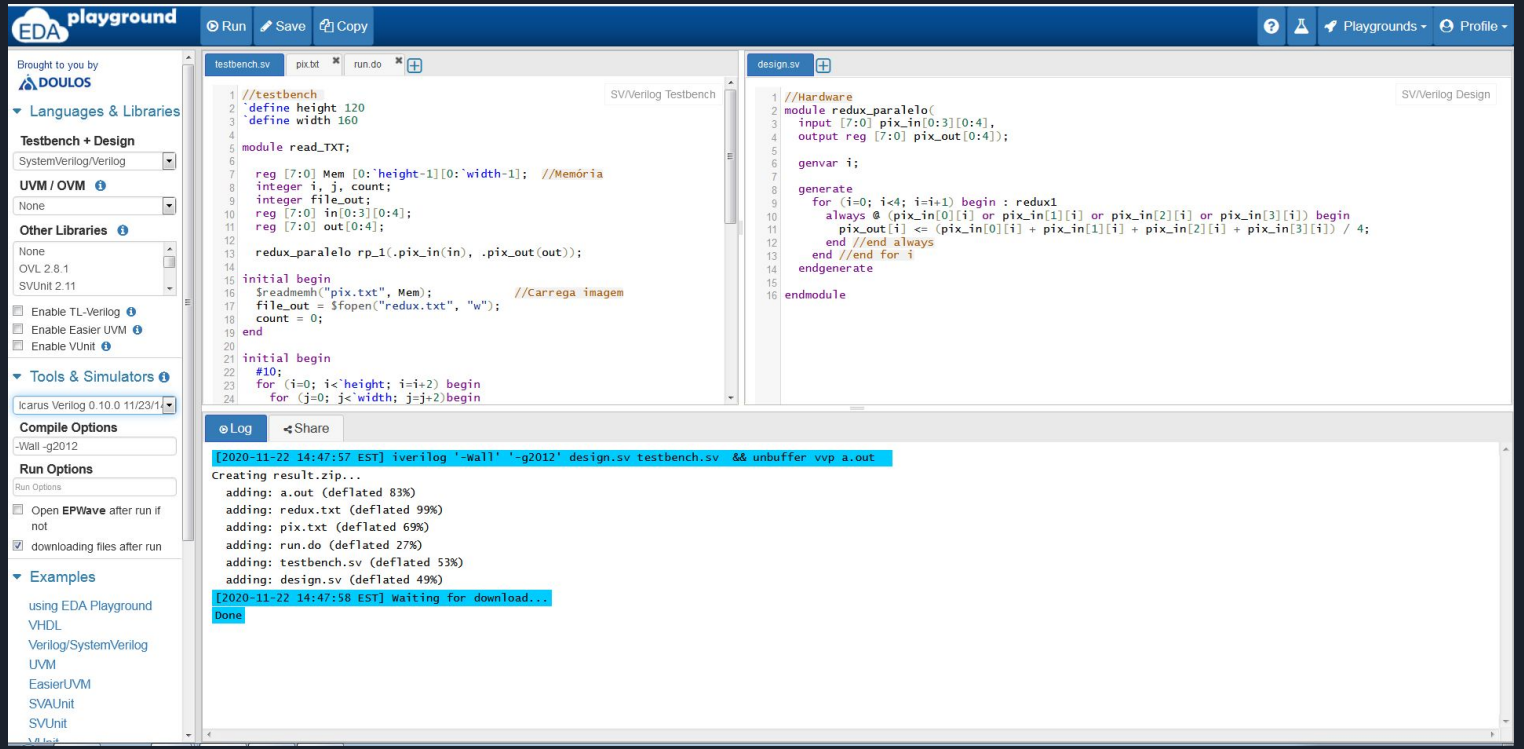
Ampliação e Redução

- Ampliação e redução das dimensões da imagem
- *Zoom in* e *Zoom out*
- Ampliação: Duplicar os pixels nos eixos X e Y



- Redução: processo inverso da ampliação
- Perda de informação
- Necessário calcular média

EDA Playground



EDA Playground

- *Online* e gratuito
- Ferramentas de sintetização (Mentor Precision 2019.2)
- Ferramentas de simulação (Icarus Verilog 0.10.0)
- Limitações para carregamento de arquivos (100 kB)
    - Resolução da imagem original 160x120 pixels

Programas Auxiliares

- *Pix* e *Repix*
- Desenvolvidos em C
- Necessários para trabalhar com imagens bitmap
- Pix - Lê bitmap e cria um arquivo TXT com os valores dos pixels em hexadecimal
- Repix - Lê o arquivo de saída do *testbench* com os valores da imagem reduzida e cria a imagem bitmap
- Manipulação do cabeçalho e da paleta de cores

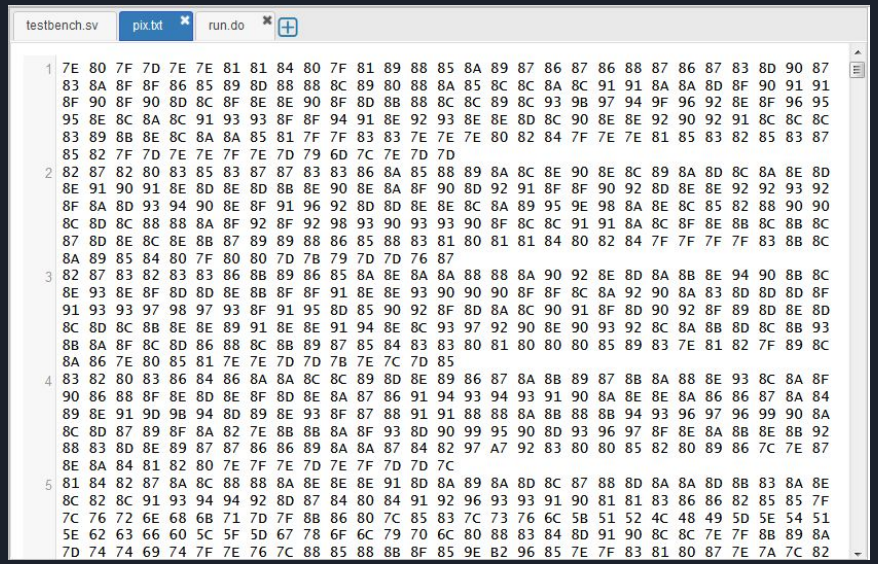
```
C:\Users\Leonardo\Downloads\Universidade\Sistemas Embarcados>Pix.exe u4.bmp
Tamanho: 20346
Offset dados bitmap: 1146
Comprimento: 160
Altura: 120
Size image: 19200
No. de cores usadas: 256
No. de bits por pixel: 8
Compressao: 0
```

Programas Auxiliares

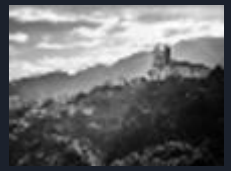
```
C:\Users\Leonardo\Downloads\Universidade\Sistemas Embarcados>Repix.exe u4.bmp re
dux.txt 0.5
Tamanho: 20346
Offset dados bitmap: 1146
Comprimento: 160
Altura: 120
Size image: 19200
No. de cores usadas: 256
No. de bits por pixel: 8
Compressao: 0

Tamanho: 5946
Offset dados bitmap: 1146
Comprimento: 80
Altura: 60
Size image: 4800
No. de cores usadas: 256
No. de bits por pixel: 8
Compressao: 0
```

Simulação

- *Icarus Verilog 0.10.0 11/23/14*
- Entrada *pix.txt*
  - Valores em hexadecimal
- *Testbench*
- *Design*
- Saída *redux.txt*
- *“download files after run”*



Exemplos

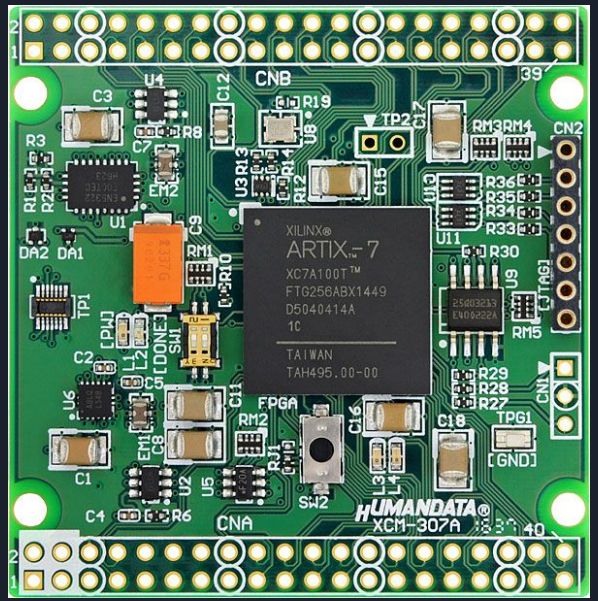


Síntese

- *Mentor Precision 2019.2*
- *Script run.do*
- Dispositivo *7A100TCSG324* da família *Artix-7* da *Xilinx*
- *Design*
- *Log* e vários arquivos de saída

testbench.sv | pix.txt | run.do

```
setup_design -manufacturer Xilinx -family Artix-7 -part 7A100TCSG324
foreach arg $::argv {
  add_input_file $arg
}

#Setup timing constraints
setup_design -frequency 1000

compile
synthesize
auto_write precision.v
report_output_file_list
report_area
report_timing
exec cat precision.v
```

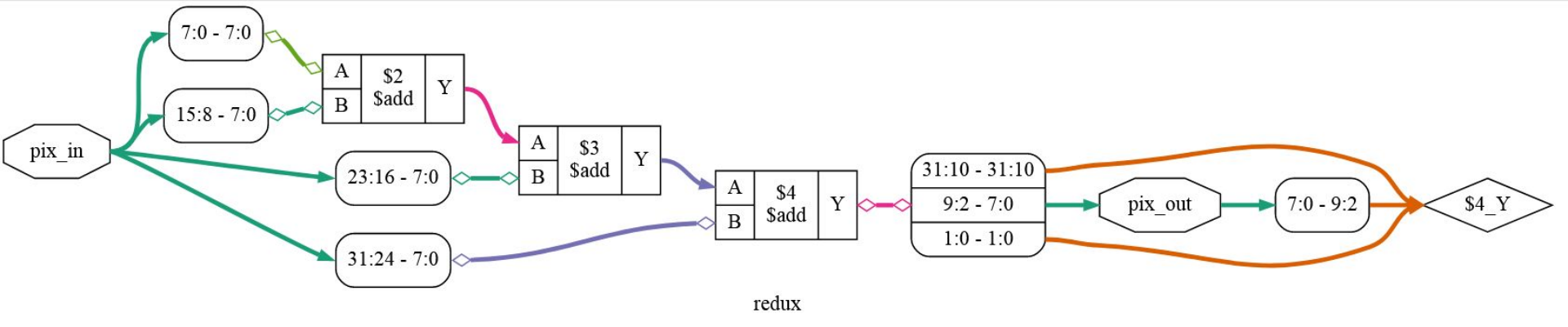


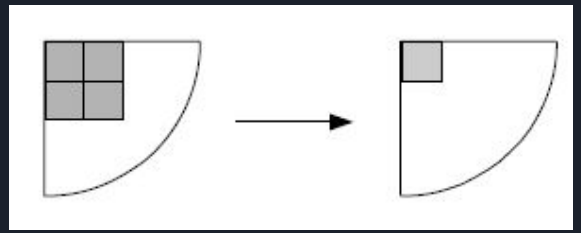
Síntese - Minimização do Hardware

```
# Info: ********************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ********************************************************************
# Info: Resource                          Used    Avail    Utilization
# Info: --------------------------------------------------------------------
# Info: IOs                               40      210       19.05%
# Info: Global Buffers                    0       32         0.00%
# Info: LUTs                              27      63400      0.04%
# Info: CLB Slices                        0       15850      0.00%
# Info: Dffs or Latches                   0       126800     0.00%
# Info: Block RAMs                        0       135        0.00%
# Info: DSP48E1s                          0       240        0.00%
# Info: --------------------------------------------------------------------
# Info: ************************************************************
# Info: Library: work    Cell: redux    View: INTERFACE
# Info: ************************************************************
# Info:  Number of ports :                          40
# Info:  Number of nets :                           136
# Info:  Number of instances :                      104
# Info:  Number of references to this view :        0
# Info: Total accumulated area :
# Info:  Number of LUTs :                           27
# Info:  Number of LUTs with LUTNM/HLUTNM :         16
# Info:  Number of MUX CARRYs :                     17
# Info:  Number of accumulated instances :          104
# Info: ****************************
```

Síntese - Esquemático

- *Yosys 0.9.0*





Síntese - Maximização do Throughput

```
# Info: ******************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ******************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ------------------------------------------------------------------
# Info: IOs                               200     210      95.24%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              135     63400     0.21%
# Info: CLB Slices                        0       15850     0.00%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: ------------------------------------------------------------------
# Info: ******************************************************************
# Info: Library: work    Cell: redux_paralelo    View: INTERFACE
# Info: ******************************************************************
# Info:  Number of ports :                          200
# Info:  Number of nets :                           672
# Info:  Number of instances :                      512
# Info:  Number of references to this view :          0
# Info: Total accumulated area :
# Info:  Number of LUTs :                           135
# Info:  Number of LUTs with LUTNM/HLUTNM :          80
# Info:  Number of MUX CARRYs :                      85
# Info:  Number of accumulated instances :          512
# Info: ****************************
```

- *5x* hardware mínimo
- *Speedup* = 5
- 200 de 210 portas IO

FIM