



Tema 4 - Redução de Imagem

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Ampliação e Redução

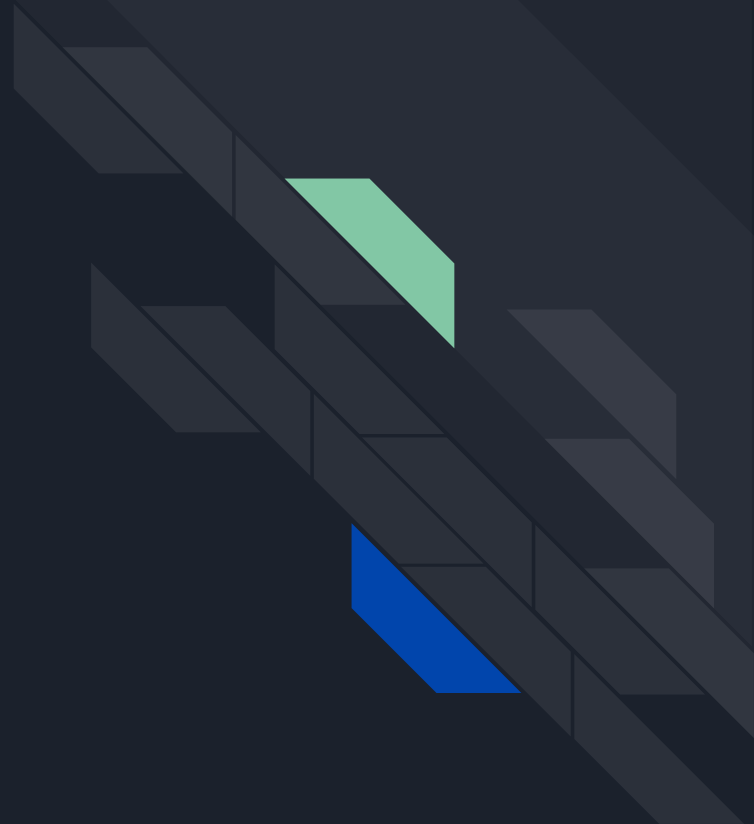
EDA Playground

Programas auxiliares

Simulação

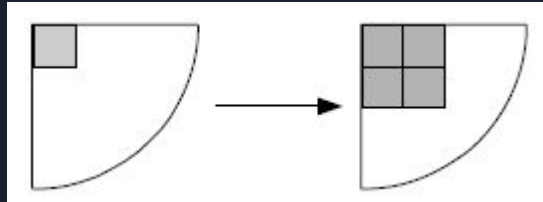
Exemplos

Síntese



Ampliação e Redução

- Ampliação e redução das dimensões da imagem
- *Zoom in* e *Zoom out*
- Ampliação: Duplicar os pixels nos eixos X e Y



- Redução: processo inverso da ampliação
- Perda de informação
- Necessário calcular média

EDA Playground

The screenshot displays the EDA Playground web interface, which is used for simulating digital logic designs. The interface is divided into several sections:

- Top Bar:** Contains the EDA Playground logo and navigation buttons: Run, Save, and Copy.
- Left Panel:** Includes a sidebar with the following sections:
 - Languages & Libraries:** A dropdown menu for 'Testbench + Design' (currently set to 'SystemVerilog/Verilog') and a section for 'UVM / OVM' (currently set to 'None').
 - Other Libraries:** A list of libraries including 'None', 'OVL 2.8.1', and 'SVUnit 2.11'.
 - Tools & Simulators:** A dropdown menu for 'Icarus Verilog 0.10.0 11/23/14'.
 - Compile Options:** A text input field for '-Wall -g2012'.
 - Run Options:** A section with checkboxes for 'Open EPWave after run if not' (checked) and 'downloading files after run' (checked).
 - Examples:** A list of example projects: 'using EDA Playground', 'VHDL', 'Verilog/SystemVerilog', 'UVM', 'EasierUVM', 'SVAUnit', and 'SVUnit'.
- Main Editor:** Displays two files: 'testbench.sv' and 'design.sv'.
 - testbench.sv:** A Verilog testbench for a 160-bit image reduction. It defines a memory array 'Mem' and a module 'read_TXT' that reads from a file 'pix.txt'. It then instantiates 'redux_paralelo' and runs a simulation for 10 time units.
 - design.sv:** A Verilog module 'redux_paralelo' that takes a 160-bit input 'pix_in' and outputs a 160-bit result 'pix_out'. It uses a 'generate' block to instantiate a series of 'redux1' modules.
- Bottom Panel:** A log window showing the compilation and execution process. It includes a 'Log' button and a 'Share' button. The log text shows the creation of a result.zip file and the addition of various files (a.out, redux.txt, pix.txt, run.do, testbench.sv, design.sv) with their respective sizes and compression ratios. The log ends with a 'Done' message.



EDA Playground

- *Online* e gratuito
- Ferramentas de síntese (Mentor Precision 2019.2)
- Ferramentas de simulação (Icarus Verilog 0.10.0)
- Limitações para carregamento de arquivos (100 kB)
 - Resolução da imagem original 160x120 pixels



Programas Auxiliares

- *Pix e Repix*
- Desenvolvidos em C
- Necessários para trabalhar com imagens bitmap
- Pix - Lê bitmap e cria um arquivo TXT com os valores dos pixels em hexadecimal
- Repix - Lê o arquivo de saída do *testbench* com os valores da imagem reduzida e cria a imagem bitmap
- Manipulação do cabeçalho e da paleta de cores

```
C:\Users\Leonardo\Downloads\Universidade\Sistemas Embarcados>Pix.exe u4.bmp
Tamanho: 20346
Offset dados bitmap: 1146
Comprimento: 160
Altura: 120
Size image: 19200
No. de cores usadas: 256
No. de bits por pixel: 8
Compressao: 0
```

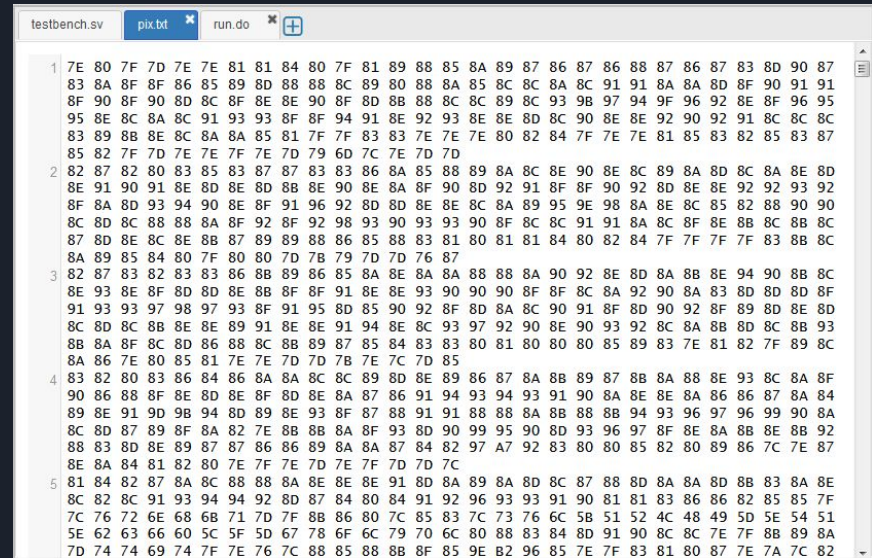


Programas Auxiliares

```
C:\Users\Leonardo\Downloads\Universidade\Sistemas Embarcados>Repix.exe u4.bmp re  
dux.txt 0.5  
Tamanho: 20346  
Offset dados bitmap: 1146  
Comprimento: 160  
Altura: 120  
Size image: 19200  
No. de cores usadas: 256  
No. de bits por pixel: 8  
Compressao: 0  
  
Tamanho: 5946  
Offset dados bitmap: 1146  
Comprimento: 80  
Altura: 60  
Size image: 4800  
No. de cores usadas: 256  
No. de bits por pixel: 8  
Compressao: 0
```

Simulação

- *Icarus Verilog 0.10.0 11/23/14*
- Entrada *pix.txt*
 - Valores em hexadecimal
- *Testbench*
- *Design*
- Saída *redux.txt*
- “download files after run”



The screenshot shows the Icarus Verilog simulation window. The top bar displays three tabs: 'testbench.sv', 'pix.txt' (active), and 'run.do'. The main window contains a large block of hexadecimal data, organized into rows and columns. The data is presented in a grid-like format, with each row starting with a line number (e.g., 1, 2, 3, 4, 5) and followed by a sequence of hexadecimal values. The values are arranged in a way that suggests they are being read from a file or a memory dump. The data is presented in a grid-like format, with each row starting with a line number (e.g., 1, 2, 3, 4, 5) and followed by a sequence of hexadecimal values. The values are arranged in a way that suggests they are being read from a file or a memory dump.

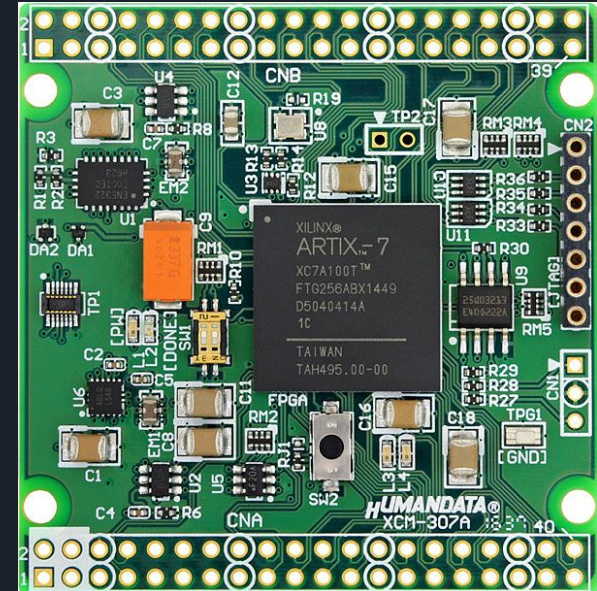
Exemplos



Síntese

- *Mentor Precision 2019.2*
- *Script run.do*
- Dispositivo 7A100TCSG324 da família Artix-7 da Xilinx
- *Design*
- *Log e vários arquivos de saída*

```
testbench.sv  pix.txt  run.do  +
1  setup_design -manufacturer Xilinx -family Artix-7 -part 7A100TCSG324
2  foreach arg $::argv {
3    add_input_file $arg
4  }
5
6  #Setup timing constraints
7  setup_design -frequency 1000
8
9  compile
10 synthesize
11 auto_write precision.v
12 report_output_file_list
13 report_area
14 report_timing
15 exec cat precision.v
16
```

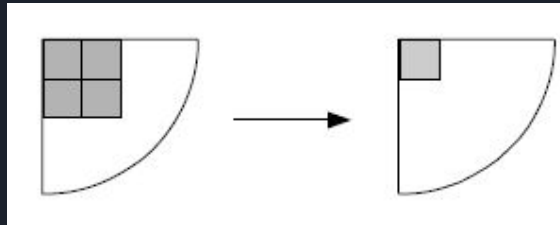
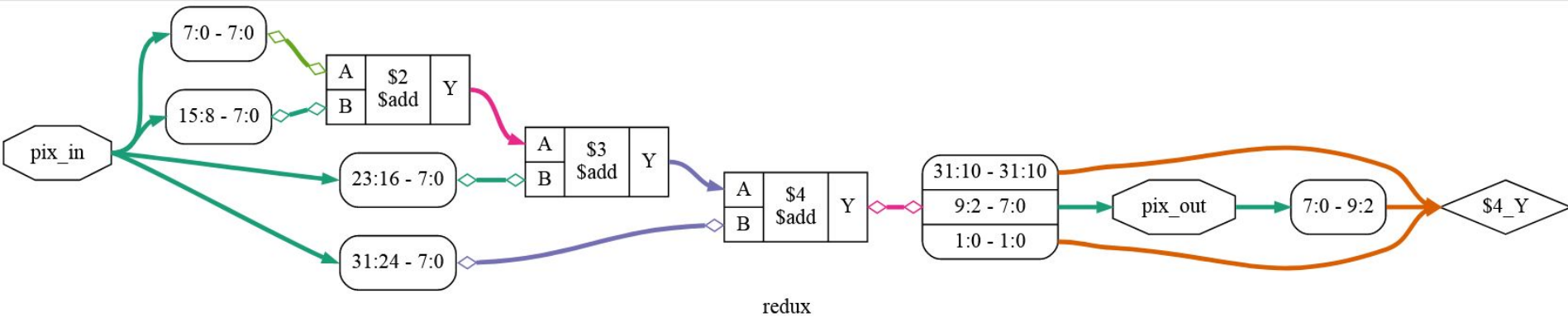


Síntese - Minimização do Hardware

```
# Info: *****
# Info: Device Utilization for 7A100TCSG324
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: I/Os                    40      210     19.05%
# Info: Global Buffers          0       32      0.00%
# Info: LUTs                     27    63400    0.04%
# Info: CLB Slices               0    15850    0.00%
# Info: DFFs or Latches          0   126800    0.00%
# Info: Block RAMs               0     135    0.00%
# Info: DSP48E1s                 0     240    0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: redux    View: INTERFACE
# Info: *****
# Info: Number of ports :                40
# Info: Number of nets :                136
# Info: Number of instances :            104
# Info: Number of references to this view :    0
# Info: Total accumulated area :
# Info: Number of LUTs :                27
# Info: Number of LUTs with LUTNM/HLUTNM :    16
# Info: Number of MUX CARRYs :          17
# Info: Number of accumulated instances :    104
# Info: *****
```

Síntese - Esquemático

- Yosys 0.9.0



Síntese - Maximização do Throughput

```
# Info: *****
# Info: Device Utilization for 7A100TCSG324
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: IOs                    200     210     95.24%
# Info: Global Buffers         0        32      0.00%
# Info: LUTs                   135    63400    0.21%
# Info: CLB Slices              0     15850    0.00%
# Info: Dffs or Latches         0    126800    0.00%
# Info: Block RAMs              0        135    0.00%
# Info: DSP48E1s                0        240    0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: redux_paralelo    View: INTERFACE
# Info: *****
# Info: Number of ports :                200
# Info: Number of nets :                672
# Info: Number of instances :            512
# Info: Number of references to this view :      0
# Info: Total accumulated area :
# Info: Number of LUTs :                135
# Info: Number of LUTs with LUTNM/HLUTNM :      80
# Info: Number of MUX CARRYS :           85
# Info: Number of accumulated instances :    512
# Info: *****
```

- 5x hardware mínimo
- *Speedup* = 5
- 200 de 210 portas IO



FIM