



# Tema 4 - Redução de Imagem

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Ampliação e Redução

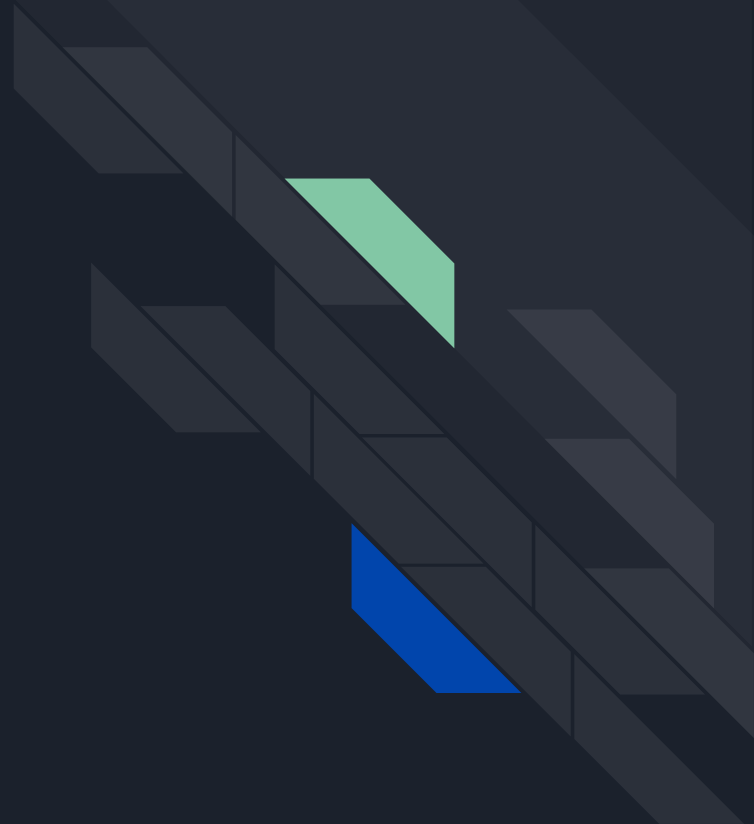
EDA Playground

Programas auxiliares

Simulação

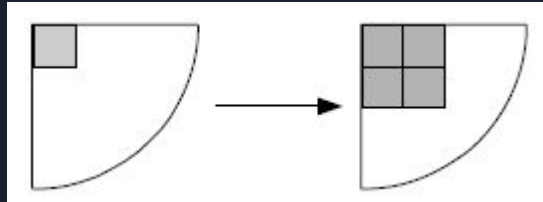
Exemplos

Síntese



# Ampliação e Redução

- Ampliação e redução das dimensões da imagem
- *Zoom in* e *Zoom out*
- Ampliação: Duplicar os pixels nos eixos X e Y



- Redução: processo inverso da ampliação
- Perda de informação
- Necessário calcular média

# EDA Playground

The screenshot displays the EDA Playground web interface. The top navigation bar includes 'Run', 'Save', and 'Copy' buttons. The left sidebar contains a 'Languages & Libraries' section with 'Testbench + Design' selected, showing 'SystemVerilog/Verilog' and 'UVM / OVM' options. Below this is a 'Tools & Simulators' section with 'Icarus Verilog 0.10.0 11/23/14' selected. The main area is split into two panels: 'testbench.v' on the left and 'design.v' on the right. The 'testbench.v' panel contains Verilog code for a testbench, including file operations and memory allocation. The 'design.v' panel contains Verilog code for a hardware module named 'redux\_paralelo'. The bottom panel shows a 'Log' section with a timestamped message: '[2020-11-22 14:47:57 EST] Icarus Verilog 'wall' '-g2012' design.v testbench.v && unbuffer vvp a.out'. Below this, a list of files being added to the result.zip is shown, including 'a.out', 'redux.txt', 'pix.txt', 'run.do', 'testbench.v', and 'design.v'. The log concludes with '[2020-11-22 14:47:58 EST] waiting for download...' and 'Done'.

EDA playground

Run Save Copy

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Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM

None

Other Libraries

None

OVL 2.8.1

SVUnit 2.11

Enable TL-Verilog

Enable Easier UVM

Enable VUnit

Tools & Simulators

Icarus Verilog 0.10.0 11/23/14

Compile Options

-Wall -g2012

Run Options

Run Options

Open EPWave after run if not

downloading files after run

Examples

using EDA Playground

VHDL

Verilog/SystemVerilog

UVM

EasierUVM

SVUnit

SVUnit

testbench.v

```
1 //testbench
2 .define height 120
3 .define width 160
4 module read_TXT;
5
6 reg [7:0] Mem [0:'height-1][0:'width-1]; //Memória
7 integer i, j, count;
8 integer file_out;
9 reg [7:0] in[0:3][0:4];
10 reg [7:0] out[0:4];
11
12
13 redux_paralelo rp_1(.pix_in(in), .pix_out(out));
14
15 initial begin
16 $readmemh("pix.txt", Mem); //Carrega imagem
17 file_out = $fopen("redux.txt", "w");
18 count = 0;
19 end
20
21 initial begin
22 #10;
23 for (i=0; i<'height; i=i+2) begin
24   for (j=0; j<'width; j=j+2)begin
```

design.v

```
1 //Hardware
2 module redux_paralelo(
3   input [7:0] pix_in[0:3][0:4],
4   output reg [7:0] pix_out[0:4]);
5
6   genvar i;
7
8   generate
9     for (i=0; i<4; i=i+1) begin : redux1
10       always @ (pix_in[0][i] or pix_in[1][i] or pix_in[2][i] or pix_in[3][i]) begin
11         pix_out[i] <= (pix_in[0][i] + pix_in[1][i] + pix_in[2][i] + pix_in[3][i]) / 4;
12       end //end always
13     end //end for i
14   endgenerate
15
16 endmodule
```

Log

Share

[2020-11-22 14:47:57 EST] Icarus Verilog 'wall' '-g2012' design.v testbench.v && unbuffer vvp a.out

Creating result.zip...

adding: a.out (deflated 83%)

adding: redux.txt (deflated 99%)

adding: pix.txt (deflated 69%)

adding: run.do (deflated 27%)

adding: testbench.v (deflated 53%)

adding: design.v (deflated 49%)

[2020-11-22 14:47:58 EST] waiting for download...

Done



# EDA Playground



- *Online* e gratuito
- Ferramentas de síntese (Mentor Precision 2019.2)
- Ferramentas de simulação (Icarus Verilog 0.10.0)
- Limitações para carregamento de arquivos (100 kB)
  - Resolução da imagem original 160x120 pixels



# Programas Auxiliares

- *Pix* e *Repix*
- Desenvolvidos em C
- Necessários para trabalhar com imagens bitmap
- *Pix* - Lê bitmap e cria um arquivo TXT com os valores dos pixels em hexadecimal
- *Repix* - Lê o arquivo de saída do *testbench* com os valores da imagem reduzida e cria a imagem bitmap
- Manipulação do cabeçalho e da paleta de cores

```
C:\Users\Leonardo\Downloads\Universidade\Sistemas Embarcados>Pix.exe u4.bmp
Tamanho: 20346
Offset dados bitmap: 1146
Comprimento: 160
Altura: 120
Size image: 19200
No. de cores usadas: 256
No. de bits por pixel: 8
Compressao: 0
```

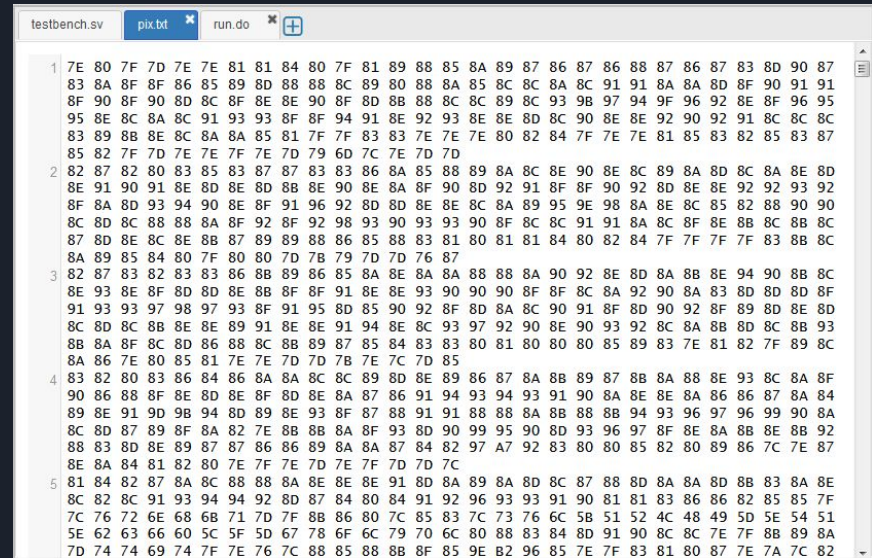


# Programas Auxiliares

```
C:\Users\Leonardo\Downloads\Universidade\Sistemas Embarcados>Repix.exe u4.bmp re  
dux.txt 0.5  
Tamanho: 20346  
Offset dados bitmap: 1146  
Comprimento: 160  
Altura: 120  
Size image: 19200  
No. de cores usadas: 256  
No. de bits por pixel: 8  
Compressao: 0  
  
Tamanho: 5946  
Offset dados bitmap: 1146  
Comprimento: 80  
Altura: 60  
Size image: 4800  
No. de cores usadas: 256  
No. de bits por pixel: 8  
Compressao: 0
```

# Simulação

- Icarus Verilog 0.10.0 11/23/14
- Entrada *pix.txt*
  - Valores em hexadecimal
- Testbench
- Design
- Saída *redux.txt*
- “download files after run”



The screenshot shows the Icarus Verilog simulation window. The top bar displays the file names: `testbench.sv`, `pix.txt` (active), and `run.do`. The main window contains a large block of hexadecimal data, organized into columns and rows, representing the simulation output. The data is displayed in a monospaced font, with line numbers visible on the left side of the output.

```
1 7E 80 7F 7D 7E 7E 81 81 84 80 7F 81 89 88 85 8A 89 87 86 87 86 88 87 86 87 83 8D 90 87
83 8A 8F 8F 86 85 89 8D 88 88 8C 89 80 88 8A 85 8C 8C 8A 8C 91 91 8A 8A 8D 8F 90 91 91
8F 90 8F 90 8D 8C 8F 8E 8E 90 8F 8D 88 88 8C 8C 89 8C 93 9B 97 94 9F 96 92 8E 8F 96 95
95 8E 8C 8A 8C 91 93 93 8F 8F 94 91 8E 92 93 8E 8E 8D 8C 90 8E 8E 92 90 92 91 8C 8C 8C
83 89 88 8E 8C 8A 8A 85 81 7F 7F 83 83 7E 7E 80 82 84 7F 7E 7E 81 85 83 82 85 83 87
85 82 7F 7D 7E 7E 7F 7E 7D 79 6D 7C 7E 7D 7D
2 82 87 82 80 83 85 83 87 87 83 83 86 8A 85 88 89 8A 8C 8E 90 8E 8C 89 8A 8D 8C 8A 8E 8D
8E 91 90 91 8E 8D 8E 8D 88 8E 90 8E 8A 8F 90 8D 92 91 8F 8F 90 92 8D 8E 8E 92 92 93 92
8F 8A 8D 93 94 90 8E 8F 91 96 92 8D 8D 8E 8E 8C 8A 89 95 9E 98 8A 8E 8C 85 82 88 90 90
8C 8D 8C 88 88 8A 8F 92 8F 92 98 93 90 93 93 90 8F 8C 8C 91 91 8A 8C 8F 8E 8B 8C 8B 8C
87 8D 8E 8C 8E 88 87 89 89 88 86 85 88 83 81 80 81 81 84 80 82 84 7F 7F 7F 7F 83 8B 8C
8A 89 85 84 80 7F 80 80 7D 7B 79 7D 7D 76 87
3 82 87 83 82 83 83 86 8B 89 86 85 8A 8E 8A 8A 88 88 8A 90 92 8E 8D 8A 8B 8E 94 90 8B 8C
8E 93 8E 8F 8D 8D 8E 8B 8F 8F 91 8E 8E 93 90 90 90 8F 8F 8C 8A 92 90 8A 83 8D 8D 8D 8F
91 93 93 97 98 97 93 8F 91 95 8D 85 90 92 8F 8D 8A 8C 90 92 8F 8D 90 92 8F 89 8D 8E 8D
8C 8D 8C 8B 8E 8E 89 91 8E 8E 91 94 8E 8C 93 97 92 90 8E 90 93 92 8C 8A 8B 8D 8C 8B 93
8B 8A 8F 8C 8D 86 88 8C 8B 89 87 85 84 83 83 80 81 80 80 80 85 89 83 7E 81 82 7F 89 8C
8A 86 7E 80 85 81 7E 7E 7D 7D 7B 7E 7C 7D 85
4 83 82 80 83 86 84 86 8A 8A 8C 8C 89 8D 8E 89 86 87 8A 8B 89 87 8B 8A 88 8E 93 8C 8A 8F
90 86 88 8F 8E 8D 8E 8F 8D 8E 8A 87 86 91 94 93 94 93 91 90 8A 8E 8E 8A 86 86 87 8A 84
89 8E 91 9D 9B 94 8D 89 8E 93 8F 87 88 91 91 88 88 8A 8B 88 88 94 93 96 97 96 99 90 8A
8C 8D 87 89 8F 8A 82 7E 8B 8B 8A 8F 93 8D 90 99 95 90 8D 93 96 97 8F 8E 8A 8B 8E 8B 92
88 83 8D 8E 89 87 87 86 86 89 8A 8A 87 84 82 97 A7 92 83 80 80 85 82 80 89 86 7C 7E 87
8E 8A 84 81 82 80 7E 7F 7E 7D 7E 7F 7D 7D 7C
5 81 84 82 87 8A 8C 88 88 8A 8E 8E 8E 91 8D 8A 89 8A 8D 8C 87 88 8D 8A 8A 8D 8B 83 8A 8E
8C 82 8C 91 93 94 94 92 8D 87 84 80 84 91 92 96 93 93 91 90 81 81 83 86 86 82 85 85 7F
7C 76 72 6E 68 68 71 7D 7F 8B 86 80 7C 85 83 7C 73 76 6C 5B 51 52 4C 48 49 5D 5E 54 51
5E 62 63 66 60 5C 5F 5D 67 78 6F 6C 79 70 6C 80 88 83 84 8D 91 90 8C 8C 7E 7F 8B 89 8A
7D 74 74 69 74 7F 7E 76 7C 88 85 88 8B 8F 85 9E B2 96 85 7E 7F 83 81 80 87 7E 7A 7C 82
```



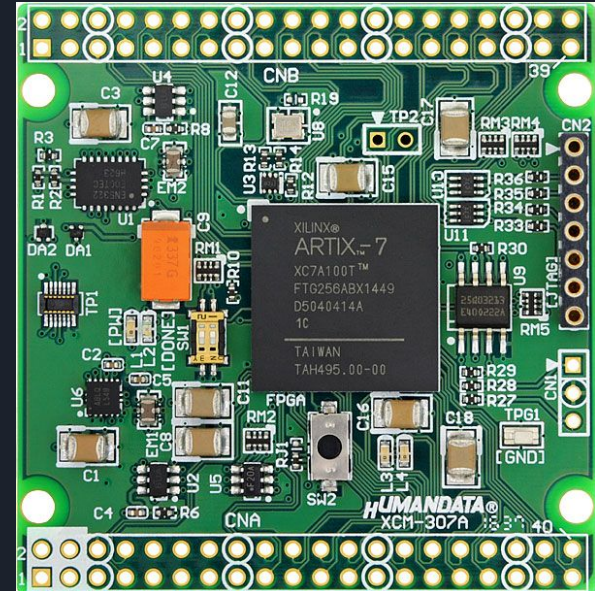
# Exemplos



# Síntese

- *Mentor Precision 2019.2*
- *Script run.do*
- Dispositivo 7A100TCSG324 da família Artix-7 da Xilinx
- *Design*
- *Log e vários arquivos de saída*

```
testbench.sv  pix.txt  run.do  +
1  setup_design -manufacturer Xilinx -family Artix-7 -part 7A100TCSG324
2  foreach arg $::argv {
3    add_input_file $arg
4  }
5
6  #Setup timing constraints
7  setup_design -frequency 1000
8
9  compile
10 synthesize
11 auto_write precision.v
12 report_output_file_list
13 report_area
14 report_timing
15 exec cat precision.v
16
```

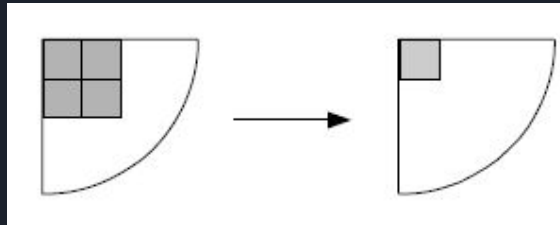
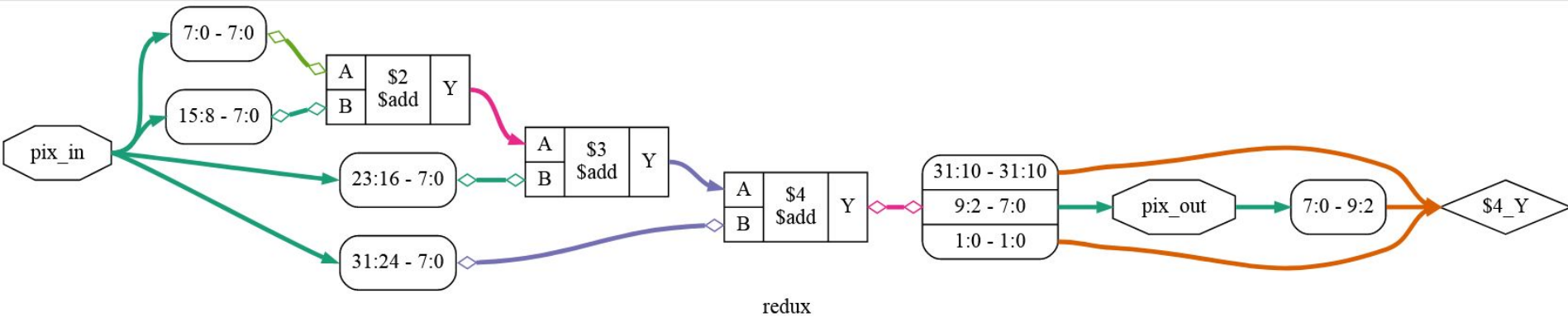


# Síntese - Minimização do Hardware

```
# Info: *****
# Info: Device Utilization for 7A100TCSG324
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: I/Os                    40      210      19.05%
# Info: Global Buffers          0       32       0.00%
# Info: LUTs                     27    63400      0.04%
# Info: CLB Slices               0    15850      0.00%
# Info: DFFs or Latches          0   126800      0.00%
# Info: Block RAMs               0     135      0.00%
# Info: DSP48E1s                 0     240      0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: redux    View: INTERFACE
# Info: *****
# Info: Number of ports :                40
# Info: Number of nets :                136
# Info: Number of instances :            104
# Info: Number of references to this view :      0
# Info: Total accumulated area :
# Info: Number of LUTs :                27
# Info: Number of LUTs with LUTNM/HLUTNM :      16
# Info: Number of MUX CARRYs :          17
# Info: Number of accumulated instances :      104
# Info: *****
```

# Síntese - Esquemático

- Yosys 0.9.0



# Síntese - Maximização do Throughput

```
# Info: *****
# Info: Device Utilization for 7A100TCSG324
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: I/Os                    200     210     95.24%
# Info: Global Buffers          0        32     0.00%
# Info: LUTs                     108    63400    0.17%
# Info: CLB Slices               0     15850    0.00%
# Info: DFFs or Latches          0    126800    0.00%
# Info: Block RAMs               0       135    0.00%
# Info: DSP48E1s                 0       240    0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: redux_paralelo    View: INTERFACE
# Info: *****
# Info: Number of ports :                200
# Info: Number of nets :                546
# Info: Number of instances :            418
# Info: Number of references to this view :      0
# Info: Total accumulated area :
# Info: Number of LUTs :                108
# Info: Number of LUTs with LUTNM/HLUTNM :      64
# Info: Number of MUX CARRYS :           68
# Info: Number of accumulated instances :      418
# Info: *****
```

- 5x hardware mínimo
- *Speedup* = 5
- 200 de 210 portas IO



FIM