

**Folha de Dados**  
**Primeira Lista de Exercícios**  
**Circuitos Sequenciais e Projeto RTL**

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**Matrícula:** 15/0039921

**EXERCÍCIO 1: Ping-pong LEDS**

**1) Diagrama de blocos proposto**

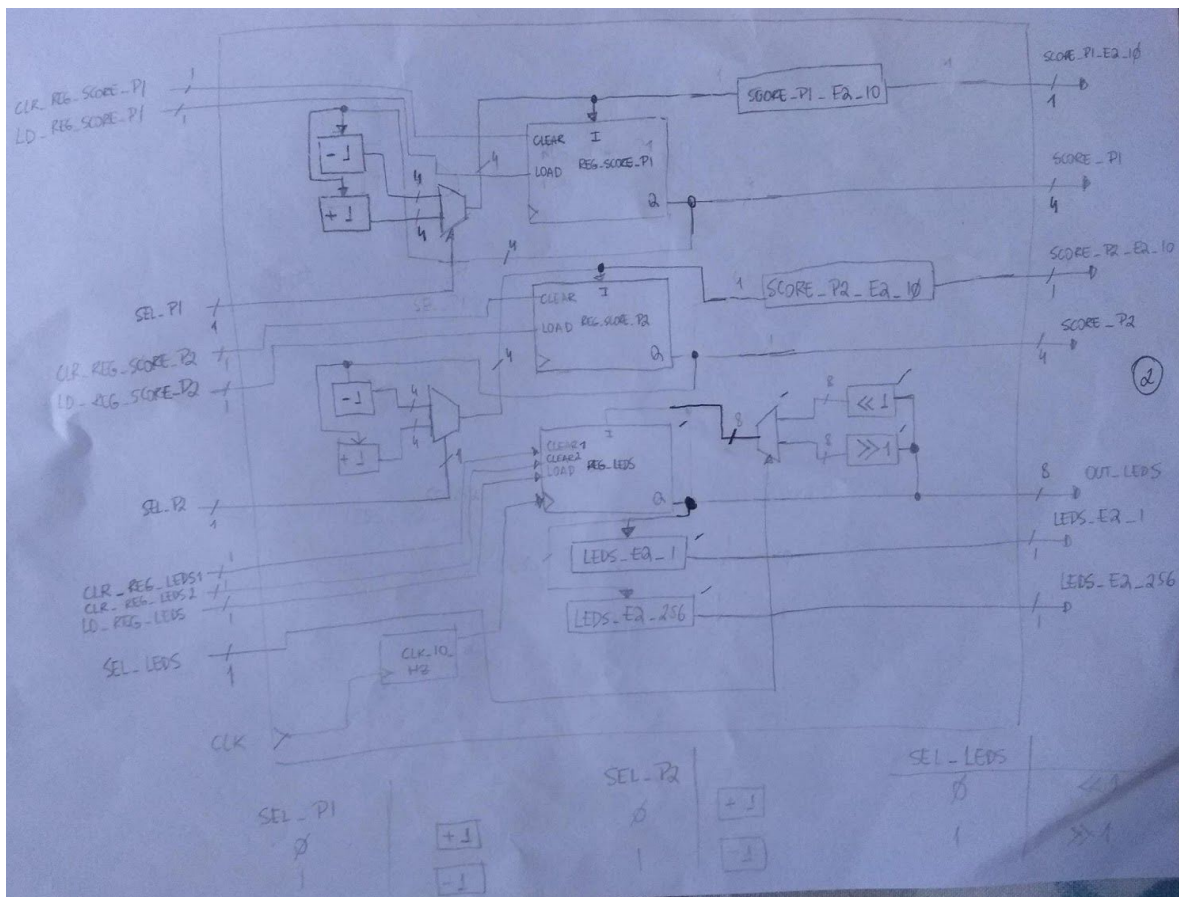


Figura 1.1 - Bloco Operacional do Ping pong leds

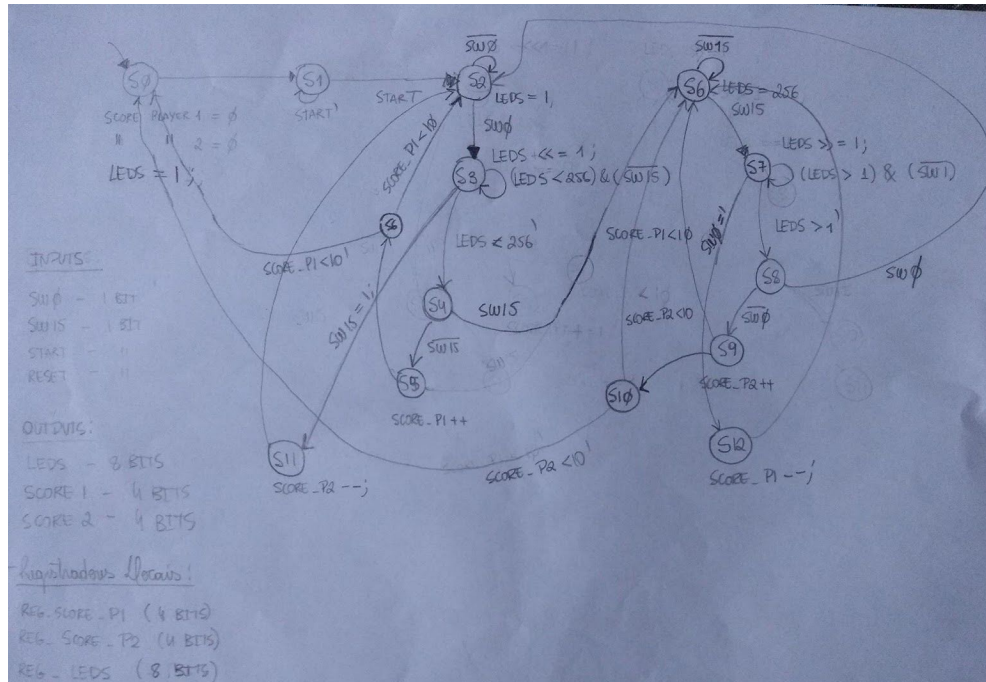


Figura 1.2 - Bloco de Controle do Ping pong leds

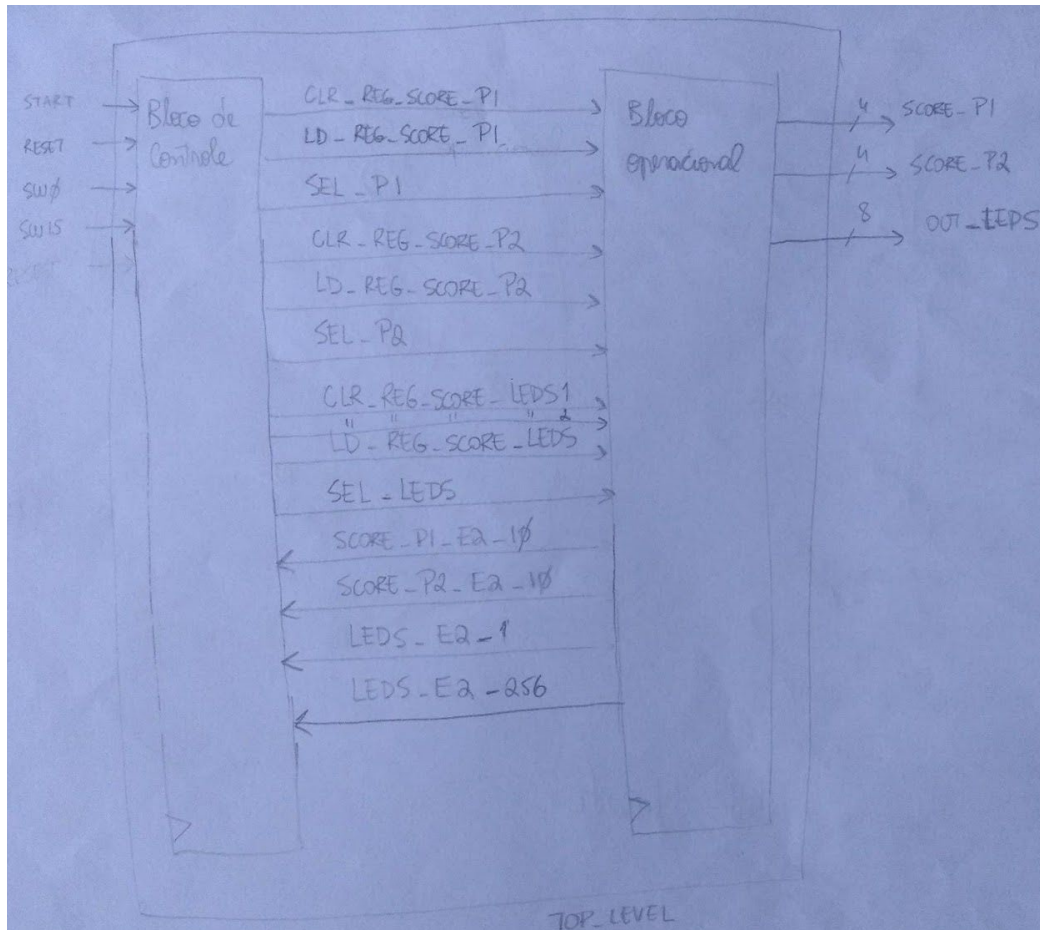


Figura 1.3 - Top level do ping-pong leds

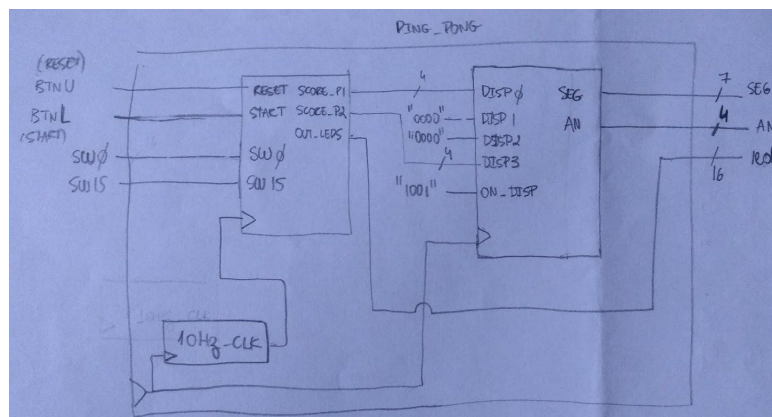


Figura 1.4 - Diagrama final do bloco ping-pong

## 2) Diagrama Esquemático (Análise RTL pré-síntese)

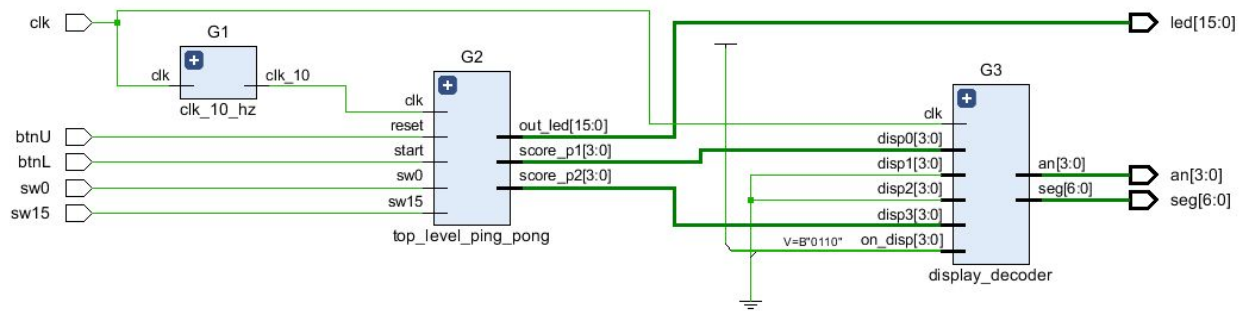


Figura 1.5 - Diagrama Esquemático do top\_ping-pong

### 3) Estimação de consumo de recursos lógicos após a síntese lógica

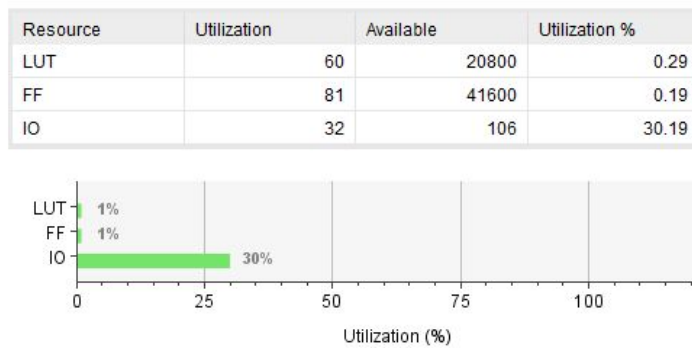


Figura 1.6 - Estimação de consumo de recursos após síntese lógica do top\_ping\_pong

### 4) Estimação de recursos após implementação (processo Place and Route - PAR)

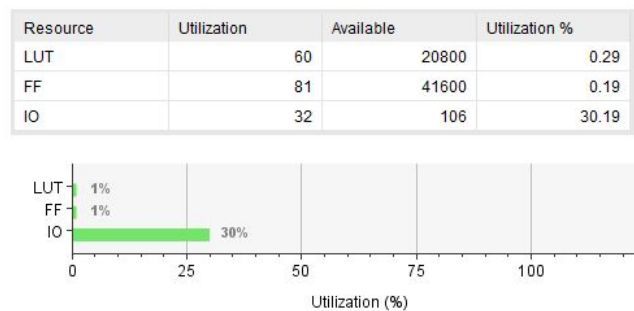


Figura 1.7 - Estimação de recursos após a implementação

### 5) Análise de Timing



## Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5,868 ns	Worst Hold Slack (WHS): 0,228 ns	Worst Pulse Width Slack (WPWS): 4,500 ns
Total Negative Slack (TNS): 0,000 ns	Total Hold Slack (THS): 0,000 ns	Total Pulse Width Negative Slack (TPWS): 0,000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 84	Total Number of Endpoints: 84	Total Number of Endpoints: 44

All user specified timing constraints are met.

Name	Waveform	Period (ns)	Frequency (MHz)
sys_clk_pin	{0.000 5.000}	10.000	100.000

### Intra-Clock Paths - sys\_clk\_pin - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay
Path 1	5.868	3	4	23	G1/sum_reg[15]/C	G1/sum_reg[0]/R	3.546	0.890	2.656
Path 2	5.868	3	4	23	G1/sum_reg[15]/C	G1/sum_reg[1]/R	3.546	0.890	2.656
Path 3	5.868	3	4	23	G1/sum_reg[15]/C	G1/sum_reg[2]/R	3.546	0.890	2.656
Path 4	5.868	3	4	23	G1/sum_reg[15]/C	G1/sum_reg[3]/R	3.546	0.890	2.656
Path 5	6.010	3	4	23	G1/sum_reg[15]/C	G1/sum_reg[4]/R	3.405	0.890	2.515
Path 6	6.010	3	4	23	G1/sum_reg[15]/C	G1/sum_reg[5]/R	3.405	0.890	2.515
Path 7	6.010	3	4	23	G1/sum_reg[15]/C	G1/sum_reg[6]/R	3.405	0.890	2.515
Path 8	6.010	3	4	23	G1/sum_reg[15]/C	G1/sum_reg[7]/R	3.405	0.890	2.515
Path 9	6.022	3	4	18	G3/G3/sum_reg[3]/C	G3/G3/sum_reg[0]/R	3.514	0.828	2.686
Path 10	6.022	3	4	18	G3/G3/sum_reg[3]/C	G3/G3/sum_reg[1]/R	3.514	0.828	2.686

### Intra-Clock Paths - sys\_clk\_pin - Hold

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay
Path 11	0.228	1	1	3	G1/sum_reg[22]/C	G1/s_clk_out_reg/D	0.334	0.209	0.125
Path 12	0.241	1	1	3	G3/G3/sum_reg[13]/C	G3/G3/s_clk_out_reg/D	0.345	0.186	0.159
Path 13	0.265	1	1	2	G1/sum_reg[10]/C	G1/sum_reg[10]/D	0.399	0.274	0.125
Path 14	0.267	1	1	3	G1/sum_reg[22]/C	G1/sum_reg[22]/D	0.401	0.274	0.127
Path 15	0.267	1	1	2	G1/sum_reg[6]/C	G1/sum_reg[6]/D	0.401	0.274	0.127
Path 16	0.277	1	1	3	G1/sum_reg[18]/C	G1/sum_reg[18]/D	0.411	0.274	0.137
Path 17	0.277	1	1	3	G1/sum_reg[14]/C	G1/sum_reg[14]/D	0.411	0.274	0.137
Path 18	0.280	1	1	2	G3/G3/sum_reg[10]/C	G3/G3/sum_reg[10]/D	0.385	0.252	0.133
Path 19	0.280	1	1	2	G3/G3/sum_reg[14]/C	G3/G3/sum_reg[14]/D	0.385	0.252	0.133
Path 20	0.280	1	1	2	G3/G3/sum_reg[2]/C	G3/G3/sum_reg[2]/D	0.385	0.252	0.133

Figura 1.8 - Análise de Timing após a implementação

6) Layout do circuito após a implementação (após o processo Place and Route – PAR)

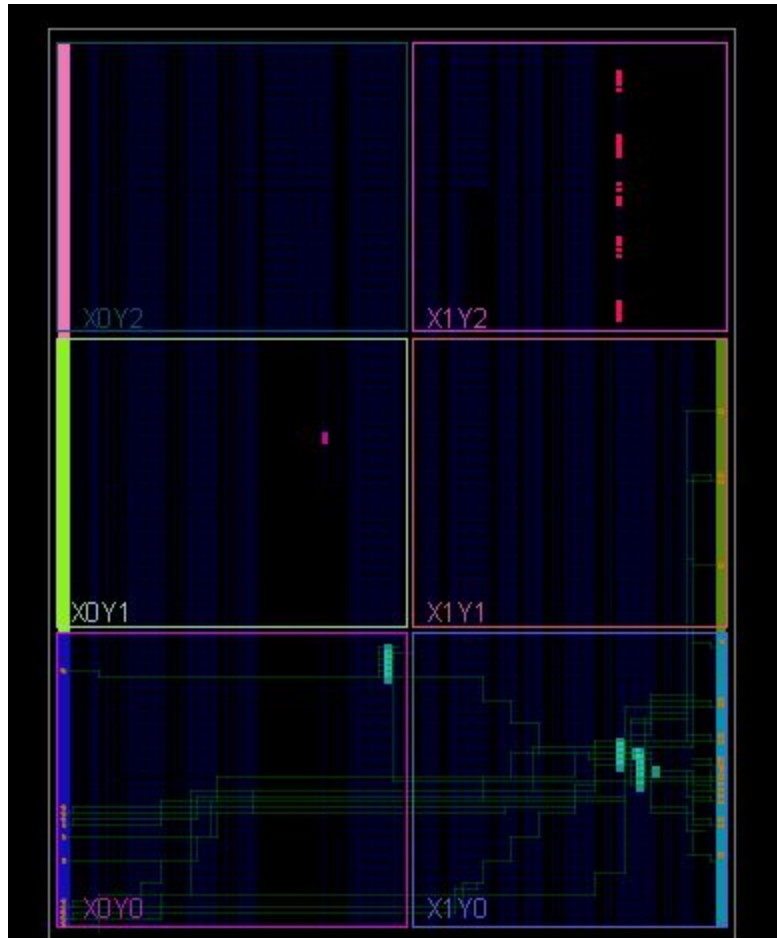


Figura 1.9 - Layout do circuito após a implementação

## 7) Estimação do consumo de energia após a implementação do circuito

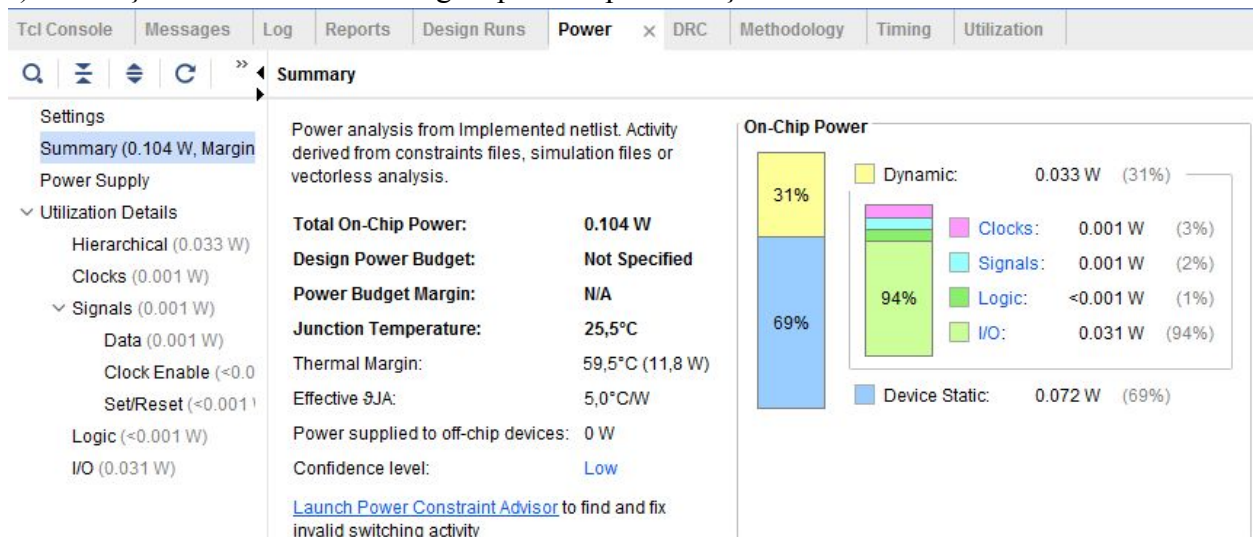


Figura 1.10 - Estimação do consumo de energia do bloco top\_ping\_pong

## Exercício 2: Ping-pong LEDS FSM

### 1) Diagrama de blocos proposto

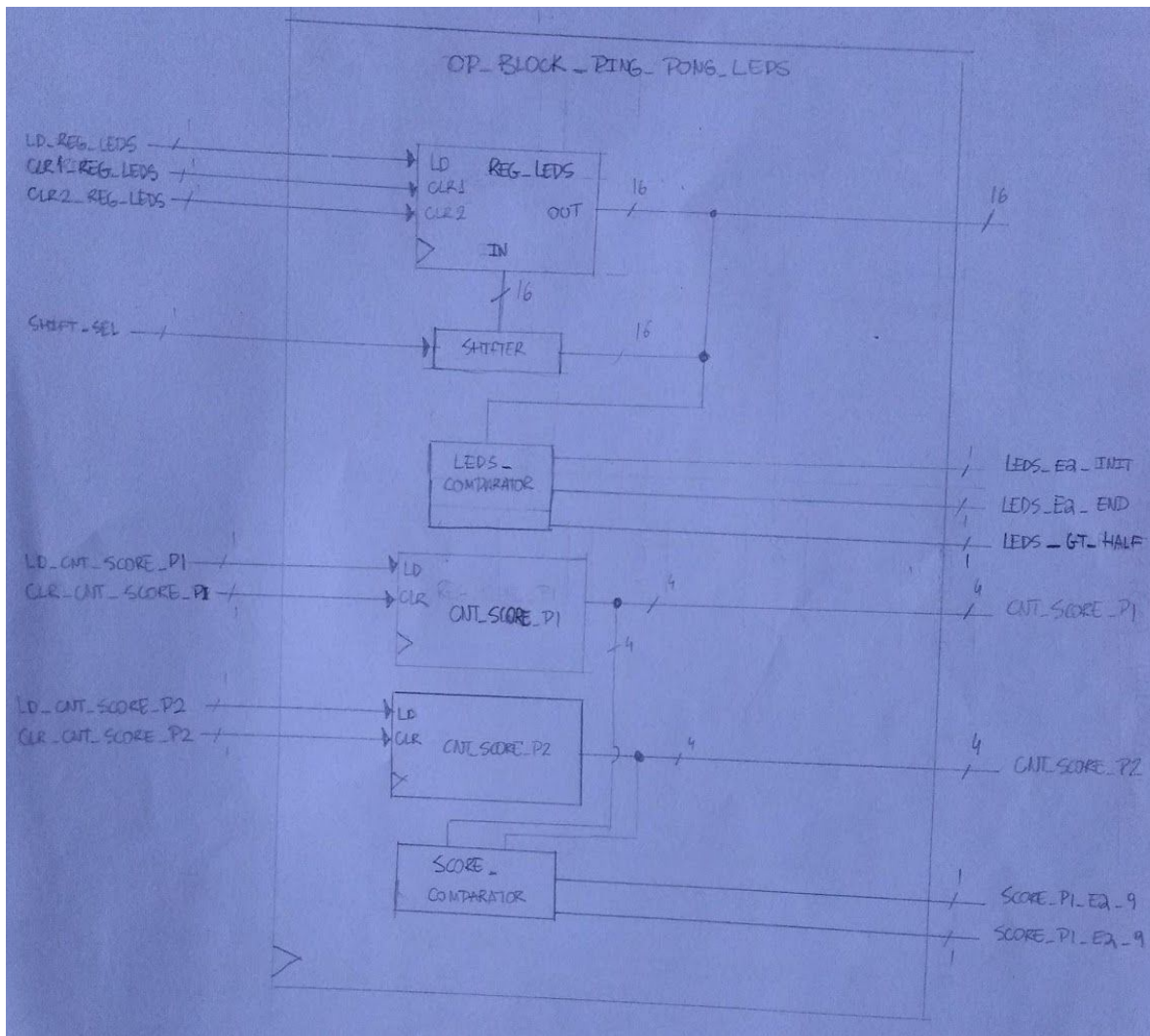


Figura 2.1 - Bloco Operacional do Ping-Pong



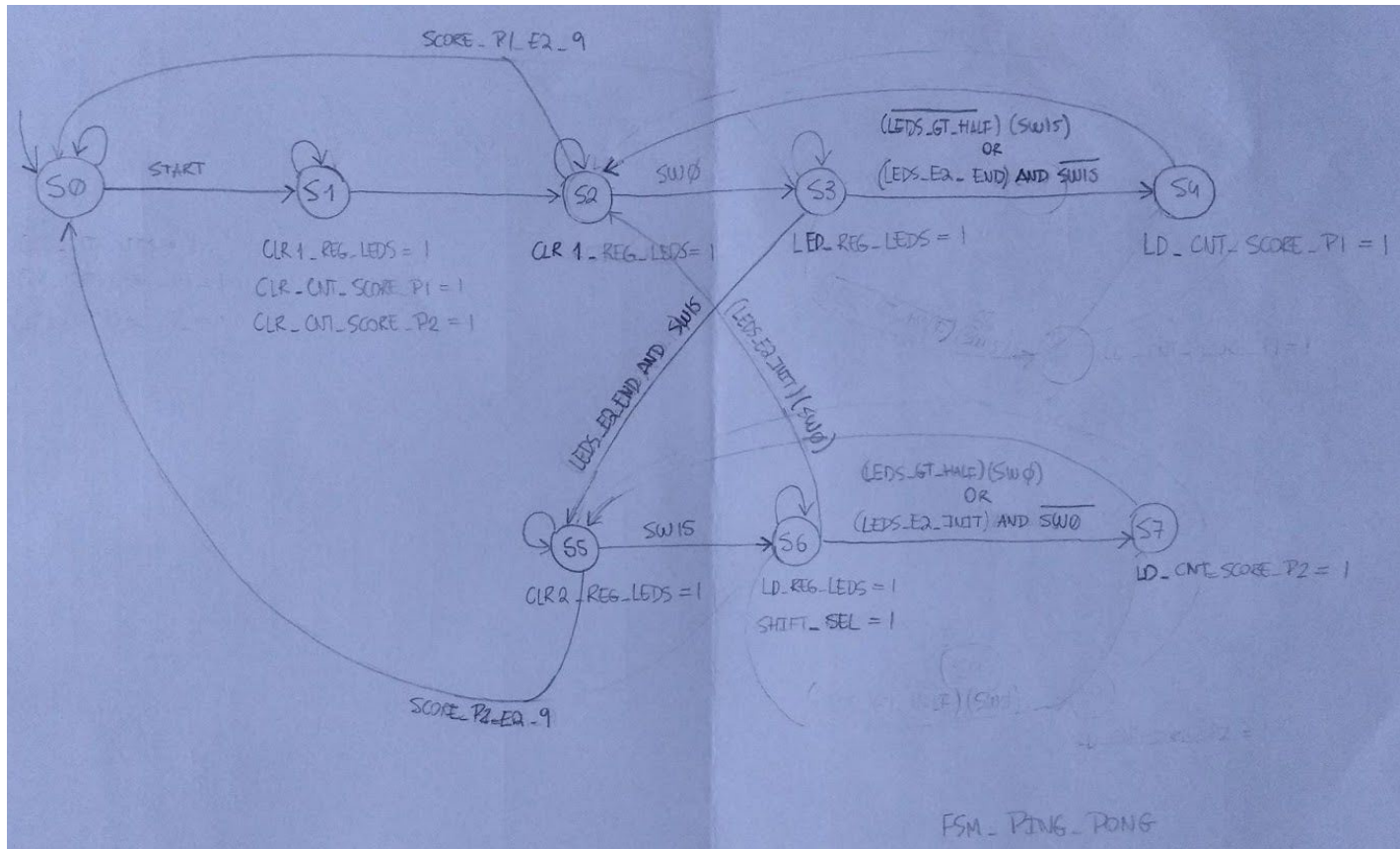


Figura 2.2 - Máquina de estados utilizada para controlar o bloco operacional, chamada de fsm\_ping\_pong

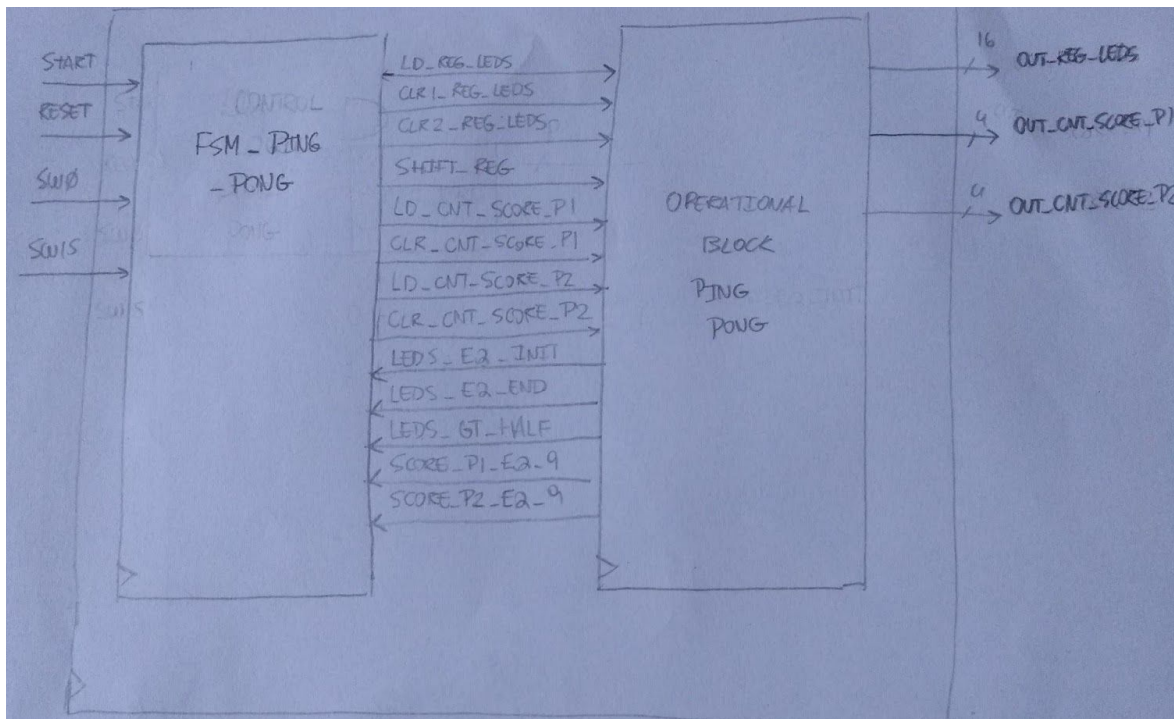




Figura 2.3 - Conexão do bloco operacional com a máquina de estados, gerando o component ping-pong

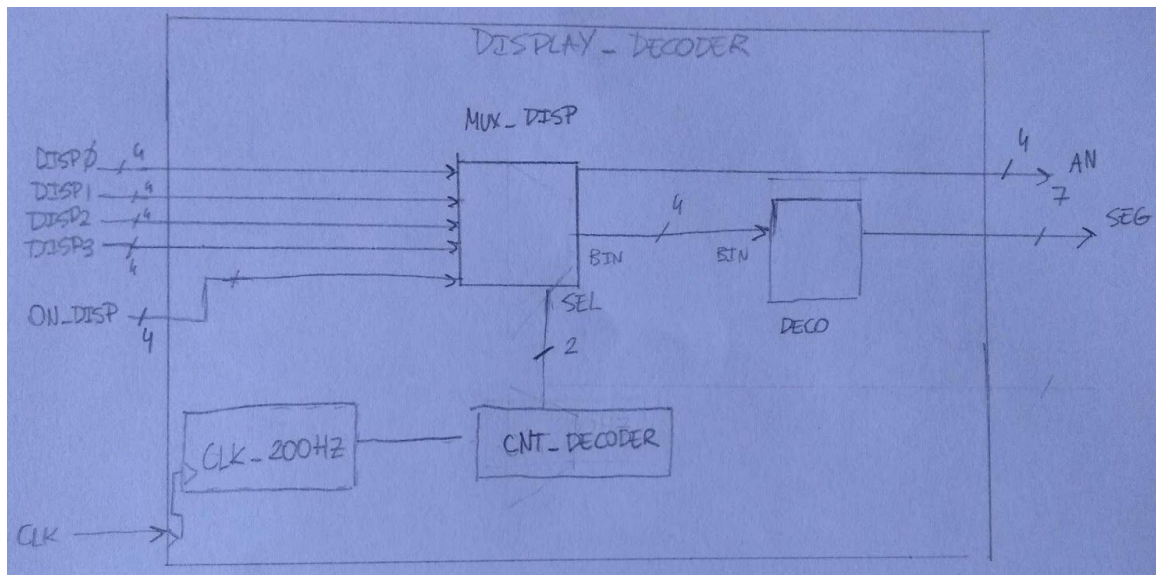


Figura 2.4 - Decodificador e multiplexador para os displays de 7 segmentos da placa basys 3

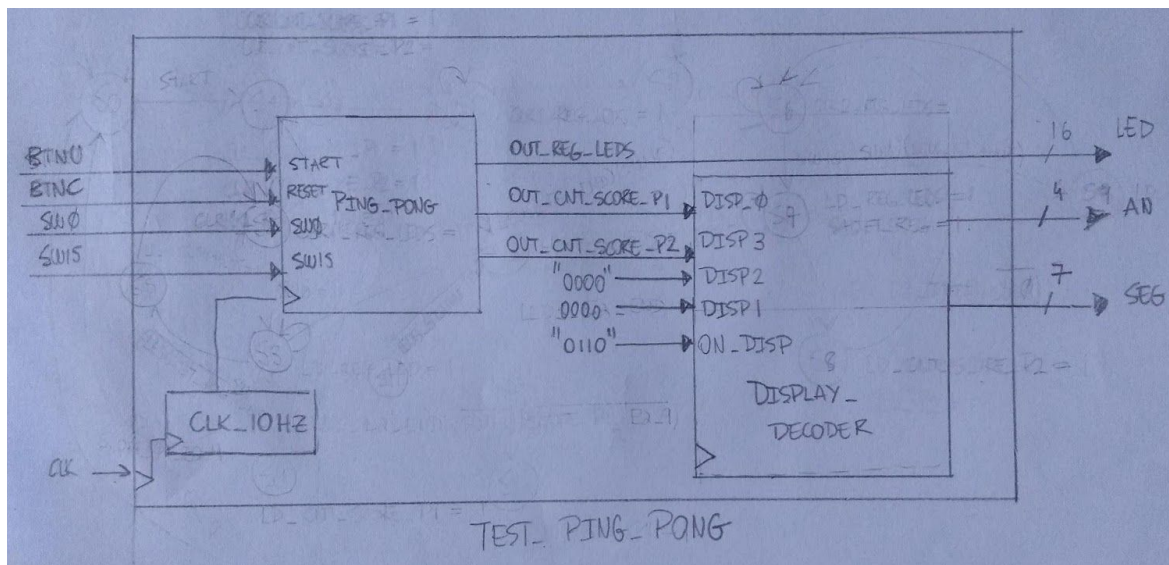


Figura 2.5 - Diagrama final chamado de test\_ping\_pong para teste na placa de desenvolvimento Basys 3, conectando o bloco display\_decoder com o bloco ping\_pong

## 2) Diagrama Esquemático (Análise RTL pré-síntese)

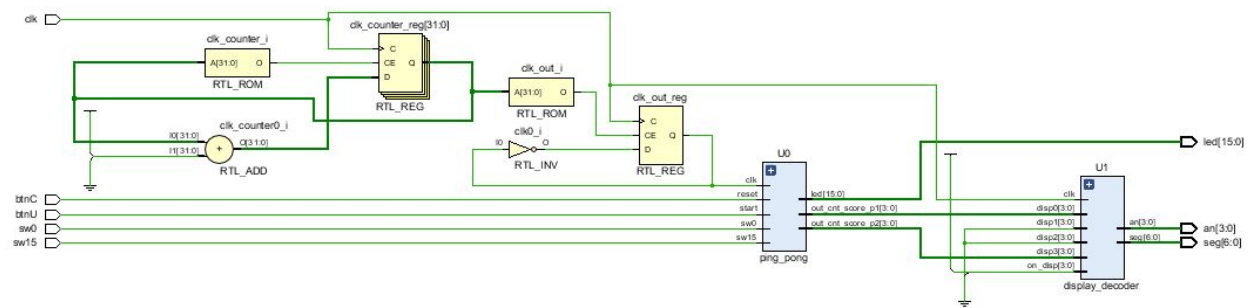


Figura 2.6 - Diagrama Esquemático do bloco test\_ping\_pong

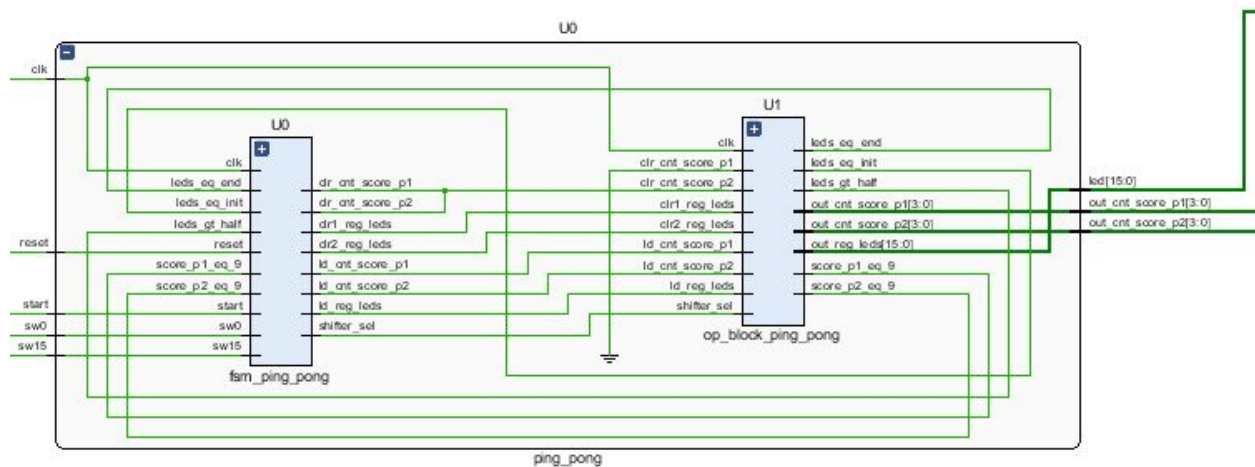


Figura 2.7 - Diagrama esquemático do bloco ping\_pong conectando o bloco operacional com a máquina de estados

### 3) Estimação de consumo de recursos lógicos após a síntese lógica

Resource	Utilization	Available	Utilization %
LUT	73	20800	0.35
FF	112	41600	0.27
IO	32	106	30.19

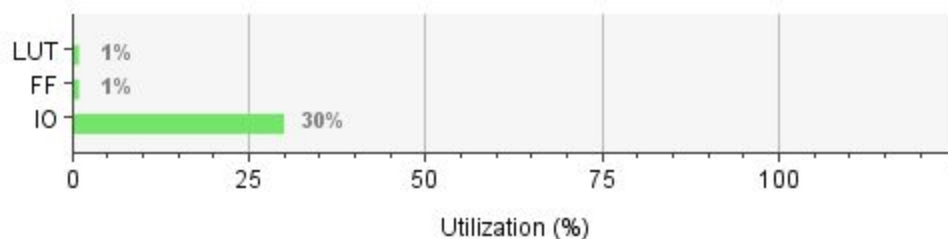


Figura 2.8 - Estimação do consumo de recursos após síntese lógica

#### 4) Estimação de recursos após implementação (processo Place and Route - PAR)

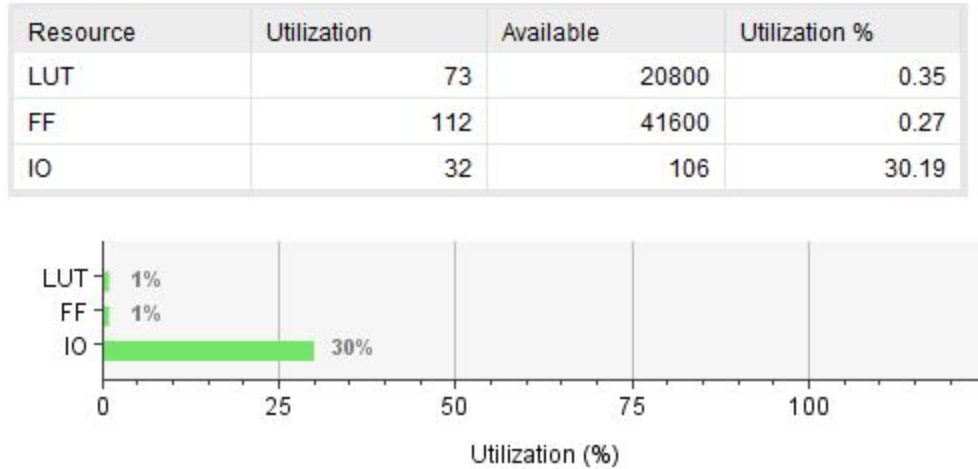


Figura 2.9 - Estimação do consumo de recursos após implementação

#### 5) Análise de Timing

##### Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5,608 ns	Worst Hold Slack (WHS): 0,263 ns	Worst Pulse Width Slack (WPWS): 4,500 ns
Total Negative Slack (TNS): 0,000 ns	Total Hold Slack (THS): 0,000 ns	Total Pulse Width Negative Slack (TPWS): 0,000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 129	Total Number of Endpoints: 129	Total Number of Endpoints: 67

All user specified timing constraints are met.

##### Clock Summary

Name	Waveform	Period (ns)	Frequency (MHz)
sys_clk_pin	{0.000 5.000}	10.000	100.000

Intra-Clock Paths - sys_clk_pin - Setup										
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	
Path 1	5.608	3	4	31	U1/clk_div_cnt_reg[4]/C	U1/clk_div_cnt_reg[5]/R	3.902	0.828	3.074	
Path 2	5.608	3	4	31	U1/clk_div_cnt_reg[4]/C	U1/clk_div_cnt_reg[6]/R	3.902	0.828	3.074	
Path 3	5.608	3	4	31	U1/clk_div_cnt_reg[4]/C	U1/clk_div_cnt_reg[7]/R	3.902	0.828	3.074	
Path 4	5.608	3	4	31	U1/clk_div_cnt_reg[4]/C	U1/clk_div_cnt_reg[8]/R	3.902	0.828	3.074	
Path 5	5.655	3	4	31	U1/clk_div_cnt_reg[4]/C	U1/clk_div_cnt_reg[21]/R	3.851	0.828	3.023	
Path 6	5.655	3	4	31	U1/clk_div_cnt_reg[4]/C	U1/clk_div_cnt_reg[22]/R	3.851	0.828	3.023	
Path 7	5.655	3	4	31	U1/clk_div_cnt_reg[4]/C	U1/clk_div_cnt_reg[23]/R	3.851	0.828	3.023	
Path 8	5.655	3	4	31	U1/clk_div_cnt_reg[4]/C	U1/clk_div_cnt_reg[24]/R	3.851	0.828	3.023	
Path 9	5.657	3	4	31	U1/clk_div_cnt_reg[4]/C	U1/clk_div_cnt_reg[10]/R	3.853	0.828	3.025	
Path 10	5.657	3	4	31	U1/clk_div_cnt_reg[4]/C	U1/clk_div_cnt_reg[11]/R	3.853	0.828	3.025	

Intra-Clock Paths - sys_clk_pin - Hold										
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	
Path 11	0.263	1	1	3	U1/clk_div_cnt_reg[0]/C	U1/clk_div_cnt_reg[0]/D	0.368	0.183	0.185	
Path 12	0.263	1	1	2	clk_out_reg/C	clk_out_reg/D	0.354	0.186	0.168	
Path 13	0.264	1	1	2	U1/clk_div_cnt_reg[20]/C	U1/clk_div_cnt_reg[20]/D	0.369	0.249	0.115	
Path 14	0.264	1	1	2	U1/clk_div_cnt_reg[24]/C	U1/clk_div_cnt_reg[24]/D	0.369	0.249	0.115	
Path 15	0.264	1	1	2	U1/clk_div_cnt_reg[28]/C	U1/clk_div_cnt_reg[28]/D	0.369	0.249	0.115	
Path 16	0.264	1	1	2	U1/clk_div_cnt_reg[4]/C	U1/clk_div_cnt_reg[4]/D	0.369	0.249	0.115	
Path 17	0.264	1	1	2	U1/clk_div_cnt_reg[8]/C	U1/clk_div_cnt_reg[8]/D	0.369	0.249	0.115	
Path 18	0.264	1	1	2	U1/clk_div_cnt_reg[16]/C	U1/clk_div_cnt_reg[16]/D	0.369	0.249	0.115	
Path 19	0.264	1	1	2	U1/clk_div_cnt_reg[12]/C	U1/clk_div_cnt_reg[12]/D	0.369	0.249	0.115	
Path 20	0.266	1	1	2	U1/clk_div_cnt_reg[17]/C	U1/clk_div_cnt_reg[17]/D	0.371	0.256	0.115	

Figura 2.10 - Análise de Timing do test\_ping\_pong

6) Layout do circuito após a implementação (após o processo Place and Route – PAR)



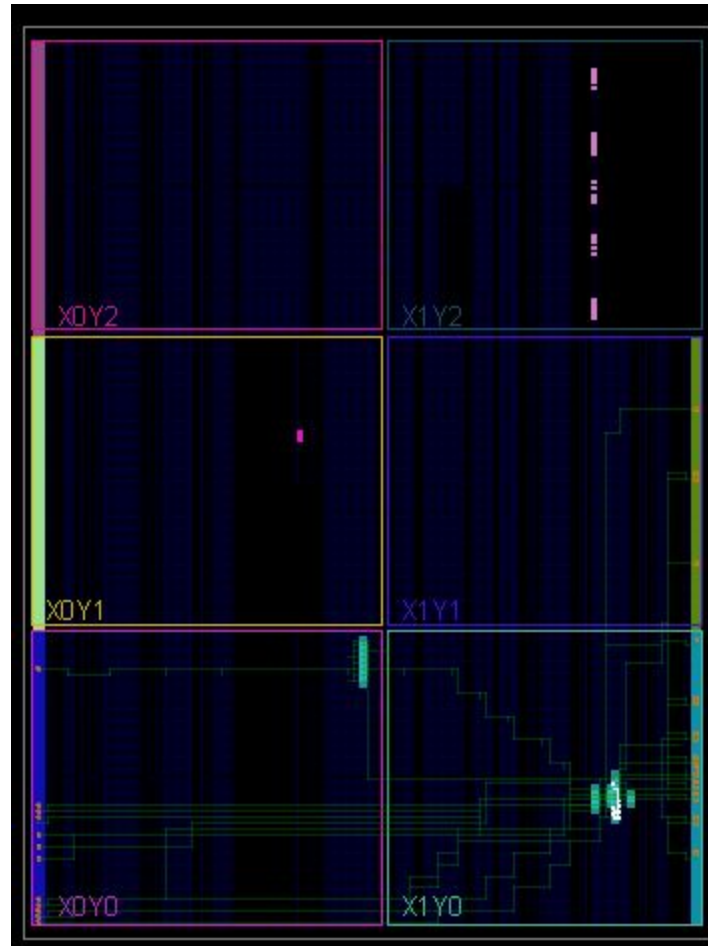


Figura 2.11 - Layout do circuito após a implementação

## 7) Estimação do consumo de energia após a implementação do circuito

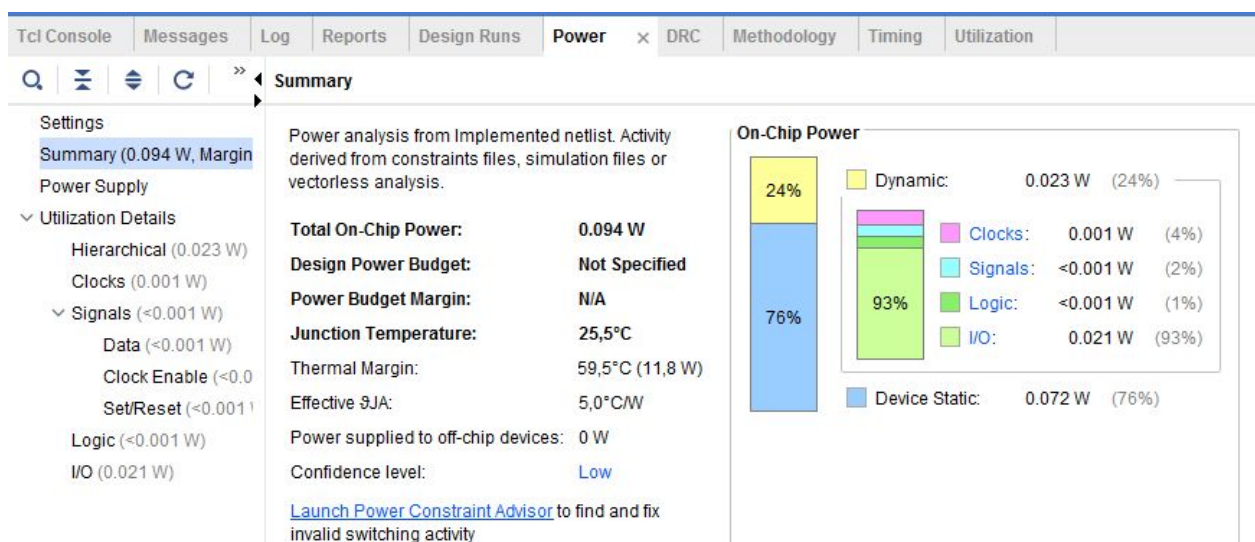


Figura 2.12 - Estimação do consumo de energia após implementação

### Exercício 3: Neurônio GMBH de segunda ordem usando IP-Cores em ponto flutuante

#### 1) Diagrama de blocos proposto

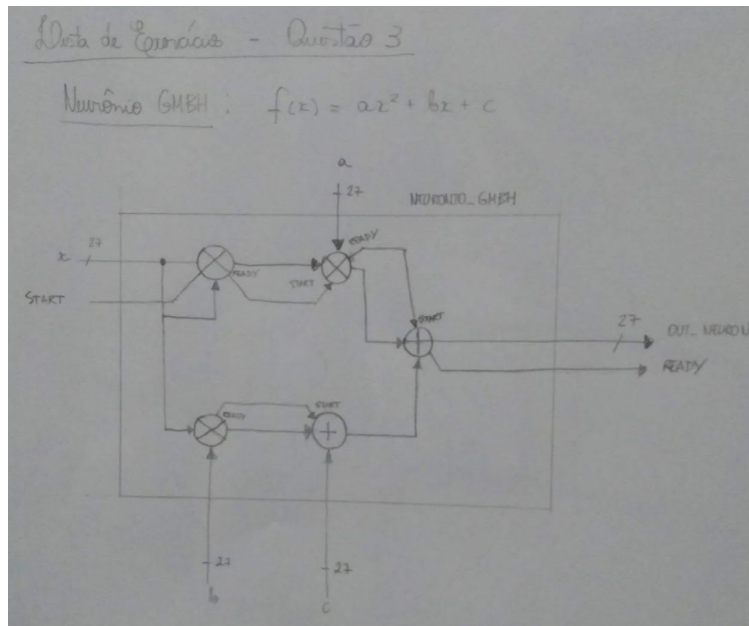


Figura 3.1 - Diagrama de blocos do neurônio GMBH que implementa a função  $f(x) = ax^2 + bx + c$

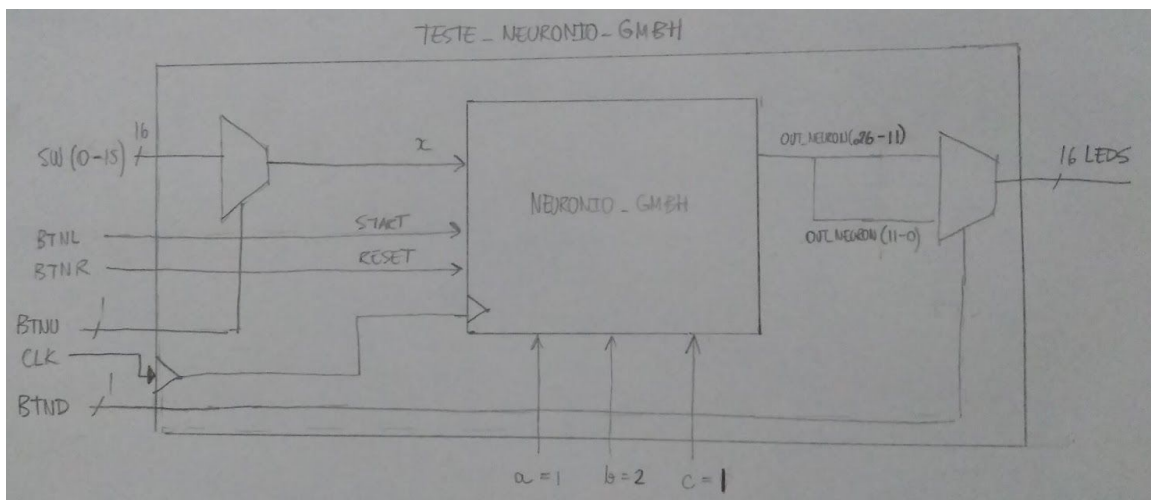


Figura 3.2 - Diagrama de blocos de teste utilizando os switches, push buttons e leds da Basys 3

#### 2) Diagrama Esquemático (Análise RTL pré-síntese)

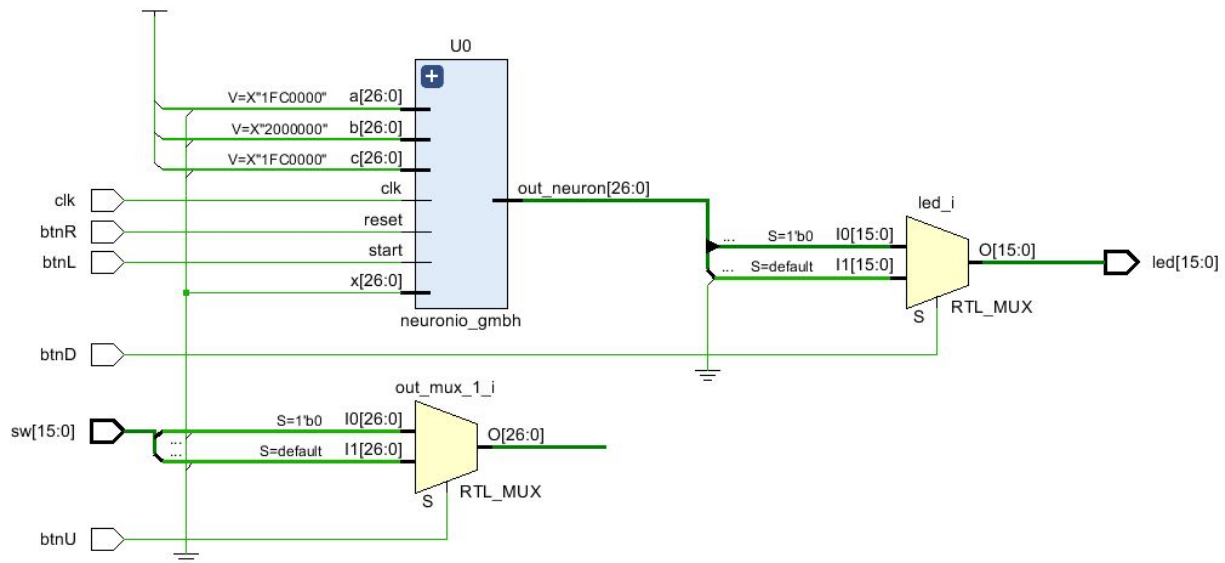


Figura 3.3 - Diagrama Esquemático pré-síntese do bloco teste\_neuronio\_gmbh

### 3) Estimação de consumo de recursos lógicos após a síntese lógica

Resource	Utilization	Available	Utilization %
LUT	740	20800	3.56
FF	190	41600	0.46
DSP	3	90	3.33
IO	37	106	34.91

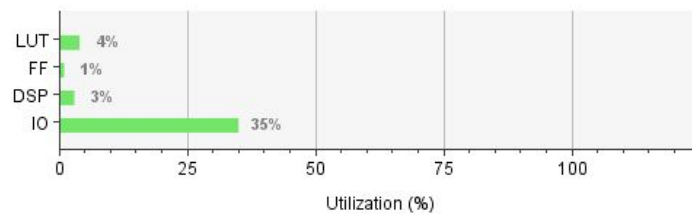


Figura 3.4 - Estimação de consumo de recursos após a síntese lógica

### 4) Estimação de recursos após implementação (processo Place and Route - PAR)

Resource	Utilization	Available	Utilization %
LUT	735	20800	3.53
FF	190	41600	0.46
DSP	3	90	3.33
IO	37	106	34.91

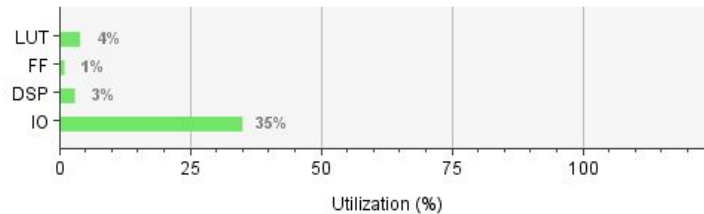


Figura 3.5 - Estimação de consumo de recursos após a implementação

## 5) Análise de Timing:

### Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 1,630 ns	Worst Hold Slack (WHS): 0,106 ns	Worst Pulse Width Slack (WPWS): 4,500 ns
Total Negative Slack (TNS): 0,000 ns	Total Hold Slack (THS): 0,000 ns	Total Pulse Width Negative Slack (TPWS): 0,000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 337	Total Number of Endpoints: 337	Total Number of Endpoints: 191

All user specified timing constraints are met.

### Clock Summary

Name	Waveform	Period (ns)	Frequency (MHz)
sys_clk_pin	{0.000 5.000}	10.000	100.000

Intra-Clock Paths - sys_clk_pin - Setup									
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic	
Path 1	1.630	11	10	19	U0/add_gen[0]..._out_reg[19]/C	U0/add_gen[1]...man_reg[17]/D	8.362		
Path 2	1.651	11	10	19	U0/add_gen[0]..._out_reg[19]/C	U0/add_gen[1]...man_reg[19]/D	8.341		
Path 3	1.725	11	10	19	U0/add_gen[0]..._out_reg[19]/C	U0/add_gen[1]...man_reg[18]/D	8.267		
Path 4	1.741	11	10	19	U0/add_gen[0]..._out_reg[19]/C	U0/add_gen[1]...man_reg[16]/D	8.251		
Path 5	1.745	10	9	19	U0/add_gen[0]..._out_reg[19]/C	U0/add_gen[1]...man_reg[13]/D	8.248		
Path 6	1.766	10	9	19	U0/add_gen[0]..._out_reg[19]/C	U0/add_gen[1]...man_reg[15]/D	8.227		
Path 7	1.840	10	9	19	U0/add_gen[0]..._out_reg[19]/C	U0/add_gen[1]...man_reg[14]/D	8.153		
Path 8	1.856	10	9	19	U0/add_gen[0]..._out_reg[19]/C	U0/add_gen[1]...man_reg[12]/D	8.137		
Path 9	1.861	9	8	19	U0/add_gen[0]..._out_reg[19]/C	U0/add_gen[1]...s_man_reg[9]/D	8.134		
Path 10	1.882	9	8	19	U0/add_gen[0]..._out_reg[19]/C	U0/add_gen[1]...man_reg[11]/D	8.113		



Intra-Clock Paths - sys_clk_pin - Hold								
Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic
Path 11	0.106	1	1	1	U0/add_gen[1].a...state_reg[2]/C	U0/add_gen[1].a...state_reg[0]/D	0.240	
Path 12	0.152	1	1	3	U0/add_gen[0].a...state_reg[2]/C	U0/add_gen[0].a...state_reg[0]/D	0.285	
Path 13	0.172	1	1	12	U0/mult_gen[1]...state_reg[0]/C	U0/mult_gen[1]...l_out_reg[25]/D	0.306	
Path 14	0.174	1	1	12	U0/mult_gen[1]...state_reg[0]/C	U0/mult_gen[1]...l_out_reg[24]/D	0.308	
Path 15	0.212	0	1	28	U0/add_gen[0].a...state_reg[1]/C	U0/add_gen[0].a...state_reg[2]/D	0.295	
Path 16	0.218	1	1	1	U0/add_gen[0].add/s_sign_reg/C	U0/add_gen[0]...out_reg[26]/D	0.324	
Path 17	0.244	1	1	29	U0/mult_gen[2]...state_reg[0]/C	U0/mult_gen[2]...state_reg[1]/D	0.351	
Path 18	0.259	1	1	12	U0/mult_gen[1]...state_reg[0]/C	U0/mult_gen[1]...l_out_reg[22]/D	0.393	
Path 19	0.261	1	1	12	U0/mult_gen[1]...state_reg[0]/C	U0/mult_gen[1]...l_out_reg[21]/D	0.394	
Path 20	0.262	1	1	2	U0/add_gen[0].a...state_reg[0]/C	U0/add_gen[0].a...state_reg[1]/D	0.383	

Figura 3.6 - Análise de Timing do Bloco

6) Layout do circuito após a implementação (após o processo Place and Route – PAR):

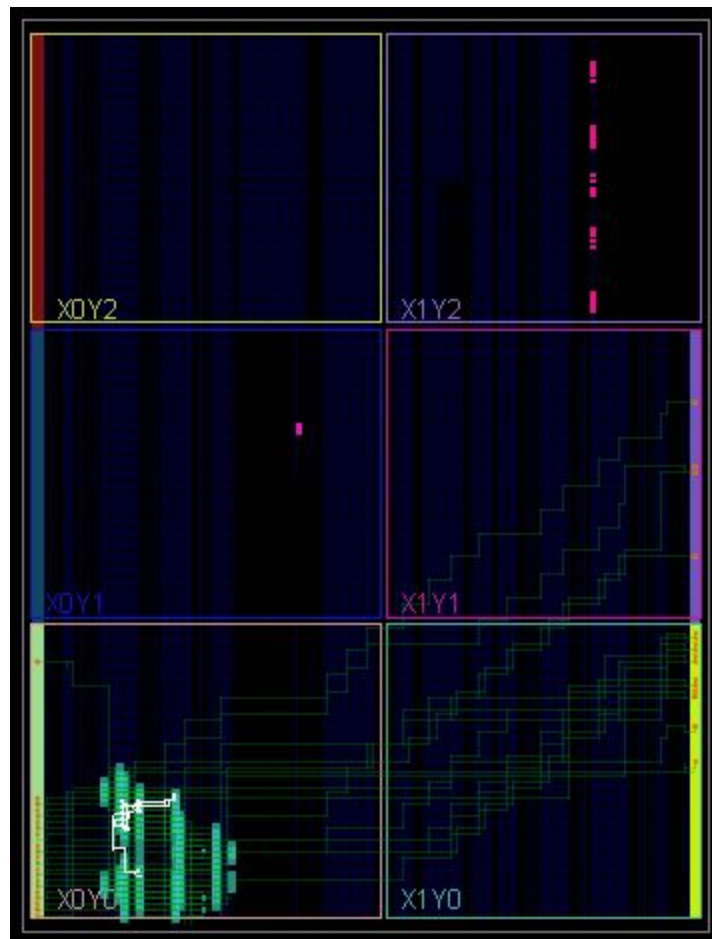


Figura 3.7 - Layout do circuito após a implementação

7) Estimação do consumo de energia após a implementação do circuito:

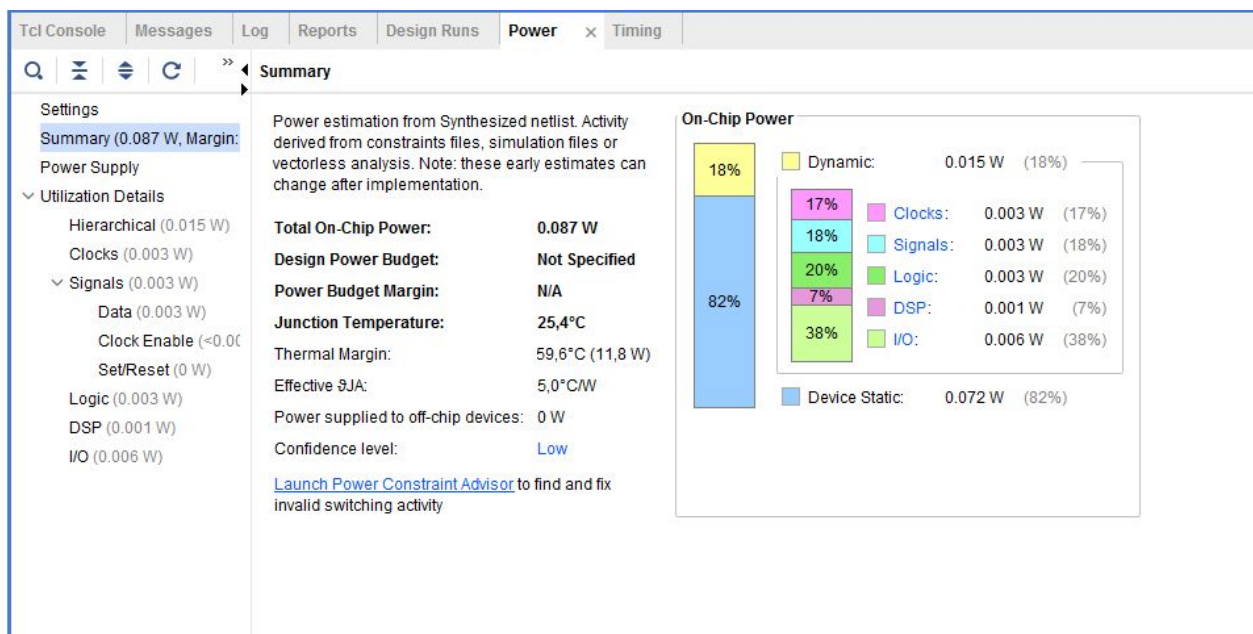


Figura 3.8 - Estimação do Consumo de energia após a implementação do circuito