Examiners' commentaries 2015–16

CO1110 Introduction to computing and the Internet – Zone A

General remarks

The examination was set to test candidates' basic and deeper understanding of the material contained in the Introduction to computing and the Internet subject guide (Volumes 1 and 2). The examination was split into two parts, A and B. In part A, candidates had to show their understanding of computer architecture, data representation and operating systems. In part B, candidates were tested on their understanding of computer networks, network protocols, the internet, computer viruses, the Computer Misuse Act 1990 and the Data Protection Act 1998. Candidates were required to attempt two questions from each part. In general, candidates did well in this examination.

Comments on specific questions

Part A

Question 1

The main aim of this question was to assess candidates' understanding of a different number of systems, e.g. binary and hexadecimal, integer and fraction representation. The majority of candidates attempted this question and scored a high mark.

Part (a) consisted of four multiple-choice questions, which were generally well answered. A good understanding of the two's complement notation, its range and the notion of overflow were required to achieve a high mark in this part of the question.

In part (b), candidates had to demonstrate their understanding of the memory addressing system. Candidates were asked to find the number of bits needed to address a single memory location. This includes an understanding of the concept of a word in computing and being able to work out the number of bits needed to address a single word. A number of candidates failed to answer this part of the question correctly.

In part (c), candidates had to demonstrate a general understanding of the IEEE 754 single-precision binary floating-point format: the sign, the exponent and the mantissa. In part (c) (i) candidates were required to show how to represent a decimal number in an IEEE 754 single-precision binary floating-point format. This part was generally well answered.

In part (c) (ii) candidates were asked to give the range of positive expressible numbers in IEEE 754 that leads to positive underflow in single-precision representation (positive number less than 2^{-127}). A large number of candidates failed to answer this part correctly.

Question 2

This question aimed to test candidates' understanding of computer memory storage, the central processing unit (CPU), the notion of pipelining and the problems related to it.

Part (a) was a three part multiple-choice style question related to computer memory storage and was successfully completed by the majority of candidates.

Part (b) was related to the CPU. Candidates were asked to draw a diagram showing the three main components of the CPU and explain the role of each. This question was successfully completed by the majority of candidates.

Part (c) tested candidates' understanding of how pipelining improves a computer's performance, pipelining hazards (data and control hazards) and different ways to reduce pipelining stalls. This part of the question was successfully answered by a large number of candidates.

Question 3

This question aimed to test candidates' understanding of the relationship between a computer's address bus and memory chips, and the role of input/output modules. Overall, the majority of candidates answered this question correctly.

Part (a) tested candidates' understanding of the computer memory hierarchy. This part was generally well answered.

Part (b) focused on the relationship between a computer's memory chip and the number of address lines used to identify a particular memory cell. A large number of candidates failed to answer this part correctly. A model answer is given as follows:

i. *The number of 128 x 8 RAM chips needed to provide a memory capacity of 2048 bytes is 2048/128 = 16.*

ii. *16 = 2^4, hence 4 address lines are used for chip selection.*

iii. *2048 = 2^{11}, 11 address lines are needed to access 2048 bytes of memory.*

iv. *11 – 4 = 7 are required to address each chip.*

Part (c) was answered by the majority of candidates. A good answer to this part of the question requires a clear explanation of the role of input/output modules: direct memory address (DMA) and interrupt-driven I/O, including the advantages/disadvantages of each.

Part B

Question 4

This question aimed to test candidates' general understanding of computer networks, network protocols and the role of subnetting.

Part (a) was a simple multiple choice question regarding network protocols and network classes, and was correctly answered by all candidates.

Part (b) focused on the understanding of TCP/IP layering and how TCP/IP uses headers to implement layering. To score a high mark on this question, candidates needed to give a clear explanation of the TCP/IP layering model as well as a clear explanation of the role of headers in implementing layering.

Part (c) focused on the understanding of the concept of subnetting in computer networks, as well as the problems subnetting addresses. A large number of candidates failed to score a high mark in this question, by not giving either a clear explanation of what subnetting is or the problems it addresses.

Question 5

Part (a) and (b) of this question aimed to test candidates' general understanding of the HTML web language and XML. These parts were correctly answered by the majority of candidates.

Part (c) aimed to test candidates' understanding of the practical side of subnetting; namely, their technical ability to design a subnet. Parts (i) and (ii) were correctly answered by the majority of candidates. However, a large number of candidates failed to correctly answer parts (iii) and (iv). A model answer for part (c) is given below:

i. *The subnet mask is 255.255.255.248 =11111111 11111111 11111111 11111000*

   The number of borrowed bits is 4. Hence, the number of possible subnets is $2^5 - 2=30$.

ii. *There are 3 bits representing the host. Hence, the number of possible hosts is* $2^3 - 2=6$.

iii. *The address of the first subnet is 220.193.97.8*

iv. *The range of host addresses in the first subnet is 220.193.97.9 – 220.193.97.14*

Question 6

The main aim of this question was to examine the candidates' general understanding of computer viruses, software patents, the Data Protection Act 1998 (DPA) and the issues related to it.

Parts (a) and (b) were successfully completed by the majority of candidates.

In part (c), candidates were given a scenario in which a European Union (EU) company collects and sends customers' personal data to a non-EU country to be processed. Candidates were examined on their understanding of the measures to be taken in order to secure and protect data from any corruption and accidental or malicious loss. A good way to tackle this question would be to list all the steps required to achieve a high level of data security. In order to achieve high marks, candidates would need to provide a well-structured argument, detailing how these steps could be achieved, and the importance of each one.

Examiners' commentaries 2015–16

CO1110 Introduction to computing and the Internet – Zone B

General remarks

The examination was set to test candidates' basic and deeper understanding of the material contained in the Introduction to computing and the Internet subject guide (Volumes 1 and 2). The examination was split into two parts, A and B. In part A, candidates had to show their understanding of computer architecture, data representation and operating systems. In part B, candidates were tested on their understanding of computer networks, network protocols, the internet, computer viruses, the Computer Misuse Act 1990 and the Data Protection Act 1998. Candidates were required to attempt two questions from each part. In general, candidates did well in this examination.

Comments on specific questions

Part A

Question 1

The main aim of this question was to assess the candidates' understanding of a different number of systems, e.g. binary and hexadecimal, integer and fraction representation. The majority of candidates attempted this question and scored high marks.

Part (a) consisted of four multiple-choice questions, which were generally well answered. A good understanding of the two's complement notation, its range and the notion of overflow were required to achieve a high mark in this part of the question.

In part (b), candidates had to demonstrate their understanding of the memory addressing system. Candidates were asked to find the number of bits needed to address a single memory location. This includes an understanding of the concept of a word in computing and being able to work out the number of bits needed to address a single word. A number of candidates failed to answer this part of the question correctly.

In part (c), candidates had to demonstrate a general understanding of the IEEE 754 single-precision binary floating-point format: the sign, the exponent and the mantissa. In part (c) (i) candidates were required to show how to represent a decimal number in an IEEE 754 single-precision binary floating-point format. This part was generally well answered. In part (c) (ii) candidates were asked to give the range of positive expressible numbers in IEEE 754 single-precision representation (2^{-127} to $(2- 2^{-23})\ 2^{127}$). A large number of candidates failed to answer this part correctly.

Question 2

This question aimed to test candidates' understanding of computer memory storage, the central processing unit (CPU), the notion of pipelining and the problems related to it.

Part (a) was a multiple-choice question related to computer memory storage and was successfully completed by the majority of candidates.

Part (b) was related to the CPU. Candidates were asked to draw a diagram showing the three main components of the CPU and explain the role of each. This question was successfully completed by the majority of candidates.

Part (c) tested candidates' understanding of how pipelining improves a computer's performance, pipelining hazards (data and structural hazards) and different ways to reduce pipelining stalls. This part of the question was successfully answered by a large number of candidates. However, a considerable number of candidates failed to explain the notion of structural hazards correctly.

Question 3

This question aimed to test candidates' understanding of the relationship between a computer's address bus and memory chips and the role of input/output modules. Overall, the majority of candidates answered this question correctly.

Part (a) tested candidates' understanding of the computer memory hierarchy. This part was generally well answered.

Part (b) focused on the relationship between a computer's memory chip and the number of address lines used to identify a particular memory cell. A large number of candidates failed to answer this part correctly. A model answer is given as follows:

i. *The number of 128 x 8 RAM chips needed to provide a memory capacity of 1024 bytes is 1024/128 = 8.*

ii. *$8=2^3$, hence 3 address lines are used for chip selection.*

iii. *$1024= 2^{10}$, 10 address lines are needed to access 1024 bytes of memory.*

iv. *10 – 3 = 7 are required to address each chip.*

Part (c) was answered by the majority of candidates. A good answer to this part of the question requires a clear explanation of the role of input/output modules: programmed I/O and interrupt-driven I/O, including the advantages/disadvantages of each.

Part B

Question 4

This question aimed to test candidates' general understanding of computer networks, network protocols and the role of subnetting.

Part (a) was a simple multiple choice style question regarding network protocols and network classes, and was correctly answered by all candidates.

Part (b) focused on the understanding of TCP/IP layering and the role of the two main protocols of the transport layer (TCP and UDP). To score a high mark on this question, candidates needed to give a clear explanation of both protocols, TCP and UDP, and highlight the main difference between the two, as well as give cases where one protocol is used or preferred over the other.

Part(c) focused on the understanding of how TCP deals with flow control. To score a high mark on this question, candidates had to give a clear explanation of how a sliding window protocol is used to deal with this problem.

Question 5

Part (a) and (b) of this question aimed to test candidates' general understanding of the HTML web language and XML. These parts were correctly answered by the majority of candidates.

Part (c) aimed to test candidates' understanding of the practical side of subnetting; name their technical ability to design a subnet. Parts (i) and (ii) were correctly answered by the majority of candidates. However, a large number of candidates failed to correctly answer parts (iii) and (iv). A model answer for part (c) is given below:

i. *The subnet mask is 255.255.255.224 = 11111111 11111111 11111111 11100000*

   The number of borrowed bits is 3. Hence, the number of possible subnets is $2^3 - 2 = 6$.

ii. *There are 5 bits representing the host. Hence, the number of possible hosts is* $2^5 - 2 = 30$.

iii. *The address of the first subnet is* 193.132.112.32

iv. *The range of host addresses in the first subnet is* 193.132.112.*33* – 193.132.112.*62*.

Question 6

The main aim of this question was to examine candidates' general understanding of computer viruses, software patents, the Data Protection Act 1998 (DPA) and the issues related to it.

Parts (a) and (b) were successfully completed by the majority of candidates.

In part (c), candidates were given a scenario in which a European Union (EU) company collects and sends customers' personal data to a non-EU country to be processed. Candidates were examined on their understanding of the measures needed to be taken in order to secure and protect data from any corruption and accidental or malicious loss. A good way to tackle this question would be to list all the steps required to achieve a high level of data security. In order to achieve high marks, candidates would need to provide a well-structured argument, detailing how these steps could be achieved, and the importance of each one.