University of London International Programmes

CO1110 – Introduction to computing and the Internet
Coursework assignment 1

2016–2017

This coursework consists of three questions. Full marks will be awarded for complete answers to all three questions. The marks for each part of a question are indicated at the end of the part in [.] *brackets.*

There are 100 marks available on this coursework assignment.

Your coursework should be submitted as a single PDF file, using the following file-naming conventions:

FamilyName_SRN_COxxxxcw#.pdf (e.g. Zuckerberg_920000000_CO1110cw1.pdf)

- ***FamilyName*** *is your family name (also known as last name or surname) as it appears in your student record (check your student portal)*
- ***SRN*** *is your Student Reference Number, for example 920000000*
- ***COXXXX*** *is the course number, for example CO1108, and*
- ***cw#*** *is either cw1 (coursework 1) or cw2 (coursework 2).*

Question 1

a) A cache may be organised as follows:

Case 1: there are more data elements per block and fewer blocks

Case 2: there are fewer elements per block but more blocks.

In both cases the total capacity of the cache memory is the same. What are the advantages and disadvantages of each organisation? Support your answer with a short example assuming that the cache is direct mapped.

b) Assume a processor with the following characteristics:

- a direct mapped cache
- data words are 8 bits long
- data addresses are to the word
- a physical address is 20 bits long
- the tag is 11 bits
- each block holds 16 bytes of data.

Work out the number of blocks in this cache. Show all of your working.

c) Explain the following two types of mapping procedures: direct mapping and associative mapping in the organisation of cache memory. Illustrate your answer with a diagram showing how each of these two mapping procedures work.

d) A computer memory unit contains 512k words. Each word has 64 bits. A binary instruction has four parts: an indirect bit, an operation code, a register code part to specify one of the 32 registers and an address part. An instruction binary code is stored in word memory.

1. How many bits are needed for the operation code, the register code and the address part?
2. Draw the instruction in word format indicating the number of bits of each part.
3. How many bits are there in the data and address inputs of the memory?

[40 marks]

Question 2

a) Assume we use a pipeline with a 5-stage instruction: IF, ID, EX, MEM and WR. Consider the following sequence of instructions:

ADD R8, R5, R5

ADD R2, R5, R8

SUB R3, R8, R4

ADD R2, R2, R3

1. Identify all the data dependencies in the above instruction sequence.
2. Assume that the pipeline does not use operand forwarding and that the only sources

of pipeline stalls are the data hazards. Draw a multi-cycle pipeline diagram to show the execution of the five instructions listed in (a). How long does it take for the instruction sequence to complete?

3. Assume the pipeline does now use operand forwarding. Draw a diagram that represents the flow of instructions through the pipeline during each clock cycle. Indicate operand forwarding by arrows. How long does it take for the instruction sequence to complete in this case?

[30 marks]

Question 3

a) Given the following bit pattern:

1110 0100 1001 0010 0100 0000 0000 0000

1. What decimal number does it represent, assuming it is represented in a signed integer?
2. What decimal number does it represent, assuming it is a two's complement integer?
3. What decimal number does it represent, assuming it is a single-precision floating point number?

b) Explain how addition and subtraction of floating point operations are carried out. Give an example showing how each step is carried out.

[30 marks]

[Total 100 marks]

[END OF COURSEWORK ASSIGNMENT 1]