Coursework commentaries 2016–2017

CO1110 Introduction to Computing and the Internet

Coursework assignments 1 and 2

General remarks

There were three questions for each coursework assignment with 100 marks available for each one.

Overall, the majority of students did well on this coursework assignment – unless where specified below – answering most questions correctly, if not always giving complete explanations for their answers.

Comments on specific questions

Coursework assignment 1

Question 1

This question tested students on their understanding of computer memory. Parts (a), (b) and (c) focused on cache memory architecture, and different cache memory mapping techniques, such as direct mapping and associative mapping.

A few students lost marks in part (c) by not including a graph, or by providing only a cursory or unclear explanation. A high mark required detailed explanation, and illustrative graphs for direct mapping and associative mapping.

Part (d) tested focused on the four instruction parts: indirect bit, operation code, register code and the address:

Indirect:1 bit

Address: 512K = $2^9 * 2^{10} = 2^{19}$. So, 19 bits are needed for the address part.

Register: 32 registers = 2^5. So, 5 bits are needed for the register code.

OP-code: The remaining bits 64 – 1 – 19 – 5 bits = 39. So, 39 bits are used as parts of the operation-code

The majority of students answered this part of the question correctly.

Question 2

This question tested students on their understanding of the concept of pipelining, and the hazards related to it. Students were required to understand the syntax of the sequence of instructions given and identify all the data dependencies (RAW).

In part (2) students were expected draw a diagram of a pipeline to execute the five instructions, and to identify which of the dependencies gave rise to hazards (i.e. where pipeline stalls would be triggered). Students were also asked to identify the type of hazard.

Those who drew good diagrams (as most did) could easily identify that the dependencies gave rise to the Read After Write (RAW) data hazard, that is where one instruction reads a location after an earlier instruction would have written new data to it, had the instructions been performed sequentially, but in the pipeline the write occurs after the read, so the instruction doing the read gets out-of-date data.

Students were required to address data hazards in their diagrams, showing where stalls were triggered by the hazards.

The last part of this question focused on the forwarding technique and how it is used to eliminate the data hazards identified. Students were asked to draw a new pipeline diagram. A number of students failed to answer this part of the question successfully.

With forwarding, this sequence of instruction will be executed in eight cycles.

Question 3

Part (a) of this question tested students on their understanding of integer and fraction representations: signed notation, two's complement notation and floatIng-point representation. Students were given the following 32-bit pattern 1110 0100 1001 0010 0100 0000 0000 0000 and were asked to find the value it represents in different notations. Most students gave correct answers.

Part (b) focused on how addition and subtraction of floating-point operations are carried out. To score a high mark required a detailed explanation, with an example showing all the steps required (alignment of the radix point, addition of the mantissa and normalisation) to achieve these arithmetic operations. While most students gave correct answers, some failed to provide a clear illustrative example to show how these operations are carried out.

Coursework assignment 2

Question 1

Part (a) tested students on their understanding of the Von Neumann architecture. A number of students lost marks on this question by giving a very cursory explanation or not including diagrams for clarification.

In Part (b), students were asked to explain the role of cache memory and how it is used to improve a computer's performance. The answer requires a clear explanation of how cache memory uses spatial and temporal locality of reference to reduce cache misses. The majority of students explained how cache memory uses temporal locality. However, some failed to explain how spatial locality of reference is used to increase cache hits.

Part (c) focused on how TCP handles error and flow control. The answer requires a clear explanation of how positive acknowledgement is used to deal with lost packets and how TCP sliding window works to deal with congestion. This question was answered correctly by the majority of students.

Part (d) focused on the Set-Associated Mapping cache. Almost all students answered this part of the question correctly.

Question 2

For this question, students were required to show their understanding of the concept of subnetting, and its advantages. For part (a), most students correctly explained the role subnetting plays in computer networks. For part (b), students were required to build a subnet. In part b(i) students were asked to justify their answer, and a significant number lost marks by not doing so.

Question 3

This question required students to demonstrate their understanding of the Computer Misuse Act 1990 (CMA). They were required to explain the three categories of offence under the CMA, to identify the shortcomings of CMA in the fight against computer misuse offences, and to show how the UK Police and Justice Act 2006 addresses these shortcomings. Marks were given for clear explanations, for well-structured argument and for the inclusion of illustrative examples.