University of London International Programmes

CO1110 – Introduction to Computing and the Internet

Coursework assignment 1

2017 – 2018

This coursework assignment consists of four questions. Full marks will be awarded for complete answers to all four questions. The marks for each part of a question are indicated at the end of the part in [.] brackets.

There are 100 marks available from this coursework assignment.

Your coursework should be submitted as a single PDF file, using the following file-naming conventions:

YourName_SRN_COxxxxcw#.pdf (e.g. MarkZuckerberg_920000000_CO1110cw1.pdf)

- ***YourName** is your full name as it appears in your student record (check your student portal);*
- ***SRN** is your Student Reference Number, for example 920000000;*
- ***COXXXX** is the course number, for example CO1110; and*
- ***cw#** is either cw1 (coursework 1) or cw2 (coursework 2).*

You should read the CO1110 subject guide and recommended reading for this course before completing this coursework assignment. In addition, you should also consult appropriate library and internet resources. It is important that your submitted assignment is your own individual work and, for the most part, written in your own words. You must provide appropriate in-text citation for both paraphrase and quotation, with a detailed reference section at the end of your assignment (this should not be included in any word count). Copying, plagiarism and unaccredited and wholesale reproduction of material from books or from any online source is unacceptable, and will be penalised (see our guide on how to avoid plagiarism on the VLE).

Question 1

(a) Convert the positive decimal number 17.45 to IEEE 754 single precision representation. Show all of your working out.

[15 marks]

(b) In IEEE 754 single precision, 1.25 is represented as:

0 01111111 01000000000000000000000

In IEEE 754 single precision 1.26 is represented as:

0 01111111 01000010100011110101110

Explain why there are many more 1's in the mantissa of the IEEE 754 representation of 1.26 than 1.25. [10 marks]

(c) Why is the exponent biased in IEEE representation? [5 marks]

Question 2

Consider the problem of finding the total time to access and read data stored as tracks on a computer disk. This can be described, at its simplest, as access time plus transfer time. Access time is comprised of the average time for the reading head to find the correct track (known as *seek* time) plus the rotational delay, or latency. Seek time is zero for fixed-head systems. The rotational latency is the average time taken for the disc to spin around to the correct place to start reading. This is considered to be, on average, half the time taken for one complete disk rotation.

The time taken to read data, the transfer time, is given by the amount of data on the track to be read, divided by the total data on the track, all multiplied by the time taken for one disk rotation. Clearly if all of the data on a track is to be read, then this reduces to the time taken for one disk rotation.

There may, in fact, be delays caused by I/O queuing (see Stallings, section *Disk Performance Parameters,* pages 225-227, tenth global edition), but in the following problem we will just consider access time plus transfer time.

Given a moveable-head system with a constant disk rotation speed of 12,000 revolutions per minute (rpm), an average seek time of 6 milliseconds and 512 byte sectors with 500 sectors per track, answer the following questions, giving all your working. Give your final answers to (a) and (b) in milliseconds (ms).

(a) The file is sequentially organised, and is stored on 6 complete tracks followed by exactly one half of a track. [12 marks]

(b) The same file as that in part (a) is now distributed at random across the disk, *i.e.* each sector of the file is randomly placed on the disk. [12 marks]

(c) If the answer to part (a) is X, and the answer to part (b) is Y, express X as a percentage of Y, giving your answer to one significant figure. [6 marks]

Question 3

(a) Explain what is meant by *Locality of reference* and how this is exploited in cache memory to improve performance.

Your answer should be at most two paragraphs long – a paragraph is considered to consist of no more than 8 sentences here.

[10 marks]

(b) Assume a processor with the following characteristics:

- a direct mapped cache
- data words are 8 bits long
- data addresses are to the word
- a physical address is 33 bits long
- the tag is 11 bits
- each block holds 16 kB of data.

Work out the number of lines (blocks) in this cache. Show all of your working. [10 marks]

Question 4

Assume we use a pipeline with a 5-stage instruction cycle:

1. IF = Instruction Fetch
2. ID = Instruction Decode
3. EX = Execute
4. MEM = Memory access
5. WB = Register write back

Consider the following sequence of instructions (the final register in each instruction is where the value computed is stored):

```
1:    ADD R1, R2, R1
2:    INC* R5, R5
3:    ADD R2, R5, R5
4:    SUB R1, R3, R3
5:    ADD R3, R4, R4
```

*Increment by one, ie +1 to R5

(a) Assume that the pipeline does not use operand forwarding and that the only sources of pipeline stalls are the data hazards. Draw a multi-cycle pipeline diagram to show the execution of the five instructions listed above. [8 marks]

(b) How long does it take for the instruction sequence to complete? [2 marks]

(c) Can you reorder the instructions such that they give the same results and stalls are reduced or eliminated? Justify your answer. [10 marks]

[Total 100 marks]

[END OF COURSEWORK ASSIGNMENT 1]