

# **Electronics and Communication Systems**

## **Electronics Systems**

**Master Degree in Computer Engineering**  
**<https://computer.ing.unipi.it/ce-lm>**

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**Email:** massimiliano.donati@unipi.it

# Course Schedule

				1M Computer Eng		
	Lu	Ma	Me	Gi	Ve	Sa
8:30/9:30	Performance evaluation of Computer Systems and networks AV 1M CE	Electronics and Communications Systems AV 1M CE				
9:30/10:30	Performance evaluation of Computer Systems and networks AV 1M CE	Electronics and Communications Systems AV 1M CE			Performance evaluation of Computer Systems and networks AV 1M CE	
10:45/11:45	Electronics and Communications Systems AV 1M CE	Electronics and Communications Systems AV 1M CE			Performance evaluation of Computer Systems and networks AV 1M CE	
11:45/12:45	Electronics and Communications Systems AV 1M CE	Electronics and Communications Systems AV 1M CE		Large scale and multist. databases AV 1M AI	Large scale and multist. databases AV 1M AI	
12:45/13:45		Electronics and Communications Systems AV 1M CE			Large scale and multist. databases AV 1M AI	
14:00/15:00	Electronics and Communications Systems AV 1M CE					
15:00/16:00	Electronics and Communications Systems AV 1M CE	Large scale and multist. databases AV 1M AI		Performance evaluation of Computer Systems and networks AV 1M CE	Large scale and multist. databases AV 1M AI	
16:00/17:00	Electronics and Communications Systems AV 1M CE	Large scale and multist. databases AV 1M AI		Performance evaluation of Computer Systems and networks AV 1M AI	Large scale and multist. databases AV 1M AI	
17:15/18:15			Performance evaluation of Computer Systems and networks AV 1M AI	Large scale and multist. databases AV 1M AI		
18:15/19:15			Performance evaluation of Computer Systems and networks AV 1M AI	Large scale and multist. databases AV 1M AI		

# Question Time

**by appointment:**

Tel. 347 5013837

Email: [luca.fanucci@unipi.it](mailto:luca.fanucci@unipi.it)

# Students' background and contacts

Name Surname	Telephone	E-mail	Home Town/Country	Bachelor Degree/ University
Luca Fanucci	347 5013837	luca.fanucci@unipi.it	Montecatini Terme (PT) Italy	Electronic Engineering University of Pisa



# Course Goals and Prerequisites

- **Goals**
  - Provide you with an introduction to the **techniques** and **methodologies** used to produce embedded systems based on Very Large Scale Integration (VLSI) technology
    - **Circuits** and **Architectures** for **basic digital signal processing blocks** to be used for complex system synthesis according to given **performance criteria**: area, speed, power consumption and reliability.
    - Give you some **hands-on experience** with software tools used for Computer Aided Design (**CAD**)
    - Create a foundation for further exploration of VLSI
    - Basic of **sensor conditioning** electronics and **smart sensors**
- **Prerequisites**
  - Basic understanding of circuits and electronics
  - Basic understanding of logic design

# Prerequisiti-Reti Logiche - Prof. Stea (1/2)

**ORGANIZZAZIONE FUNZIONALE DI UN CALCOLATORE:** Schema a blocchi.  
Tecniche di indirizzamento degli operandi e principali istruzioni dei processori della famiglia INTEL 80x86. Il linguaggio assembler MASM, il Debug ed il Code View per processori della famiglia 80x86

**RETI COMBINATORIE:** Le porte AND, OR, NOT, NAND e NOR; il decodificatore/demultiplicatore; il moltiplicatore. Le porte a tre strati e le loro applicazioni. Modalità di descrizione, trattazione algebrica e sintesi ottima delle reti combinatorie. I transitori e le alee.

**RETI SEQUENZIALI ASINCRONE:** Modelli funzionali, modalità di descrizione e modelli implementativi. I flip-flop SR, D latch e D edge-triggered. Le memorie RAM.

# Prerequisiti-Reti Logiche - Prof. Stea(2/2)

**RETI SEQUENZIALI SINCRONIZZATE:** L'elemento di registro; i registri in traslazione e i contatori. Reti sequenziali sincronizzate di Moore, di Mealy e di Mealy Ritardato: modelli funzionali, modalità di descrizione, modelli implementativi. Il flip-flop J-K. Reti sequenziali complesse: descrizione in un linguaggio di trasferimento tra registri, sintesi in accordo al modello strutturale con parte operativa e parte controllo (con particolare riferimento ai modelli microprogrammati).

**STRUTTURA FISICA DI UN CALCOLATORE:** Moduli di base e loro collegamento. Struttura interna del processore; della memoria e di alcune interfacce (parallele, seriali, di conteggio e per la conversione A/D e D/A). L'ingresso/uscita dati a controllo di programma. Il meccanismo di interruzione ed il controllore di interruzione. Tecniche di interruzione nell'ingresso/uscita dati.

**ALGORITMI E RETI DI TIPO ARITMETICO:** Richiami sulla rappresentazione dei numeri naturali, interi e reali; gli algoritmi e le reti fondamentali per una aritmetica dei numeri naturali e dei numeri interi.

# Prerequisiti-Elettronica Digitale-Prof. Piotto

**PORTE LOGICHE IN TECNOLOGIA CMOS:** Inverter CMOS, parametri caratteristici dei circuiti digitali, calcolo dell'energia dissipata durante la commutazione, fan-in, fan-out, sintesi delle porte logiche tramite il metodo della pull-up/pull-down network, protezione ingressi da scariche elettrostatiche, logica a pass transistor, body effect.

**LOGICA SEQUENZIALE:** Latch realizzato con inverter, flip-flop S/R in tecnologia CMOS, flip-flop D e D edge triggered, il circuito integrato NE555 e le sue applicazioni.

**MEMORIE A SEMICONDUTTORE:** Struttura a matrice delle memorie, ROM a diodi, ROM e PROM a MOS, memoria SRAM e DRAM, principio di funzionamento del decoder degli indirizzi (wired NOR), memorie EEPROM e EEPROM.

**GENERATORI DI CLOCK:** Generatore di onda quadra, oscillatore quarzato di Pierce.

# Course Main Topics (1/2)

- **Fundamental Design metrics** in digital integrated circuits design.  
Design space exploration, in terms of area, speed, power consumption, reliability and flexibility addressing the exponential growth in complexity and performance (Moore's law).
- **Design methodologies for full-custom and semi-custom digital integrated circuits** including Field Programmable Gate Arrays (FPGA), Gate Arrays and Standard-Cells. High-level electronic design automation (EDA) tools for hardware-software co-design. Hardware description languages (SystemC, VHDL and Verilog) modeling, simulation and logic synthesis.

# Course Main Topics (2/2)

- **CMOS device** and **interconnect modeling**, static and dynamic logic families, latch and flop design, ALU and MAC design, power supply and clock distribution, signal integrity, and I/O design.
- **Power Consumption in CMOS digital integrated circuits.** Design techniques for the reduction of power consumption at different level of abstractions: logic design, clock gating, multi-VDD, multi-VT, dynamic frequency scaling, dynamic voltage scaling, dynamic thermal management.
- **Sensors** definition, classification and characterization, with focus on **inertial MEMS sensors**, **vital parameter sensors**, etc.. Sensor compensation and calibration techniques. Sensor readout electronics and sensor data fusion.

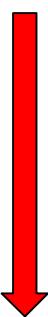
# Course Material (1/2)

- Course Material:
  - Digital Systems Design, SEU. Slides presented **only** for VHDL and logic synthesis.
  - Material available on the web site <https://vlsi.iit.unipi.it/~fanucci/es20>  
(userid: es20 , passwd: 1703es20)
- CMOS Design Bibliographic References:
  - Weste and Eshraghian, "Principles of VLSI Design - A Systems Perspective (2nd ed)", Addison Wesley
  - M. Smith, "Application Specific Integrated Circuits", Addison-Wesley, 1997
  - J. M. Rabaey, "Digital Integrated Circuits - A Design Perspective", Prentice Hall
- Course mailing list:
  - Subscription @ <https://vlsi.iit.unipi.it/~fanucci/DSDList>

# Course Web Site - 28 September 2020

- Slides
  - Introduction.pdf
- Lab

# Course Material (2/2)

- VHDL Bibliographic References:
  - IEEE Standard VHDL Language Reference Manual : IEEE Std 1076-1993
  - S. Mazor, P. Langstraat, "A guide to VHDL", Kluwer Academic Publishers
  - Douglas L. Perry, "VHDL" (2nd edition), McGraw Hill
  - B. Cohen, "VHDL Coding Styles and Methodologies", Kluwer Academic Publishers
  - K.C. Chang, "**Digital Systems Design with VHDL and Synthesis**", **IEEE Computer Society**
  - W.F. Lee, "VHDL: Coding and Logic Synthesis with Synopsys™", Academic Press
- PC-based VHDL simulation tools:
  - Aldec (<http://www.aldec.com>): **Active HDL**
  - [https://www.aldec.com/en/products/fpga\\_simulation/active\\_hdl\\_student](https://www.aldec.com/en/products/fpga_simulation/active_hdl_student)
  - Mentor (<http://www.mentor.com>): **ModelSim** 
  - <http://ghdl.free.fr/> (+ <http://gtkwave.sourceforge.net/>)
- Xilinx Development tool:
  - <http://www.xilinx.com/products/design-tools/vivado/vivado-webpack.html> 

# VHDL Simulation (2/2)

The screenshot shows the Mentor Graphics website with a dark blue header. The header includes the Mentor logo, navigation links for PRODUCTS & SOLUTIONS, TRAINING & SERVICES, COMPANY, BLOGS, SUPPORT, and SIGN IN | CREATE. Below the header, there's a search bar labeled "Search Mentor.com".

The main content area has a dark blue sidebar on the left with links for Higher Education, ModelSim PE Student Edition, Company, and Higher Education.

The main content area features several sections:

- ModelSim PE Student Edition**: A large section with a blue button labeled "Download Student Edition". Below it, text reads: "Free download of industry leading ModelSim® HDL simulator for use by students in their academic coursework."
- About ModelSim PE Student Edition**: A section with a blue button labeled "Performance". Below it, text reads: "Capacity: 10,000 lines of executable code".
- Target Use and Upgrades**: A section with a blue button labeled "Performance". Below it, text reads: "Support for both VHDL and Verilog designs (non-mixed). • ModelSim PE Student Edition is intended for use in mixed environments."
- Highlights**: A section with a blue button labeled "Performance". Below it, text reads: "• Support for both VHDL and Verilog designs (non-mixed). • ModelSim PE Student Edition is intended for use in mixed environments."
- Partners and Foundry Support**: A section with a blue button labeled "Performance". Below it, text reads: "• Support for both VHDL and Verilog designs (non-mixed). • ModelSim PE Student Edition is intended for use in mixed environments."
- Higher Education**: A section with a blue button labeled "Performance". Below it, text reads: "• Capacity: 10,000 lines of executable code".

On the right side of the main content area, there are additional links: RESOURCES, ModelSim Student Edition, Curriculum Support, IC and ASIC Design Kits, Participating Schools, Contact Us, and FAQ.

# VHDL Simulation (1/2)

The screenshot shows the Aldec website with the following navigation bar:

- Home
- > Products
- > FPGA Simulation
- > Active-HDL Student Edition

The main content area features a large blue banner with the text "Active-HDL™ | Student Edition". Below the banner, there is a "Free Download" button.

The "PRODUCTS" section includes links to:

- FPGA Simulation
- Active-HDL
- Functional Verification
- Riviera-PRO
- ALINT
- ALINT-PRO
- High-Level Synthesis
- CyberWorkBench
- Emulation
- HES-DVM
- Requirements Management
- Spec-TRACER
- Mil/Aero Verification
- DO-254
- Prototyping
- HES-7
- RTAX/RTSX
- University Programs
- VIP/IP Products

The "SOLUTIONS" section includes links to:

- Active-HDL™ | Student Edition

The "COMPANY" section includes links to:

- Sign In | Register
- Search aldec.com
- Free Download

The "SUPPORT" and "DOWNLOADS" sections are also present.

On the right side, there is a sidebar with the following sections:

- Free Active-HDL Student Edition
- Active-HDL Student Edition is a mixed language design entry and simulation tool offered at no cost by Aldec for students to use during their course work.
- Licensing
- Active-HDL Student Edition includes a "load and go" license. This means students can begin using it immediately after installing. License Expire? [Download this update](#) to extend license though March 31, 2016.
- Key Features of Active-HDL Student Edition
  - Mixed language simulator
  - Multi-FPGA & EDA Tool Design Flow Manager
  - Graphical Design entry & editing
  - Code2Graphics and Graphics2Code
  - Pre-compiled FPGA vendor libraries
  - IEEE Language Support: VHDL2008, Verilog®, SystemVerilog(Design), SystemC
  - Accelerated Waveform Viewer and List Viewer
  - Interface with MATLAB®/Simulink®
  - HTML and PDF Design Documentation

# VHDL Logic Synthesis and FPGA Programming

The screenshot shows the Xilinx website with a dark theme. At the top, there's a navigation bar with icons for back, forward, search, and user account. The main header features the Xilinx logo and the text "ALL PROGRAMMABLE". Below the header, there's a search bar with the placeholder "All" and a magnifying glass icon. The main menu includes links for APPLICATIONS, PRODUCTS, DEVELOPER ZONE, SUPPORT, and ABOUT.

The page content starts with a section titled "Evaluate the Vivado Design Suite HLx Edition - Free for 30 days!". It includes a call-to-action button labeled "Get Started". Below this, there's a paragraph about the evaluation license and two bullet points: "Download the Vivado Design Suite HLx Edition and start your evaluation today." and "Get a free 30-day Vivado Design Suite HL System Edition Evaluation License.". A "Download Vivado HL WebPACK Edition" section follows, with a paragraph about the edition and a "Download Now!" button.

A sidebar on the right is titled "Vivado Design Suite Evaluation and WebPACK" and lists several links:

- Downloads
- Vivado Video Tutorials
- Intellectual Property
- Support and Documentation
- EDA Solutions Partners

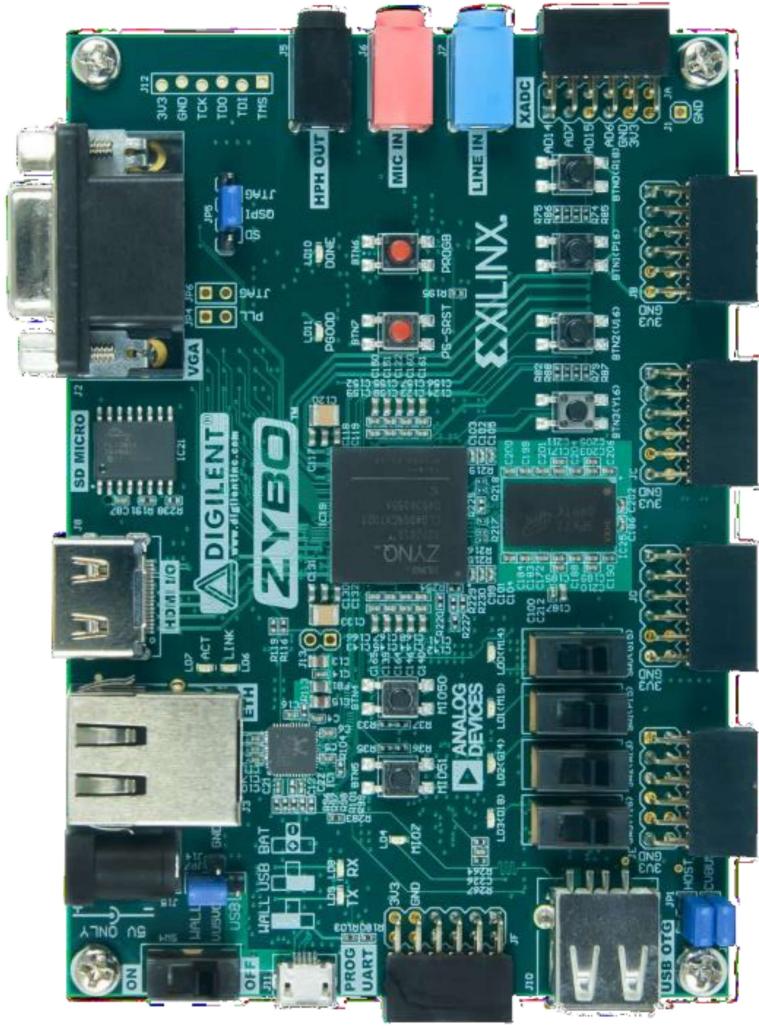
At the bottom of the sidebar, there's a "+ More" link.

The footer of the page includes links for Home, Products, Developer Zone, Vivado Design Suite, Vivado Design Suite Evaluation and WebPACK, and Contact Us.

# ZyBo Development Board (1/3)

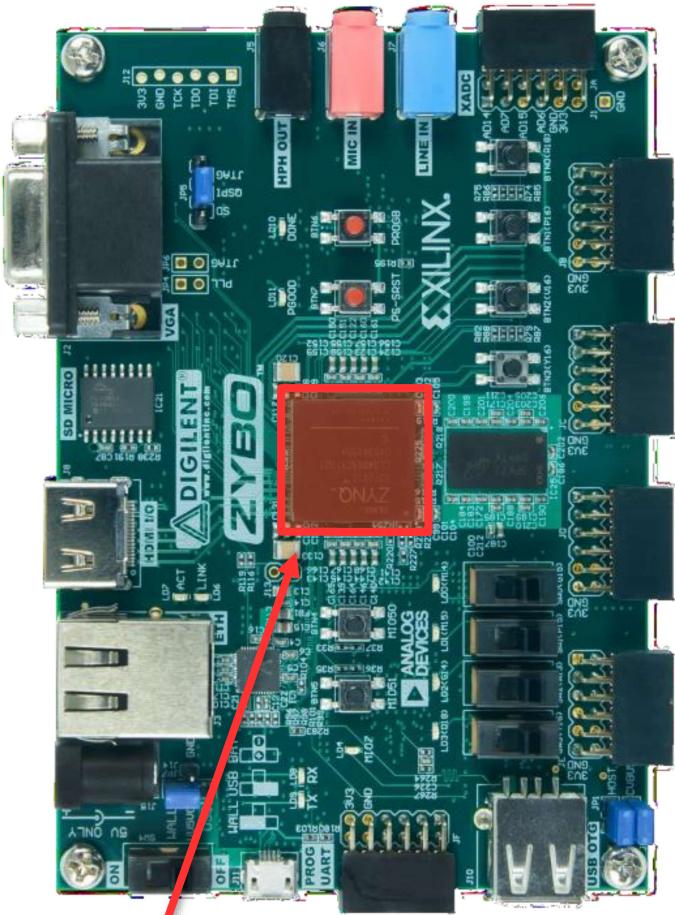
The ZYBO (ZYnq BOard) is a feature-rich, ready-to-use, entry-level embedded software and digital circuit development platform built around the smallest member of the Xilinx Zynq-7000 family, the Z-7010.

The Z-7010 is based on the Xilinx All Programmable System-on-Chip (AP SoC) architecture, which tightly integrates a dual-core ARM Cortex-A9 processor with Xilinx 7-series Field Programmable Gate Array (FPGA) logic.



# ZyBo Development Board (2/3)

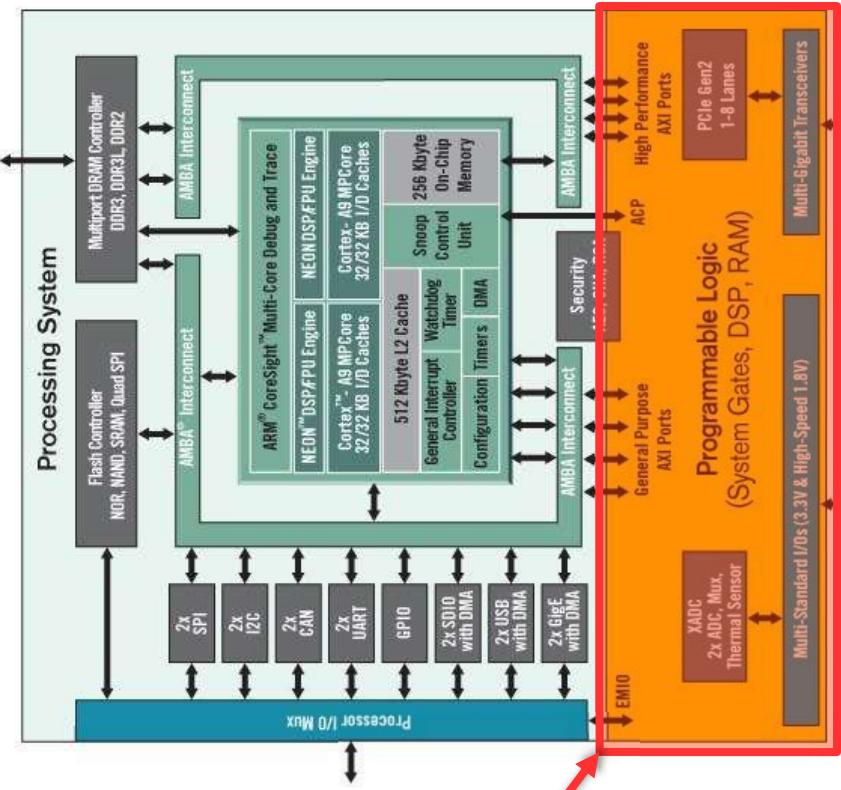
- **ZYNQ XC7Z010-1CLG400C**
- 512MB x32 DDR3 w/ 1050Mbps bandwidth
- Dual-role (Source/Sink) HDMI port
- 16-bits per pixel VGA source port
- Trimode (1Gbit/100Mbit/10Mbit) Ethernet PHY
- MicroSD slot (supports Linux file system)
- OTG USB 2.0 PHY (supports host and device)
- External EEPROM (programmed with 48-bit globally unique EUI-48/64™ compatible identifier)
- Audio codec with headphone out, microphone and line in jacks
- 128Mb Serial Flash w/ QSPI interface
- On-board JTAG programming and UART to USB converter
- GPIO: 6 pushbuttons, 4 slide switches, 5 LEDs
- Six Pmod connectors (1 processor-dedicated, 1 dual analog/digital, 3 high-speed differential, 1 logic-dedicated)



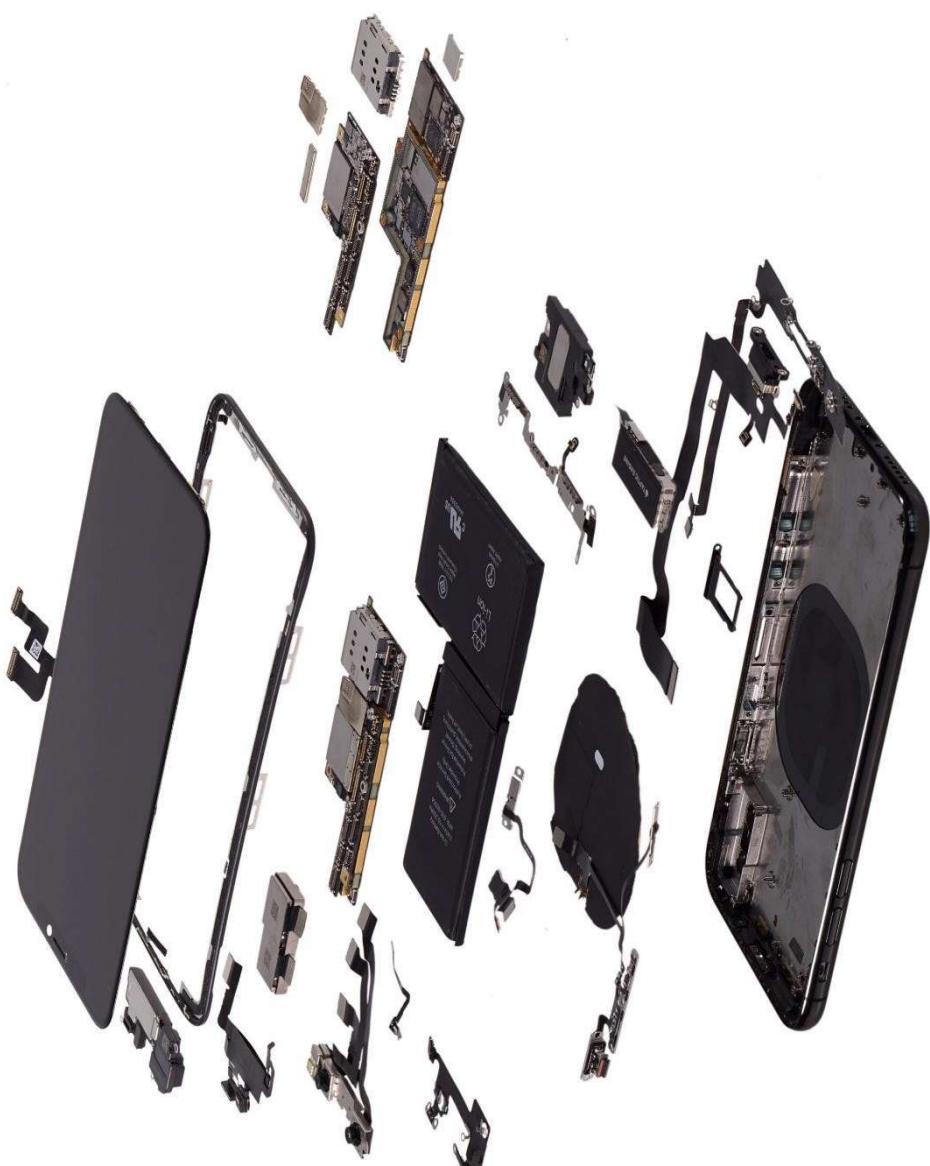
# ZyBo Development Board (3/3)

## ZYNQ XC7Z010-1CLG400C

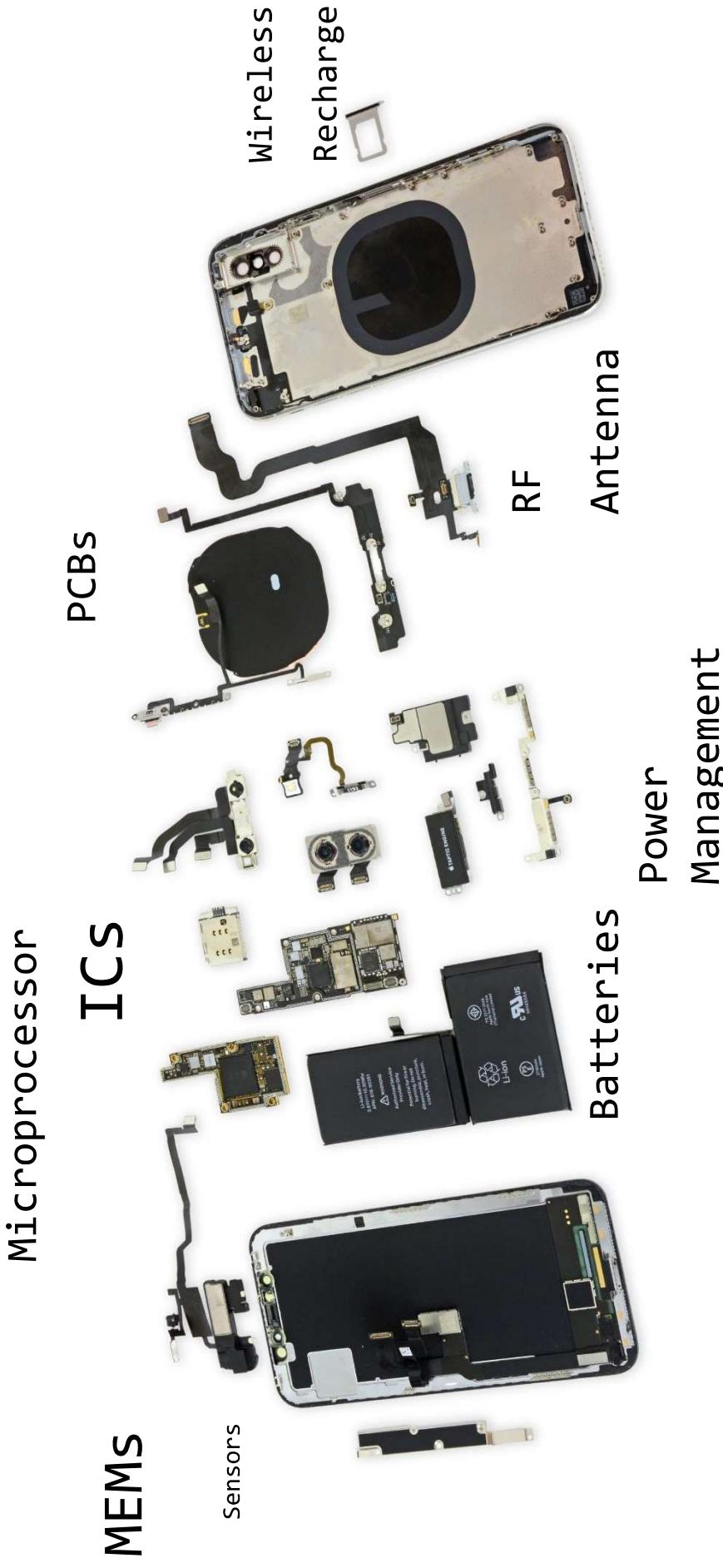
- 650Mhz dual-core Cortex-A9 processor
- DDR3 memory controller with 8 DMA channels
- High-bandwidth peripheral controllers: 1G Ethernet, USB 2.0, SDIO
- Low-bandwidth peripheral controller: SPI, UART, CAN, I2C
- **Reprogrammable logic equivalent to Artix-7 FPGA**
  - 4,400 logic slices, each with four 6-input LUTs and 8 flip-flops
  - 240 KB of fast block RAM
  - Two clock management tiles, each with a phase-locked loop (PLL) and mixed-mode clock manager (MMCM)
  - 80 DSP slices
  - Internal clock speeds exceeding 450MHz
  - On-chip analog-to-digital converter (XADC)



Let's start !!



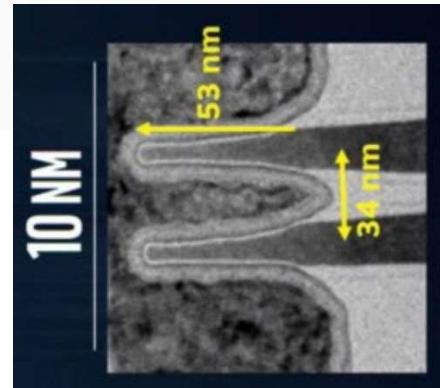
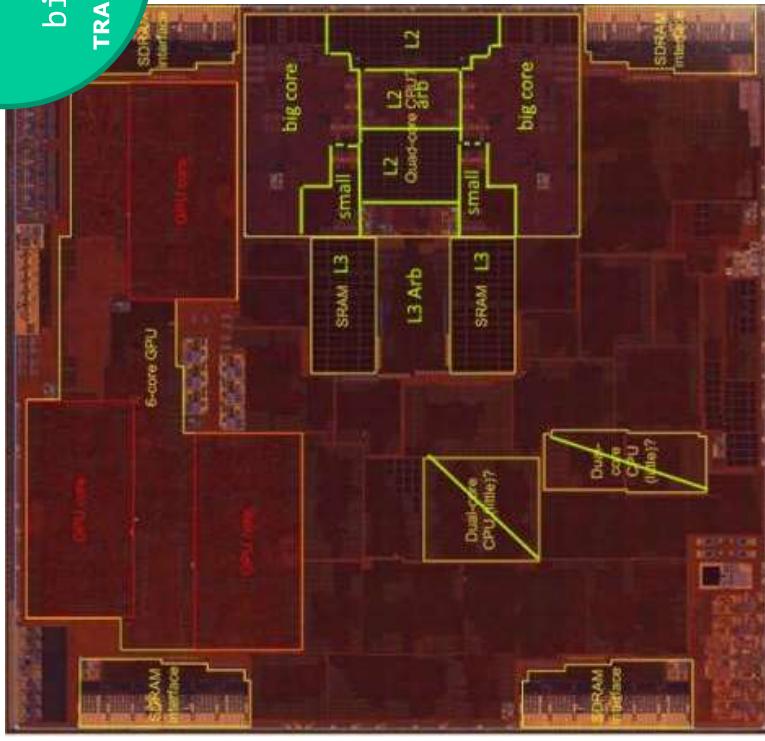
# MULTIDISCIPLINARITY



# MicroProcessor

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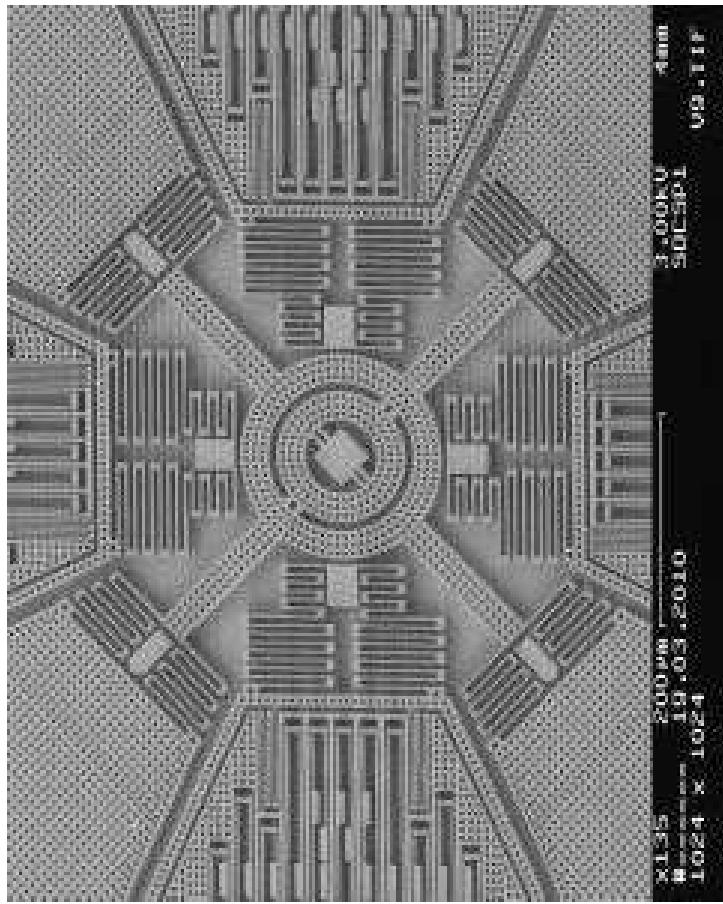
# Sensors

- DOT PROJECTOR
- 7MP CAMERA
- MICROPHONE
- SPEAKER
- AMBIENT LIGHT SENSOR
- FLOOD ILLUMINATOR
- PROXIMITY SENSOR
- INFRARED CAMERA



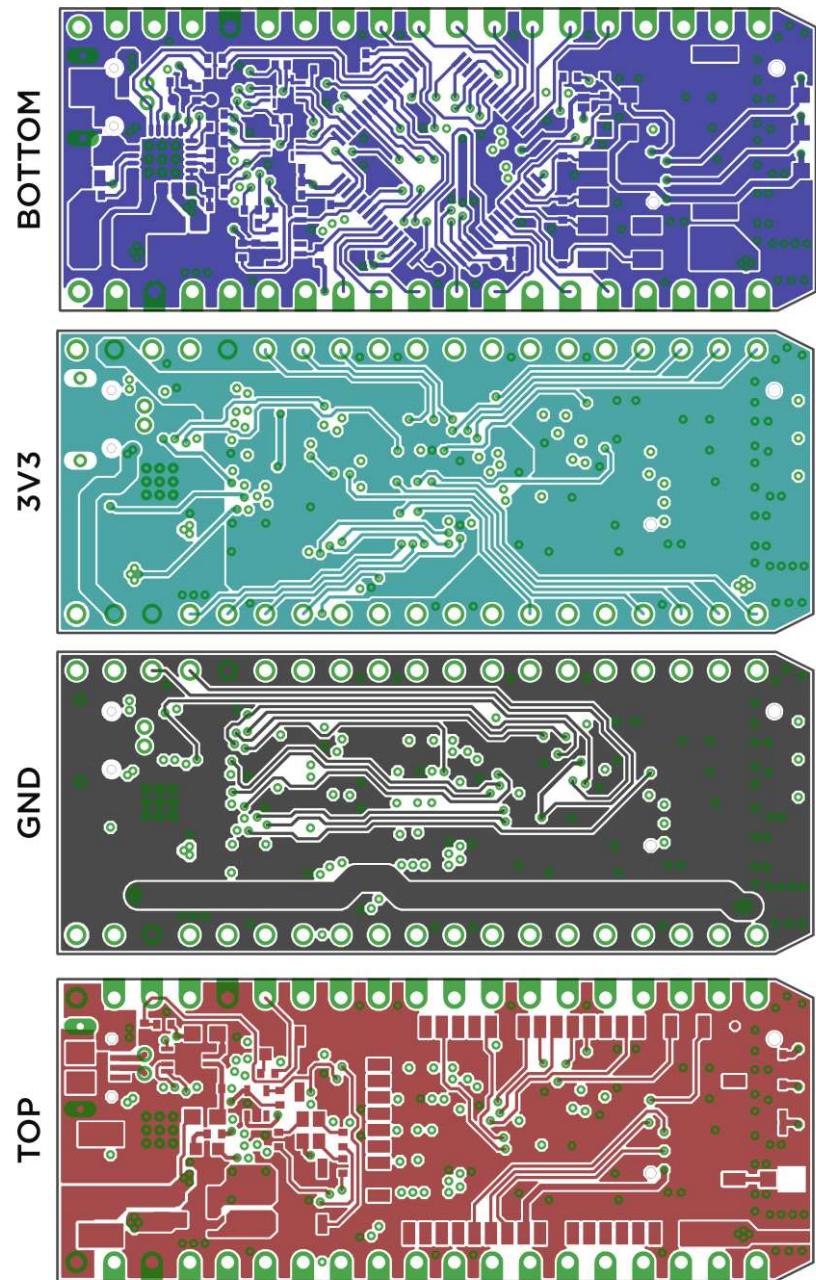
**MEMS**

# Micro-Electro-Mechanical systems



**PCB**

# Printed Circuit Boards





# Batteries



Antenna



Search

Q

Joe



Repair Guides

Answers Forum

Parts & Tools Store

Teardowns

Translate

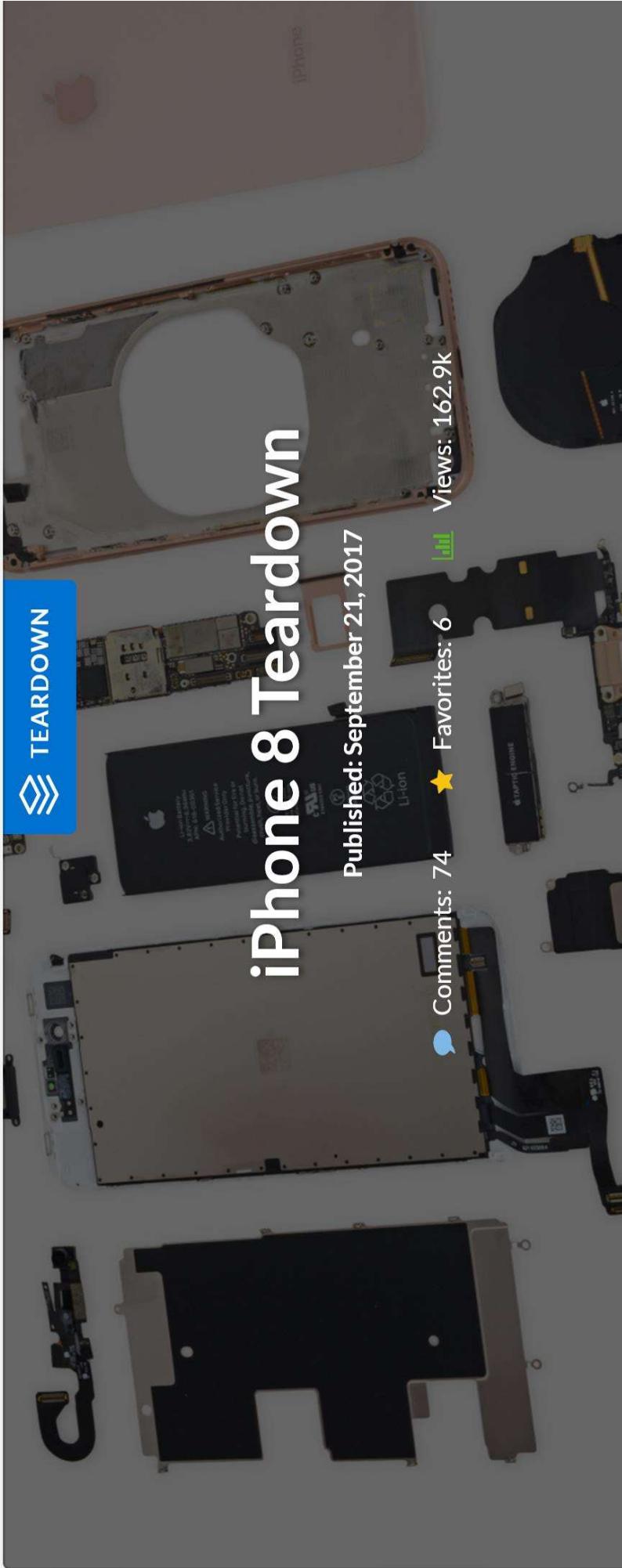
← iPhone 8 Repair

Comments: 74

Edit

Full Screen

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<https://www.ifixit.com/Teardown/iPhone+8+Teardown/97481>

Tools Continued in the Thread

# iPhone 8



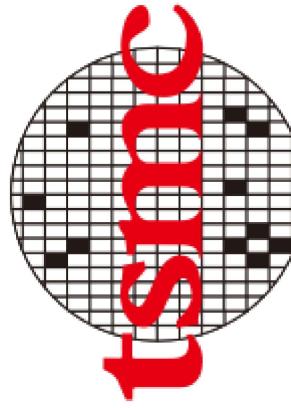
- Apple **339S00434** A11 Bionic SoC layered over SK Hynix H9HKNNNNBRMMUUR 2 GB LPDDR4 RAM
- Qualcomm **MDM9655** Snapdragon X16 LTE modem
- Skyworks SkyOne **SKY78140**
- Avago **8072JD130**
- **P215 730N71T** - likely an envelope tracking IC
- Skyworks **77366-17** quad-band GSM power amplifier module
- NXP **80V18** secure NFC module

# iPhone 8



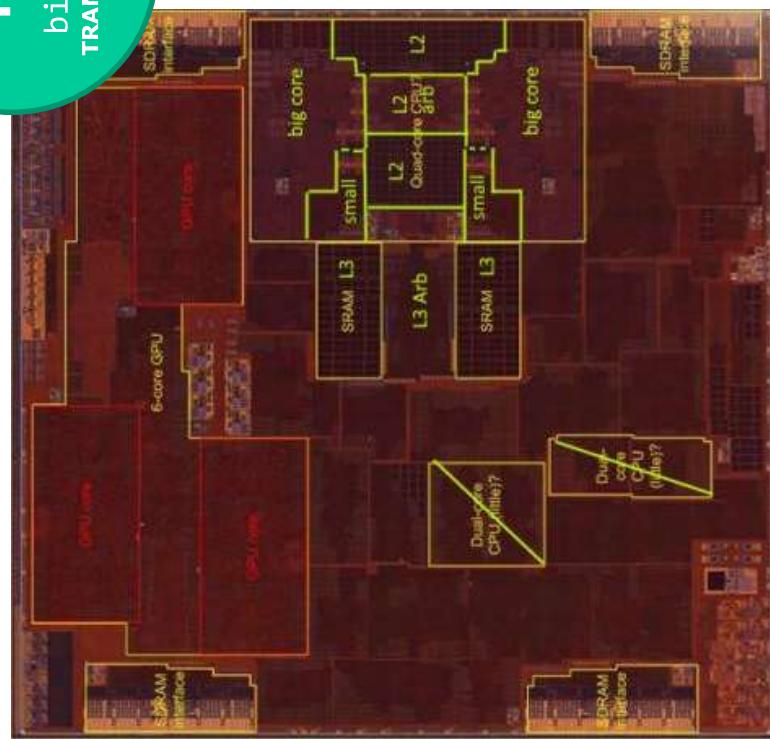
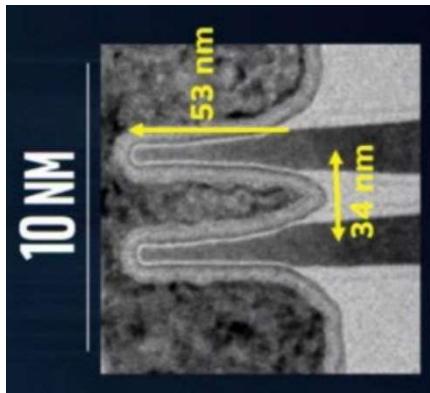
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## iPhone 8



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TRANSISTORS



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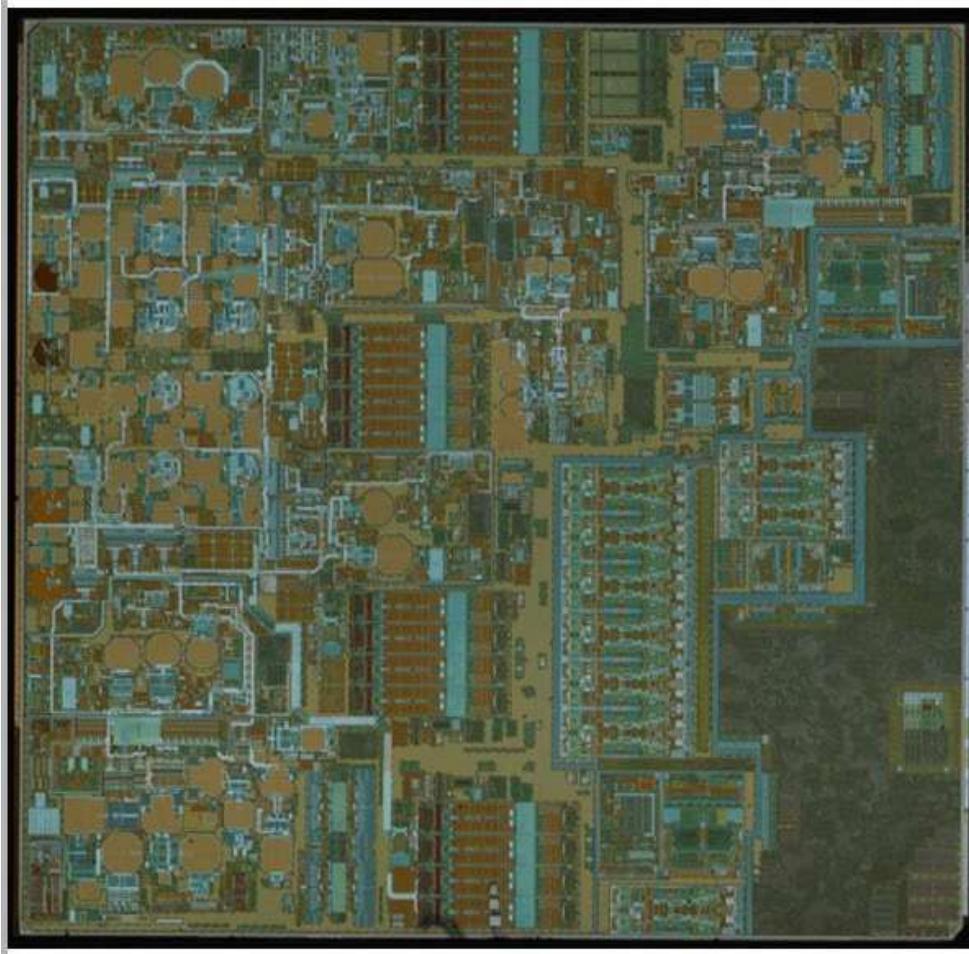
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- Qualcomm [MDM9655](#) Snapdragon X16 LTE modem
- Skyworks SkyOne [SKY78140](#)
- Avago [8072JD130](#)
- P215 [730N71T](#) - likely an envelope tracking IC
- Skyworks [77366-17](#) quad-band GSM power amplifier module
- NXP [80V18](#) secure NFC module

# iPhone 8

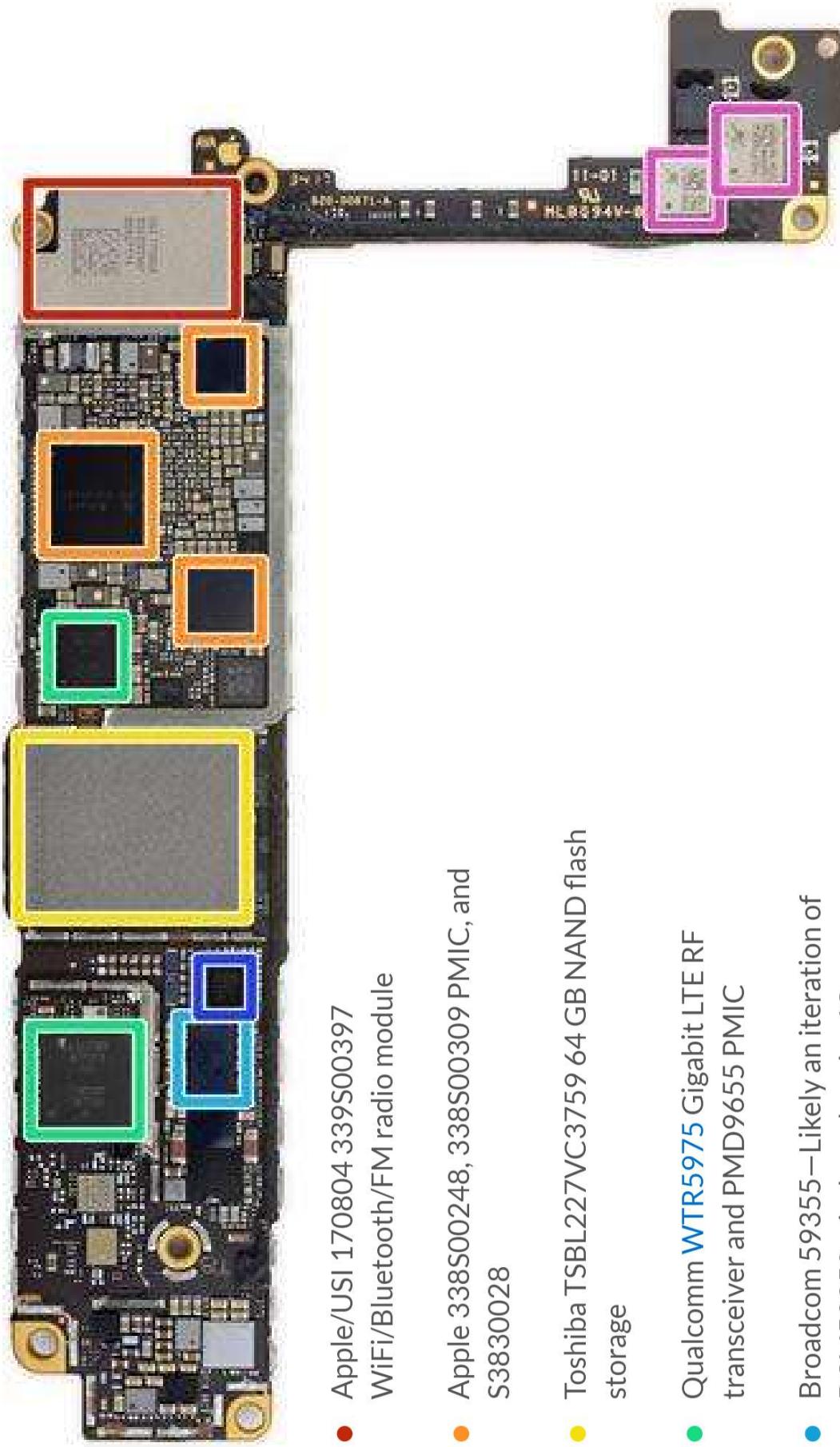


<https://www.qualcomm.com/products/snapdragon-modems-4g-lte-x16>

- Apple **339S00434** A11 Bionic SoC layered over SK Hynix H9HKNNNNBRMMUUR 2 GB LPDDR4 RAM
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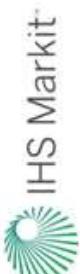


- Apple/USI 170804 339S00397 WiFi/Bluetooth/FM radio module
- Apple 338S00248, 338S00309 PMIC, and S3830028
- Toshiba TSBL227VC3759 64 GB NAND flash storage
- Qualcomm **WTR5975** Gigabit LTE RF transceiver and PMD9655 PMIC
- Broadcom 59355—Likely an iteration of BCM59350 wireless charging IC
- NXP 1612A1—Likely an iteration of the 1610 tristar IC
- Skyworks 3760 3576 1732 RF Switch and SKY762-21 247296 1734 RF Switch

L

Source: company data; Jefferies & Company, Inc. estimates

35



## Apple iPhone 8+ (A1864)

**Preliminary Cost Summary**  
**Total Cost Estimate 8+**  
*Cost Of Manufacturing*

\$288.08
\$7.36

**Total Cost Estimate 7+**  
*Cost Of Manufacturing*

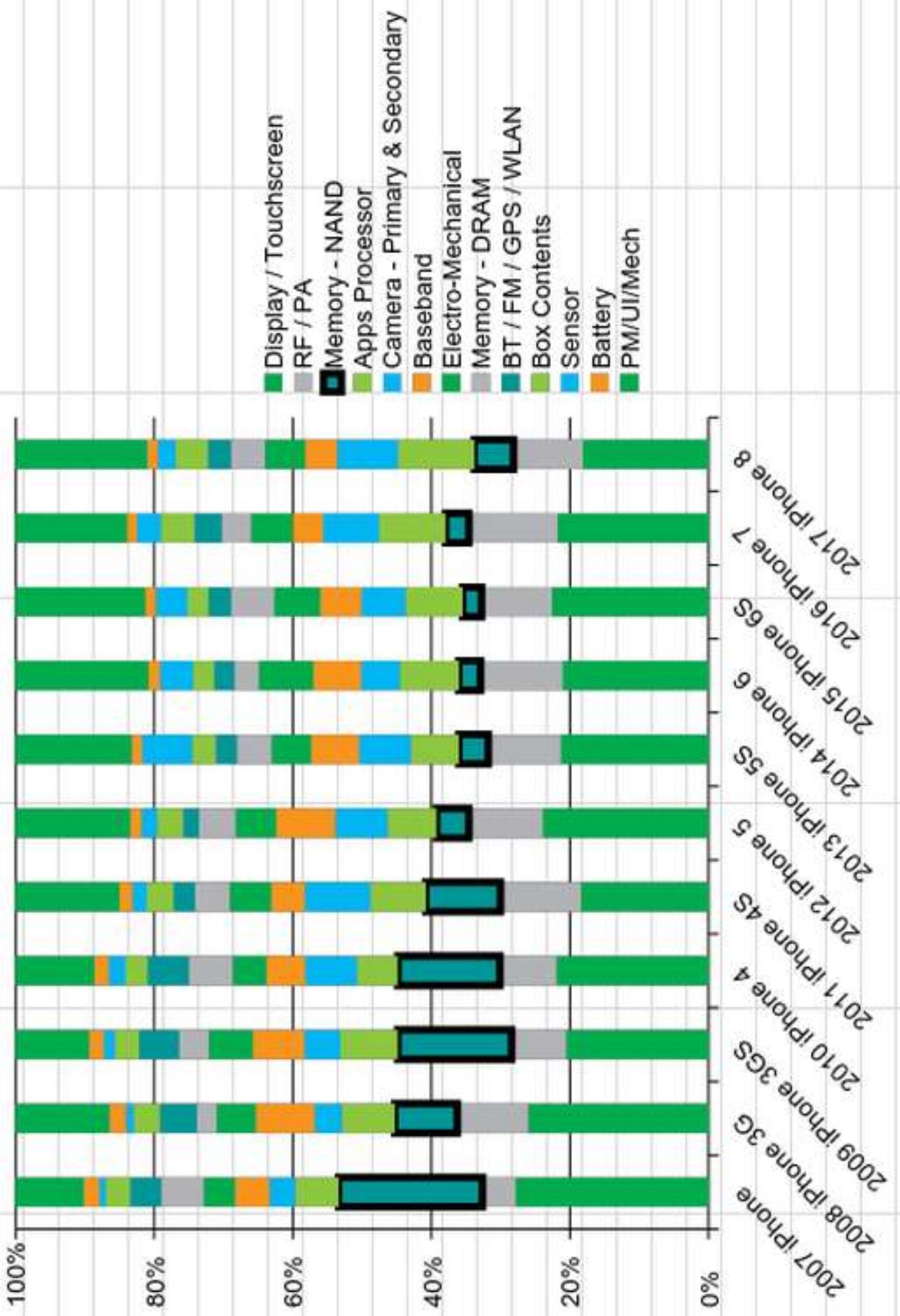
\$270.88
\$6.78

Itemized Components	MfgName	MfgPartNbr	Description	Total Cost	Comment
Display	JDI, LGD, Sharp	5.5" 1920x1080 IPS LCD w/ in-cell touch	\$52.5000		See comments tab
Mechanical / Electro-Mechanical Components				\$50.9500	
Chassis + Rear Enclosure			Enclosure, Main, Bottom, Machined 7000-Series Aluminum Alloy w/stainless insert and Gorilla glass rear cover		
Other Mechanical / Electro-Mechanical			PCBAs, Connectors, Taptic Engine, Other		
Cameras				\$32.5000	
Primary Camera Module			Dual, Wide-Angle F1.8 / Telephoto F2.8 12MP w/ OIS		1.2umx1.2um Pixel Size Wide Angle; 1.0x1.0um Pixel Size Telephoto
Secondary Camera Module			7MP F2.2		1.0umx1.0um Pixel Size
Memory				\$31.2000	
NAND (eMMC, MLC, ...)	SANDISK CORP	SDMPEGF12 064G	Flash, NAND, 64GB, TLC		Samsung, Toshiba, SanDisk, Hynix are all vendors
DRAM	MICRON TECHNOLOGY INC	MT53D384M64D4NY-046 XT:D	SDRAM, LPDDR4, 3GB, PoP		
Apps Processor	Apple		Apple A11 Bionic, 64-Bit 6-Core CPU, 3-Core GPU, 10nm	\$27.5000	

Luca Fanucci

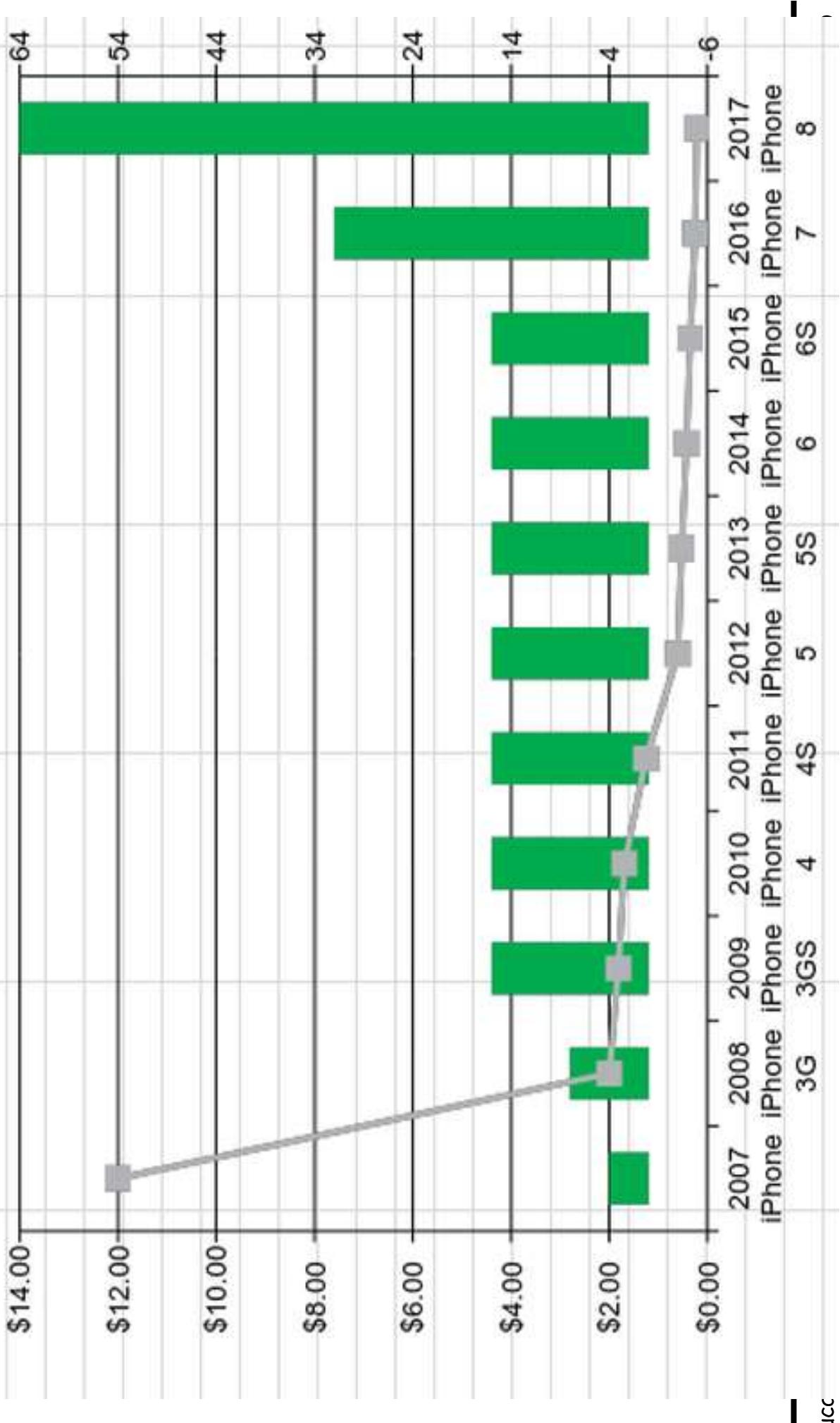
Source: company data; Jefferies & Company, Inc. estimates

Itemized Components	MfgName	MfgPartNbr	Description	Total Cost	Comment
RF / PA Section				\$24,6000	
RF Transceiver	QUALCOMM	WTR5975	RF Transceiver, Multi-Mode, Multi-Band		
Transmit Modules	BROADCOM LTD	AFEM-8072	Transmit Module		
PANS	SKYWORKS SOLUTIONS INC	SKY78140-22	Transmit Module		
Other RF/PA	SKYWORKS SOLUTIONS INC	SKY77366-17	Remaining PAMs ad other RF components not listed above		
Power Management Components				\$16,0500	
Apps Processor Power Management	DIALOG SEMICONDUCTOR GMBH		Power Management IC		
Baseband & Other Power Management	QUALCOMM	PND9655	Power Management IC		
Wireless Charging Element + Supporting Compon	BROADCOM LTD	BCM59355A2IUB3G	Wireless Charging IC		
Other Power Management Components			Remaining power management ICs, regulators, converters, LED drivers, etc.		
Baseband IC	QUALCOMM	MDM9655	Baseband Processor, Multi-Mode, 14nm - CAT16 Modem	\$11,5000	
User Interface Components				\$11,2800	
NFC Controller	NXP SEMICONDUCTORS	PN80V	NFC Controller		
Audio Codecs	CIRRUS LOGIC INC	338S00248	Audio Codec		
Other	CIRRUS LOGIC INC	CS35L26	Audio Power Amplifier		
Includes camera flash, and other interface ICs					
Other Modules					
WLAN / BT Module(s)	MURATA	339S00399	BT / WLAN Module, IEEE802.11ac, Bluetooth 5.0	\$7,3500	
Sensors				\$6,6500	
Fingerprint Sensor Module			Fingerprint Sensor Module		
Accelerometer / Gyroscope, 6-Axis			Accelerometer / Gyroscope, 6-Axis		
Electronic Compass	ALPS ELECTRIC CO LTD		Electronic Compass		
Barometric Pressure Sensor	BOSCH SENSORTEC GMBH	BMP28X	Barometric Pressure Sensor		
Color Sensor	AMS AG		Color Sensor		
Proximity - time-of-flight			Proximity - time-of-flight		
Battery Pack(s)	HUIZHOU DESAY BATTERY CO LTD		Battery, Li-Polymer, 3.82V, 2691mAh, 10.28Wh	\$4,4500	
Box Contents			Includes pkg & literature	\$11,5500	
Charger, 5V, 1A, AC to USB Type A			Charger, 5V, 1A, AC to USB Type A		
Stereo w/ Apple Lightning Plug			Stereo w/ Apple Lightning Plug		
Headphone Jack Adapter			Headphone Jack Adapter		
USB to Apple Lightning Cable			USB to Apple Lightning Cable		



■ BOM cost/GB

■ Memory Density (GB)



Luc

Let's continue !!

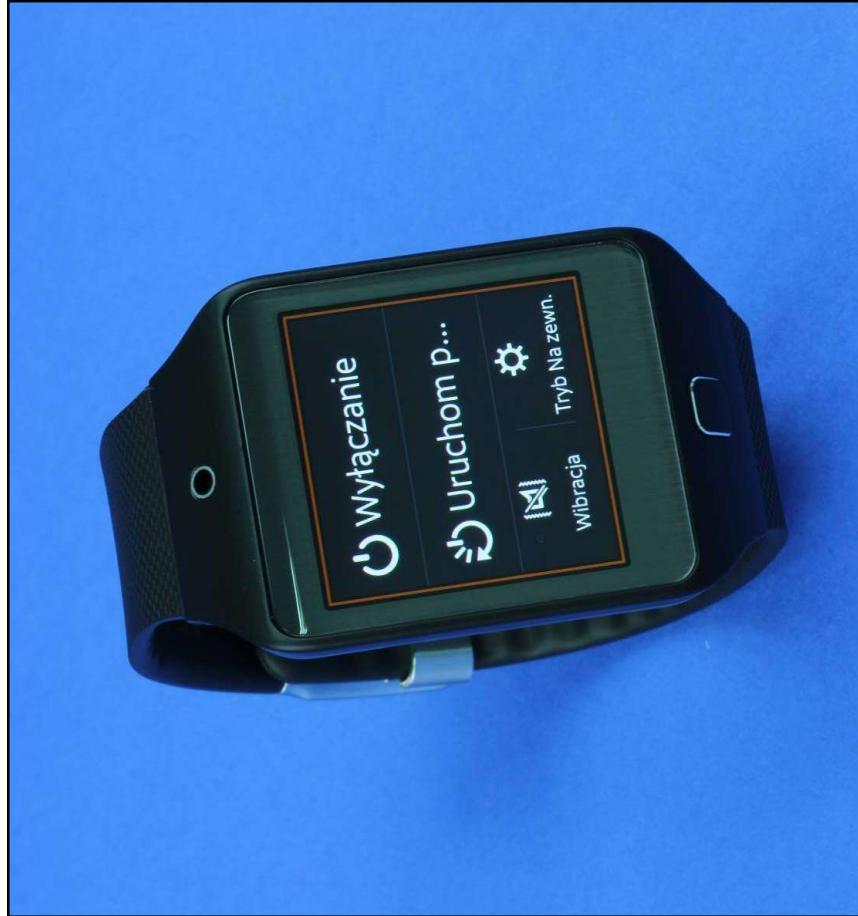
# Some wearable products in the market



# Samsung Gear 2 Neo SM-R381

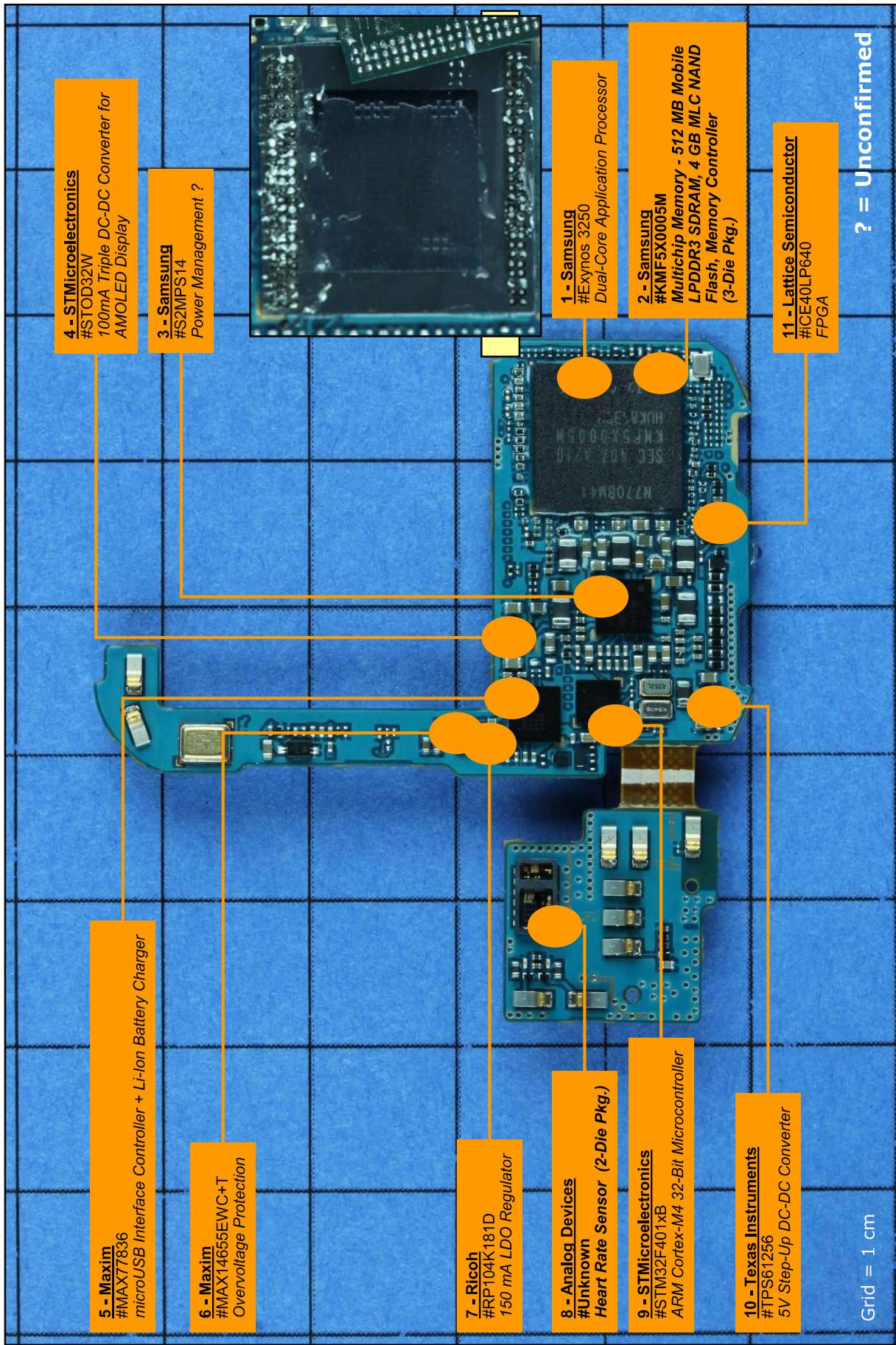
## Product Description

The Samsung Gear 2 Neo is a low-energy Bluetooth 4.0-enabled smartwatch that's resistant to both dust and water (IP67 certified). Besides the supporting functions of a normal wristwatch, it can also receive notifications and applet content when paired with a smartphone via a Bluetooth connection. A built-in **heart rate sensor** allows it to track and record the user's heart rate, while the built-in pedometer logs the numbers of steps taken during a workout routine. There's also a **6-axis accelerometer** and **gyroscope**. All notifications, time, and activity information are displayed on a 1.63-in. Super AMOLED display with 320 x 320 resolution, 16M colors, and capacitive touchscreen for easily navigating through various screens. Connectivity includes Bluetooth 4.0 LE + EDR; microUSB (for battery charging); IrLED, which allows the user to remotely control other devices; and FM radio. The Gear 2 Neo runs the open-source Tizen wearable platform (a Linux-based OS) on a 1 GHz dual-core Samsung Exynos 3250 application processor. Other features include 4 GB of internal memory, vibrational alerts, and a built-in music player that connects to Bluetooth headsets. The Gear 2 Neo is powered by a 3.8 V, 300 mAh Li-Polymer battery that supplies up to 48 hours of use time, and 144 hours standby time. It also comes with a USB AC adapter and docking station for charging.

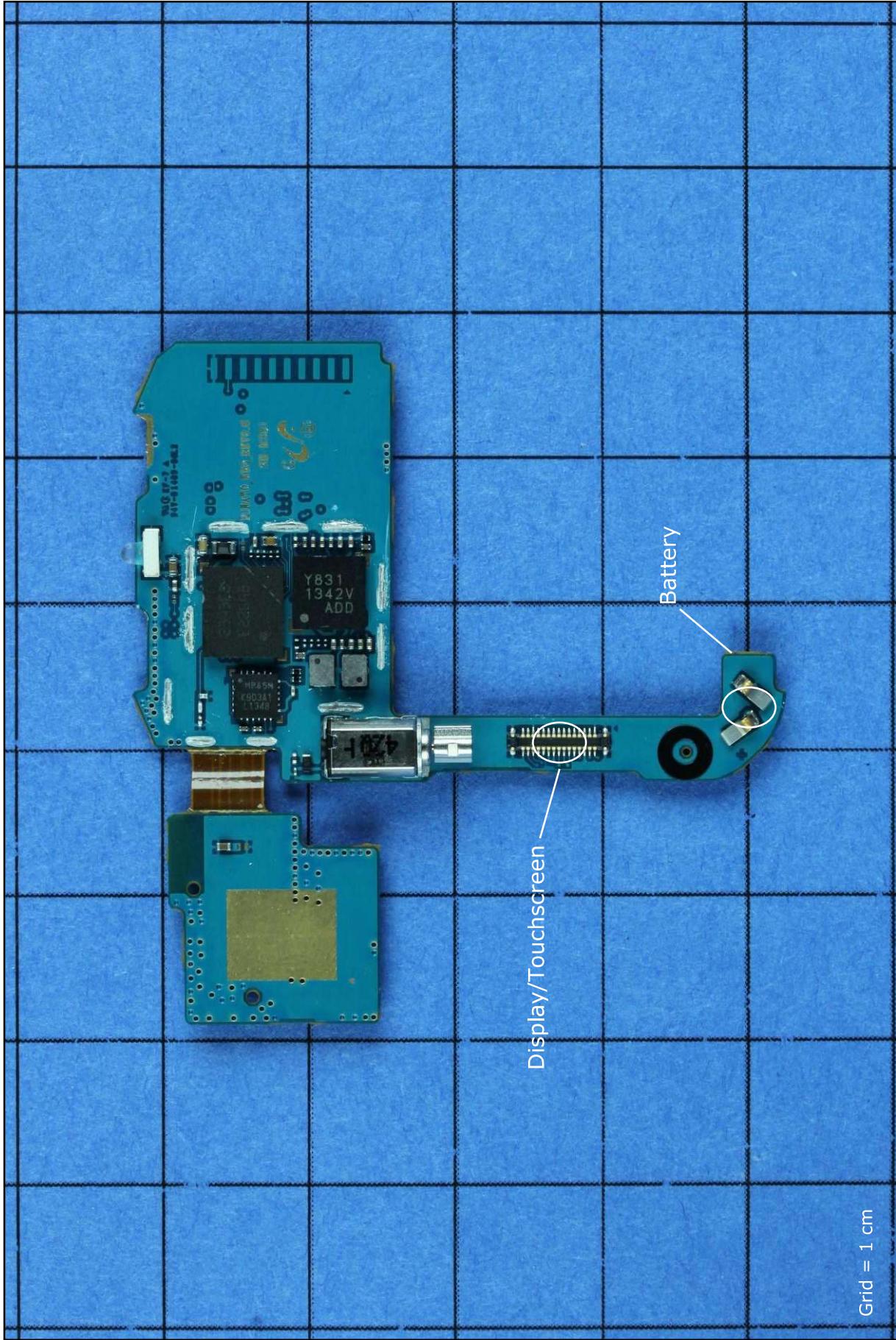




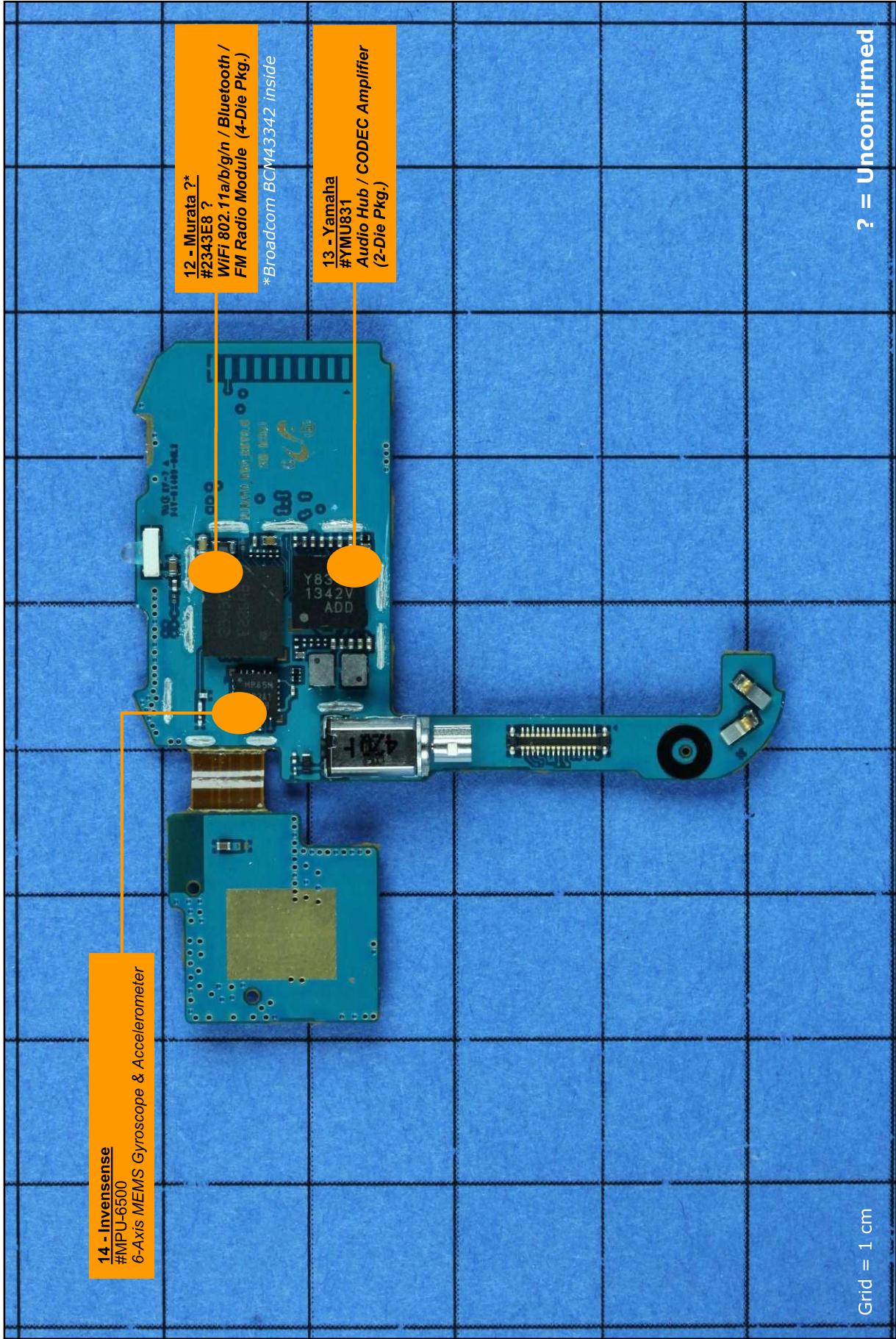
# Main Board (Side 1 IC Identification)



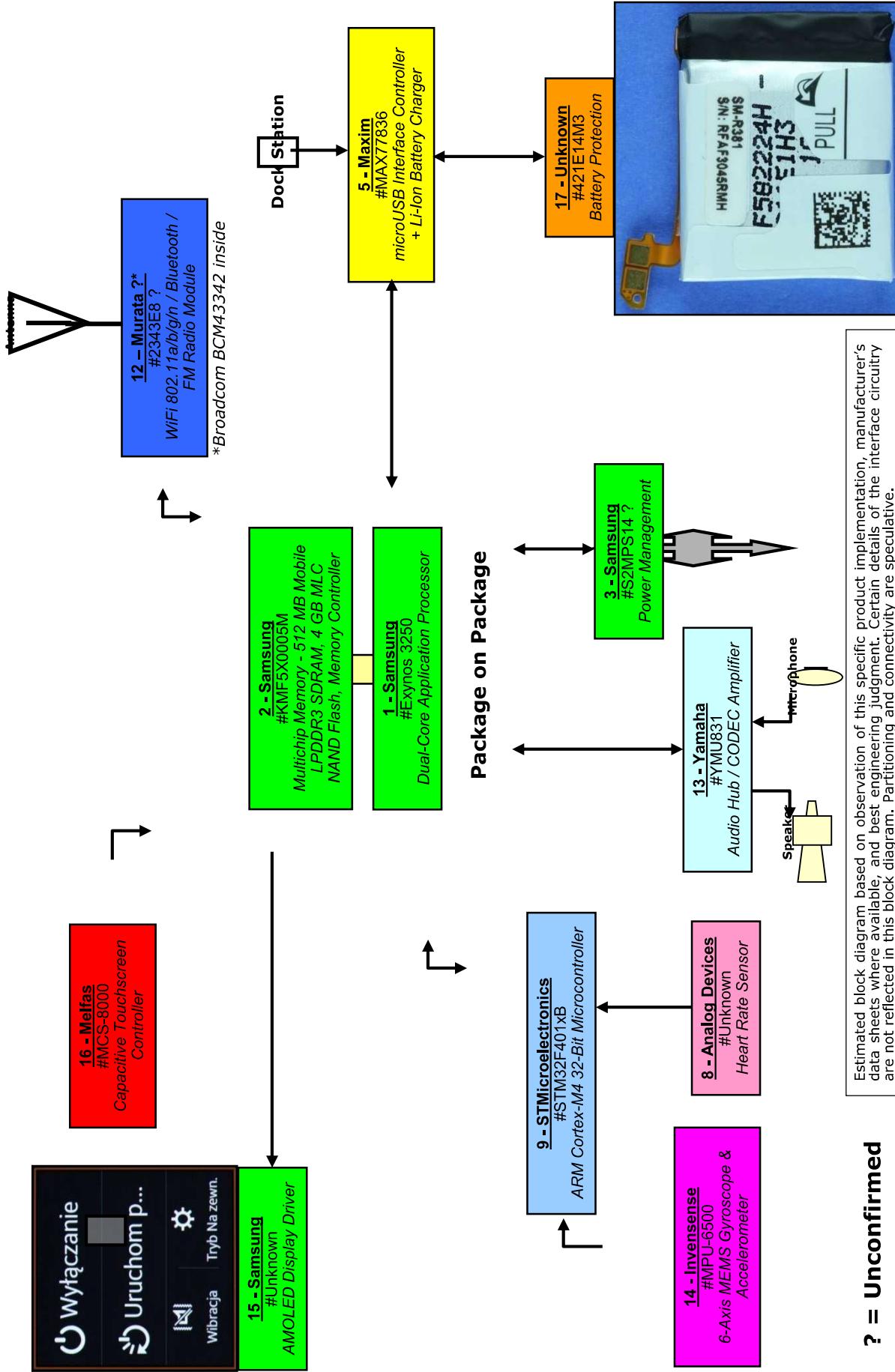
## Main Board (Side 2)



# Main Board (Side 2 IC Identification)



# Block Diagram



? = Unconfirmed

Estimated block diagram based on observation of this specific product implementation, manufacturer's data sheets where available, and best engineering judgment. Certain details of the interface circuitry are not reflected in this block diagram. Partitioning and connectivity are speculative.

# Garmin Vivofit F4 ARND00

## Product Description

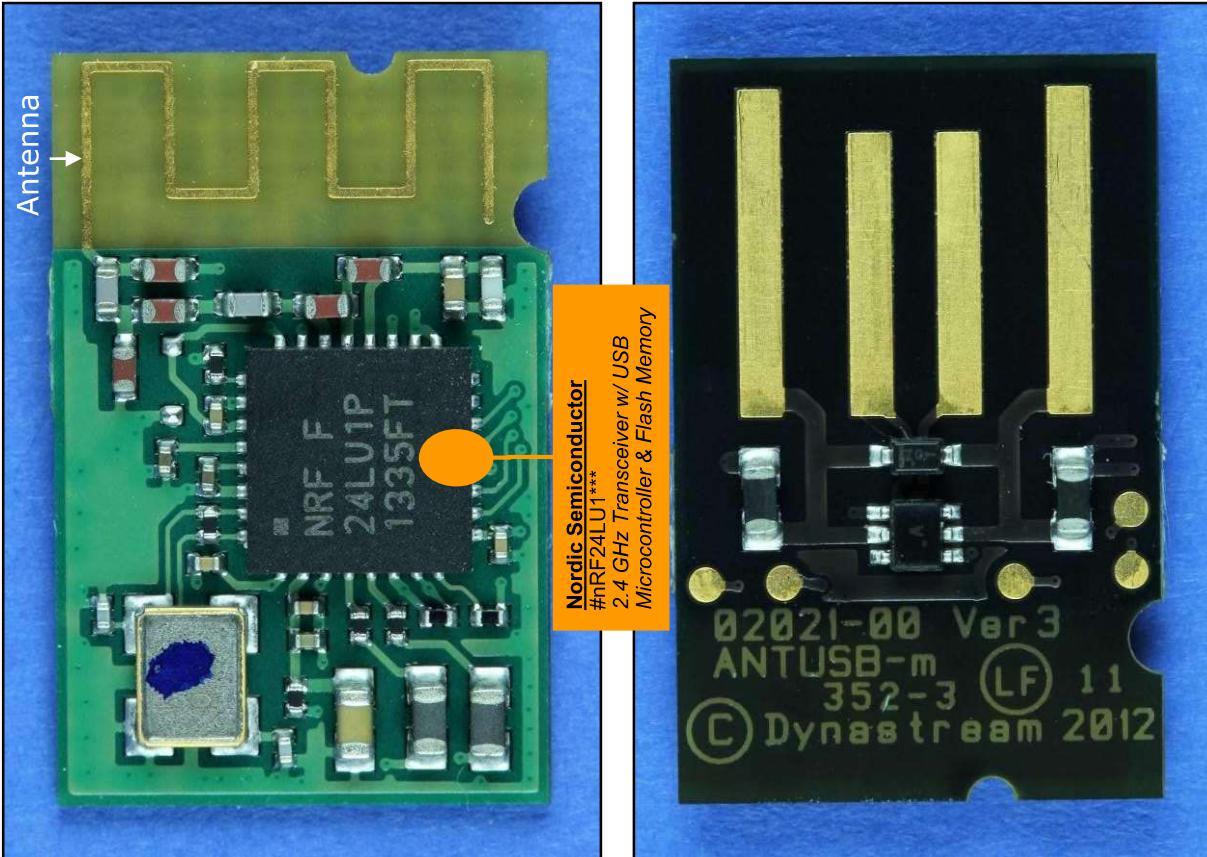
The Garmin Vivofit is a wearable fitness device that collects and records personal health data during physical activities like walking or running as well as while you're resting or sleeping. It tracks your progress 24/7 and can operate for over a year on a single battery charge. All collected data can be easily transferred via Bluetooth 4.0 or USB ANT+ to a computer or compatible mobile device via the Garmin Connect Mobile app. With the touch of a button, you can also sync the data with the Garmin Connect online fitness community for tracking your progress and getting support in meeting personal fitness goals. The Vivofit features a 1.15-in. 5-segment LCD display. It runs on a Nordic Semiconductor nRF51422 ANT/Bluetooth SOC with ARM Cortex M0 CPU, 16 KB RAM, and 256 KB flash. It's also water resistant to a depth of 50 meters and features a real-time clock with alarm and **3-axis MEMS accelerometer**. The Garmin Vivofit is powered by two CR1632 3 V batteries that provide a year of use time.



# Component Arrangement



# Supporting Materials (ANT+/BT USB Adapter)

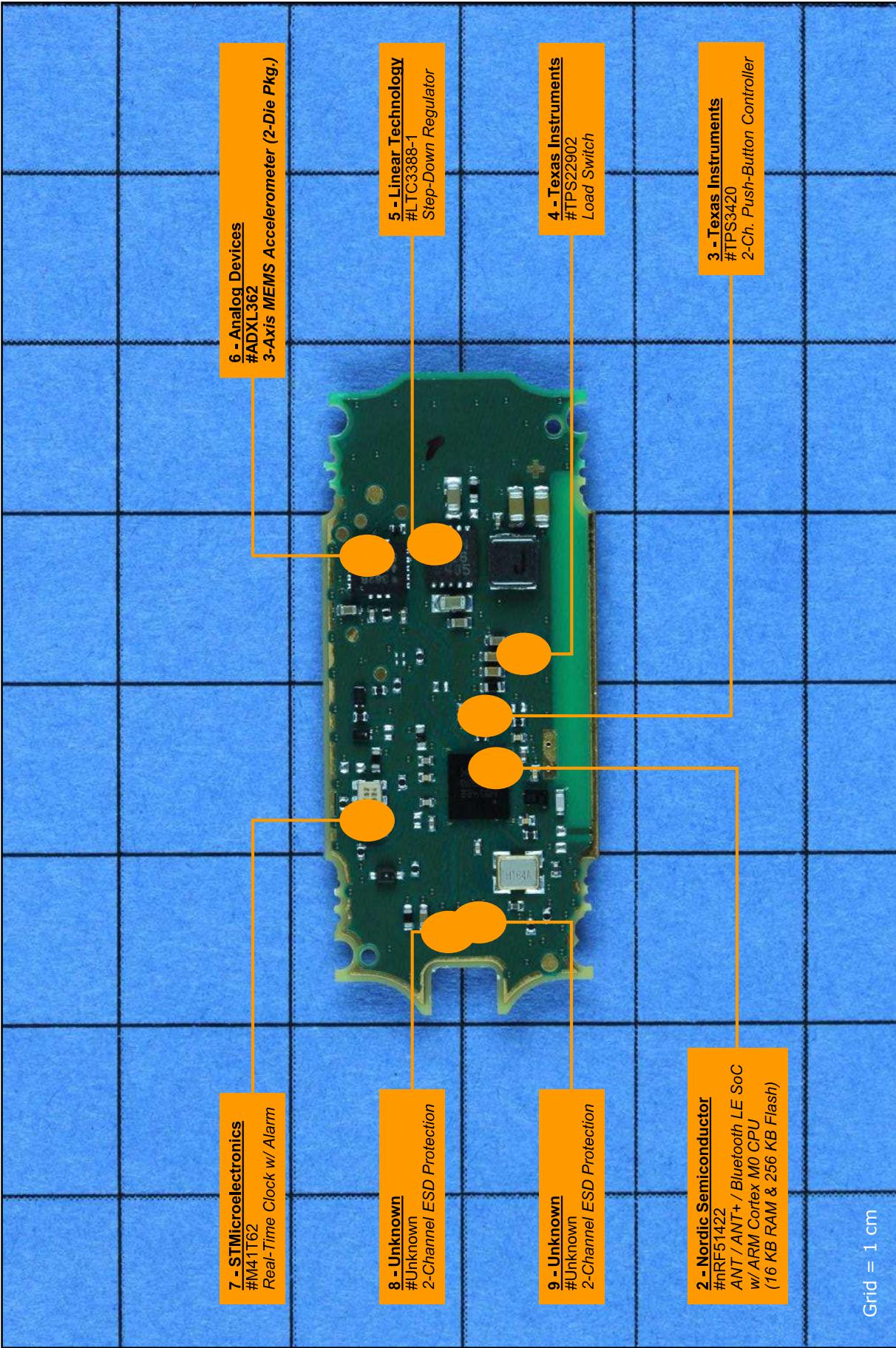


Cost Breakdown as follows:  
IC\*: \$0.73  
PCB\*\*: \$0.11  
Ceramic Crystal\*: \$0.20  
Active Discretes\*: \$0.06  
Passive Discretes\*: \$0.27  
Enclosures: \$0.10  
**Total: \$1.47**

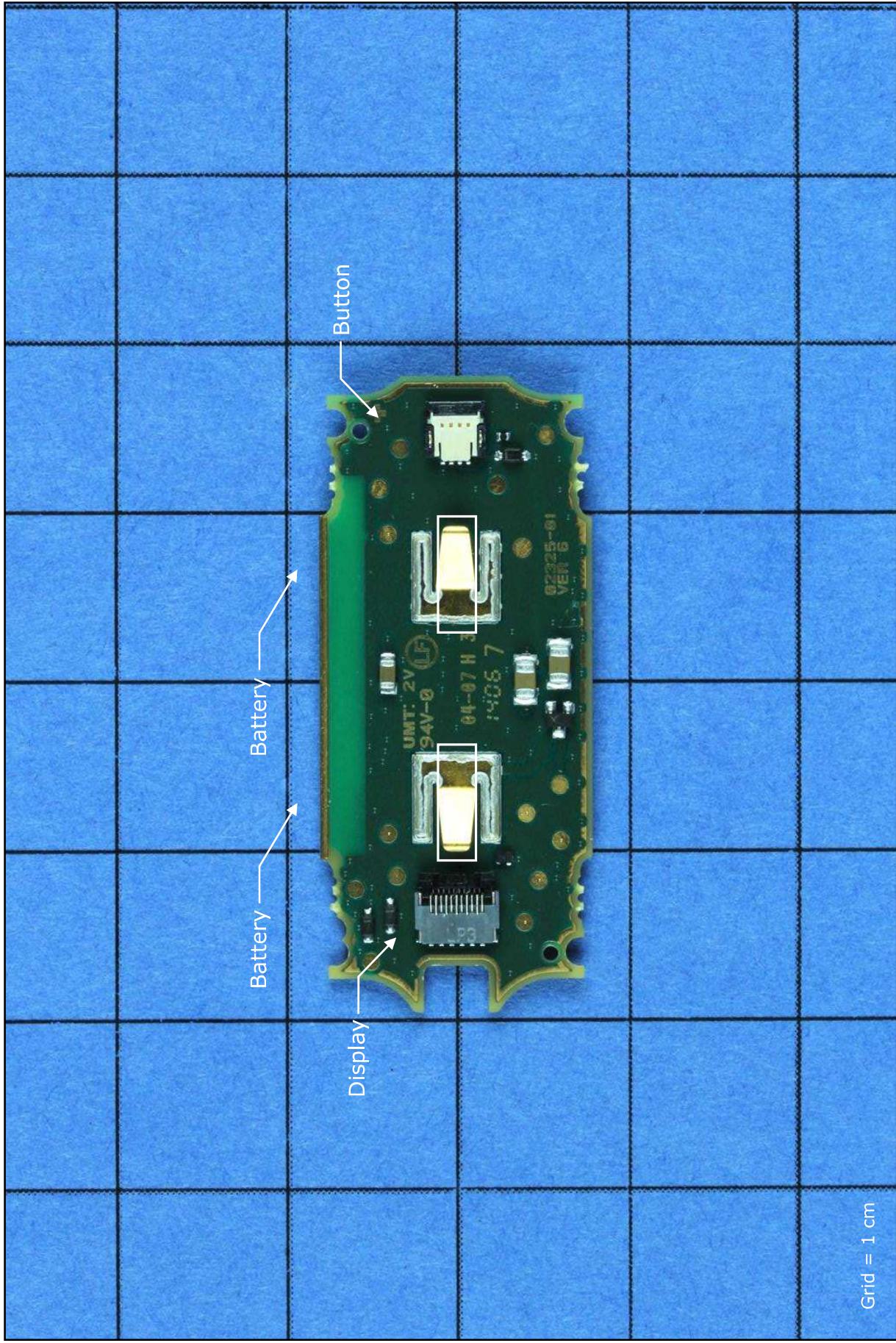
\* Includes  
insertion cost

\*\* Includes  
test cost

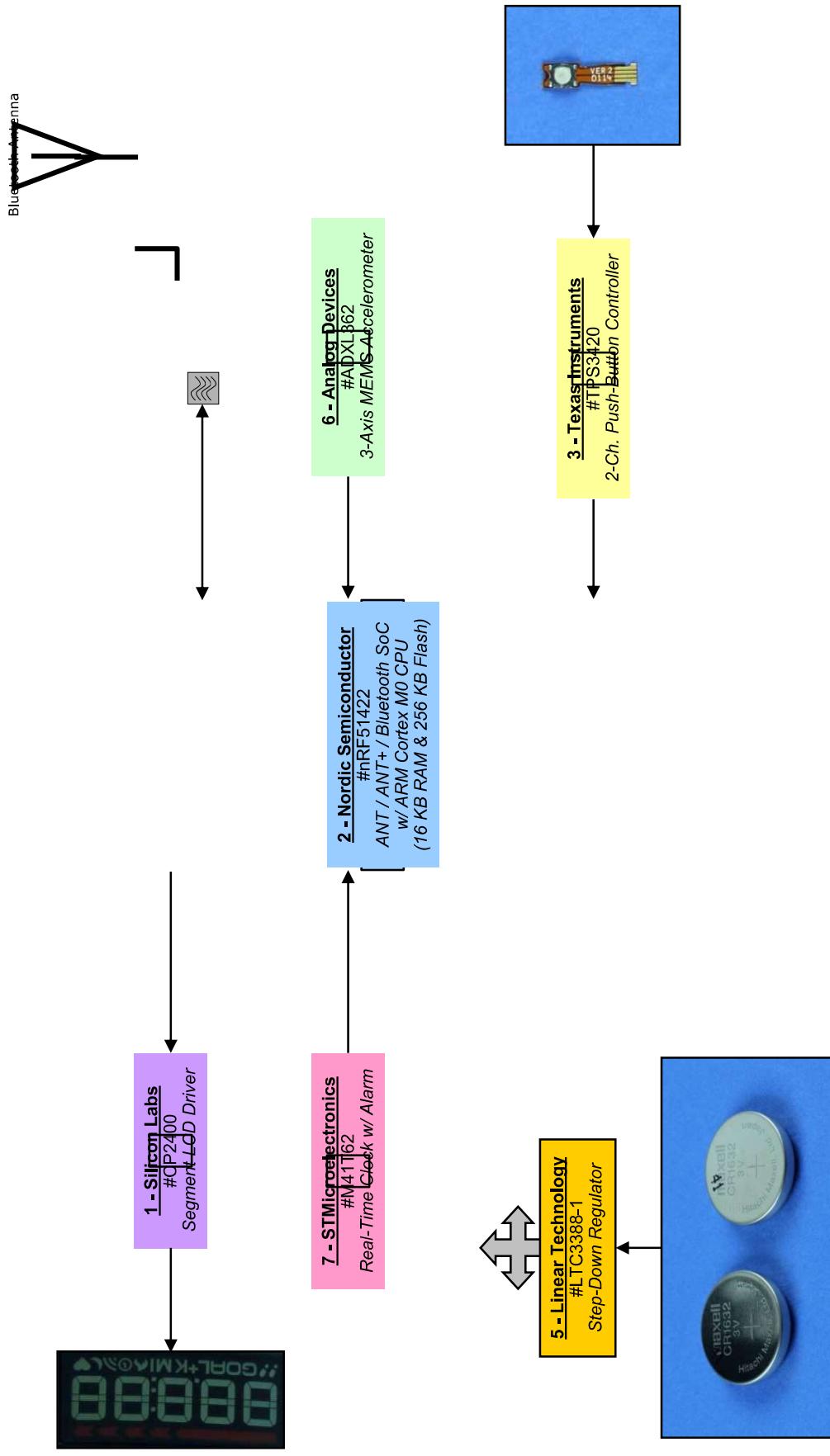
# Main Board (Side 1 IC Identification)



## Main Board (Side 2)



# Block Diagram



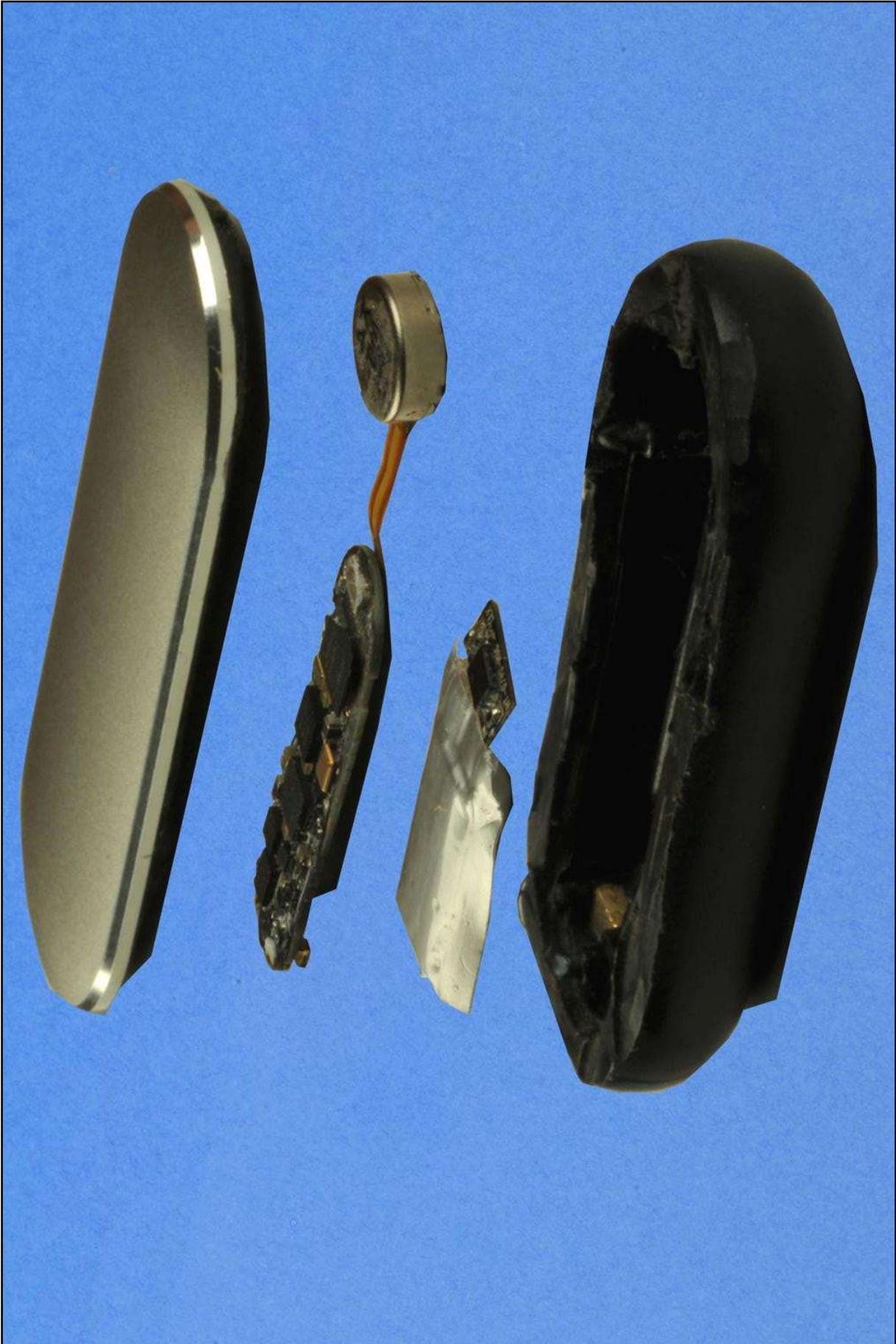
Estimated block diagram based on observation of this specific product implementation, manufacturer's data sheets where available, and best engineering judgment. Certain details of the interface circuitry are not reflected in this block diagram. Partitioning and connectivity are speculative.

# Xiaomi Mi Band XMSH01HM

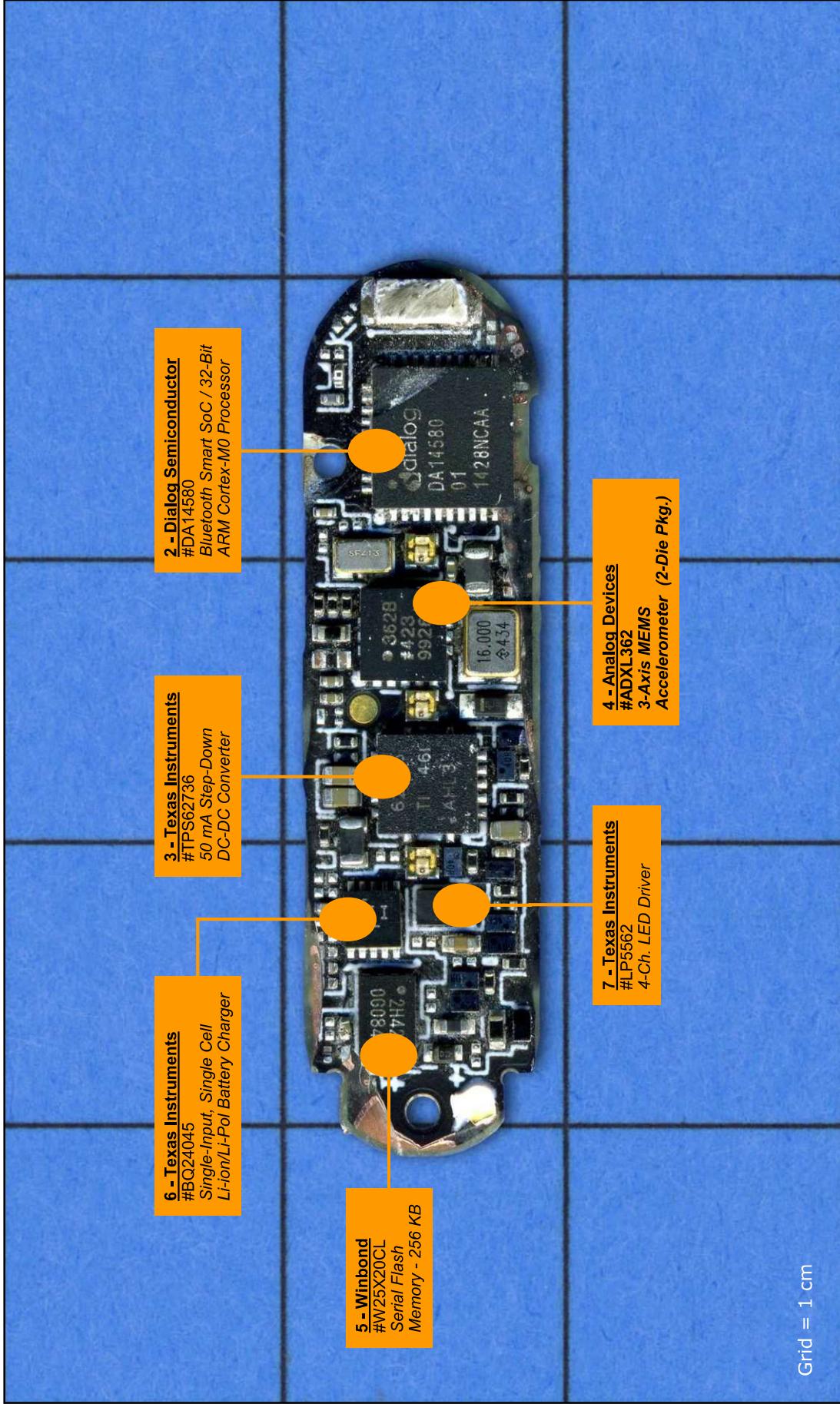
## Product Description

The Xiaomi Mi Band XMSH01HM is a wearable fitness monitor that also tracks sleep patterns. The core unit has a polycarbonate body with a brushed aluminum finish and three small LED lights on top. The LEDs glow in different colors to indicate the progress of a workout or alert you to low battery charge, incoming email, or a WhatsApp notification. The core unit fits into a wristband made of TPSiV, a durable silicone material. The Mi Band can be worn on either wrist and is water resistant (IP67). It features Dialog Semiconductor's power-efficient DA14580 Bluetooth Smart SoC as well as a **3-axis MEMS accelerometer** from Analog Devices. The Mi Band pairs automatically with smartphones running Android 4.4 "KitKat" so that it doesn't need to be turned on and off. Built-in vibration motors allow the device to function as an alarm clock, while its Smart Alarm feature wakes you at just the right moment in your sleep cycle. Via a downloadable app (in Chinese or English), the Mi Band also tracks sleep quality, tallies total daily distance and average number of steps, logs historical data, and shares results via social media. You can also use it to unlock your smartphone without a password. It's powered by a 3.7 V, 41 mAh Li-Polymer battery that supplies up to 30 days of standby power on a single charge. For recharging, the core unit slips into an included USB charging cable, which can be plugged into a PC or wall charger.



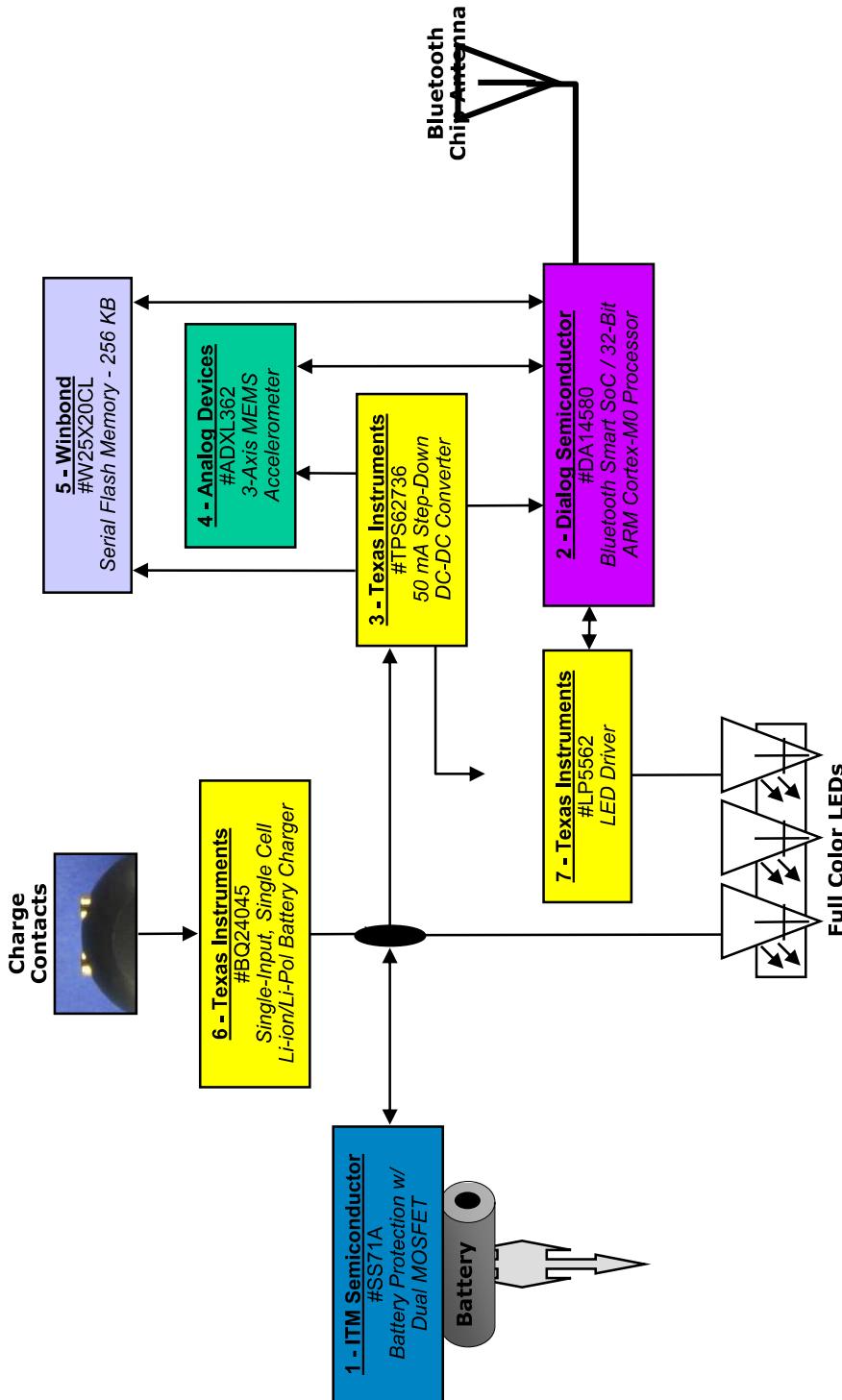


# Main Board (Side 1 IC Identification)



Grid = 1 cm

# Block Diagram



Estimated block diagram based on observation of this specific product implementation, manufacturer's data sheets where available, and best engineering judgment. Certain details of the interface circuitry are not reflected in this block diagram. Partitioning and connectivity are speculative.

# LG G Watch W100

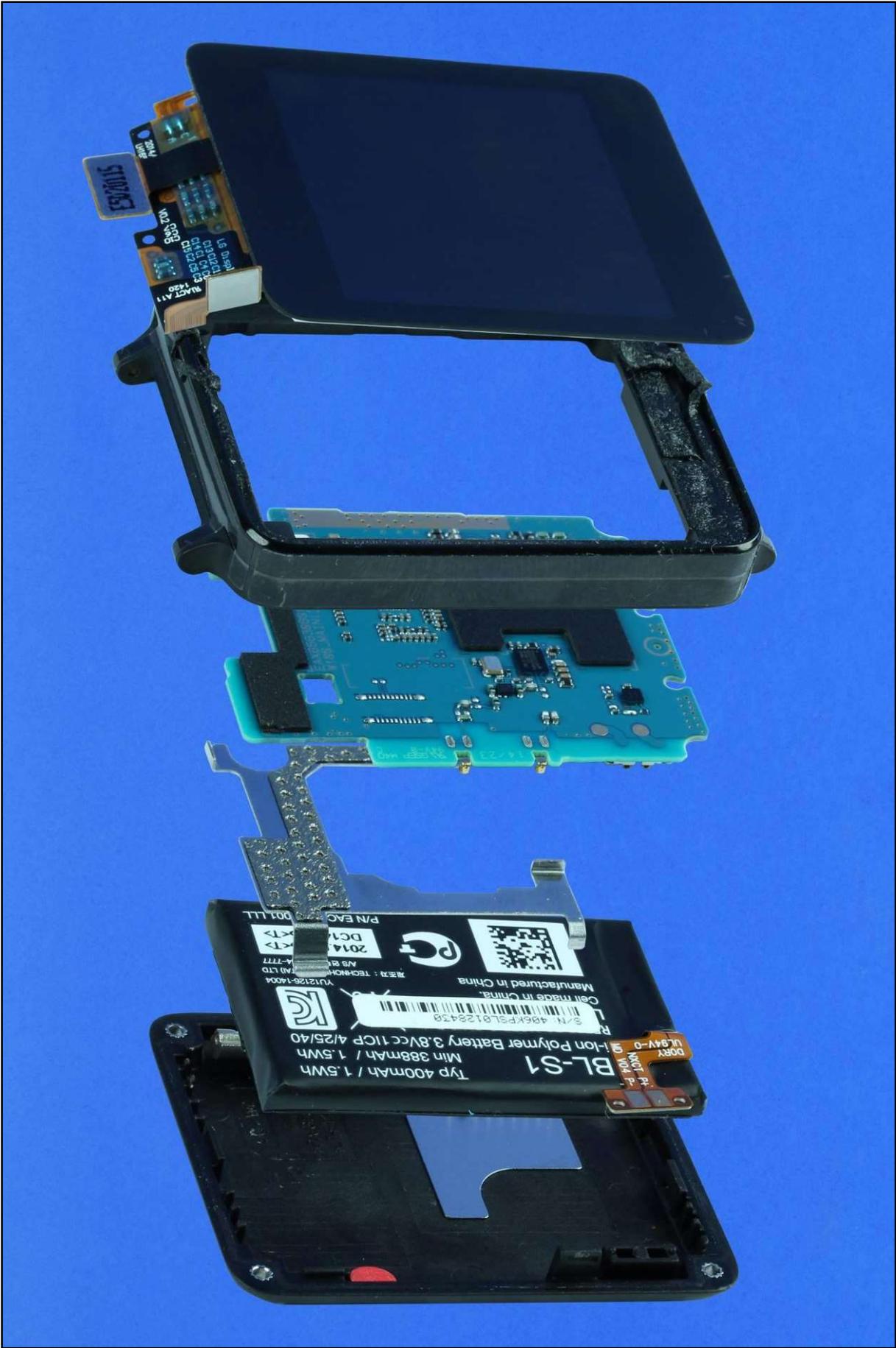
## Product Description

The LG G Watch W100 is a IP67-certified smartwatch and activity tracking device worn like a regular wristwatch. All notifications, time, and activity information are displayed on a 1.65-in. IPS TFT-LCD display with 280 x 280 resolution, 16M colors, and a Corning Gorilla Glass 3 overlay for extra durability. Navigating to various screens is made possible using the multitouch capacitive touchscreen.

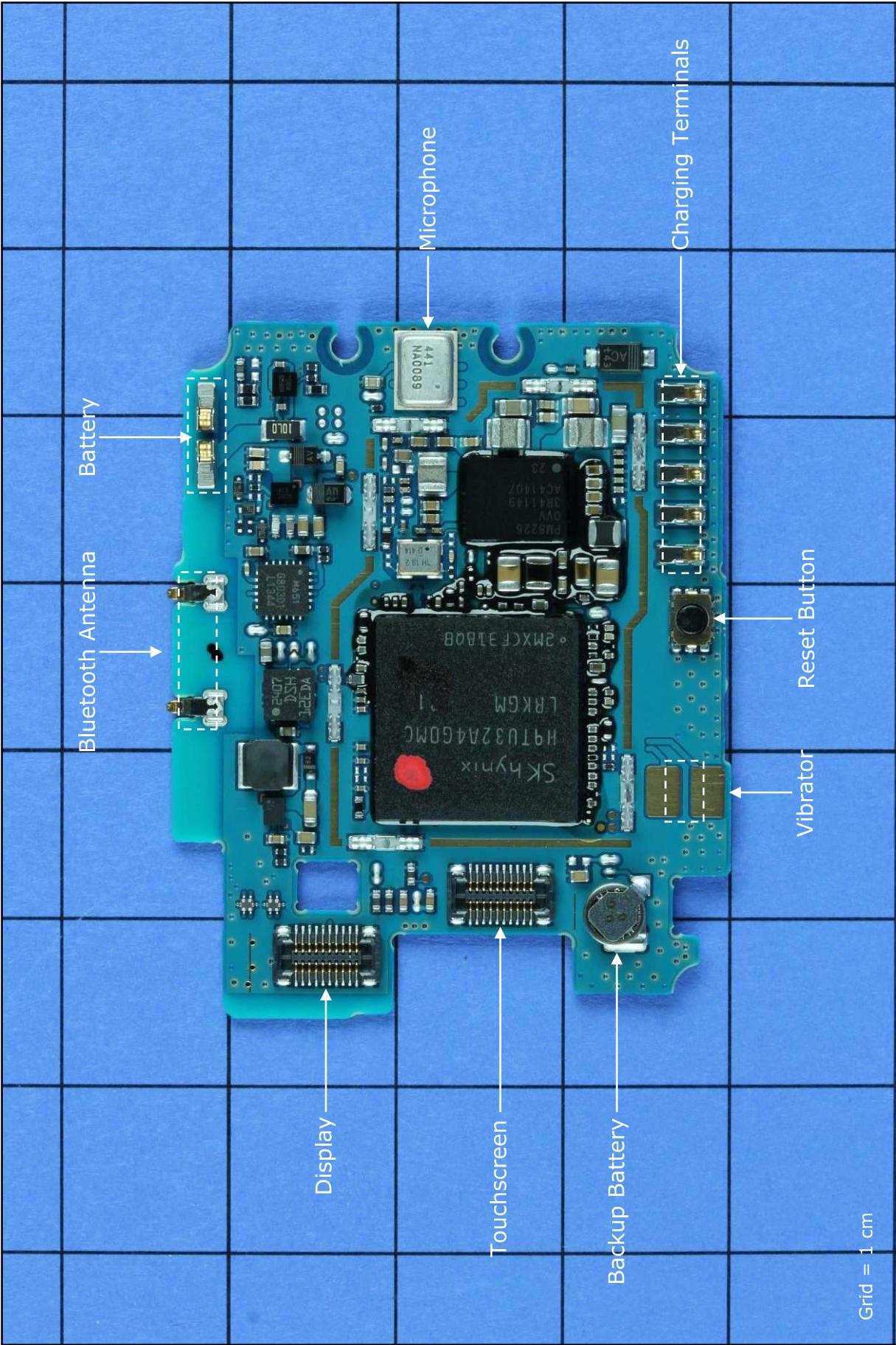
The G W100 runs the Android Wear operating system on a 1.2 GHz quad-core Qualcomm Snapdragon 400 (APQ8026) processor with 512 MB RAM. The smartwatch has 4 GB of internal memory and a built-in microphone for voice activation. Connectivity is provided by Bluetooth 4.0 while a microUSB is located on the included charging cradle. Sensors include a **6-axis MEMS gyroscope & accelerometer**, and **3-axis electronic compass**. The LG G Watch LG-W100 is powered by 3.8 V, 400 mAh Li-Polymer battery. Battery life is unknown.



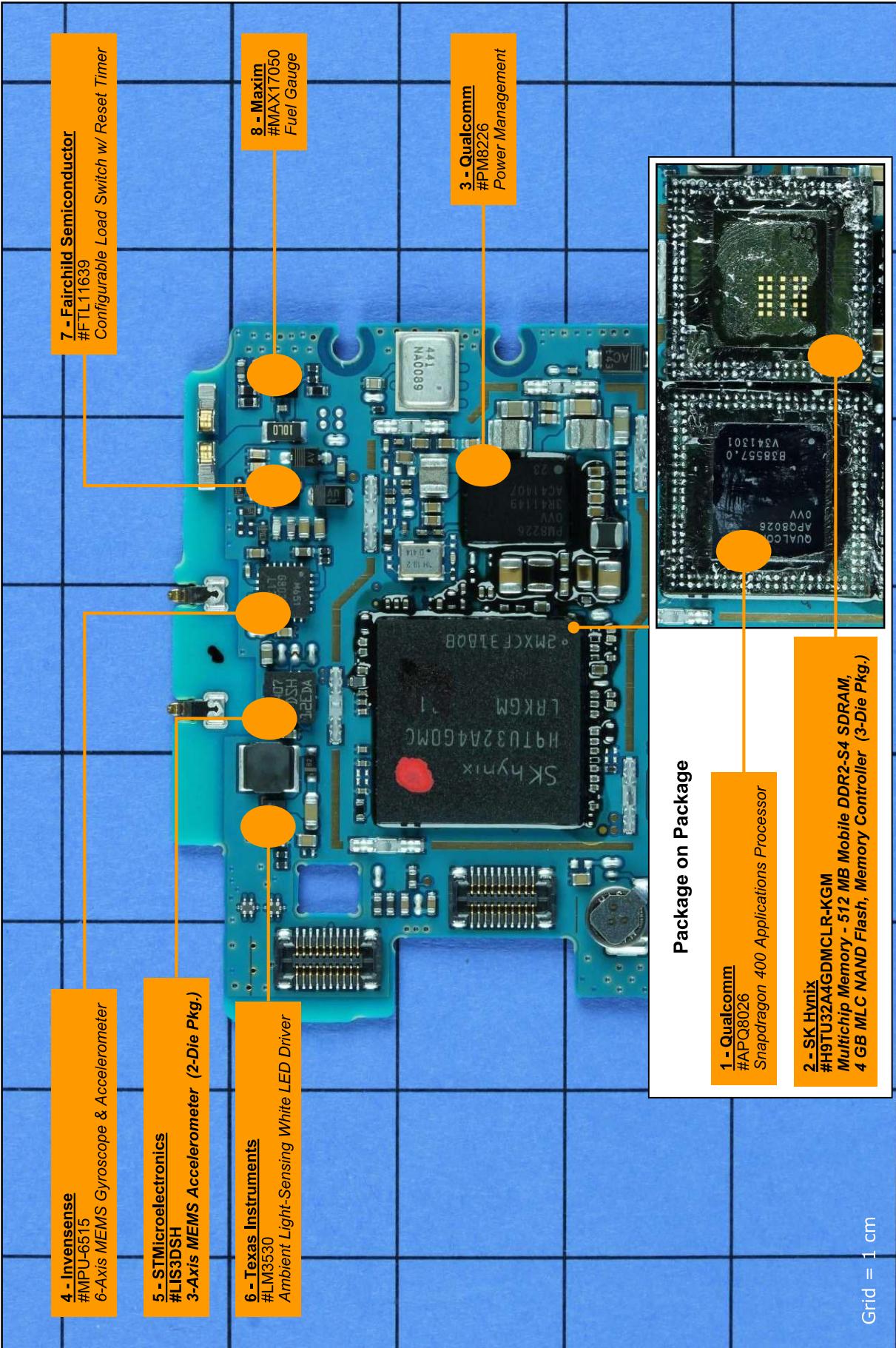
# Component Arrangement



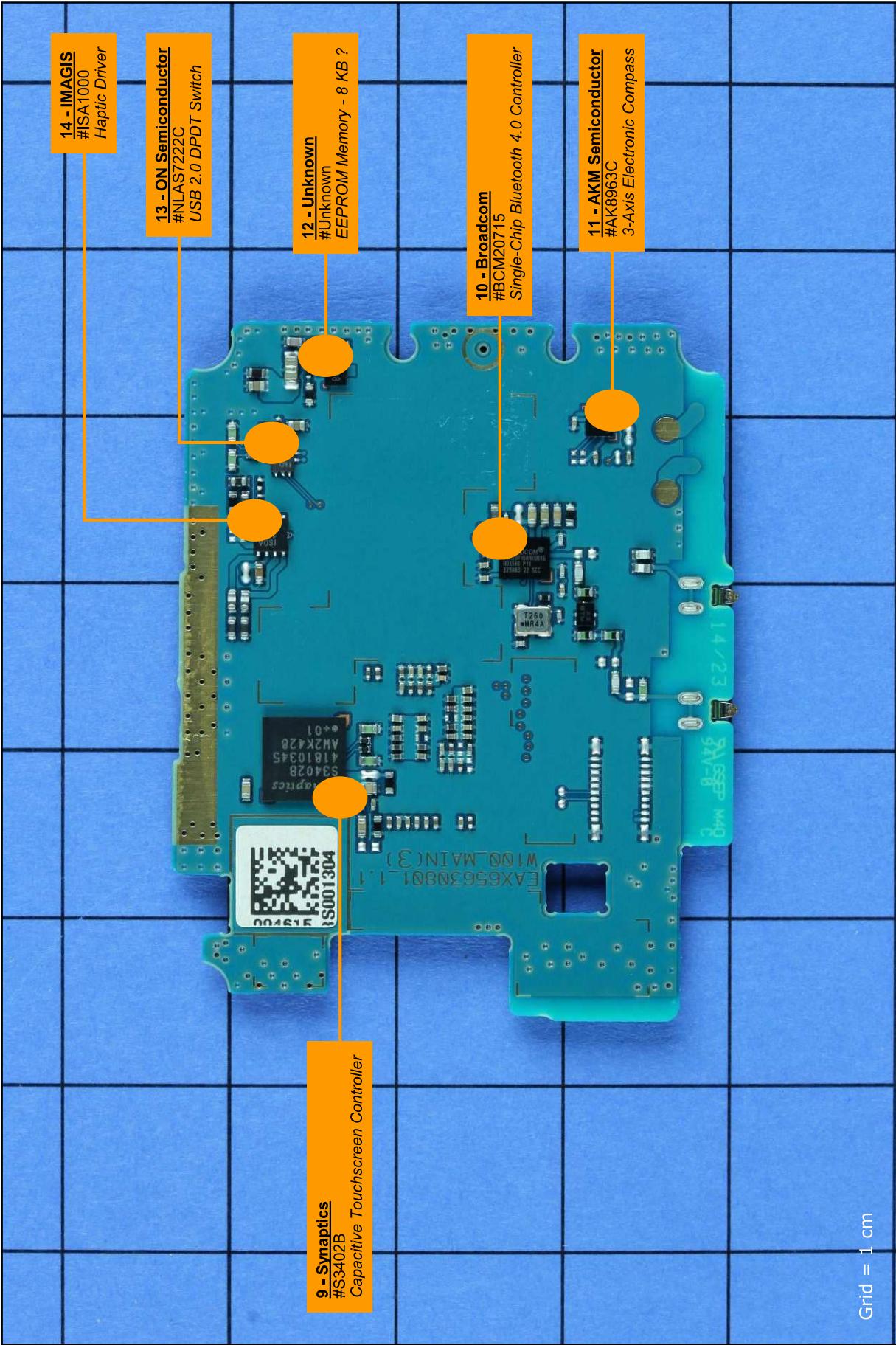
# Main Board (Side 1)



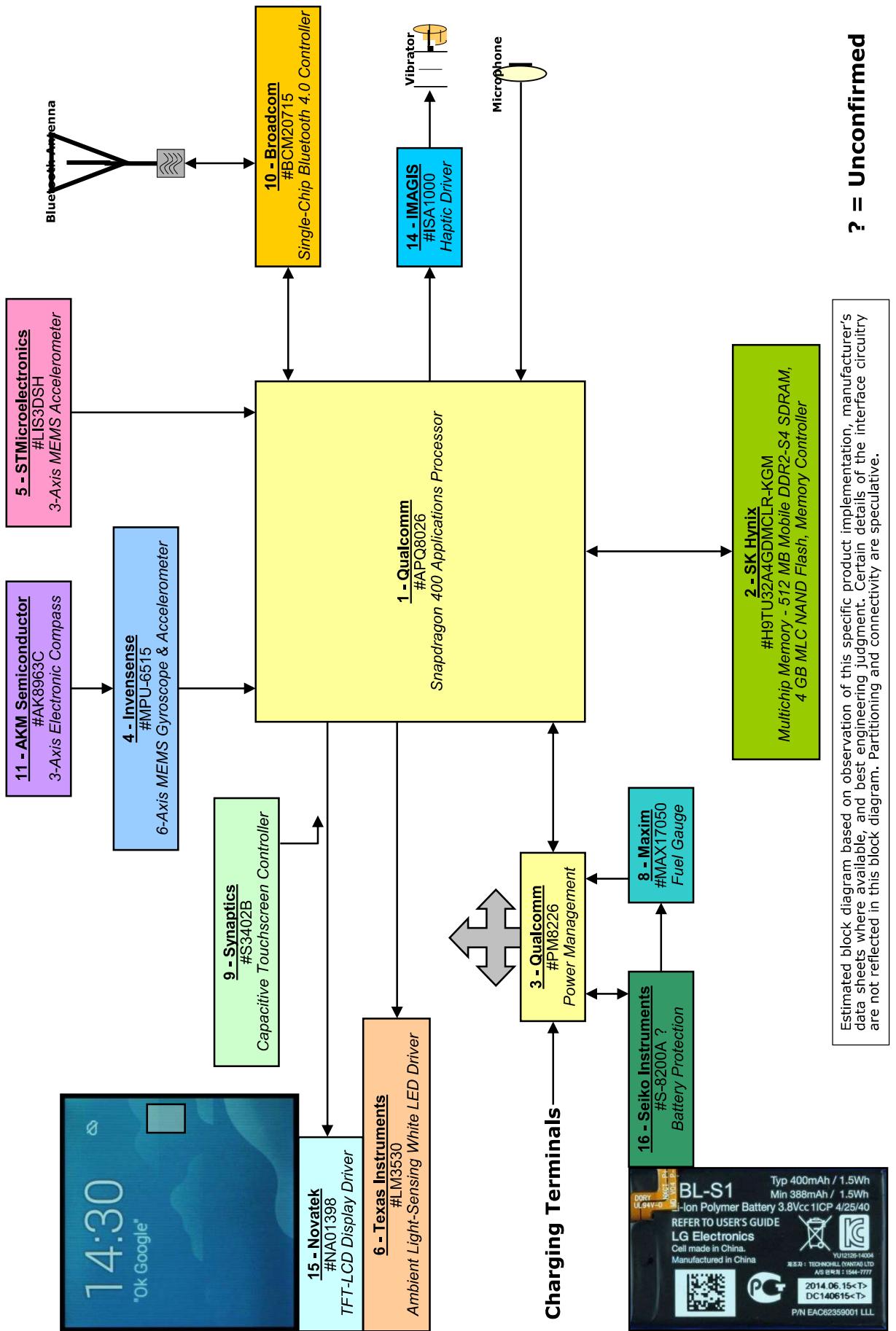
# Main Board (Side 1 IC Identification)



# Main Board (Side 2 IC Identification)



# Block Diagram

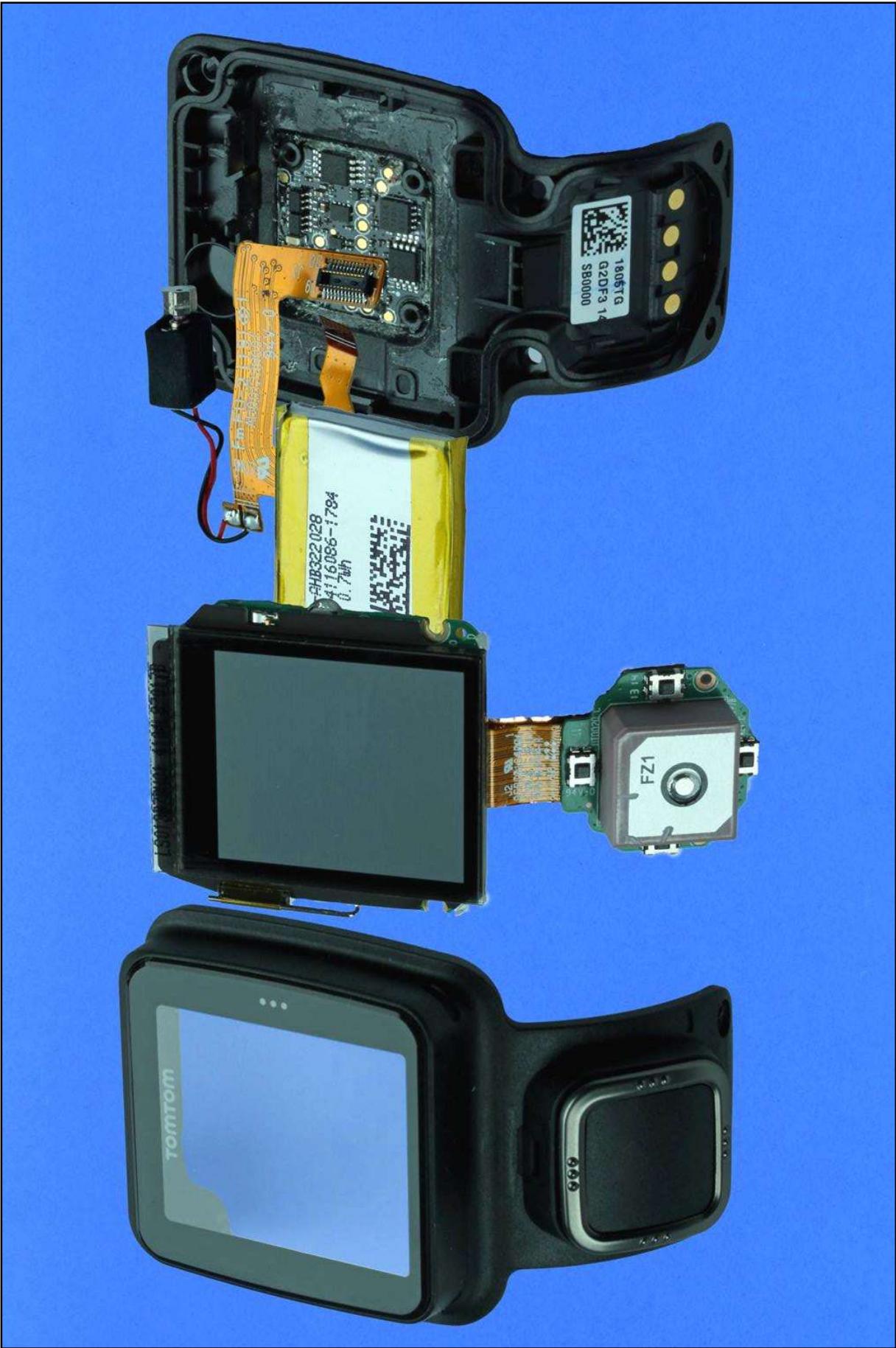


# TomTom Runner Cardio 8RAO

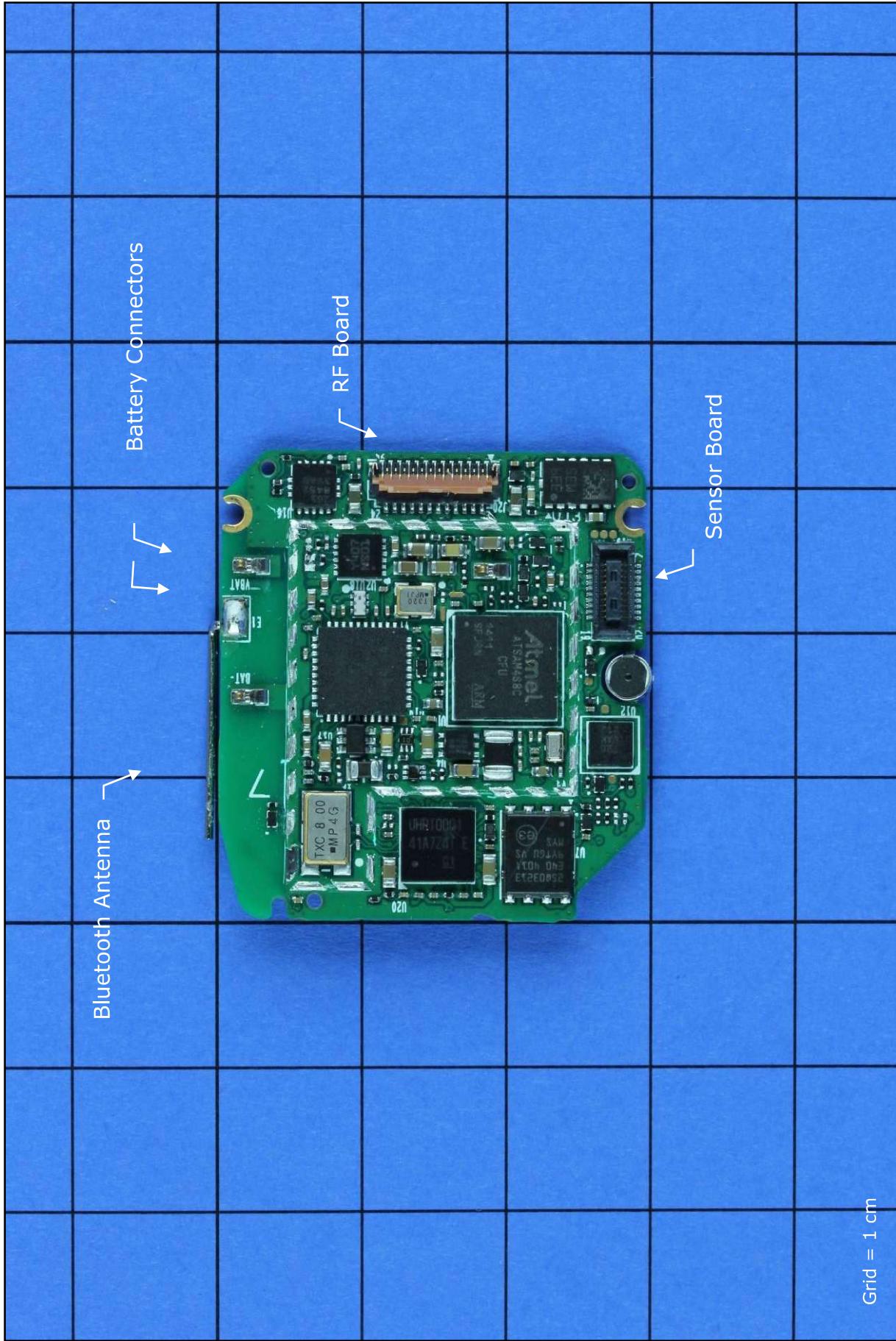
## Product Description:

The TomTom Runner Cardio 8RAO is an activity tracker worn like a wrist watch and featuring a built-in **heart rate sensor** that allows it to track and record the user's heart rate. It's also waterproof to 165 ft./50 m (5 ATM), which allows it to be worn while swimming. Time and activity information are displayed on a 1.3-in. monochrome display with 168 x 144 resolution. Touching the right side of the display turns the backlight on or off. Located directly below the display is a four-way keypad that allows the user to select various menus or return to the default clock function. In the center of the keypad is the GPS antenna. Connectivity includes Bluetooth 4.0 and GPS/GLONASS with QuickGPSfix. The TomTom Runner Cardio 8RAO runs a proprietary operating system on an Atmel 32-bit ARM-based microcontroller. Other features include two **3-axis MEMS accelerometers**, a **3-axis compass**, and vibrational and sound alerts. Supported languages are English, Spanish, German, French, and Italian. The TomTom Runner Cardio 8RAO is powered by a 3.7 V, 190 mAh Li-ion polymer battery that supplies up to 8 hours of use time (GPS + HR). It also comes with a custom USB docking connector for charging.

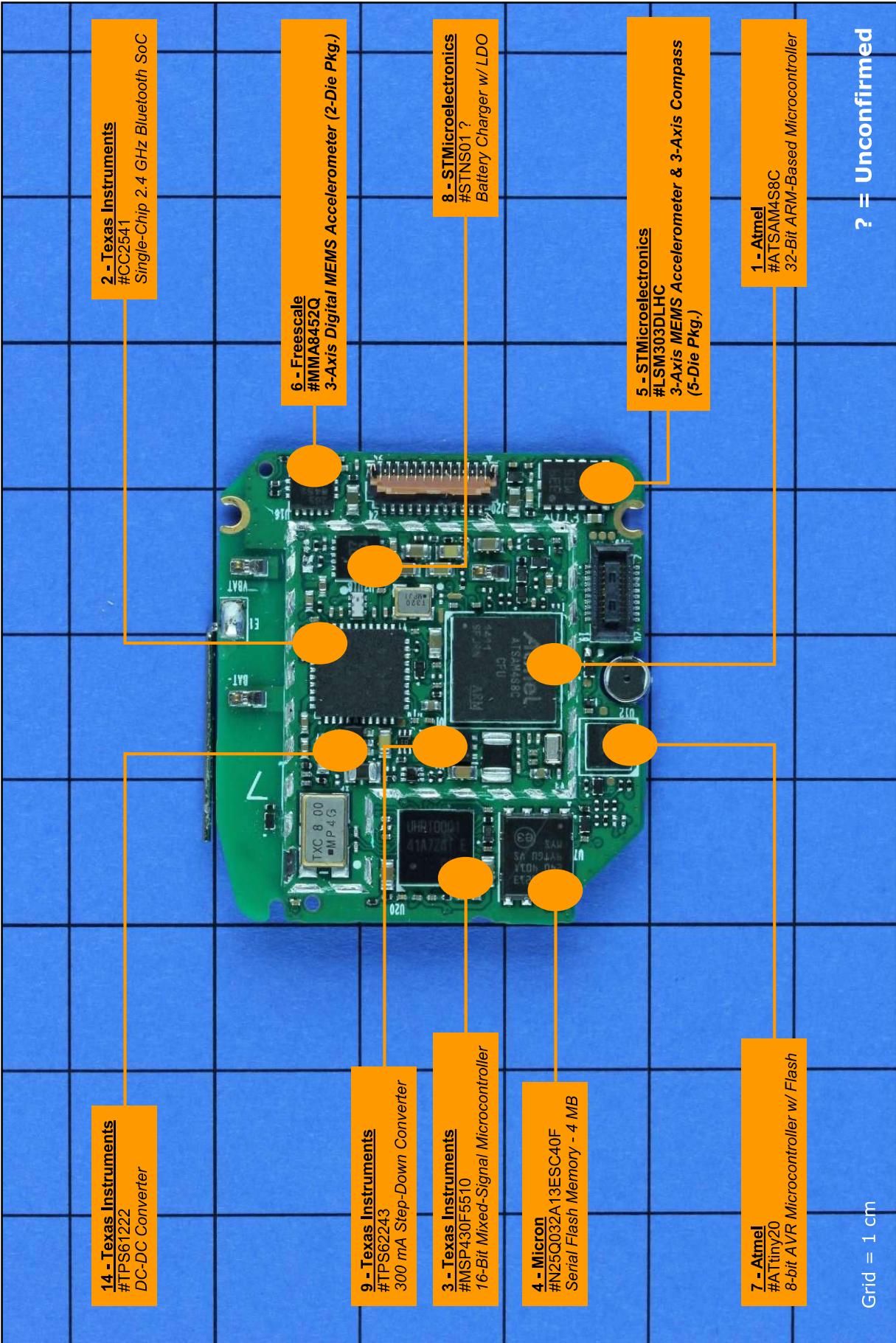




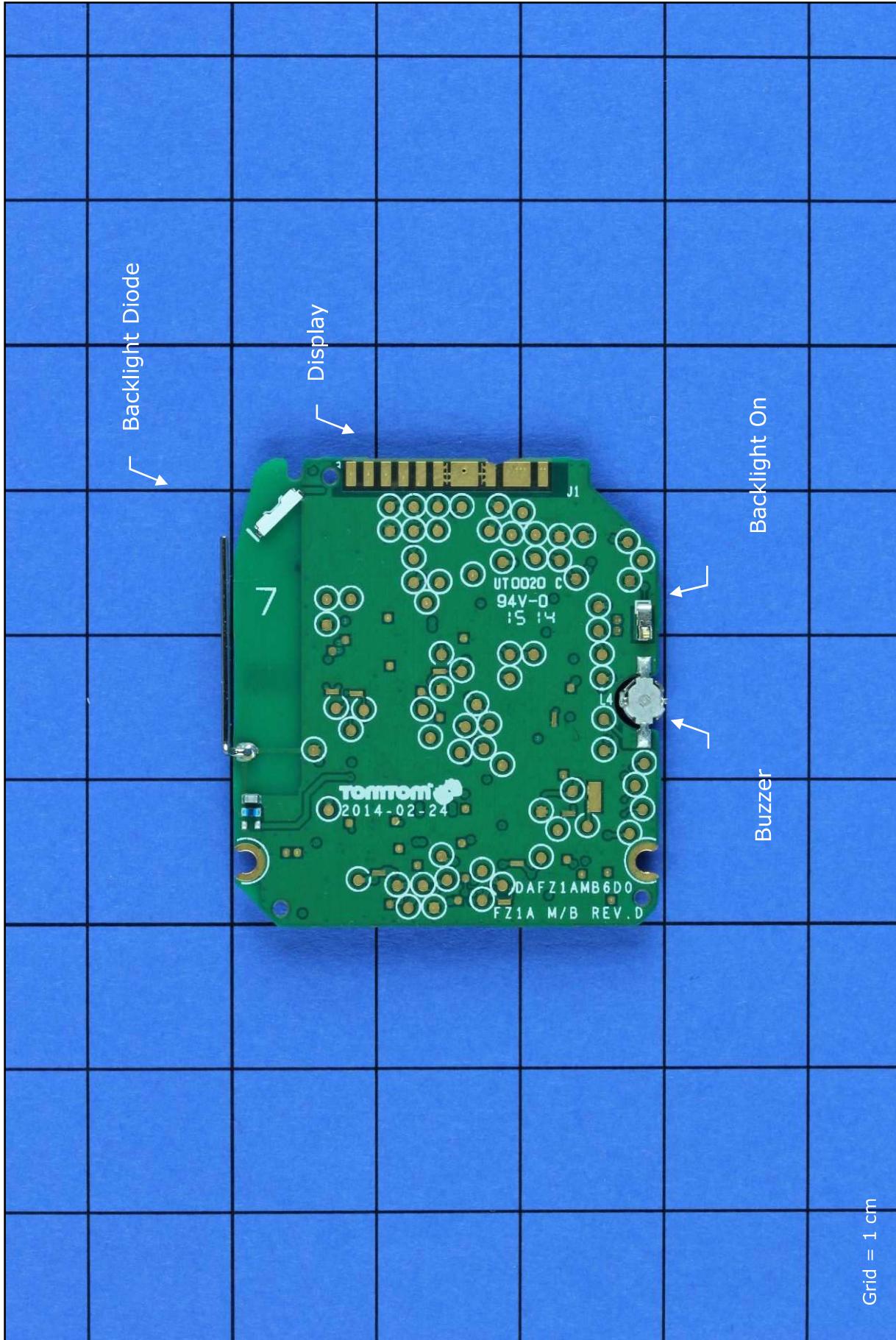
# Main Board (Side 1)



# Main Board (Side 1 IC Identification)



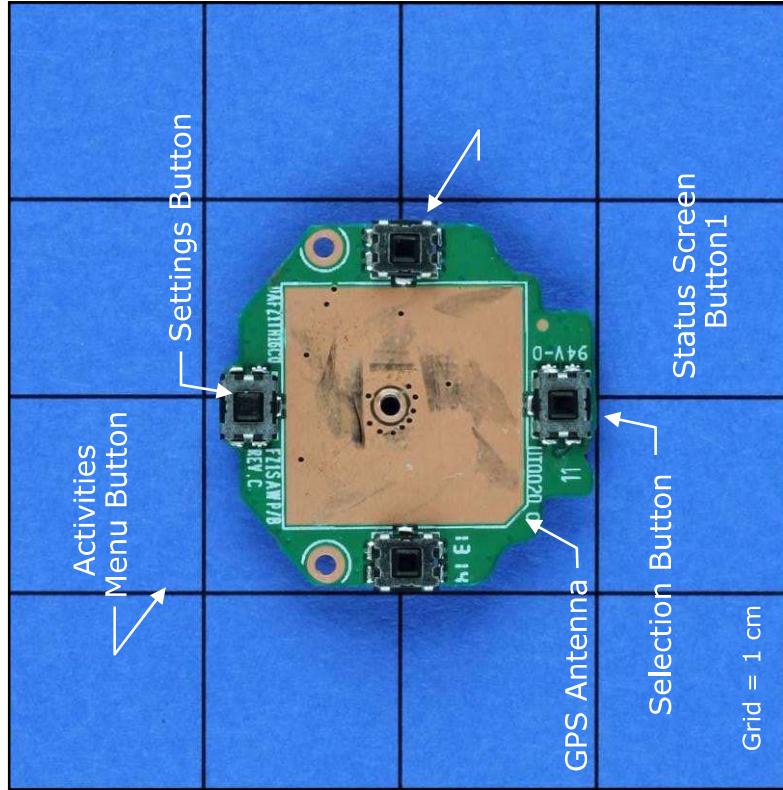
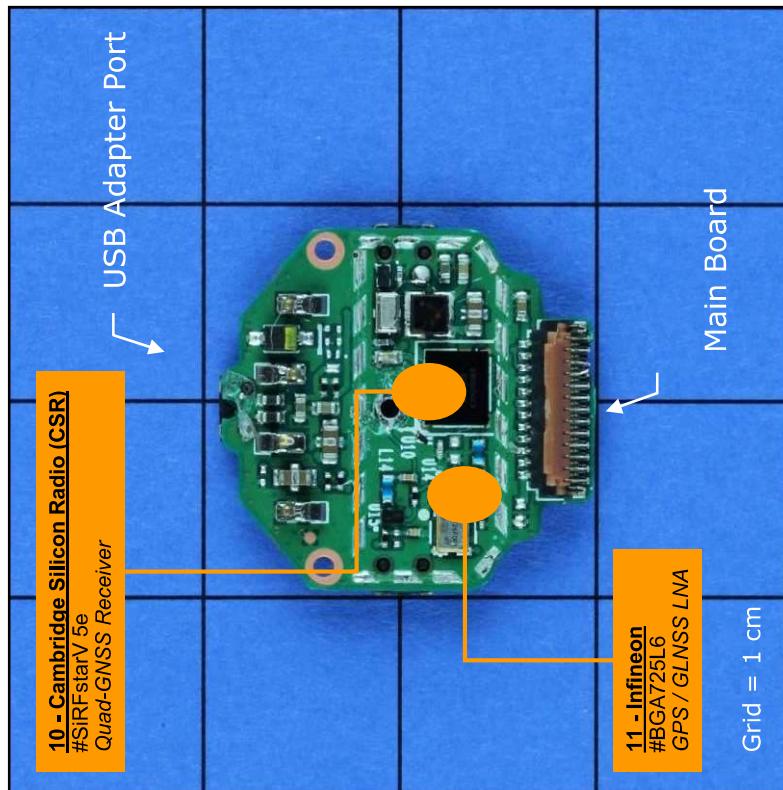
## Main Board (Side 2)



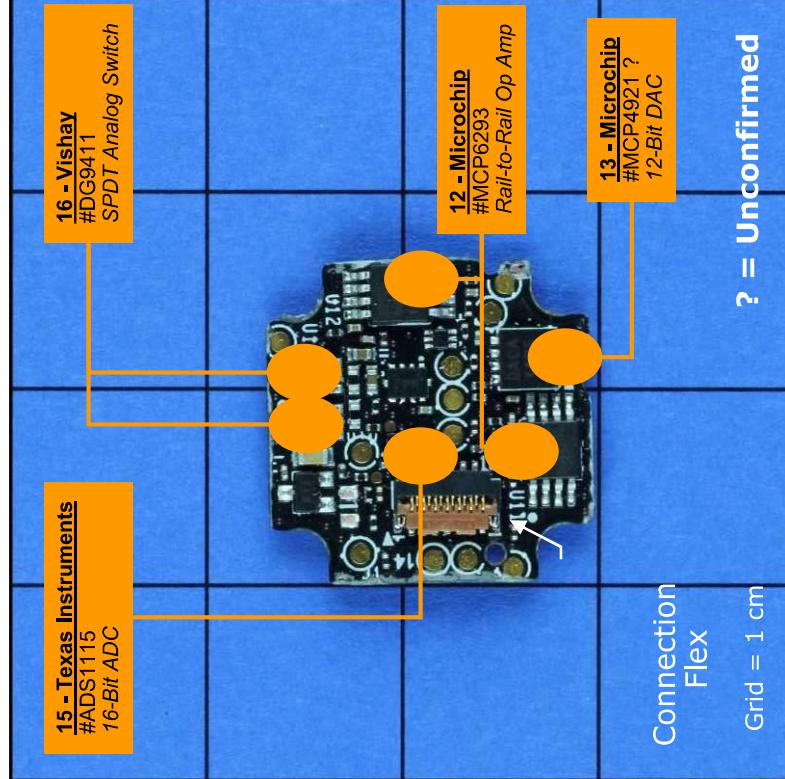
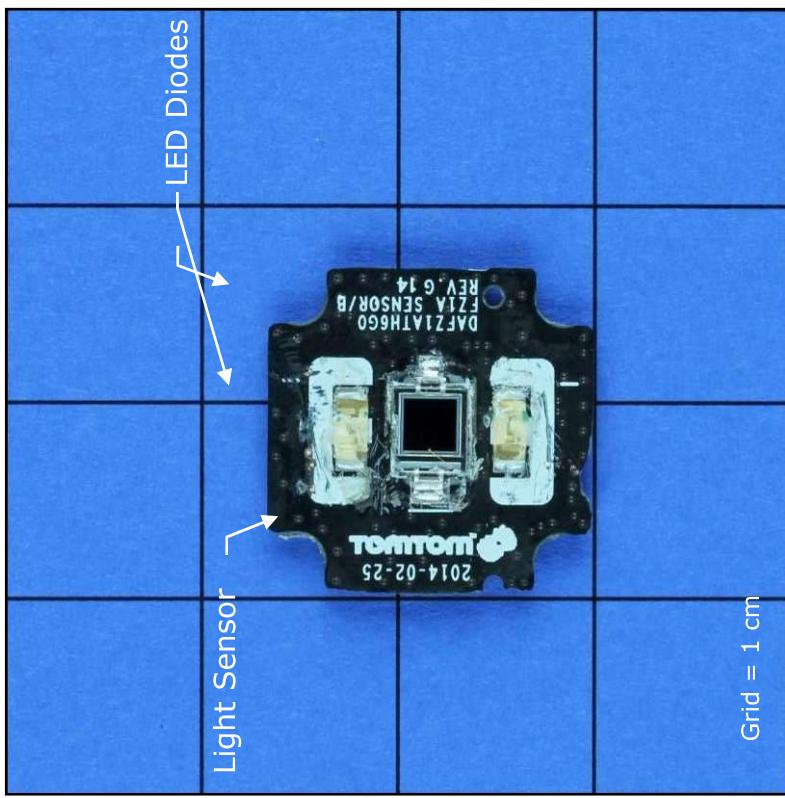
Grid = 1 cm  
Copyright © 2014, TechInsights

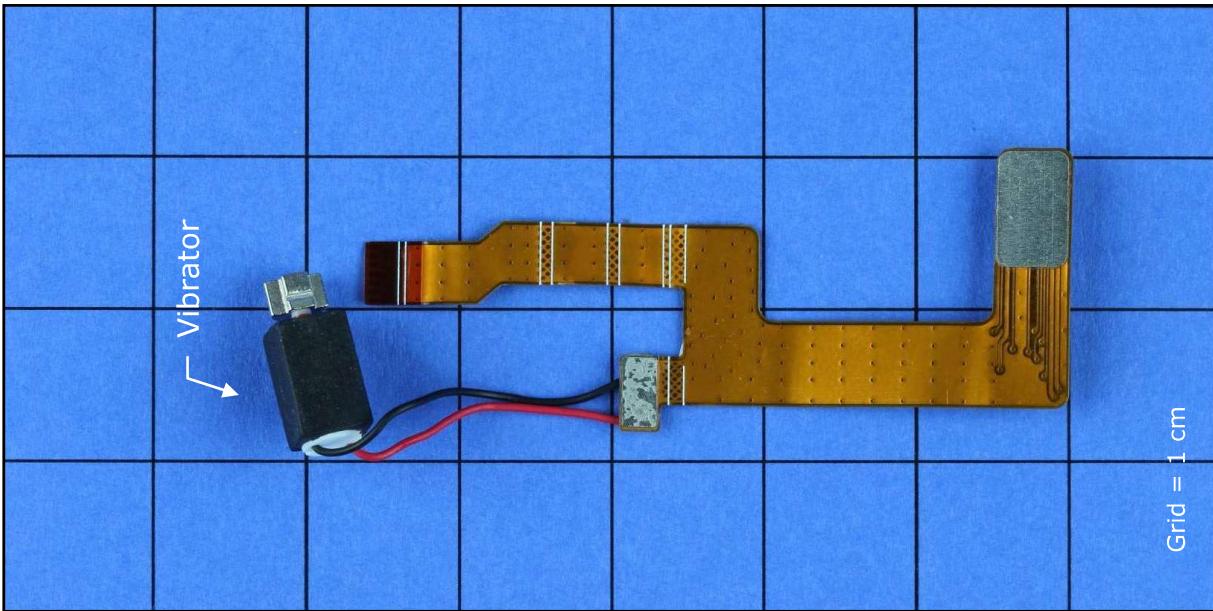
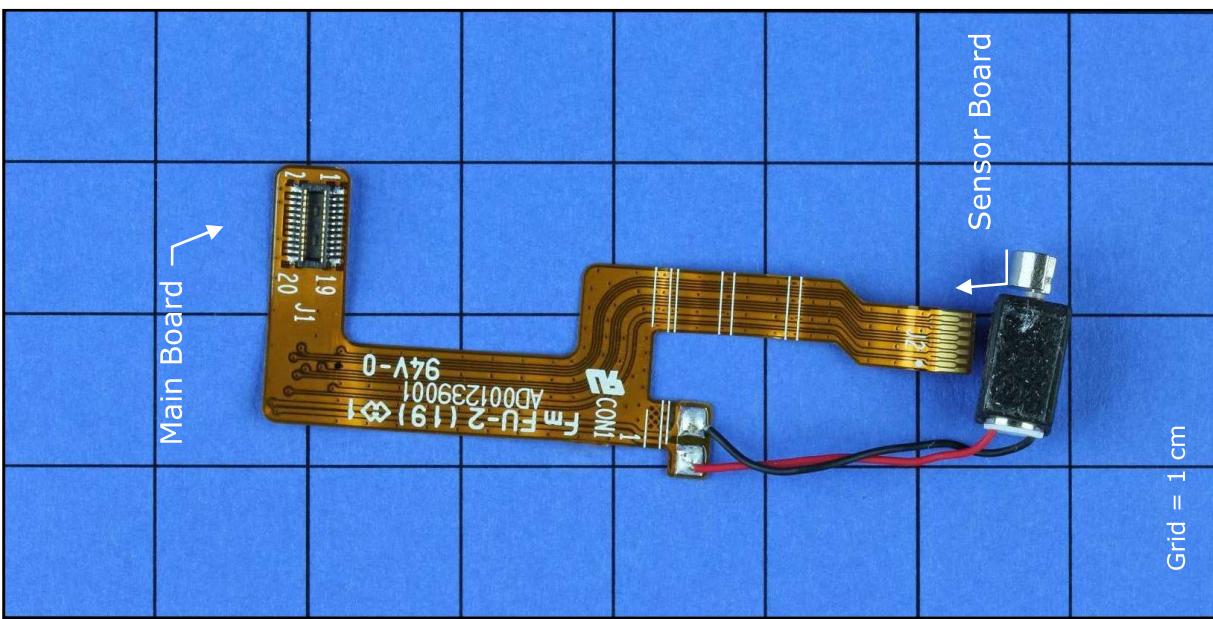
[www.teardown.com](http://www.teardown.com)  
[support@techinsights.com](mailto:support@techinsights.com)

TomTom Runner Cardio 8RA0 #17000-140613-PkC - Page 68

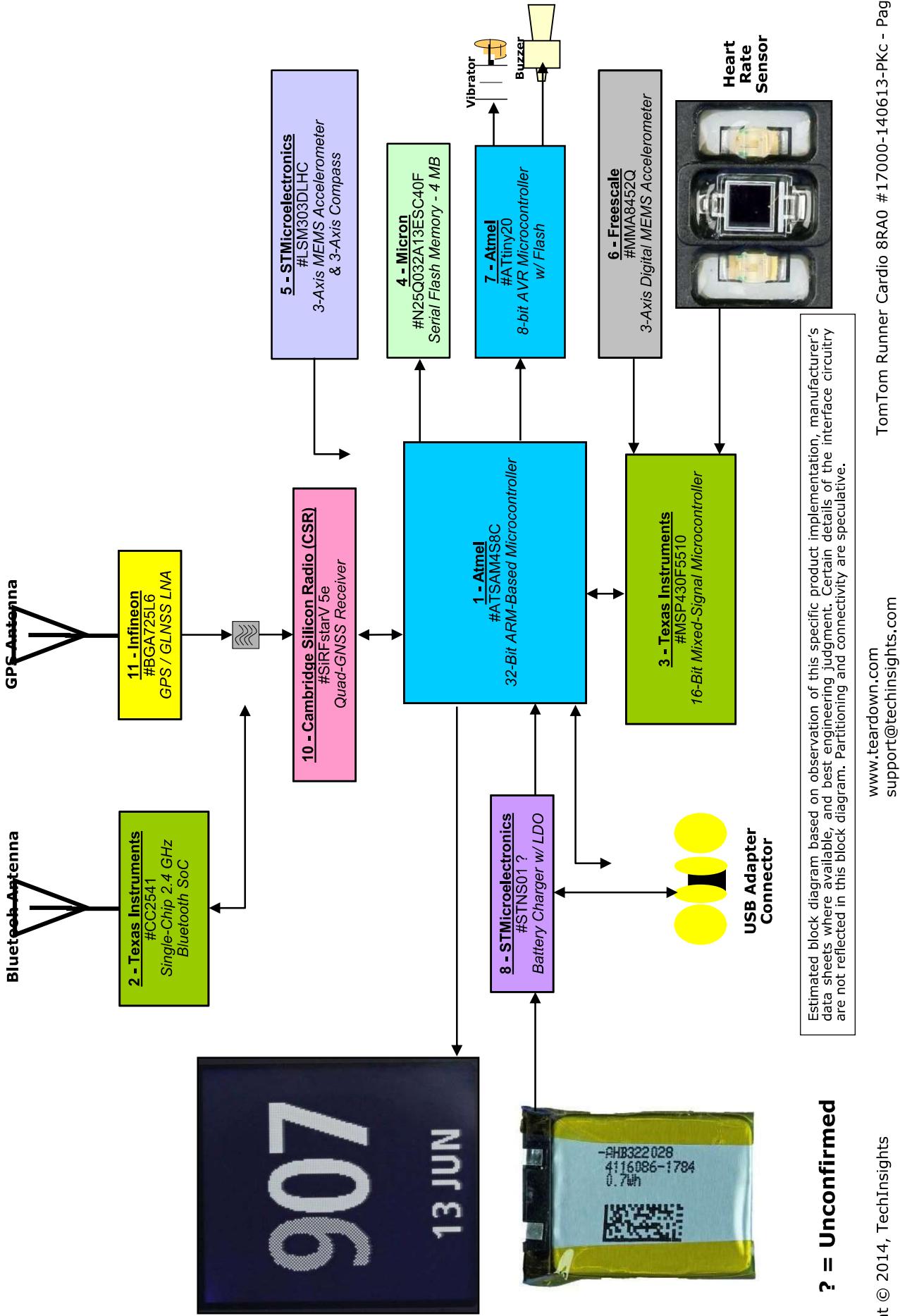


# Sensor Board





# Block Diagram



**? = Unconfirmed**

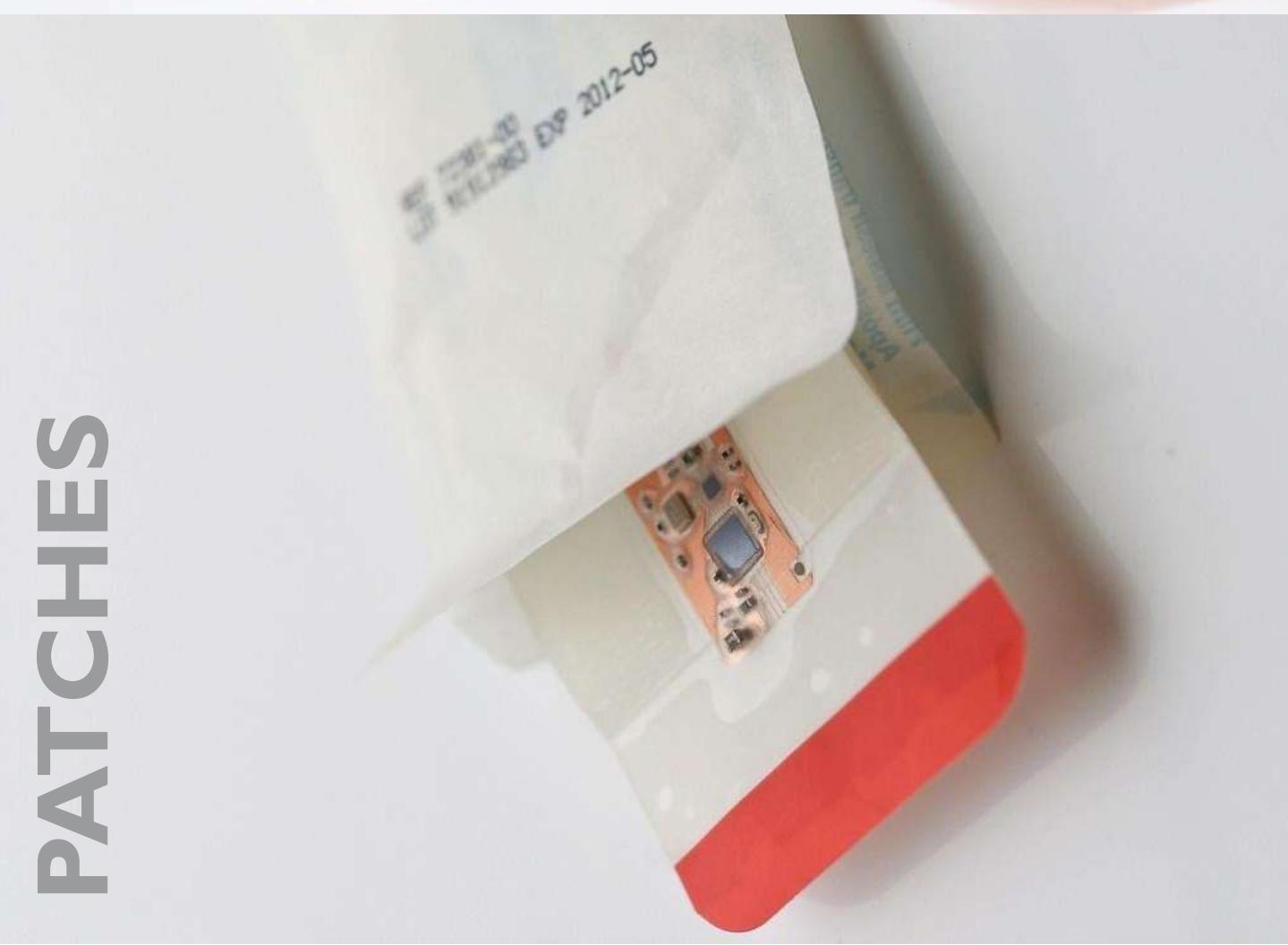


**WATCHES / WRISTBANDS**



GLASSES

# PATCHES



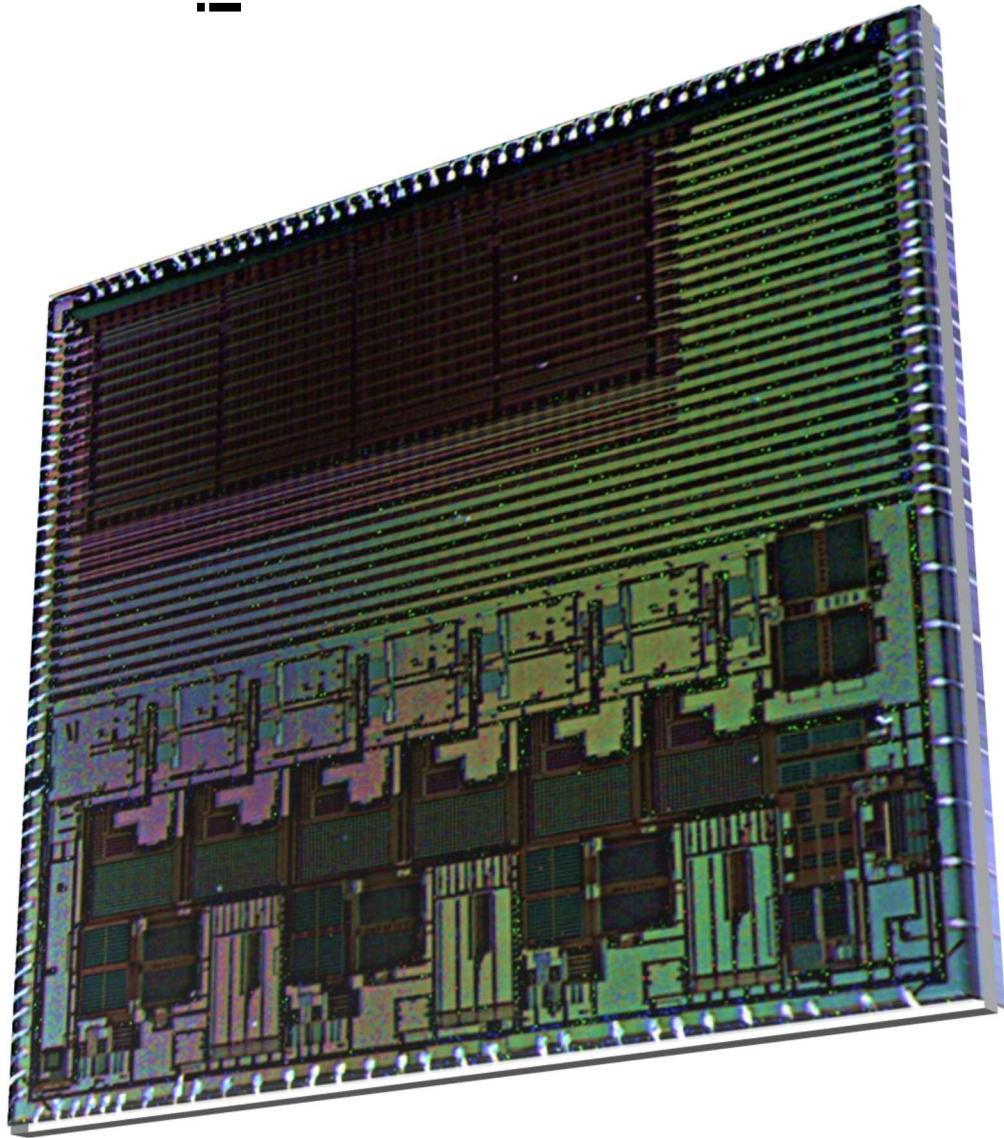


SHOES

# A System-on-Chip Example

# HOW TO DEAL WITH VERY DIVERSE APPLICATION NEEDS

imec **MUSEIC** SoC

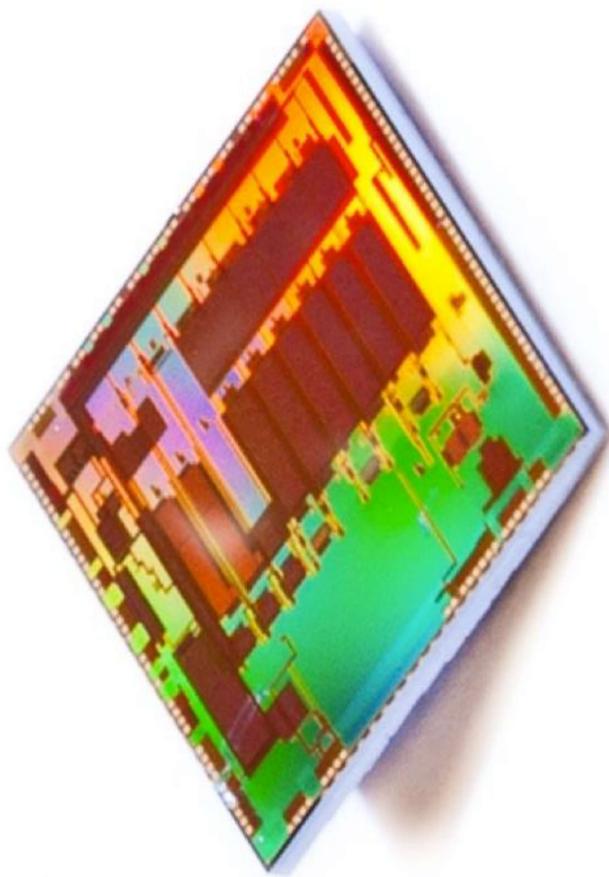


Full Multi-Sensor Mixed-Signal  
SoC with ARM core and  
Hardware Accelerators  
enabling new Healthcare and  
Lifestyle Applications

imec

# MUSEIC

Industries **smallest** and **most power efficient** sensor hub

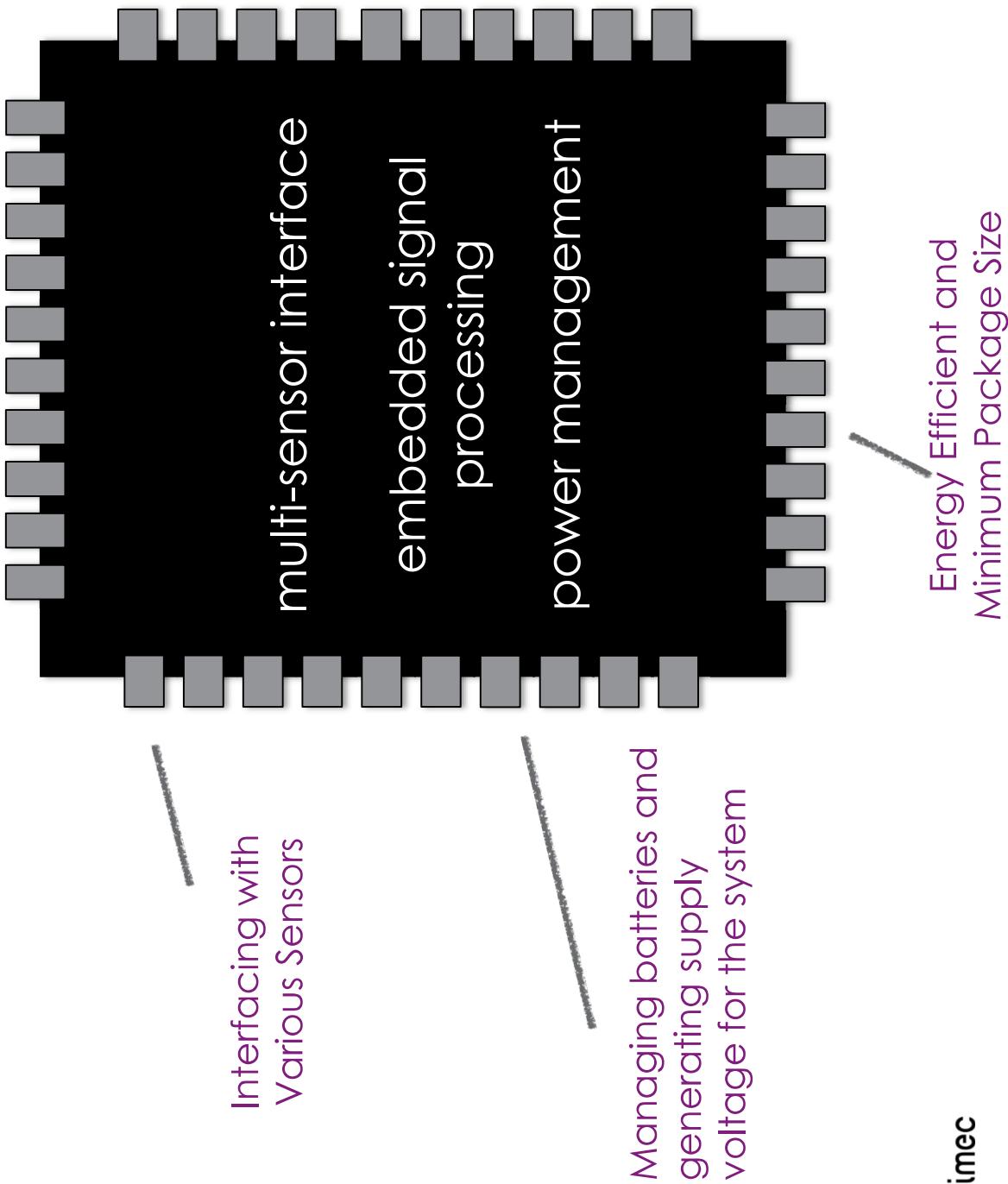


Sensors in

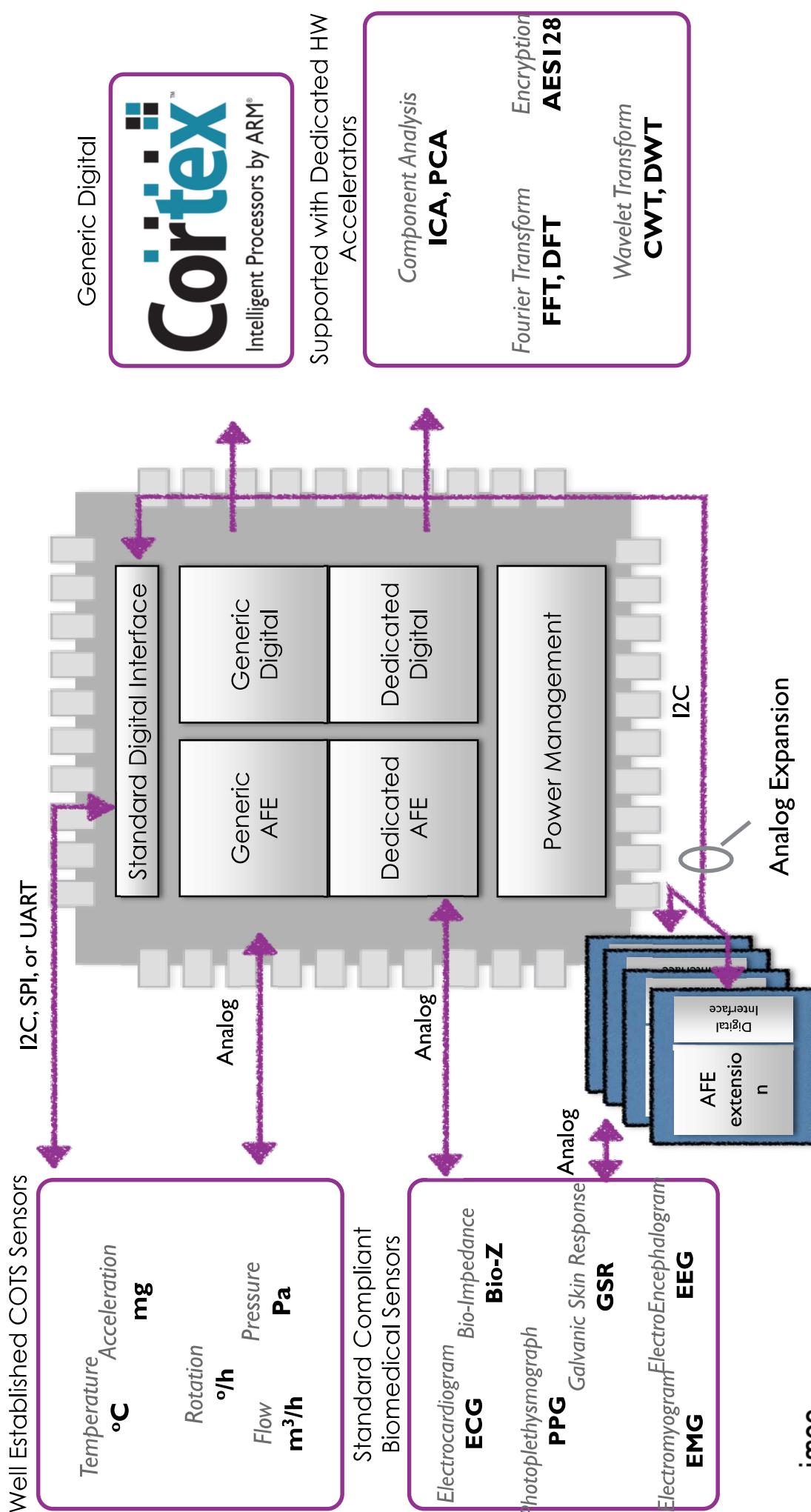
Information out

imec

# A VERSATILE PLATFORM FOR WEARABLE DEVICES



# WHAT IS INSIDE MUSEIC?



# MUSEIC

## FEATURES:

- 3 channel ECG and Electrode Tissue Impedance readouts
  - CMRR: 110dB
  - Gain: 24V/V - 880V/V
  - Noise: <700nVrms RTI (0.5Hz-150Hz)
  - Real-time motion artefact reduction based on ETI measurements
  - ADC: 18b ('14bSNR)
  - Sample speed: 128SpS/256SpS/512SpS
  - Optional 16kSpS output (pace detection)
  - Bio-impedance readout with integrated current source
    - CMRR: > 110dB
    - Resolution: 1.8-7.1mΩ/sqrt(Hz) with pseudo-sine current
    - Current source: 27.54/82/110uApp @20kHz
    - ADC: 12b @ 1024SpS/ch
    - General purpose analog inputs
    - Processor core
      - ARM™ Cortex M0 processor
      - JTAG debug with breakpoints and watchpoints
      - 128kB on-chip SRAM (data & code)
      - Digital interfaces
        - 5 general purpose SPI with DMA support
        - 2 I<sup>2</sup>C-bus Interfaces with DMA support
        - 2 UART Interfaces with DMA support
        - Up to 32 GPIO
        - Digital peripherals
          - DMA controller
          - Accelerator for matrix multiplications/additions
        - Four 32b general purpose timers
        - 32b RTC using 32kHz oscillator
        - Host SPI Interface for DMA

# SPECIFICATIONS

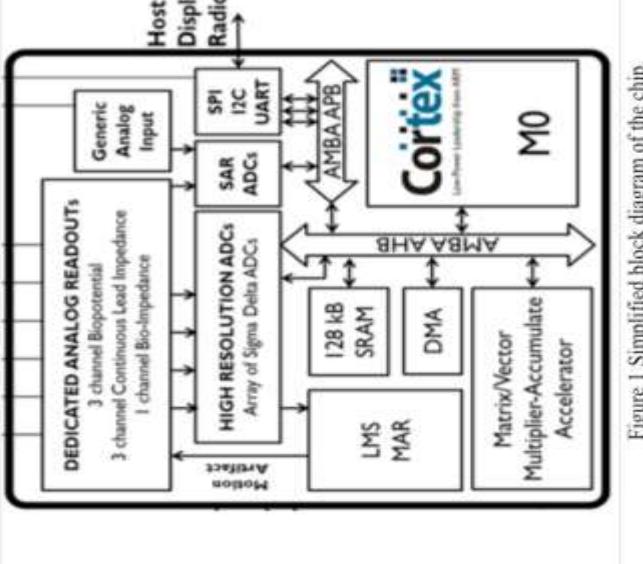
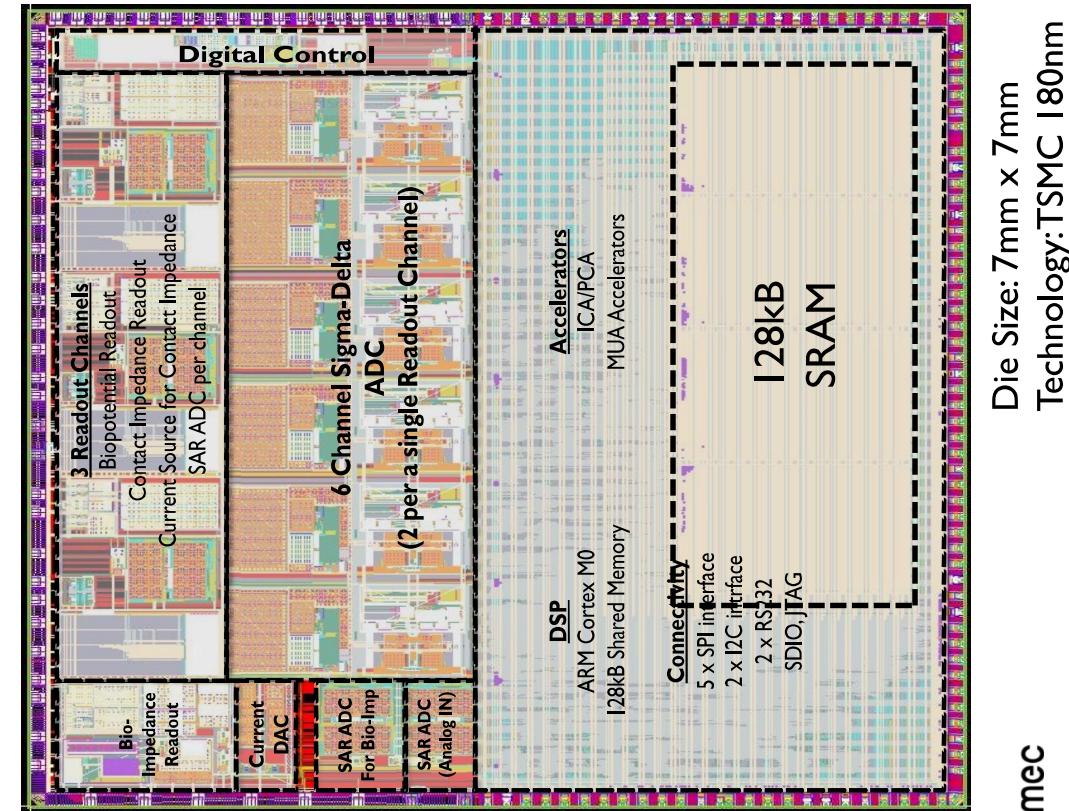


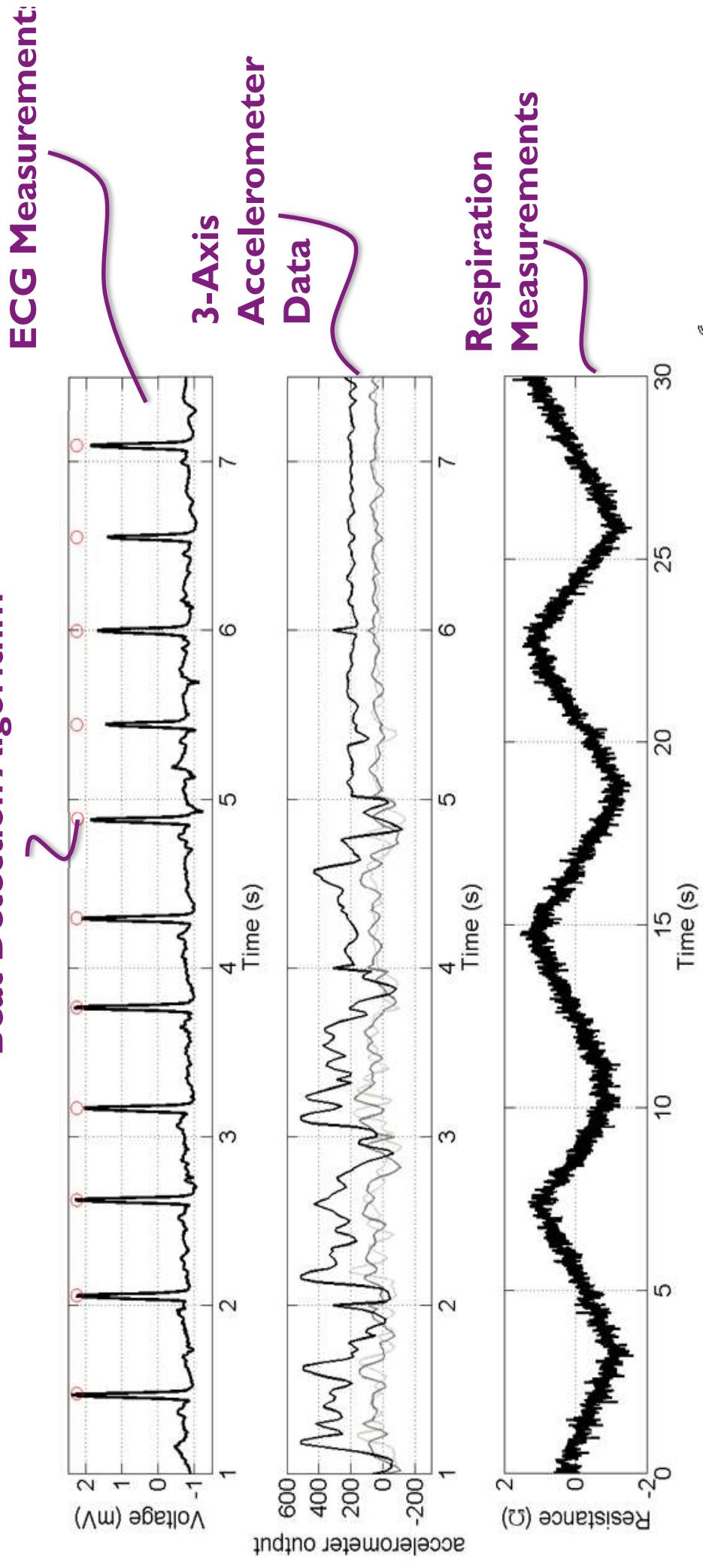
Figure 1 Simplified block diagram of the chip.

## DESCRIPTION:

MUSEIC is a single-chip solution for low-power multi-parameter signal acquisition for healthcare applications. It features 3 ECG readouts as well as a single bio-impedance readout and 2 general purpose analog readouts. Flexible digital interfaces (SPI, I<sup>2</sup>C, UART and GPIO) are provided to support additional external sensors with digital outputs. The built-in ARM™ Cortex M0 core and HW accelerator for matrix multiply/accumulate operations allows a wide range of on-chip signal conditioning/filtering to be performed. A total of 128kB on-chip SRAM (in 4 banks) is available for code and data use.

# TYPICAL APPLICATION EXAMPLE

## Beat Detection Algorithm



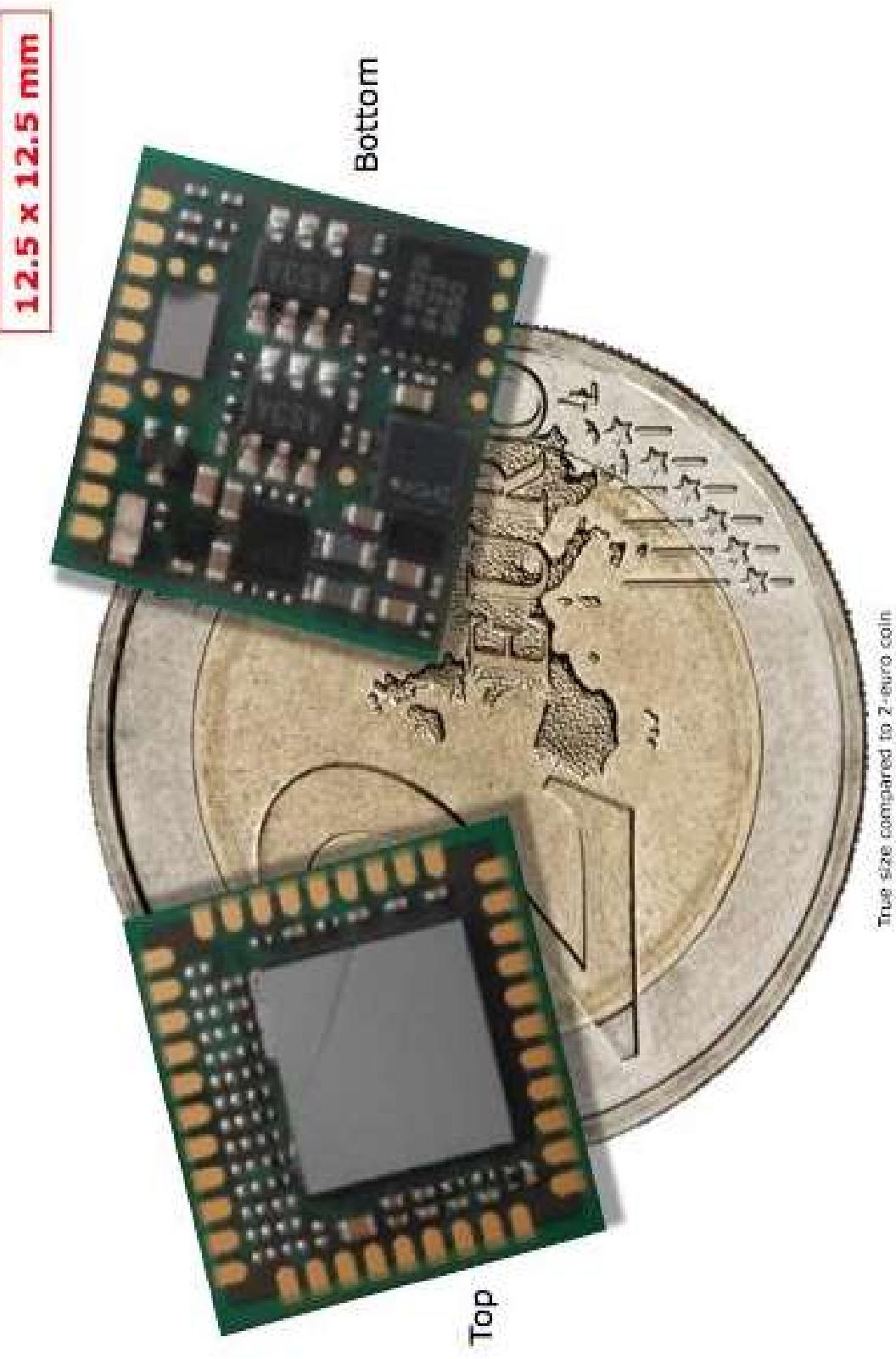
imec

# BENCHMARKING

	Atmel	freescale <sup>®</sup>	SILICON LABS	TEXAS INSTRUMENTS	ANALOG DEVICES	infineon	TOUMAZ GROUP	imec
<b>ANALOG FE</b>								
Biopotentials	○	○	●	●	●	●	●	●
Bio-Impedance	○	○	●	●	●	●	○	●
Generic Analog	●	●	●	●	●	●	●	●
Motion Artifact Removal	○	○	○	○	○	○	○	○
<b>DIGITAL BE</b>								
Microcontroller	●	●	●	●	●	●	●	●
H/W Accelerators	●	●	●	●	●	●	●	●
Memory	●	●	●	●	●	●	●	●
<b>LOW-POWER</b>								

imec

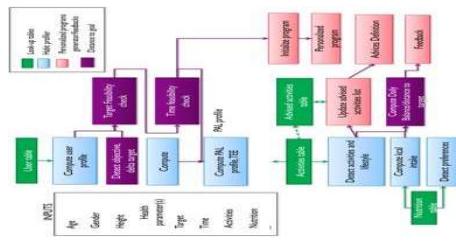
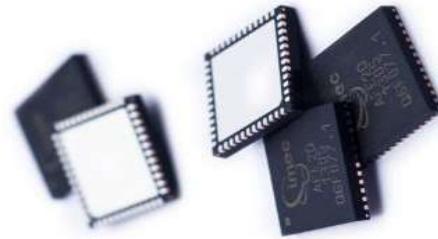
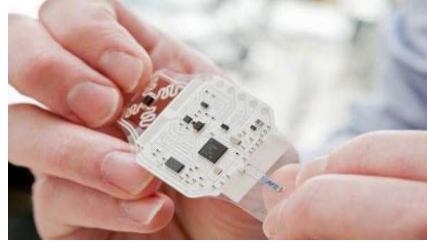
# MUSEIC SOC WITH ADVANCED PACKAGING



MUSEIC EVALUATION KIT ENABLING OUR  
PARTNERS TO EXPLORE NEW APPLICATIONS



# INTEGRATED APPROACH: FROM TECHNOLOGY BUILDING BLOCKS TO FULL APPLICATION VALIDATION



## Some Companies in this market



## Jobs' Profiles (some examples)

<https://www.apple.com/jobs/us/index.html>

<http://jobs.st.com/>

<http://www.qualcomm.com/careers>

<http://www.imgurtec.com/corporate/careers.asp>

<https://jobs.intel.com/page/show/careers>

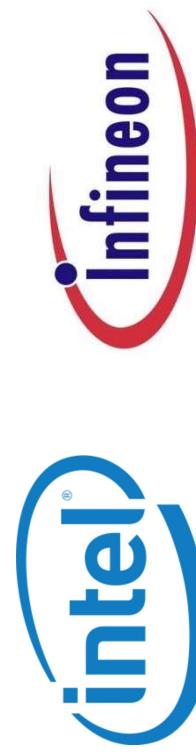
<http://www.infineon.com/cms/en/corporate/career/infineon-jobsearch/>

<http://www.dialog-semiconductor.com/careers/>

<http://arm.com/careers/>



life.augmented



<https://www.apple.com/jobs/us/index.html>

The collage consists of six distinct illustrations:

- Top Left:** A stylized, colorful, abstract sculpture of an apple.
- Top Right:** A vibrant, multi-colored apple (yellow, orange, red) with a small yellow leaf.
- Middle Left:** An abstract, colorful blob or cluster of shapes resembling an apple.
- Middle Right:** A minimalist, glowing blue and red outline of an apple.
- Bottom Left:** A green, textured illustration of an apple with a small tree growing out of its top, featuring a figure in a yellow dress.
- Bottom Right:** A cartoonish, red, blob-like character with large white eyes, a wide mouth, and small ears.

On the left side of the collage, there is a vertical sidebar with the following text and links:

- Jobs at Apple**
- Apple**
- [Mac](#)
- [iPad](#)
- [iPhone](#)
- [Watch](#)
- [TV](#)
- [Music](#)
- [About Apple](#)
- [Teams](#)
- [Apple Retail](#)
- [Students](#)
- [Profile](#)
- [Support](#)
- [Search](#)

At the top right of the sidebar, there is a search bar with a magnifying glass icon and a clear icon.

**Join us. Be you.**

Watch the film

# Digital Design Engineer

Livorno, Italy  
Hardware

## Summary

At Apple, we work every single day to craft products that enrich people's lives. Do you love working on challenges that no one has solved yet? Do you like changing the game? We have an opportunity for a visionary and uncommonly talented RTL Design Engineer. As a member of our dynamic group, you will have the rare and rewarding opportunity to craft upcoming products that will delight and inspire millions of Apple's customers every single day.

You will join the DDR PHY design team. We provide best-in-class PHY designs for high-performance, low power applications. As a logic design engineer, you will be involved in all phases of the design, from concept study, architecture definition, design and verification, to silicon bring-up and characterization.

Posted: Feb 26, 2020

Role Number: 200154676

## Key Qualifications

- The ideal candidate will have **several years experience in digital design including RTL design experience**
- Knowledge of best practices with respect to implementation of digital logic
- Understanding of digital design flow including RTL simulation, logic synthesis, timing constraints, timing closure, STA, back annotation of parasitics, gate level simulation, equivalence checking
- Understanding of Design Verification and the ability to write self-checking test suites
- Ability to write assembly level code and higher level code
- Ability to analyze a design and partition between HW implementation and SW control
- Experience in hands-on lab evaluation
- Understanding of ASIC test methodology such as scan insertion, memory BIST and test pattern generation
- Good written and verbal communication skills
- Experience in working with international teams

**Description**

- Work with systems team to understand the top level requirements of the digital functions and develop detailed specifications
- Implement the function in Verilog RTL to specification
- Partition the function between HW and FW for most efficient implementation
- Develop RTL and FW to implement the function
- Perform unit level testing on the RTL function

Other responsibilities could include:-

- RTL synthesis
- Equivalence checking or Static Timing Analysis
- Support the DV team by writing self-checking tests as required
- Develop FW to support DV and ATE environments

**Education & Experience**

Masters Degree in Electrical Engineering or equivalent experiences

**Additional Requirements**

Apple is an Equal Opportunity Employer that is committed to inclusion and diversity. We also take affirmative action to offer employment and advancement opportunities to all applicants, including minorities, women, protected veterans, and individuals with disabilities. Apple will not discriminate or retaliate against applicants who inquire about, disclose, or discuss their compensation or that of other applicants.

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## Job Detail

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Security Red-Team Engineers (up to Senior Staff/Principal Engineer level) - QCT, Cork, Ireland

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Job Title

Digital ASIC Design Engineers (up to Senior Staff/Principal Engineer level) - QCT, Cork, Ireland

Post Date

02/25/2020

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**Job Detail**

E1973218

**Digital ASIC Design Engineers (up to Senior Staff/Principal Engineer level) - QCT,****Cork, Ireland****02/25/2020****Qualcomm Technologies, Inc.****Engineering - Hardware****Ireland - Cork****Job Overview**

Qualcomm is a company of inventors that unlocked 5G ushering in an age of rapid acceleration in connectivity and new possibilities that will transform industries, create jobs, and enrich lives. But this is just the beginning. It takes inventive minds with diverse skills, backgrounds, and cultures to transform 5Gs potential into world-changing technologies and products. This is the Invention Age - and this is where you come in.

**About the role**

We are seeking Digital Design Engineers for our SnapDragon team in Cork, Ireland. The Cork site is home to a range of digital IP teams working on cutting edge IP for the latest Snapdragon chip sets. The team work on IPs related to security, encryption, power control, contextual awareness, debug, profiling and processing. Each team is working with the latest tools and digital design and verification techniques in bleeding edge silicon nodes, 10nm and below. High quality and low cost are all key design points for our products.

Team members work directly with architecture, software and SoC teams in Ireland and other global Qualcomm locations. Low power micro-architecture and efficient verification are valued design techniques.

Successful candidates will be responsible for leading and participating in the design of leading-edge ASIC's and SoC's, in advanced digital CMOS processes for multi-function mobile platforms.



## **Where you will be working**

Cork has a proud reputation as Ireland's second largest economic engine and is now one of the Top 20 location choices in Europe with 39,000 people being employed by over 170 overseas companies. There's a growing diversity in the region with people from many nationalities relocating to Cork, relishing the opportunity to work and live in a location that offers an excellent quality of life. A gateway to Europe, Cork airport provides access to almost 50 international destinations including transatlantic air routes.

## **About Us**

Qualcomm Cork, a greenfield site based in the beautiful harbour city of Cork opened its doors in August 2013 and has been growing ever since across our QCT Engineering, OneIT and HR teams.

The Cork QCT engineering team is now over 220+ engineers strong and is continuing to expand. Our engineers work on all aspects of leading-edge technology (7nm, 5nm), including; Analog Mixed Signal, Security, Power Management, Sensors, Machine Learning, Modelling, Validation, Design Automation, Automotive and Physical Design. We are the R&D engine that benefits the world in three ways: Enabling Customers, Transforming Industries and Enriching Lives.

## **Equal Opportunities**

We are an Equal Opportunity employer; all qualified applicants will receive consideration for employment without regard to race, colour, religion, sexual orientation, gender identity, national origin, disability, veteran status, or any protected classification.

## **Giving Back**

Employees in Cork have a strong sense of community. We are encouraged through the philanthropic endeavours of the Qualcomm Foundation to support causes that matter to us.



Apart from working in an open, relaxed and collaborative space, you will enjoy:

- Salary, stock and performance related bonus
- Employee stock purchase scheme
- Matching pension scheme
- Education Assistance
- Relocation and immigration support
- Life, Medical, Income and Travel Insurance
- Subsidised gym membership
- Bicycle purchase scheme
- As much Nespresso as you can handle!!!
- Free fruit every Monday and Wednesday
- Employee run clubs, including, running, football, chess, badminton + many more
- Bachelor's degree in Science, Engineering, or related field.
- 2+ years ASIC design, verification, or related work experience.

#### Minimum Qualifications

\*References to a particular number of years experience are for indicative purposes only.  
Applications from candidates with equivalent experience will be considered, provided that the candidate can demonstrate an ability to fulfil the principal duties of the role and possesses the required competencies.

This position requires detailed knowledge of:

- **ASIC design experience including architecture, RTL design in Verilog/VHDL, low power design techniques, UPF.**
- Experience with synthesis, and timing closure.
- Experience with DC, LINT, PTSI, and CDC.
- Experience working in a multi-disciplinary, global team focused on advanced, high volume applications



Required: Bachelor's, Electrical Engineering  
Preferred: Master's, Electrical Engineering

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**Job ID:** JRO129918  
**Job Category:** Engineering Support  
**Primary Location:** Munich, DE

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## Neuromorphic Applications Researcher (f/m/d)

### Job Description

Intel Labs is seeking research scientists to join our Neuromorphic Computing Lab to advance the state-of-the-art in neuromorphic applications. As a member of a neuromorphic applications-focused team in Munich, you will pioneer the development of new methods that exploit the power, performance, and functional advantages of Intel's neuromorphic research platforms for solving real-world problems. You will work with Intel's neuromorphic software, hardware, and algorithms researchers, as well as with a large ecosystem of external collaborators. Applications will span IoT/edge devices (e.g. robotics, wearables, sensors) to PCs and mobile devices (e.g. personalized UIs, speech, gesture, and natural language processing) to datacenter systems (e.g. real-time analytics, optimization, and security monitoring). The work is expected to lead to discoveries of new programming models and algorithms at the forefront of AI and neuromorphic computing. Results will be demonstrated at industry/academic forums and published in peer-reviewed conferences and journals. Your work will also influence the definition of Intel's next generation neuromorphic chips.

This is a unique opportunity to join a talented and innovative team pioneering a promising frontier of non von Neumann computing. You will be at the front line in Intel Labs advancing this technology to commercialization. Please note that this is a temporary position for 2 years.



## Qualifications

- PhD in computer science, computational neuroscience, systems engineering, electrical/computer engineering, or a related field.
- At least 2 years of research in the area of developing and applying novel neuro-inspired algorithms, with a strong publication history in this area.
- Experience developing neural network applications, preferably including spiking neural networks (SNNs) using Brian, PyNN, Nengo, NxSDK, or similar
- Expertise in Python, C, and OOP languages.
- Working knowledge of mainstream machine learning algorithms, including deep learning.
- Strong grasp of computational fundamentals, computer architecture, and dynamical systems.
- Fluent in English, both written and spoken

## Inside this Business Group

Intel Labs is the company's world-class, industry leading research organization, responsible for driving Intel's technology pipeline and creating new opportunities. The mission of Intel Labs is to deliver breakthrough technologies to fuel Intel's growth. This includes identifying and exploring compelling new technologies and high risk opportunities ahead of business unit investment and demonstrating first-to-market technologies and innovative new usages for computing technology. Intel Labs engages the leading thinkers in academia and industry in addition to partnering closely with Intel business units.

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Martin from Warstein manages 12 employees – in part time to share responsibility with his wife to raise their three children..

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# HiPEAC Jobs

The screenshot shows a web browser displaying the HiPEAC Jobs website. The page has a light gray header with a dark blue navigation bar. The navigation bar includes links for 'Jobs - HiPEAC', 'The Network', 'Events', 'Jobs', 'Vision', 'Research', 'News', 'Press room', 'About', 'Open positions' (which is the active tab), 'Career center', 'Internship programme', 'Log in', 'Join', and social media icons for Twitter, LinkedIn, and RSS.

A large yellow banner in the center of the page reads: "Find your ideal computing job in Europe. There are currently **90** open positions!"

Below the banner, there are three job listing cards:

- TU/e**: One PhD position on the ChEOPS project in Twente (Netherlands): Verified Construction of Correct and Optimised Parallel Software @ TU/e. Date: Oct 1, 2019. Status: New.
- ECMWF**: Production Analyst – environmental applications forecasts @ ECMWF.
- EPFL**: System Engineer (storage focus) W/M @ EPFL.

At the bottom left, there is a search bar with the placeholder text "Search open positions by title, company, country, topic or keywords..." and a "Show filters" button.