

Electronics and Communication Systems

Electronics Systems

Master Degree in **Computer Engineering**

<https://computer.ing.unipi.it/ce-lm>

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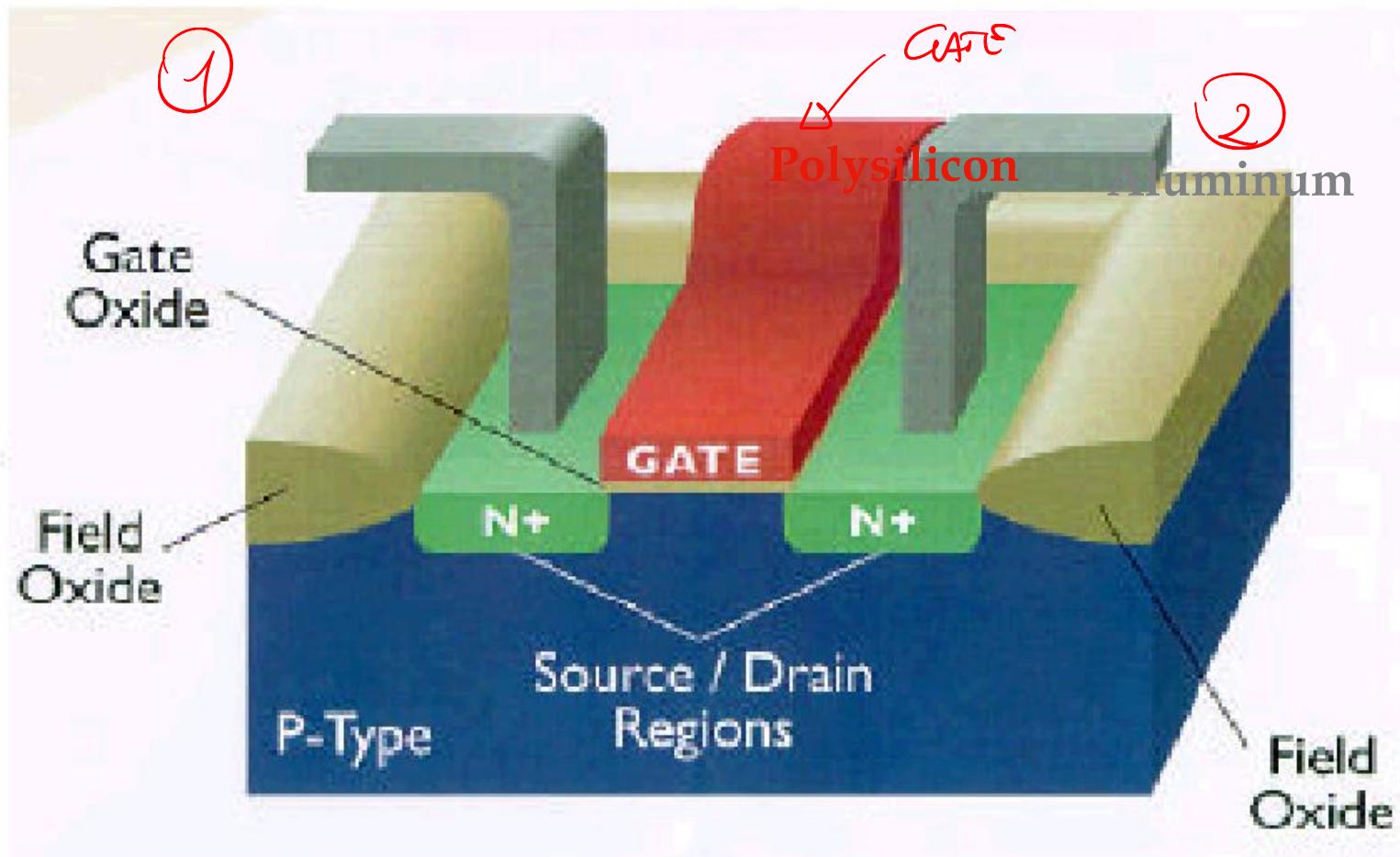
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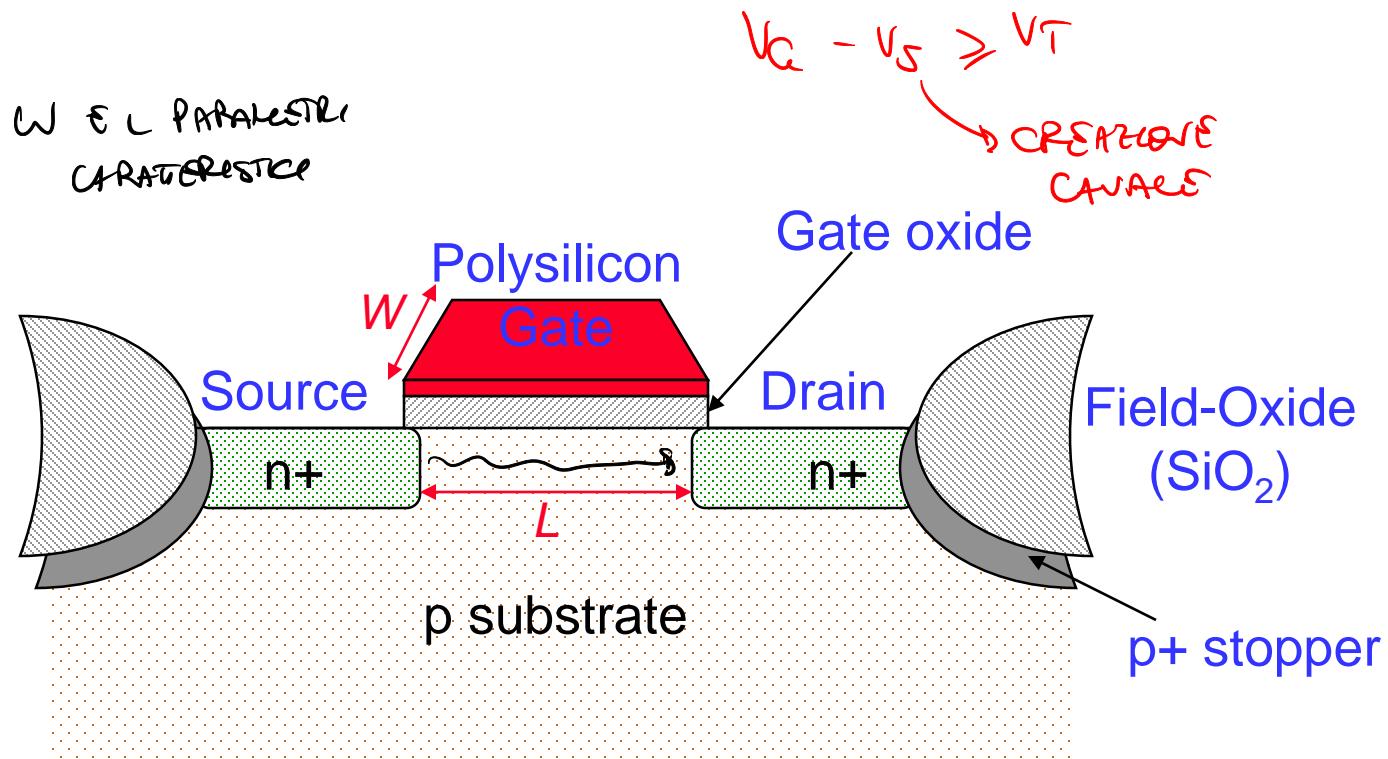
Outline

- MOS Transistor Switch Model
- Pass Gate
- Inverter
- Review of IC Manufacturing

The MOS Transistor



The NMOS Transistor Cross Section



$$f_m = \mu_n \cdot C_{ox} \cdot \frac{W}{L}$$

FISSATI

POSSO VIVERE

CARATTERISTICA

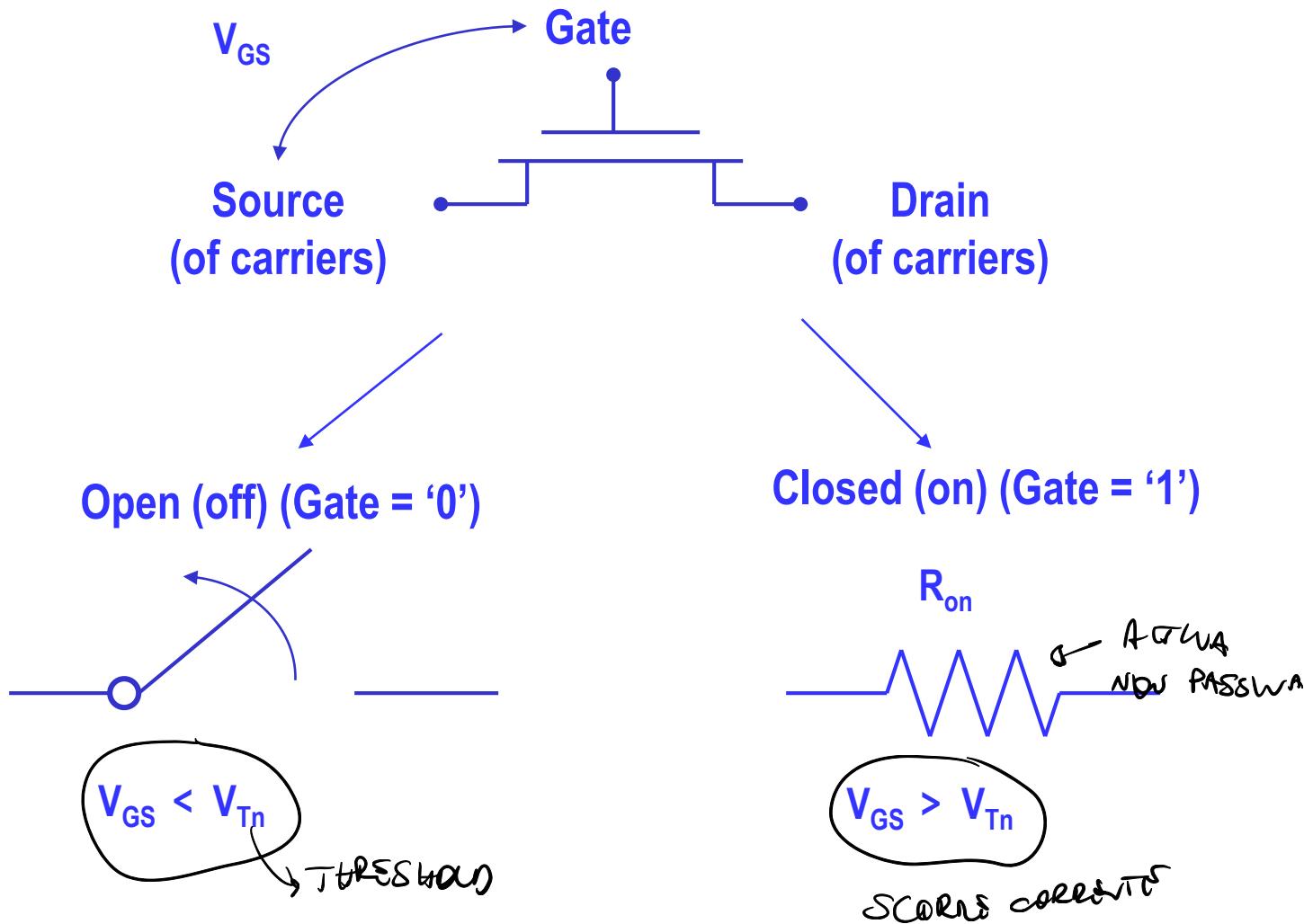
PER UN'AREA DI UNITÀ

VELOCITÀ AREA

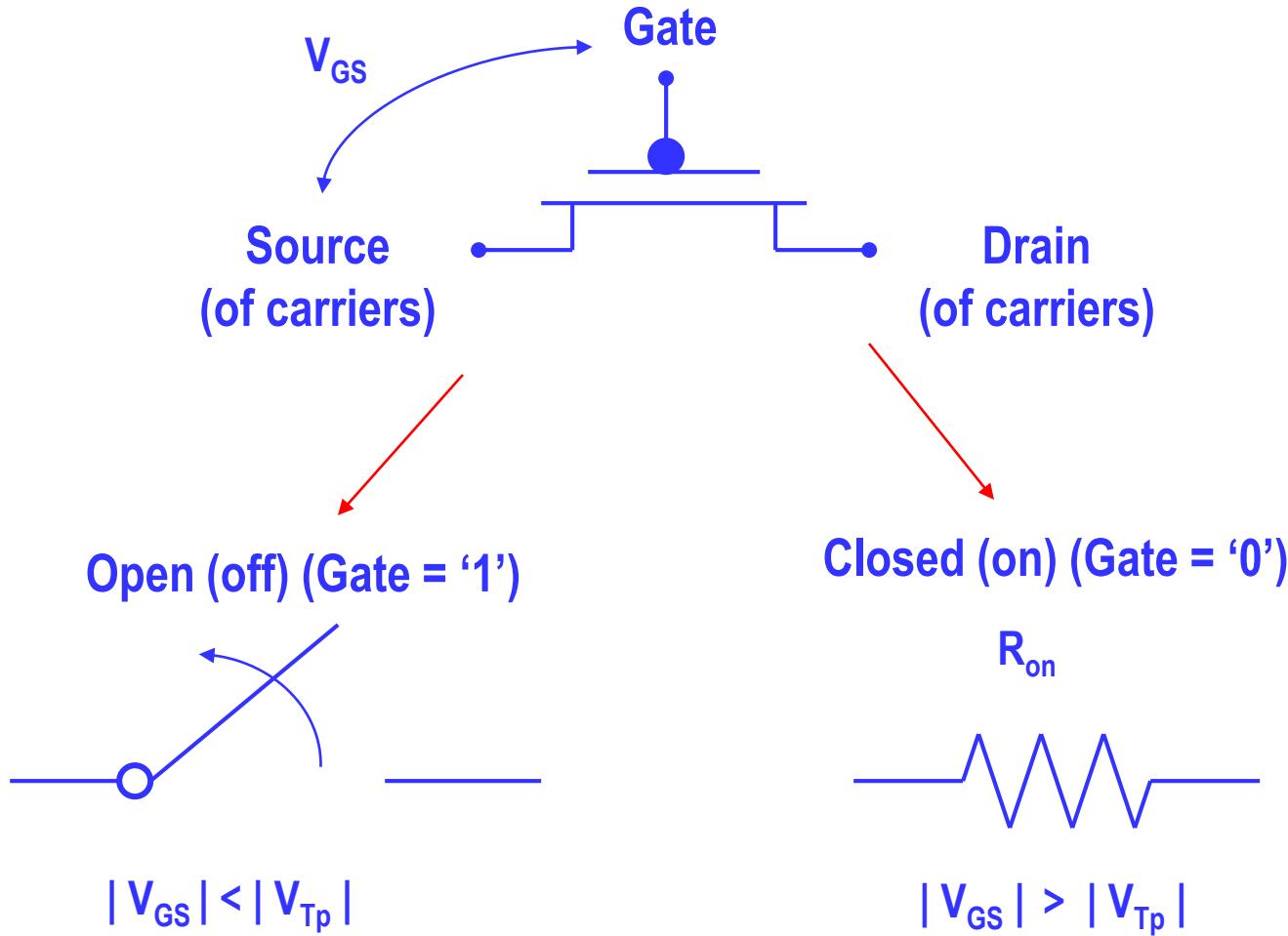
SCESSIONI NECESSARIE

$$\mu_n \approx 2-4 \text{ m/s}$$

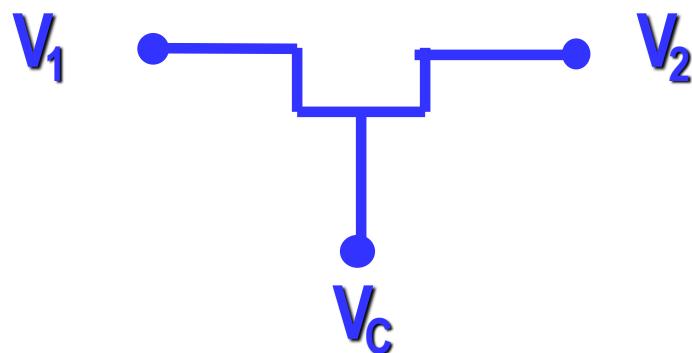
Switch Model of NMOS Transistor



Switch Model of PMOS Transistor



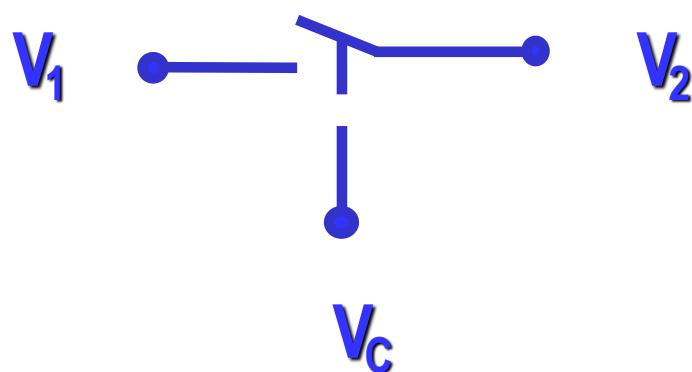
CONTROLLED SWITCH



$V_C = V_H$ **CONDUCT**

$V_C = V_L$ **BLOCK**

CONTROLLED SWITCH

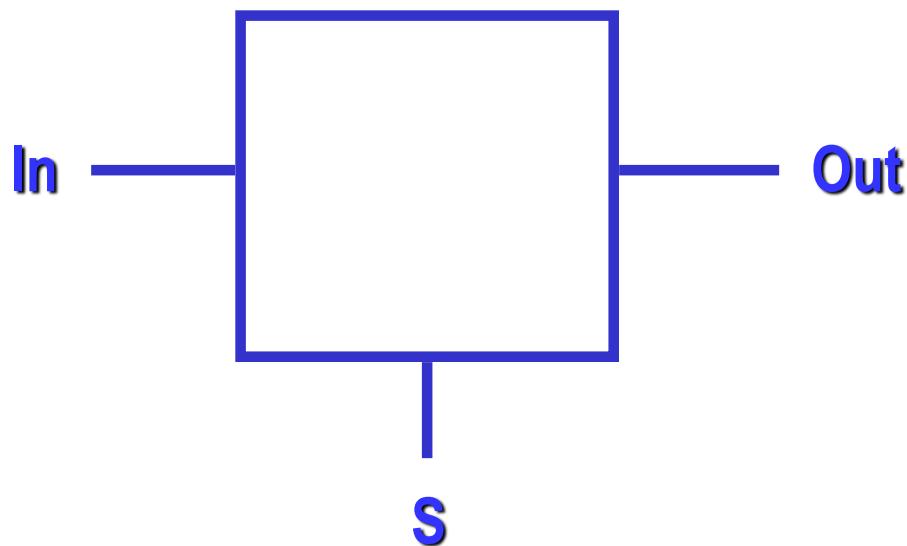


$V_C = V_H$ CLOSE

$V_C = V_L$ OPEN

PASS GATE

- ❖ Three-state logic gates: high (H), low (L) and high-impedance (Z)



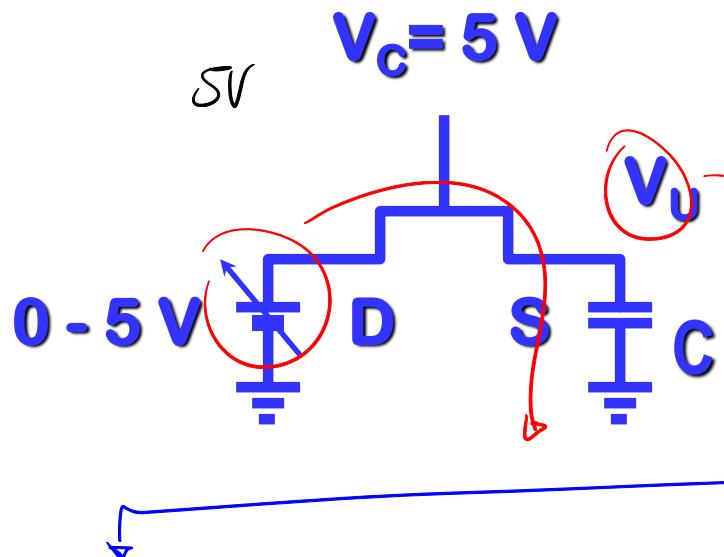
S	In	Out
0	0	Z
0	1	Z
1	0	0
1	1	1

PASS TRANSISTOR

Equivalent Resistance

$$V_{GS} > V_T = 1 \text{ V}$$

$$, U_{t+} = 5 \text{ V}$$



$$I_D = \beta_n \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right] \approx \beta_n (V_{GS} - V_T)V_{DS}$$

$$\frac{1}{R} = \frac{dI_D}{dV_{DS}} = \beta_n (V_{GS} - V_T)$$

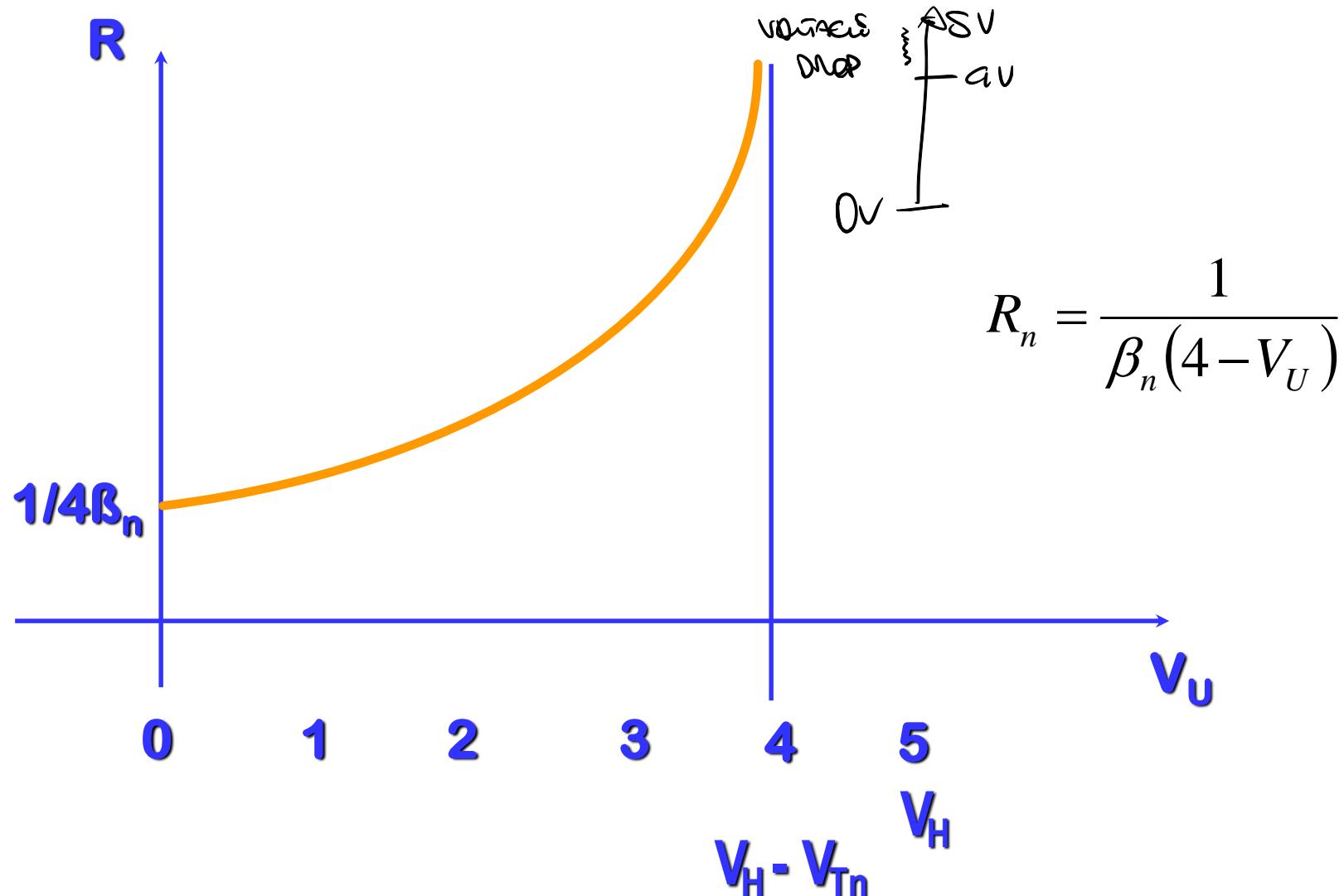
$$R = \frac{1}{\beta_n (V_{GS} - V_T)} = \frac{1}{\beta_n (4 - V_U)}$$

$$V_T = 1 \text{ V}$$

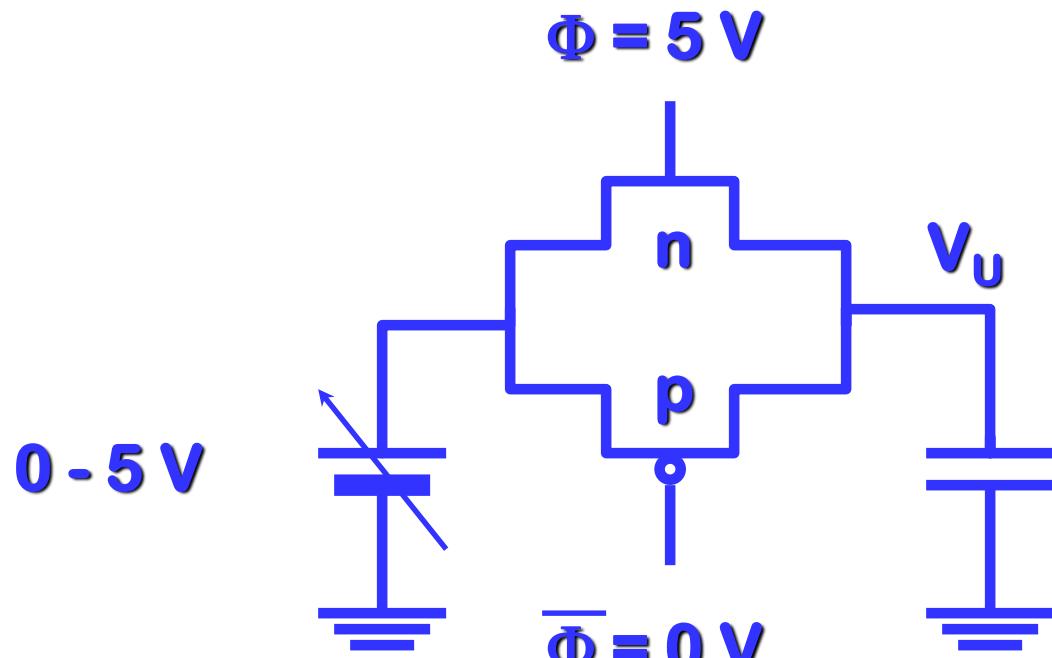
\downarrow vicendo $A_{UV, OFF}$

β_n ? supe 25

Equivalent Resistance Graph



PASS GATE Equivalent Resistance

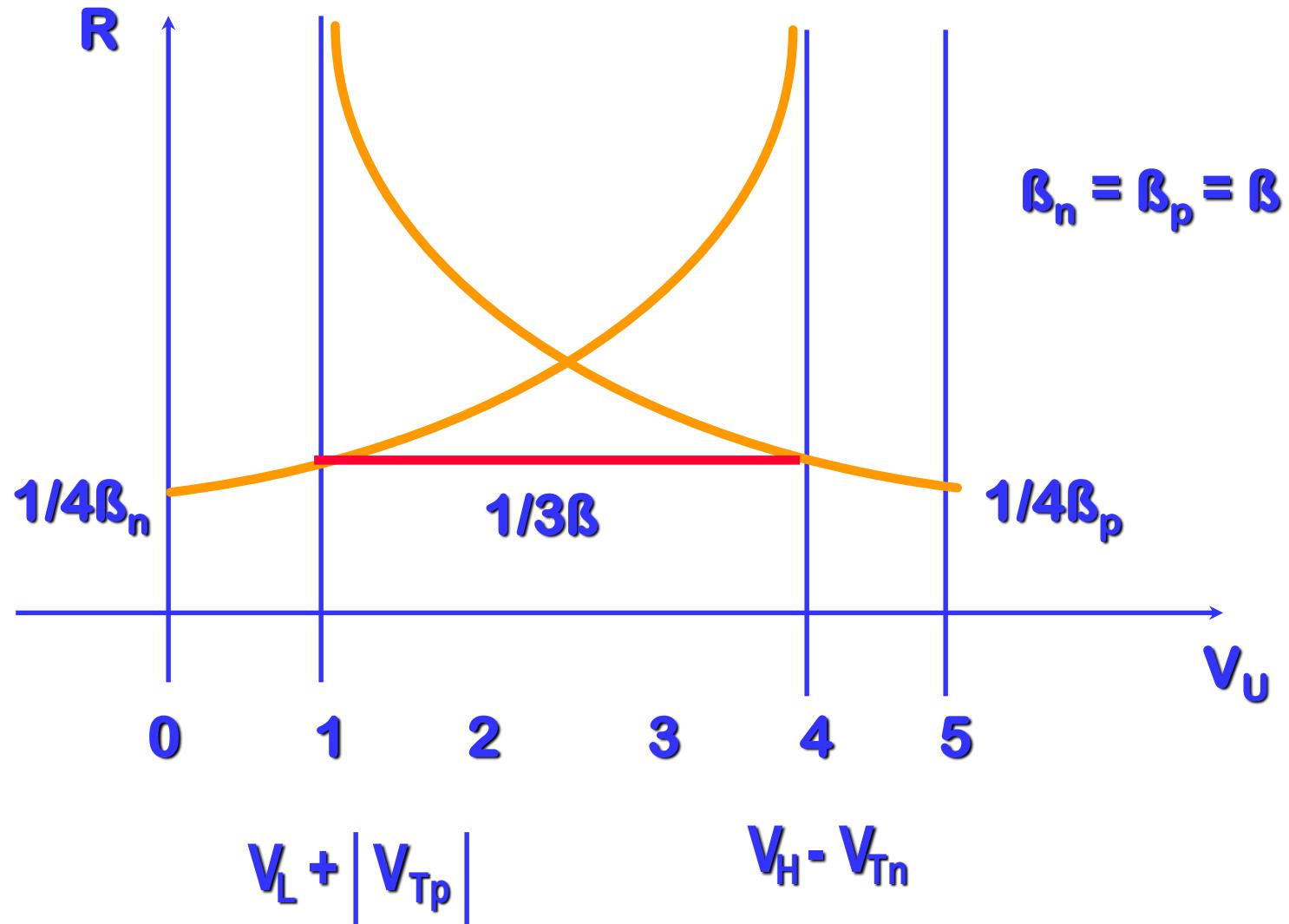


$$R_n = \frac{1}{\beta_n (4 - V_U)}$$

$$R_p = \frac{1}{\beta_p (V_U - 1)}$$

Equivalent Resistance Graph

Posso TRASFORMARE TUTTO A VOLTAGE!



Lay-out rules

❖ Silicon Foundries provides rules for:

- Minimum size for diffusion
- Minimum size for poly
- Minimum size for metal
- Minimum size for contacts
- Well distance
-

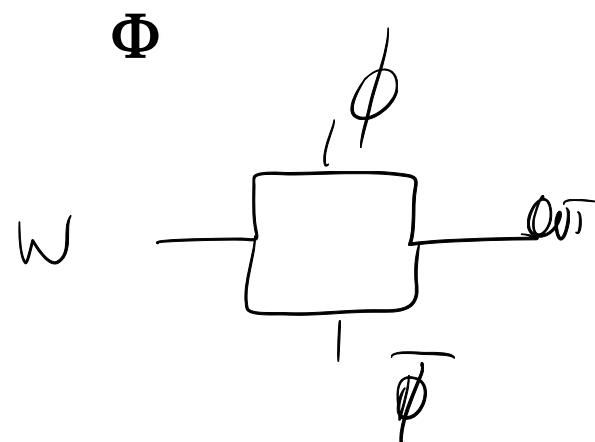
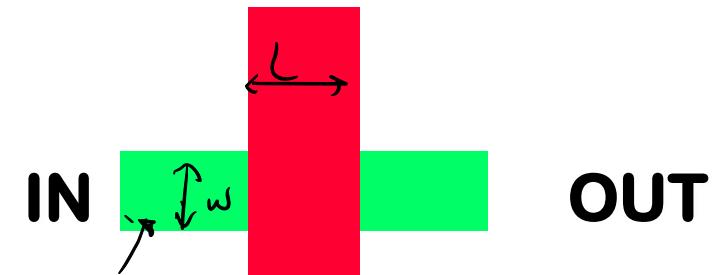


Color codes

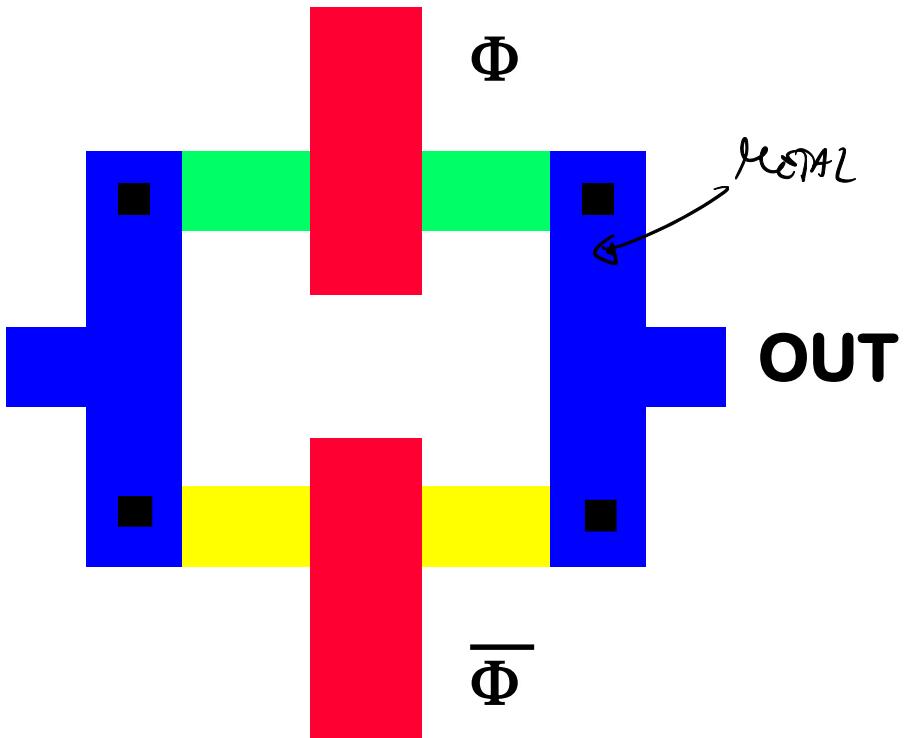
❖ Green	=	diffusion“n”
❖ Yellow	=	diffusion“p”
❖ Red	=	poly
❖ Blue	=	metal 1
❖ Light Blue	=	metal 2
❖ Black	=	contacts
❖ White	=	via

Lay-out

✿ Pass Transistor

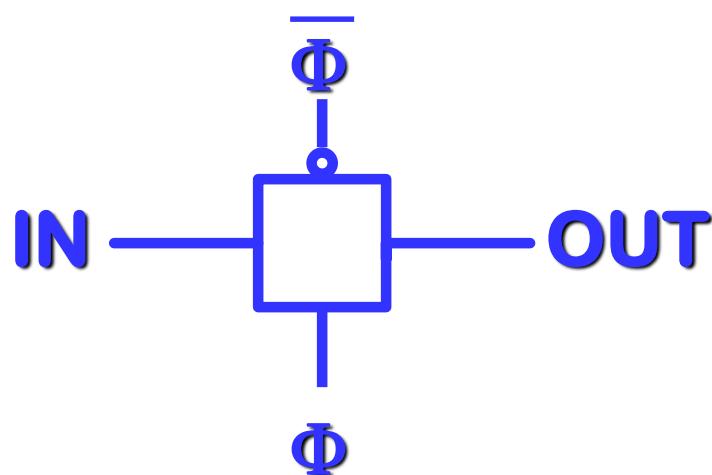
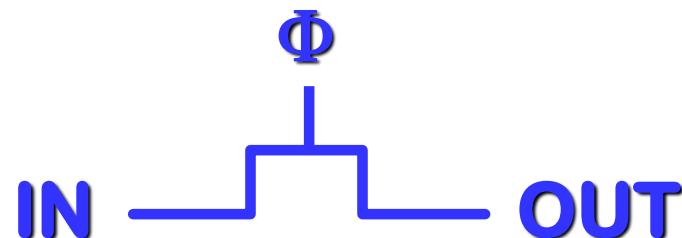


Pass Gate

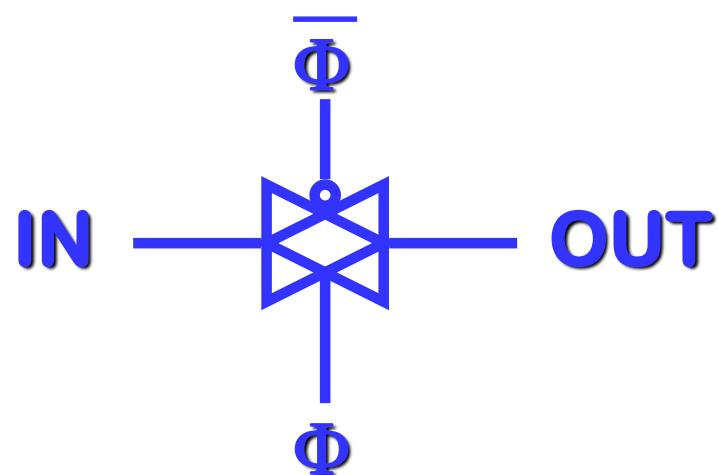
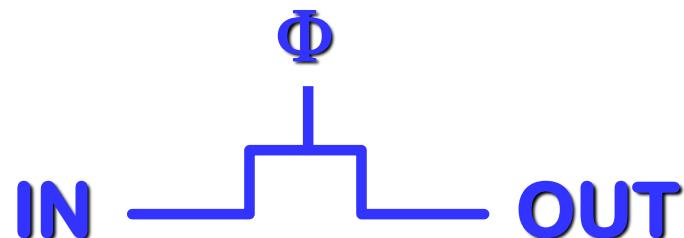


Pass Transistor e Pass Gate

✧ Electrical Symbol



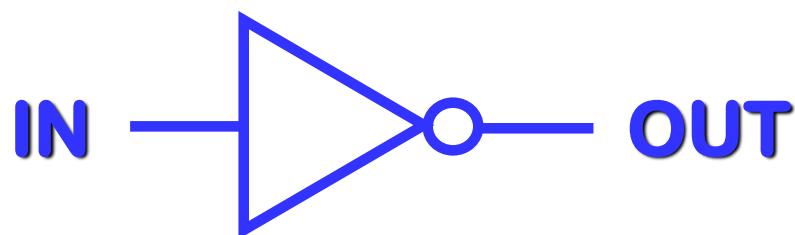
Logic Symbol



INVERTER

❖ Implementation of the logic NOT Function

Logic Symbol

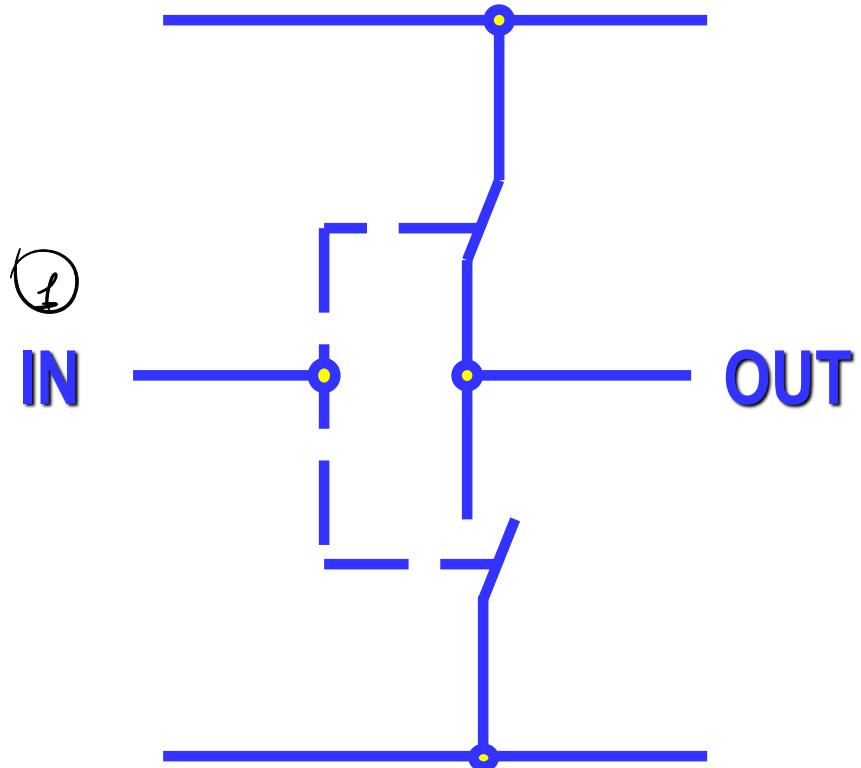


Truth Table

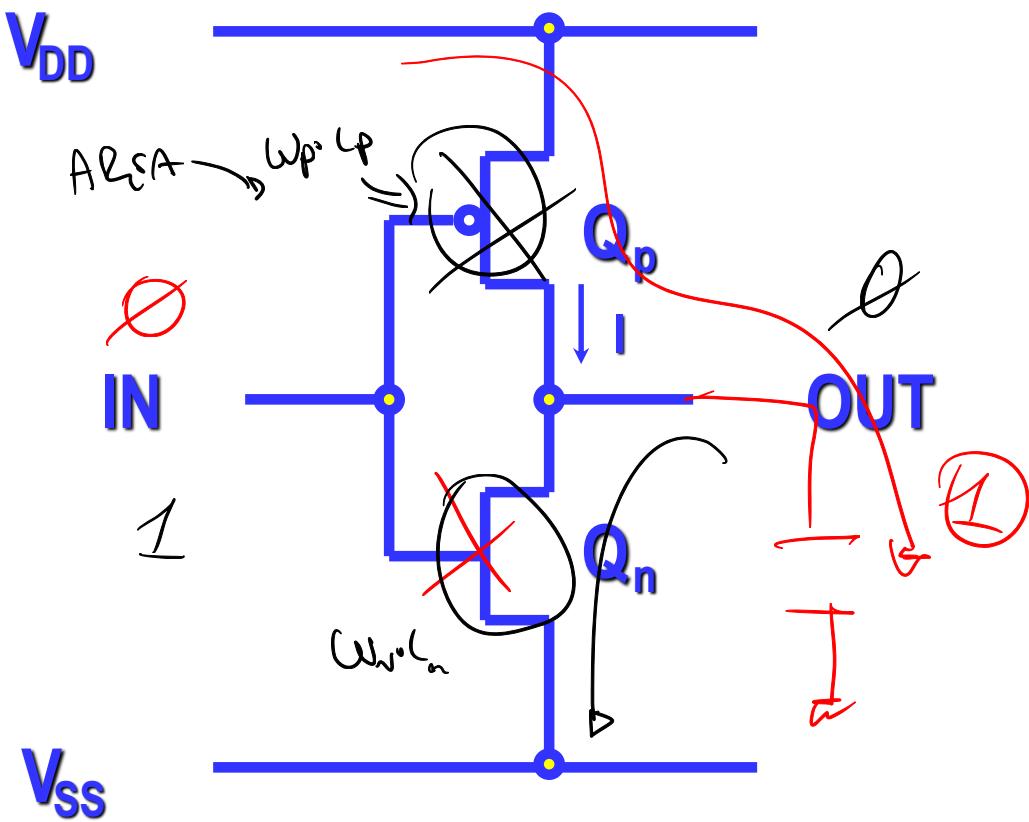
IN	OUT
0	1
1	0

INVERTER Circuit

Switch based idea

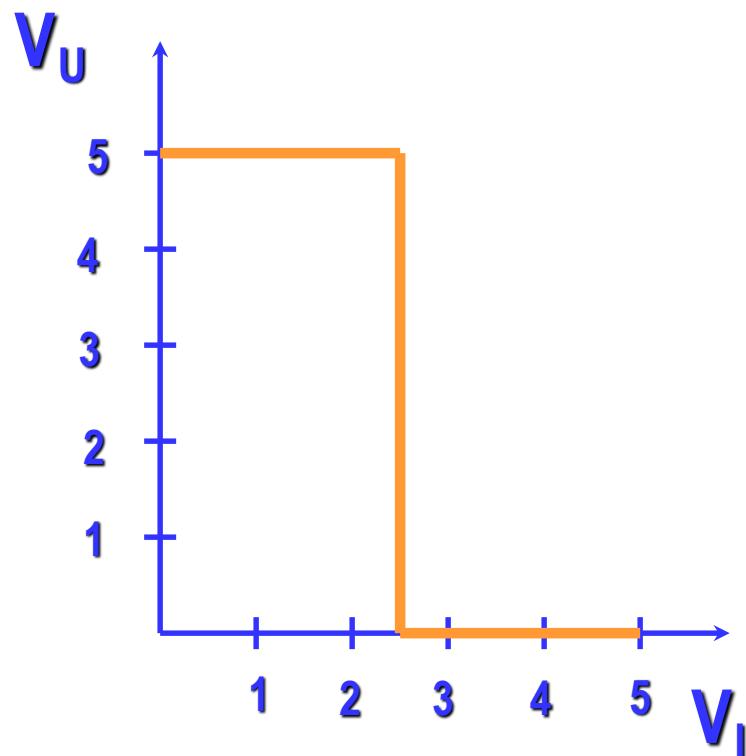


CMOS

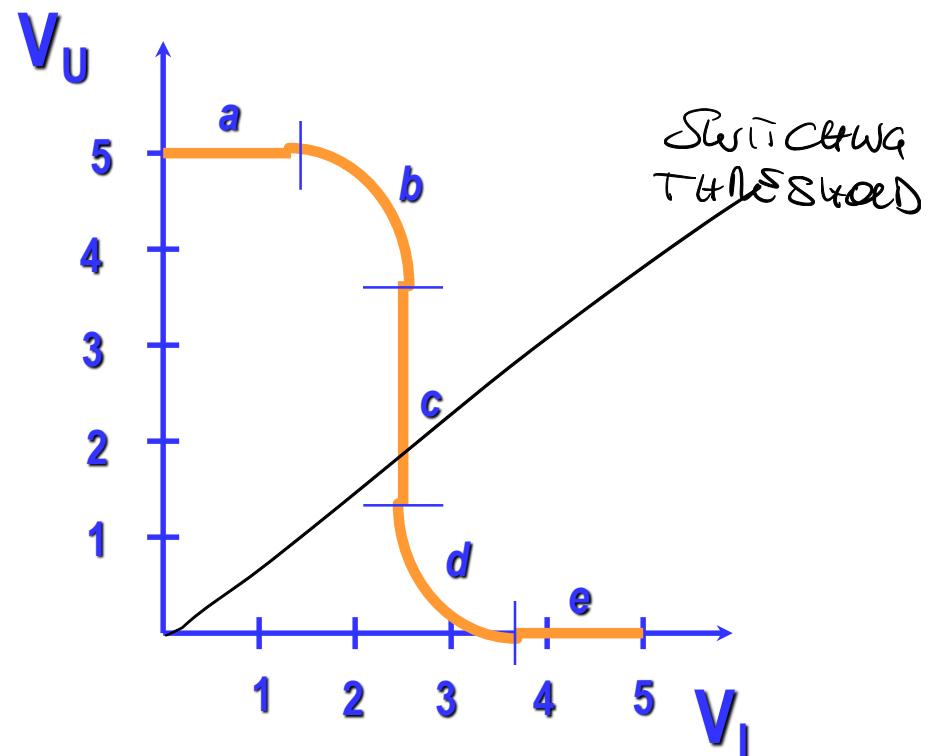


INVERTER Voltage Transfer Curve

IDEAL

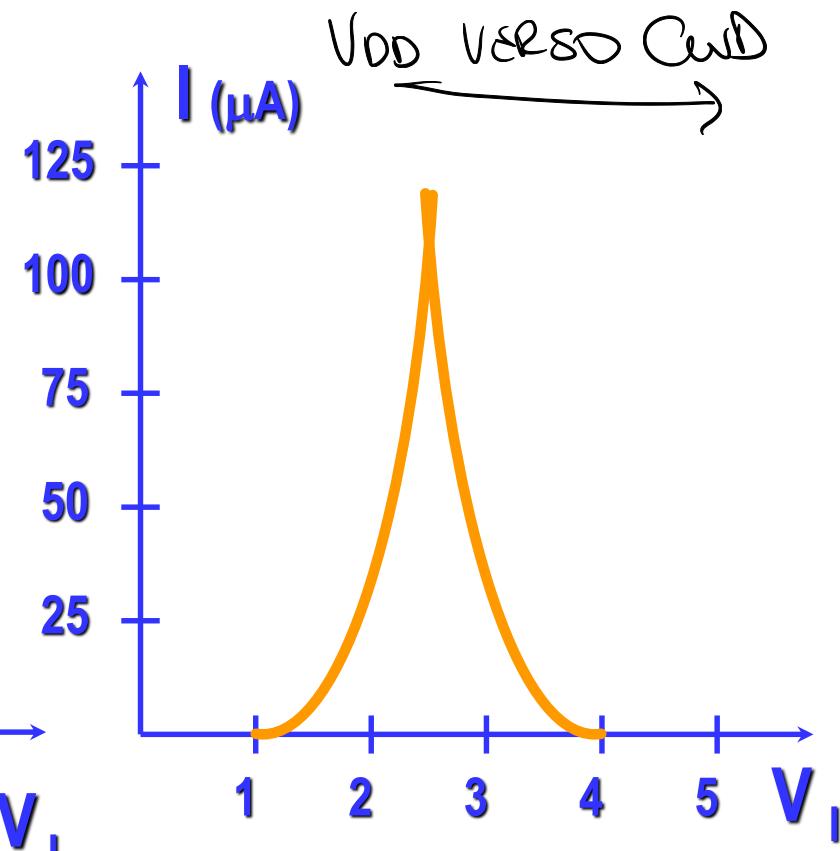
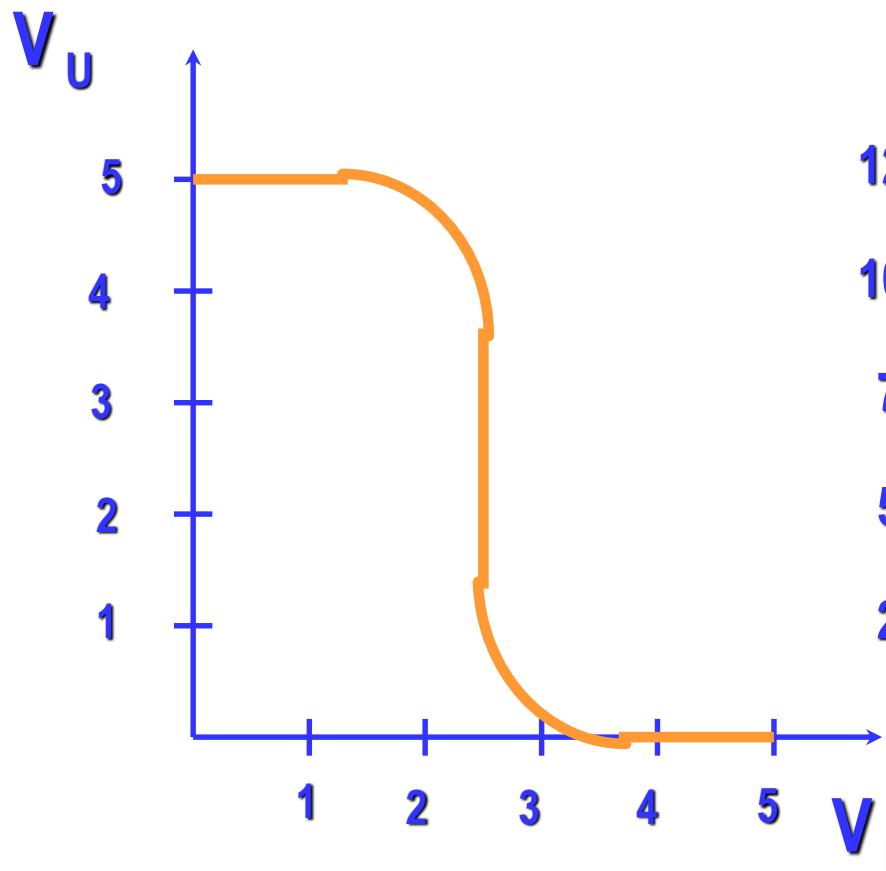


REAL

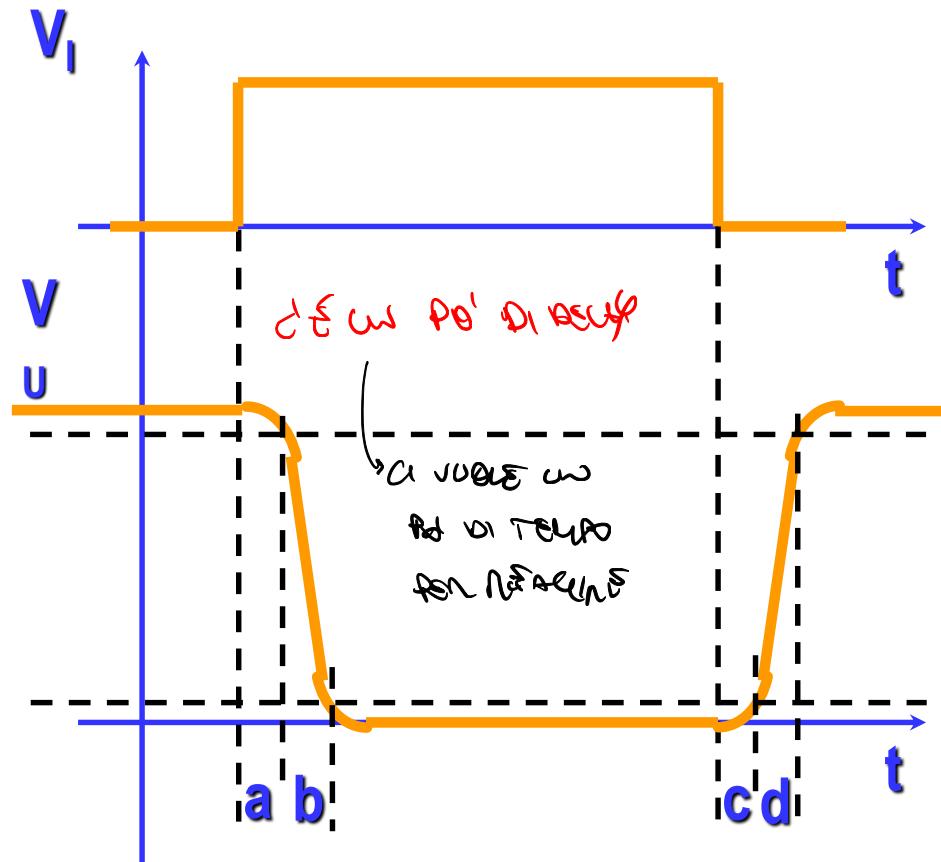
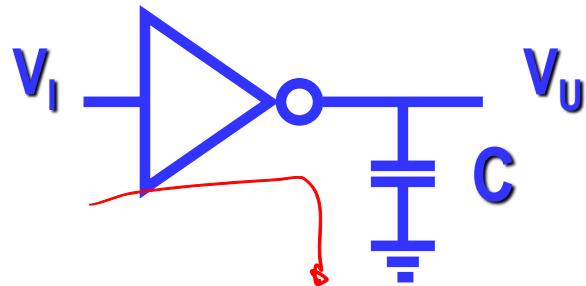


Current Transfer Curve

With $\beta_n = \beta_p$



Driving Capacitive Loads



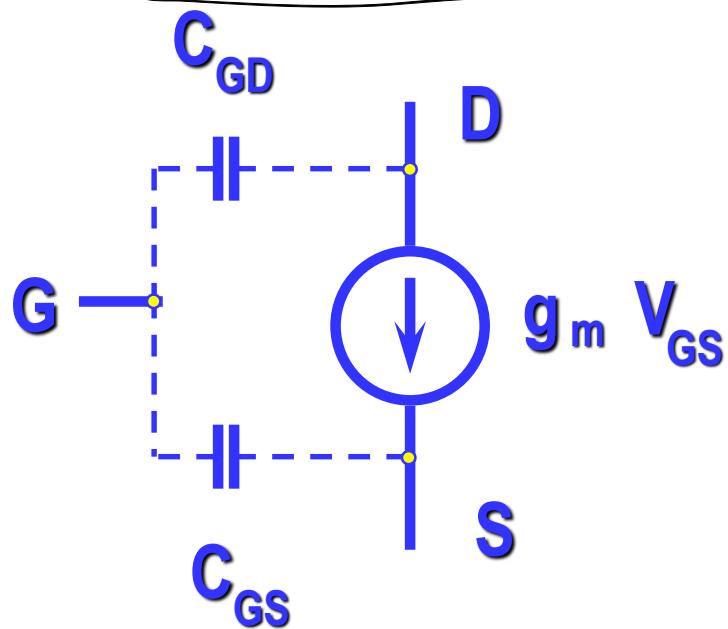
Capacitance

- 1 ✨ Input Capacitance of driven Gates
- 2 ✨ Drain-Sub and Source-Sub Juction Capacitance

CAPACITÄT DER GATE

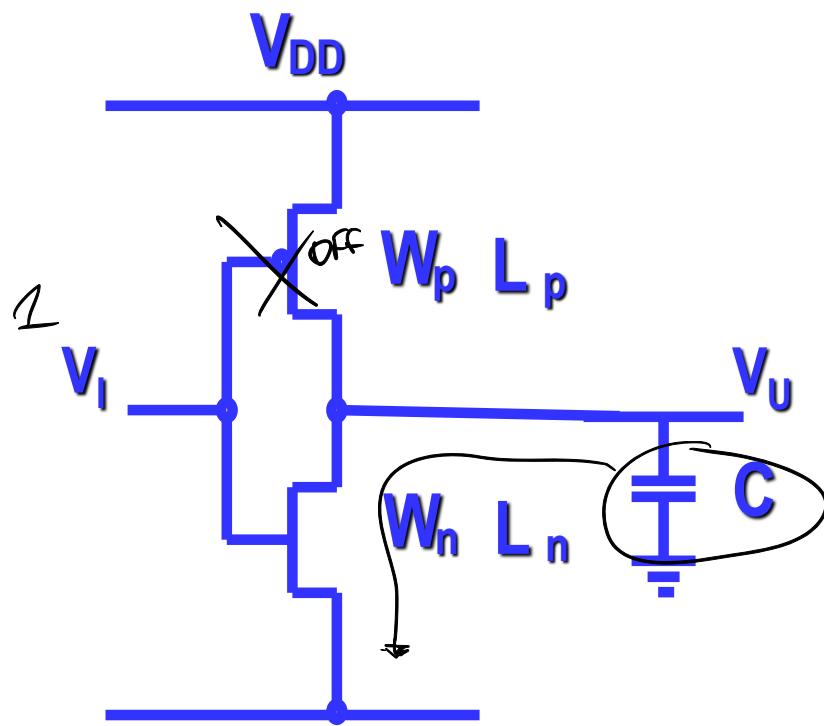
$$C_G = C_{ox} W * L$$

$$C_{ox} = \epsilon_{ox} / t_{ox}$$



- 3 ✨ Routing Capacitance → Distanz und Widerstandswerte

Propagation Delay



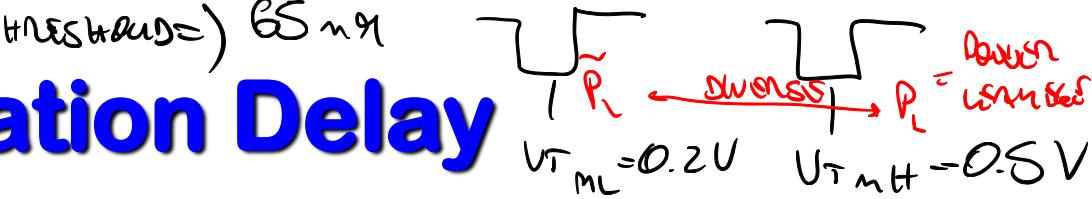
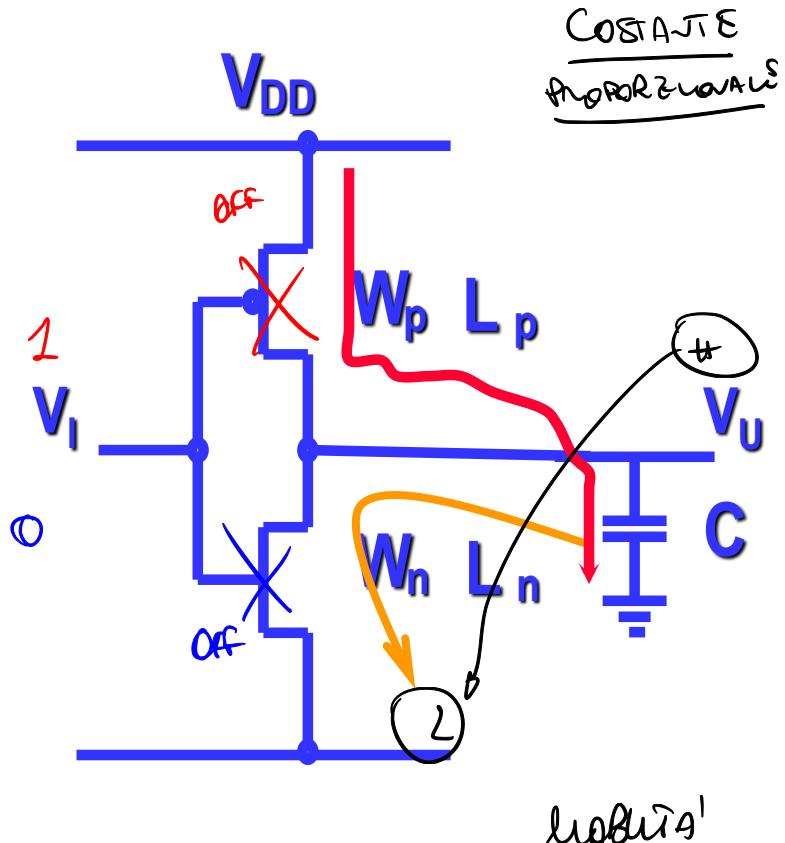
$$P_{DN} \propto \frac{C V_{DD}^2}{T}$$

$$P_{LSAN} \propto V_{DD} \cdot I_{LSAN}$$

$$I_L(V_{TM_L}) < I_C(V_{TM_C})$$

STESO PROCESSO, DIVERSO THRESHOLD = 65 nm

Propagation Delay



$$t_{pH} \propto \frac{KC}{\beta_n} \frac{1}{V_{DD} - V_{Tn}}$$

t_{pH} = t_{wait to low}

DIPENDE DA QUANTO ESSO A VOLO -

$$t_{pL} \propto \frac{KC}{\beta_p} \frac{1}{V_{DD} + V_{Tp}}$$

VELOCITA' \rightarrow SPESA POTENZA

POTENZA \rightarrow PESO VELOCITA'

$$\text{CONTRACCIA} \text{ EQUIVALENTE} = \beta_n = \mu_n C_{ox} \frac{W_n}{L_n}$$

CAPACITA'

OSSIMO

$$\beta_p = \mu_p C_{ox} \frac{W_p}{L_p}$$

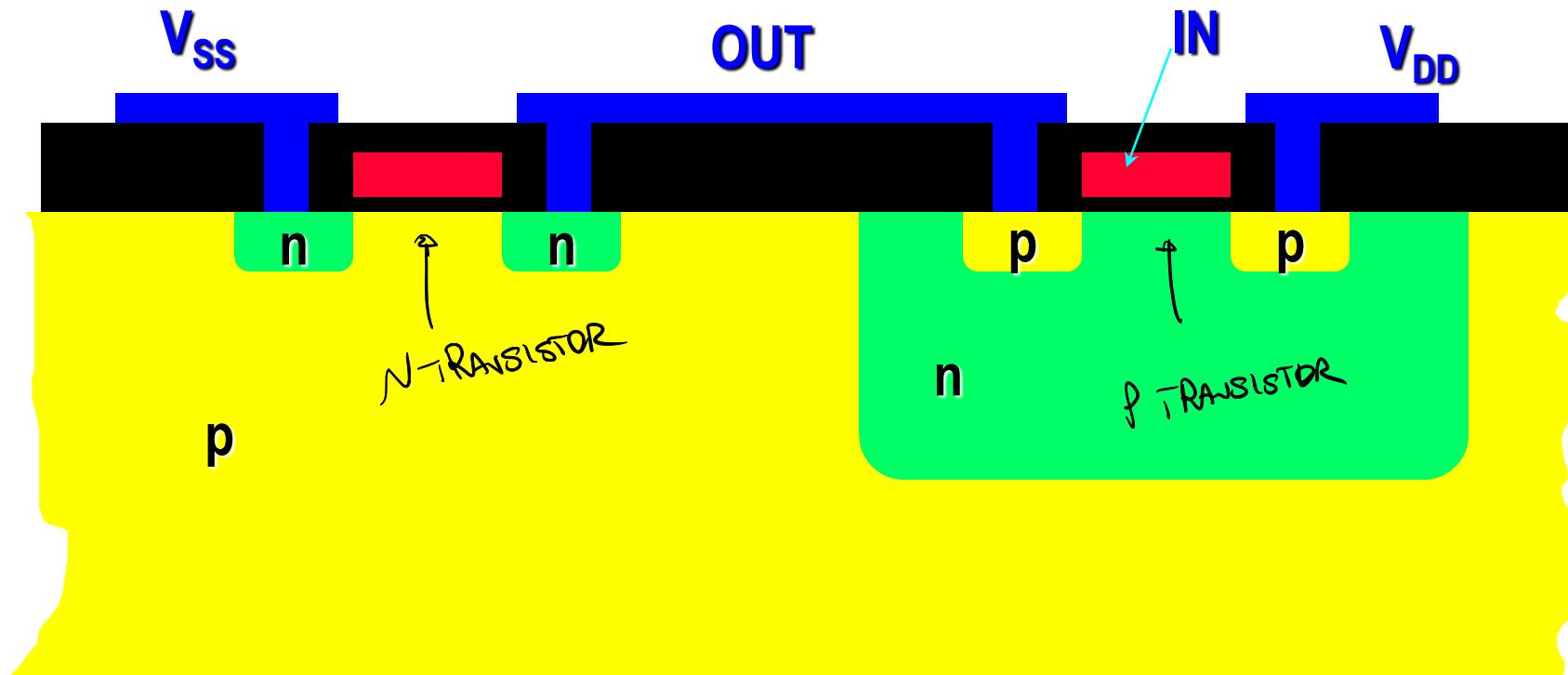
Power Consumption

- ❖ Charge: Capacitor store energy $E_C = \frac{1}{2} CV^2$
- ❖ Power Supply provides energy $E_f = CV^2$
- ❖ Discharge: Capacitor gives its energy to the inverter
- ❖ In one cycle the inverter consumes an energy equal to $E_D = CV^2$
- ❖ In the time T the inverter consumes a power consumption of $P_D = E_D/T =$

$$P_D = C V^2 / T = C V^2 f$$

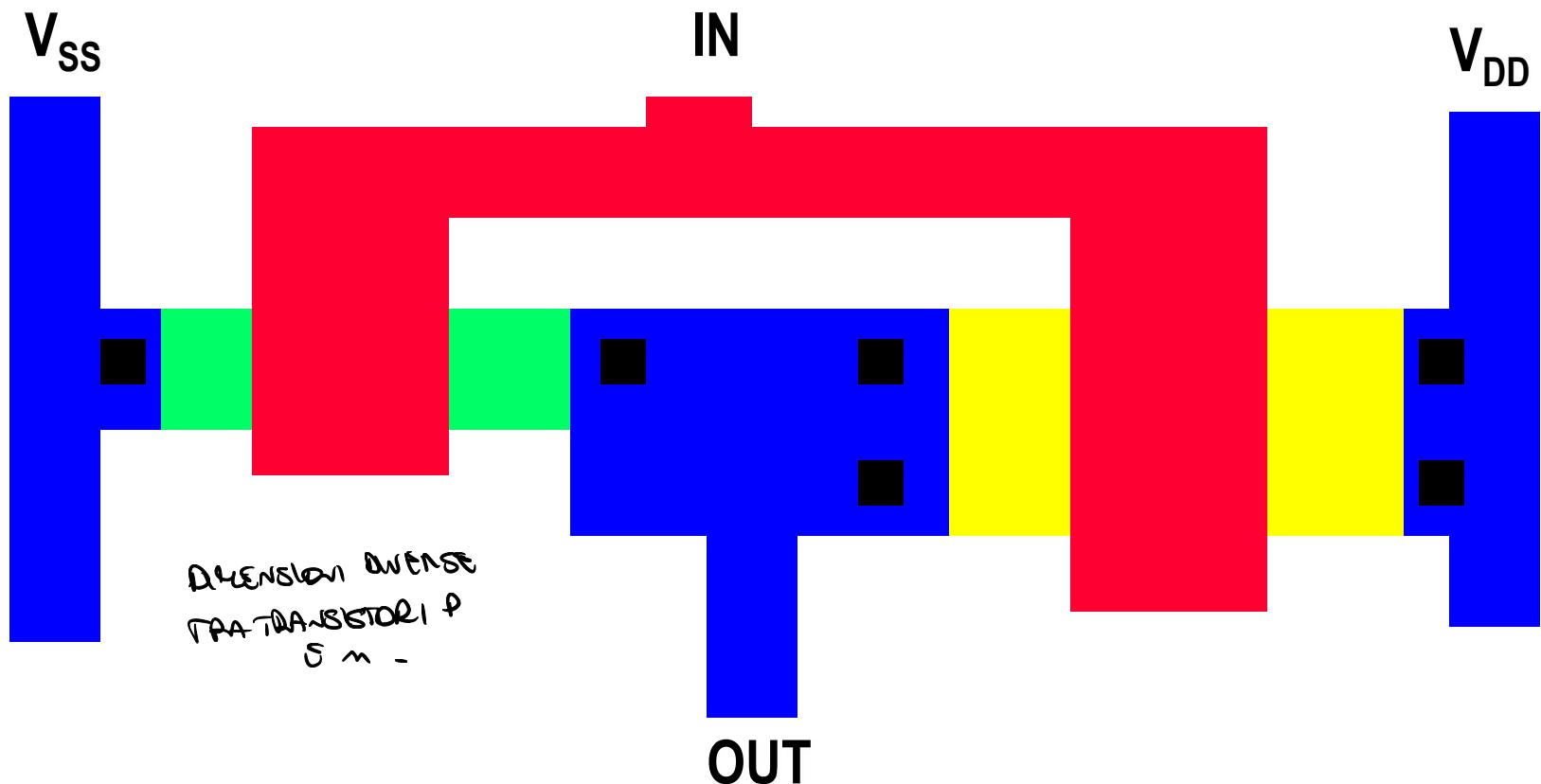
INVERTER Lay-out 1

✧ Cross Section for “n” well process



INVERTER Lay-out 2

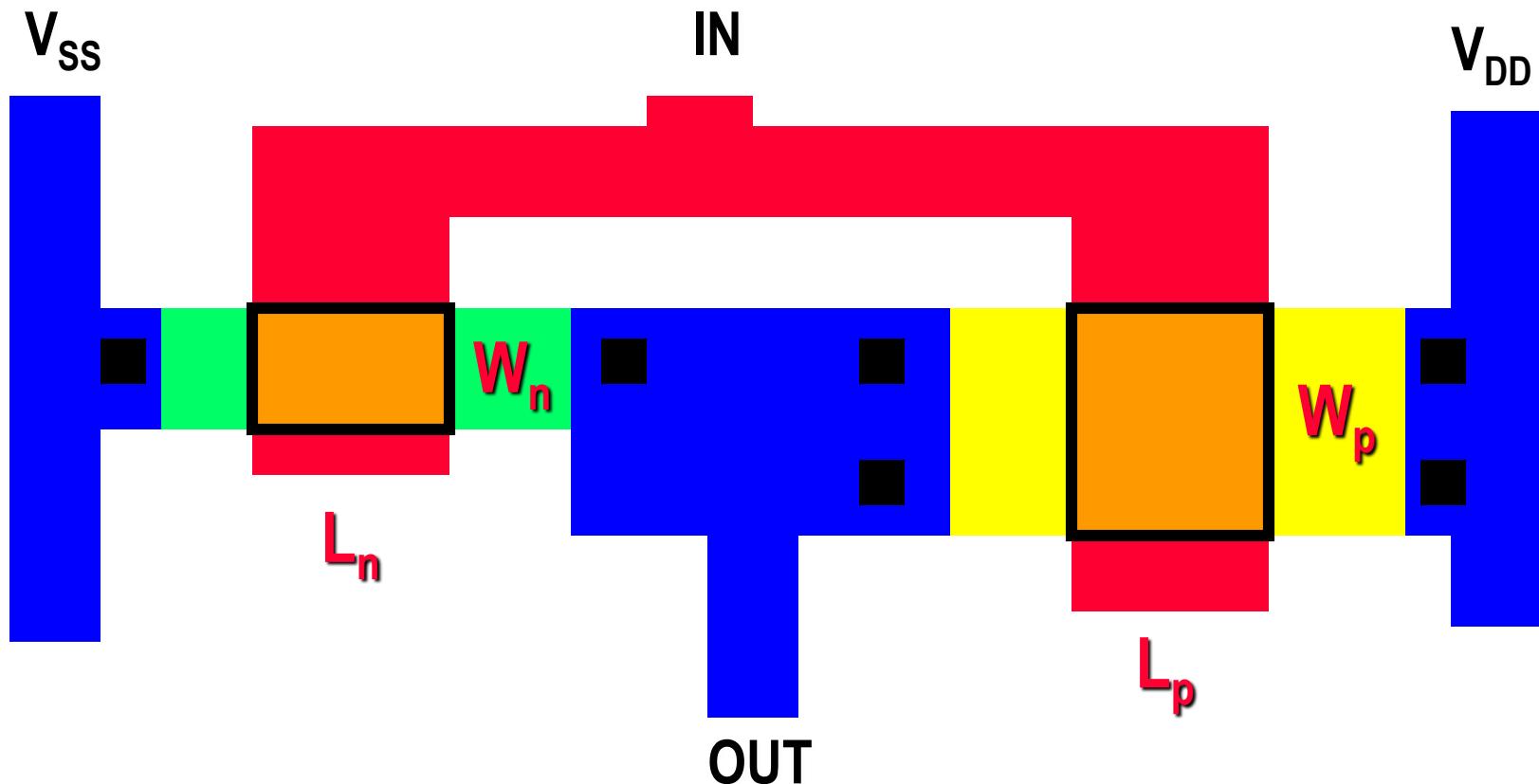
✿ Top view



INVERTER Lay-out 2

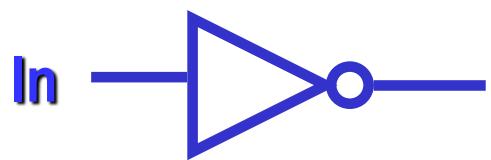
✿ Top view

$$\underline{ST_{ReqA}} \approx A \sim W_n L_n + W_p L_p$$

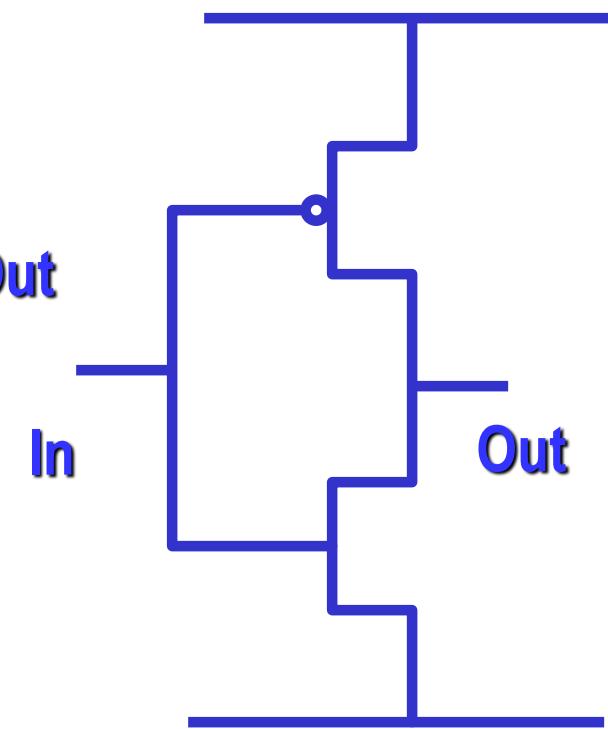


Electronic Abstraction Levels

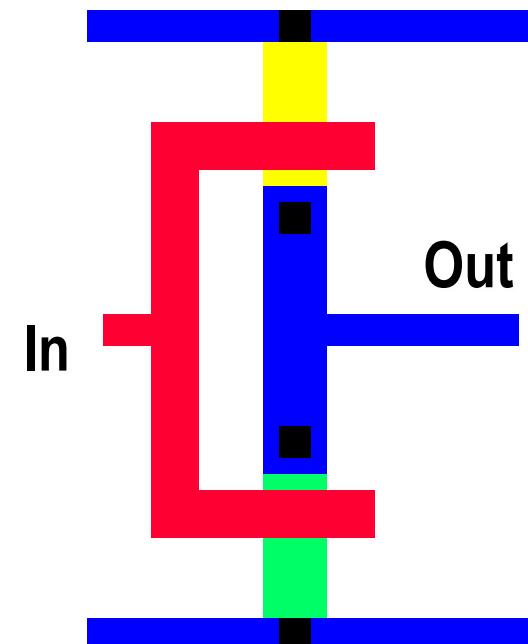
✿ Logic Symbol



Circuit



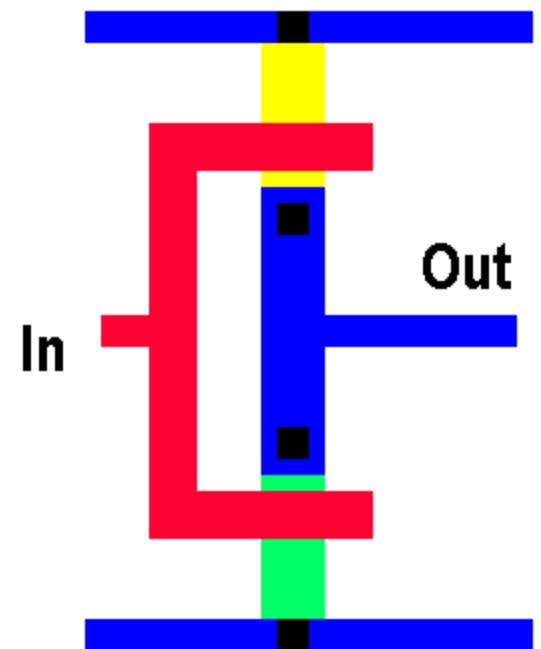
Lay-out



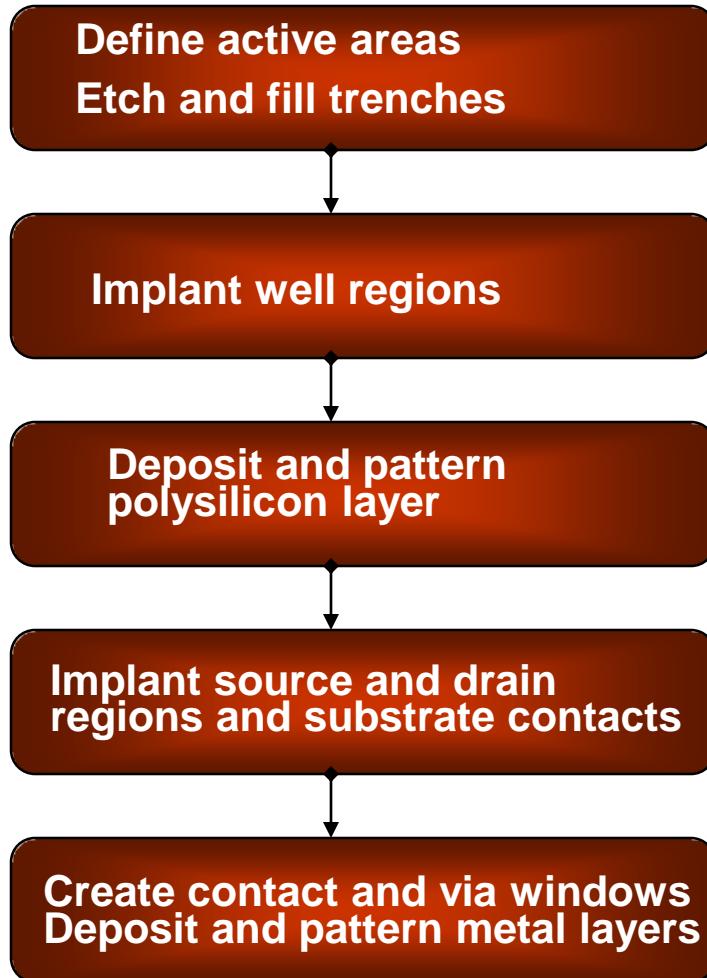
Inverter: Electronic Abstraction Levels

Let's review basic CMOS manufacturing steps and see how to build up a CMOS inverter

Lay-out

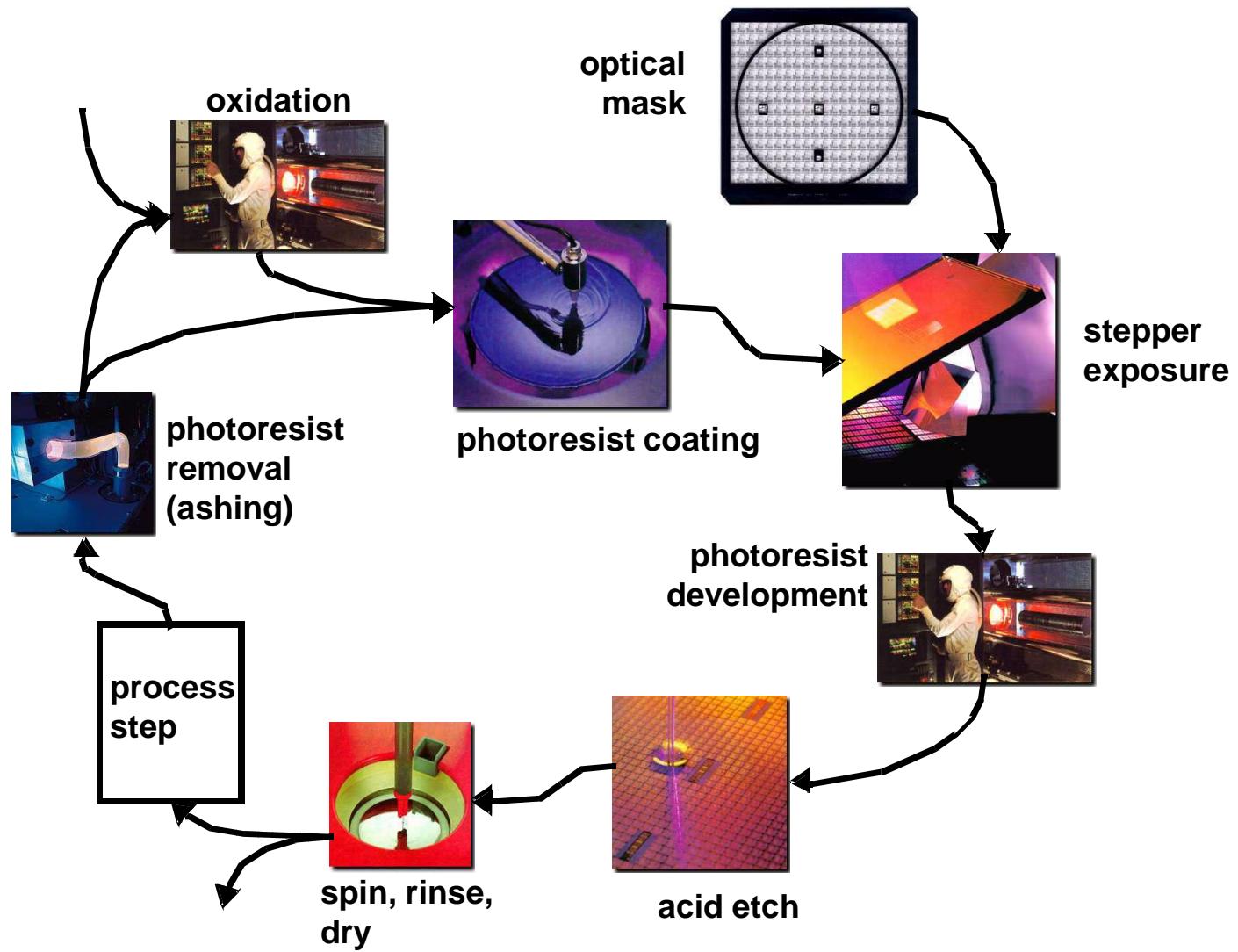


CMOS Process at a Glance



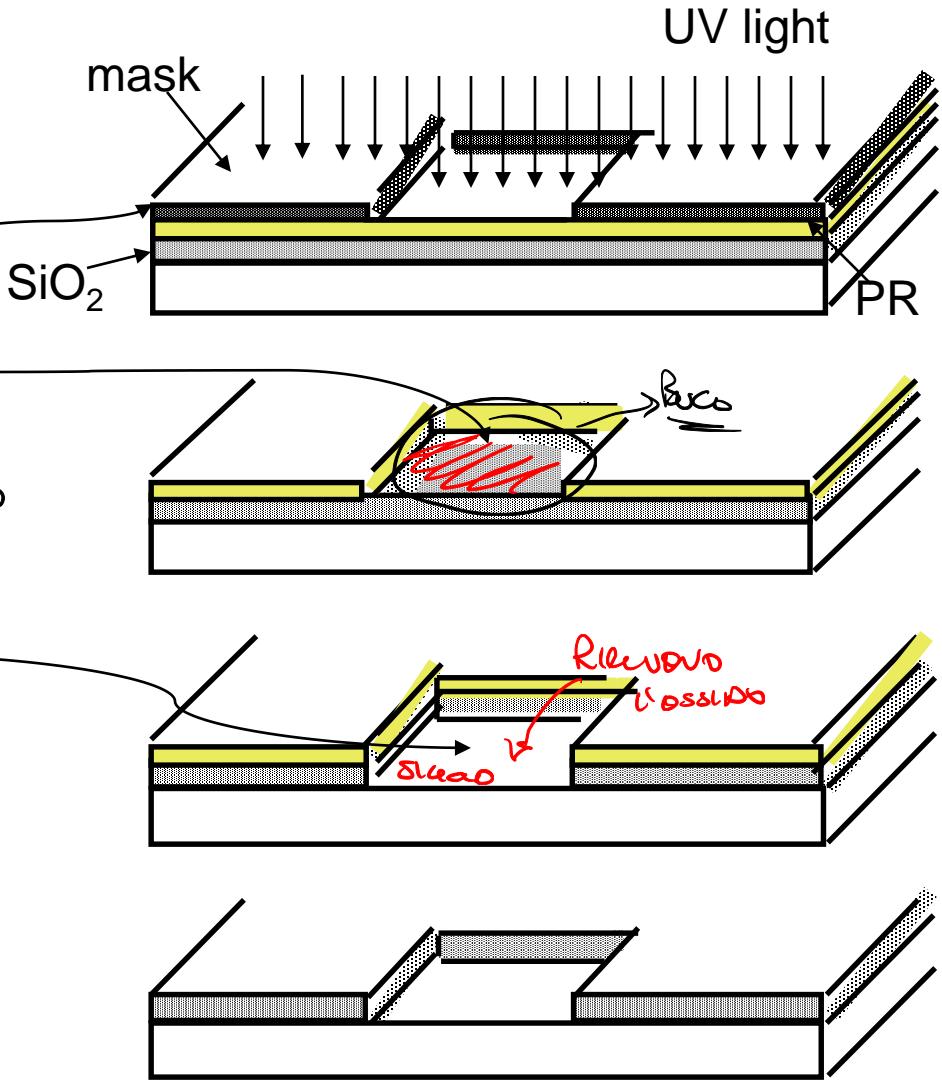
- ❑ One full photolithography sequence per layer (mask)
 - ❑ Built (roughly) from the bottom up
 - 5 metal 2
 - 4 metal 1
 - 2 polysilicon
 - 3 source and drain diffusions
 - 1 tubs (aka wells, active areas)
- exception!

Photolithographic Process

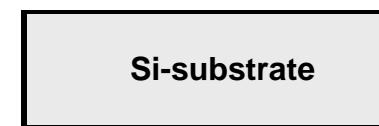


Patterning - Photolithography

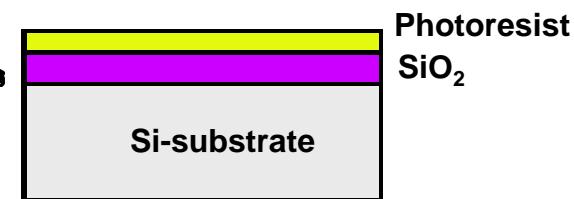
1. Oxidation
2. Photoresist (PR) coating
3. Stepper exposure
4. Photoresist development and bake
 - de exposed Area UV
D'UV' ESSERE RICOSSO
5. Acid etching
 - Unexposed (negative PR)
 - Exposed (positive PR)
6. Spin, rinse, and dry
7. Processing step
 - Ion implantation
 - Plasma etching
 - Metal deposition
8. Photoresist removal (ashing)



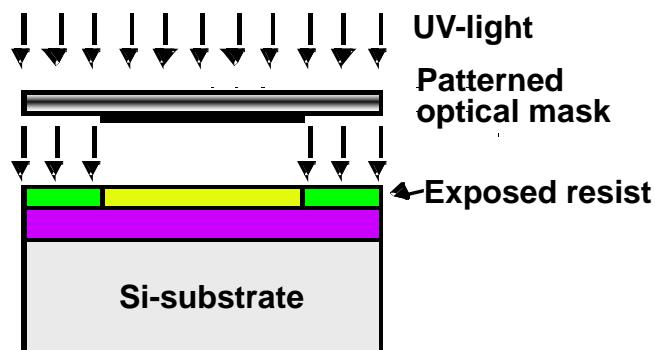
Example of Patterning of SiO₂



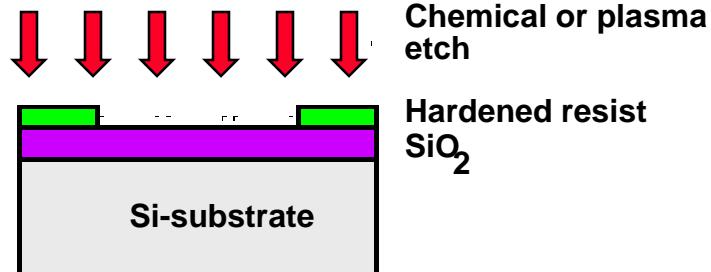
Silicon base material



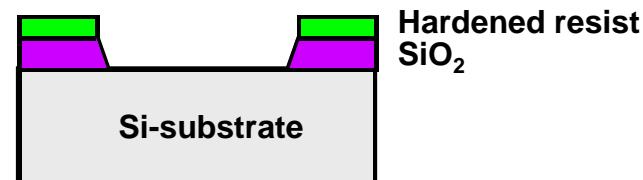
1&2. After oxidation and deposition of negative photoresist



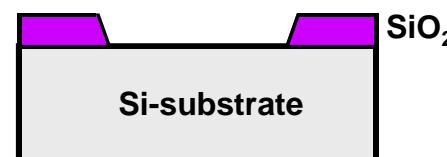
3. Stepper exposure



4. After development and etching of resist, chemical or plasma etch of SiO₂



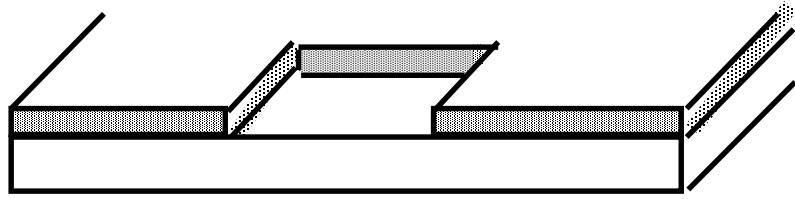
5. After etching



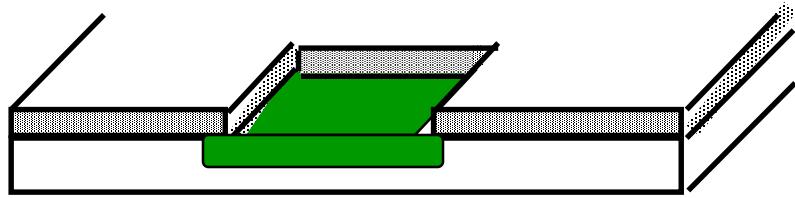
8. Final result after removal of resist

Diffusion and Ion Implantation

1. Area to be doped is exposed
(photolithography)

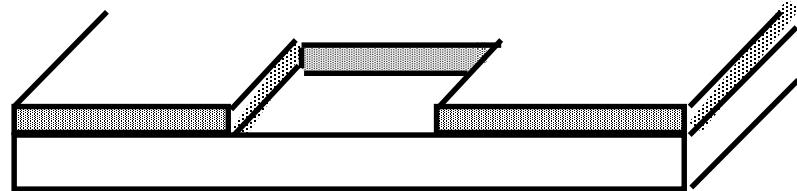


2. Diffusion
or
Ion implantation



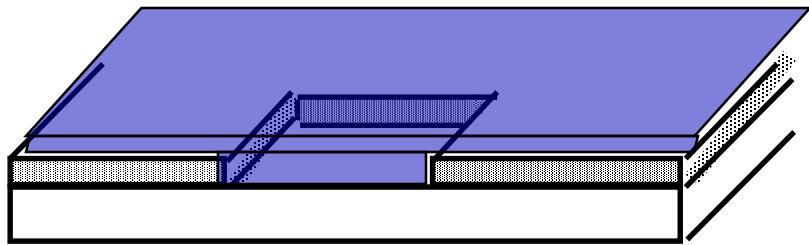
Deposition and Etching

1. Pattern masking
(photolithography)



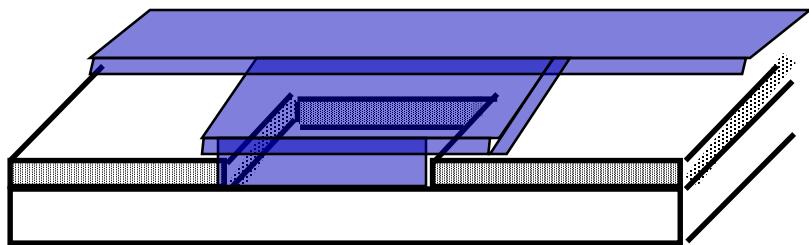
2. Deposit material over entire wafer

CVD (Si_3N_4)
chemical deposition
(polysilicon)
sputtering (Al)



3. Etch away unwanted material

wet etching
dry (plasma) etching



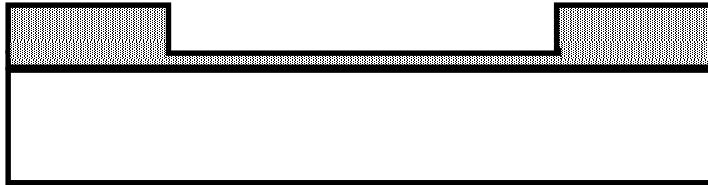
Planarization: Polishing the Wafers



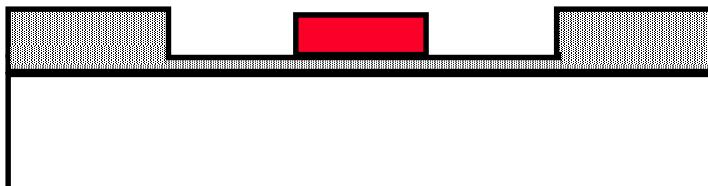
From Smithsonian, 2000

Self-Aligned Gates

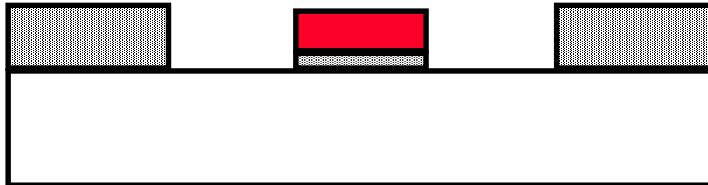
1. Create thin oxide in the “active” regions, thick elsewhere



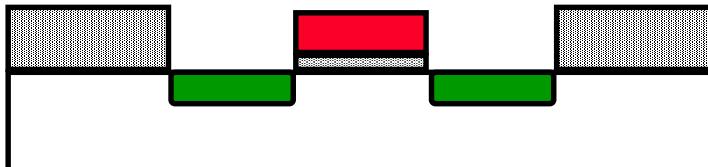
2. Deposit polysilicon



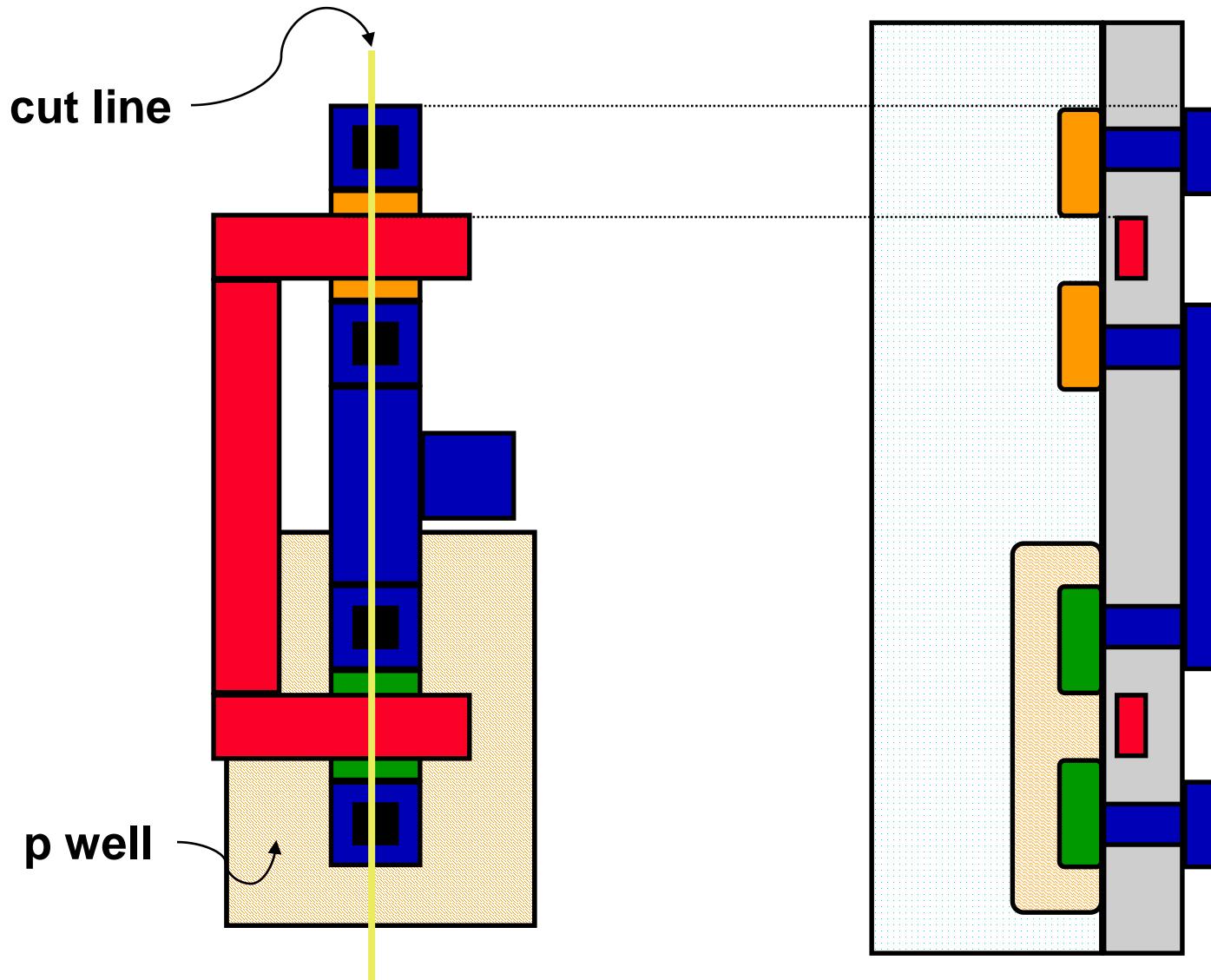
3. Etch thin oxide from active region (poly acts as a mask for the diffusion)



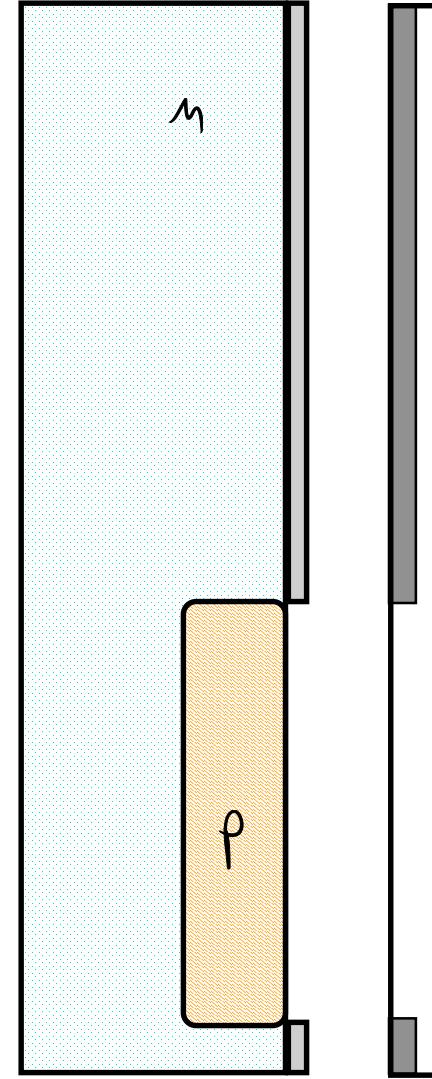
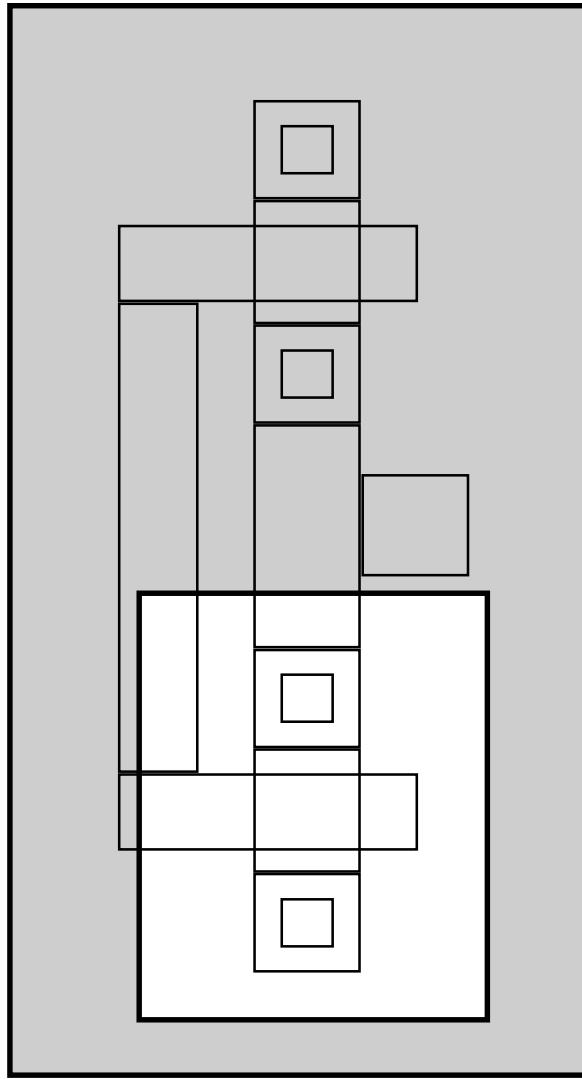
4. Implant dopant



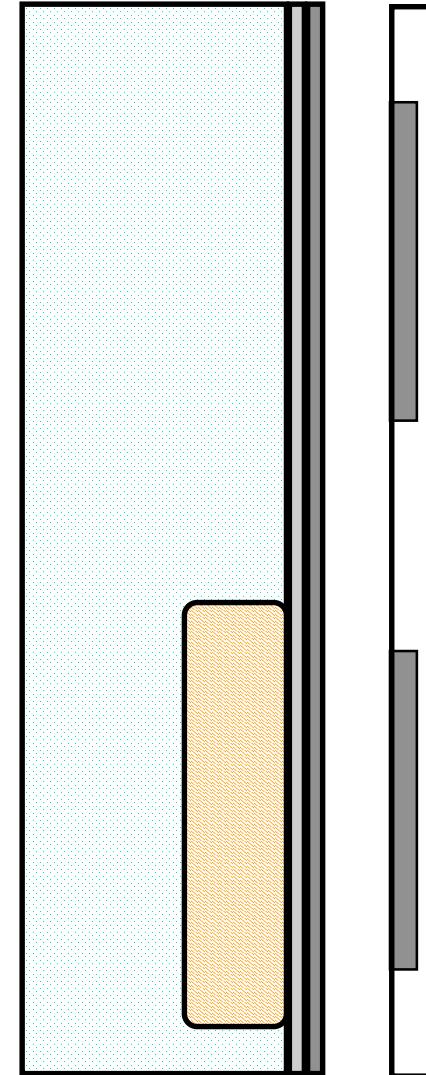
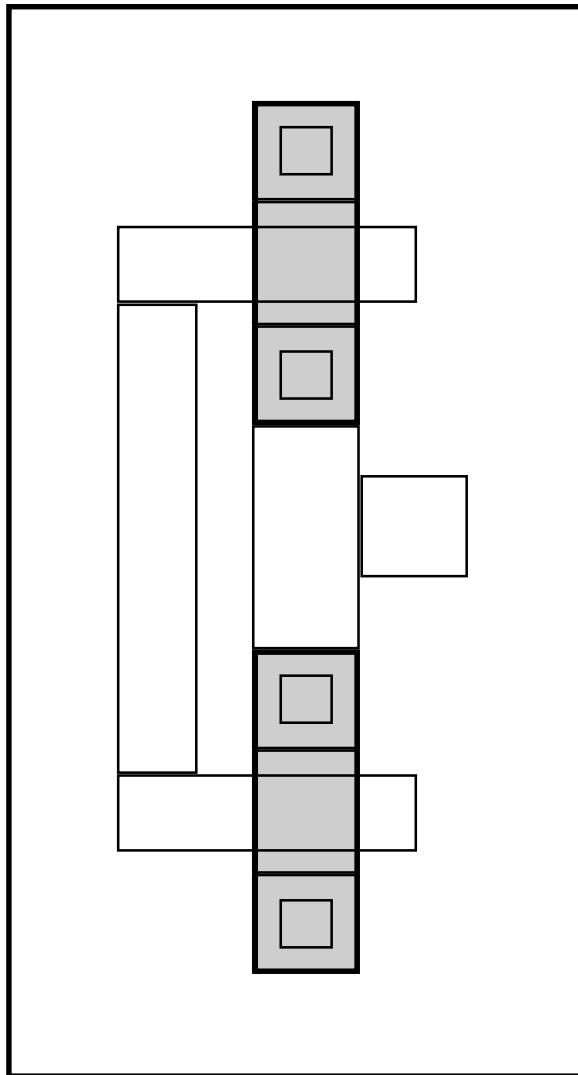
Simplified CMOS Inverter Process



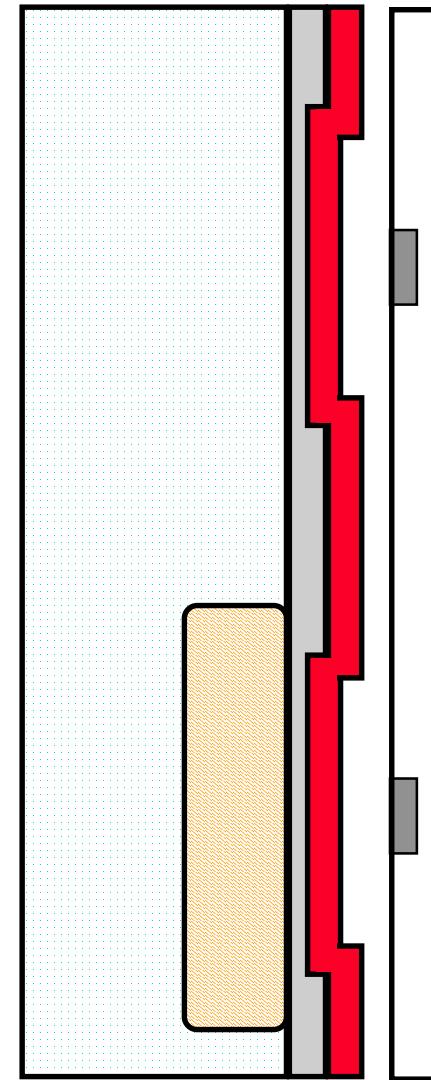
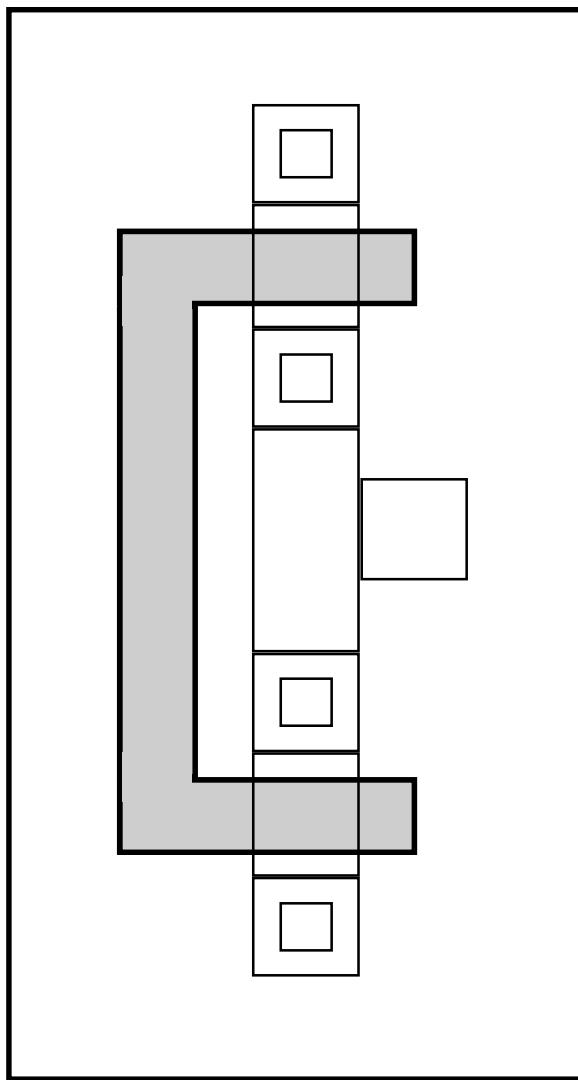
P-Well Mask



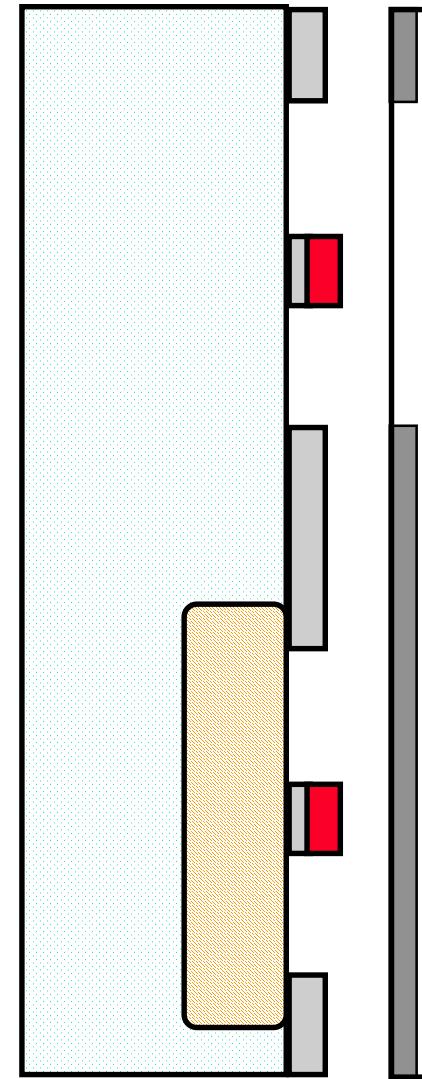
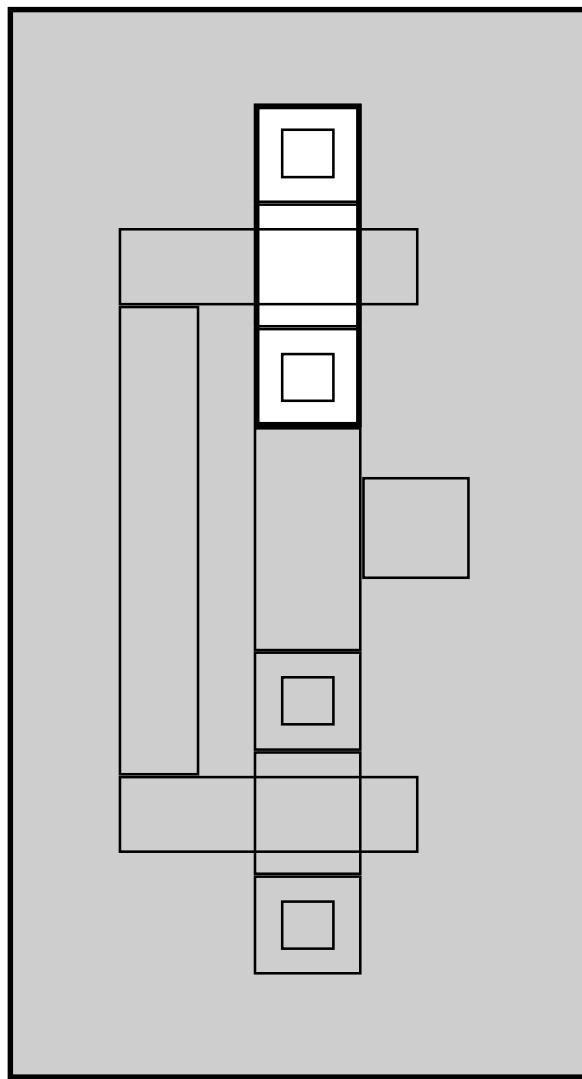
Active Mask



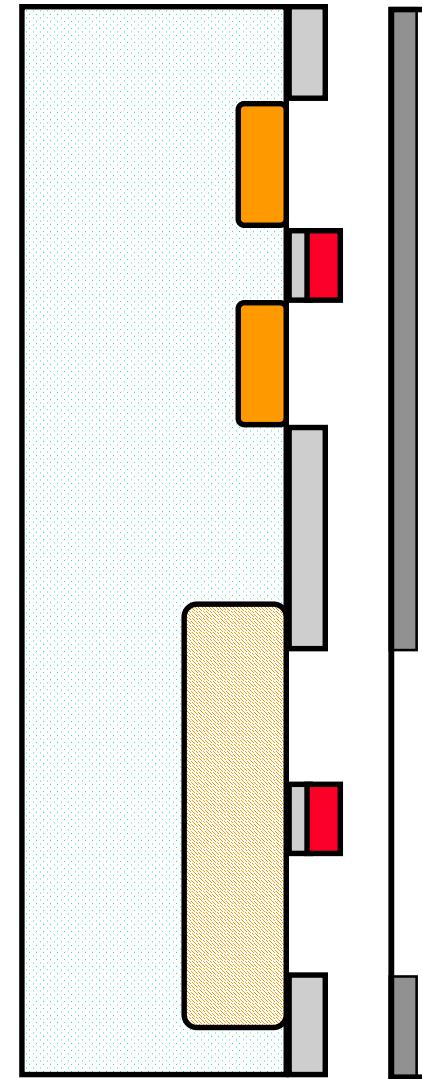
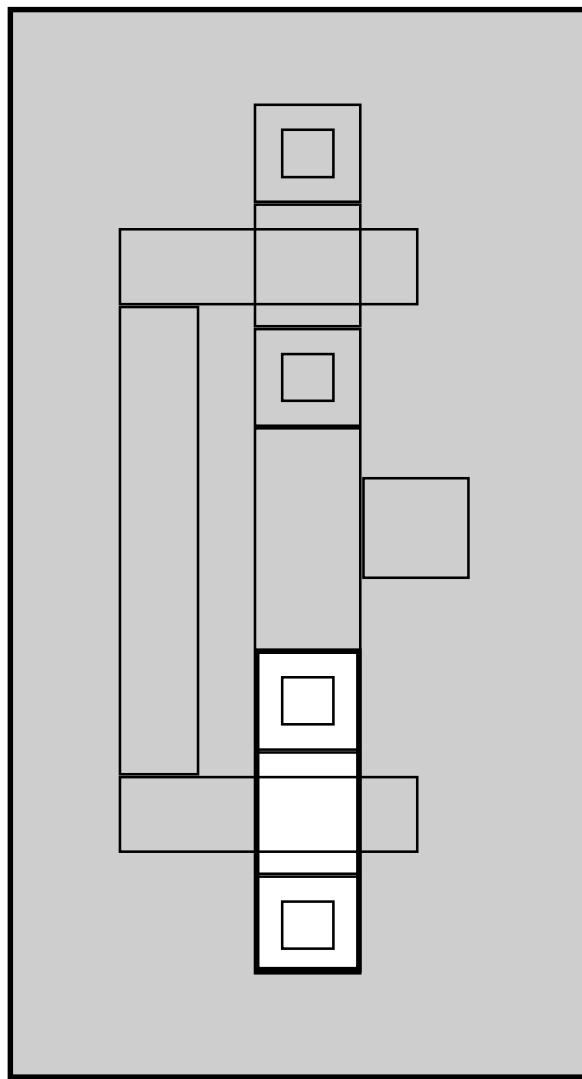
Poly Mask



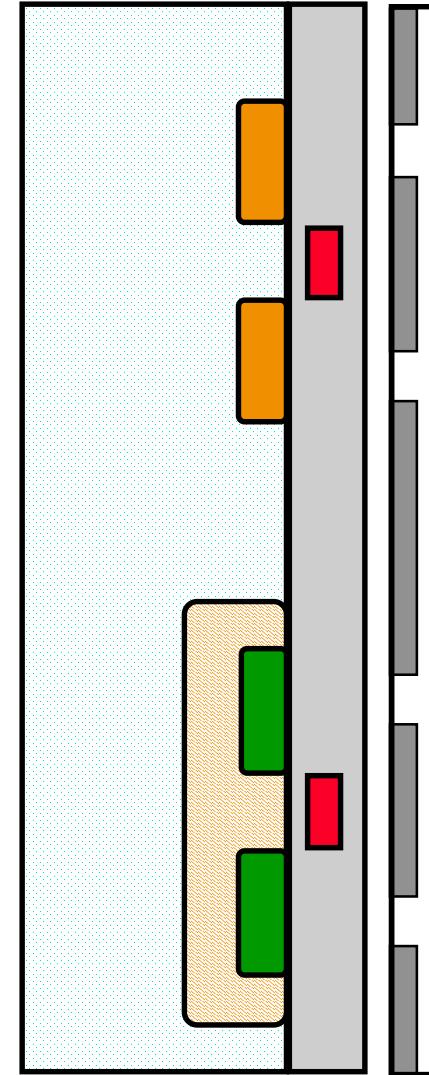
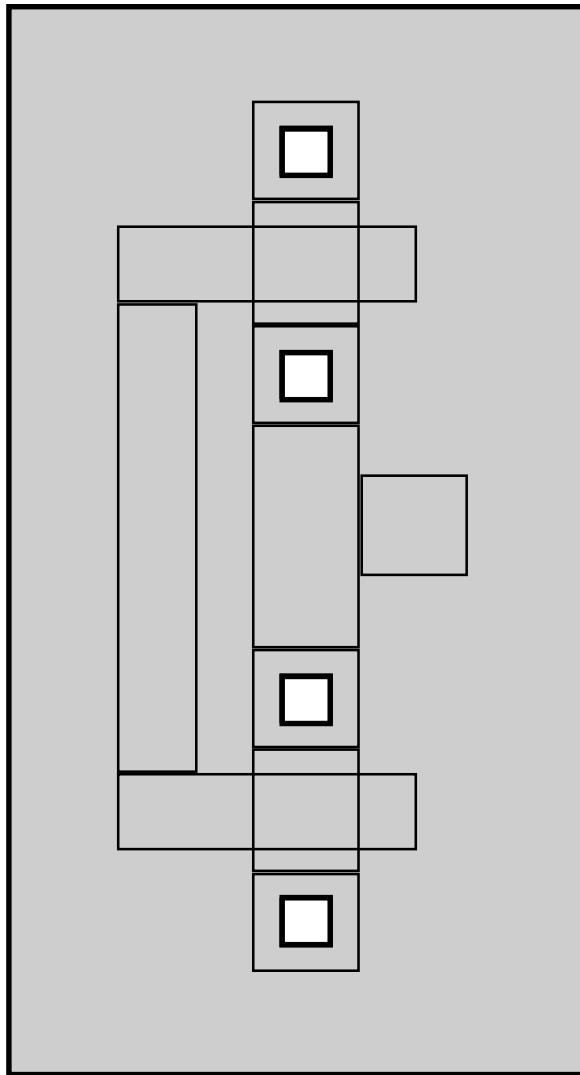
P+ Select Mask



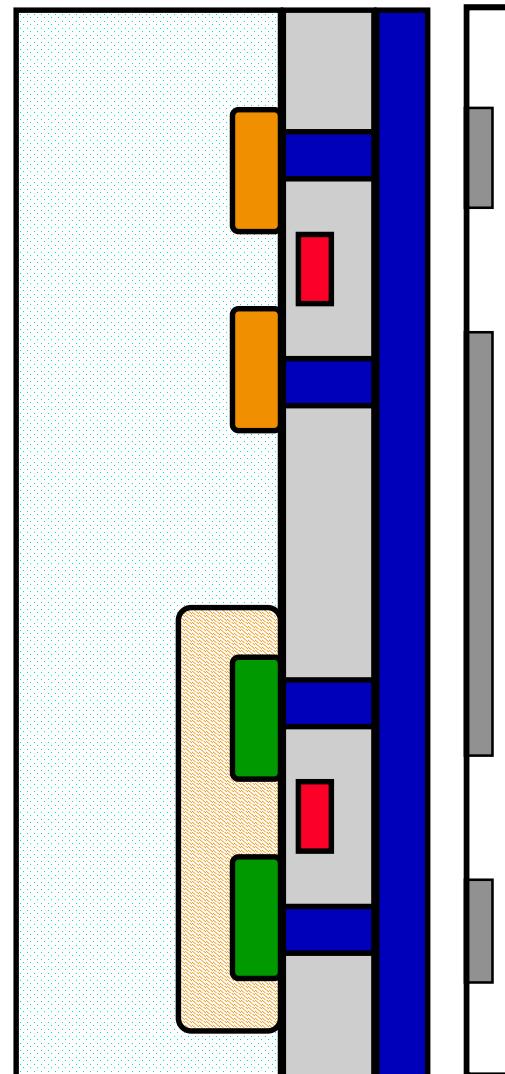
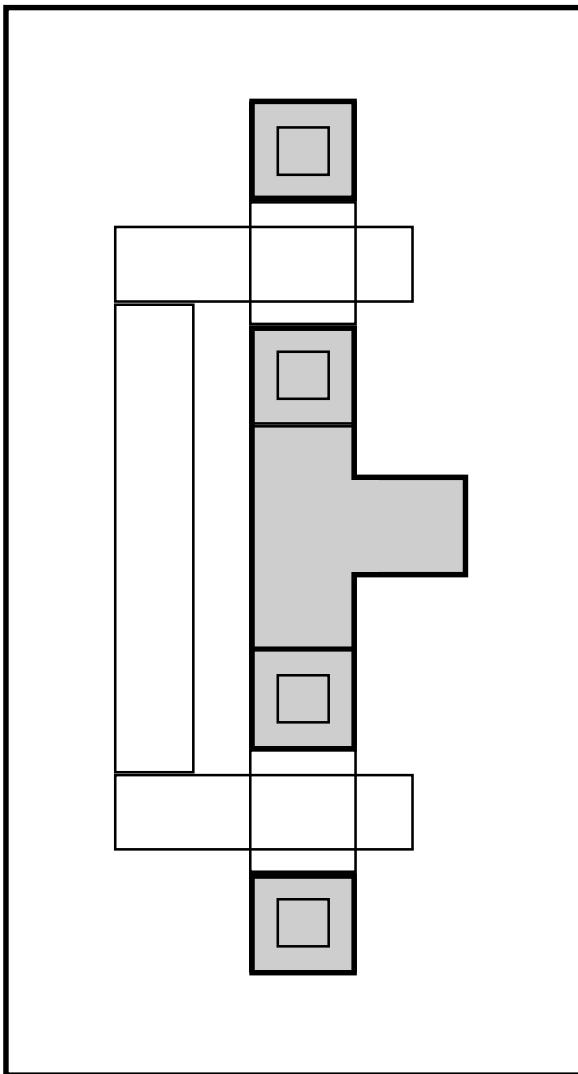
N+ Select Mask



Contact Mask

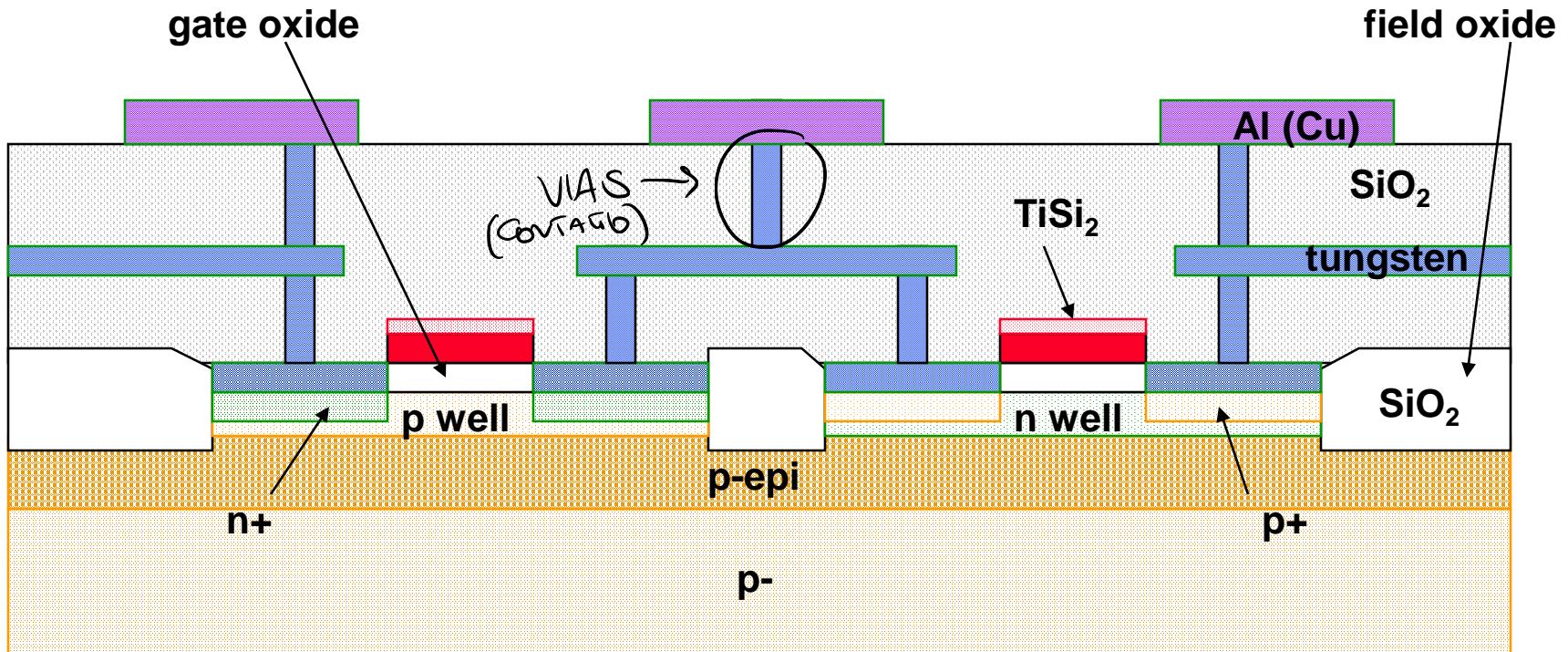


Metal Mask

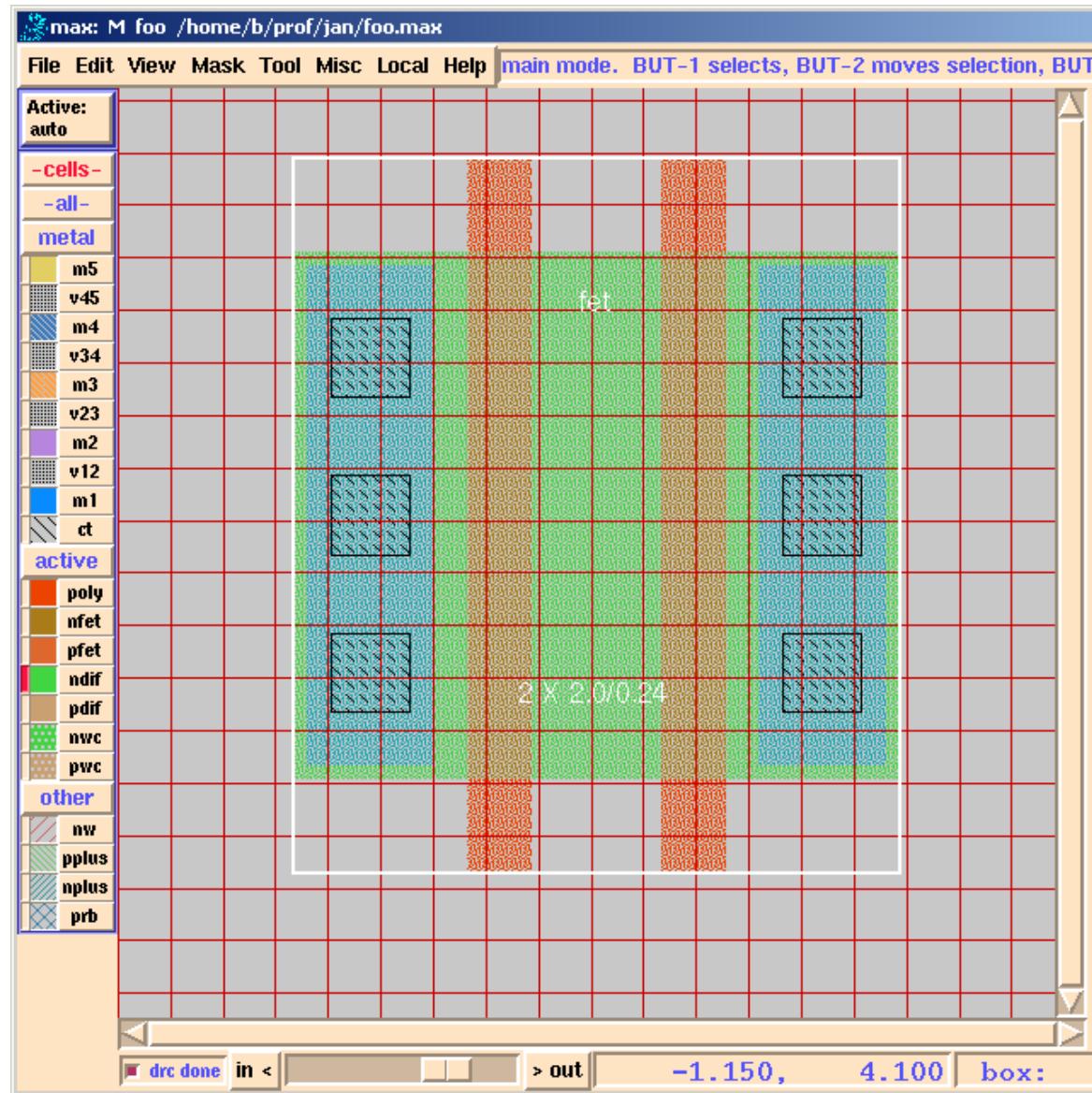


A Modern CMOS Process

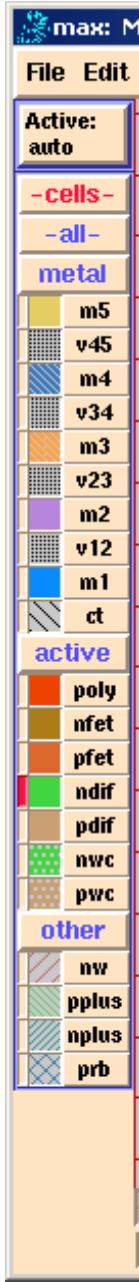
Dual-Well Trench-Isolated CMOS



Layout Editor: max Design Frame

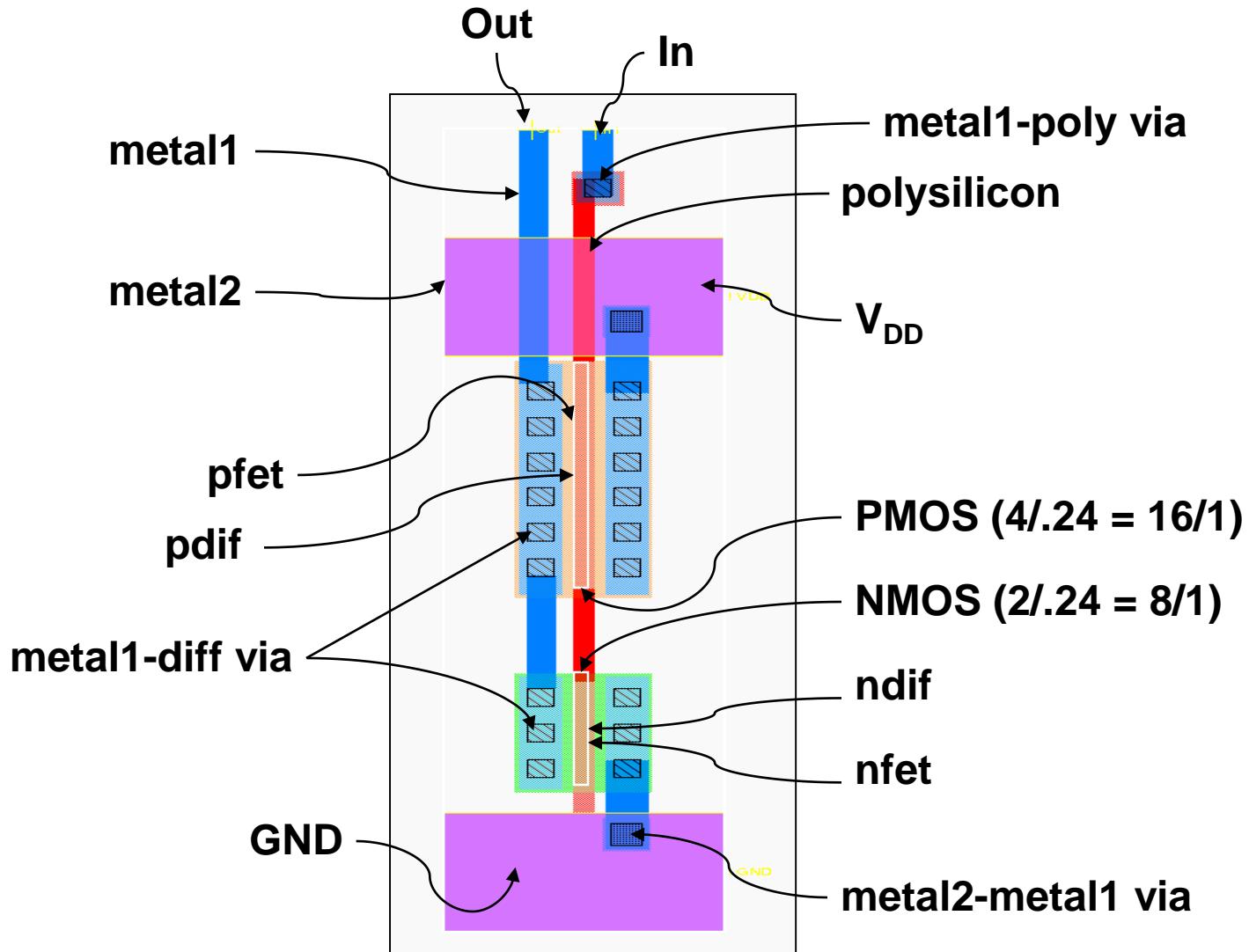


max Layer Representation



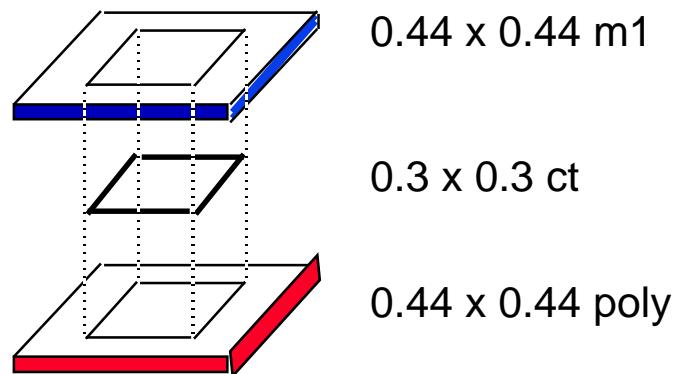
- ❑ Metals (five) and vias/contacts between the interconnect levels
 - Note that **m5** connects only to **m4**, **m4** only to **m3**, etc., and **m1** only to poly, ndif, and pdif
 - Some technologies support “stacked vias”
- ❑ Active – active areas on/in substrate (**poly** gates, transistor channels (**nfet**, **pfet**), source and drain diffusions (**ndif**, **pdif**), and well contacts (**nwc**, **pwc**))
- ❑ Wells (**nw**) and other select areas (**pplus**, **nplus**, **prb**)

CMOS Inverter *max* Layout

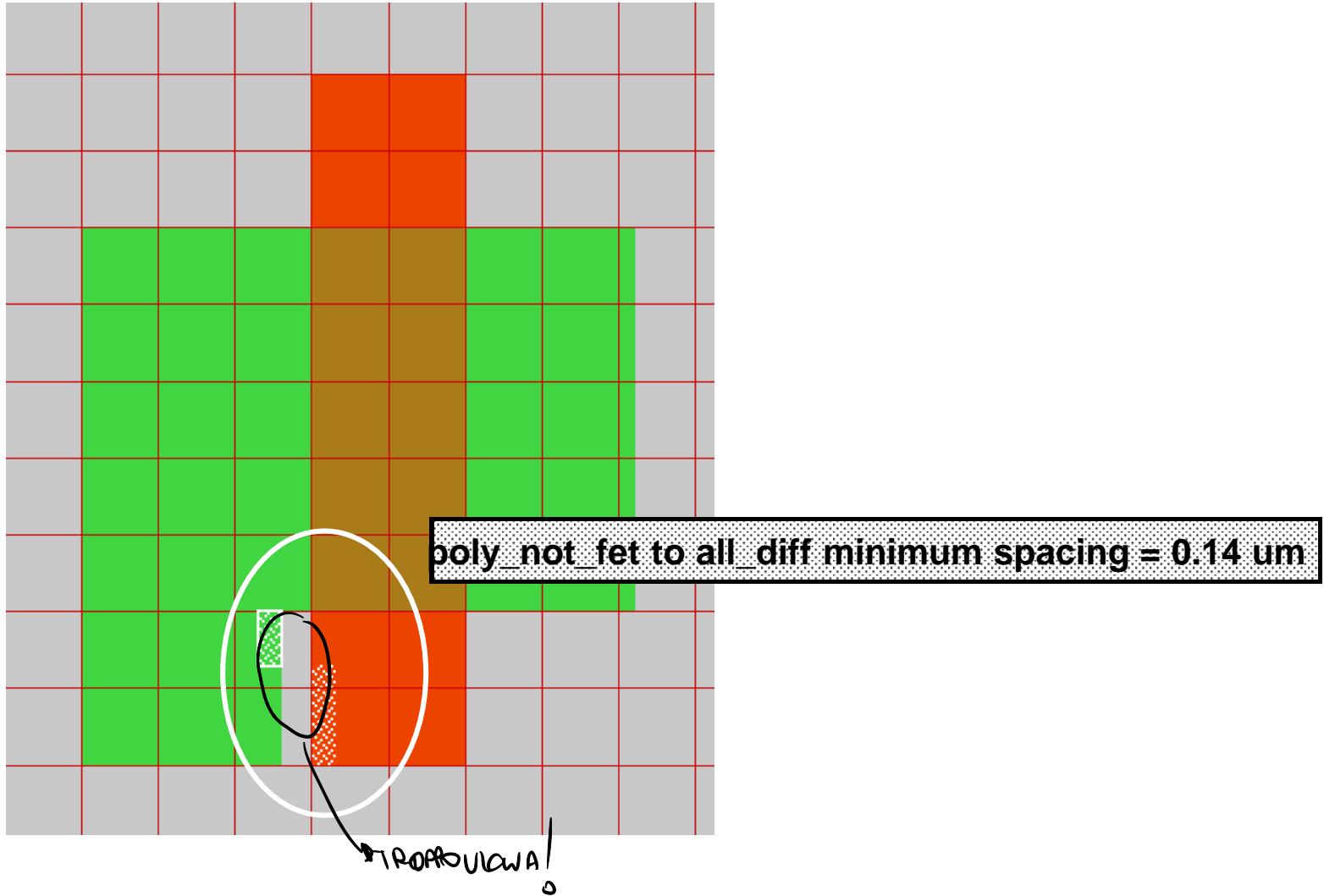


Simplified Layouts in *max*

- ❑ Online design rule checking (DRC)
- ❑ Automatic fet generation (just overlap poly and diffusion and it creates a transistor)
- ❑ Simplified via/contact generation
 - v12, v23, v34, v45
 - ct, nwc, pwc



Design Rule Checker



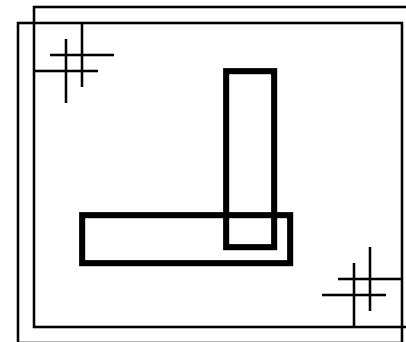
Design Rules

- ❑ Interface between the circuit designer and process engineer
- ❑ Guidelines for constructing process masks
- ❑ Unit dimension: minimum line width
 - scalable design rules: lambda parameter
 - absolute dimensions: **micron rules**
- ❑ Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- ❑ A complete set includes
 - set of layers
 - intra-layer: relations between objects in the same layer
 - inter-layer: relations between objects on different layers

Why Have Design Rules?

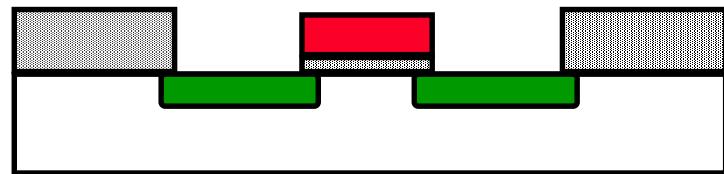
- ❑ To be able to tolerate some level of fabrication errors such as

1. Mask misalignment



2. Dust

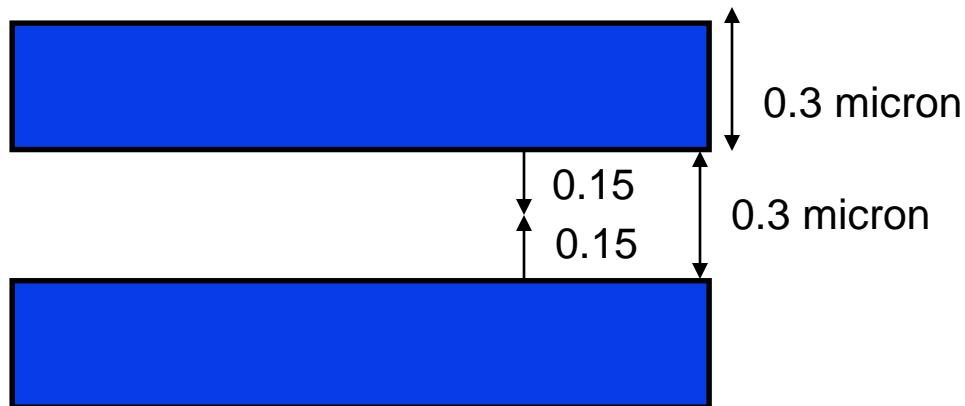
3. Process parameters
(e.g., lateral diffusion)



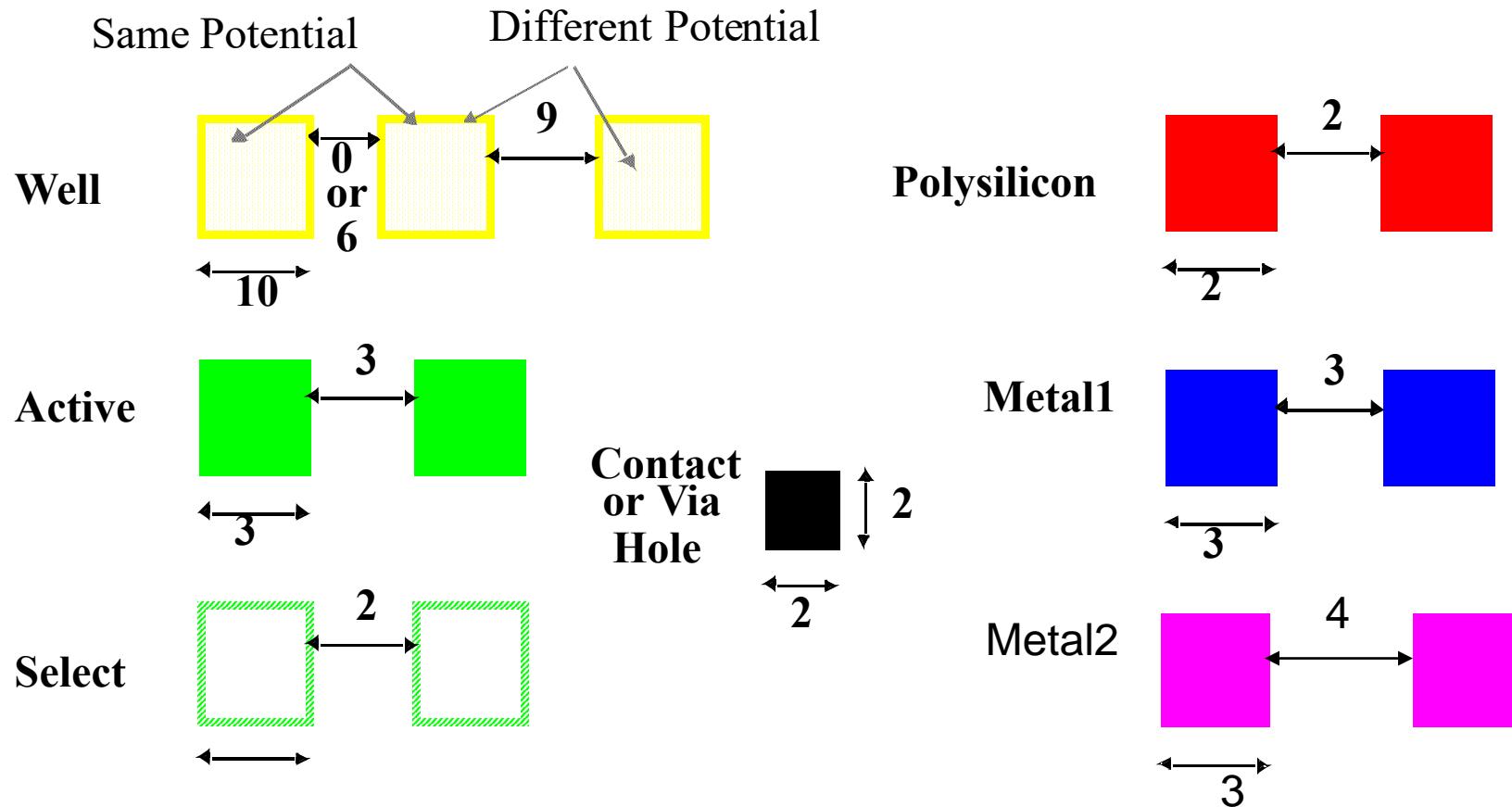
4. Rough surfaces

Intra-Layer Design Rule Origins

- ❑ Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
 - minimum line width is set by the resolution of the patterning process (photolithography)
- ❑ Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fab



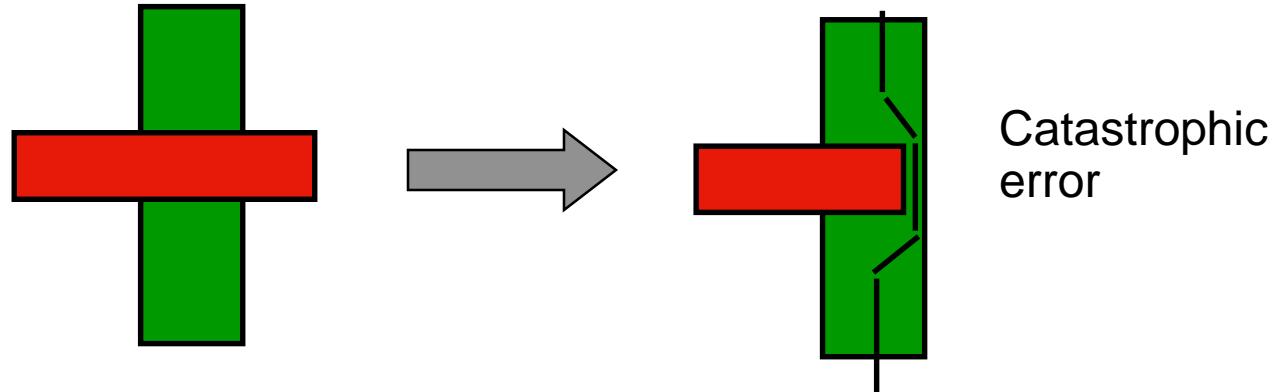
Intra-Layer Design Rules



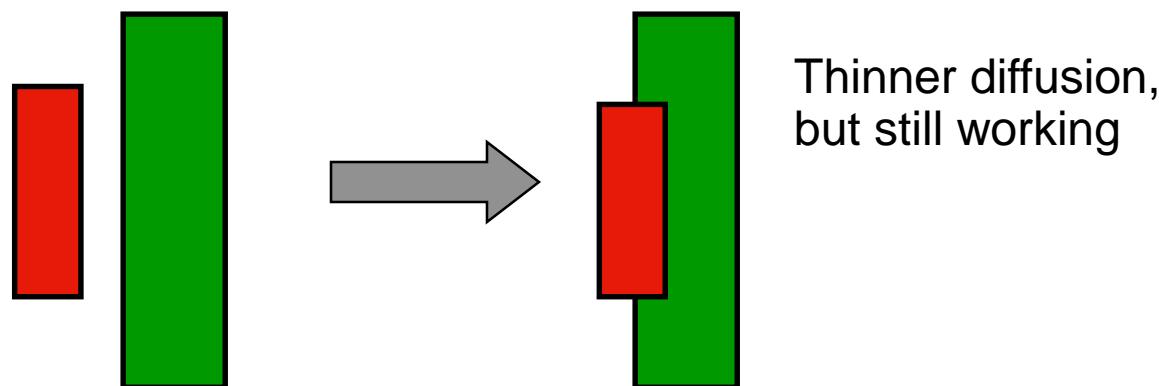
Inter-Layer Design Rule Origins

1. Transistor rules – transistor formed by overlap of active and poly layers

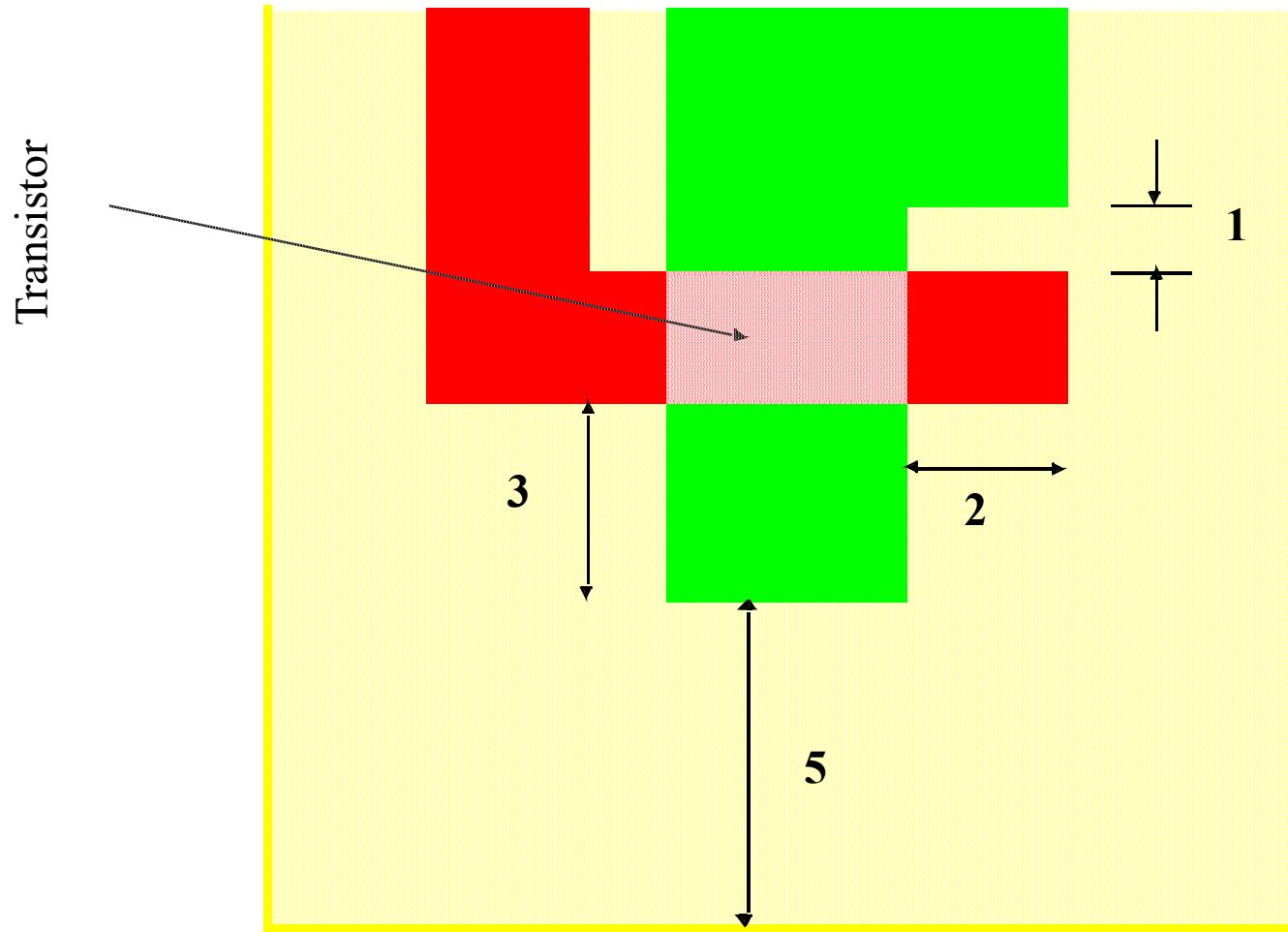
Transistors



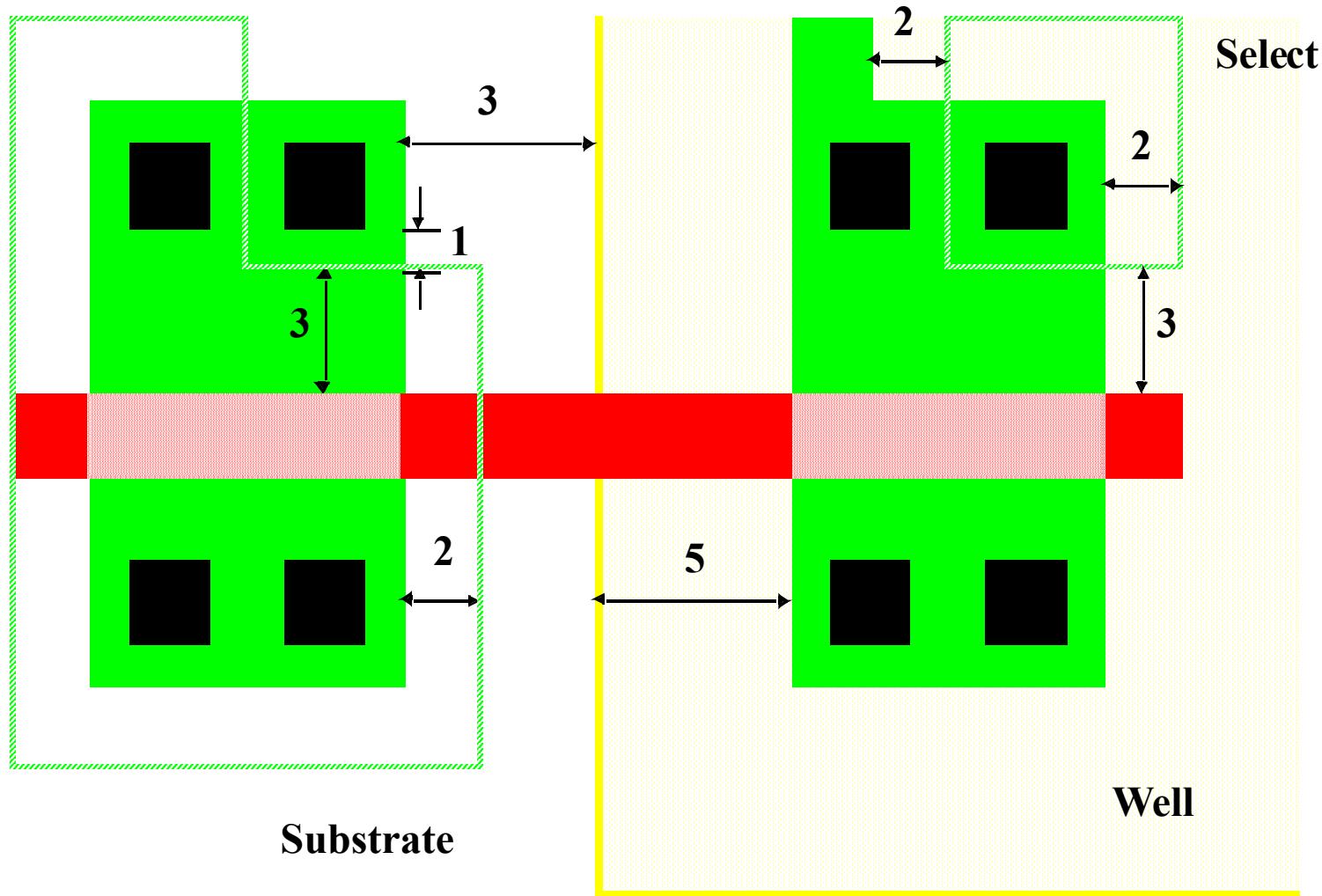
Unrelated Poly & Diffusion



Transistor Layout

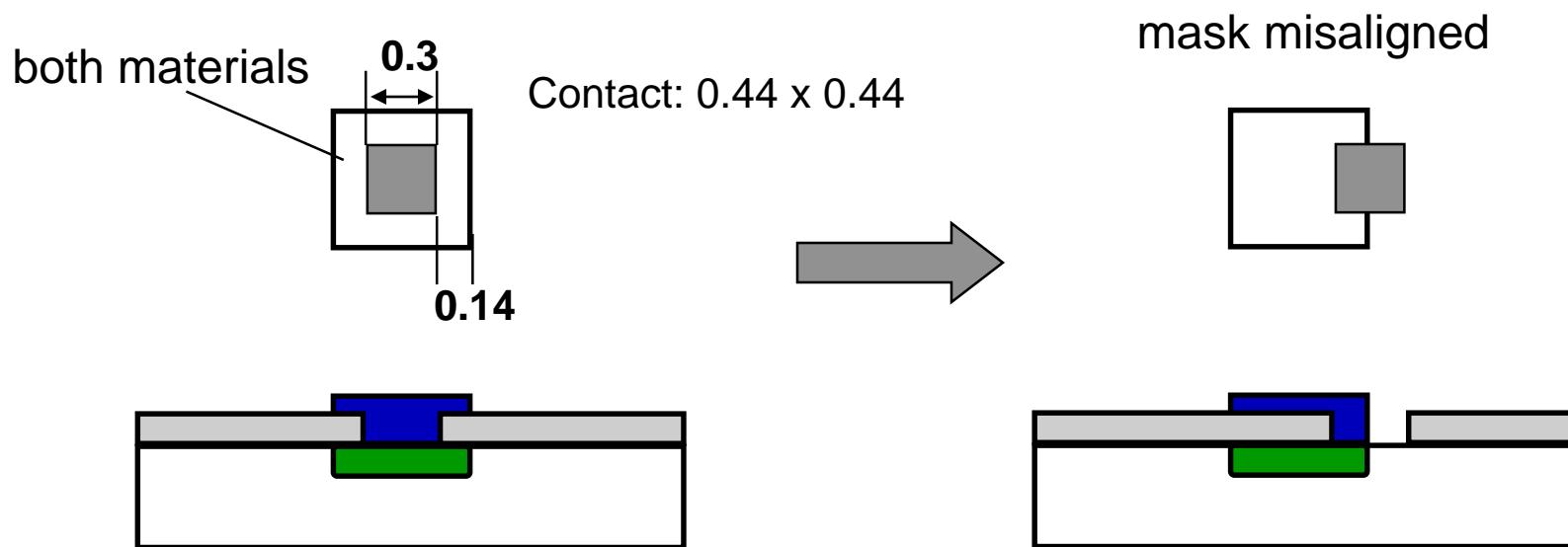
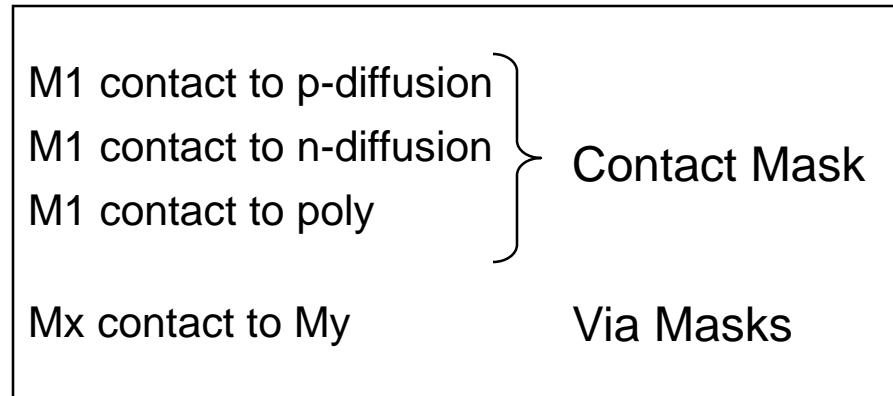


Select Layer

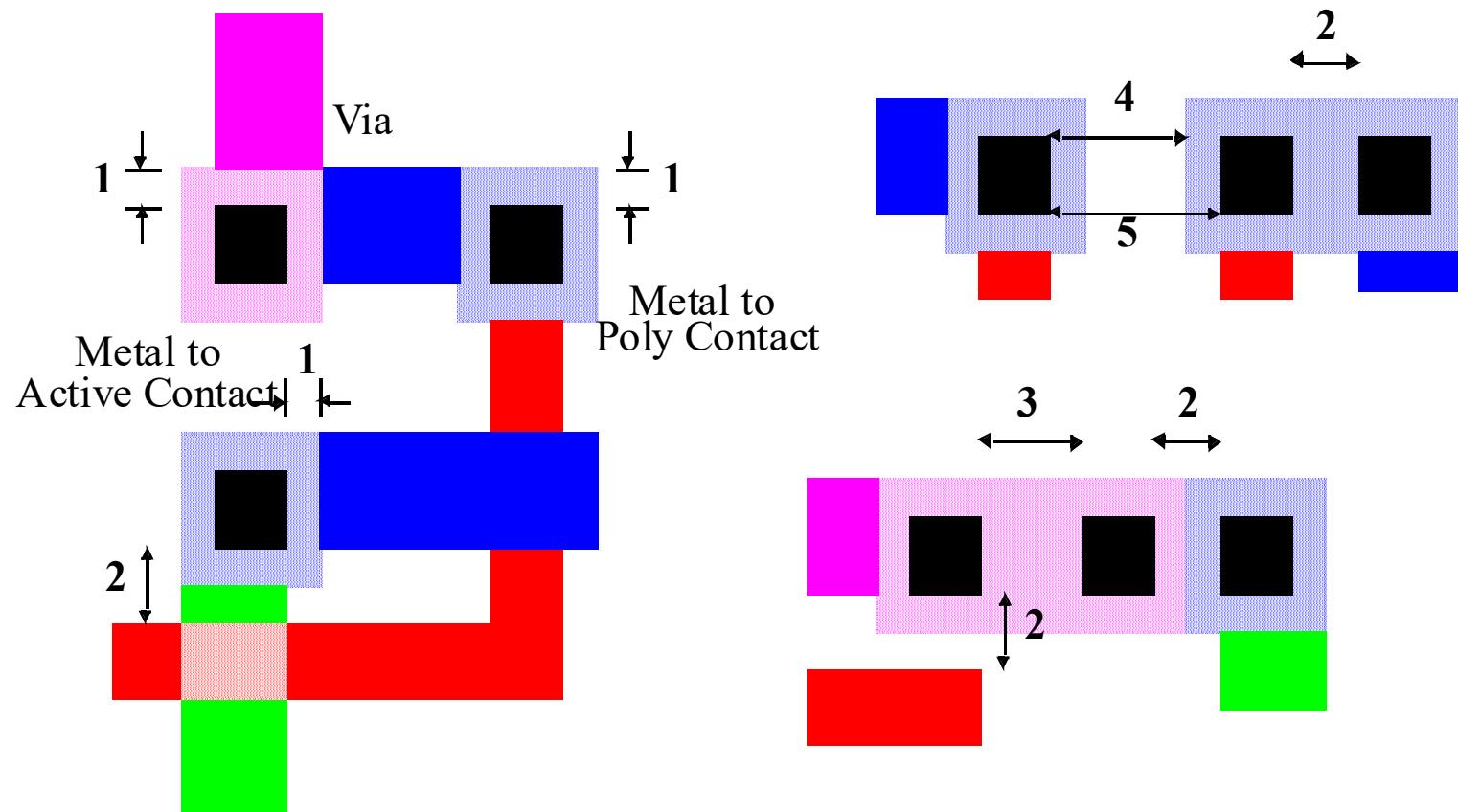


Inter-Layer Design Rule Origins, Con't

2. Contact and via rules



Vias and Contacts



End, Questions ?

- MOS Transistor Switch Model
- Pass Gate
- Inverter
- Review of IC Manufacturing

