

Electronics and Communication Systems

Electronics Systems

Luca Fanucci

Dipartimento di Ingegneria dell'Informazione

Via Caruso 16 - I-56122 - Pisa - Italy

Phone: +39 050 2217 668

Fax: +39 050 2217 522

Mobile: +39 347 5013837

Email: luca.fanucci@unipi.it

Outline

- ❖ **Review**
 - Sync. and Async Sequential Logic
 - Finite State Machine (**MEALY, MOORE, MEALY Rit.**)
- ❖ **Complementary CMOS Logic**
 - Synthesis
 - Dynamic Analysis
 - Examples: NAND, NOR and comparison
 - Stick Diagram
 - Body Effect
 - Standard-cell AMS 0,35 um
- ❖ **Example: Inverter Chain**
 - Driving an high value capacitor
 - Dynamic Analysis
 - Power-Speed Trade-Off
- ❖ **Example: Pass Transistor Chain**
 - Dynamic Analysis
 - Area – Speed Trade-Off

Logic

❖ Combinational Logic

- Output are a pure function of the present input
 - only

❖ Sequential Logic

- Output depends not only on the present input
 - but also on the history of the input

Sequential Logic

- ❖ **MEMORY concept**
- ❖ **Asynchronous sequential**
 - Outputs of the circuit change directly in response to changes in inputs
- ❖ **Synchronous sequential**
 - Outputs of the circuit change only with the rising (falling) edge of a reference control signal, named **clock**

Asynchronous sequential

- ★ Ripple Design
- ★ Pro
 - High Speed
 - Low Power
- ★ Cont
 - Race Conditions
 - Difficult Design

Synchronous sequential

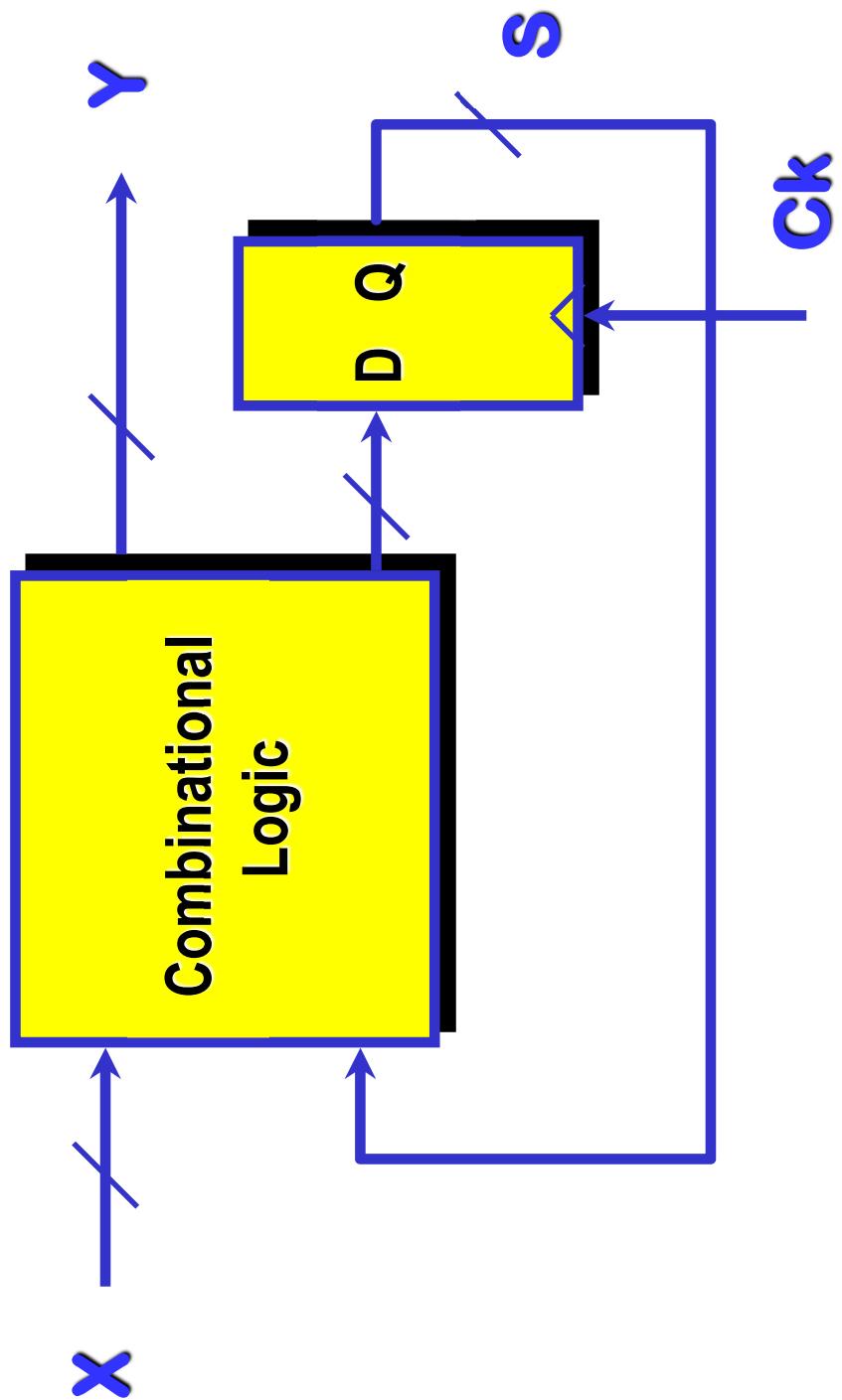
- ★ Clocked Design
- ★ Pro
 - Easy Design
 - Robust Design
- ★ Cont
 - High complexity
 - High Power Consumption
 - «Reduced» Speed

MEALY Machine1/2

- ❖ **Output values are determined both by its current state and the current inputs**
- ❖ **Asynchronous Logic**
- ❖ **Based on one combinational Logic**

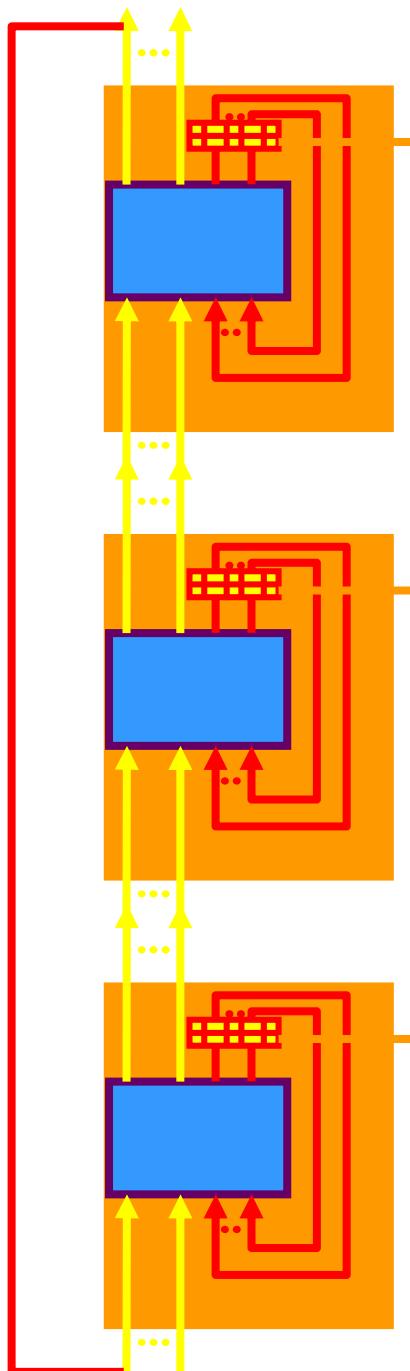
MEALY Machine 2/2

★ Block Diagram



Notes

- ❖ Outputs are asynchronous
- ❖ Critical to have a cascaded of MEALY machines due to hidden asynchronous logic

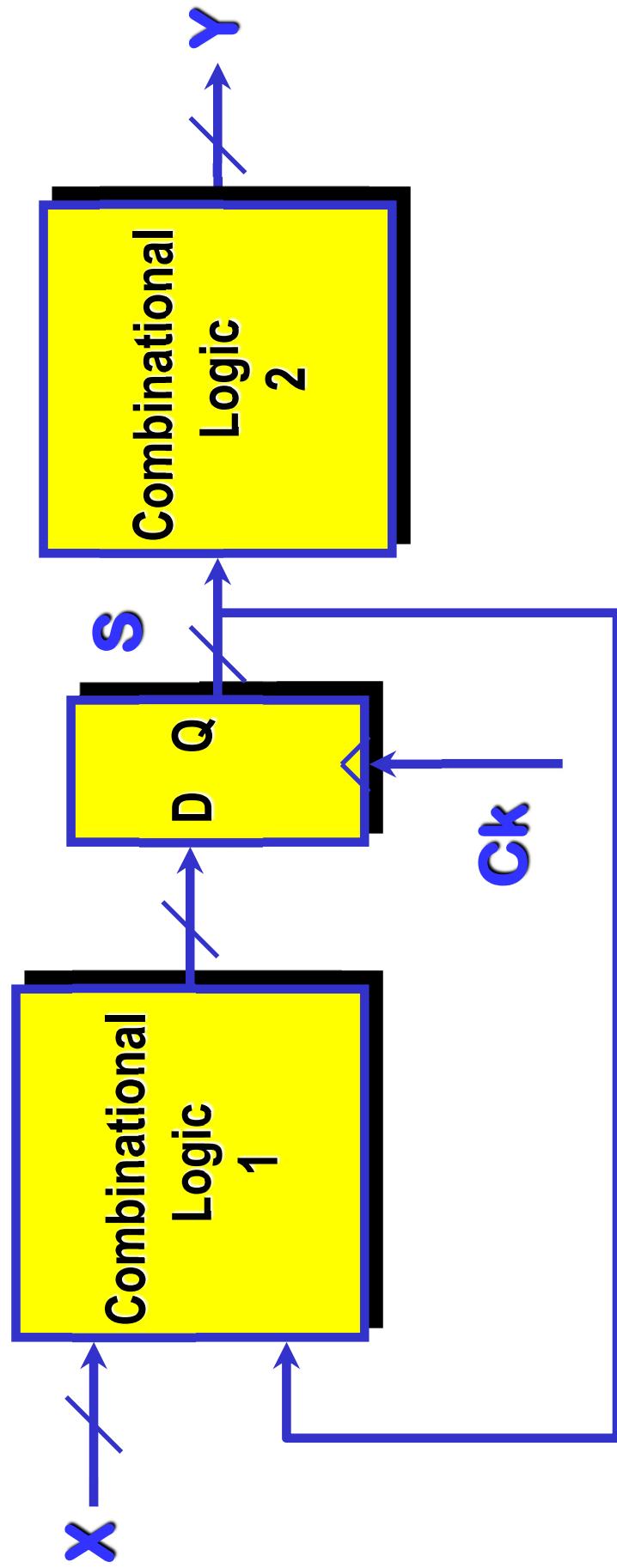


MOORE Machine 1/2

- ❖ output values are determined solely by its current state
- ❖ Synchronous Logic
- ❖ Required **two** Combinational Logics
- ❖ Never Unstable

MOORE Machine 2/2

* Block diagram

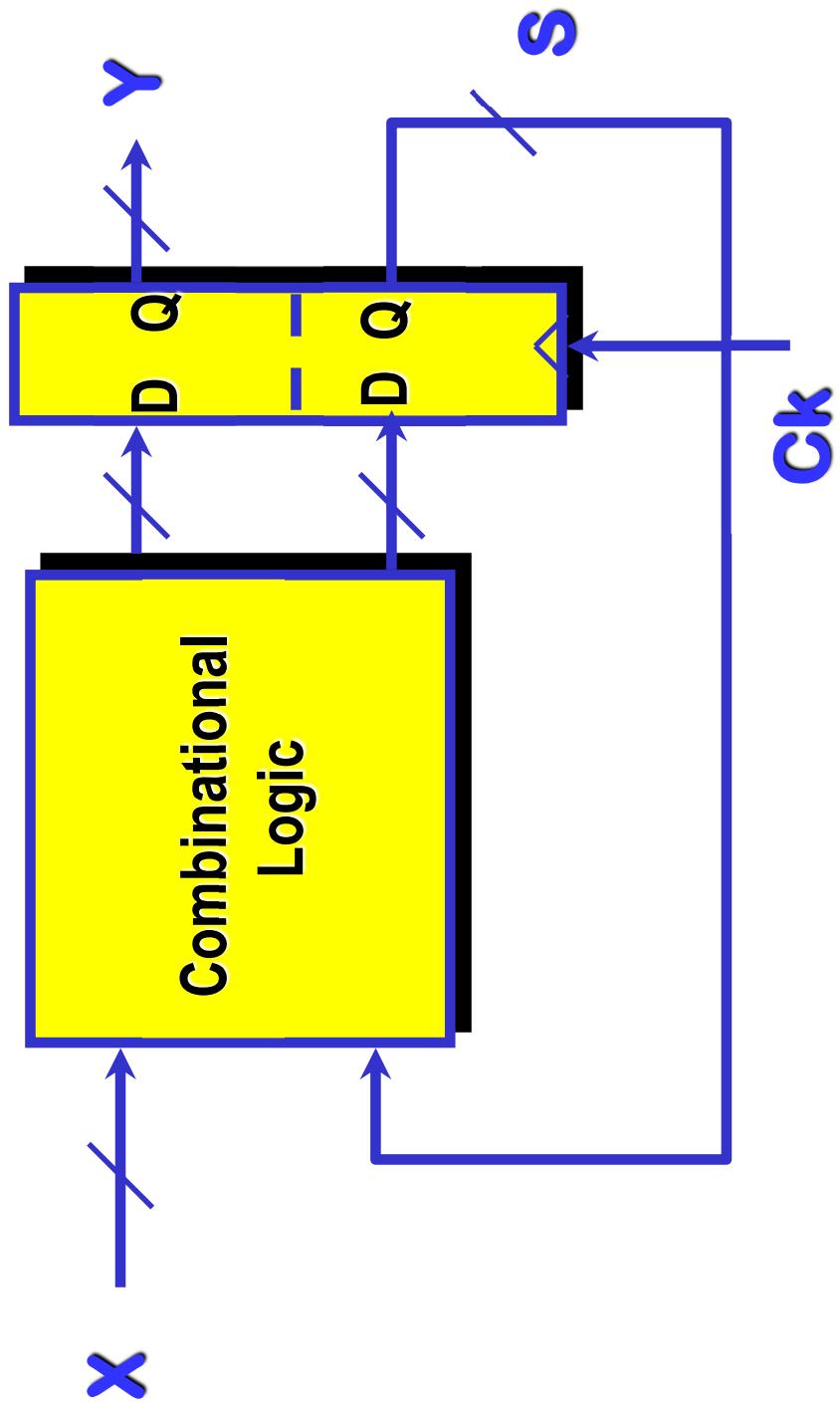


Modified MEALY machine 1/2

- ❖ Output are synchronized to solve stability problem
- ❖ Output are delayed w.r.t MEALY
- ❖ Synchronous Logic
- ❖ It is a MOORE Machine
- ❖ Sometimes required one internal state less than MOORE Machine

Modified MEALY machine 2/2

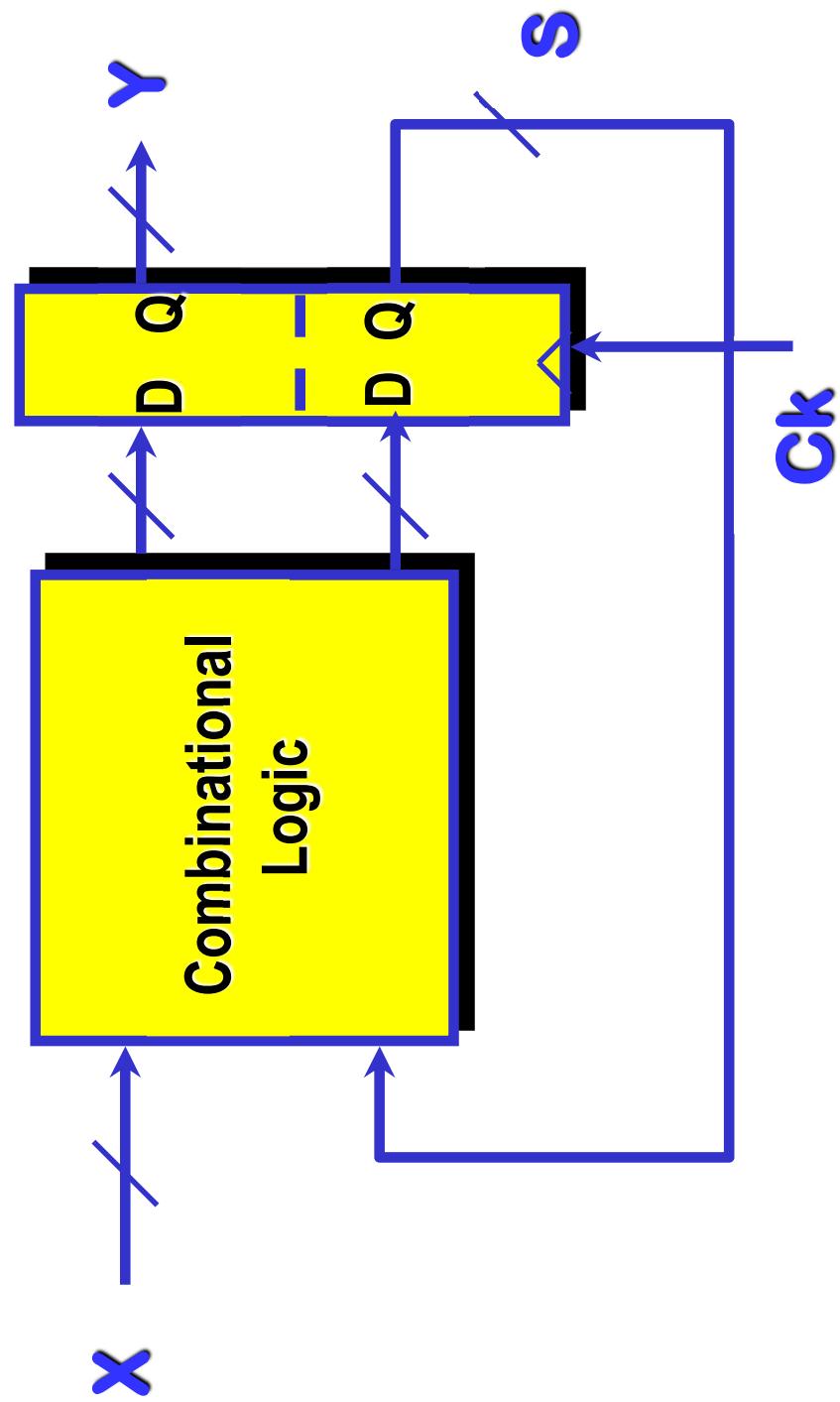
★ Block Diagram



Finite State Machine: Basic Elements

Combinational Logic

Memory Element (Flip Flop D edge triggered)



Finite State Machine: Basic Elements

❖ How to build them ?

- Static Logic (hard node)
- Dynamic Logic (soft node)

Hard-Node (Static Logic)

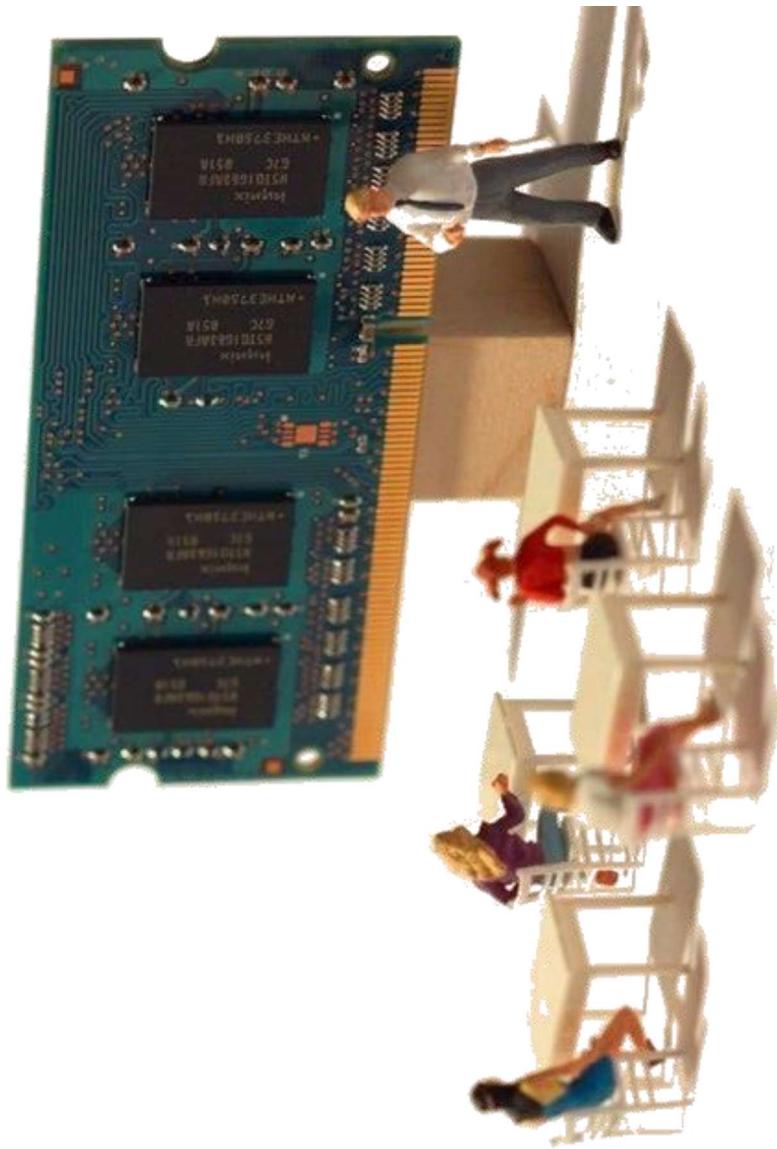
- ❖ Have positive feedback (regeneration) with an internal connection between the output and the input. Storage is performed through circuit topology
- ❖ Preserve state as long as the power is on
- ❖ Useful when updates are infrequent

Soft Node (Dynamic Logic)

- ❖ Store state on parasitic capacitors
- ❖ Only hold state for short periods of time
- ❖ Require periodic refresh
- ❖ Usually simpler, so higher speed and lower power

End **Review**, Questions ?

- Sync. and Async Sequential Logic
- Finite State Machine (MEALY, MOORE, MEALY Ritt.)



Outline

❖ Review

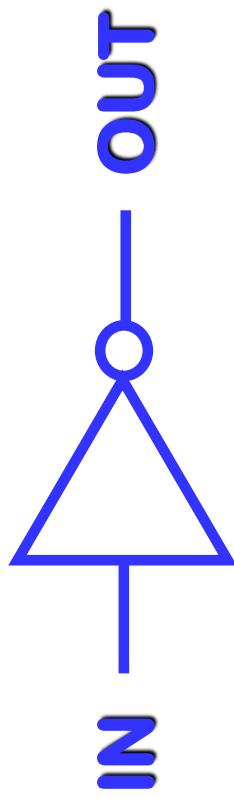
- Sync. and Async Sequential Logic
- Finite State Machine (MEALY, MOORE, MEALY Rit.)
- ❖ Complementary CMOS Logic

- Synthesis
- Dynamic Analysis
- Examples: NAND, NOR and comparison
- Stick Diagram
- Body Effect
- Standard-cell AMS 0,35 um
- ❖ Example: Inverter Chain
 - Driving an high value capacitor
 - Dynamic Analysis
 - Power-Speed Trade-Off
- ❖ Example: Pass Transistor Chain
 - Dynamic Analysis
 - Area – Speed Trade-Off

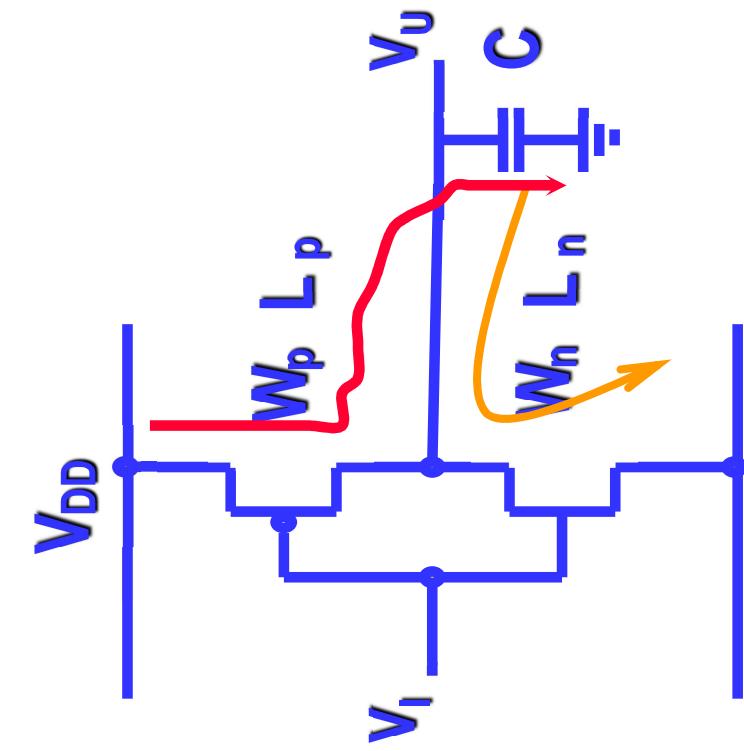
INVERTER

- * Implementation of the logic NOT Function
- * Truth Table
- * Logic Symbol

IN	OUT
0	1
1	0



Propagation Delay



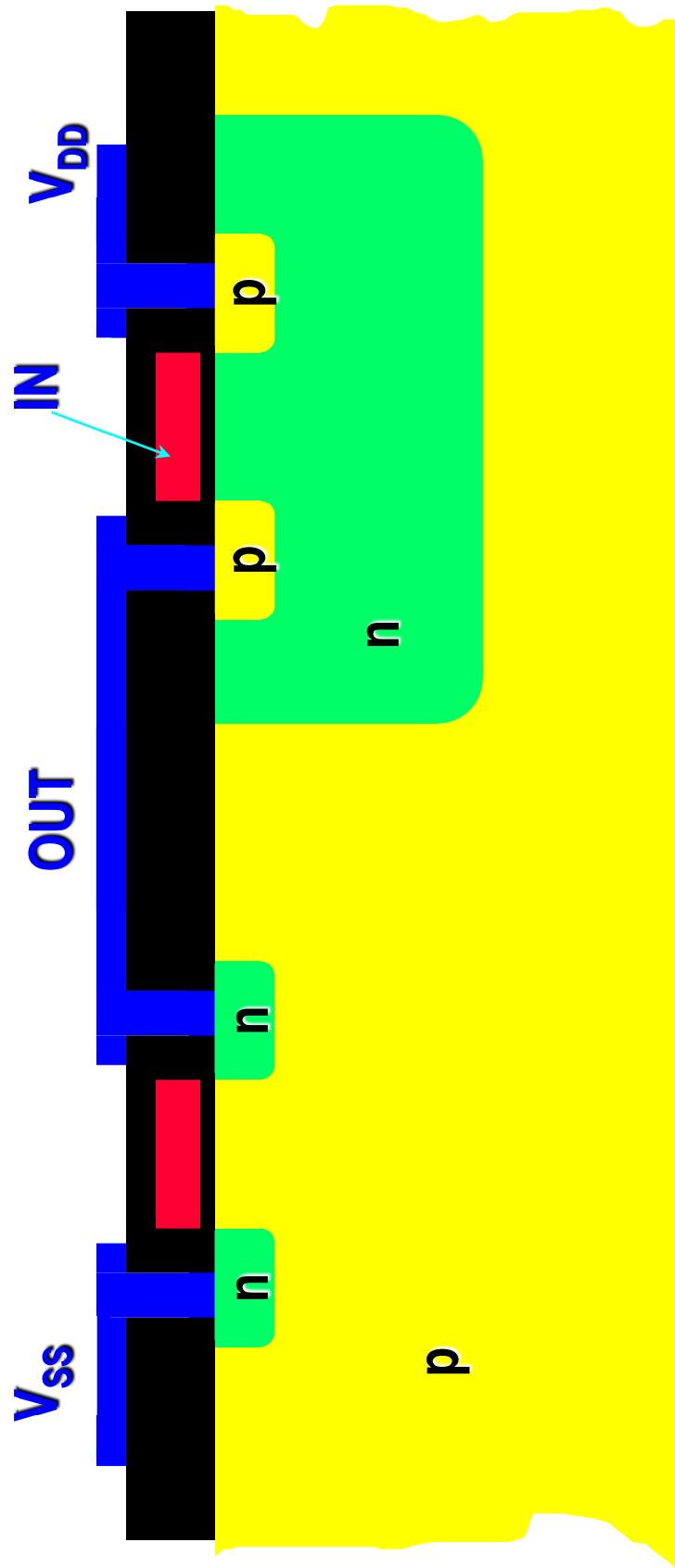
$$t_{pHL} \propto \frac{KC}{\beta_n} \frac{1}{V_{DD} - V_{Tn}}$$

$$t_{pLH} \propto \frac{KC}{\beta_p} \frac{1}{V_{DD} + V_{Tp}}$$

$$\beta_n = \mu_n C_{ox} \frac{W_n}{L_n} \quad \beta_p = \mu_p C_{ox} \frac{W_p}{L_p}$$

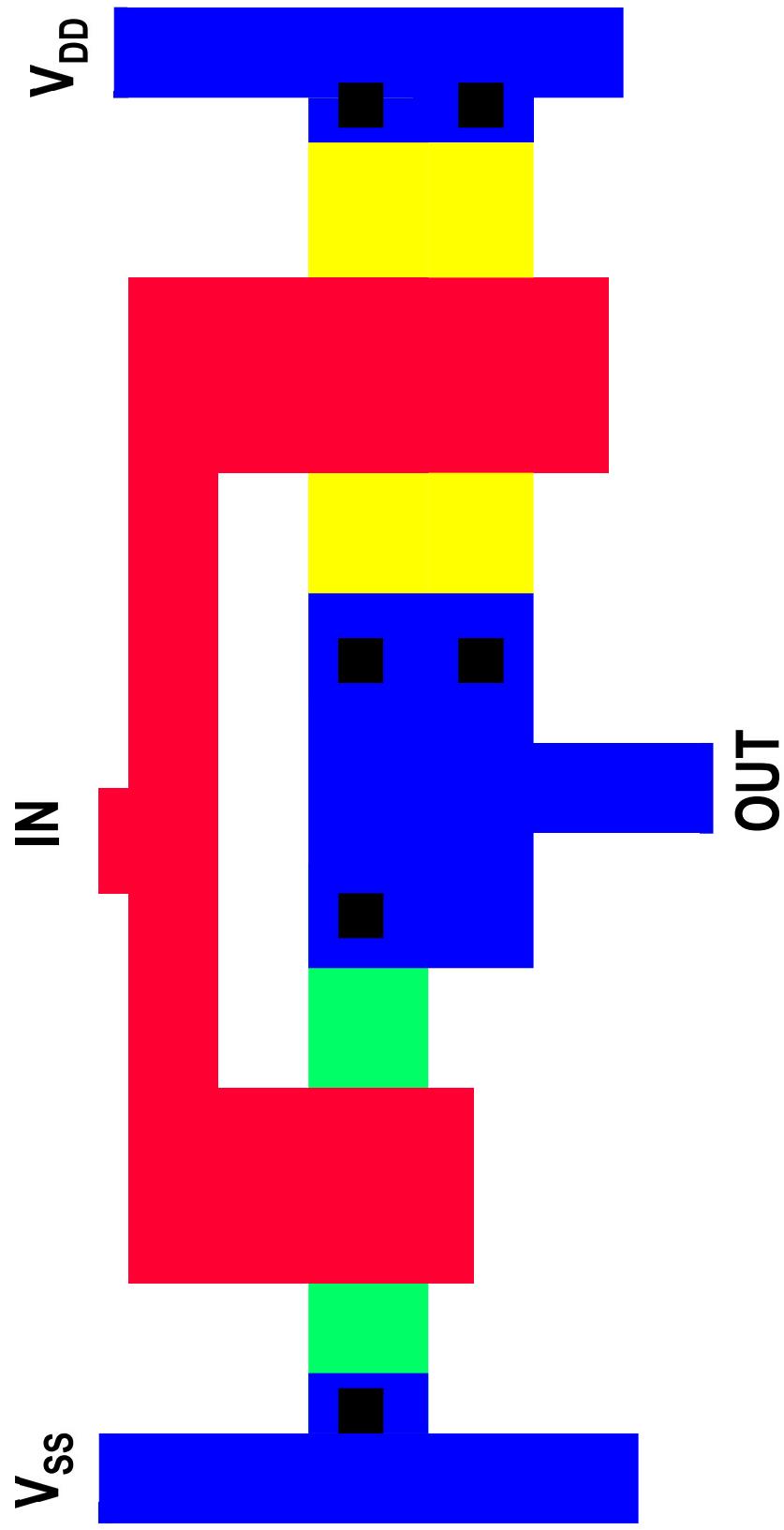
INVERTER Lay-out 1

► Cross Section for “n” well process



INVERTER Lay-out 2

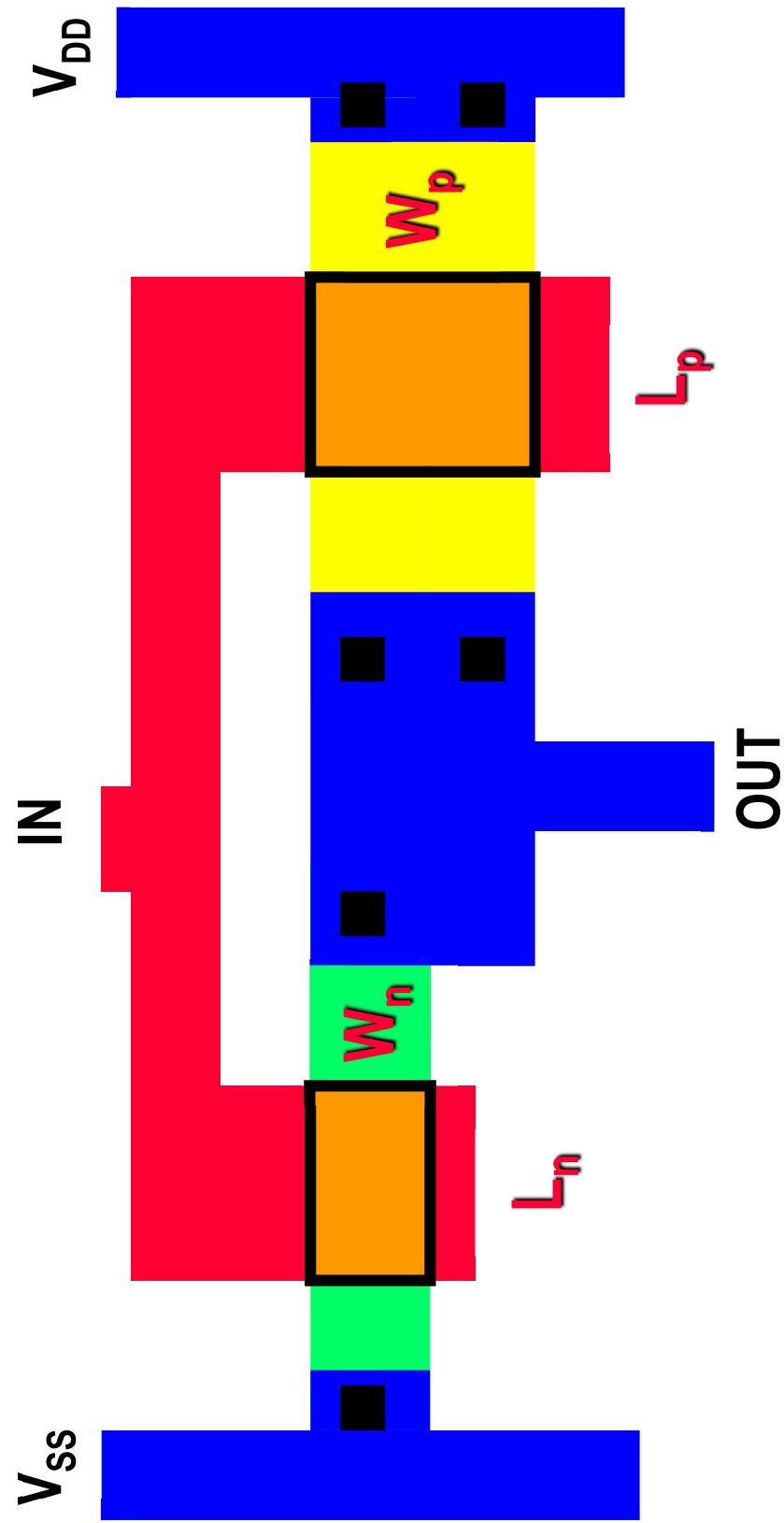
★ Top view



INVERTER Lay-out 2

$$A \sim W_n L_n + W_p L_p$$

★ Top view

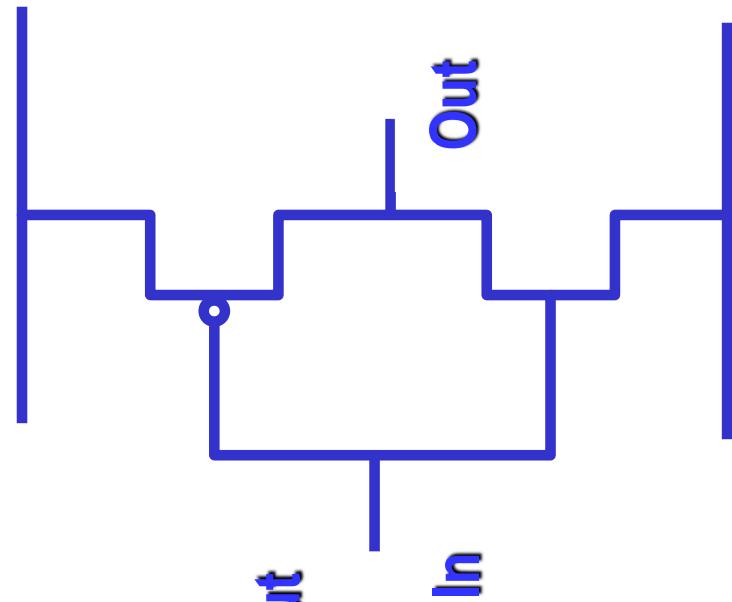
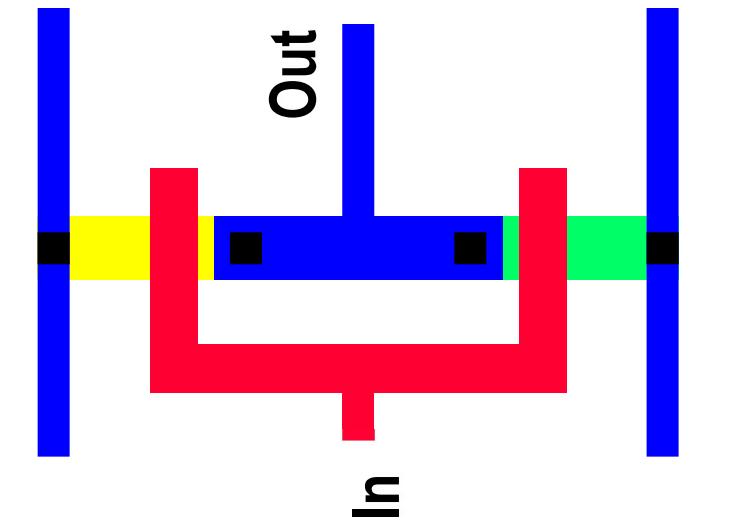


Stick Diagram

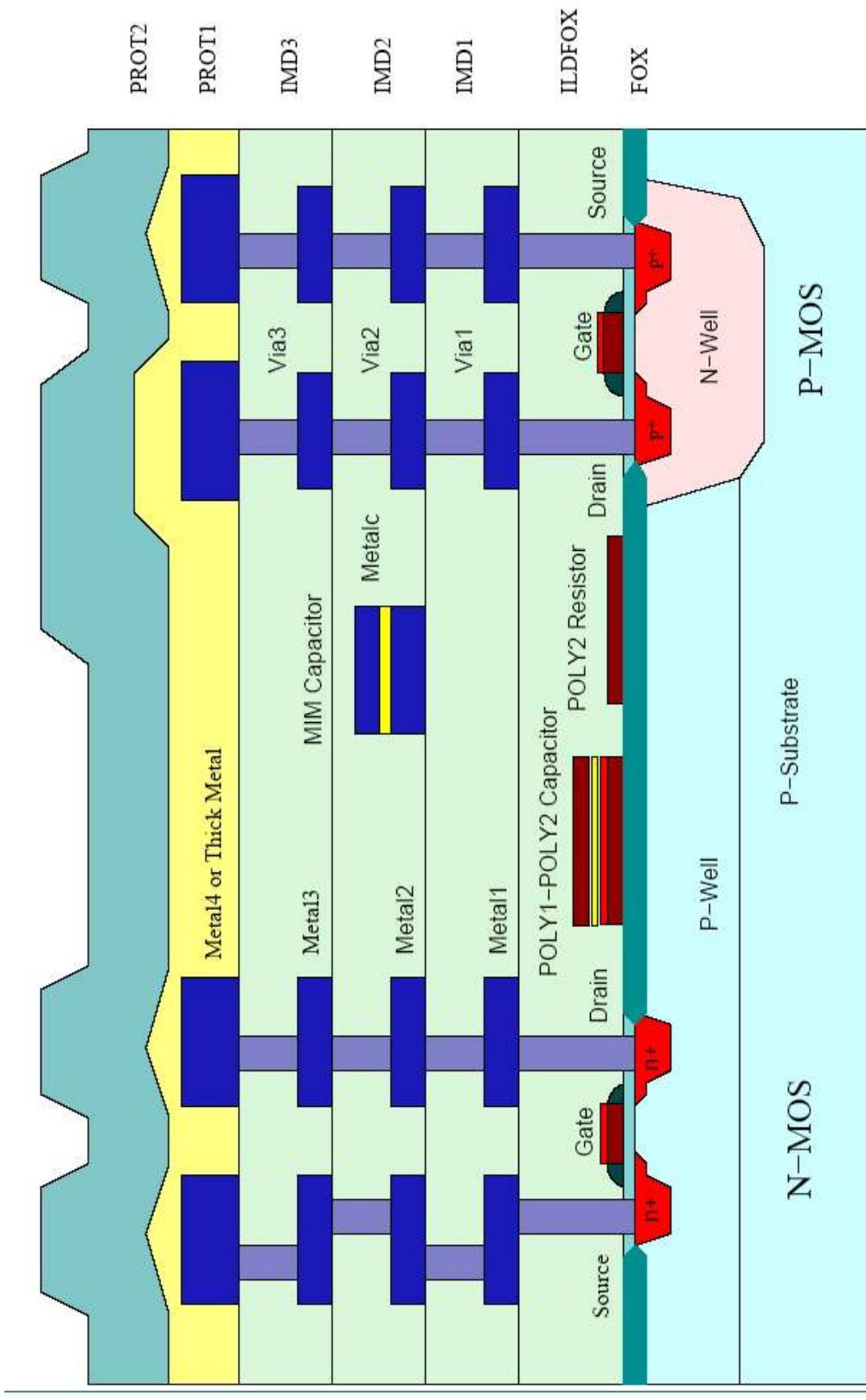
♦ Logic Symbol

Circuit

Lay-out



Wafer Cross-Section Austriamicrosystems, 0,35 um CMOS



Austriamicrosystems, 0,35 um CMOS Technology Overview

Process technology specifications	units	C35B3C3	C35B4C3
Drawn MOS Channel Length	μm	0,35	0,35
Operating Voltage	V	2.5 - 3.6	10 - 5.5
Number of Masks	#	14	20
Number of Masking layers	#	19	24
Number of Metal Layers	#	3	4
Number of Poly Layers	#	2	p
Substrate Type			
Diffusion Pitch	μm	0,9	0,9
Metal1/2/3/4 Pitch	μm	0.95 / 1.1 / 1.1 / 1.2	1.05 / 1.2 / 1.2 / 1.3
Metal1/2/3/4 conacted Pitch	μm		
Poly1 Pitch	μm	0,8	
High Resistive Poly	kOhm/#	-	1,2
Poly1/Poly2 Precision Caps	fF/μm ²	0,9	
N/PMOS Channel Length	μm	0.30/0.30	
N/PMOS Saturation Current	μA/μm	520 / 240	

Standard-Cell Austria microsystems, 0,35 µm CMOS Technology Library



0.35µm CMOS

Digital Standard Cell Databook

Inverter

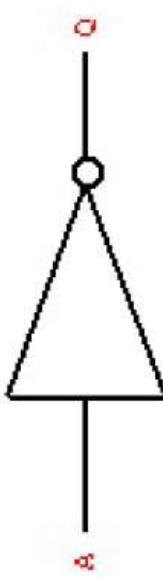
dim

www.am5.com

INWXX1

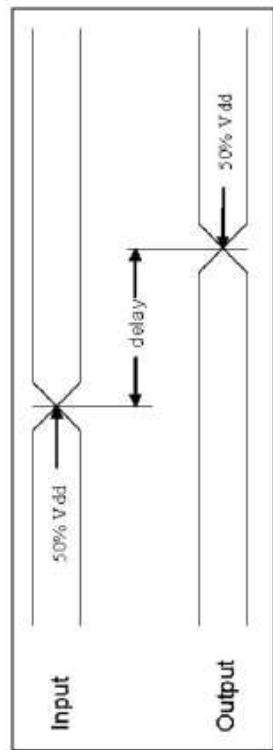
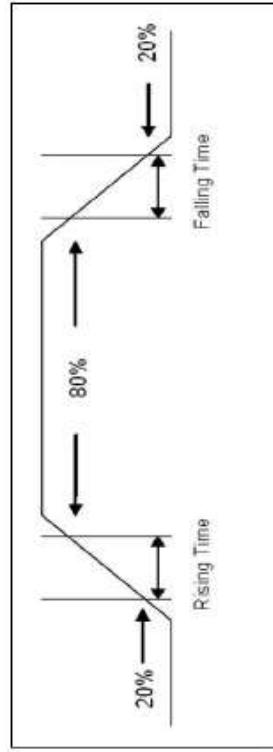
Conditions for characterization library **c35_CORELIBD_BC**, corner **c35_CORELIBD_BC_best**: $V_{dd} = 3.63V$, $T_j = -50.0$ deg. C . Output transition is defined from 20% to 80% (rising) and from 80% to 20% (falling) output voltage. Propagation delay is measured from 50% (input rise) or 50% (input fall) to 50% (output rise) or 50% (output fall).

Strength 1	Cell Area 29.120 μm^2	Equation Q = "IA"	Type Combinational	Input A	Output Q
------------	----------------------------------	-------------------	--------------------	---------	----------



State Table	A	Q
	L	H
	H	L

Capacitance [fF] 2.8210 A



Propagation Delay

Transition Time

Inverter

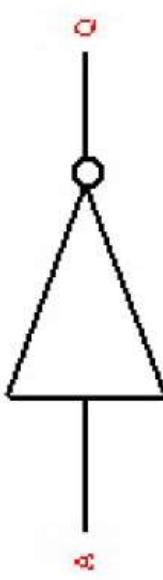
dim

INWIX

WWW.AMS.COM

Conditions for characterization library c35_CORELIBD_BC, corner c35_CORELIBD_BC_best: Vdd= 3.63V, Tj= -50.0 deg. C . Output transition is defined from 20% to 80% (rising) and from 80% to 20% (falling) output voltage. Propagation delay is measured from 50% (input rise) or 50% (input fall) to 50% (output rise) or 50% (output fall).

Strength	1
Cell Area	29.120 μm^2
Equation	$Q = "IA"$
Type	Combinational
Input	A
Output	Q



State Table	A	Q
	L	H
	H	L

Capacitance [fF] A 2.8210

Propagation Delay [ns]					
Input Transition [ns]		0.01		4.00	
Load Capacitance [fF]		5.00	100.00	5.00	100.00
A to Q	fall	0.04	0.41	-0.36	0.63
	rise	0.06	0.67	0.83	1.88

Output Transition [ns]					
Input Transition [ns]	0.01		4.00		
Load Capacitance [fF]	5.00	100.00	5.00	100.00	
A to Q	fall	0.04	0.54	0.70	1.43
	rise	0.08	1.03	0.62	1.58

Inverter

dim

www.ams.com

INWX1

Conditions for characterization library c35 **CORELIBD_BC**, corner c35 **CORELIBD_BC_best**: $Vdd = 3.63V$, $Tj = -50.0\text{ deg. C}$. Output transition is defined from 20% to 80% (rising) and from 80% to 20% (falling) output voltage. Propagation delay is measured from 50% (input rise) or 50% (input fall) to 50% (output rise) or 50% (output fall).

Strength	1
Cell Area	29.120 μm^2
Equation	$Q = "!A"$
Type	Combinational
Input	A
Output	Q



State Table	A	Q
	L	H
	H	L

Capacitance [fF] A 2.8210

Leakage [pW]
0.26

Dynamic Power Consumption [nW/MHz]					
Input Transition [ns]	0.01	0.01	0.01	4.00	4.00
Load Capacitance [fF]	5.00	100.00	100.00	5.00	100.00
A to Q	fall	1.93	2.35	516.63	510.09
	rise	38.82	40.07	813.89	712.95

Inverter

am
uT

INVX1

www.ams.com

Conditions for characterization library c35_CORELIBD_BC, corner c35_CORELIBD_BC best: Vdd= 3.63V, Tj= -50.0 deg. C.

Output transition is defined from 20% to 80% (rising) and from 80% to 20% (falling) output voltage.

Propagation delay is measured from 50% (input rise) or 50% (input fall) to 50% (output rise) or 50% (output fall).

Strength	1
Cell Area	29.120 μm^2
Equation	$Q = \text{!}A$
Type	Combinational
Input	A
Output	Q



State Table	
A	Q
L	H
H	L

Capacitance [fF]	
A	2.8210

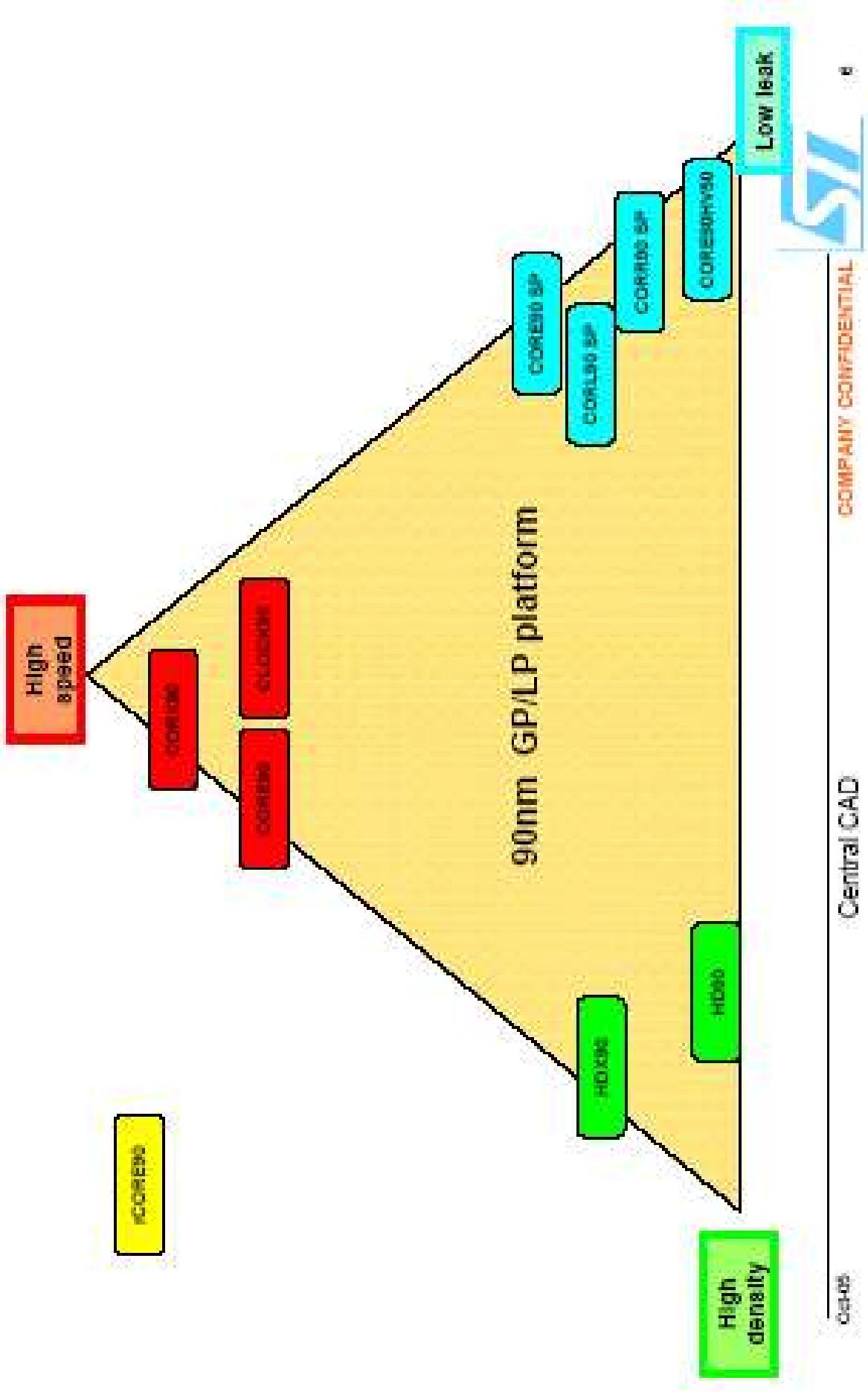
Dynamic Power Consumption [nW/MHz]	
Input Transition [ns]	0.01
Load Capacitance [fF]	5.00
A to Q	4.00
fall	1.93
rise	5.00
	100.00
	5.00
	100.00
	516.63
	510.09
	813.89
	712.95

Leakage [pW]	
A	0.26

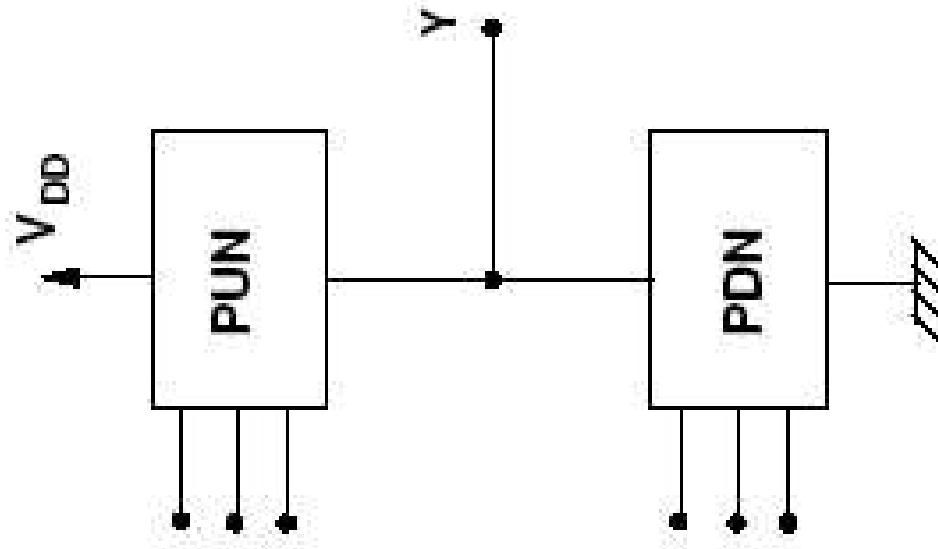
CMOS Technology Corners

BEST	TYPICAL	WORST
-40 - 0 °C	25 °C	85 - 125 °C
1,1*VDD	VDD	0,9*VDD
Process	FAST	SLOW

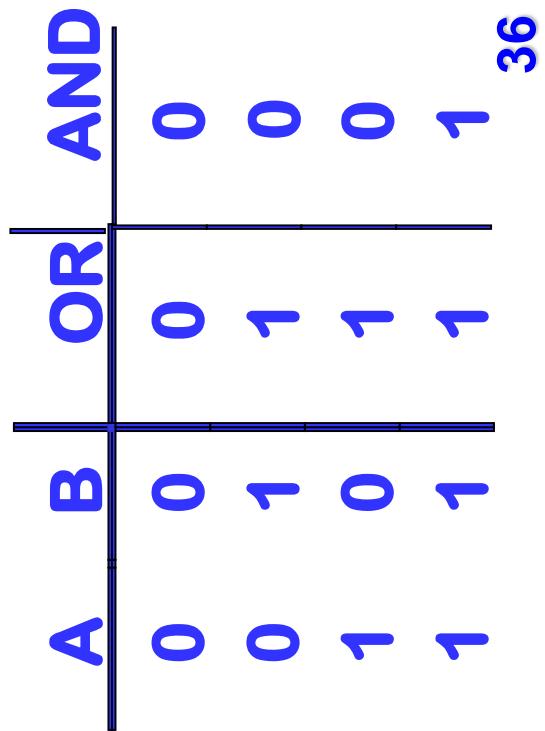
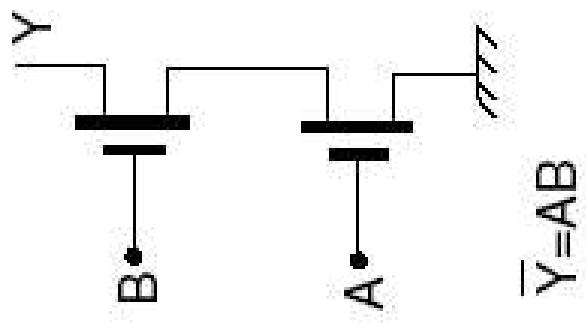
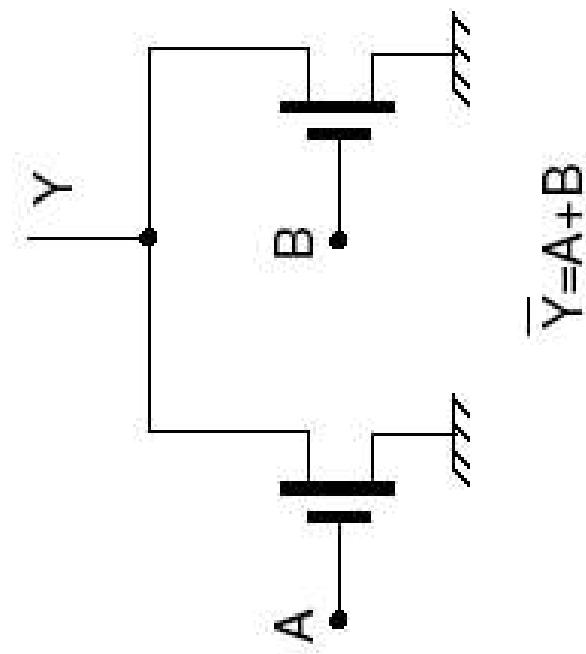
90nm Standard cells Libraries



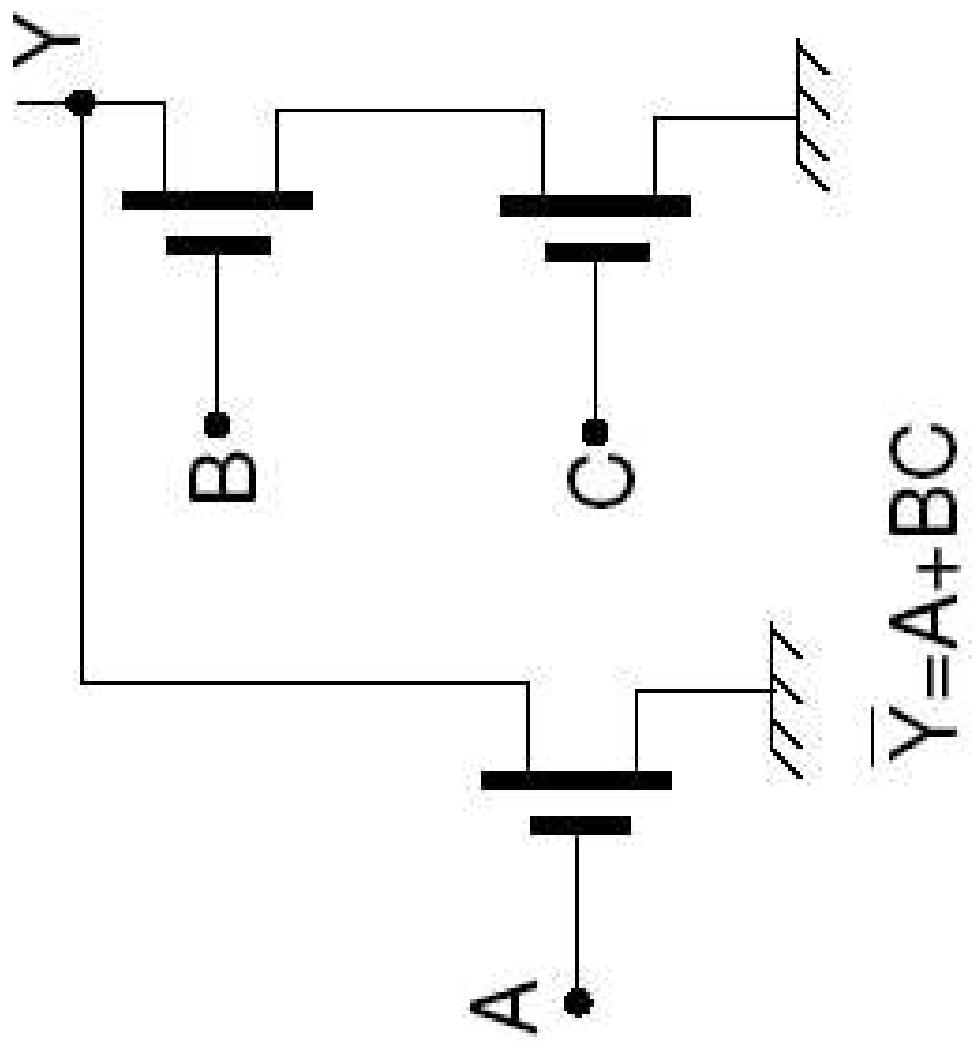
Complementary CMOS



PDN



PDN

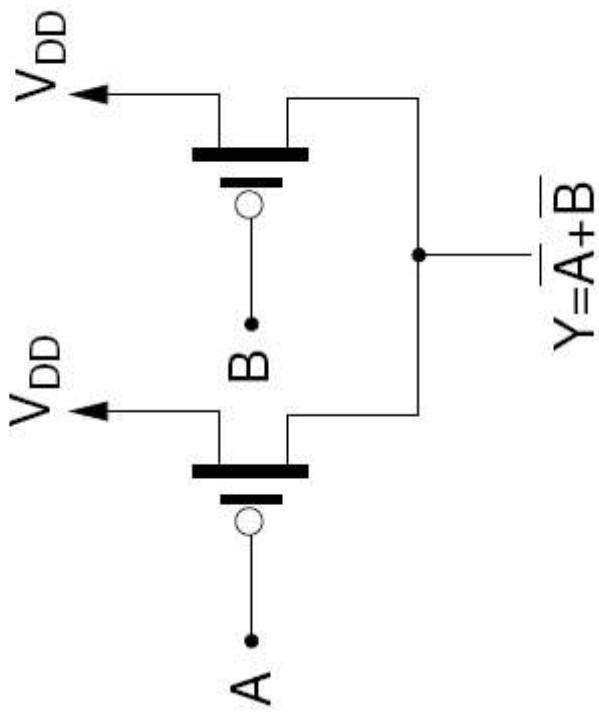
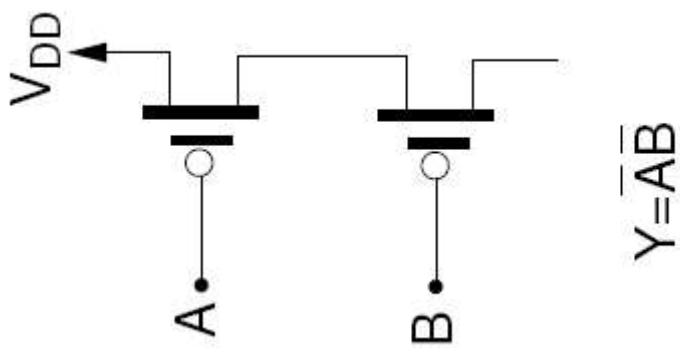


PUN

★ PUN is DUAL of PDN

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$



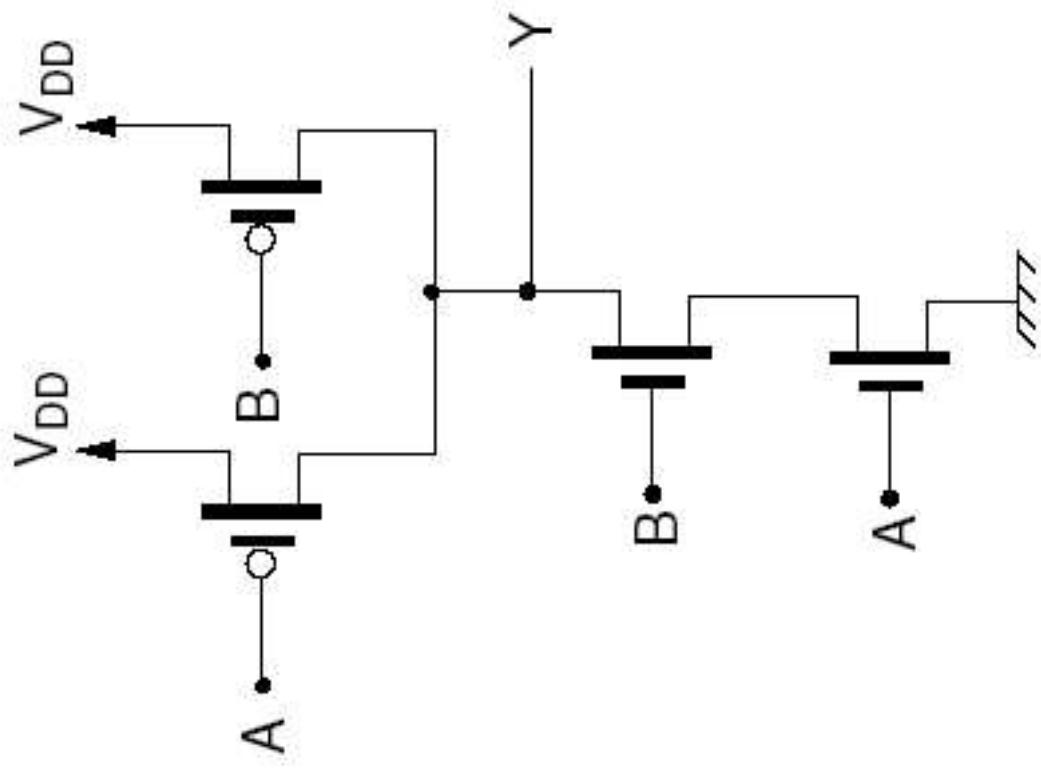
A	B	NAND	
0	0	1	
0	1	1	
1	0	1	0
1	1	0	

PDN / PUN

- ❖ $\bar{Y} = f_{PDN}(A, B)$
- ❖ $Y = f_{PUN}(\bar{A}, \bar{B})$

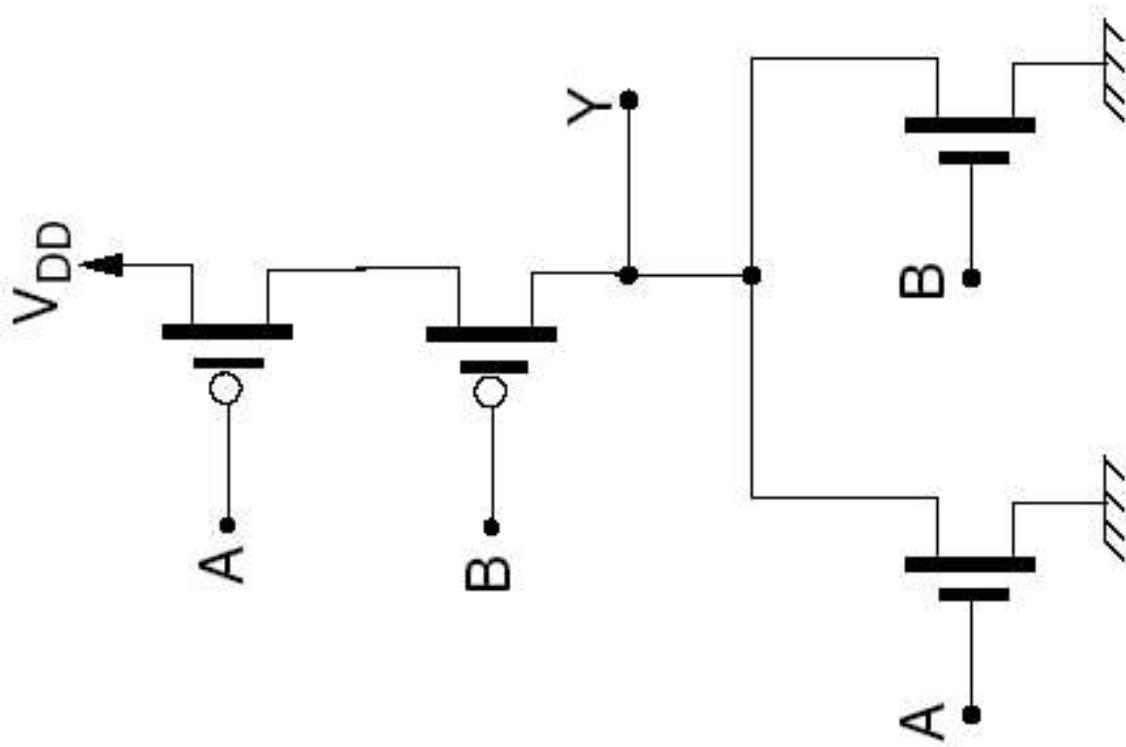
NAND 2

- ★ $Y = \overline{A} \cdot \overline{B}$
- ★ PUN $\rightarrow Y = \overline{\overline{A}} + \overline{\overline{B}}$
- ★ PDN $\rightarrow \overline{Y} = A \cdot B$



NOR 2

$$\begin{aligned}\star Y &= \overline{A+B} \\ \star PUN &\rightarrow Y = \overline{\overline{A}} \cdot \overline{\overline{B}} \\ \star PDN &\rightarrow \overline{Y} = A + B\end{aligned}$$



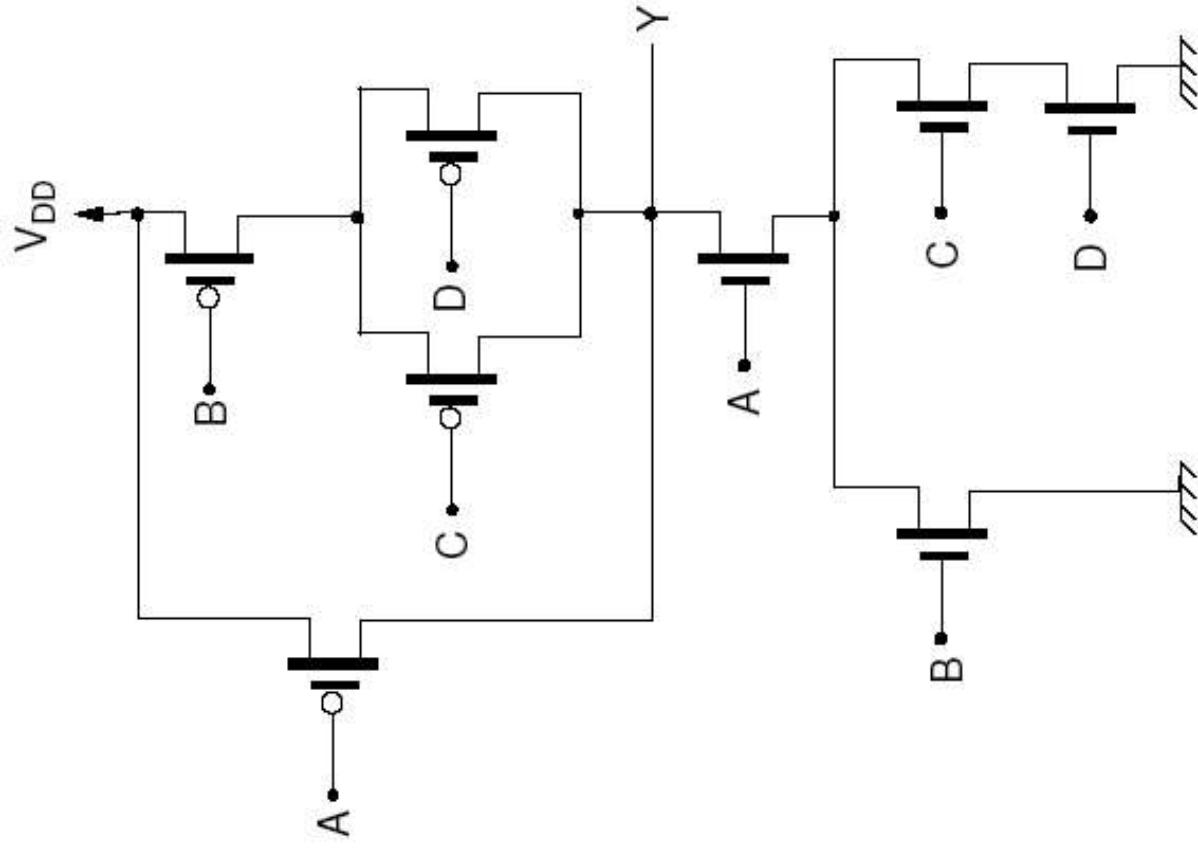
COMPLEX FUNCTION

$$Y = \overline{A(B + CD)}$$

PUN \rightarrow
$$\begin{aligned} Y &= \overline{A(B + CD)} \\ &= \overline{A} + \overline{B + CD} \\ &= \overline{A} + \overline{B} \overline{CD} \\ &= \overline{A} + \overline{B}(\overline{C} + \overline{D}), \end{aligned}$$

PDN \rightarrow
$$\overline{Y} = A(B + CD)$$

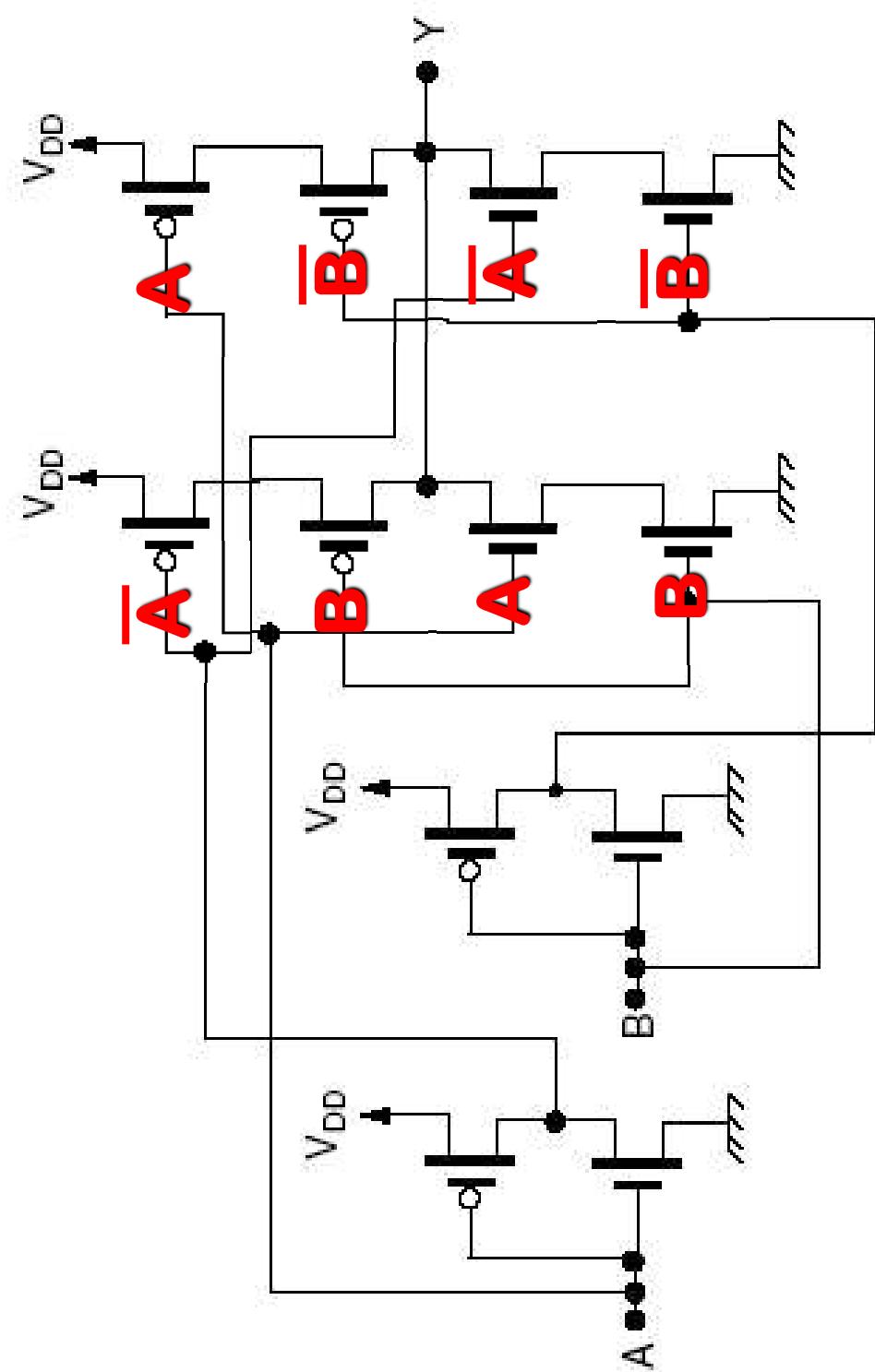
V_{DD}



A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

XOR

$$Y = A\overline{B} + \overline{A}B.$$



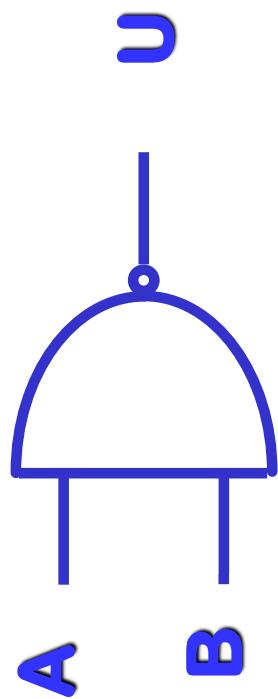
NAND

Truth Table

A	B	U	1	1	1	0
0	0	0	1	0	1	
0	1	0	1	1	1	

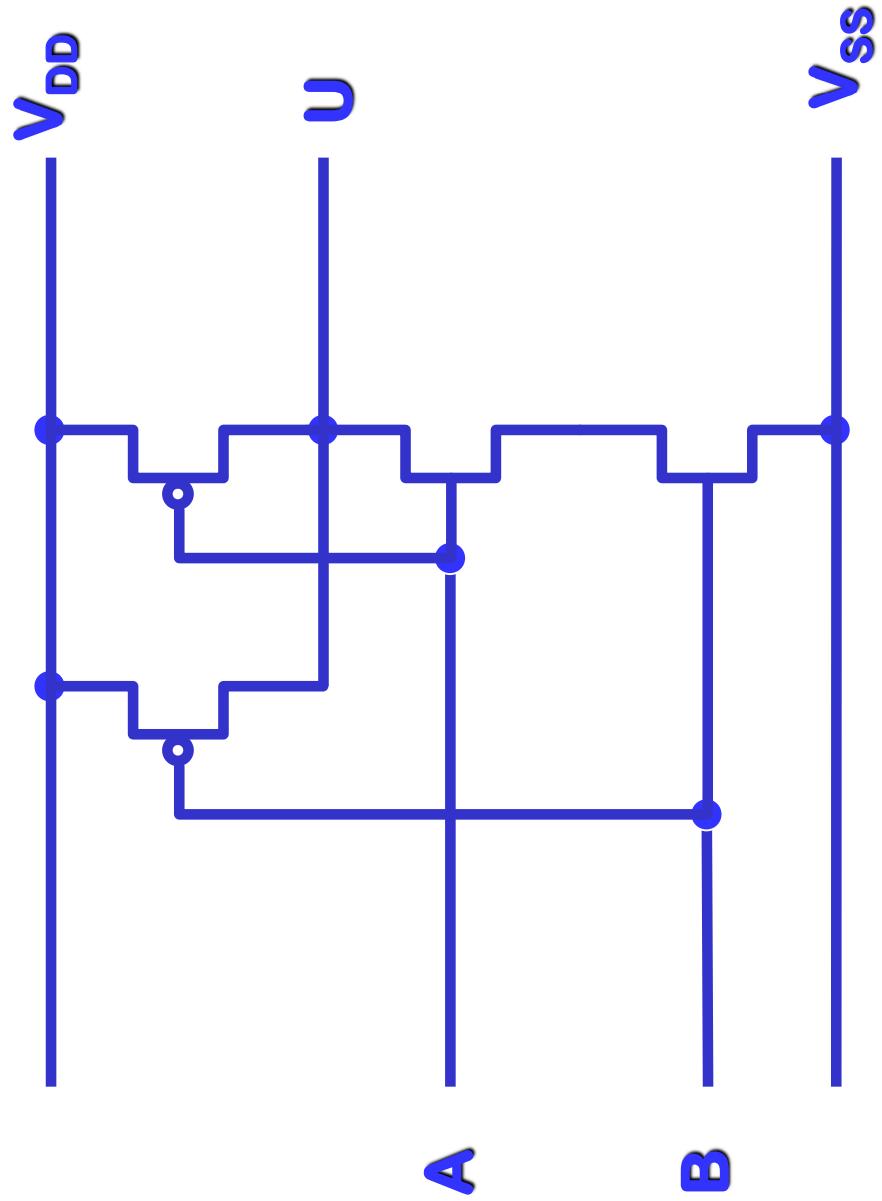
Logic Symbol

$$U = A * B$$



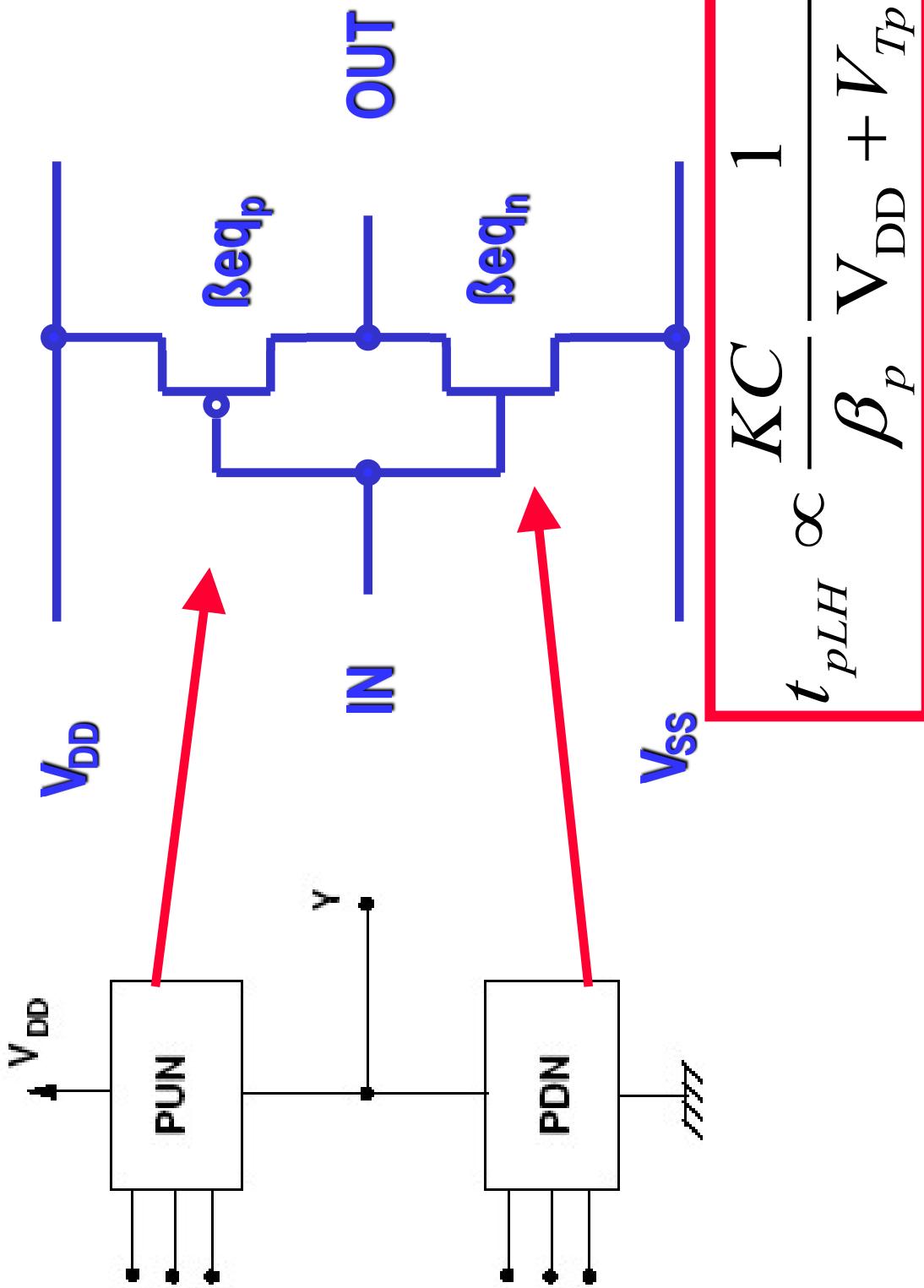
CMOS Implementation

❖ Electric Circuit

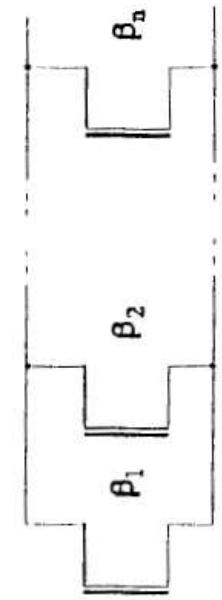


Dynamic A

$$t_{pHL} \propto \frac{KC}{\beta_n} \frac{1}{V_{DD} - V_{Tn}}$$



Dynamic Analysis



$$\beta_{\text{eq}} = \sum_{i=1}^n \beta_i$$

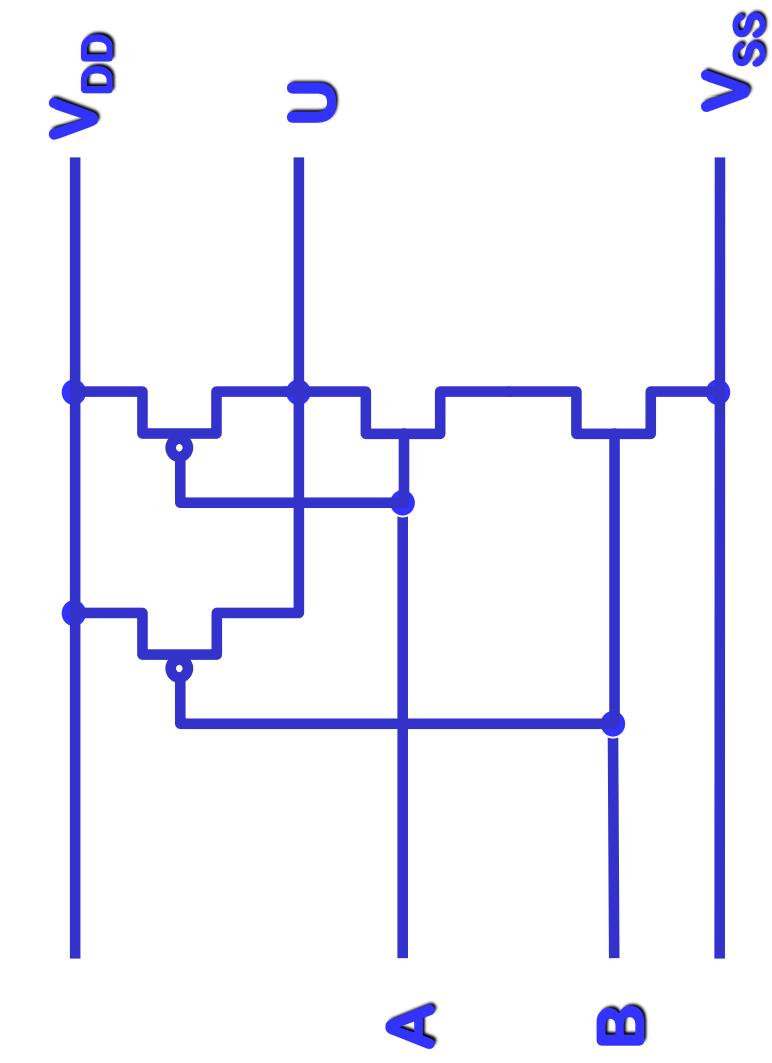
$$\beta_1 \quad \beta_2 \quad \equiv \quad \beta_n$$

Periodic signals

$$\beta_{\text{eq}} = \frac{1}{\sum_{i=1}^n \frac{1}{\beta_i}}$$

?

Dynamic Analysis



A	B	U			
0	0	1	$2\beta_p$		
0	1	1	β_p		
1	0	1	β_p	0	$\beta_n/2$

$$t_{pLH} \propto \frac{KC}{\beta_{eqp}} = \frac{KC}{\beta_p}$$

$$t_{pHL} \propto \frac{KC}{\beta_{eqn}} = \frac{2KC}{\beta_n}$$

48

Dynamic Analysis

$$t_{pLH} \propto \frac{KC}{\beta_{eqp}} = \frac{KC}{\beta_p}$$

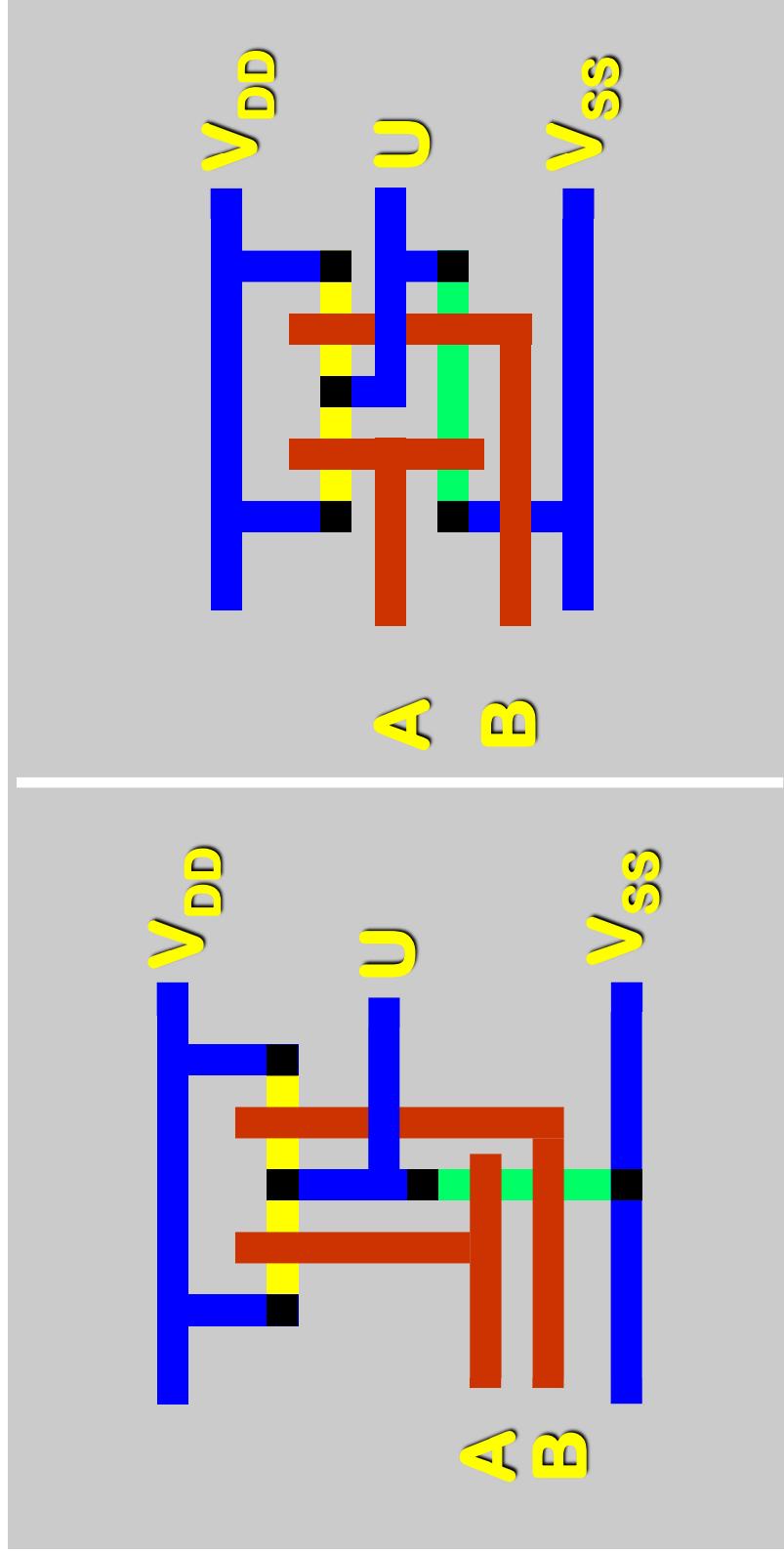
♦ **tp_{HL} = tp_{LH} in the worst case**

$$\beta_p = \frac{\beta_n}{2} \rightarrow \beta_n = 2\beta_p \rightarrow \mu_n \frac{W_n}{L_n} = 2\mu_p \frac{W_p}{L_p}$$

If $\mu_p = \frac{\mu_n}{2}$ $L_n = L_p = L_{\min}$ \longrightarrow $W_n = W_p$

Stick Diagram

❖ Different topological solutions



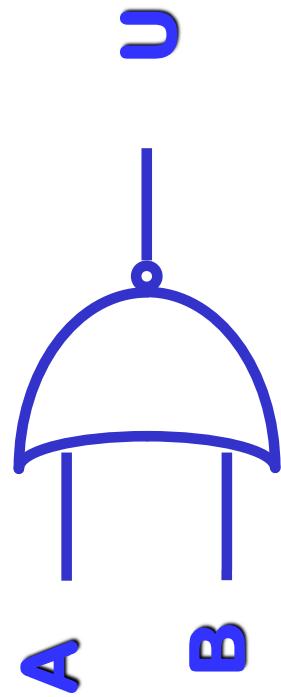
NOR

Truth Table

A	B	U
0	0	1
0	1	0
1	0	0
1	1	0

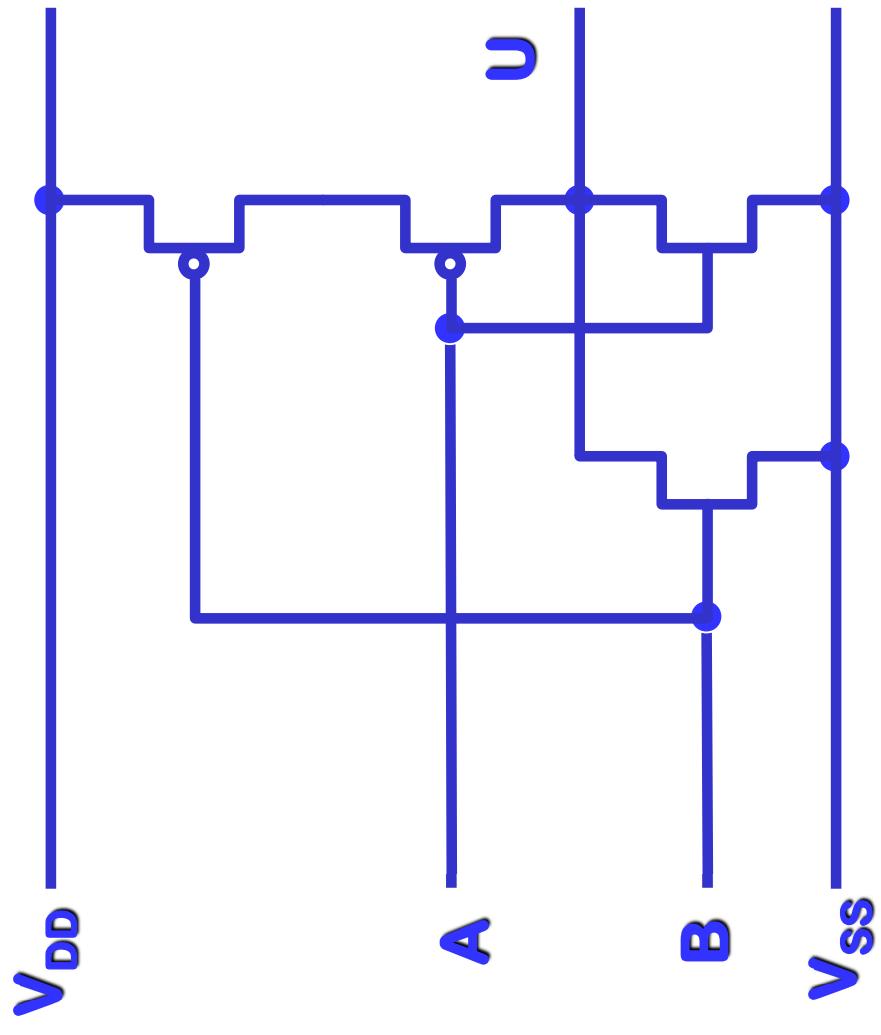
Logic Symbol

$$U = \overline{A + B}$$



Dynamic Analysis

Electric Circuit

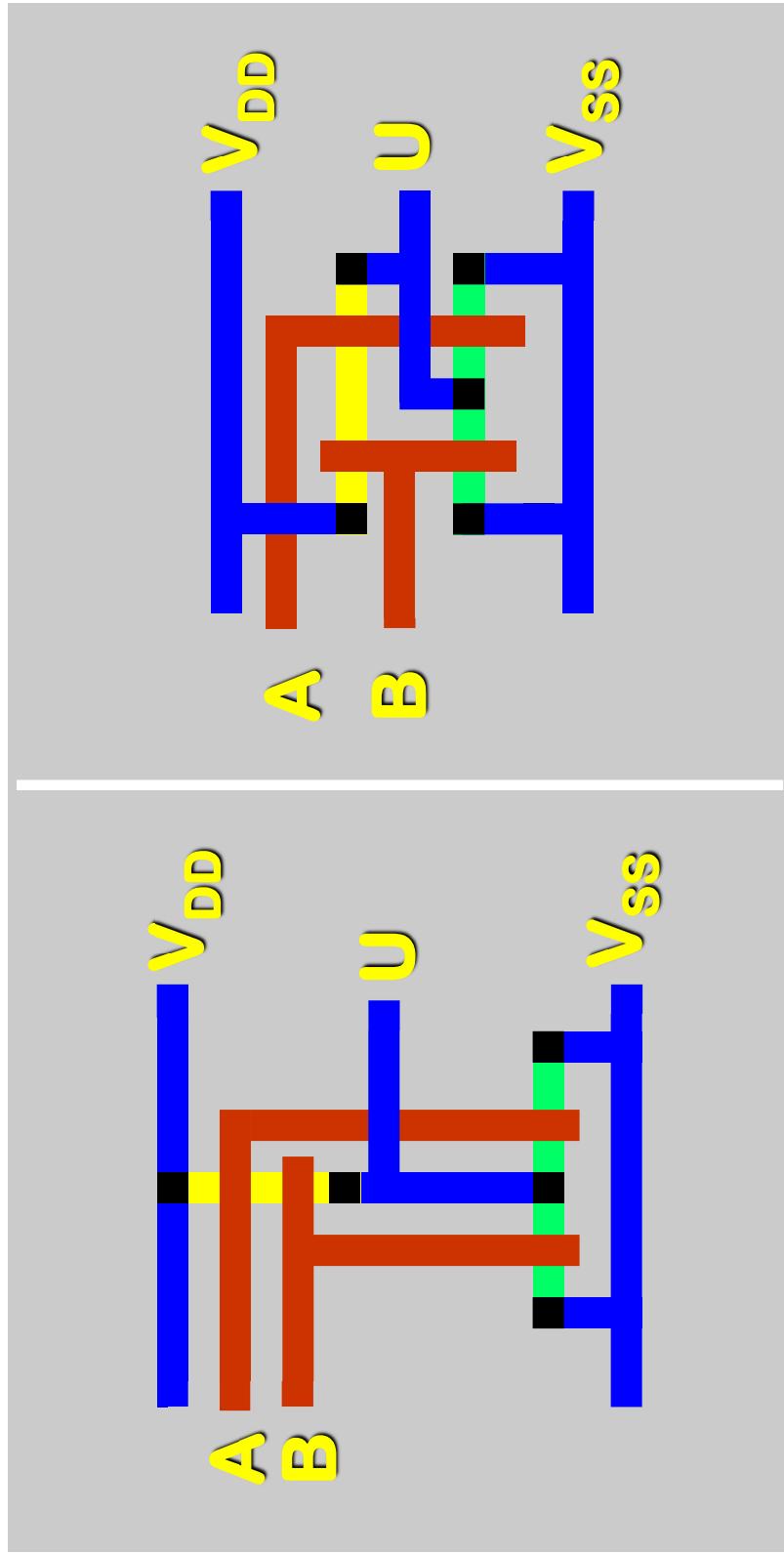


A	B	U	$\beta_p/2$	β_n	β_n	$2\beta_n$
0	0	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	1	1	1	1
1	1	1	1	1	1	1

$$52 \quad \text{if } \mu_p = \frac{\mu_n}{2} \quad L_n = L_p = L_{\min} \longrightarrow W_p = 4W_n$$

Stick Diagram

❖ Different topological solutions



NOR2 - NAND2 Comparison

$$\beta_{eq\ NAND} = \beta_p^{NAND} = \frac{\beta_n^{NAND}}{2}$$

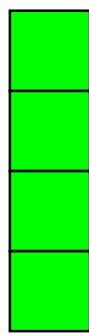
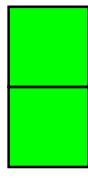
$$\beta_{eq\ NOR} = \beta_n^{NOR} = \frac{\beta_p^{NOR}}{2}$$

$$W_n^{NOR} = W_p^{NOR} = 4W$$

$$\beta_n^{NAND} = 2\beta_n^{NOR} \Rightarrow W_n^{NAND} = 2W_n^{NOR} = 2W$$

$$\beta_p^{NAND} = \frac{\beta_p^{NOR}}{2} \Rightarrow W_p^{NAND} = \frac{W_p^{NOR}}{2} = \frac{4W}{2} = 2W$$

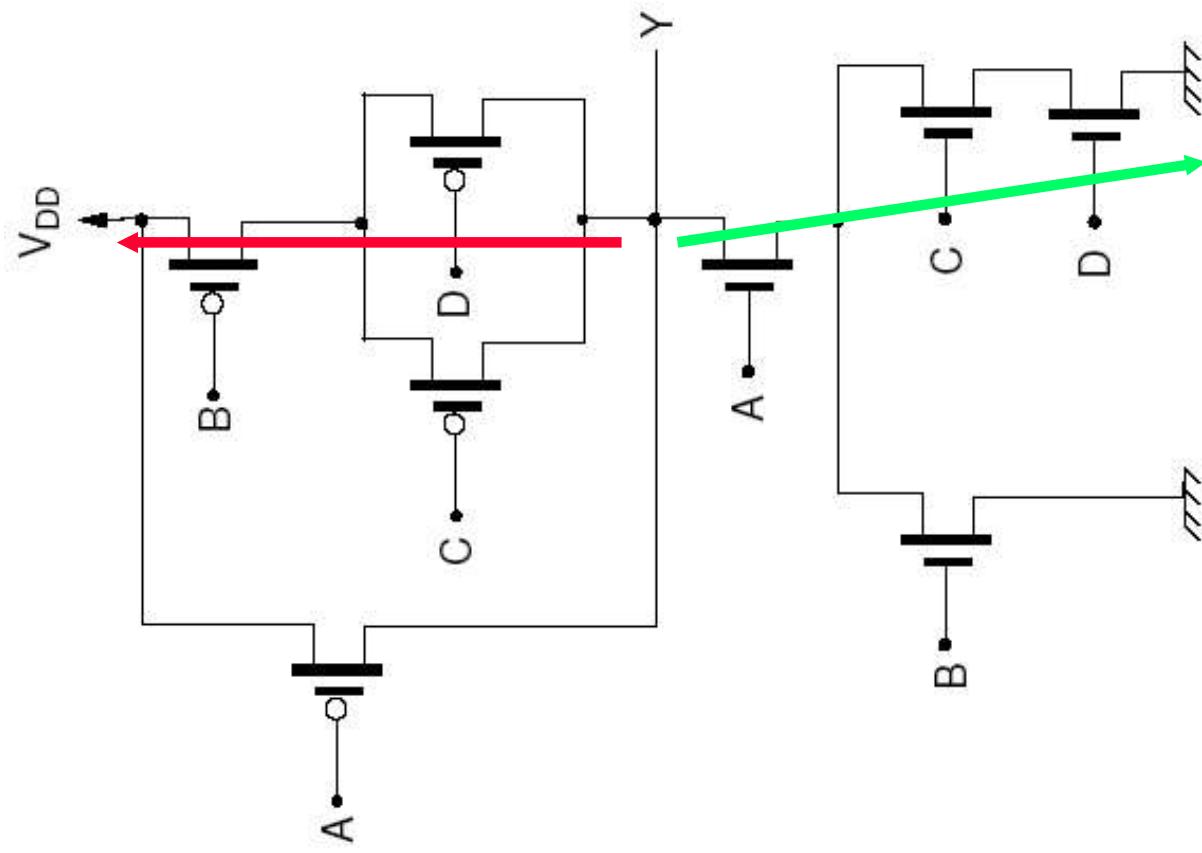
NOR2 – NAND2 Comparison



8 WL

10 WL

$$Y = \overline{A(B + CD)}$$



A	B	C	D	Y	B
0	0	0	0	1	5/3
0	0	0	1	1	3/2
0	0	1	0	1	3/2
0	0	1	1	1	1
0	1	0	0	1	1
0	1	0	1	1	1
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	1	2/3
1	0	0	1	1	1/2
1	0	1	0	1	1/2
1	0	1	1	0	1/3
1	1	0	0	0	1
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	0	4/3

$$t_{pLH} \propto \frac{KC}{\beta eq_p}$$

$$t_{pHL} \propto \frac{KC}{\beta eq_n}$$

$$\beta eq_p = \frac{\beta_p}{2} = \frac{\mu_p W_p}{2 L_p}$$

♦ **tp_{HL} = tp_{LH} in the worst case**

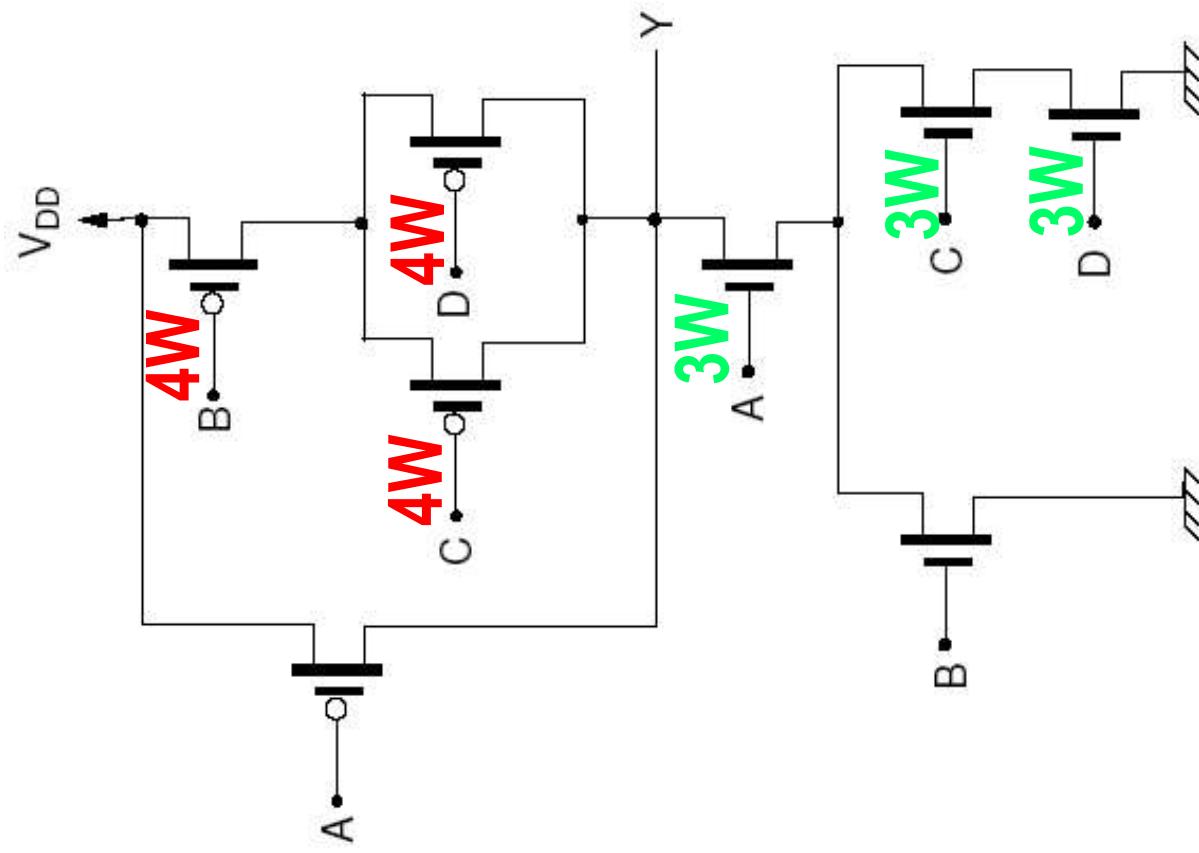
$$\frac{\mu_p W_p}{2 L_p} = \frac{\mu_n W_n}{3 L_n}$$

$$\frac{W_p}{W_n} = \frac{4}{3}$$

If $\mu_p = \frac{\mu_n}{2}$ $L_n = L_p = L_{\min}$

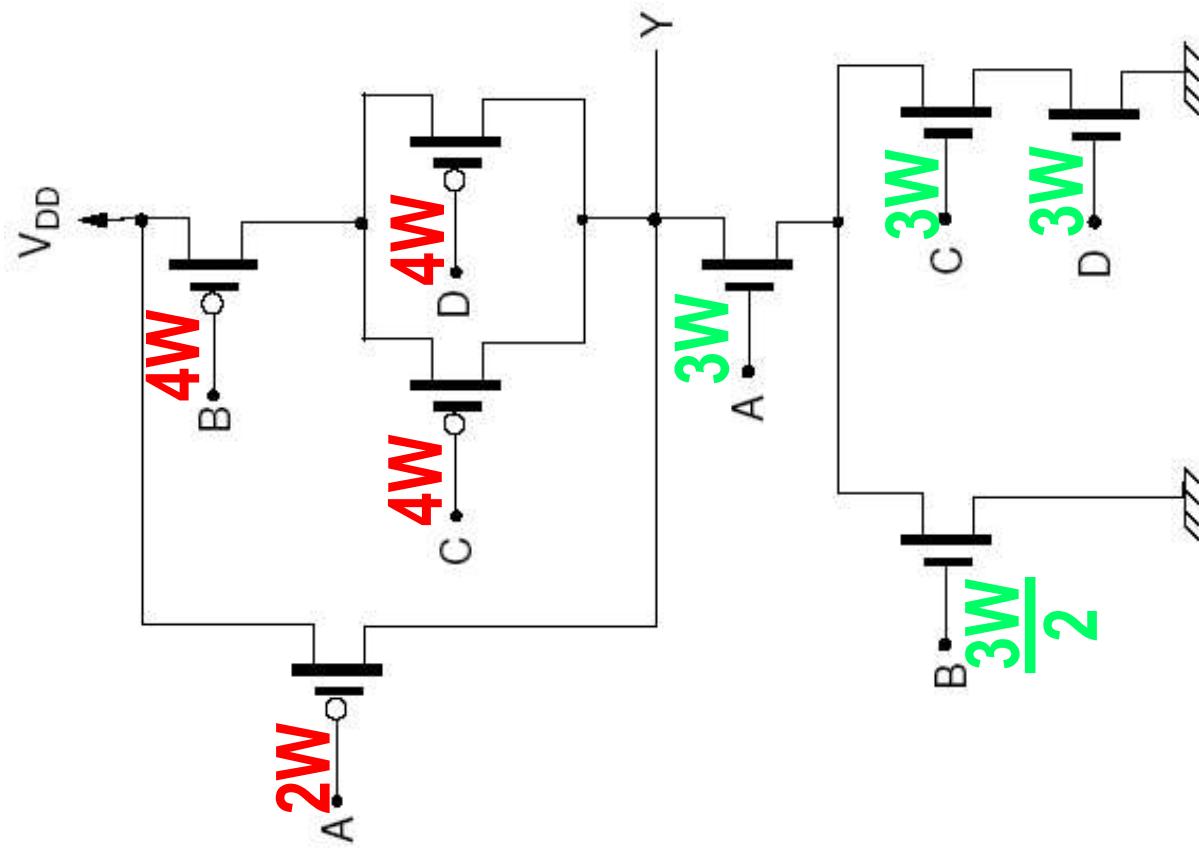


$$Y = \overline{A(B + CD)}$$



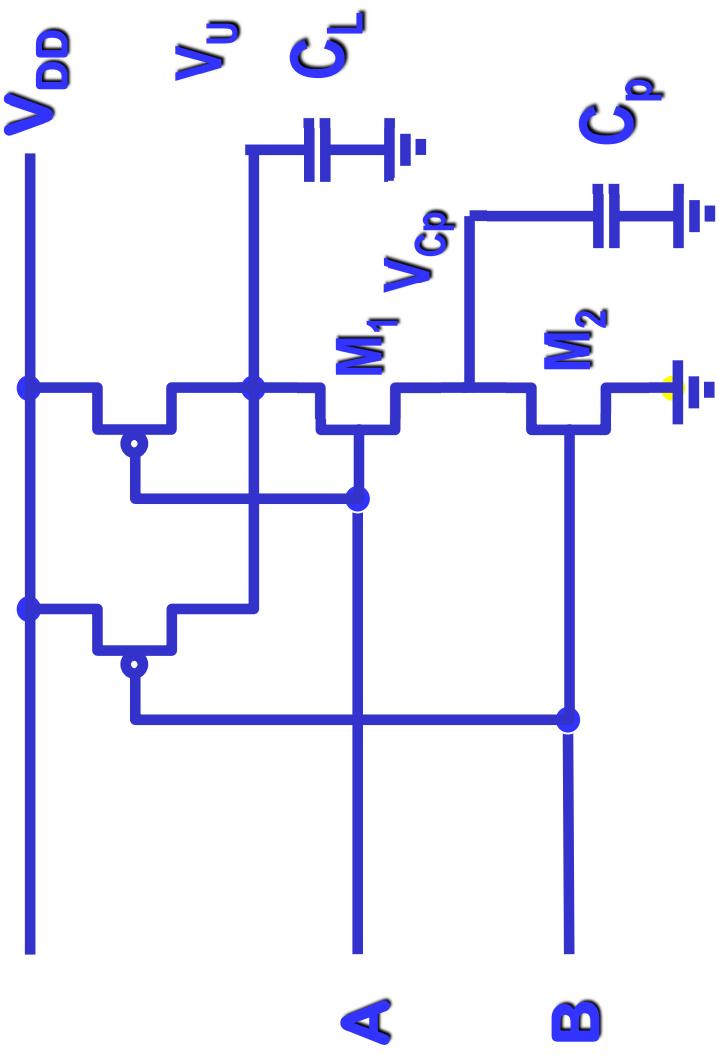
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$$Y = \overline{A(B + CD)}$$



A	B	C	D	Y	B
0	0	0	0	1	5/3
0	0	0	1	1	3/2
0	0	1	0	1	3/2
0	0	1	1	1	1
0	1	0	0	1	1
0	1	0	1	1	1
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	1	2/3
1	0	0	1	1	1
1	0	1	0	1	1/2
1	0	1	1	0	1/2
1	1	0	0	0	1/3
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	1	1	4/3

CMOS gate - Body Effect

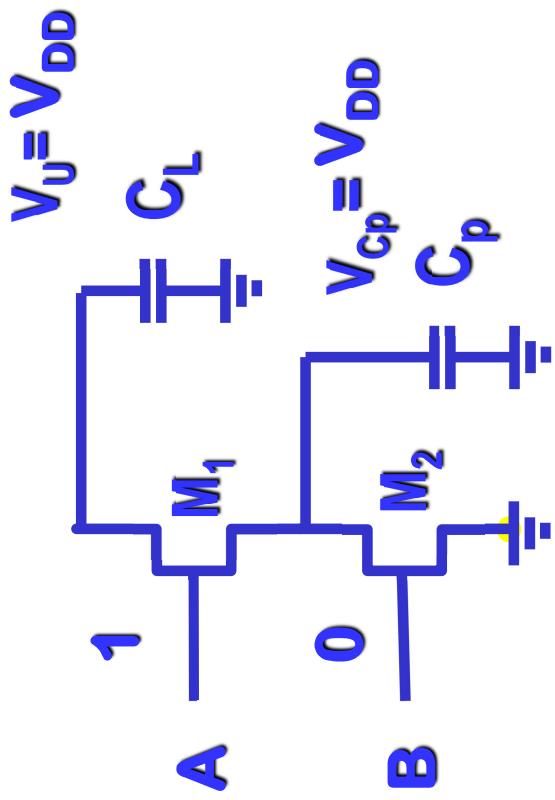


$A = 1 \quad B = 1$
 $A = 1 \quad B = 0$
 $A = 0 \quad B = 1$

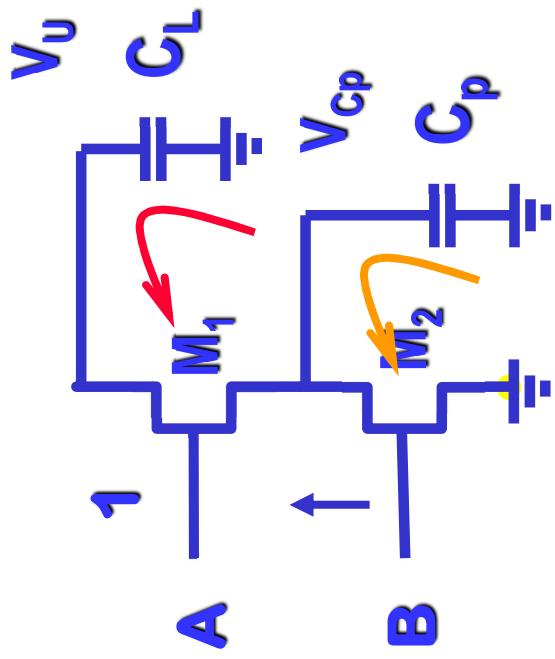
		U			
		1	1	1	0
		0	0	0	1
A	B	0	0	1	0
A	B	0	1	0	1

CMOS gate - Body Effect

$A = 1 \quad B = 0$
 $t \leq 0$



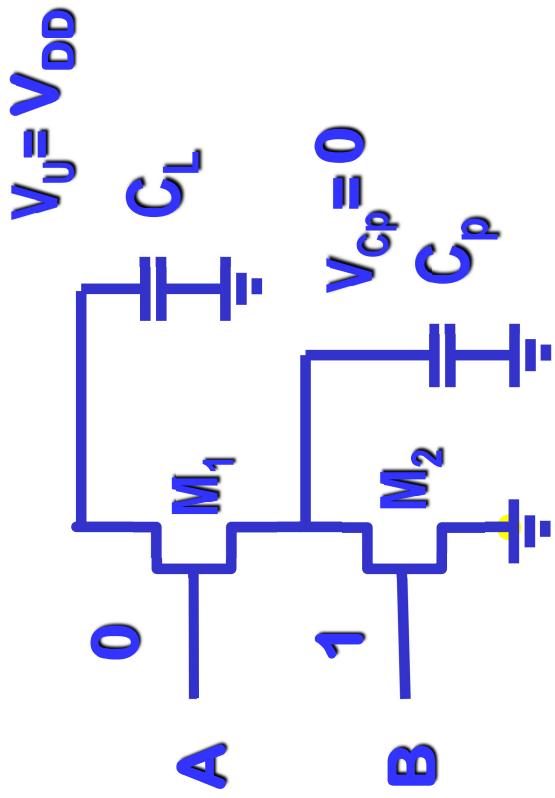
$A = 1 \quad B = 1$
 $t \geq 0$



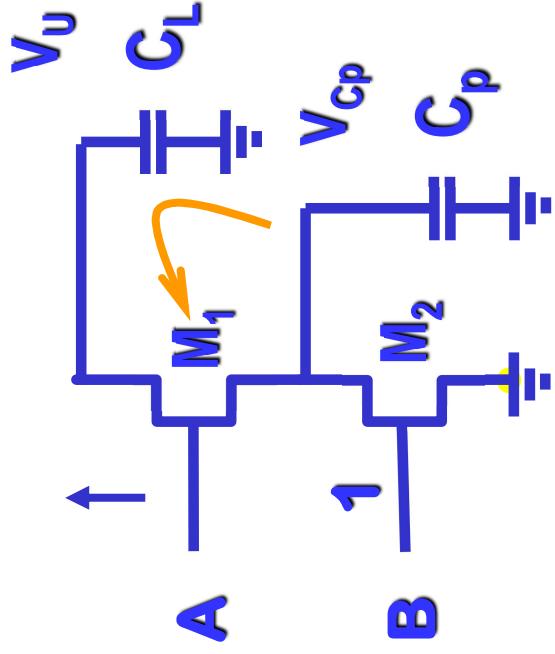
First C_p discharges through M_2 , M_1 starts with $V_s = V_{DD}$, so low M_1 current due to body effect. Longer propagation time w.r.t. to the one estimated with β_{req}

CMOS gate - Body Effect

$A = 0 \quad B = 1$
 $t \leq 0$

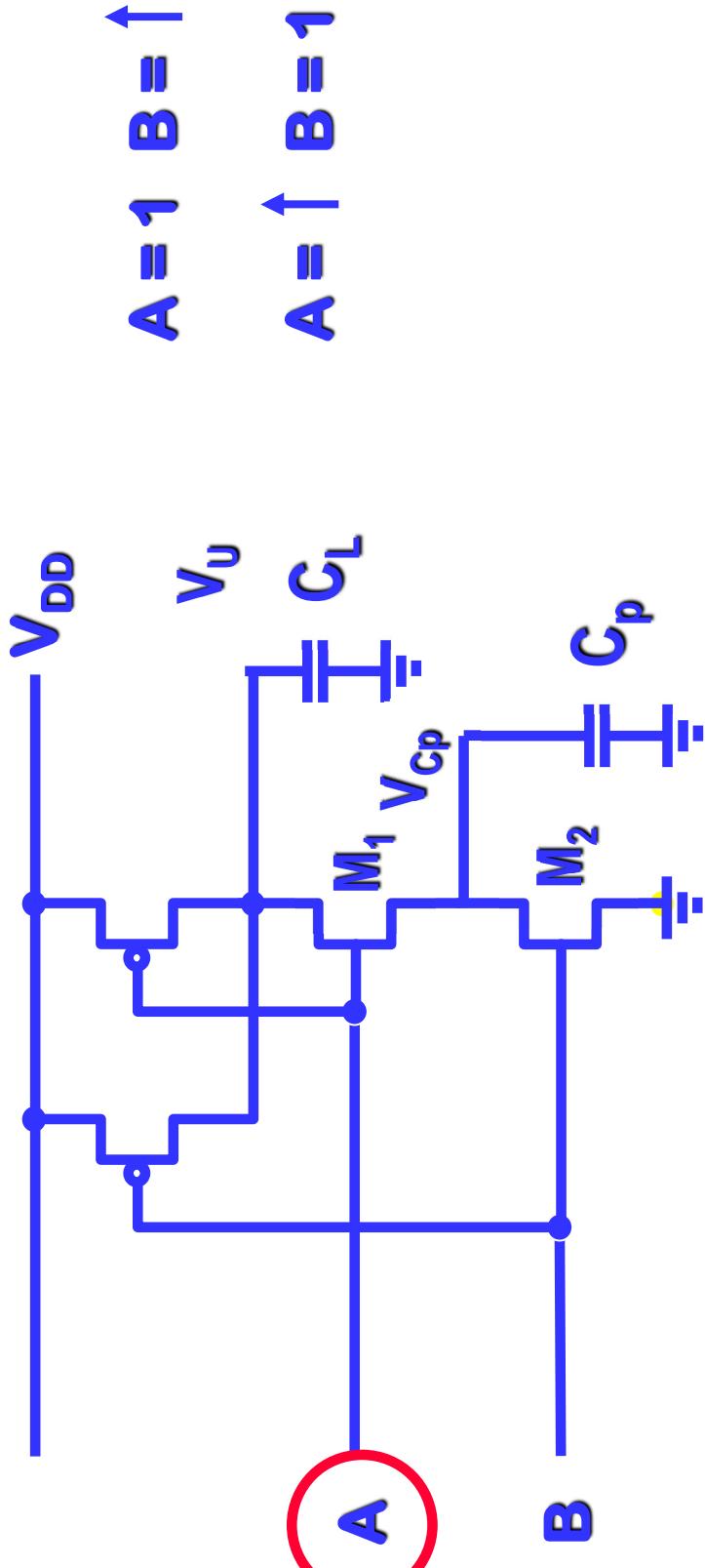


$A = 1 \quad B = 1$



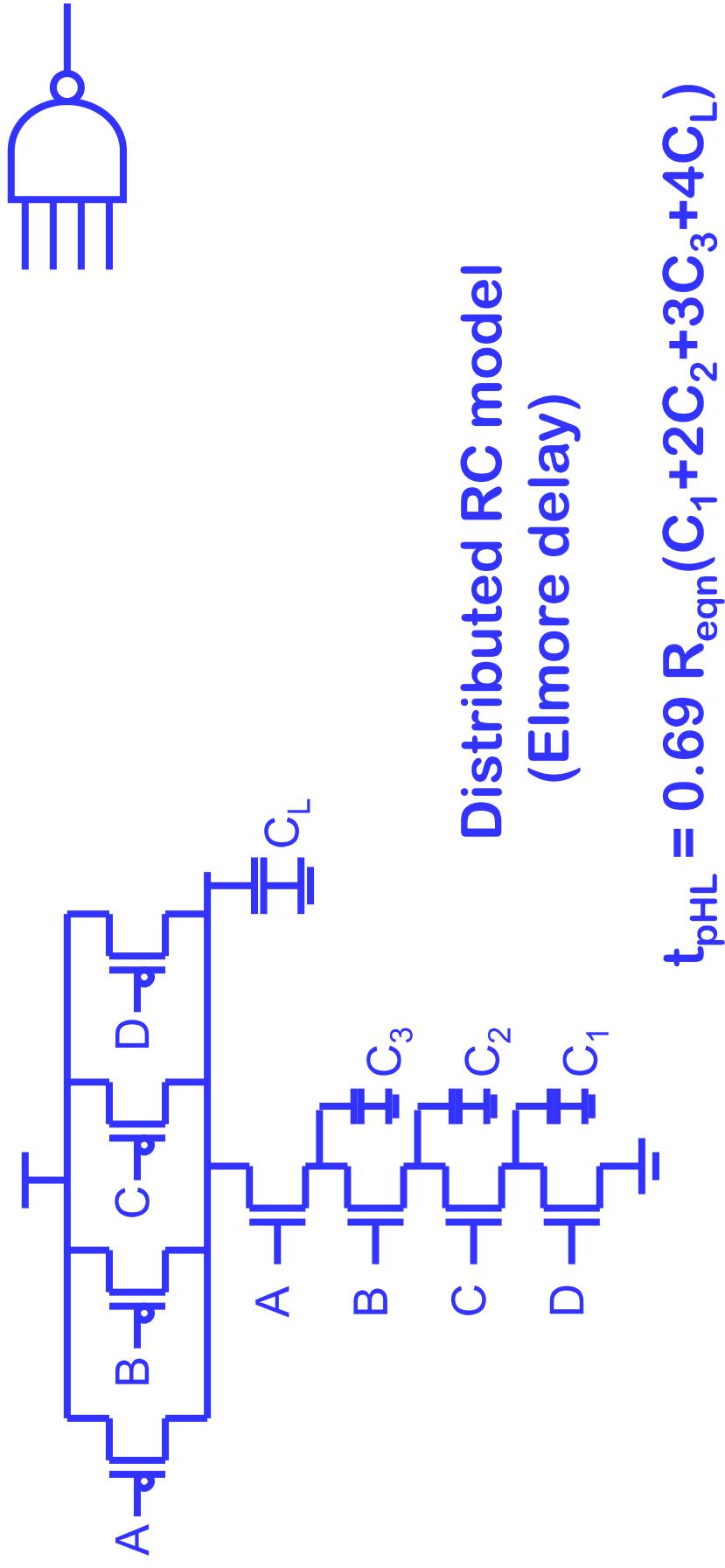
C_p is at ground. So after A input switching, M_1 source is at ground through C_p . Reduced body effect and so faster gate switching.

CMOS gate - Body Effect



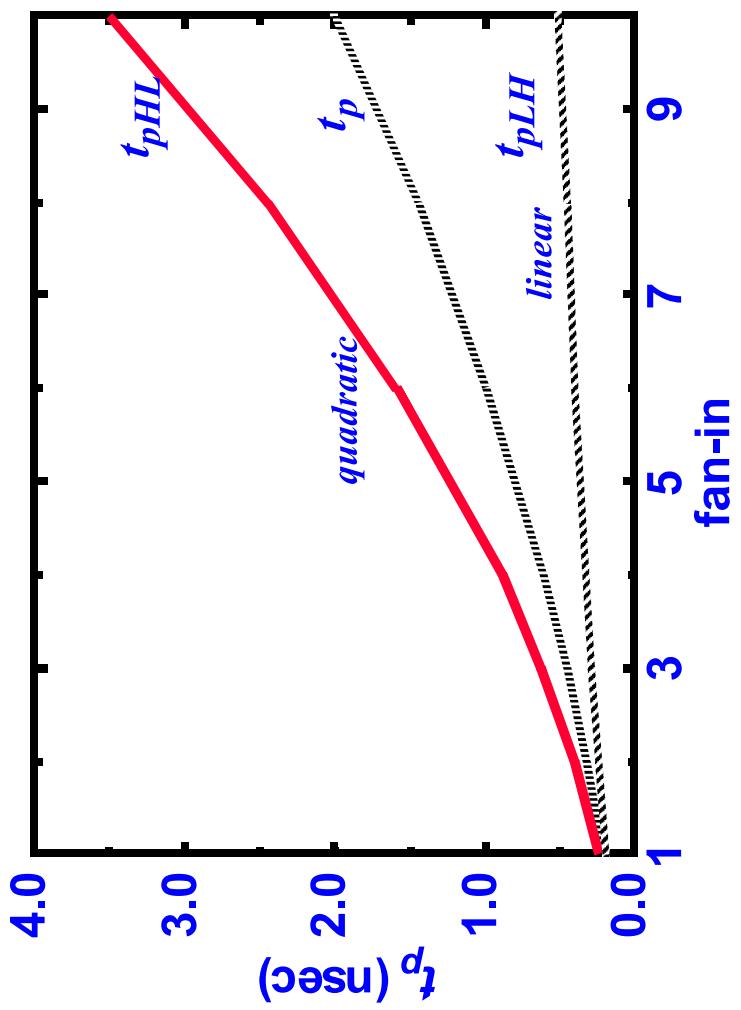
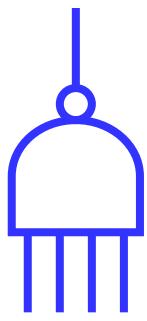
Faster output switching are the ones due to switching of input closer to the output

Dynamic Analysis



Propagation delay deteriorates rapidly as a function of fan-in – quadratically in the worst case

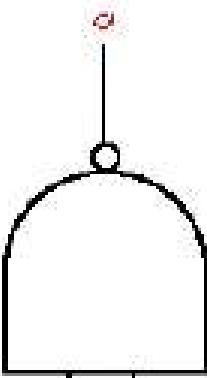
Dynamic Analysis



Gates with fan-in greater than 4 should be avoided

Strength 1

Cell Area	43.680 μm^2
Equation	$Q = \overline{!(A \& B)}$
Type	Combinational
Input	A, B
Output	Q

**State Table**

A	B	Q
L	-	H
H	H	L
-	L	H

Propagation Delay [ns]

Input Transition [ns]	0.01	4.00
Load Capacitance [fF]	5.00	100.00
A to Q	tall	0.06
	rise	0.07
B to Q	tall	0.06
	rise	0.08

Output Transition [ns]

Input Transition [ns]	0.01	4.00
Load Capacitance [fF]	5.00	100.00
A to Q	tall	0.58
	rise	0.68
B to Q	tall	0.58
	rise	0.69

Input Transition [ns]

Input Transition [ns]	0.01	4.00
Load Capacitance [fF]	5.00	100.00
A to Q	tall	0.13
	rise	0.70
B to Q	tall	0.37
	rise	0.91

Leakage [pW]

A	2.7240
B	3.0190

Capacitance [fF]

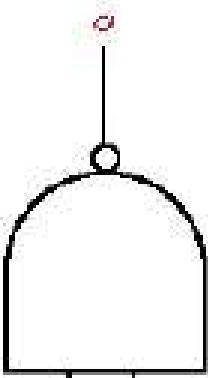
A to Q	tall	8.00
	rise	54.46
B to Q	tall	7.37
	rise	64.63

Dynamic Power Consumption [nW/MMHz]

Input Transition [ns]	0.01	4.00
Load Capacitance [fF]	5.00	100.00
A to Q	tall	8.49
	rise	55.63
B to Q	tall	7.81
	rise	64.73

NAND2X1

Strength 2
Cell Area 43.680 μm^2
Equation Q = "!(A & B)"
Type Combinational
Input A, B
Output Q



State Table	
A	B
L	-
H	H
-	L
	H

Propagation Delay [ns]			
Input Transition [ns]	0.01	4.00	
Load Capacitance [fF]	10.00	200.00	10.00
A to Q	Fall	0.66	-0.69
	Rise	0.65	0.61
B to Q	Fall	0.66	-0.27
	Rise	0.69	0.75

Output Transition [ns]			
Input Transition [ns]	0.01	0.01	4.00
Load Capacitance [fF]	10.00	200.00	10.00
A to Q	Fall	0.07	0.92
	Rise	0.08	1.16
B to Q	Fall	0.07	0.92
	Rise	0.08	1.07

Leakage [pW]	
A	0.31

Capacitance [fF]	
A	3.8420
B	4.4020

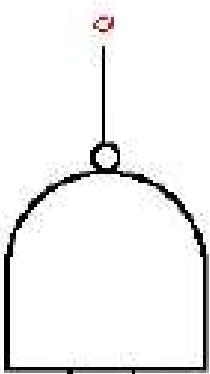
Dynamic Power Consumption [nW/MHz]			
Input Transition [ns]	0.01	4.00	
Load Capacitance [fF]	10.00	200.00	10.00
A to Q	Fall	5.99	6.95
	Rise	64.40	64.67
B to Q	Fall	4.28	5.14
	Rise	77.18	78.81
		1504.40	1252.61

NAND2X2



www.ams.com

Strength	6
Cell Area	72.800 μm^2
Equation	$Q = \overline{A}(\overline{A} \& B)$
Type	Combinational
Input	A, B
Output	Q



State Table		
A	B	Q
L	-	H
H	H	L
-	L	H

Propagation Delay [ns]			
Input Transition [ns]	0.01	4.00	
Load Capacitance [fF]	30.00	600.00	600.00
A to Q	fall	0.05	0.65
	rise	0.05	0.68
B to Q	fall	0.05	0.65
	rise	0.06	0.69

Output Transition [ns]			
Input Transition [ns]	0.01	4.00	
Load Capacitance [fF]	30.00	600.00	600.00
A to Q	fall	0.06	0.92
	rise	0.07	1.06
B to Q	fall	0.06	0.92
	rise	0.08	1.07

Leakage [pW]	
Capacitance [fF]	0.01
A	10.1390
B	11.0760

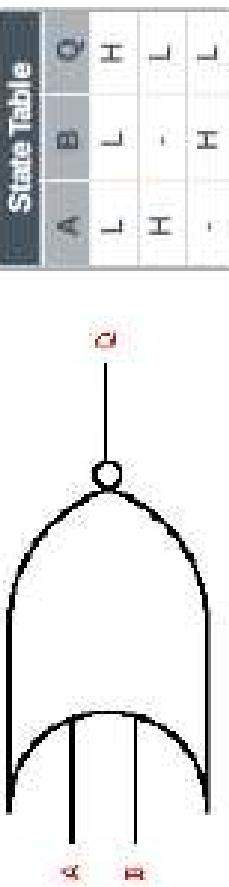
Dynamic Power Consumption [nW/MHz]			
Input Transition [ns]	0.01	4.00	
Load Capacitance [fF]	30.00	600.00	600.00
A to Q	fall	5.73	8.27
	rise	155.47	156.48
B to Q	fall	5.87	8.76
	rise	196.60	199.91

Dynamic Power Consumption [nW/MHz]			
Input Transition [ns]	0.01	4.00	
Load Capacitance [fF]	30.00	600.00	600.00
A to Q	fall	3025.58	2459.24
	rise	3806.99	3246.79
B to Q	fall	3407.23	2766.61
	rise	4408.72	3647.73

am
www.ams.com

NAND2X6

Strength 1	
Cell Area	43.680 μm^2
Equation	$Q = \overline{(\overline{A} \mid \overline{B})}$
Type	Combinational
Input	A, B
Output	Q



State Table		
A	B	Q
L	L	H
H	-	L
-	H	L

Propagation Delay [ns]					
Input Transition [ns]	0.01	0.05	0.10	4.00	
Load Capacitance [fF]	5.00	100.00	5.00	100.00	
A to Q	fall	0.04	0.41	-0.64	0.48
	rise	0.11	1.17	1.28	2.61
B to Q	fall	0.05	0.42	-0.45	0.56
	rise	0.11	1.18	1.00	2.25

Output Transition [ns]					
Input Transition [ns]	0.01	0.05	0.10	4.00	
Load Capacitance [fF]	5.00	100.00	5.00	100.00	
A to Q	fall	0.04	0.41	-0.64	0.48
	rise	0.15	1.81	0.92	2.12
B to Q	fall	0.05	0.55	0.94	1.55
	rise	0.15	1.81	0.80	2.12

Capacitance [fF]			
A	2.6610	B	2.9400
Leakage [pW]	0.26		

Dynamic Power Consumption [$\mu\text{W/MHz}$]			
Input Transition [ns]	0.01	4.00	
Load Capacitance [fF]	5.00	100.00	
A to Q	fall	4.63	5.12
	rise	45.80	47.19
B to Q	fall	7.48	7.98
	rise	55.57	56.53

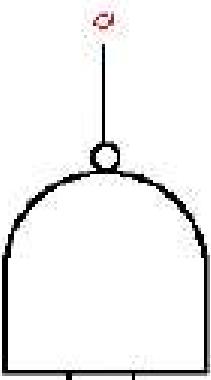
Dynamic Power Consumption [$\mu\text{W/MHz}$]				
Input Transition [ns]	0.01	4.00	Leakage [pW]	4.00
Load Capacitance [fF]	5.00	100.00	5.00	100.00
A to Q	fall	4.63	5.12	326.27
	rise	45.80	47.19	661.91
B to Q	fall	7.48	7.98	453.09
	rise	55.57	56.53	796.35

NOR2X1

am
www.ams.com

Strength 1

Cell Area	43.680 μm^2
Equation	$Q = \overline{!(A \& B)}$
Type	Combinational
Input	A, B
Output	Q

**State Table**

	A	B	Q
	L	-	H
	H	H	L
	-	L	H

Propagation Delay [ns]

Input Transition [ns]	0.01	4.00
Load Capacitance [fF]	5.00	100.00
A to Q	tall	0.06
	rise	0.07
B to Q	tall	0.06
	rise	0.08

Output Transition [ns]

Input Transition [ns]	0.01	4.00
Load Capacitance [fF]	5.00	100.00
A to Q	tall	0.58
	rise	0.68
B to Q	tall	0.58
	rise	0.69

Leakage [pW]

Capacitance [fF]	0.01	4.00
A	2.7240	0.28
B	3.0190	

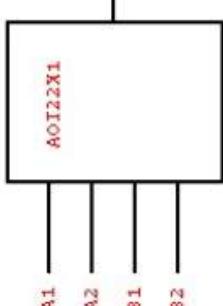
Dynamic Power Consumption [nW/MMHz]

Input Transition [ns]	0.01	4.00
Load Capacitance [fF]	5.00	100.00
A to Q	tall	8.00
	rise	54.46
B to Q	tall	7.37
	rise	64.63

NAND2X1

Example

State Table							
A1	A2	B1	B2	Q			
L	-	L	-	H			
L	-	-	L	H			
H	H	-	-	L			
-	L	L	-	H			
-	L	-	L	H			
-	-	H	H	L			



Strength	1
Cell Area	72.800 μm^2
Equation	$Q = \overline{(A1 \& A2)} \cdot (\overline{B1} \& \overline{B2})$
Type	Combinational
Input	A1, A2, B1, B2
Output	Q

Propagation Delay [ns]			
	0.01	4.00	
Load Capacitance [fF]	5.00	100.00	5.00
A1toQ	fall	0.06	0.58
	rise	0.11	1.15
A2toQ	fall	0.06	0.58
	rise	0.12	1.16
B1toQ	fall	0.09	0.61
	rise	0.15	1.19
B2toQ	fall	0.09	0.61
	rise	0.16	1.19

Output Transition [ns]			
	0.01	4.00	
Input Transition [ns]			
Load Capacitance [fF]	5.00	100.00	5.00
A1toQ	fall	0.08	0.81
	rise	0.18	1.79
A2toQ	fall	0.08	0.81
	rise	0.20	1.81
B1toQ	fall	0.11	0.84
	rise	0.18	1.79
B2toQ	fall	0.11	0.84
	rise	0.20	1.81

$$Y = \overline{A_1 \cdot A_2 + B_1 \cdot B_2}$$

Capacitance [fF]	
A1	2.7590
A2	3.0640
B1	2.9460
B2	3.2810

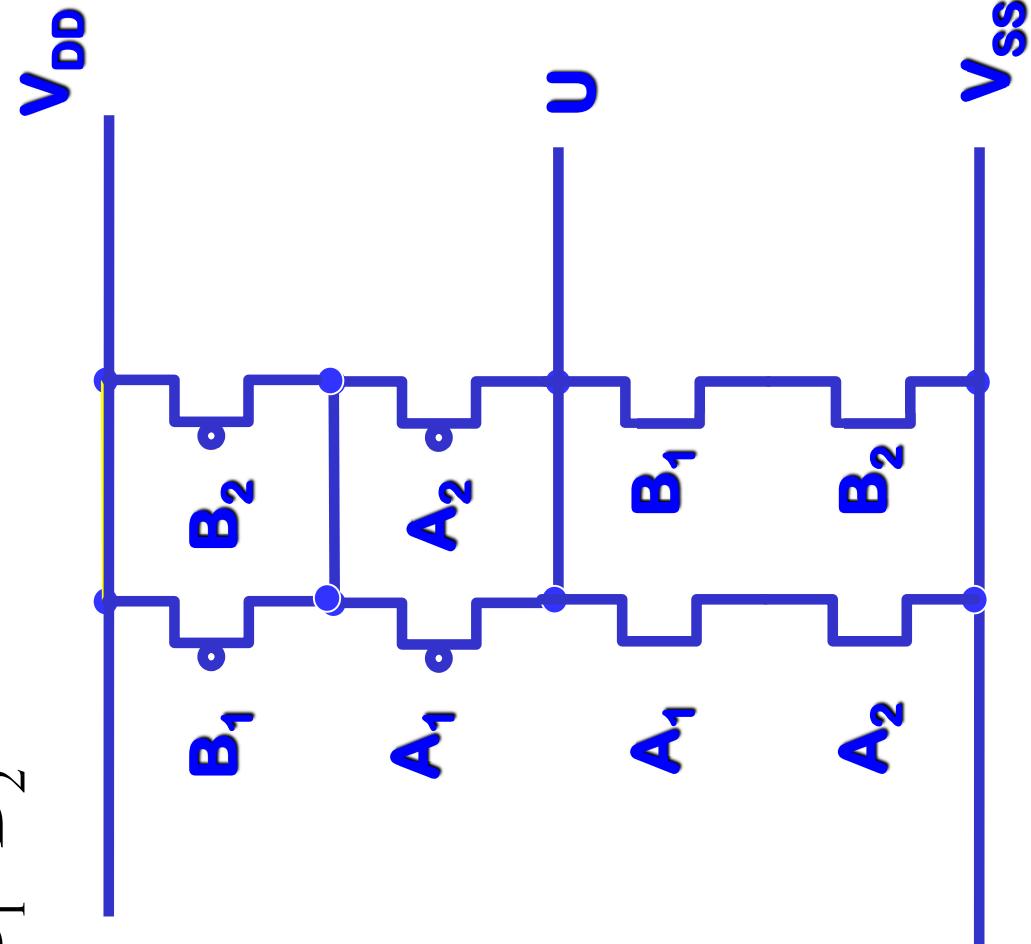
Dynamic Power Consumption [nW/MHz]			
	0.01	4.00	
Input Transition [ns]			
Load Capacitance [fF]	5.00	100.00	5.00
A1toQ	fall	4.83	5.56
	rise	52.43	53.92
A2toQ	fall	5.18	5.94
	rise	61.25	62.04
B1toQ	fall	34.51	39.00
	rise	76.53	77.52
B2toQ	fall	34.58	39.00
	rise	84.07	85.01

AOI22X1

am
www.ams.com

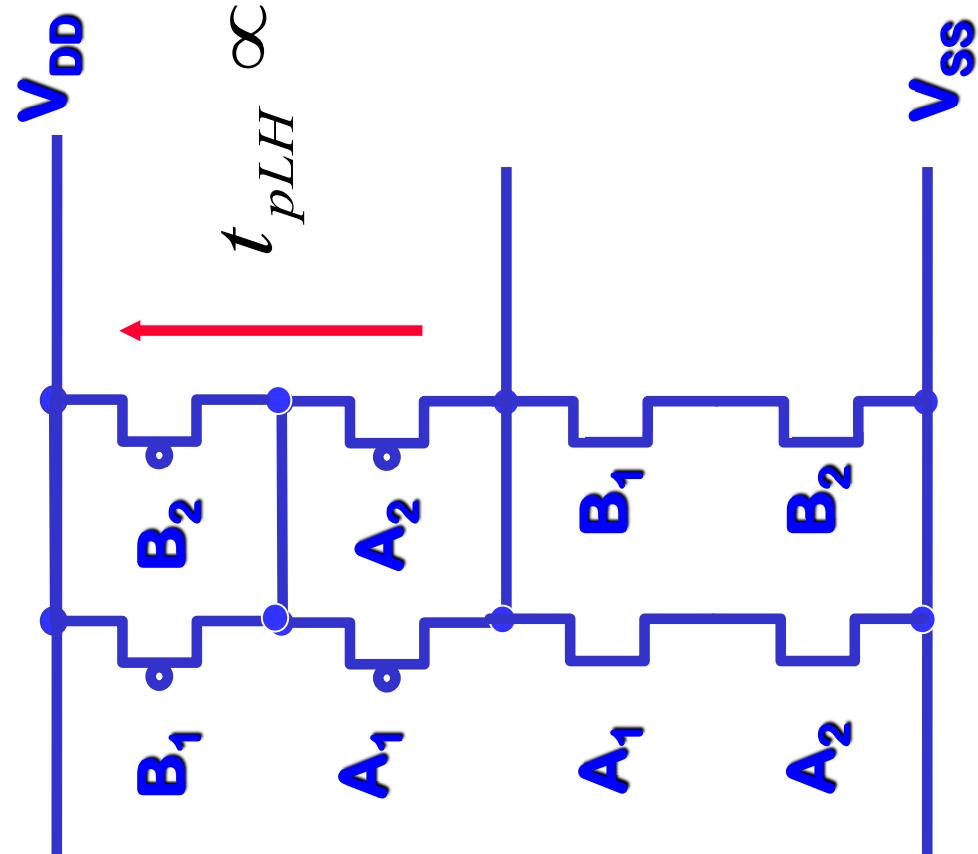
$$Y = \overline{A_1 \cdot A_2 + B_1 \cdot B_2}$$

$$\text{PDN} \quad \overline{Y} = A_1 \cdot A_2 + B_1 \cdot B_2$$



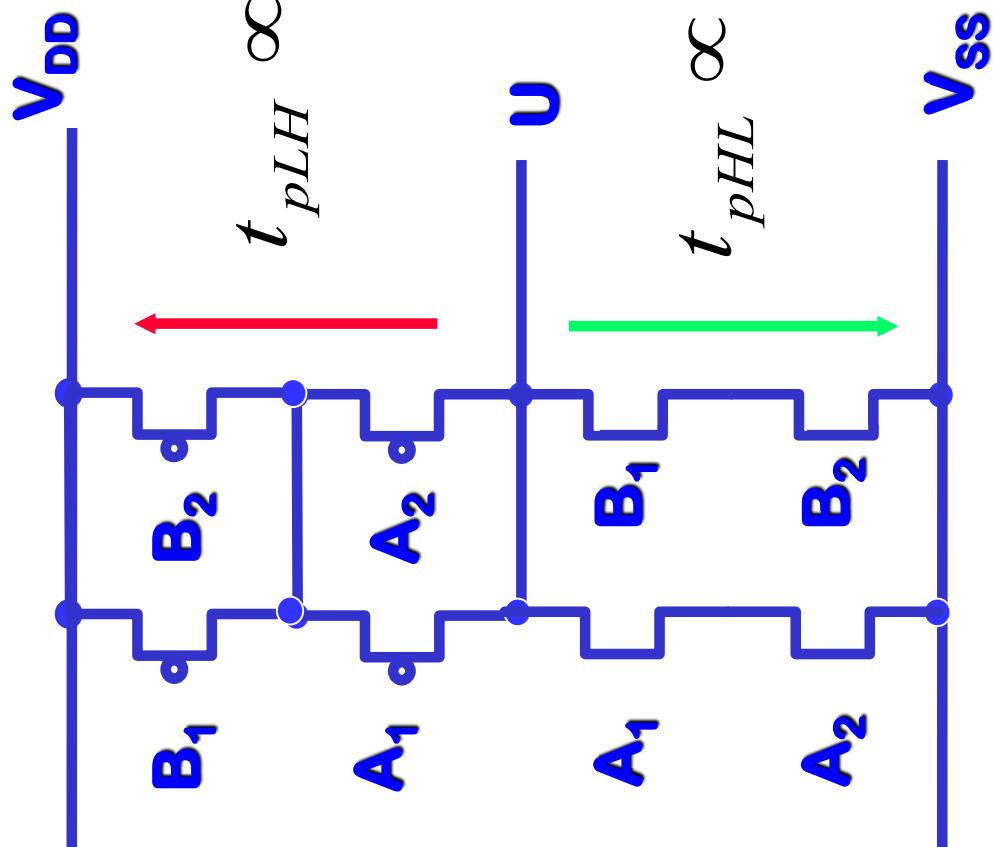
$$Y = \overline{A_1 \cdot A_2 + B_1 \cdot B_2}$$

PDN $\overline{Y} = A_1 \cdot A_2 + B_1 \cdot B_2$



$$Y = \overline{A_1 \cdot A_2 + B_1 \cdot B_2}$$

$$\text{PDN} \quad \overline{Y} = A_1 \cdot A_2 + B_1 \cdot B_2$$



$$t_{pLH} \propto \frac{KC}{\beta eq_p} \quad \beta eq_p = \frac{\beta_p}{2} = \frac{\mu_p}{2} \frac{W_p}{L_p}$$

$$t_{pHL} \propto \frac{KC}{\beta eq_n} \quad \beta eq_n = \frac{\beta_n}{2} = \frac{\mu_n}{2} \frac{W_n}{L_n}$$

$$t_{pLH} \propto \frac{KC}{\beta eq_p}$$

$$\beta eq_p = \frac{\beta_p}{2} = \frac{\mu_p W_p}{2 L_p}$$

♦ **tp_{HL} = tp_{LH} in the worst case**

$$\frac{\mu_p W_p}{2 L_p} = \frac{\mu_n W_n}{2 L_n}$$

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}$$

$$\frac{W_p}{W_n} = 2$$

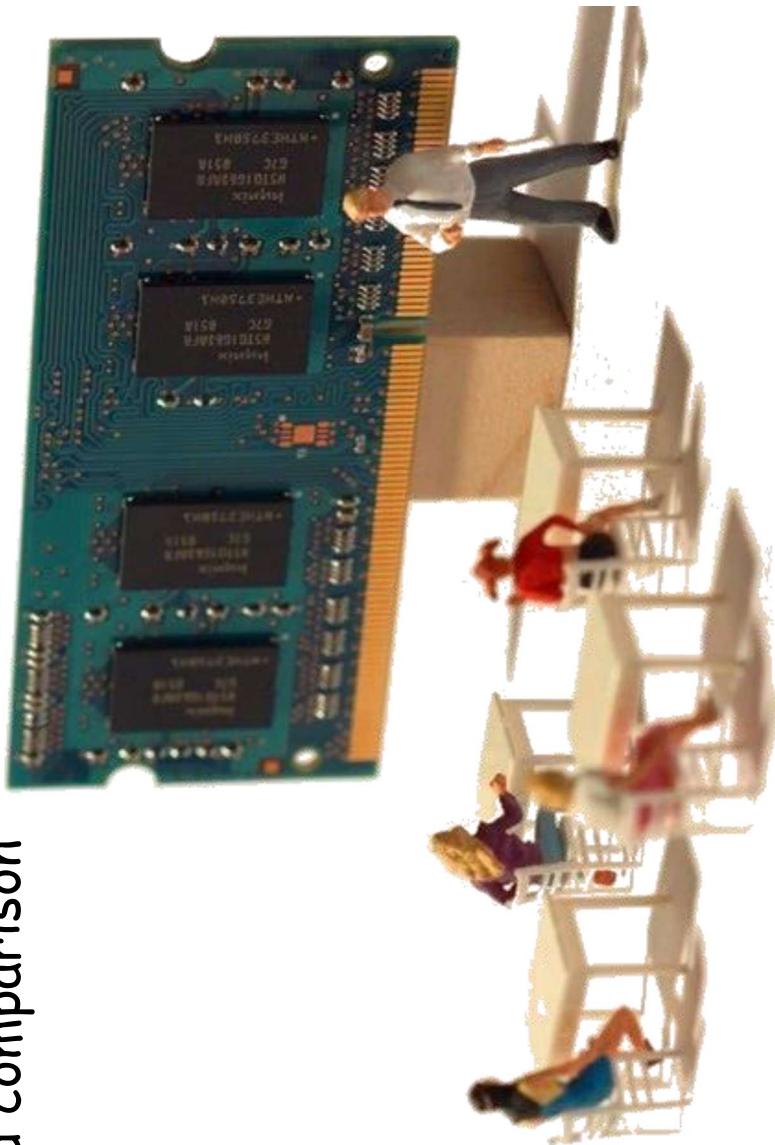
If $\mu_p = \frac{\mu_n}{2}$ $L_n = L_p = L_{\min}$



$$\frac{W_p}{W_n} = 2$$

End Complementary CMOS Logic, Questions ?

- Synthesis
- Dynamic Analysis
- Examples: NAND, NOR and comparison
- Stick Diagram
- Body Effect
- Standard-cell AMS 0,35 μm



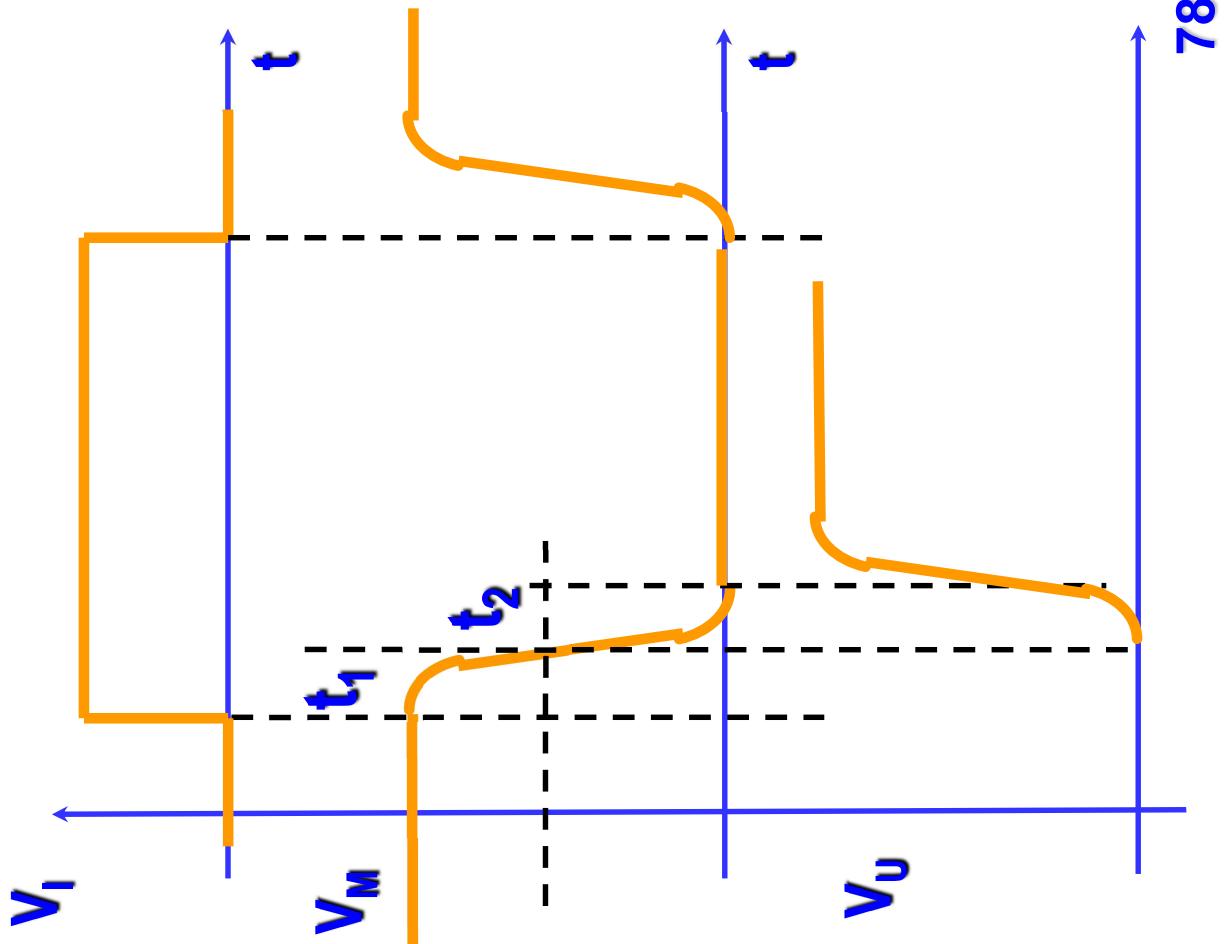
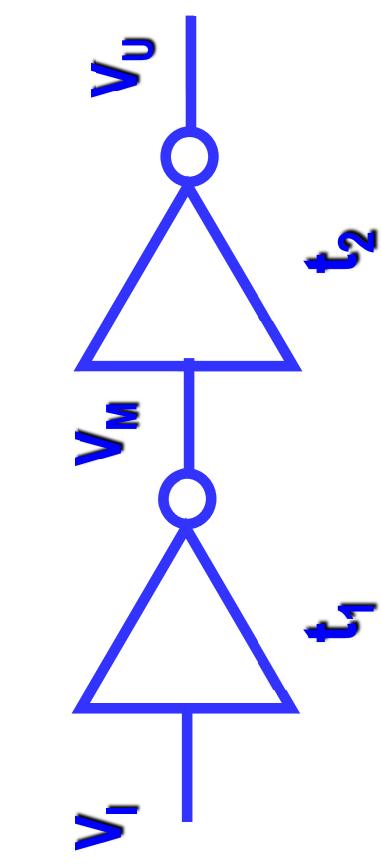
Outline

❖ Review

- Sync. and Async Sequential Logic
- Finite State Machine (MEALY, MOORE, MEALY Rit.)
- ❖ Complementary CMOS Logic

- Synthesis
- Dynamic Analysis
- Examples: NAND, NOR and comparison
- Stick Diagram
- Body Effect
- Standard-cell AMS 0,35 um
- ❖ Example: Inverter Chain
 - Driving an high value capacitor
 - Dynamic Analysis
 - Power-Speed Trade-Off
- ❖ Example: Pass Transistor Chain
 - Dynamic Analysis
 - Area - Speed Trade-Off

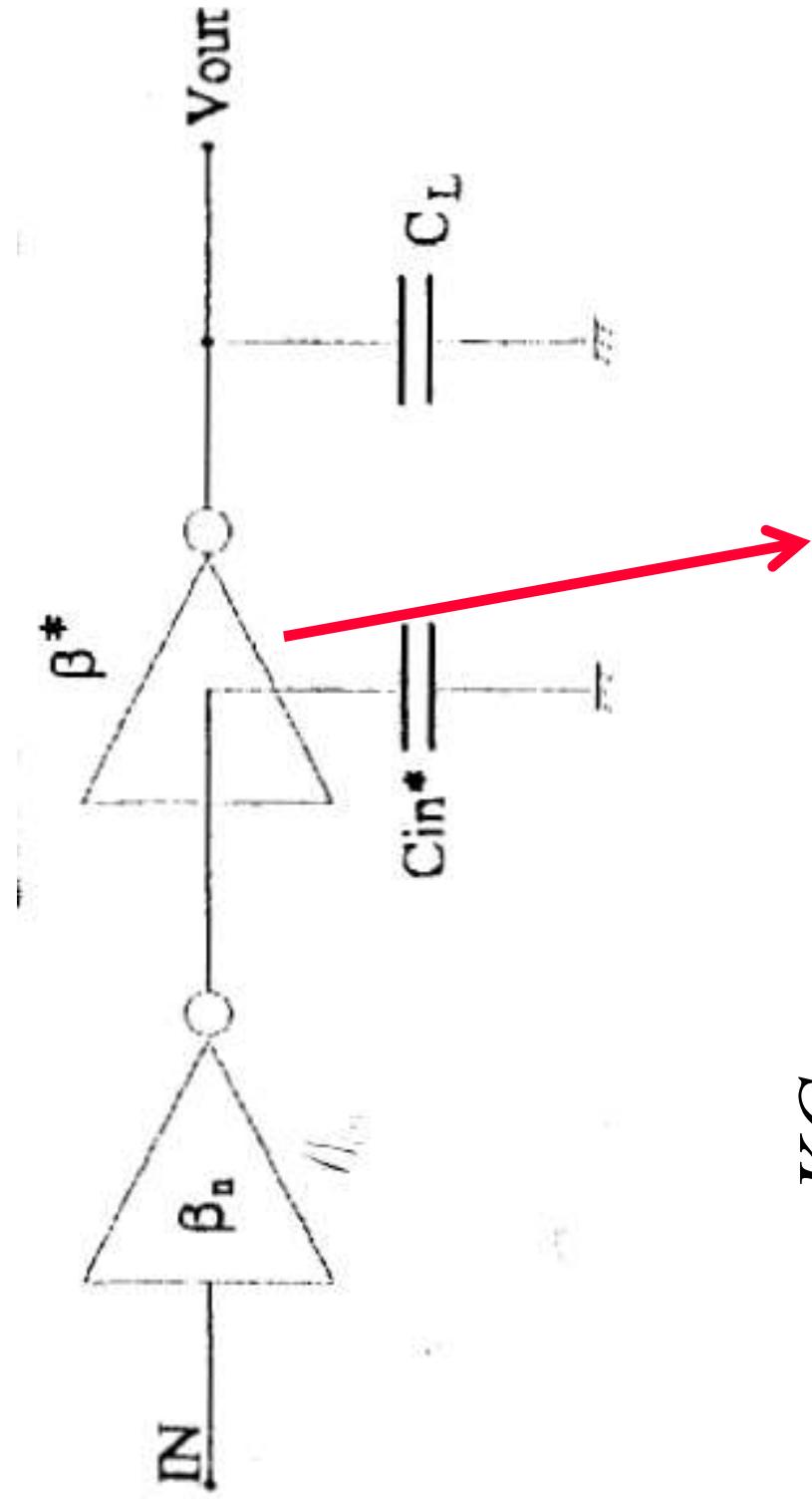
Inverter Chain



$$t_{TOT} \sim t_1 + t_2$$

78

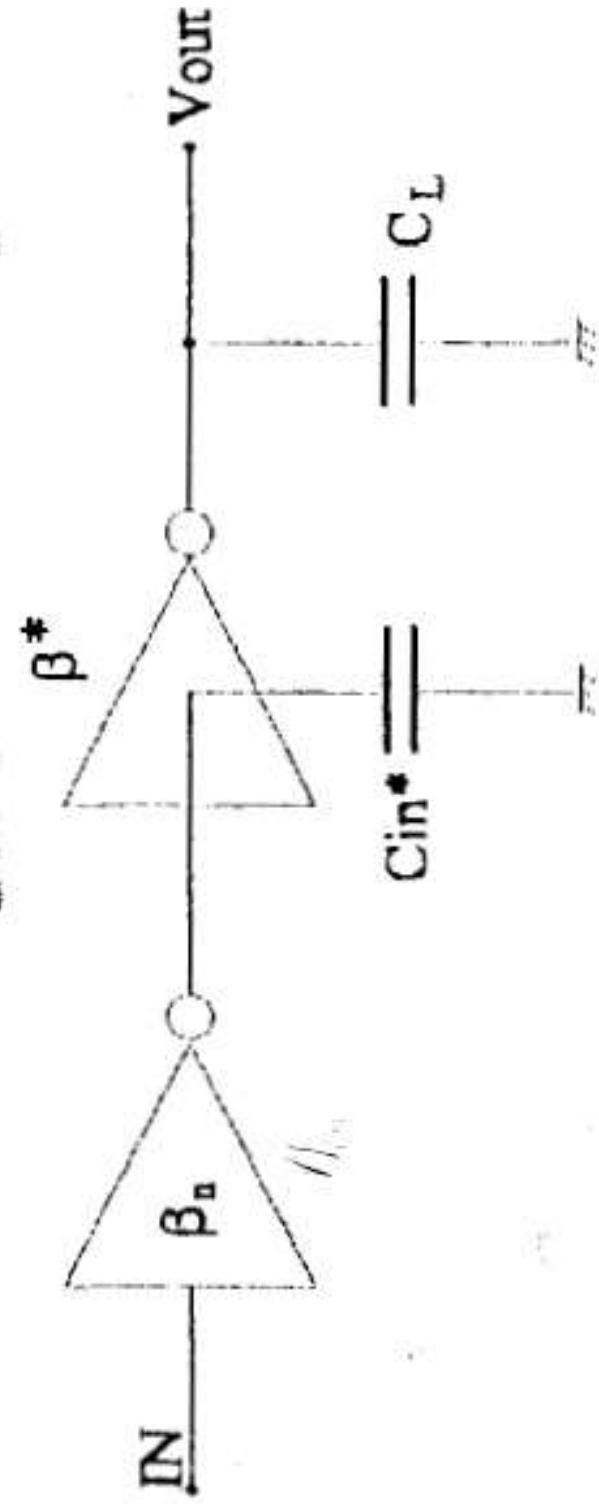
Inverter Chain



$$t_{phl} = t_{plh} = \frac{KC_{in}}{\beta_n}$$

$$\tau = \frac{KC_L}{\beta^*}$$

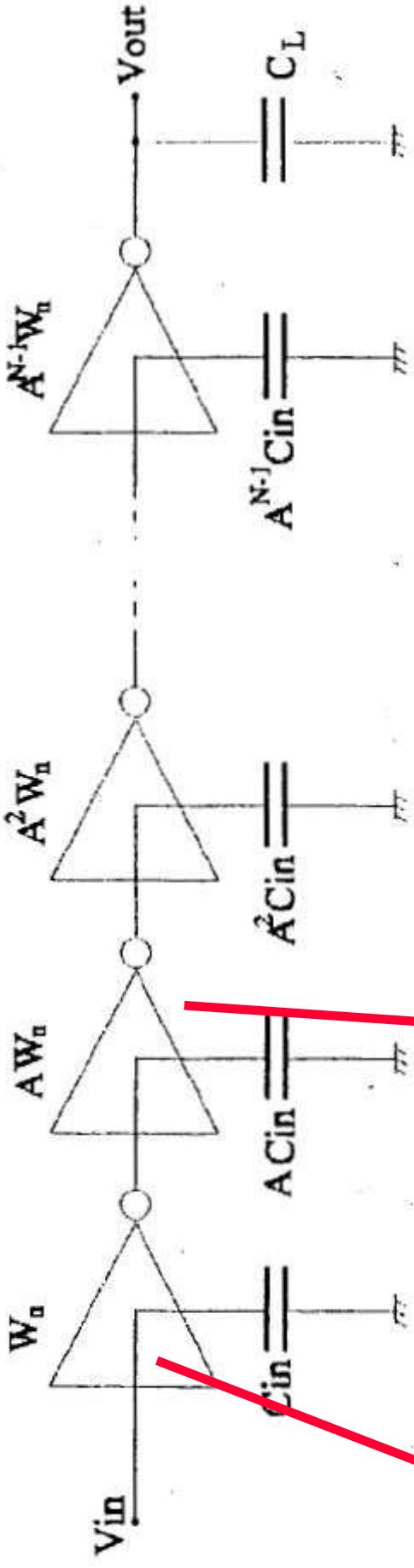
Inverter Chain



$$\tau = \frac{KC_L}{\beta^*} \quad \frac{KC_{in}}{\beta_n} = \frac{KC_L}{\beta^*} \xrightarrow{\beta^*} \beta^* = \frac{C_L \beta_n}{C_{in}} \approx 1000 \beta_n$$

$$W^* = \frac{W_n C_L}{C_{in}} \approx 1000 W_n$$

Inverter Chain



Driving Inverter

$$\tau_1 = K \frac{A C_{in}}{\beta_n} = A \tau_m \quad \tau_2 = K \frac{A^2 C_{in}}{A \beta_n} = A \tau_m = \tau_1$$

$$C_L = A^N C_{in}$$

$$\tau_m = \frac{K C_{in}}{\beta_n}$$

$$\tau_i = K \frac{A^i C_{in}}{A^{i-1} \beta_n} = A \tau_m = \tau_1 \quad \tau_{tot} = N A \tau_m$$

$$\boxed{\tau_{tot} = \frac{A}{\ln A} \tau_m \ln \frac{C_L}{C_{in}}}$$

Inverter Chain

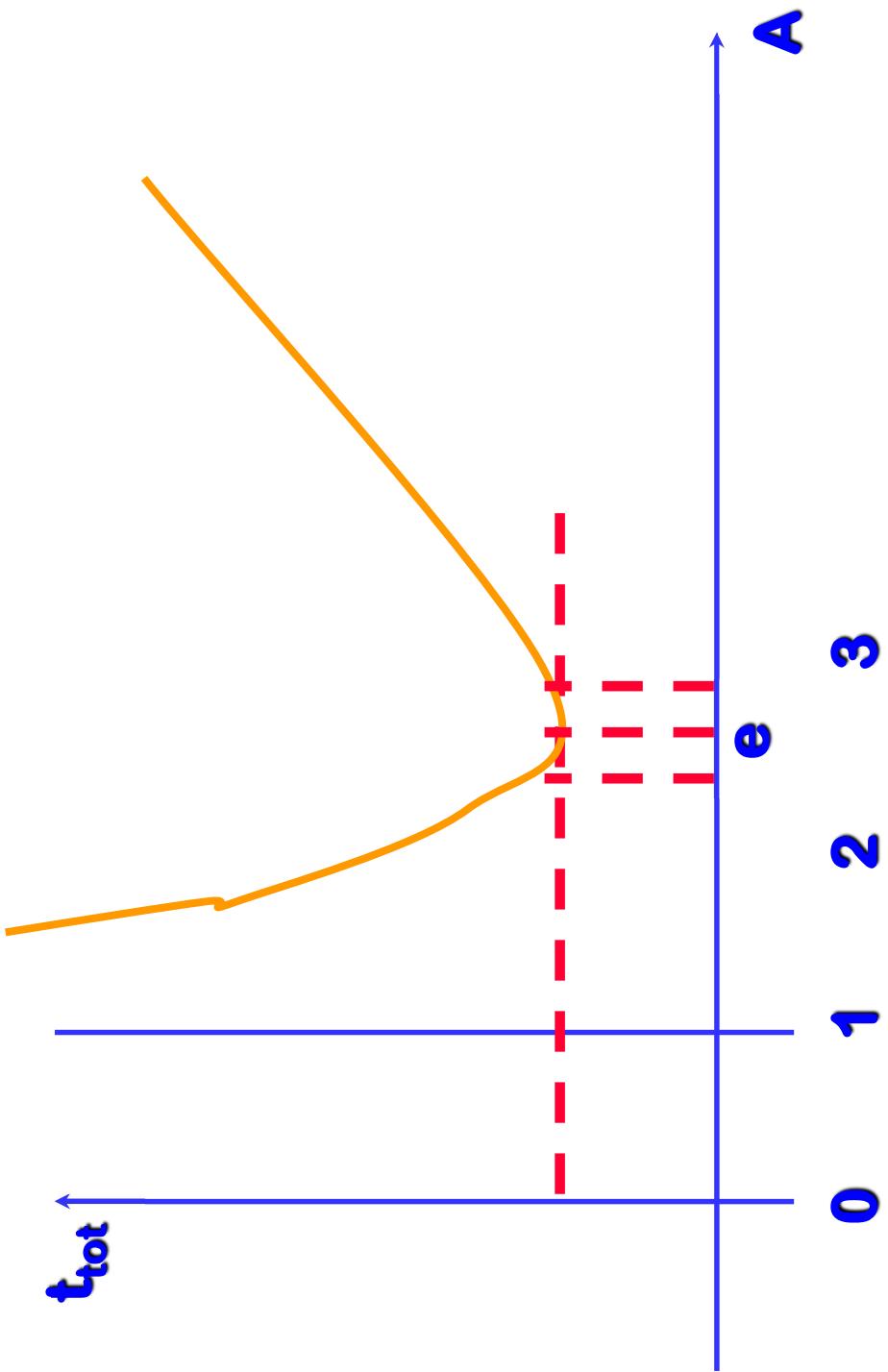
$$\boxed{\tau_{tot} = \frac{A}{\ln A} \tau_m \ln \frac{C_L}{Cin}}$$

$$1 - \ln A = 0 \quad \text{and so} \quad A = e (= 2.71\dots)$$

$$\hat{\tau}_{tot} = \frac{1 - \ln A}{\ln^2 A} \tau_m \ln \frac{C_L}{Cin}$$

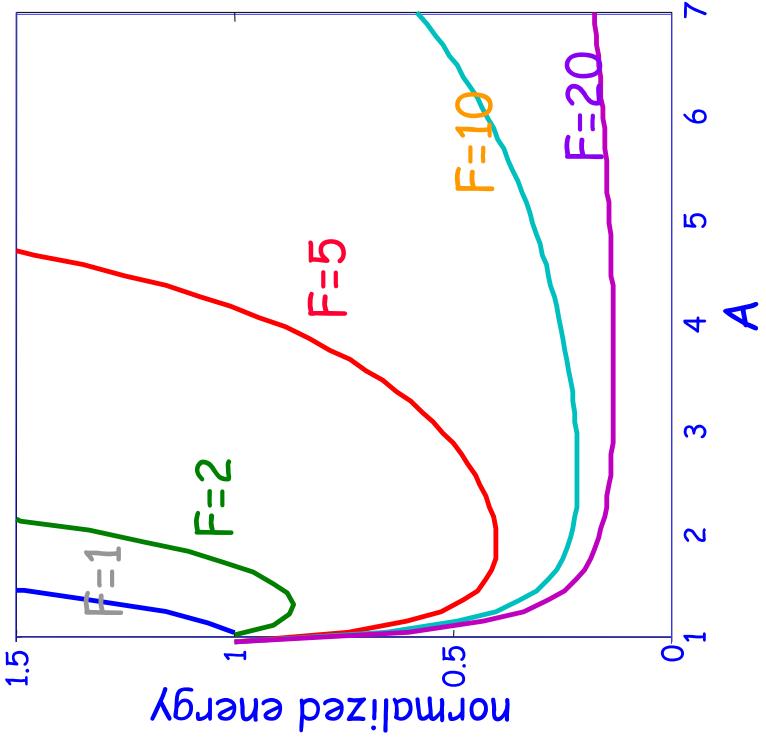
$$\tau_{tot} = 21\tau_m \quad w.r.t.$$

Inverter Chain



Dynamic Power as a Function of Device Size

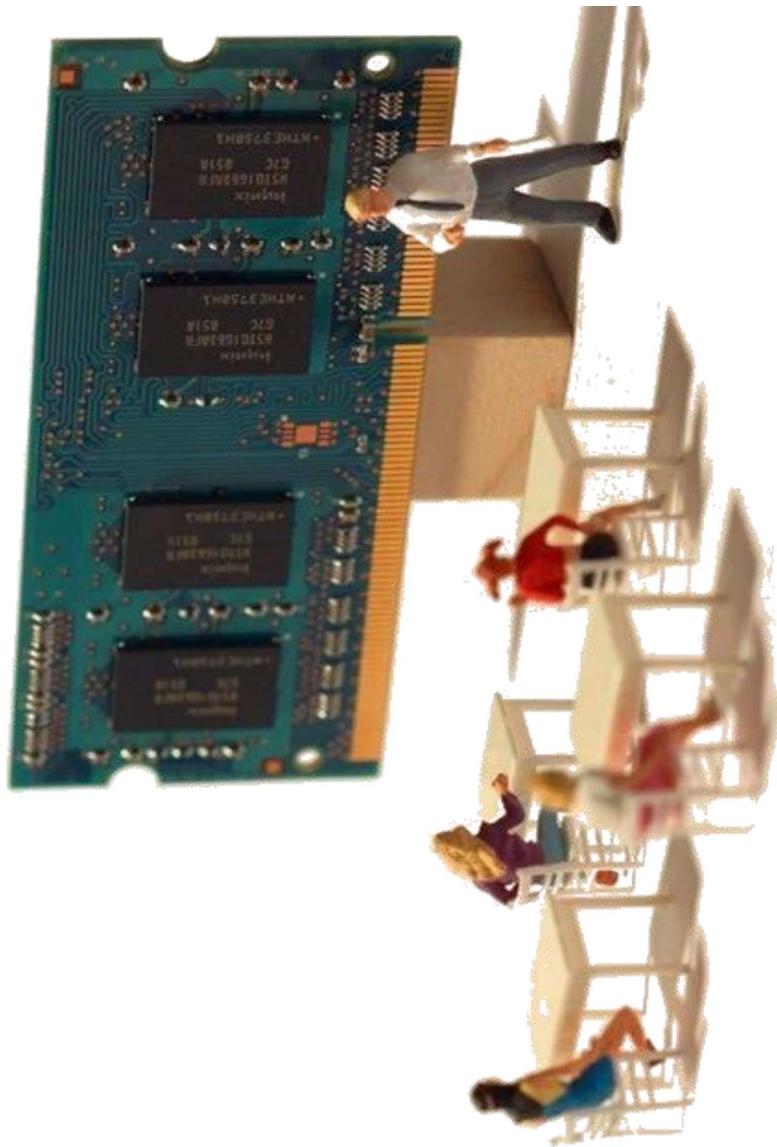
- ❖ Device sizing affects dynamic energy consumption
 - gain is largest for networks with large overall effective fan-outs ($F = C_L/C_{in}$)
- ❖ The optimal gate sizing factor (A) for dynamic energy is smaller than the one for performance, especially for large F 's
 - e.g., for $F=20$,
 $A_{opt}(\text{energy}) = 3.53$ while
 $A_{opt}(\text{performance}) = 4.47$
- ❖ If energy is a concern avoid oversizing beyond the optimal



From Nikolic, UCB

End Inverter Chain Example, Questions ?

- Driving an high value capacitor
- Dynamic Analysis
- Power-Speed Trade-Off



Outline

❖ Review

- Sync. and Async Sequential Logic
- Finite State Machine (MEALY, MOORE, MEALY Rit.)
- ❖ Complementary CMOS Logic

- Synthesis

- Dynamic Analysis

- Examples: NAND, NOR and comparison

- Stick Diagram

- Body Effect

- Standard-cell AMS 0,35 um

❖ Example: Inverter Chain

- Driving an high value capacitor

- Dynamic Analysis

- Power-Speed Trade-Off

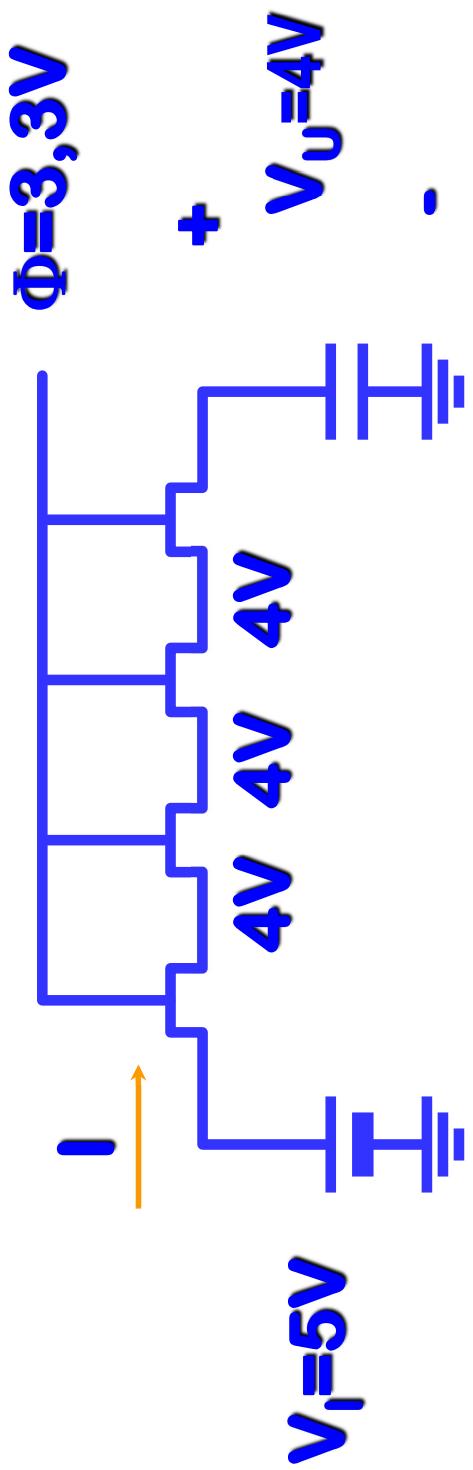
❖ Example: Pass Transistor Chain

- Dynamic Analysis

- Area – Speed Trade-Off

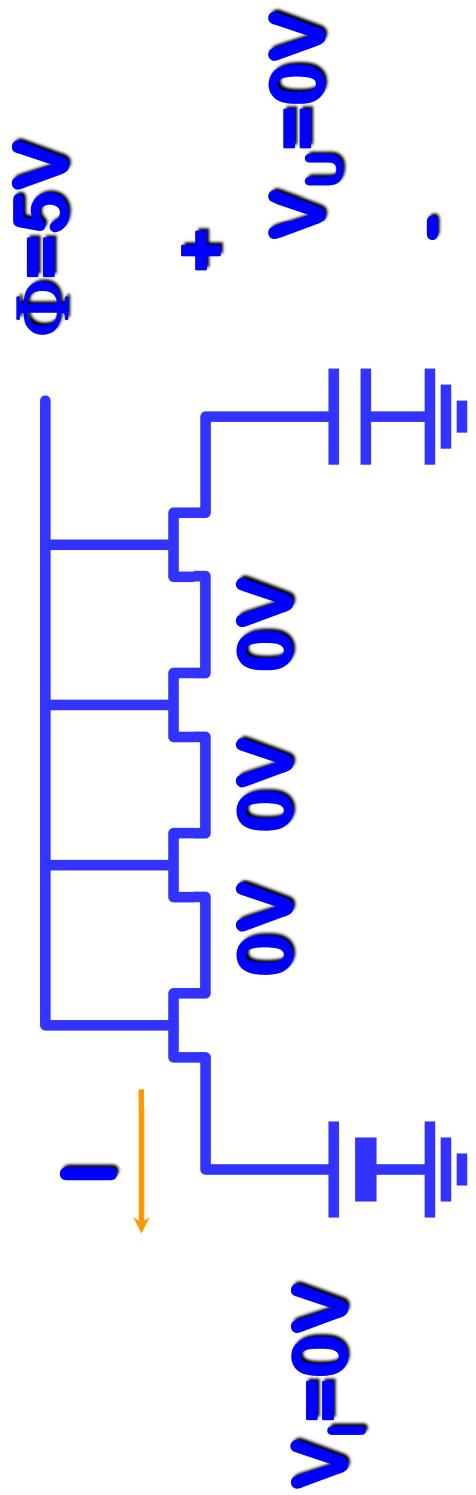
N pass transistor chain

★ Threshold Drop at V_H

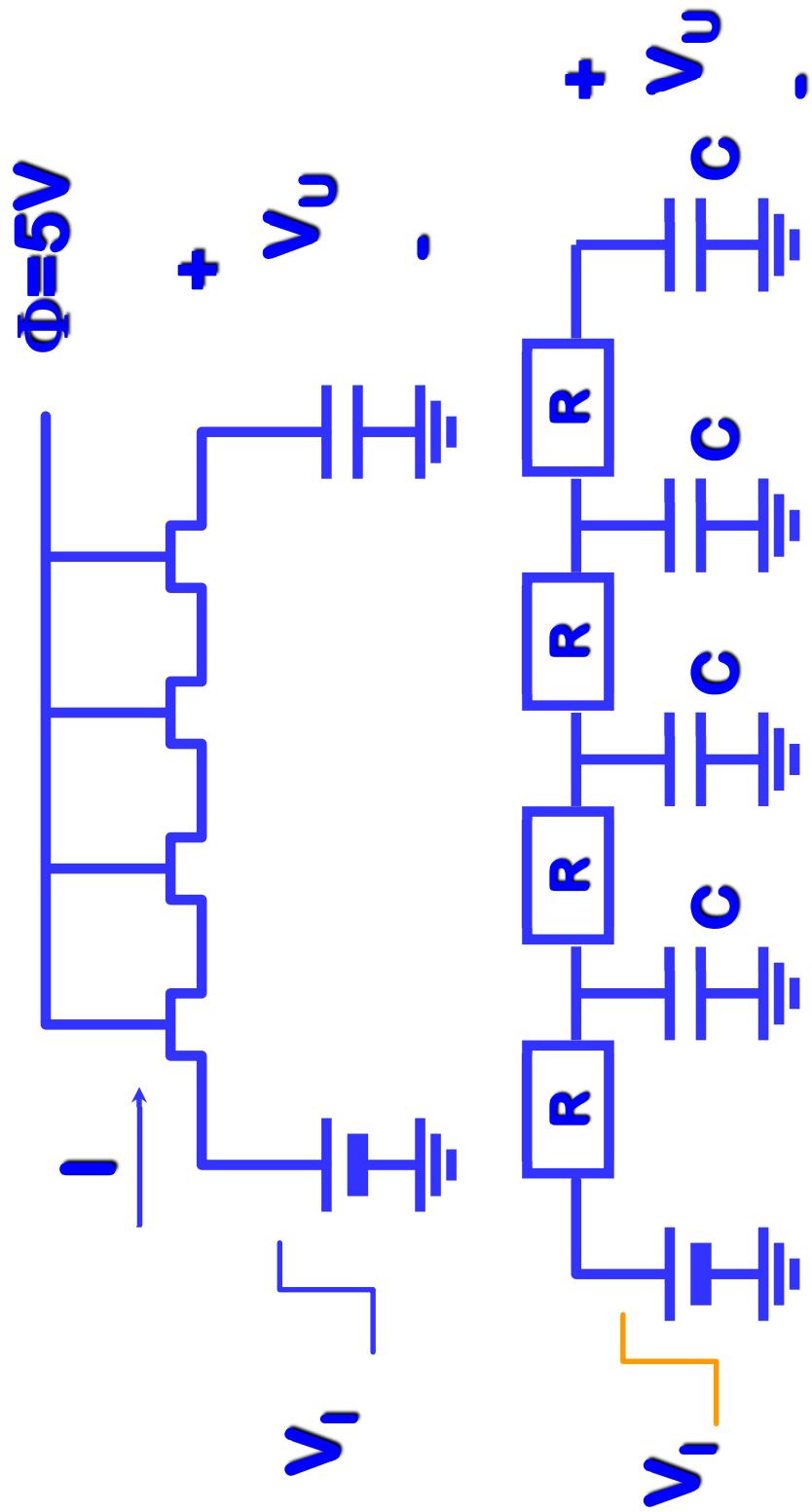


N pass transistor chain

❖ No Threshold Drop at V_L



N pass transistor chain Dynamic Analysis

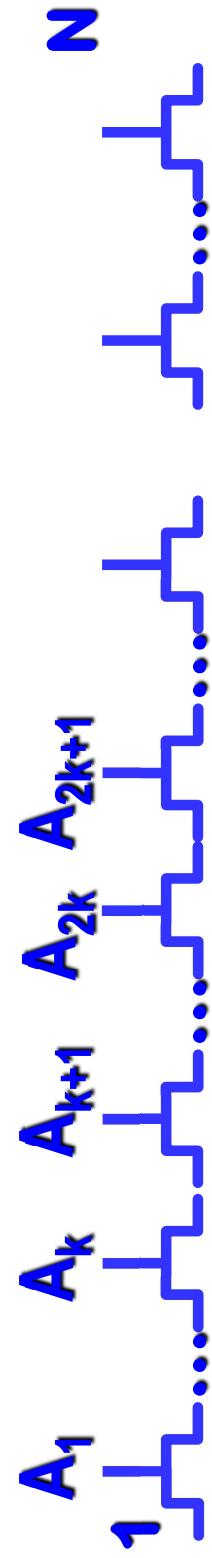


Delay

- ❖ T_p = delay of one R-C cell
- ❖ Overall delay grows with N^2
- ❖ $T_{\text{tot}} = T_p N^2$
- ❖ Overall delay becomes very high just after few pass transistors

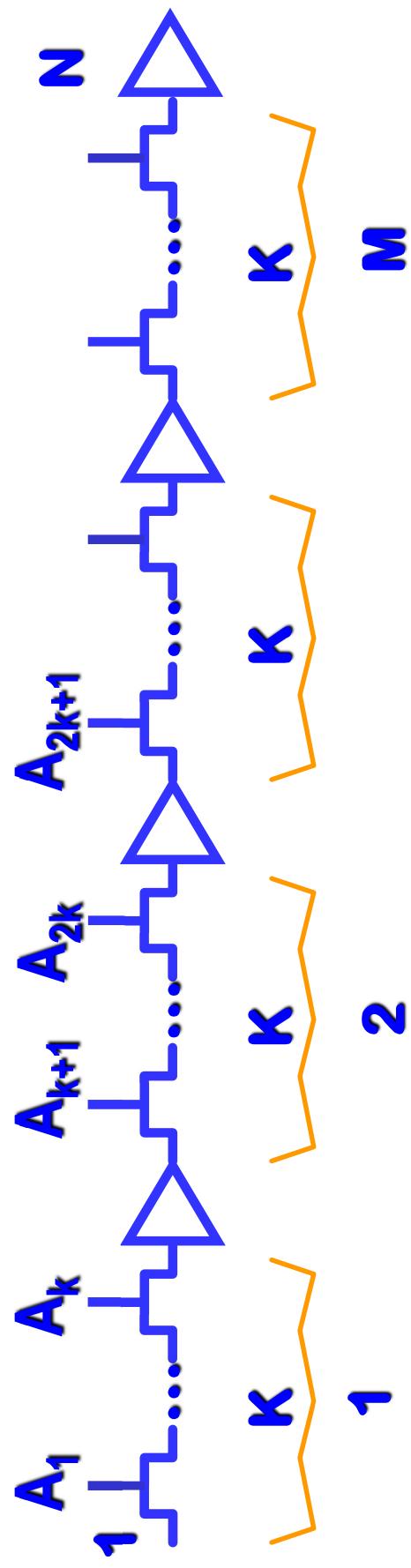
Delay Optimization

- Note:
 - Delay in a buffer chain grows linearly
- Solution
 - Introduce buffers in the pass transistor chain
- Let's consider a N pass transistor chain with « N » elements



Circuit Solution

- T_P = pass transistor delay
- T_B = buffer delay
- M groups made by K pass transistors



Analysis

$$N = K \bullet M; \quad M = \frac{N}{K}$$

$$T_{tot} = MT_B + M(K^2 T_P) = \frac{N}{K} T_B + \frac{N}{K} (K^2 T_P) = \frac{N}{K} T_B + NKT_P$$

$$\frac{dT_{tot}}{dK} = -\frac{N}{K^2} T_B + NT_P = 0$$

$$K = \sqrt{\frac{T_B}{T_P}}$$

Example

♦ Example: 16 Bit Manchester Carry Adder

$$N = 16 \quad T_B = 4nS \quad T_P = 0,2nS$$

$$K = \sqrt{\frac{T_B}{T_P}} = \frac{4,47}{4} \Rightarrow 4 \Rightarrow M = 16 : 4 = 4$$

$$T_{tot} = 4T_B + 4(16T_P) = 28,8nS$$

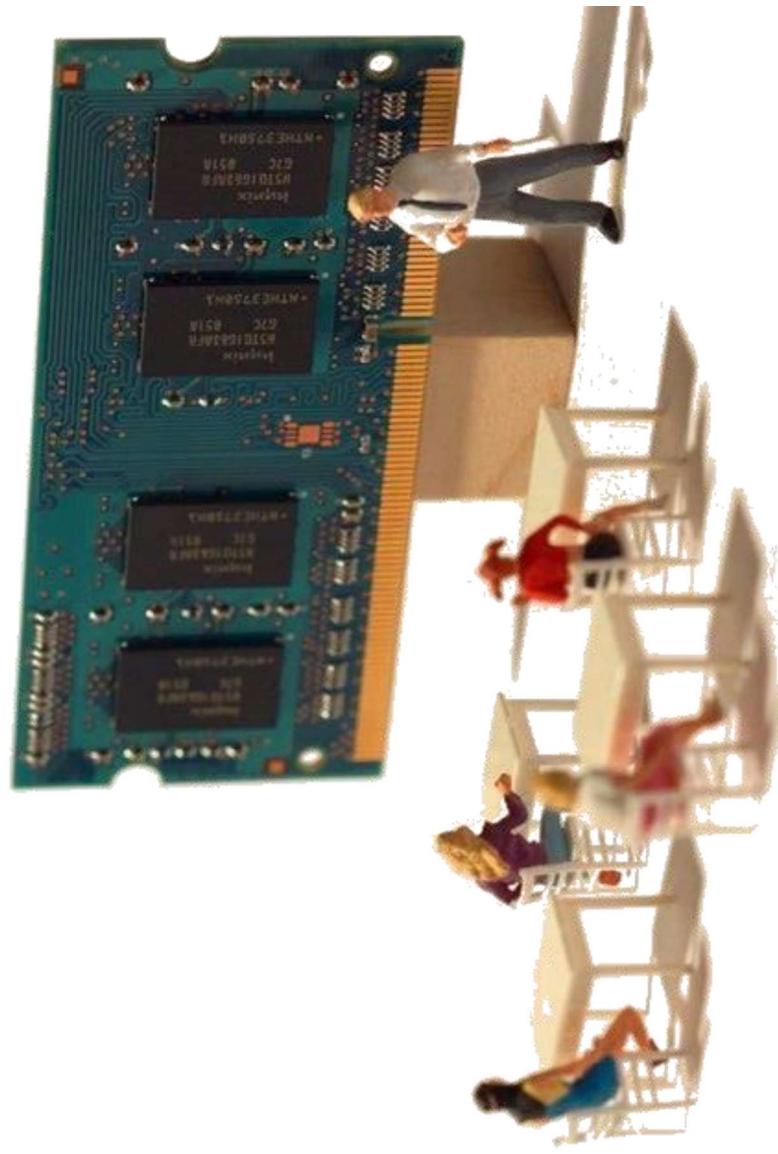
$$w.r.t. \quad N^2 T_P = 51,2nS$$

Pass Gate Chain

- ❖ No Threshold drop
- ❖ Pass gate delay is lower than pass transistor one
- ❖ Delay optimization works as just shown for the pass transistor chain

End Pass Transistor Chain Example, Questions ?

- Dynamic Analysis
- Area - Speed Trade-Off



End, Questions ?

- Review
 - Sync. and Async Sequential Logic
 - Finite State Machine (MEALY, MOORE, MEALY Rit.)
- Complementary CMOS Logic
 - Synthesis
 - Dynamic Analysis
 - Examples: NAND, NOR and comparison
 - Stick Diagram
 - Body Effect
 - Standard-cell AMS 0,35 um
- Example: Inverter Chain
 - Driving an high value capacitor
 - Dynamic Analysis
 - Power-Speed Trade-Off
- Example: Pass Transistor Chain
 - Dynamic Analysis
 - Area - Speed Trade-Off

