

# **Electronics and Communication Systems**

## **Electronics Systems**

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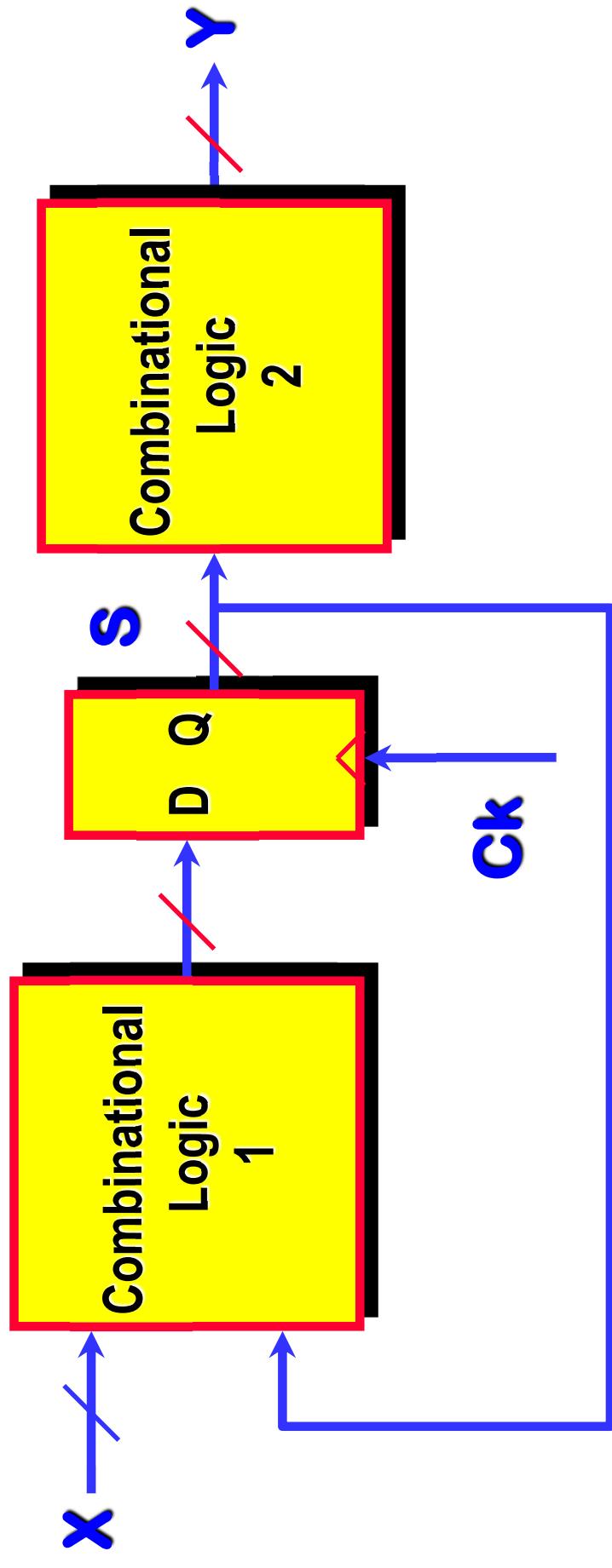
Email: luca.fanucci@unipi.it

# Outline

- ❖ **Flip Flop: Static Solution**
  - **Flip-Flop S-R: NOR2 e NAND2**
  - **Flip-Flop S-R with enable**
  - **D-Latch**
  - **Flip Flop S-R Edge Triggered: NOR2, NAND2**
  - **Flip Flop D Edge Triggered: NOR2, NAND2, MUX**
  - **Flip Flop D Edge Triggered based on pass gate**
- ❖ **Flip Flop: Dynamic Solution**
  - **Flip Flop D Edge Triggered**
  - **Shift Register**

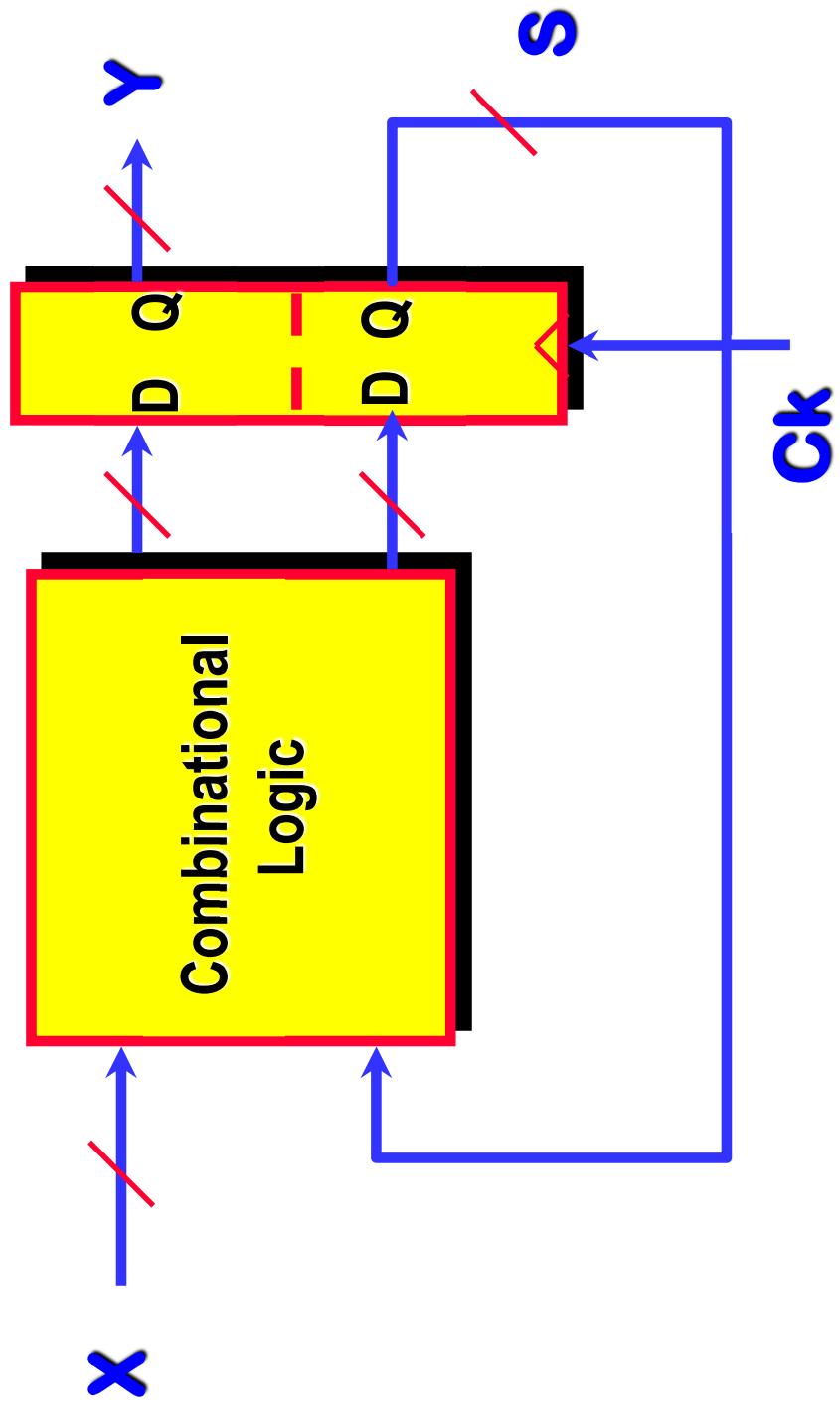
# MOORE Machine

★ Block diagram



# Modified MEALY machine

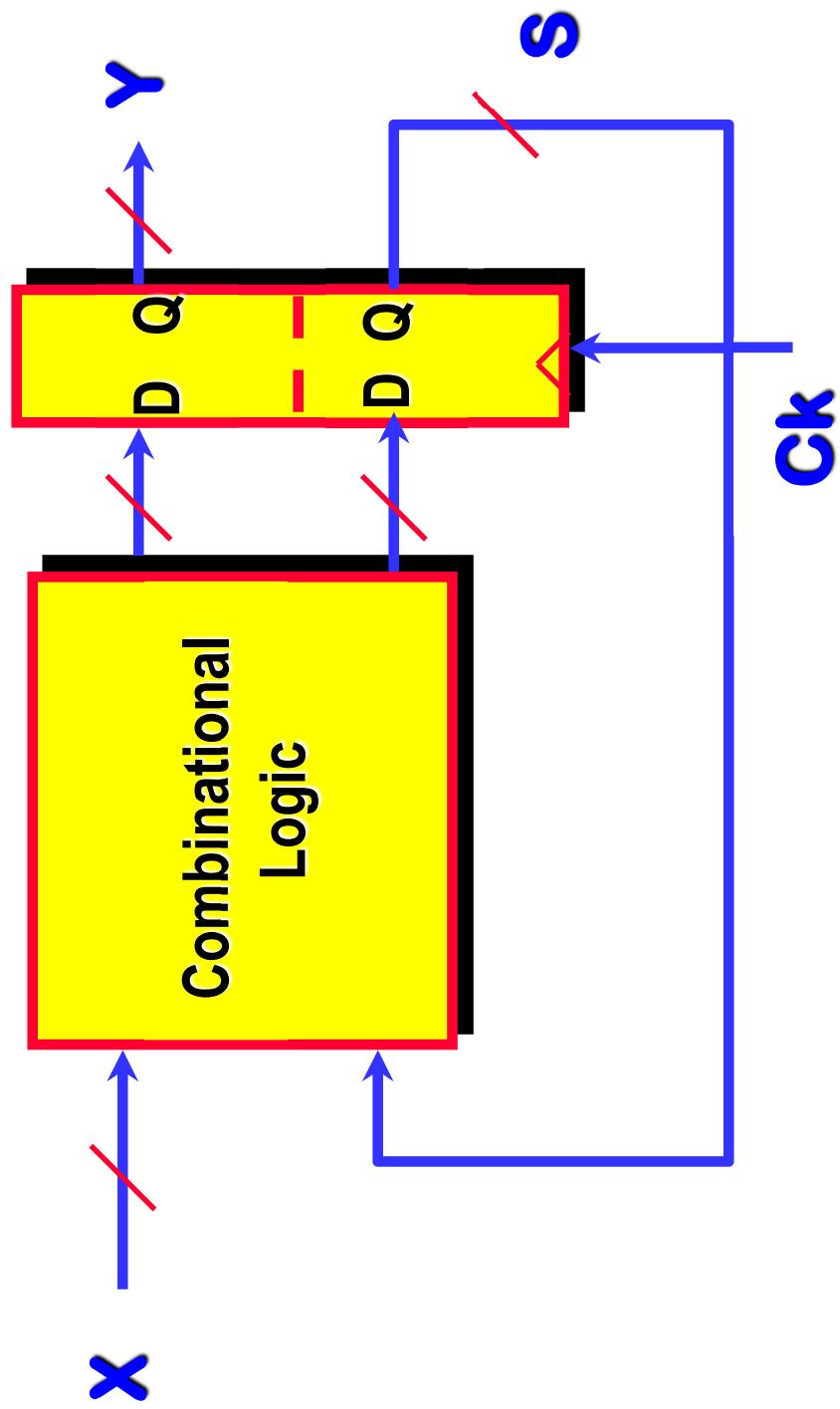
★ Block Diagram



# Finite State Machine: Basic Elements

## Combinational Logic

## Memory Element (Flip Flop D edge triggered)



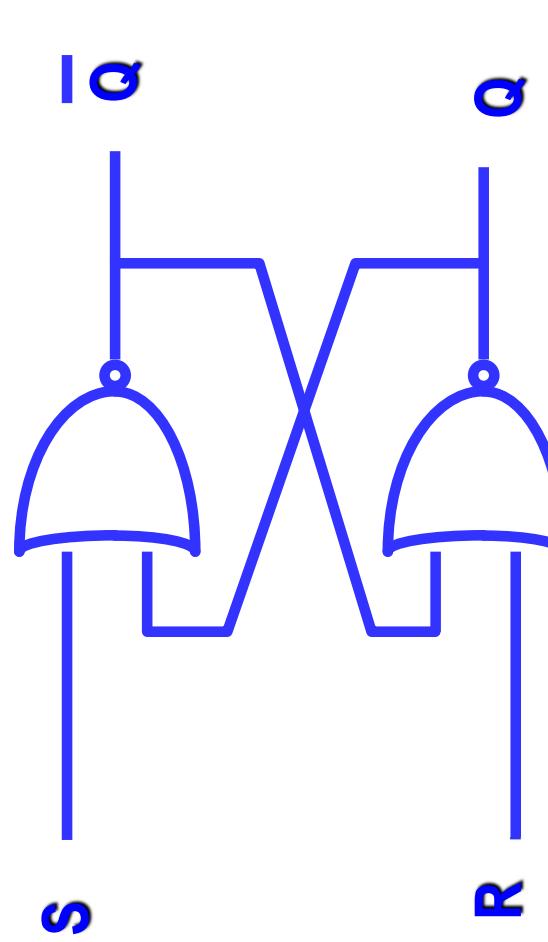
# Flip - Flop

# NOR2 BASED

Truth Table

R	S	$\bar{Q}$	Q
0	0	0	0
1	0	1	1
0	1	1	0
1	1	0	1
...			

Logic Scheme



		NOR
A	B	
0	0	1
0	1	0
1	0	0
1	1	0

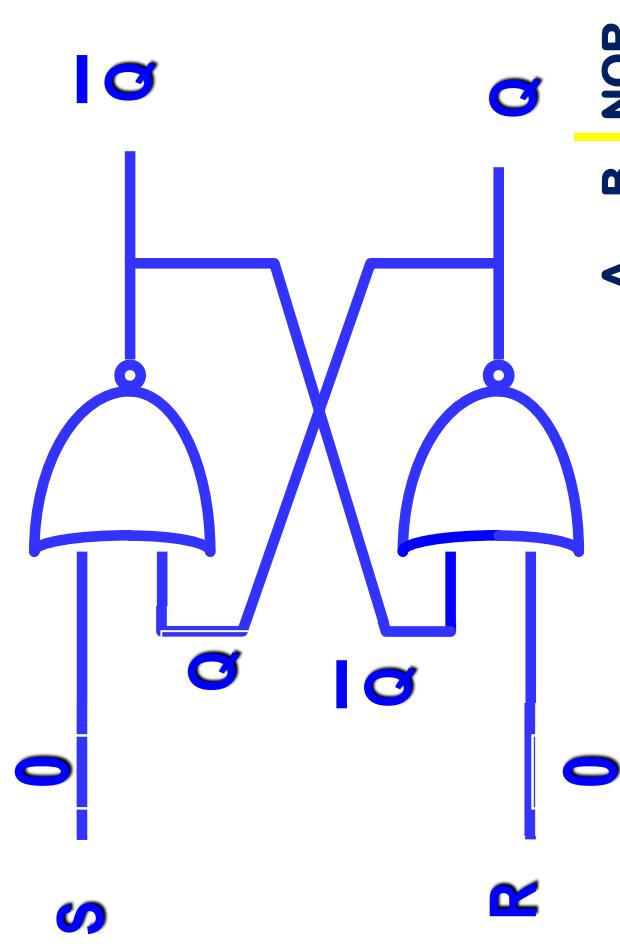
# Flip - Flop

## NOR2 BASED

Truth Table

R	S	$\bar{Q}$	Q
0	0	1	0
1	0	0	1
0	1	1	0
1	1	0	1
...			

Logic Scheme



		NOR
A	B	
0	0	1
0	1	0
1	0	0
1	1	0

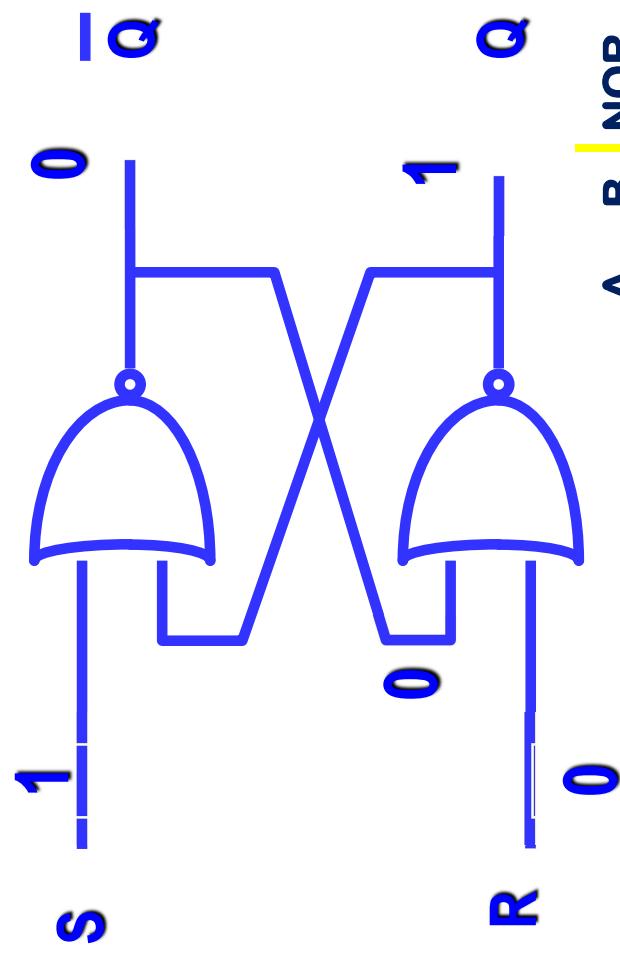
# Flip - Flop

## NOR2 BASED

Truth Table

R	S	Q	$\bar{Q}$
0	0	0	1
1	0	0	1
0	1	1	0
1	1	1	0
...			

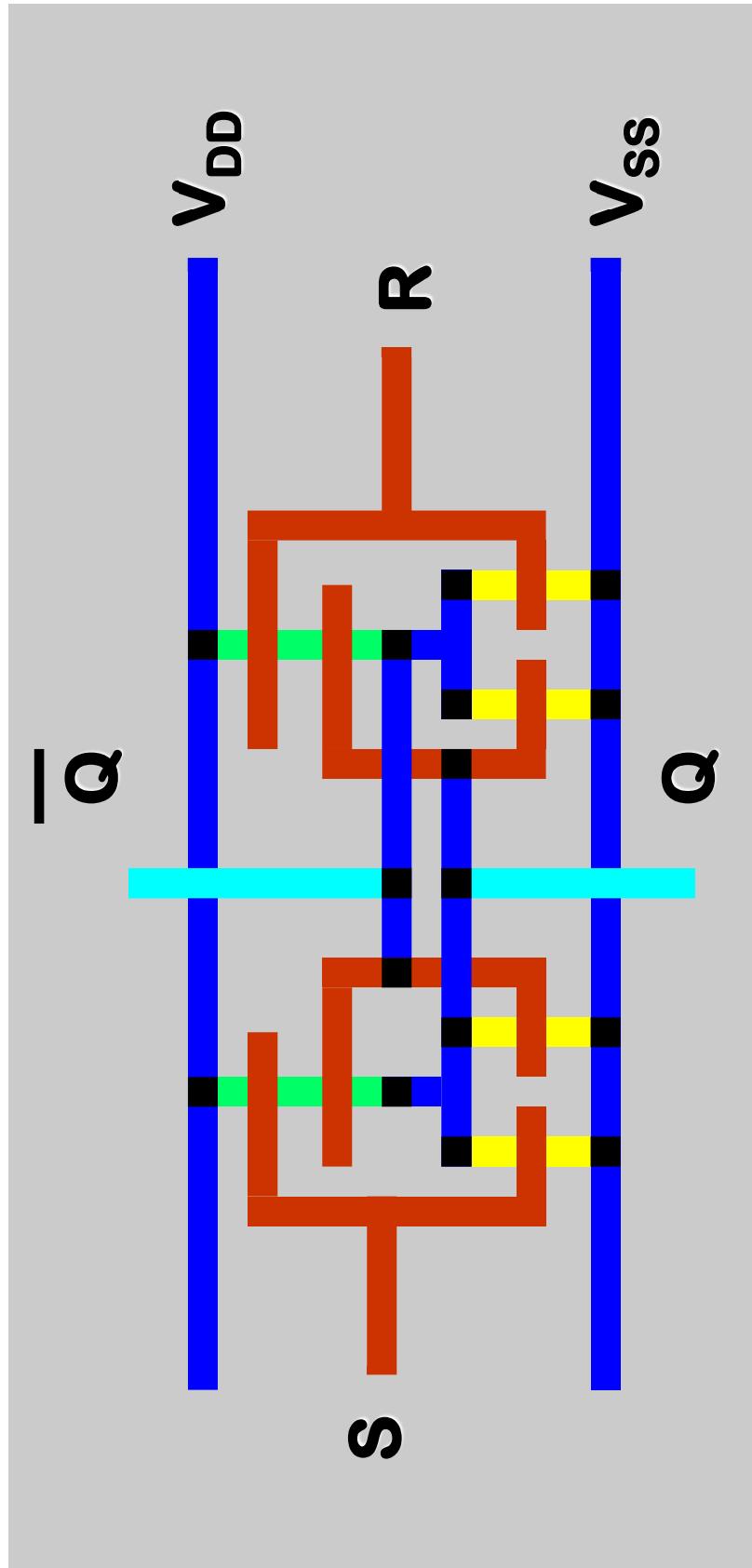
Logic Scheme



		NOR
A	B	
0	0	1
0	1	0
1	0	0
1	1	0

# Stick Diagram FF SR (NOR2)

★ Number of Transistors = 8



# Flip - Flop

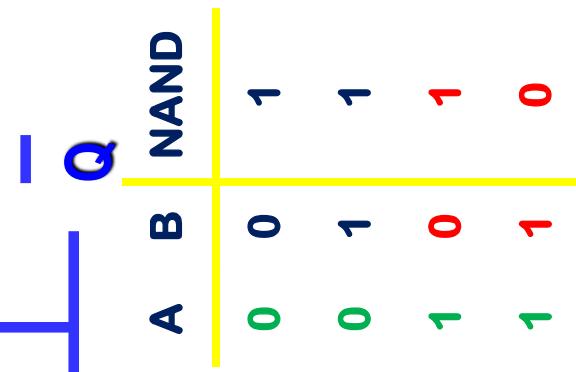
## $S - R$

## NAND2 BASED

Truth Table

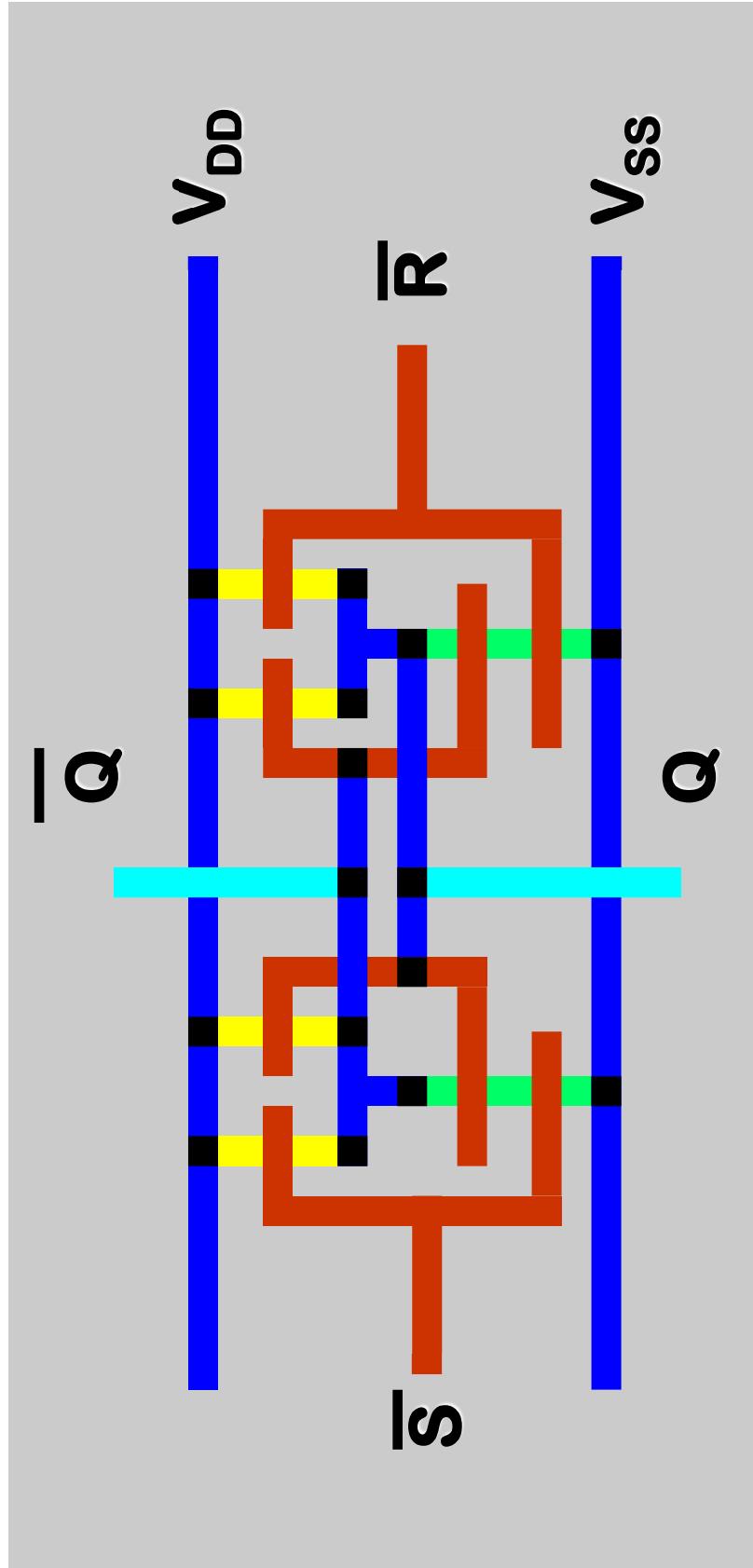
$S$	$R$	$\bar{S}$	$\bar{R}$	$Q$	$\bar{Q}$	$Q$	$\bar{Q}$
1	1	0	0	0	1	0	1
1	0	0	1	1	0	1	0
0	1	1	0	0	1	1	0
0	0	1	1	1	0	0	1
.....							

Logic Scheme



# Lay-Out simbolico FF SR (NAND2)

✿ Number of Transistors = 8 + 4 (for  $\bar{S}$  and  $\bar{R}$ )



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  - **Flip Flop S-R Edge Triggered: NOR2, NAND2**
  - **Flip Flop D Edge Triggered: NOR2, NAND2, MUX**
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- ❖ **Flip Flop: Dynamic Solution**
  - **Flip Flop D Edge Triggered**
  - **Shift Register**

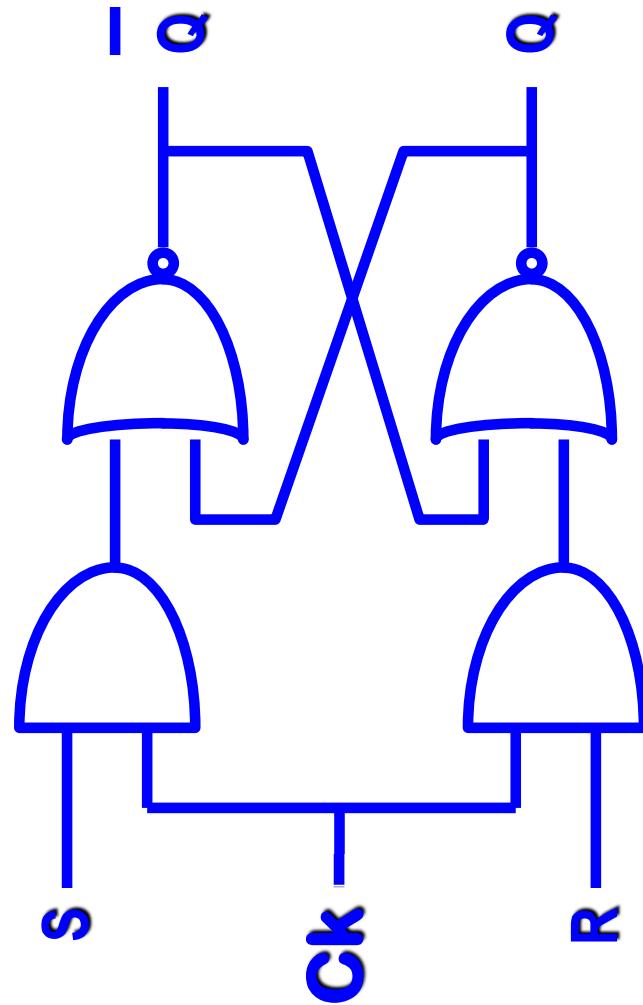
# FLIP - FLOP

# S - R with clock

Truth Table

S	R	Ck	$\bar{Q}$	Q
x	x	0	1	1
0	0	1	0	1
1	0	1	1	0

Logic Scheme



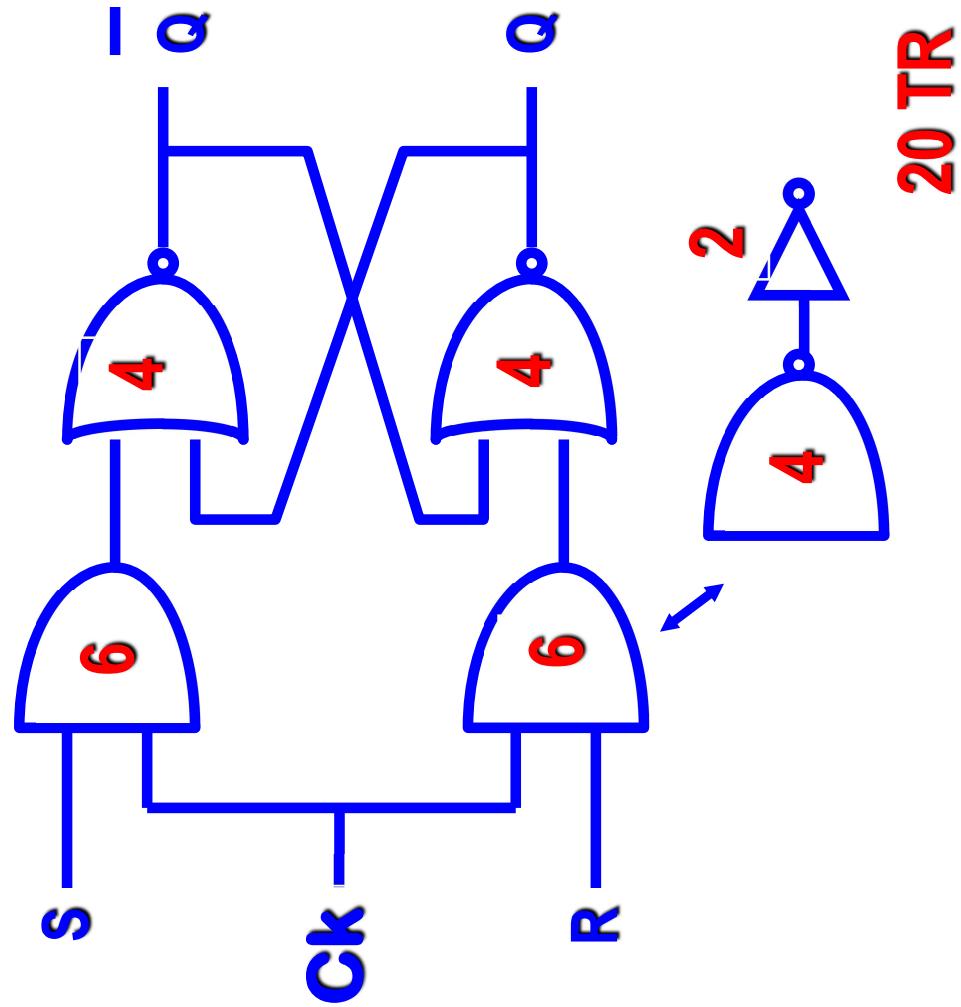
# FLIP - FLOP

# S - R with clock

Truth Table

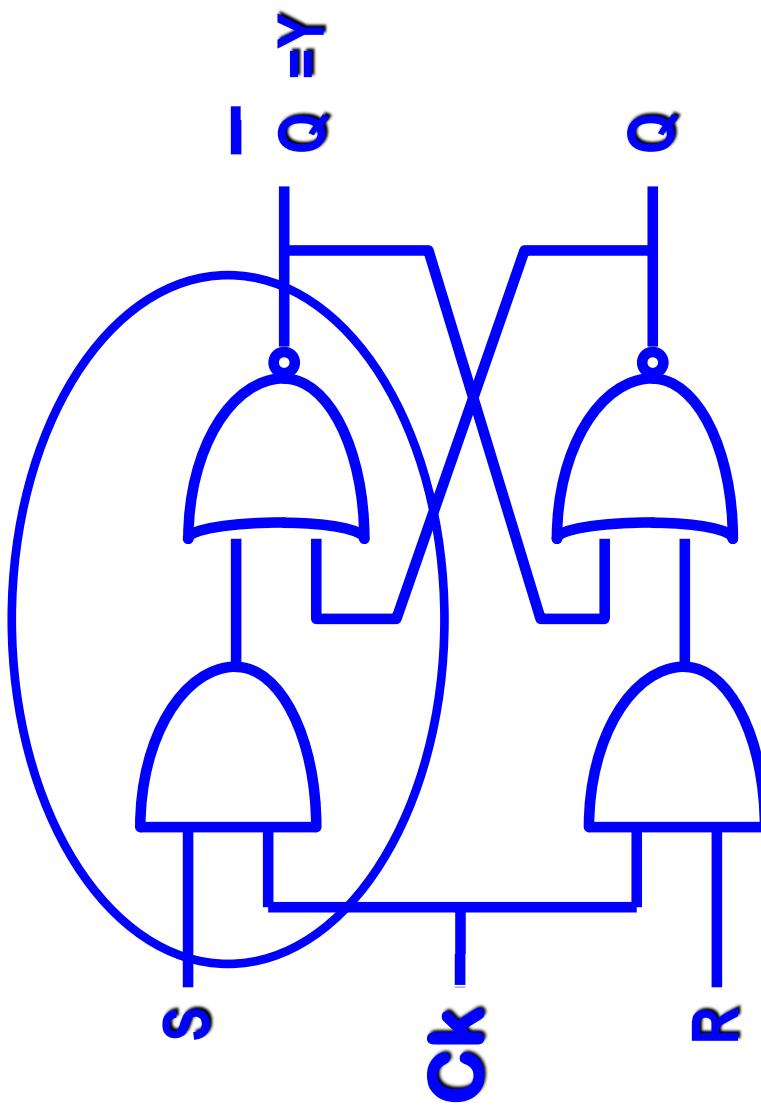
S	R	Ck	$\bar{Q}$	Q
X	X	0	Q	$\bar{Q}$
0	0	1	1	0
1	0	1	0	1

Logic Scheme



# FLIP - FLOP

# S - R con clock

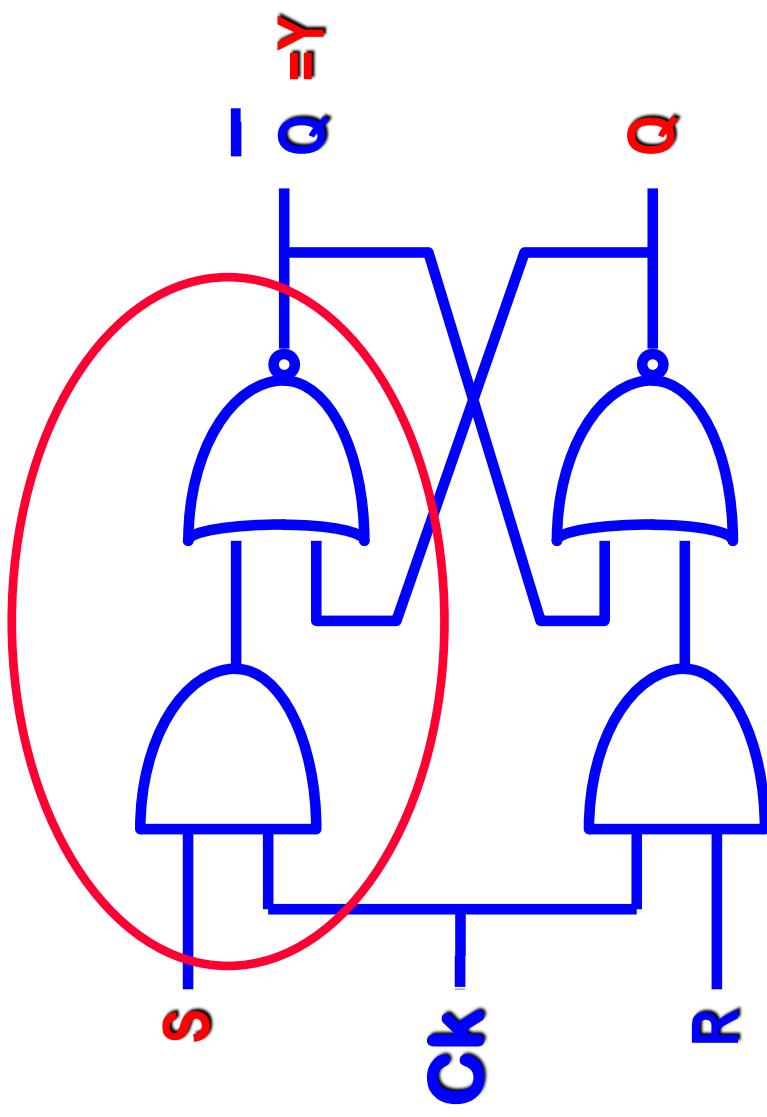


$$\bar{Y} = \bar{Q} = S \cdot \bar{\text{CK}} + Q$$

# **FLIP - FLOP**

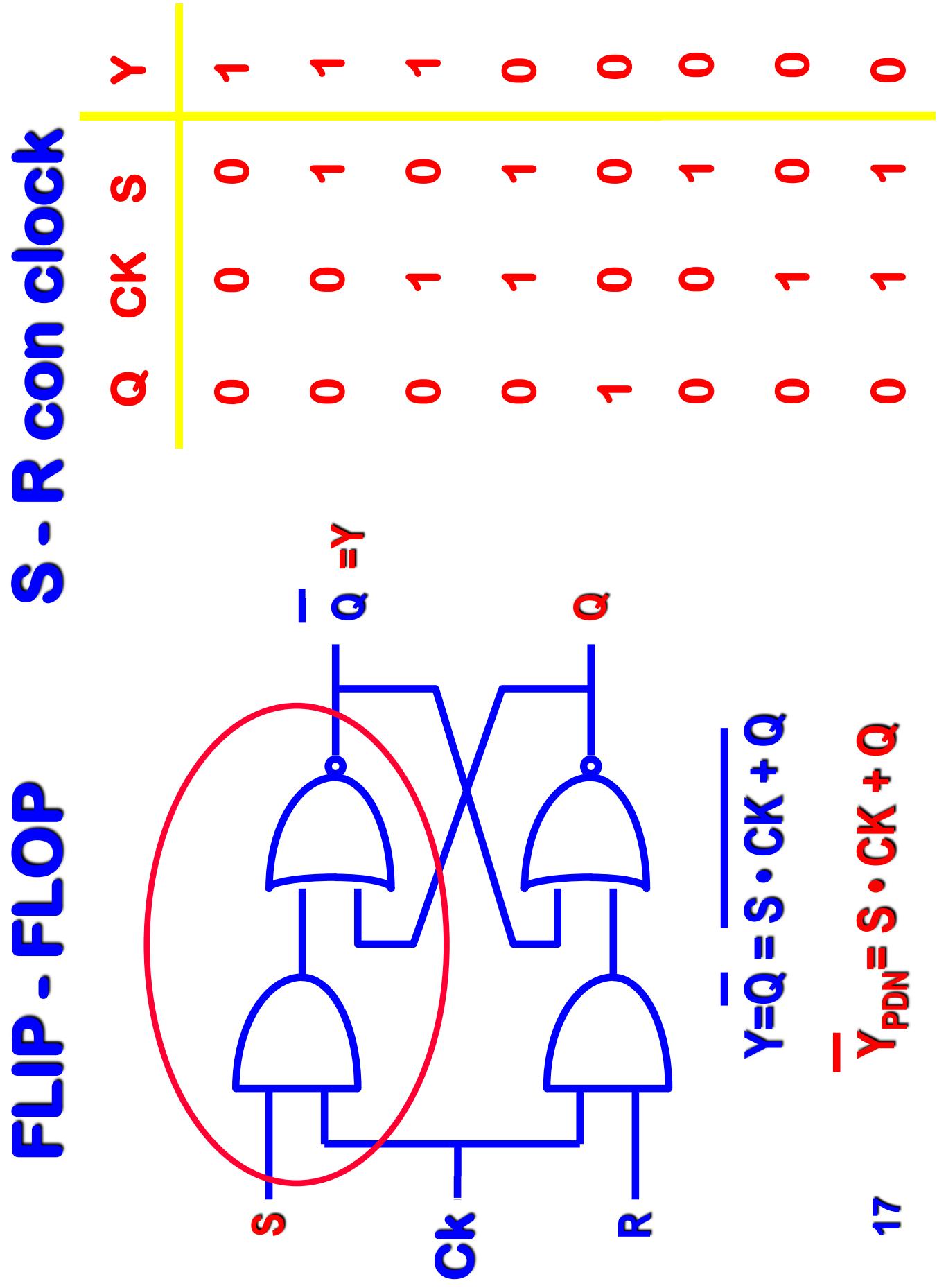
## **S - R con clock**

$y$	1	1	1	0	0	0	0	0
$s$	0	1	0	1	0	1	0	1
$c_k$	0	0	1	1	0	0	1	1
$Q$	0	0	0	0	1	0	0	0



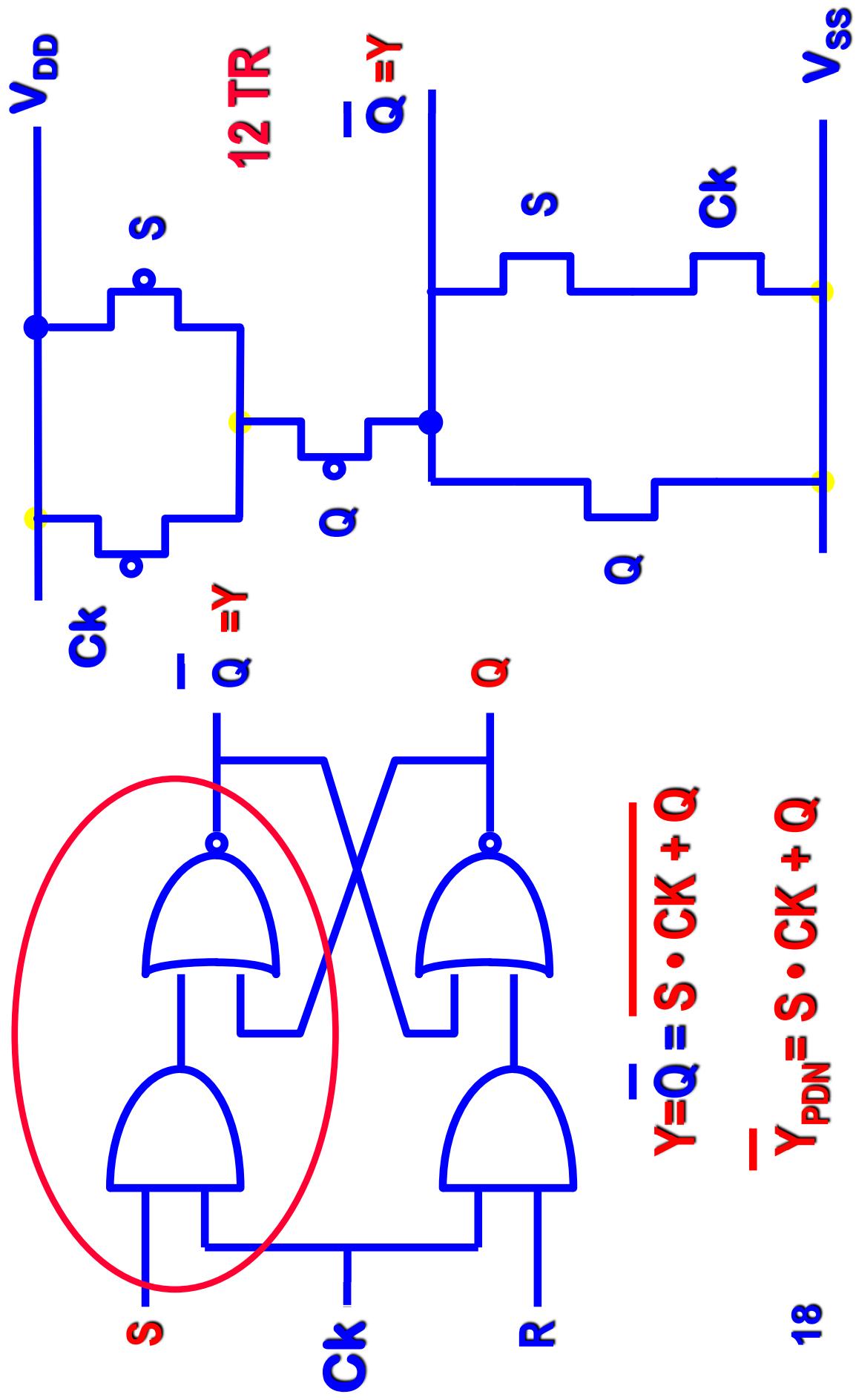
$$Y = Q = S \cdot CK + Q$$

# FLIP - FLOP



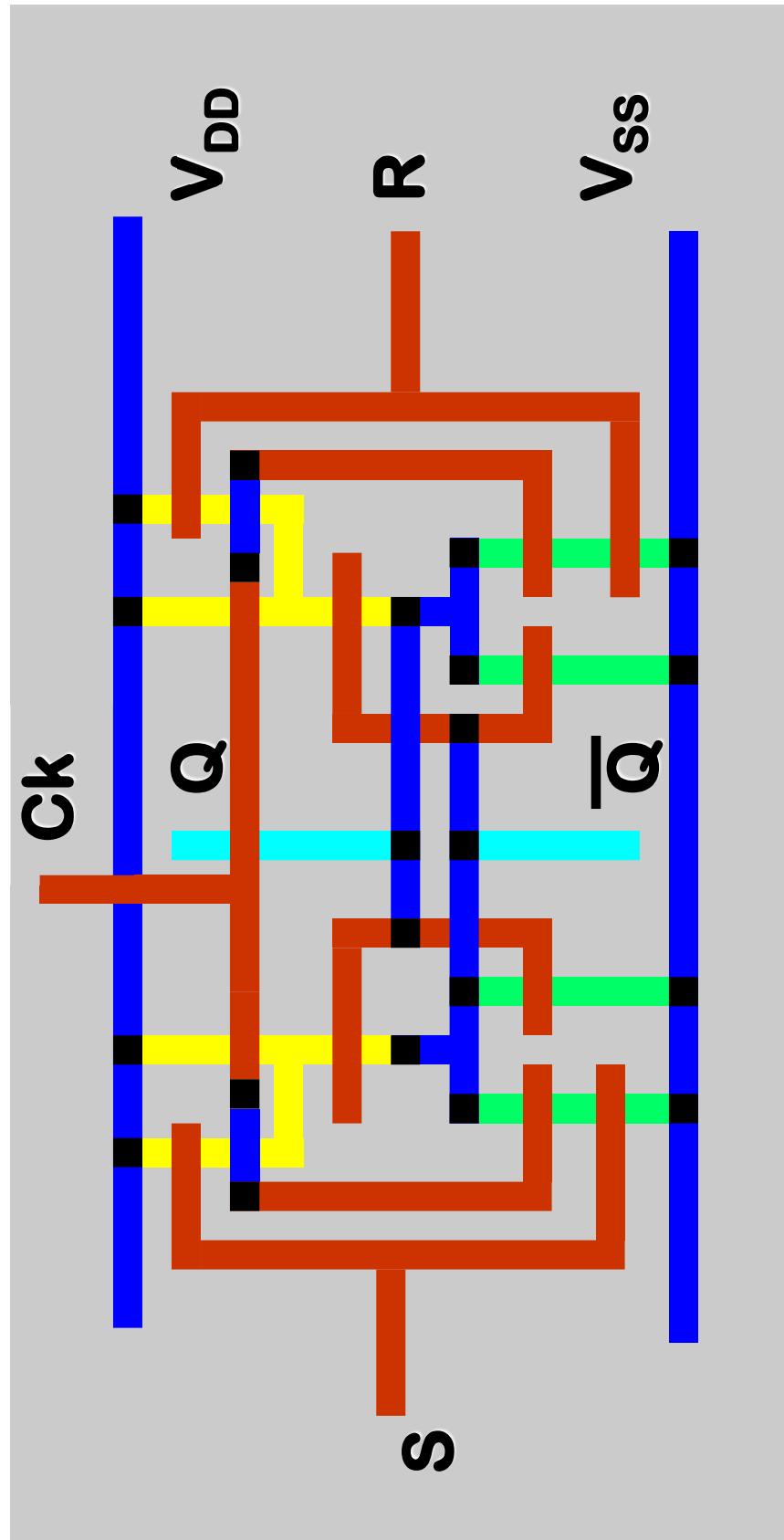
# FLIP - FLOP

## S - R con clock



# Stick Diagram

Number of Transistors = 12



**Latch**

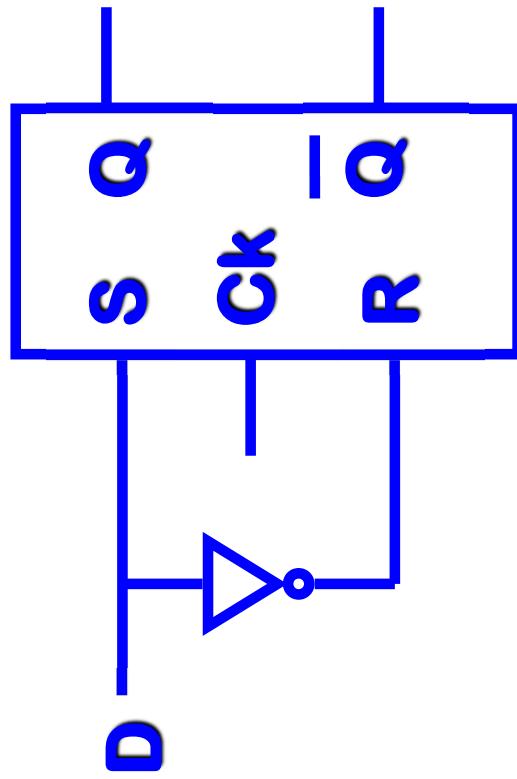
**D**

**Truth Table**

D	Ck	Q	Q
X	1	0	0
	0	0	1
	1	1	0

**Logic Scheme**

**14 transistors**

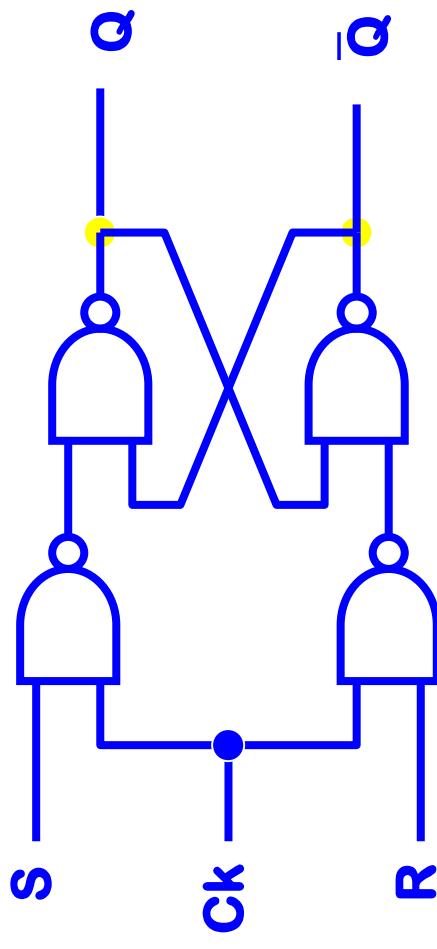


# FF SR (NAND2) with clock

❖ Truth Table

Logic Scheme

Ck	S	R	Q
0	x	x	Q
1	0	0	Q
1	0	1	0
1	1	0	1
1	1	1	-



NAND	
A	B
0	0
0	1
1	0
1	1

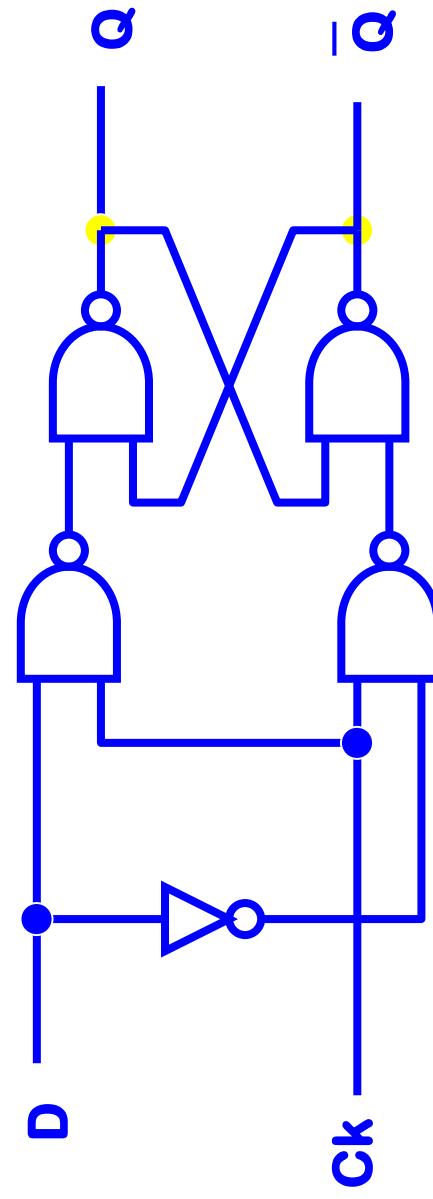
Number of Transistors = 16

# Outline

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- ❖ **Flip Flop: Dynamic Solution**
  - **Flip Flop D Edge Triggered**
  - **Shift Register**

# Flip – Flop D

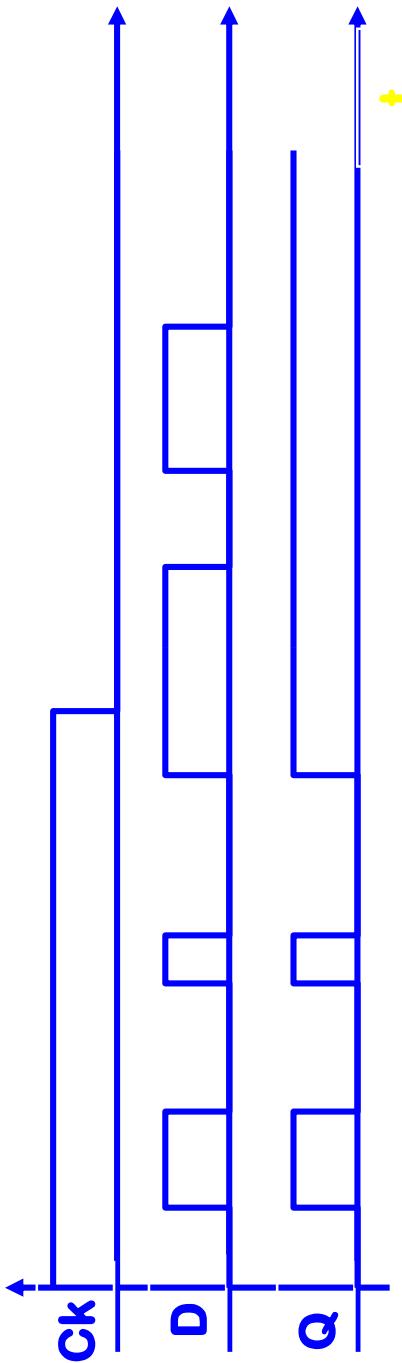
- ❖  $Ck = 1$ 
  - Output Q follows input D
- ❖  $Ck = 0$ 
  - Output maintains previous value
- ❖ Number of Transistors = 18
- ❖ Truth Table
- ❖ Logic Scheme



Ck	D	Q
0	x	Q
1	0	0
1	1	1

# Notes

❖ When Clock is 1 Output Q follows input D



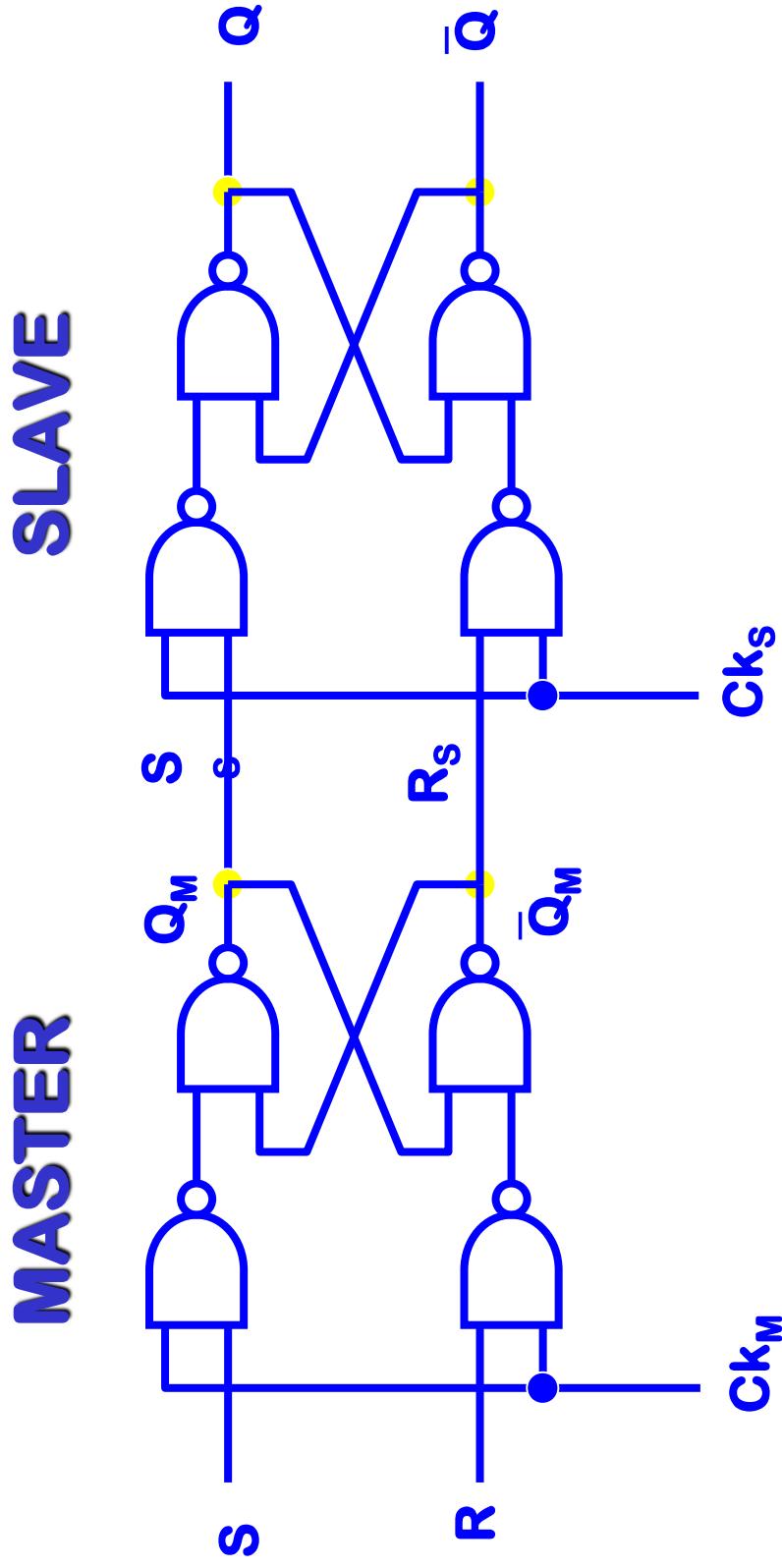
❖ Flip- Flop is “TRANSPARENT”

❖ Symbol

The symbol for a flip-flop is a red rectangle with four terminals. The 'D' terminal is on the left, 'Q' is on the top right, 'Ck' is on the bottom right, and a fourth terminal is at the bottom left.

- Sensitive to high CK level !!
- Data is stored when CK changes from 1 to 0

# MASTER – SLAVE Architecture

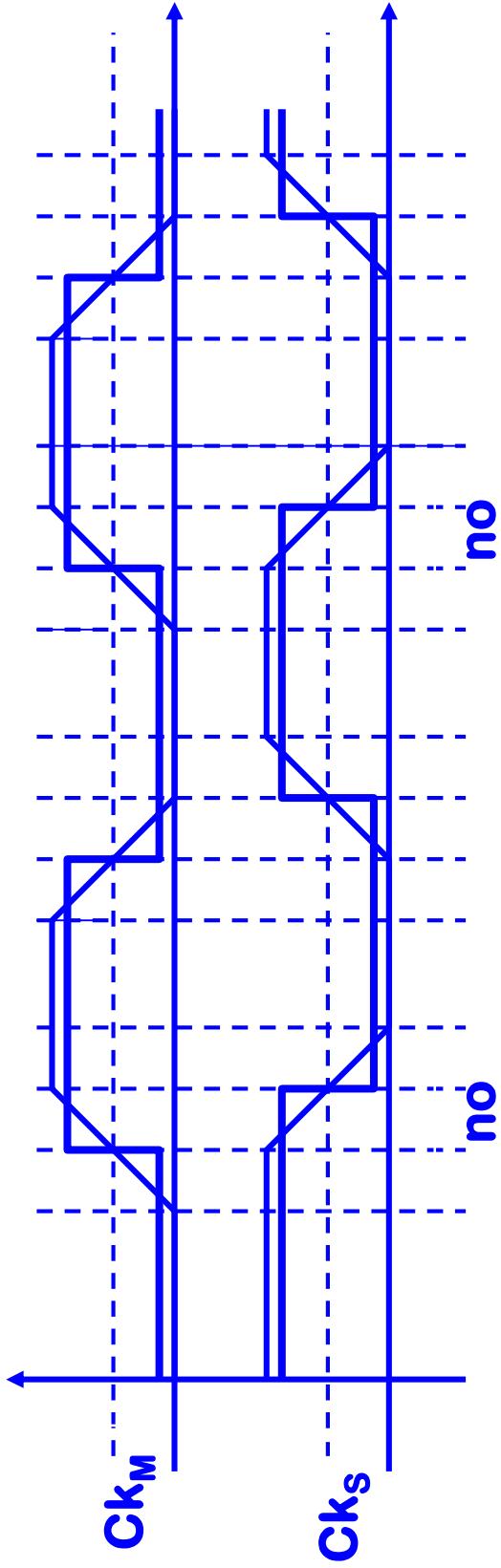


Number of Transistors = 32

# Not overlapped Clock

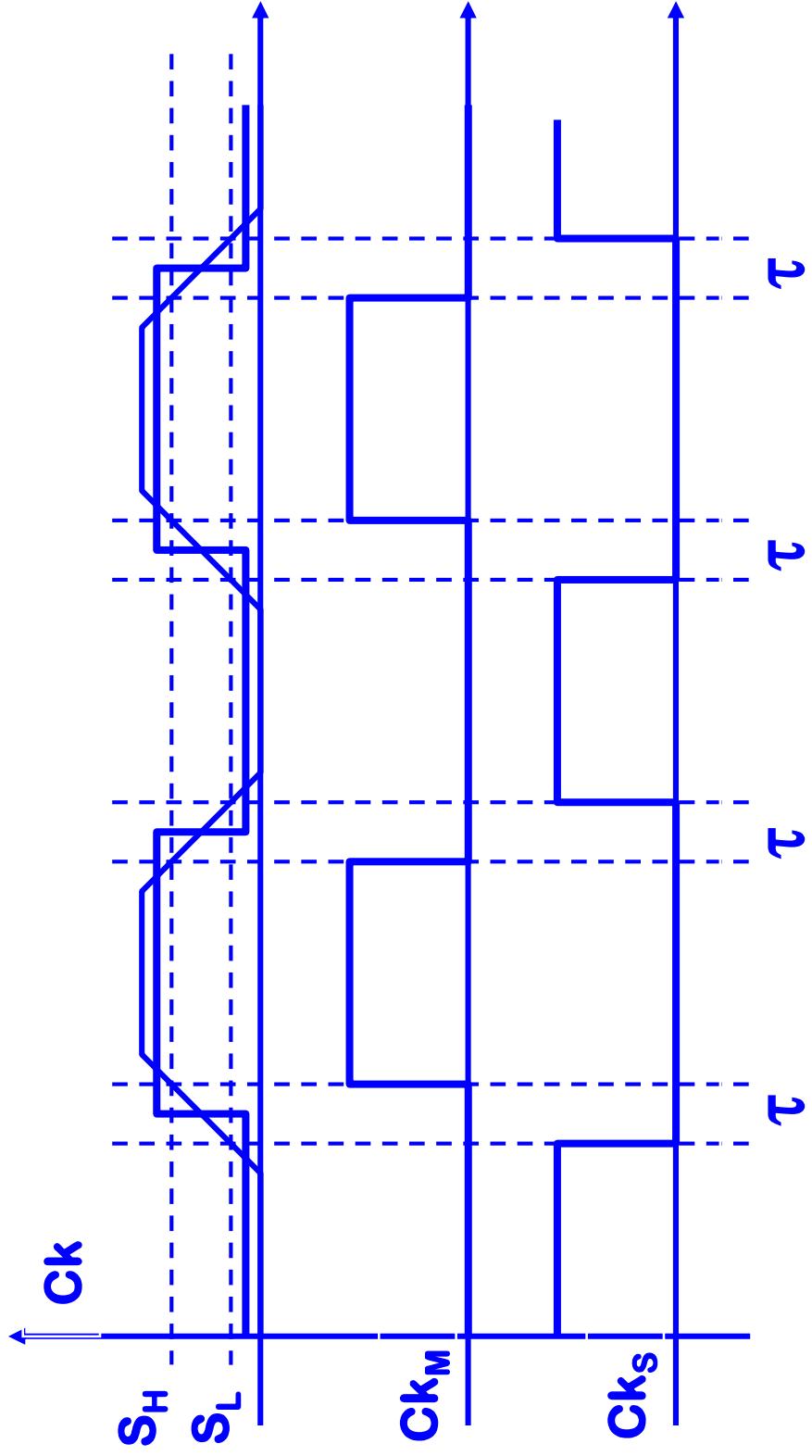
- ❖ master clock and slave clock never equal to 1 at the same time

- ❖ Slave Clock cannot be generated by inverting

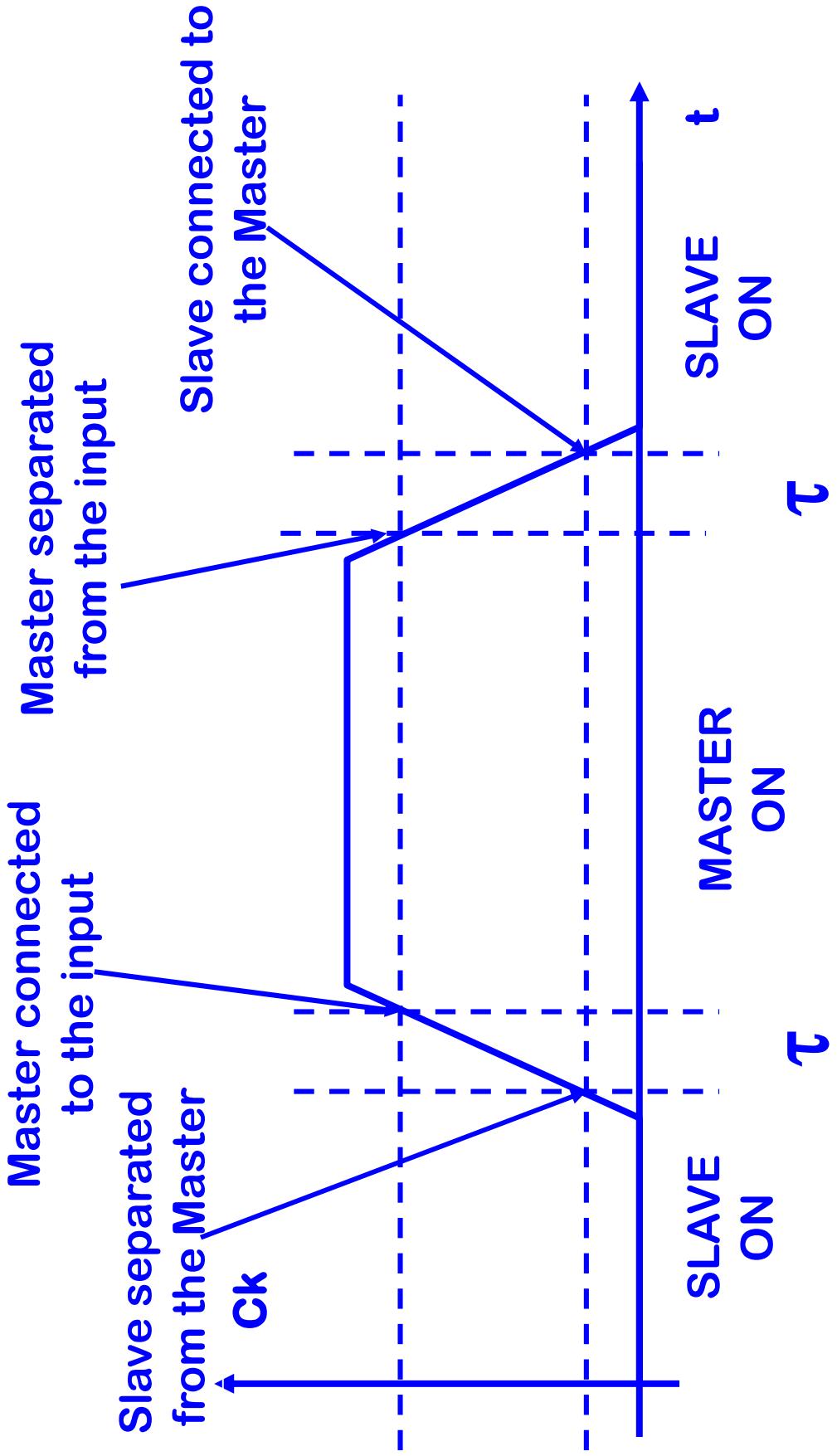


# Not Overlapped Clock

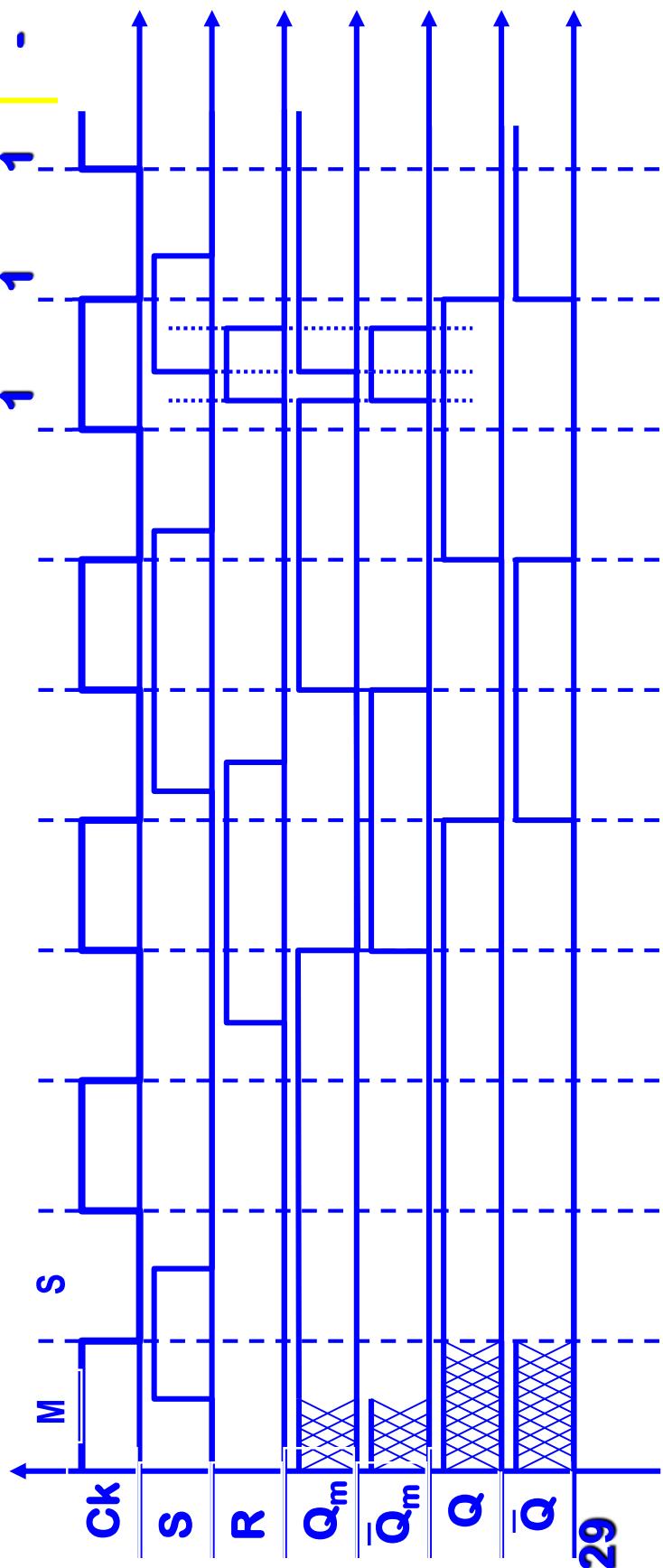
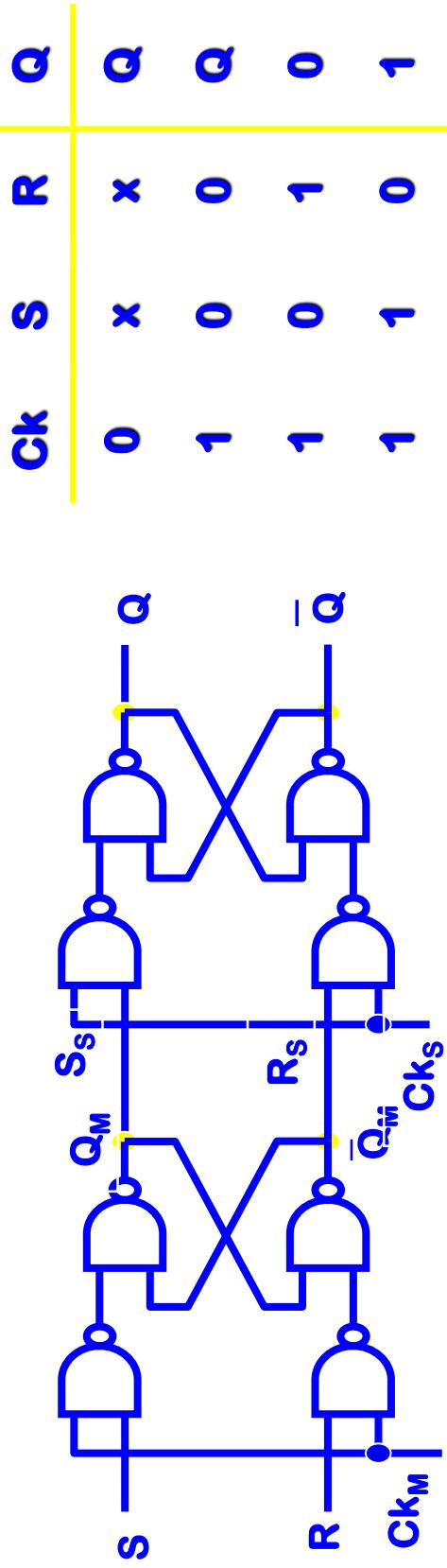
❖ Threshold Techniques



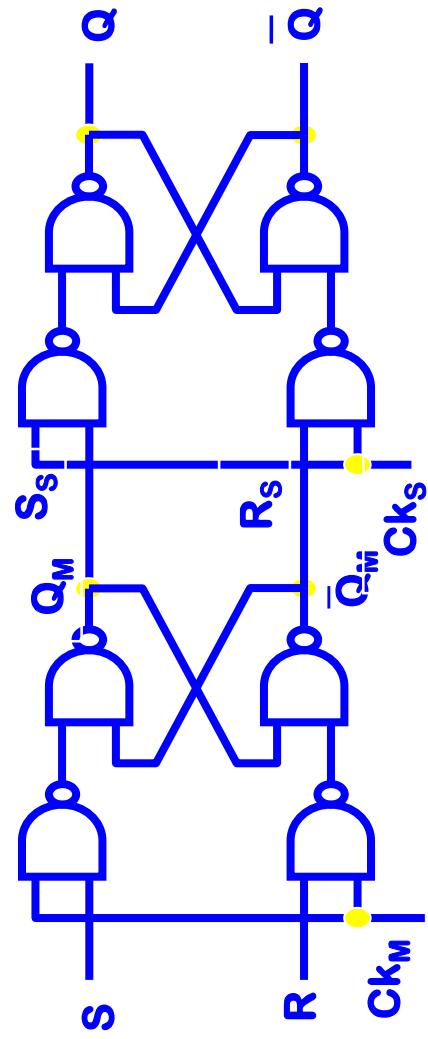
# Working Sequence



# Waveform F-F MASTER - SLAVE



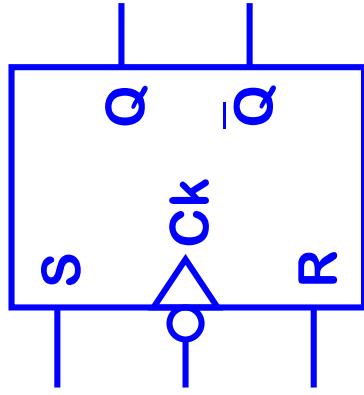
# Truth Table



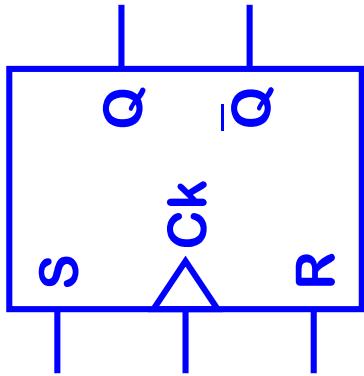
	$Q$	$Q$	$Q$	$Q$	$Q$	$0$	$1$	$1$
$R$	$\times$	$\times$	$\times$	$\times$	$0$	$1$	$0$	$1$
$S$	$\times$	$\times$	$\times$	$0$	$0$	$1$	$1$	$1$
$Ck$	$0$	$1$						

# FF S-R edge-triggered

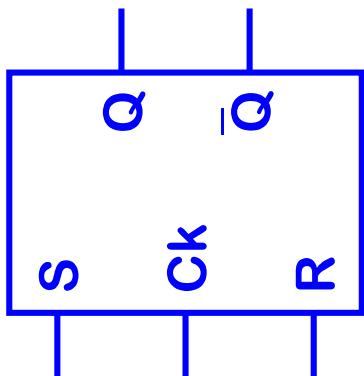
- ❖ Notes
  - Flip-Flop S-R Master Slave changes the output when  
**Clock falling edge**
  - Negative EDGE-TRIGGERED
- ❖ Symbols



FF S-R  
Negative  
Edge-Triggered

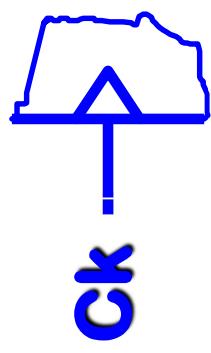


FF S-R  
Positive  
Edge-Triggered

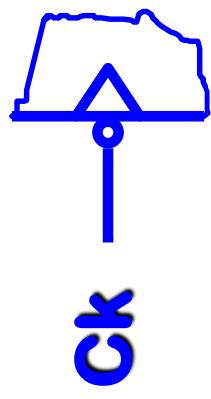


FF S-R  
With clock

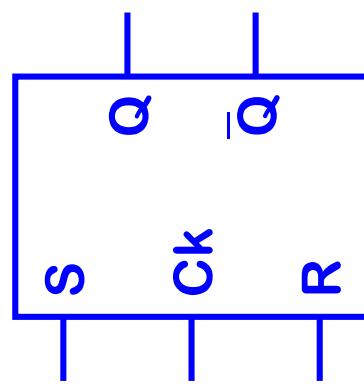
# FF S-R edge-triggered



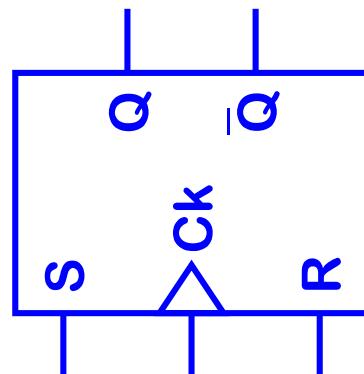
Rising Edge



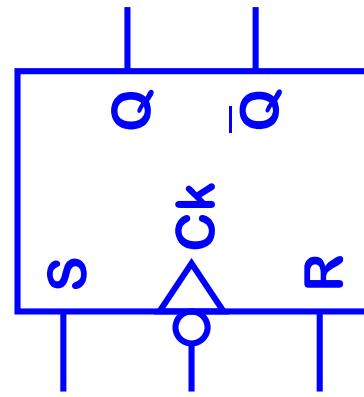
Falling Edge



FF S-R  
With Clock



FF S-R  
Positive  
Edge-Triggered



FF S-R  
Negative  
Edge-Triggered

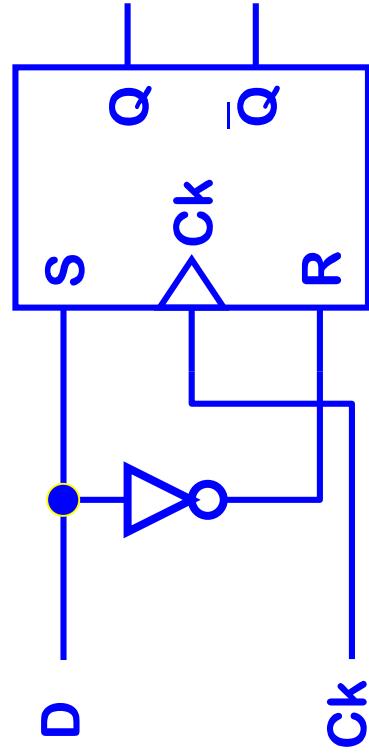
# Flip- Flop D Edge Triggered

- ◆ Data is transferred to the output when **clock rising (falling)** edge occurs

◆ **Truth Table**

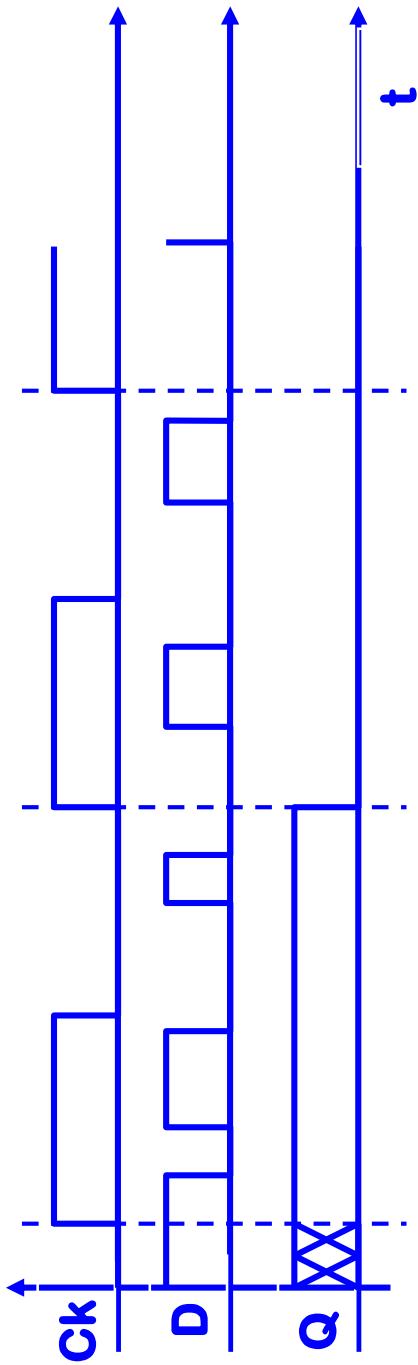
Ck	D	Q
0	X	X
1	X	X
		0
		1

◆ **Logic Scheme**

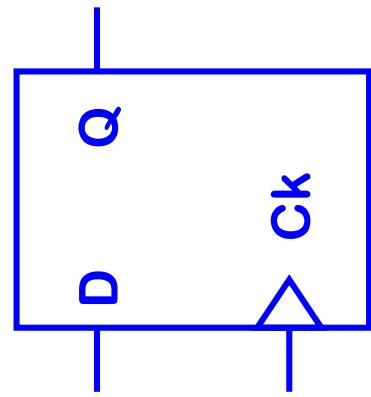


**Number of Transistors = 34**

# Notes

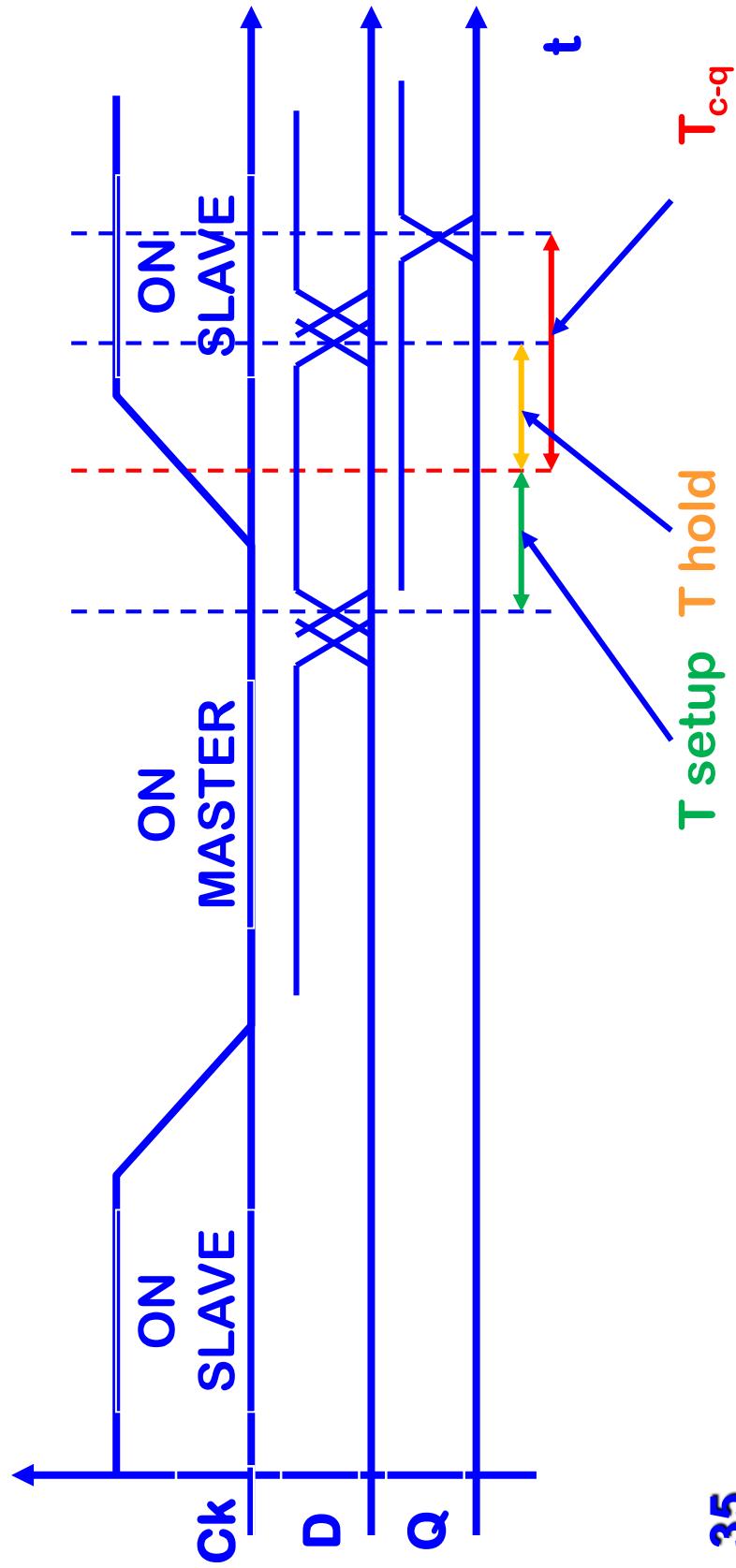


❖ Output is updated **synchronous** with the Clock



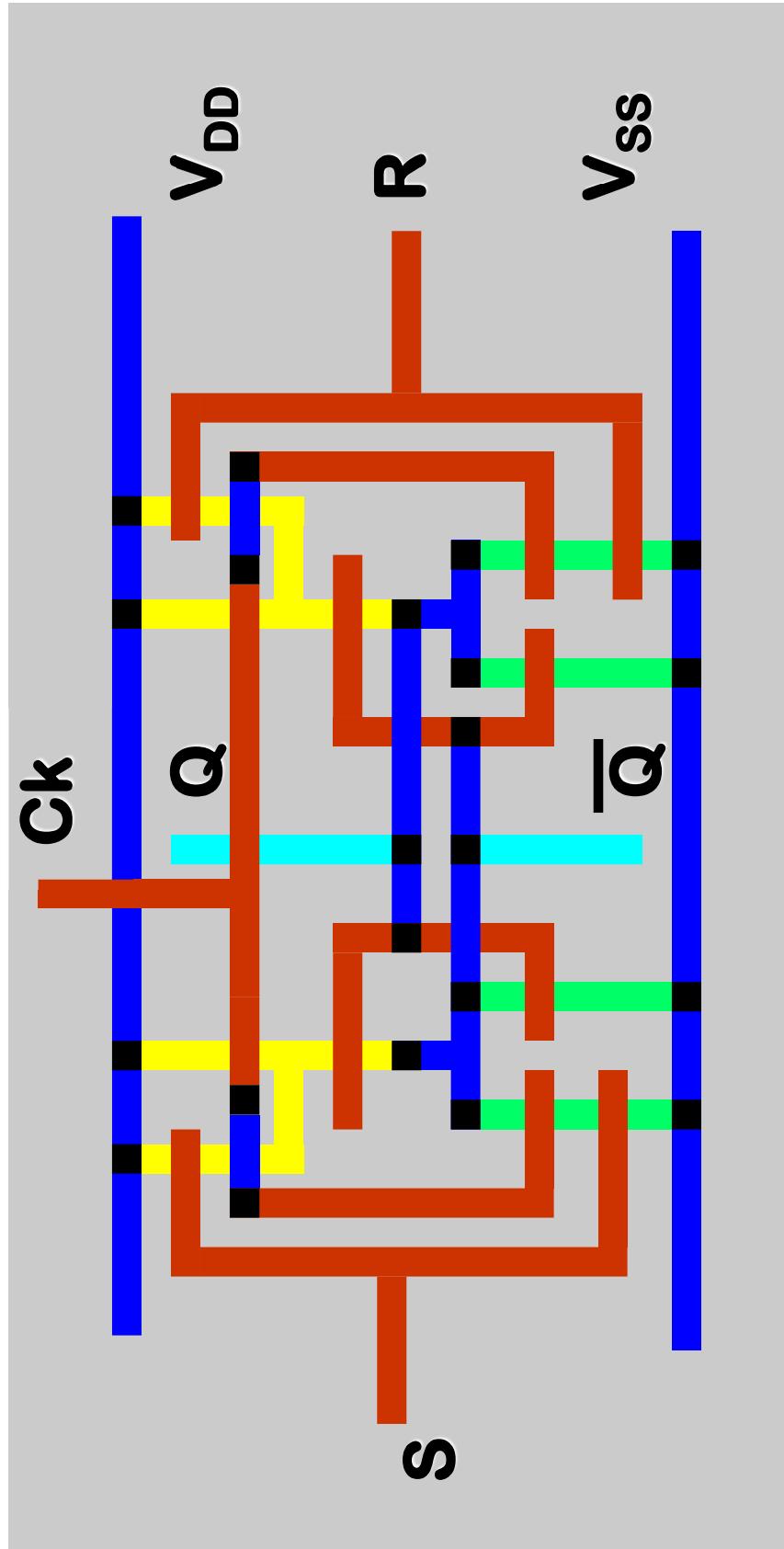
❖ Symbol

# Timing Rules



# Stick Diagram FF SR (NOR2)

★ Number of Transistors = 12

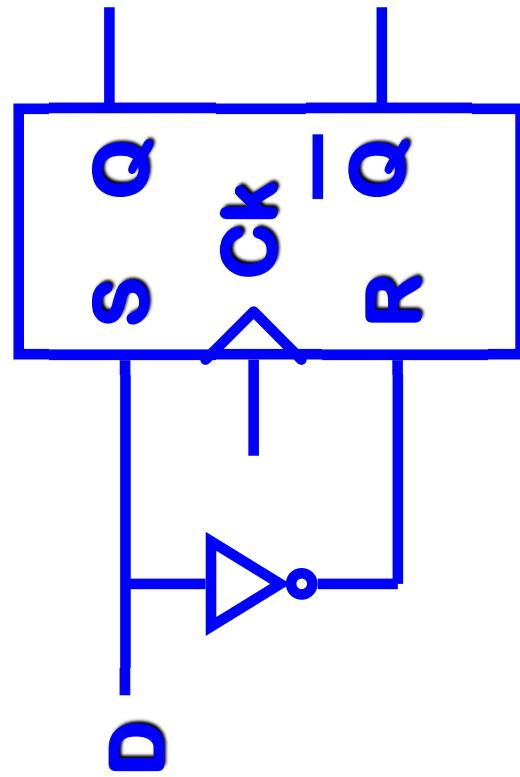


# FF D edge triggered on FFSR(NOR2)

## Truth Table

## Logic Scheme

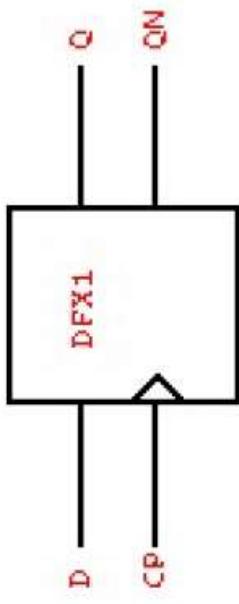
**12+12+2=26 transistors**



D	Ck	Q	Q	Q	Q	0	1
X	1	0	0	0	0	0	1
X	X	X	X	X	X	0	1

Description : p115p115p115p115p115  
strength X1

strength	1
cell Area	232.960 $\mu\text{m}^2$
equation	$Q = "D"$ $QN = "!(D)"$
Clock	CP
Type	Sequential
Input	D
Output	Q, QN



State Table						
	CP	D	$IQ_{(\text{int})}$	$IQN_{(\text{int})}$	Q	QN
	R	L	-	-	L	H
	R	H	-	-	H	L
	F	-	L	H	L	H
	F	-	H	L	H	L

#### Propagation Delay [ns]

	Input Transition [ns]	0.01	4.00
Load Capacitance [fF]	5.00	100.00	5.00
CP to Q	fall	0.30	0.68
	rise	0.26	0.87
CP to QN	fall	0.30	0.67
	rise	0.37	0.99

#### Output Transition [ns]

	Input Transition [ns]	0.01	4.00
Load Capacitance [fF]	5.00	100.00	5.00
CP to Q	fall	0.06	0.54
	rise	0.09	1.04
CP to QN	fall	0.06	0.53
	rise	0.09	1.04

#### Dynamic Power Consumption [nW/MHz]

	Input Transition [ns]	0.01	4.00
Load Capacitance [fF]	5.00	100.00	5.00
CP to Q	fall	244.10	241.45
	rise	219.04	222.00
CP to QN	fall	219.04	222.00
	rise	244.10	241.45

#### Leakage [pW]

	CP	3.5800
	D	3.4160

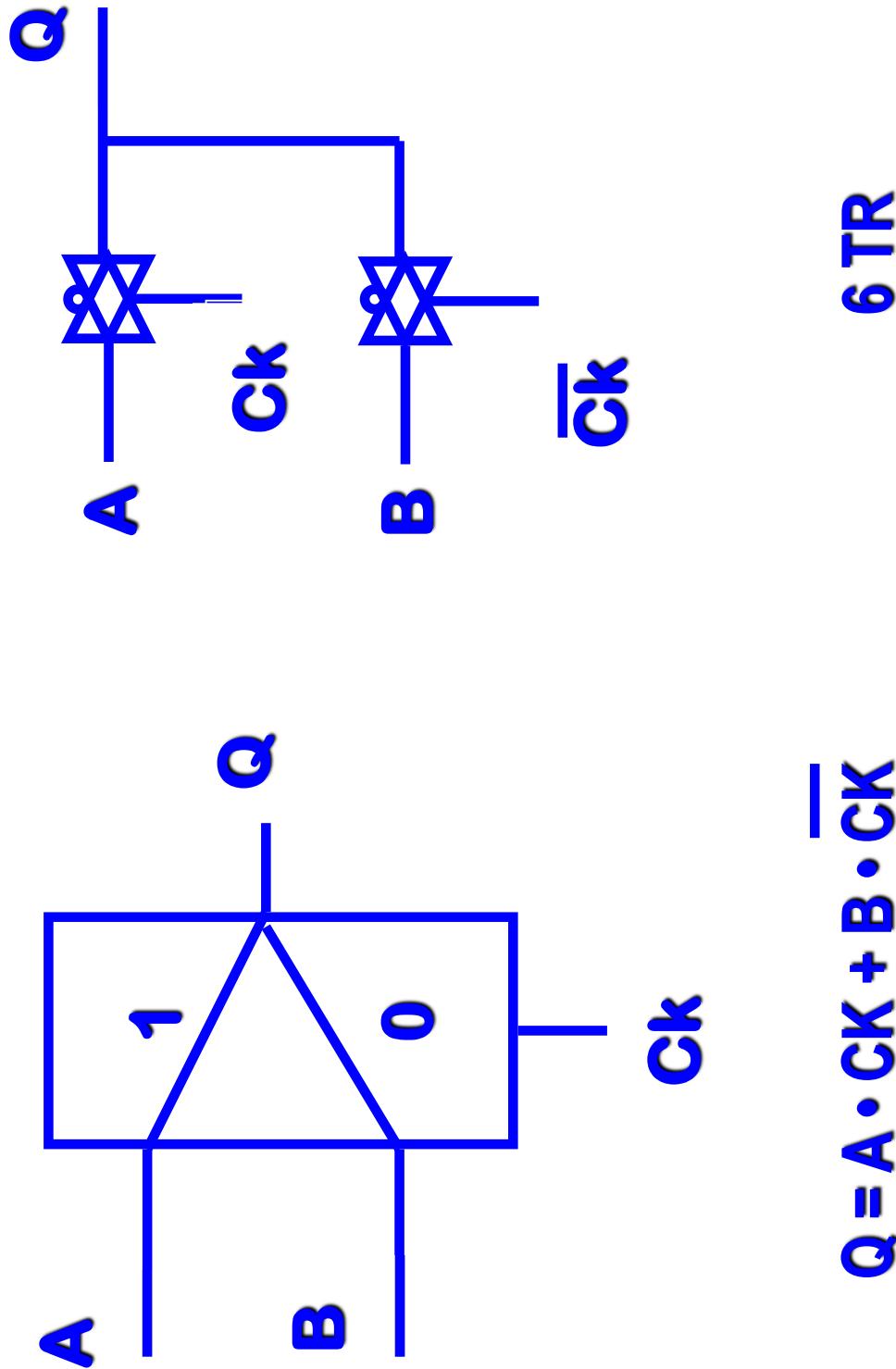
#### Capacitance [fF]

	CP	2.12
	D	2.12

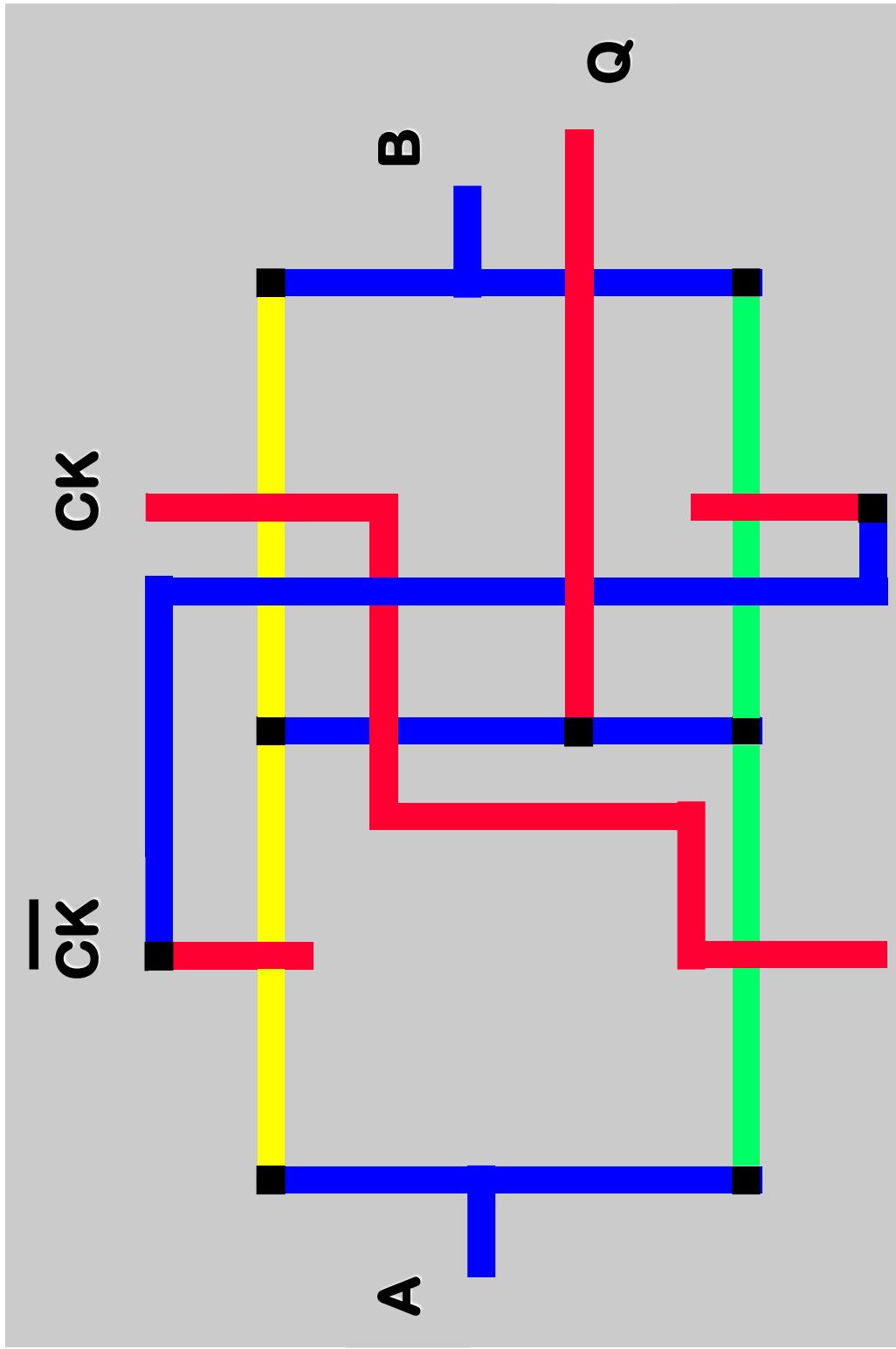
#### Constraints Time [ns]

	Setup CP to D	Hold CP to D
	fall	rise
Setup CP to D	1.06	0.48
Hold CP to D	0.67	0.68

# Two-Ways Multiplexer



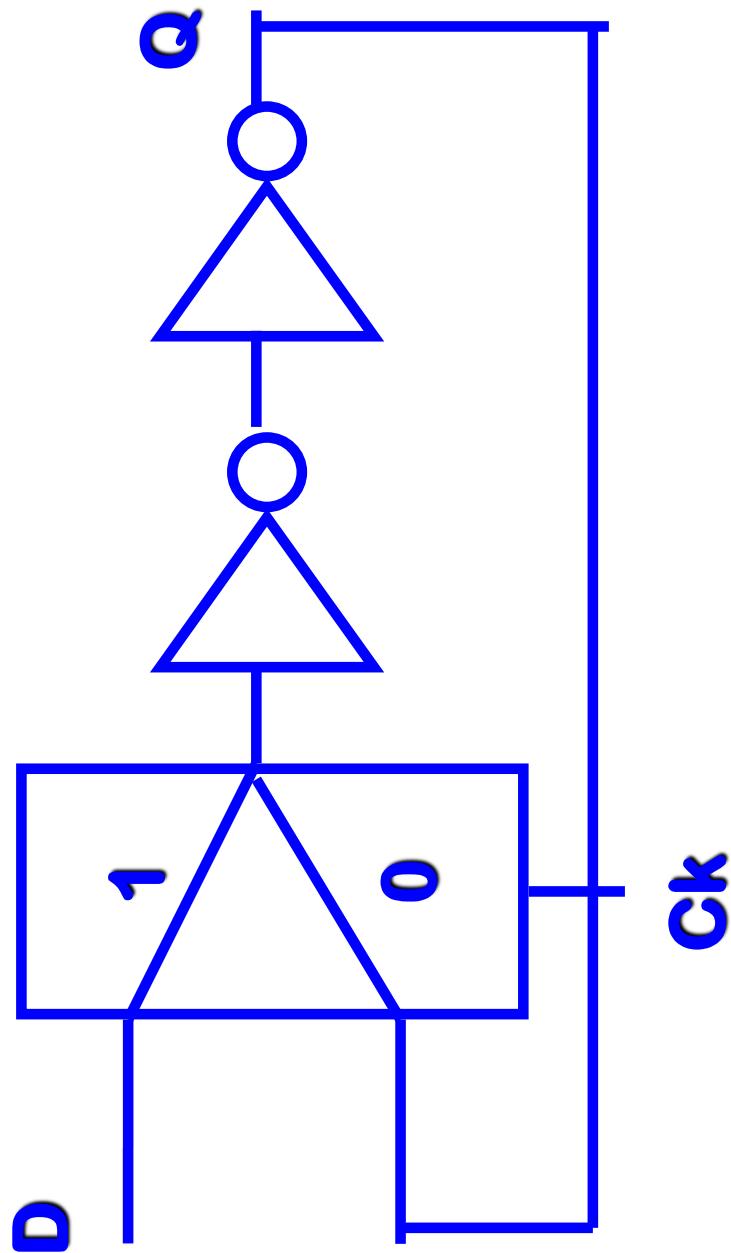
# Two-ways Multiplexer



# D-Latch

## Positive

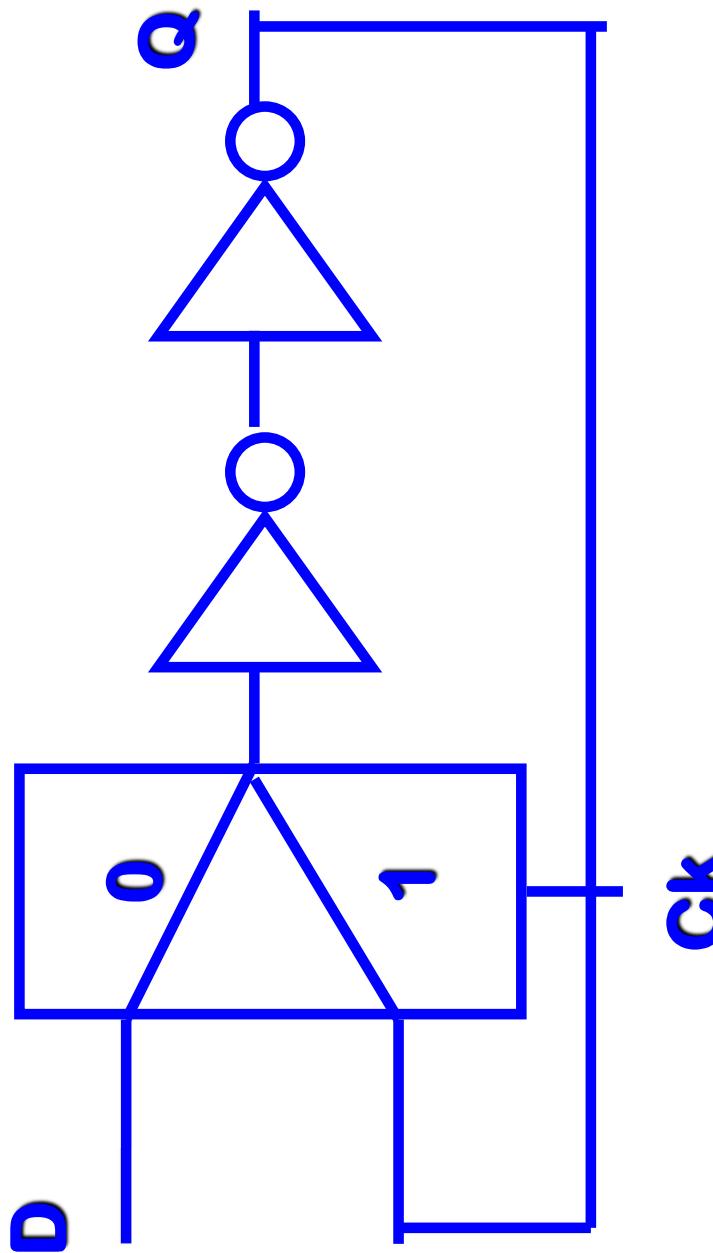
10 TR



Ck=1 : Output follows the input

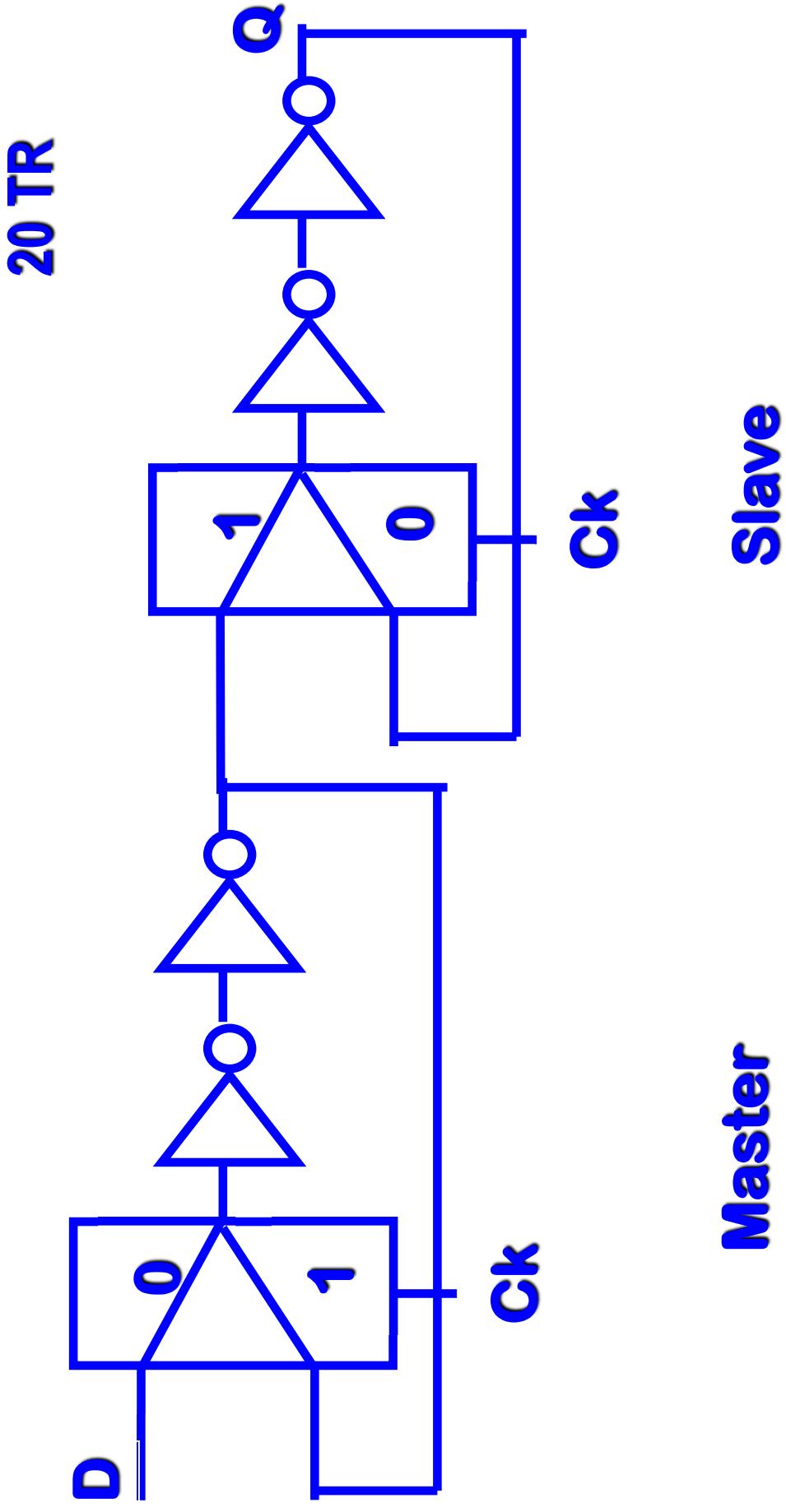
# D-Latch Negative

10 TR

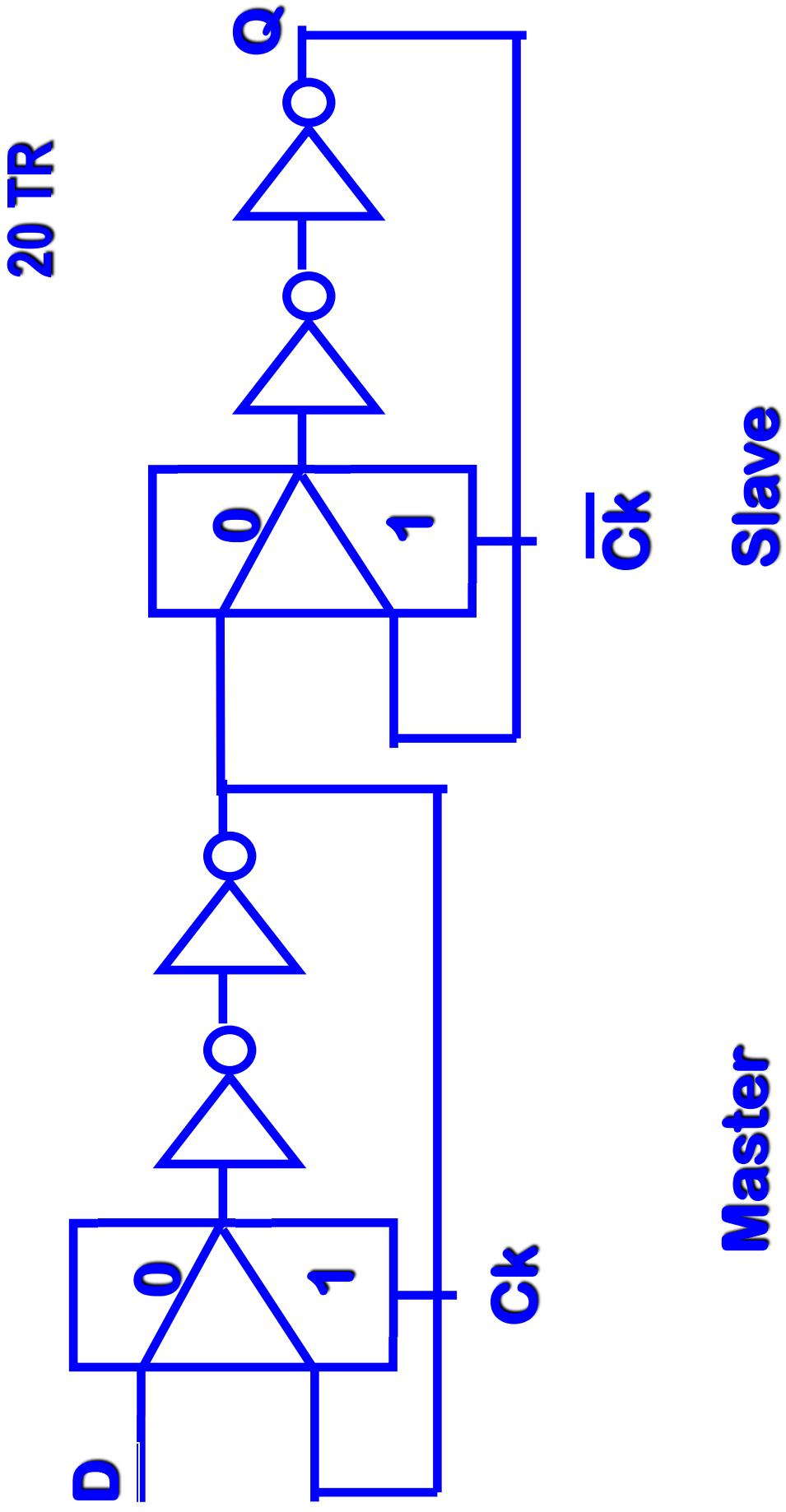


Ck=0 : Output follows the input

# Positive D-edge triggered



# Positive D-edge triggered



# **Positive D- edge triggered**

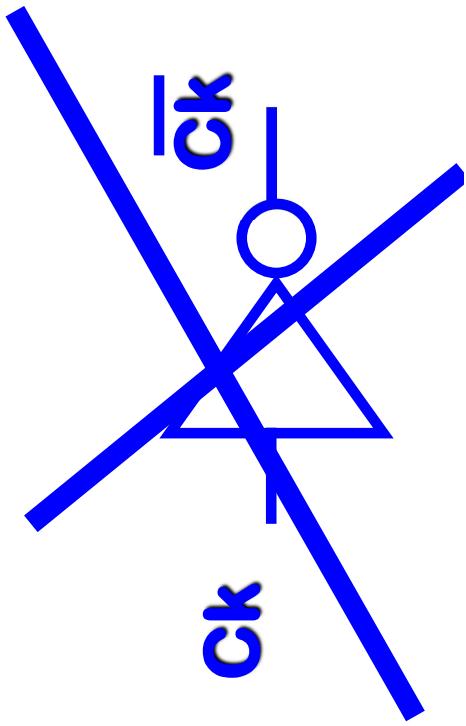
**Complexity trade-off (# of transistors)**

**FF SR (NAND2)    FF SR (NOR2)    MUX**

**34                  26                  20**

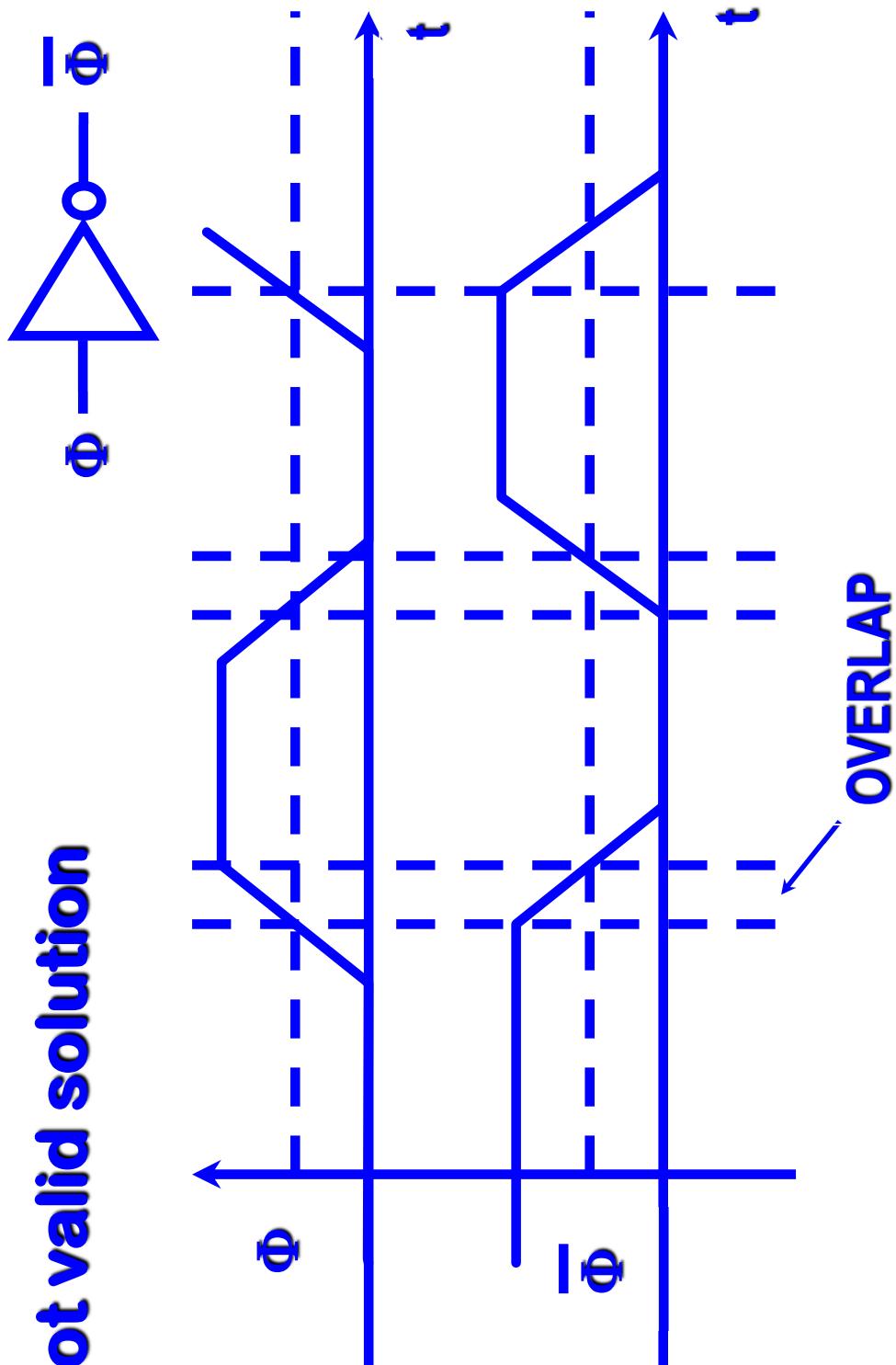
# Clock Signal

- ❖ Non transparent conditions has to be guaranteed
- ❖ CK and  $\bar{CK}$  never equal to logic 1 at the same time
- ❖ inverter Solution is not valid
- ❖ Let's see with a linear delay model for the inverter



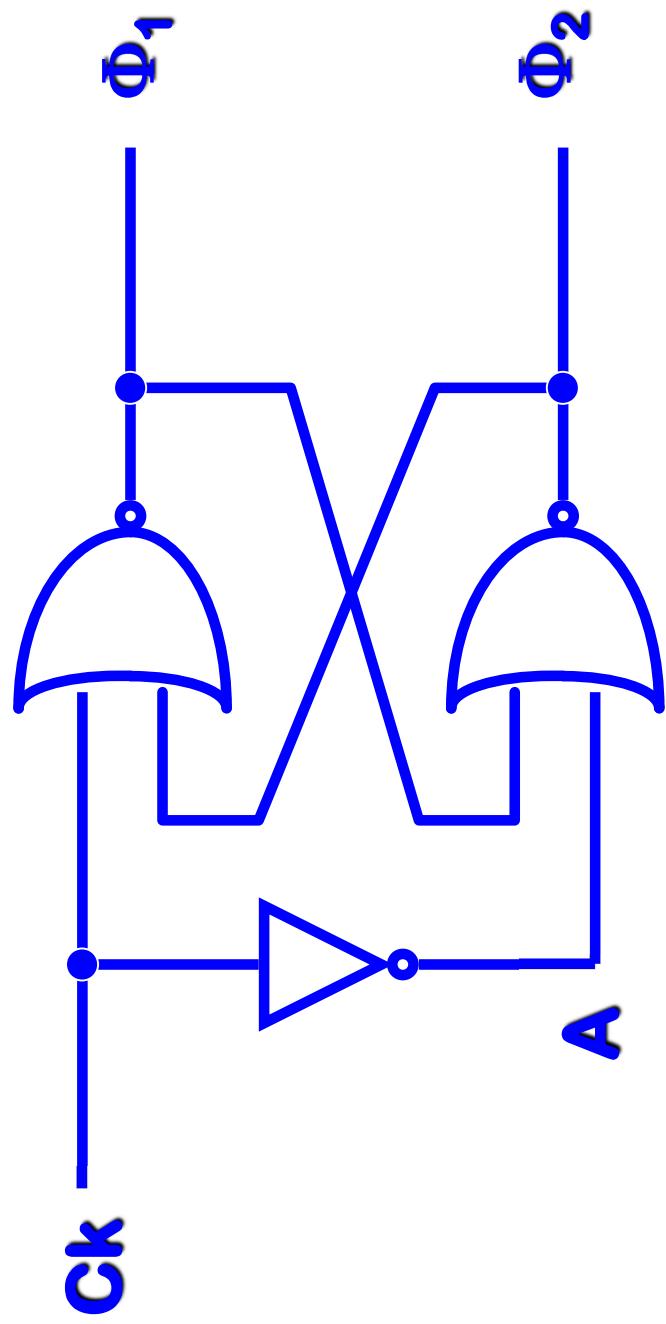
# Clock Generator with an inverter

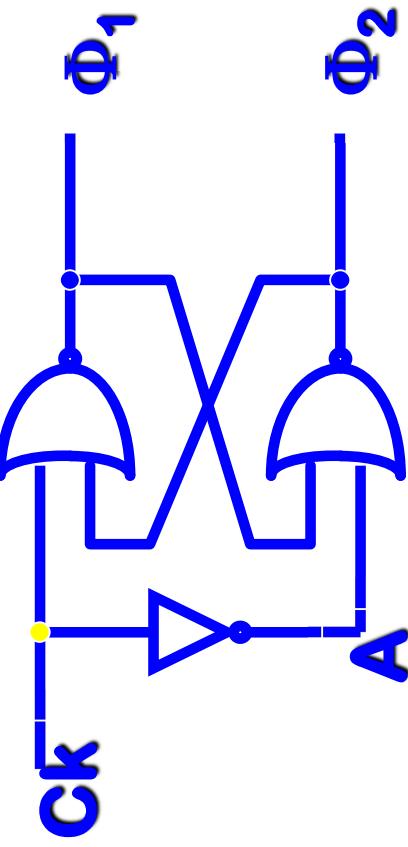
✳ Not valid solution



# Two-phases Clock Generation

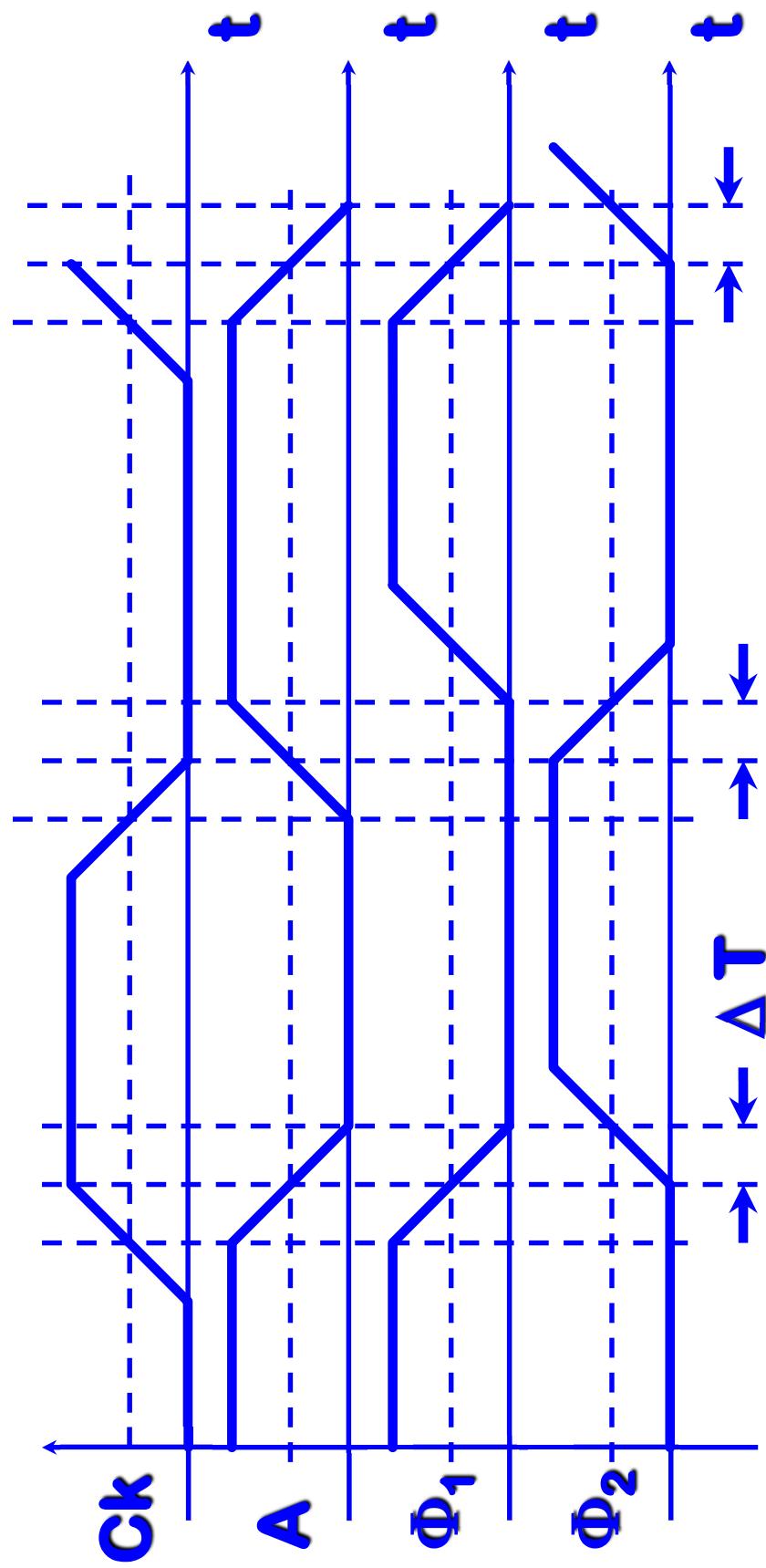
- ❖  $\Phi$  and  $\bar{\Phi}$  are not derived from an inverter
- ❖ Two signals are defined:  $\Phi_1$  and  $\Phi_2$





## Waveforms

A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0



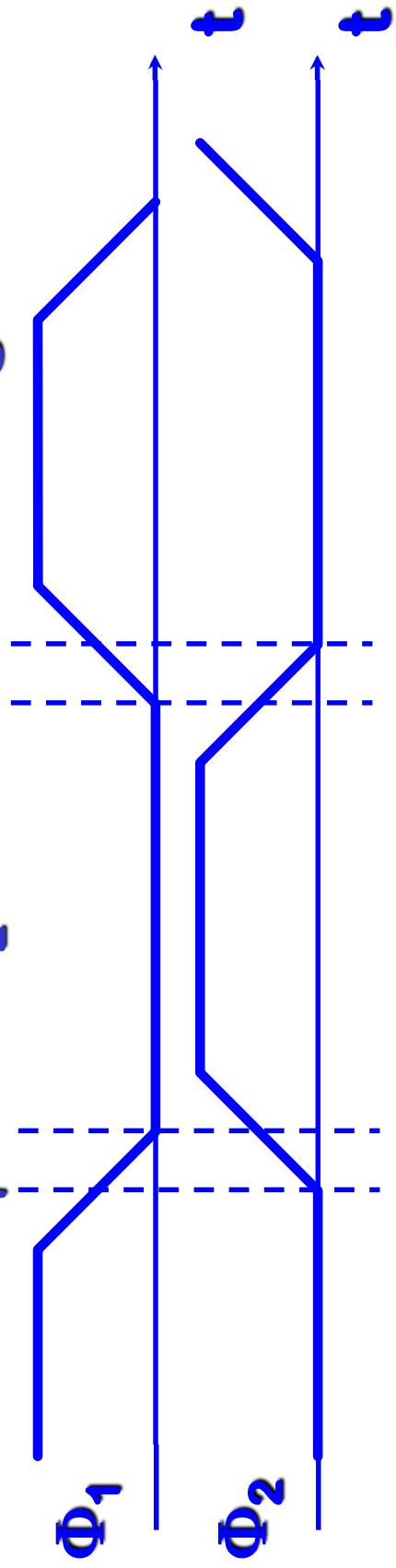
# Notes on Clock Generation

- ❖ Not overlapped condition is maintained also when driving high value capacitance
- ❖ NOR gates could be sized in order to provide the required buffering

# Static Flip - Flop

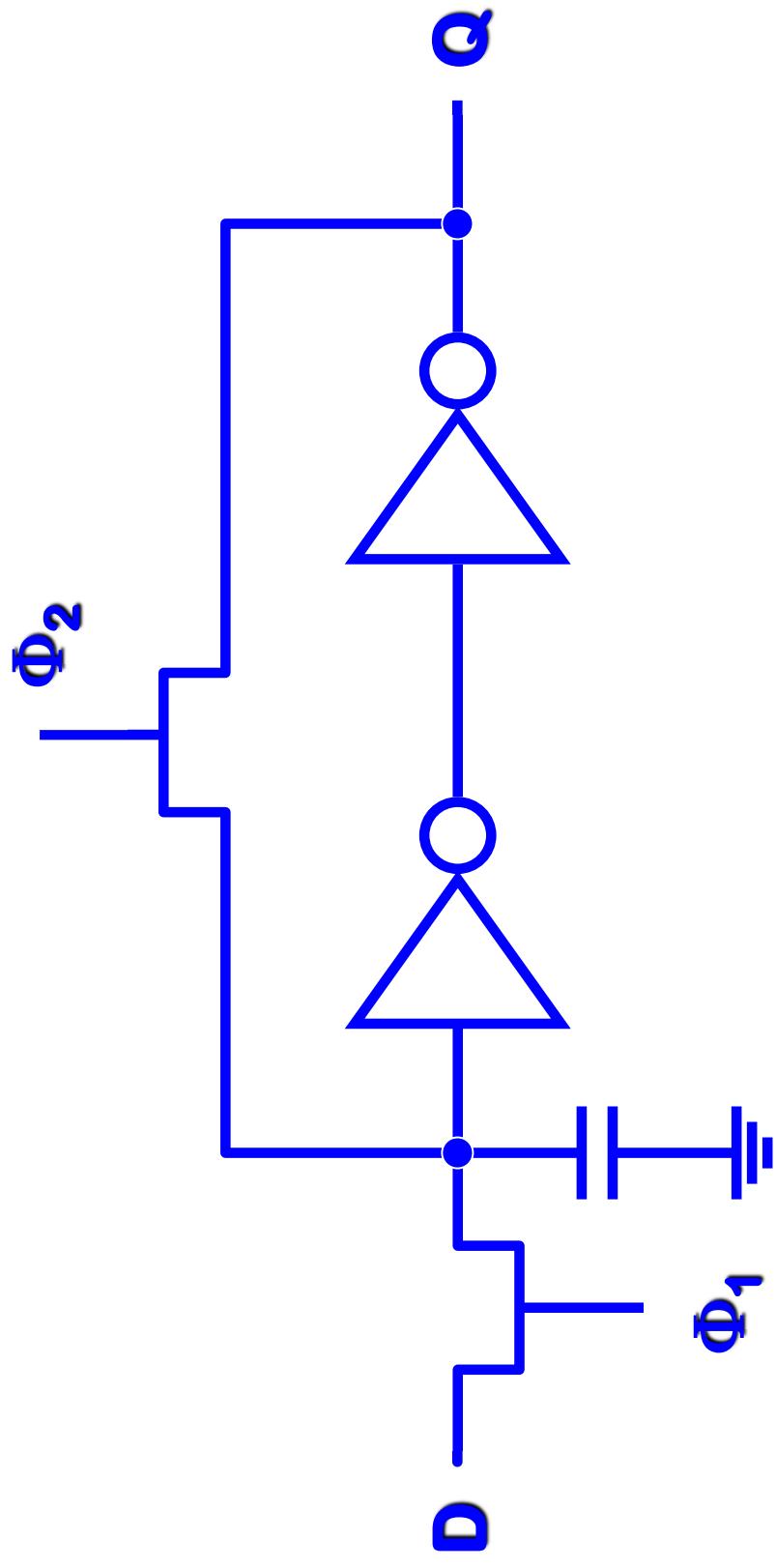
- ❖ Analyzed Flip – Flop solution are complex
- ❖ They do not rely on high impedance of MOS input
- ❖ There is an interval when both  $\Phi_1$  and  $\Phi_2$  are at the low logic level

- ❖ MOS input capacitance could store the data when both  $\Phi_1$  and  $\Phi_2$  are at the low logic level

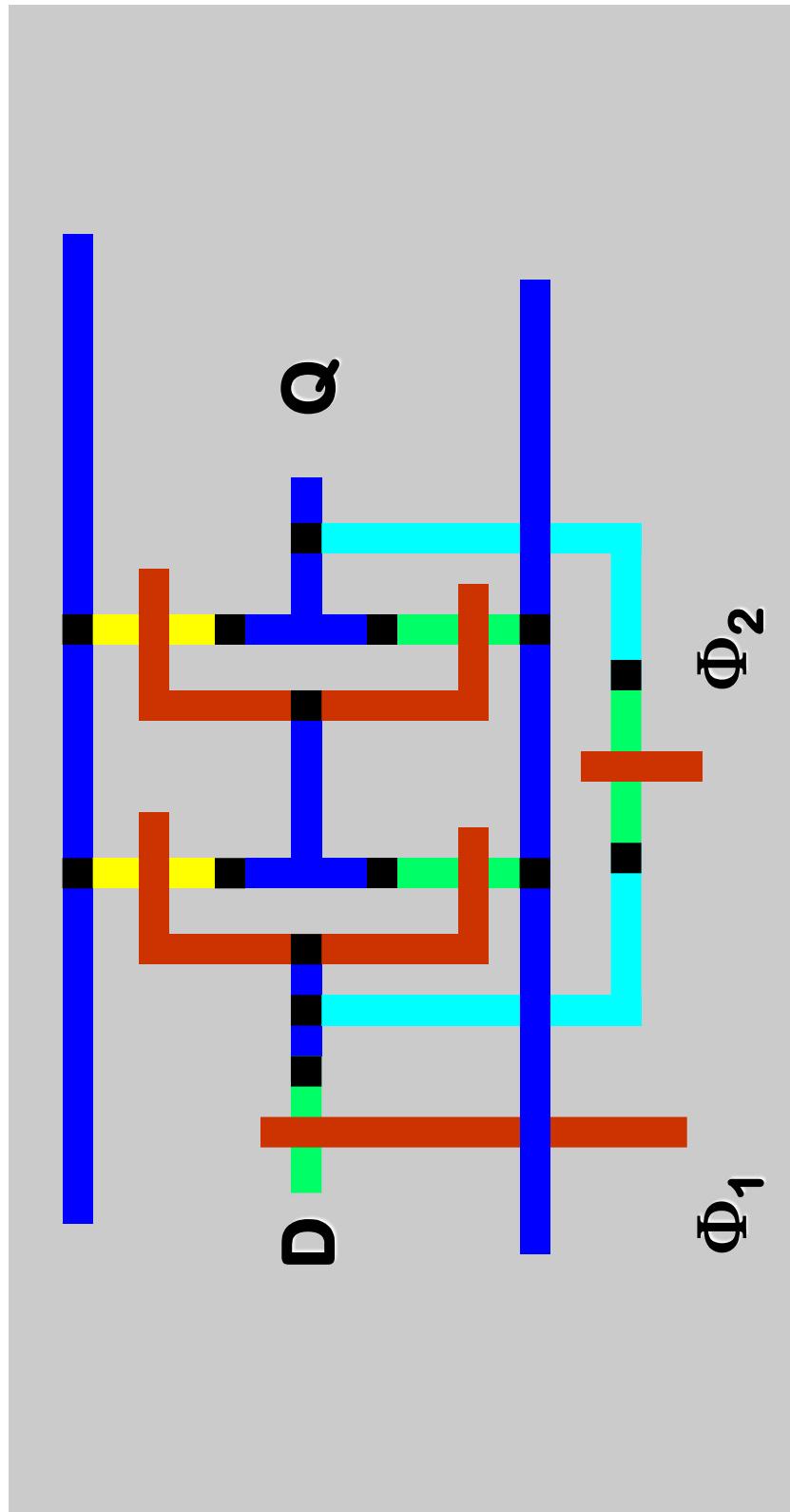


# Transparent D-Latch

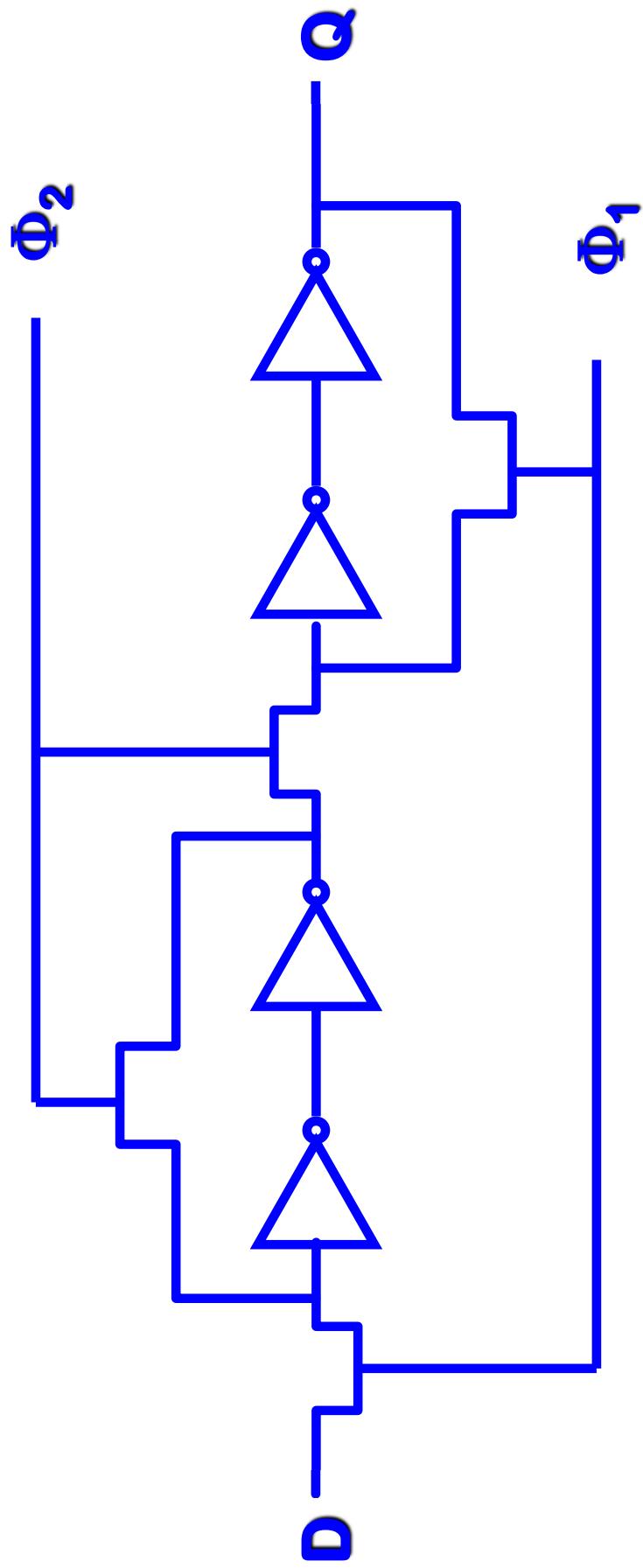
\* Pass Transistor based



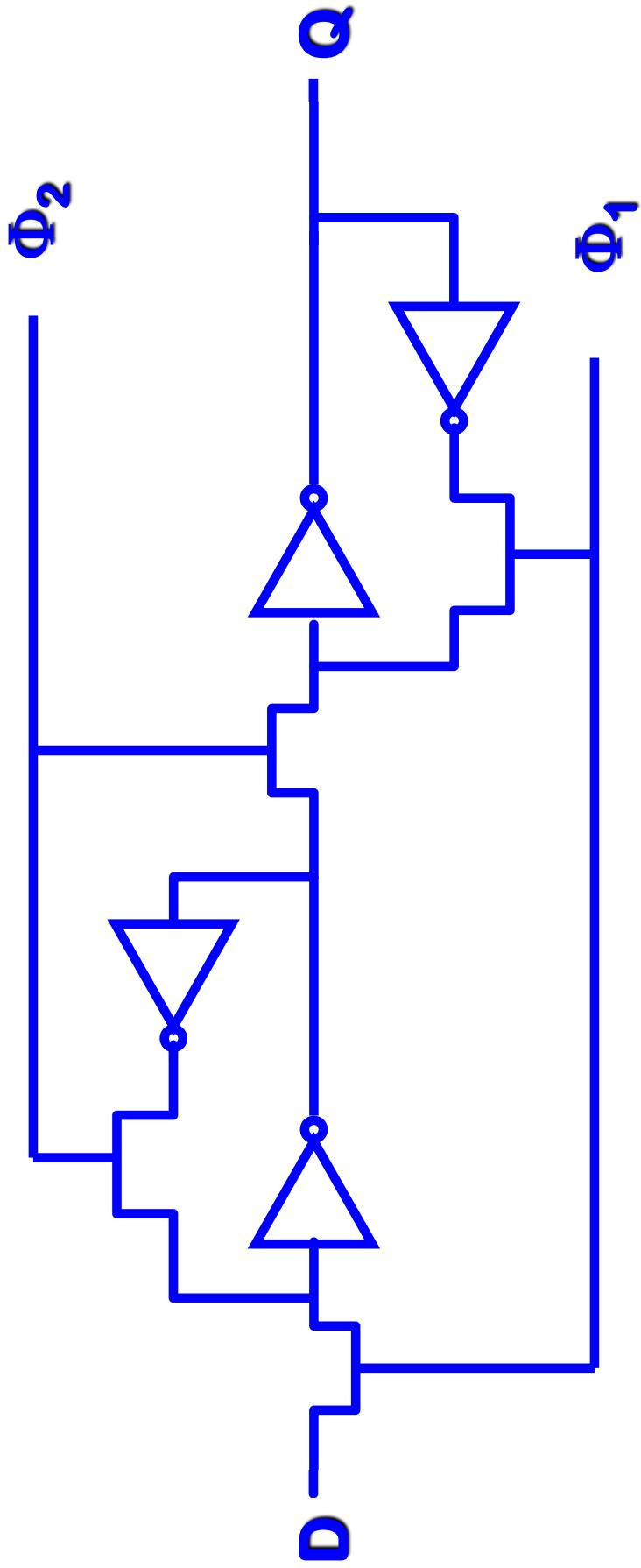
# Stick diagram



# Flip - Flop D Edge Triggered

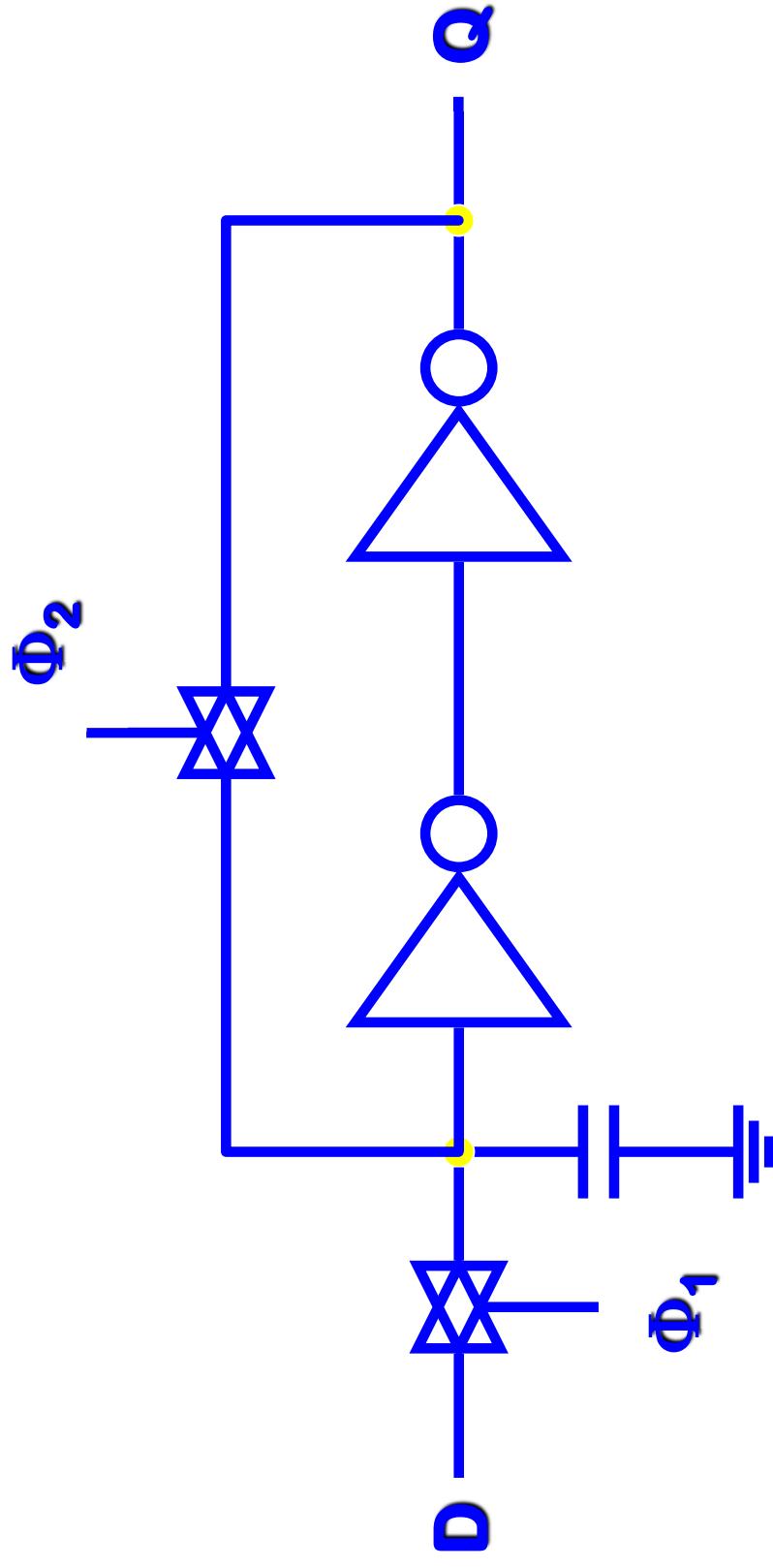


# Delay Optimization



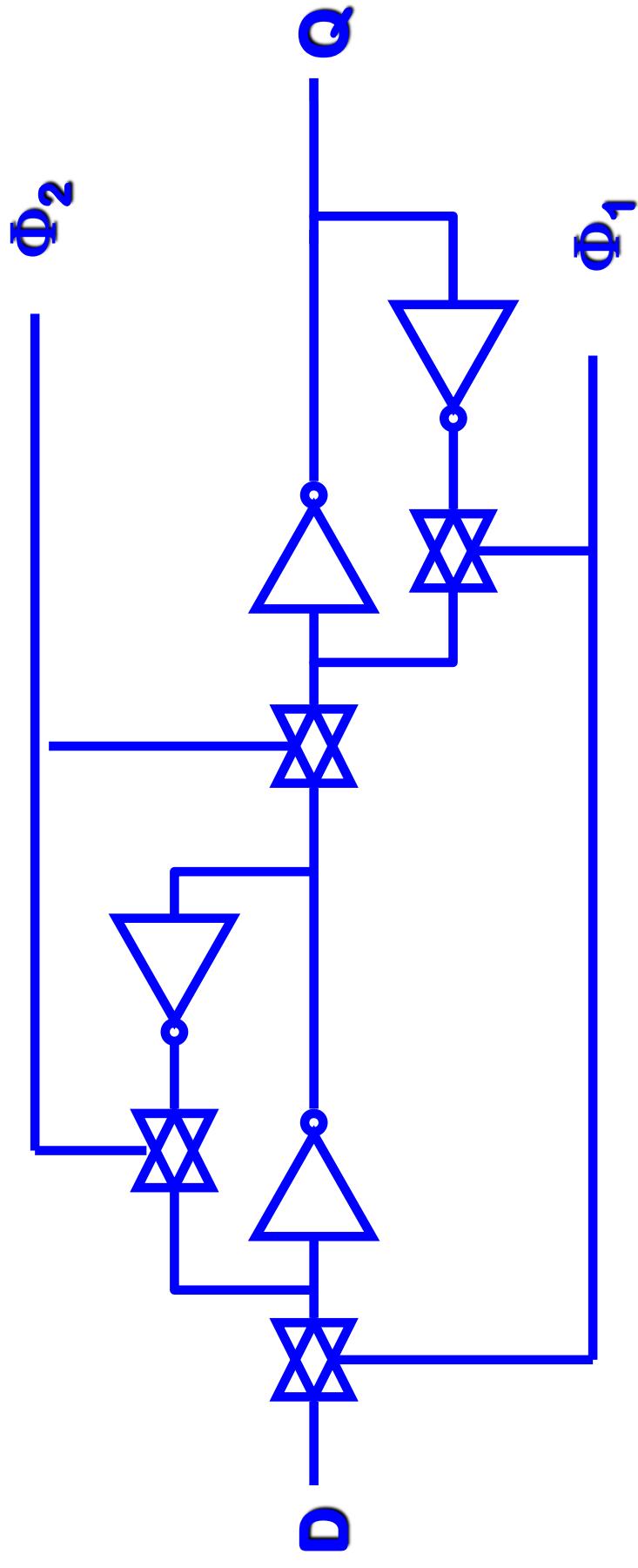
# Transparent D-Latch with Pass Gate

\*Only positive signals are shown  
\*◆



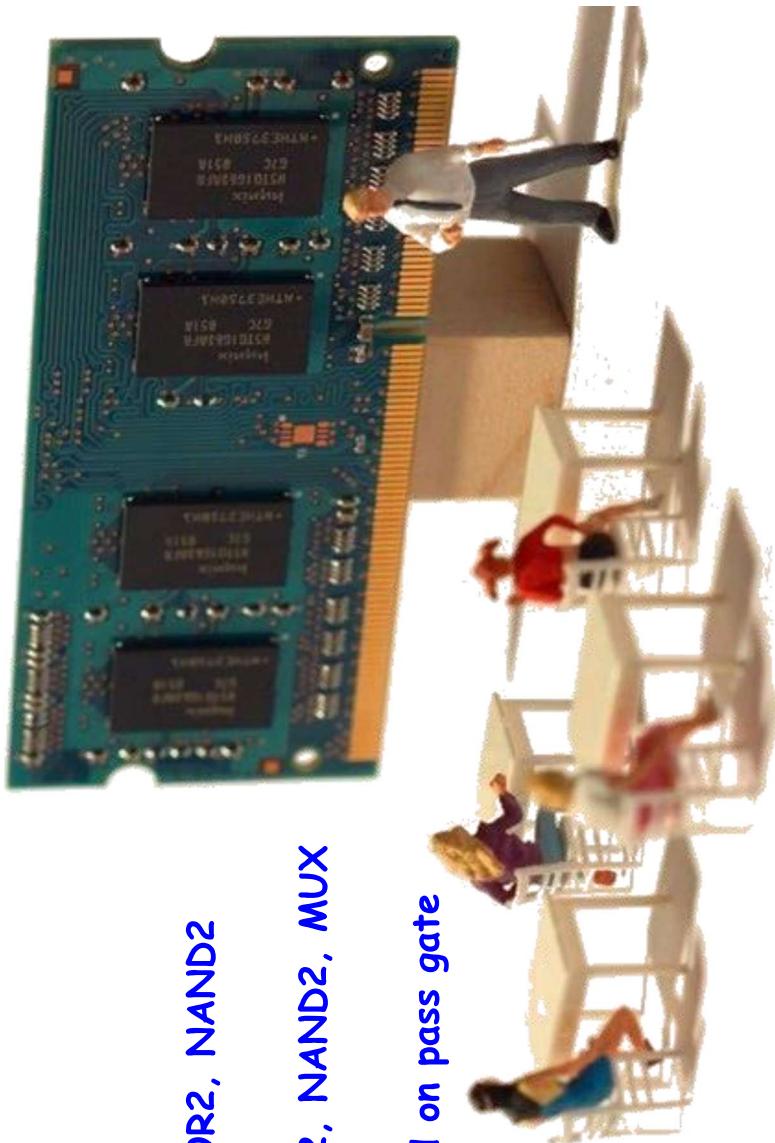
# Flip - Flop D Edge Triggered with Pass Gate

★ 16 transistors



# End, Questions ?

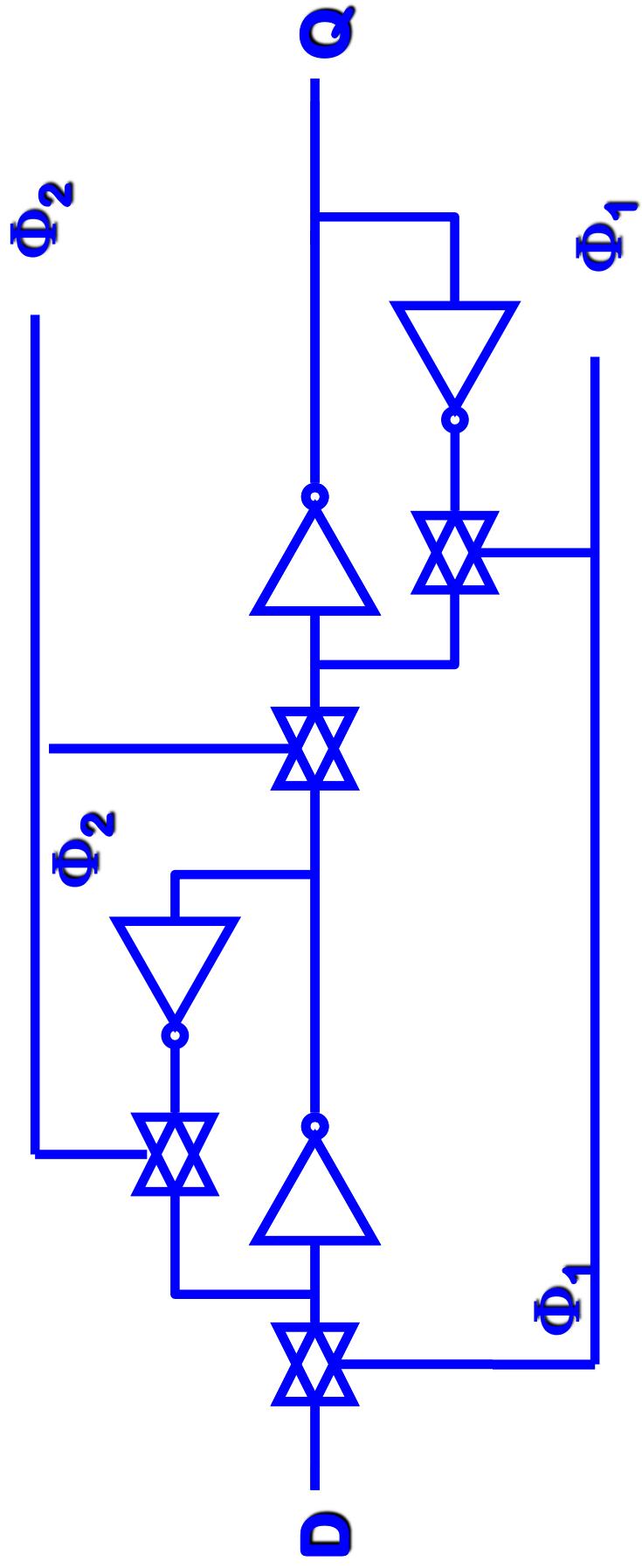
- **Flip Flop: Static Solution**
  - Flip- Flop S-R: NOR2 e NAND2
  - Flip-Flop S-R with enable
  - D -Latch
  - Flip Flop S-R Edge Triggered: NOR2, NAND2
  - Flip Flop D Edge Triggered: NOR2, NAND2, MUX
  - Flip Flop D Edge Triggered based on pass gate



# Dynamic Flip - Flop

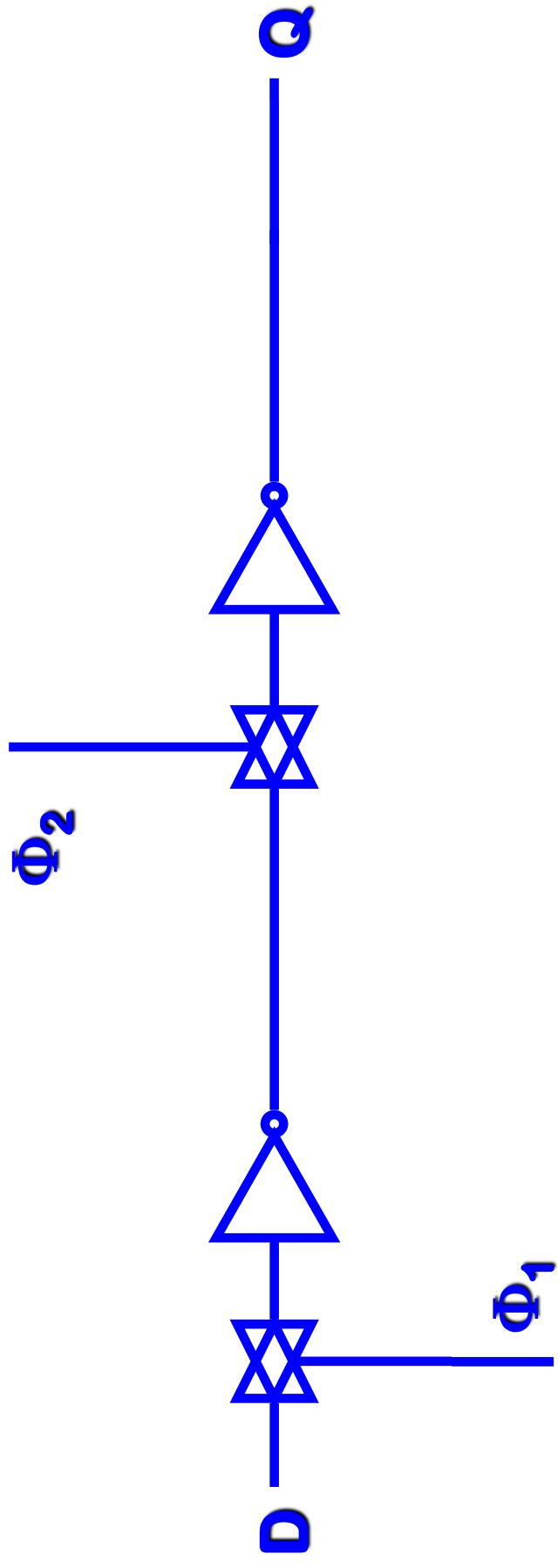
- ★ Clock is always running
  - ★ Reduced MOS Sizes
  - ★ Reduced net length
- Greater Speed

# Flip - Flop D Edge Triggered

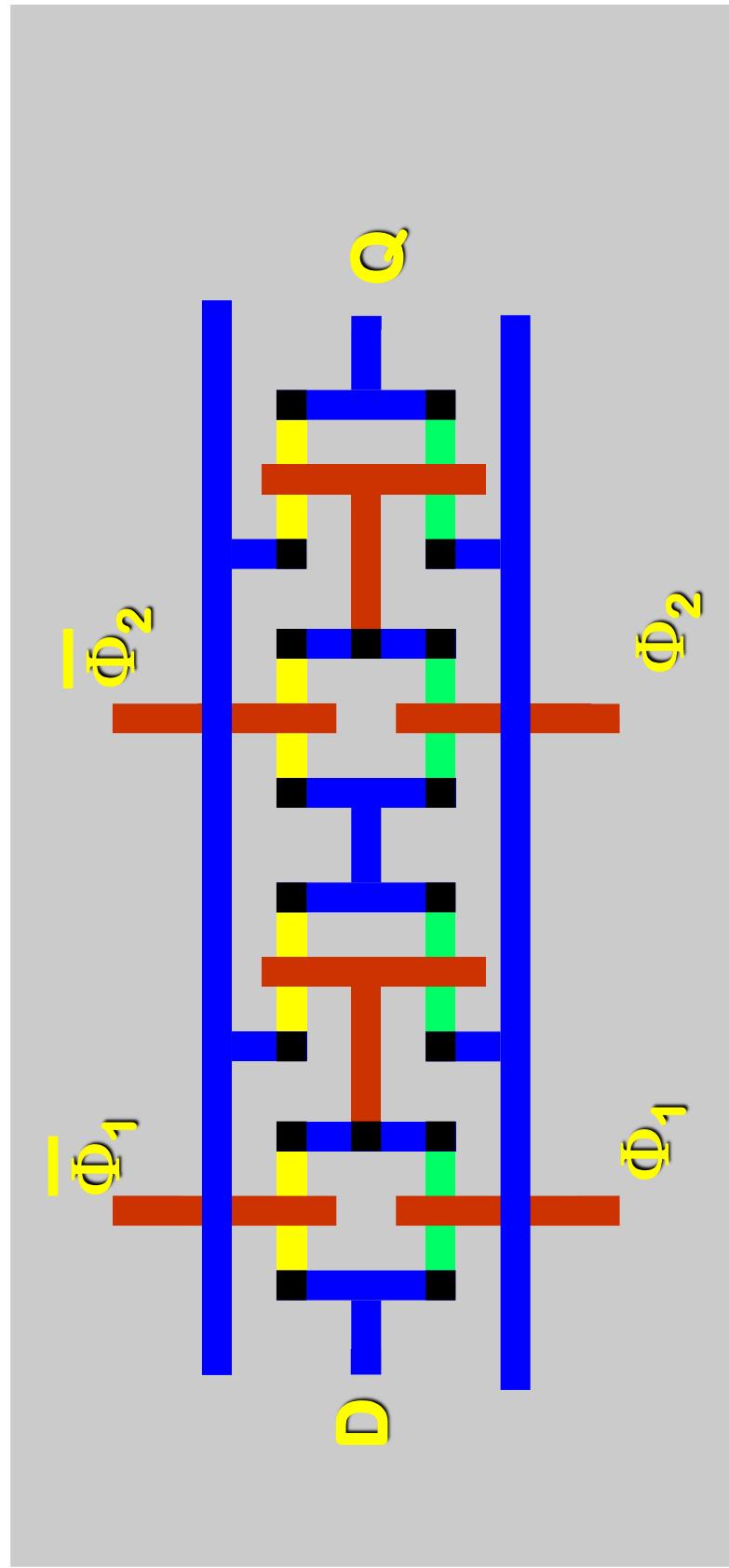


# Flip - Flop D Edge Triggered

☆ 8 transistors !

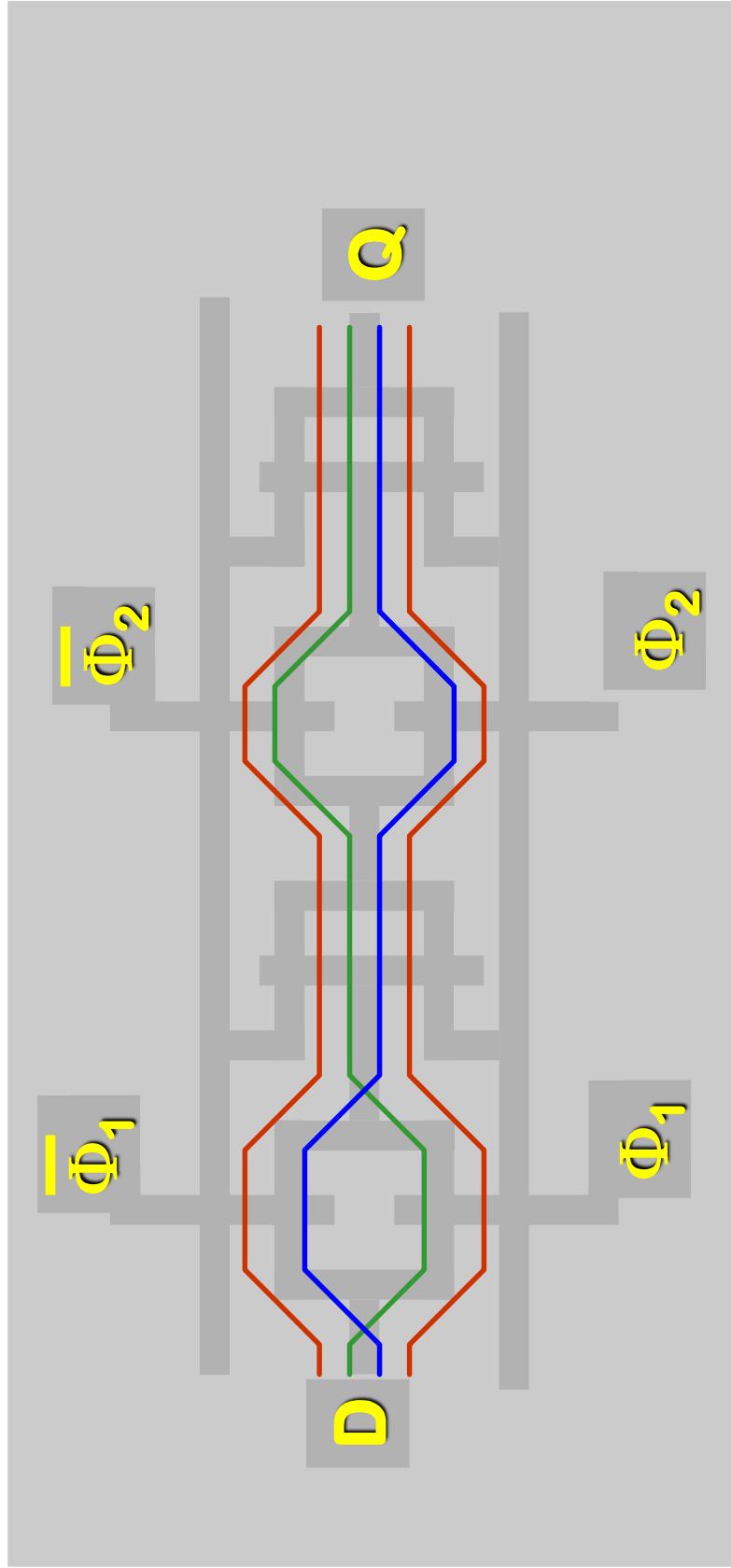


# Stick Diagram



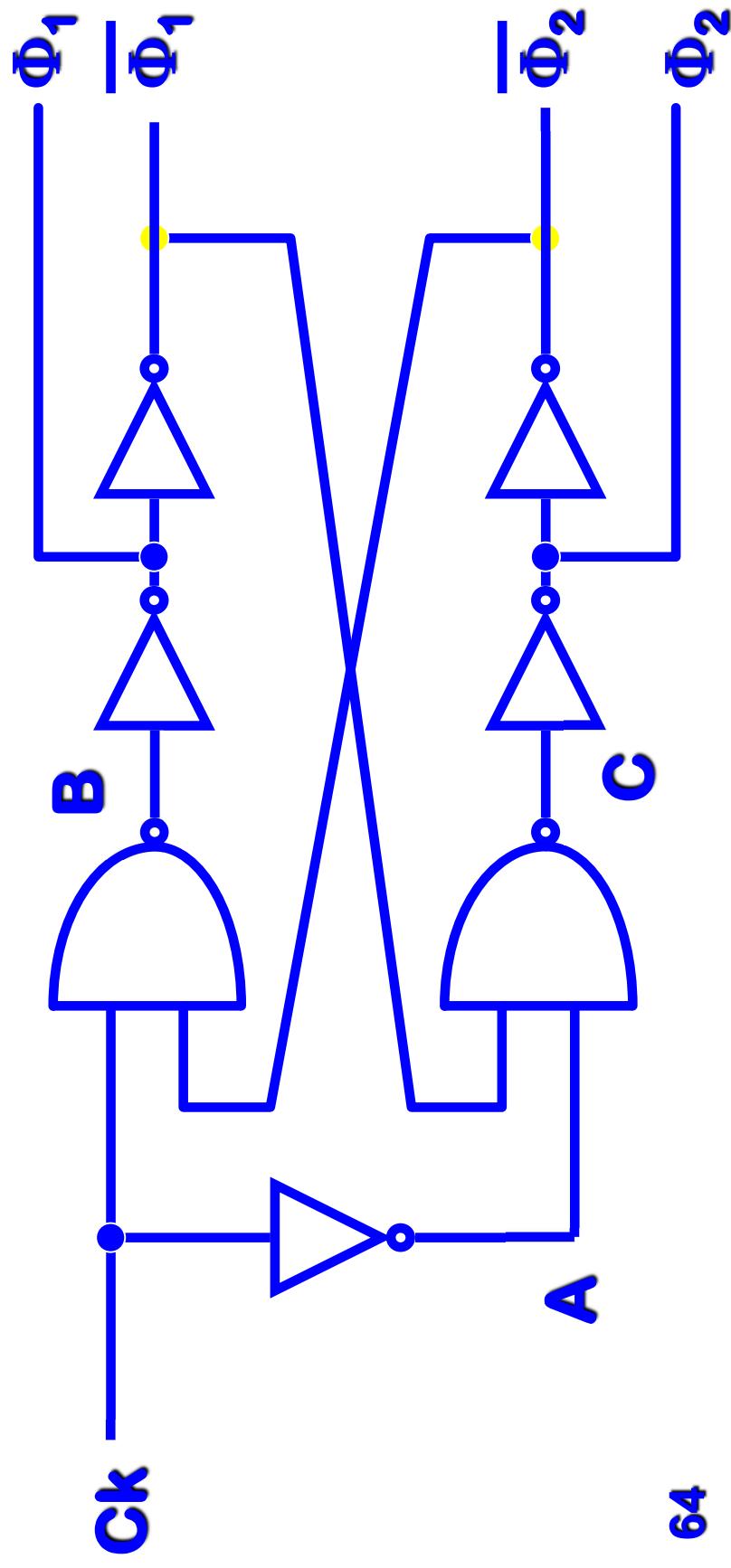
# Clock Generation

★ Possible Transparent Paths

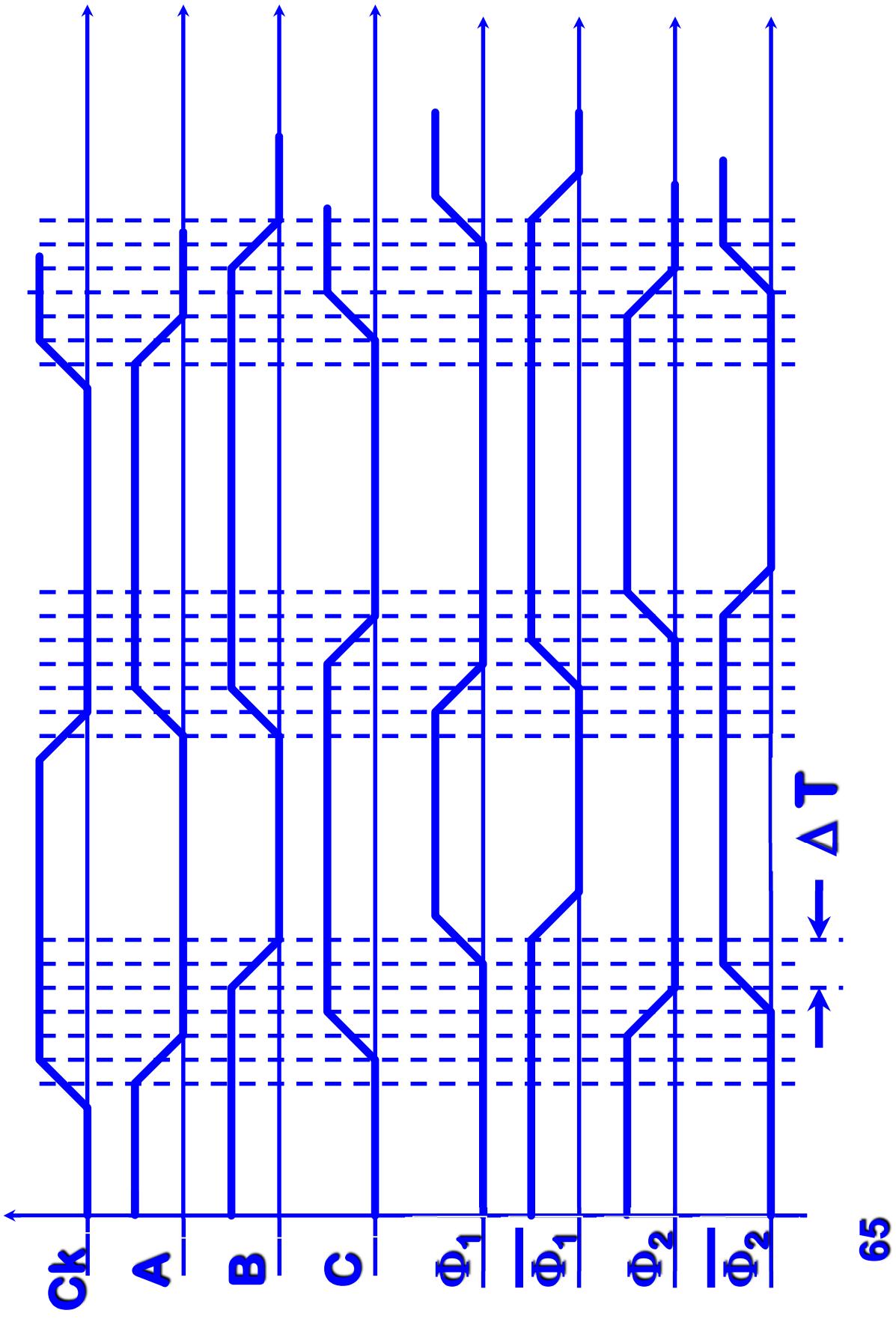


# Two Phases Clock Generation for CMOS (pseudo 4 phases clock)

- ❖  $\Phi$  and  $\bar{\Phi}$  are not derived by an inverter
- ❖ Two phases Clock even if 4 signals are present



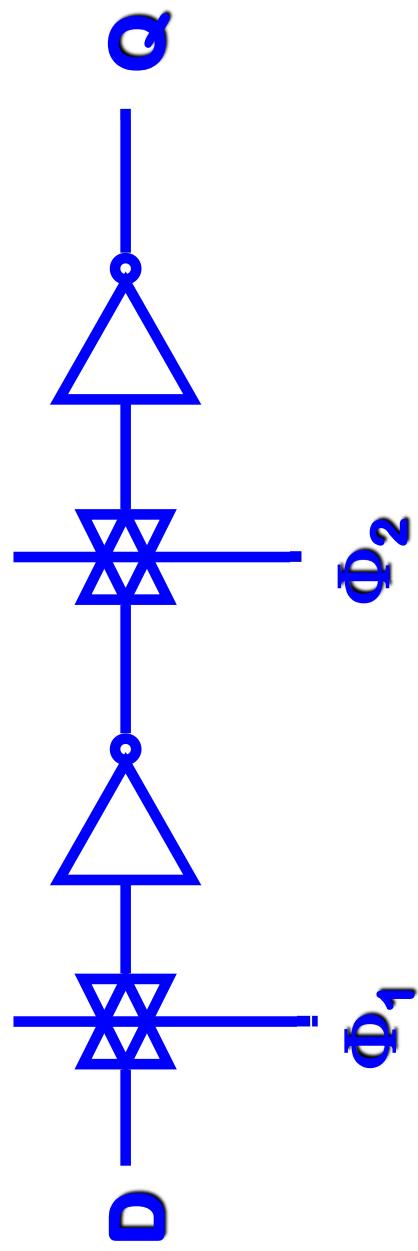
# Waveforms



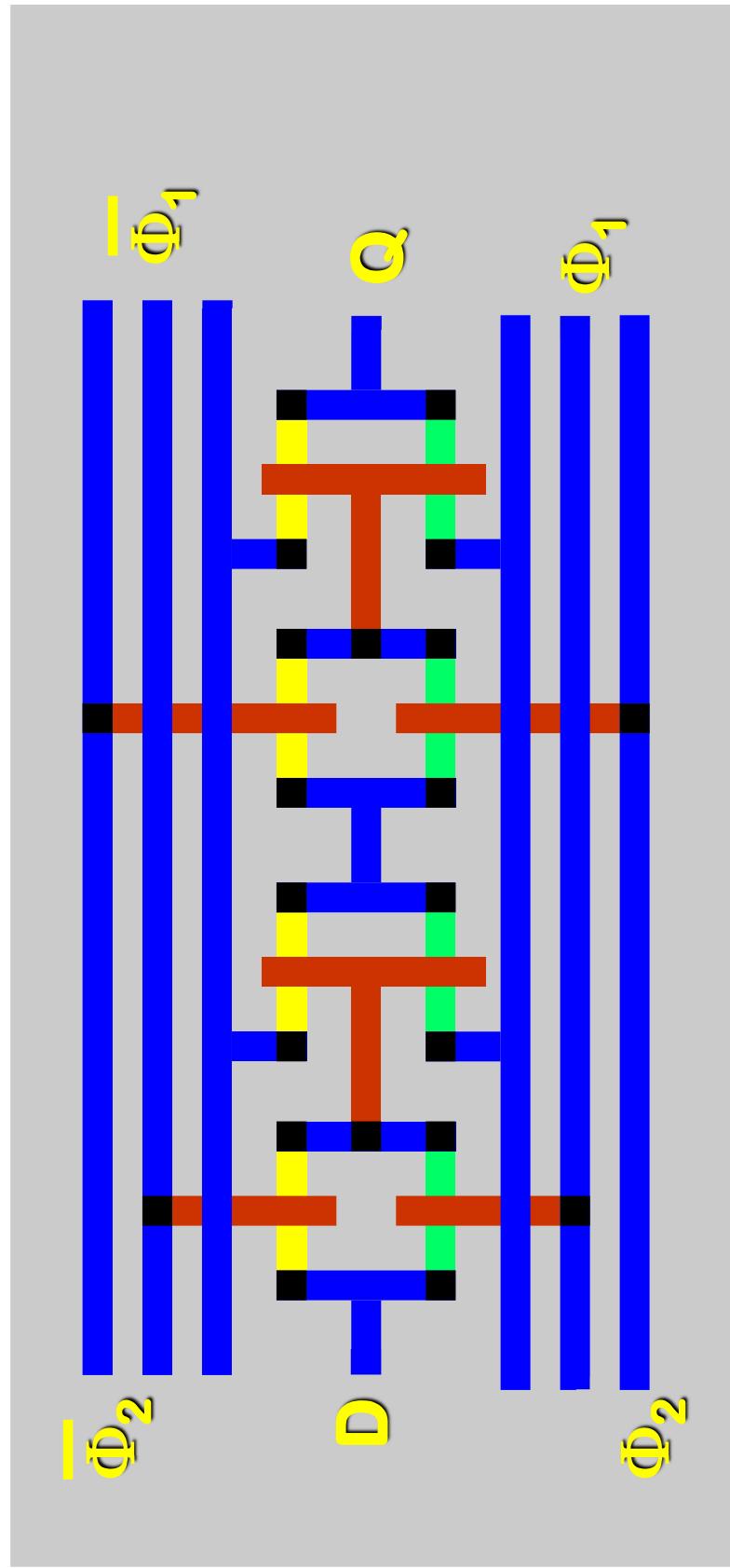
65

# Shift Register Basic Cell

- ★ Shift register is the basic cell in digital delay line
- ★ It is based on a dynamic flip flop D edge-triggered



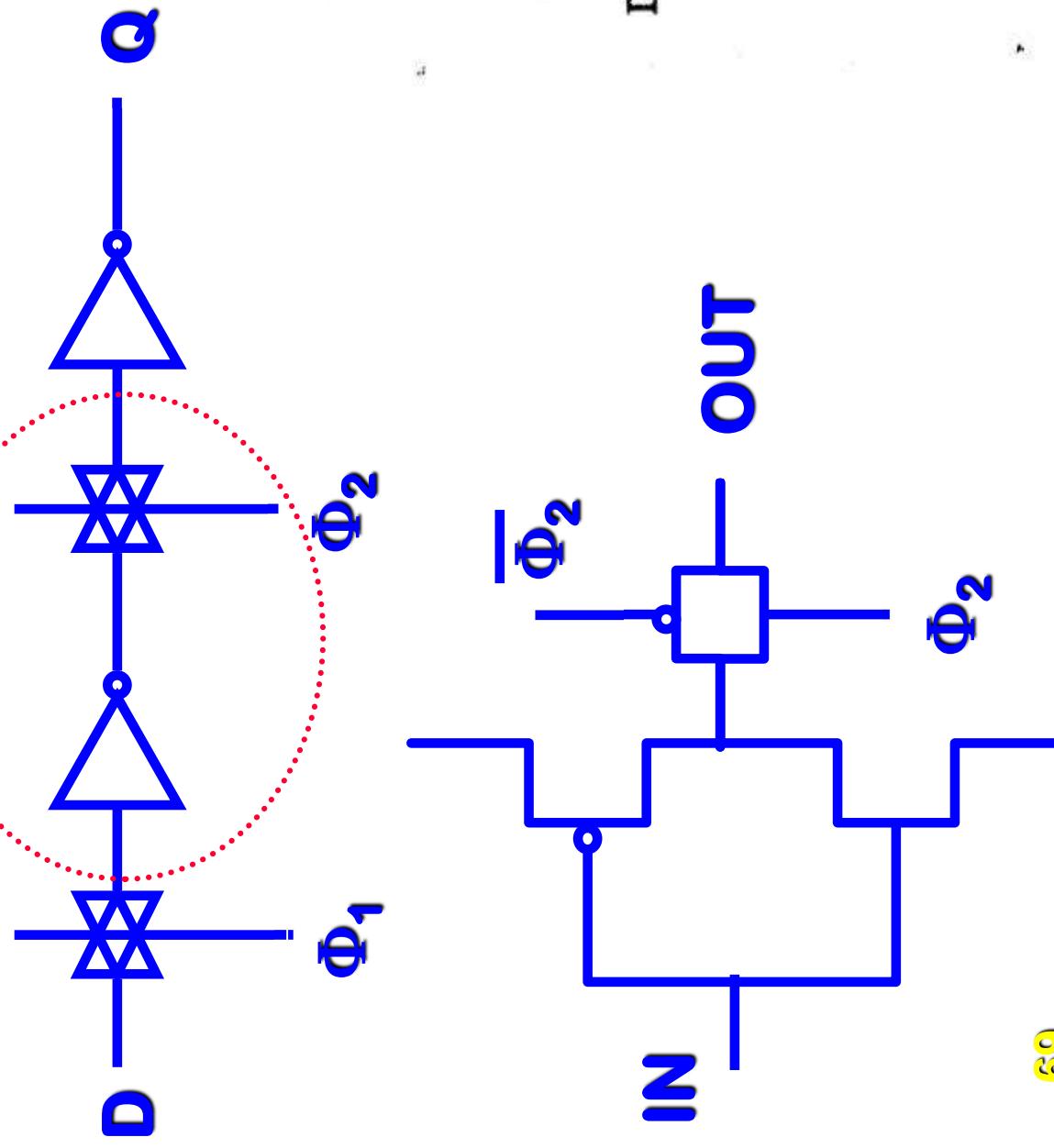
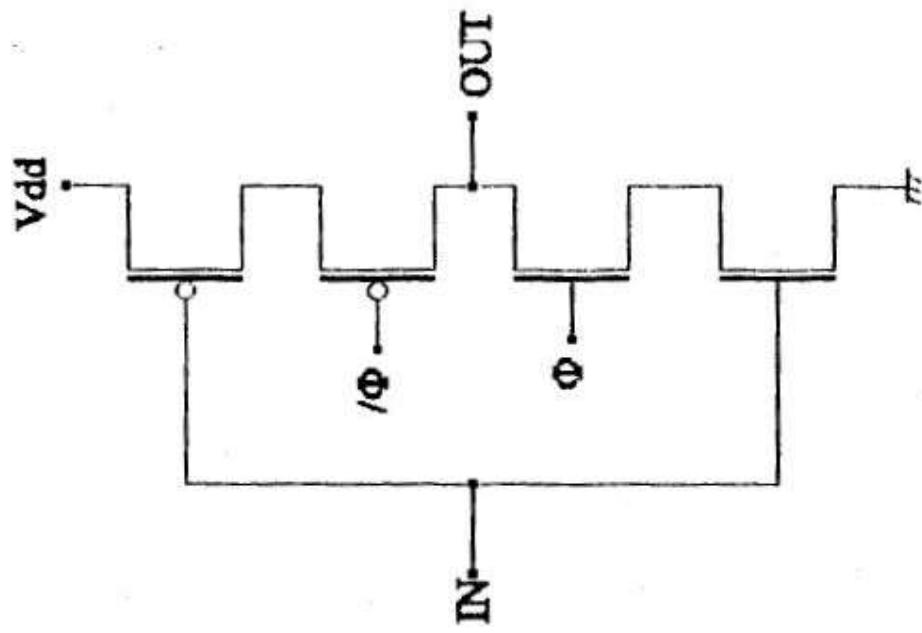
# Stick Diagram



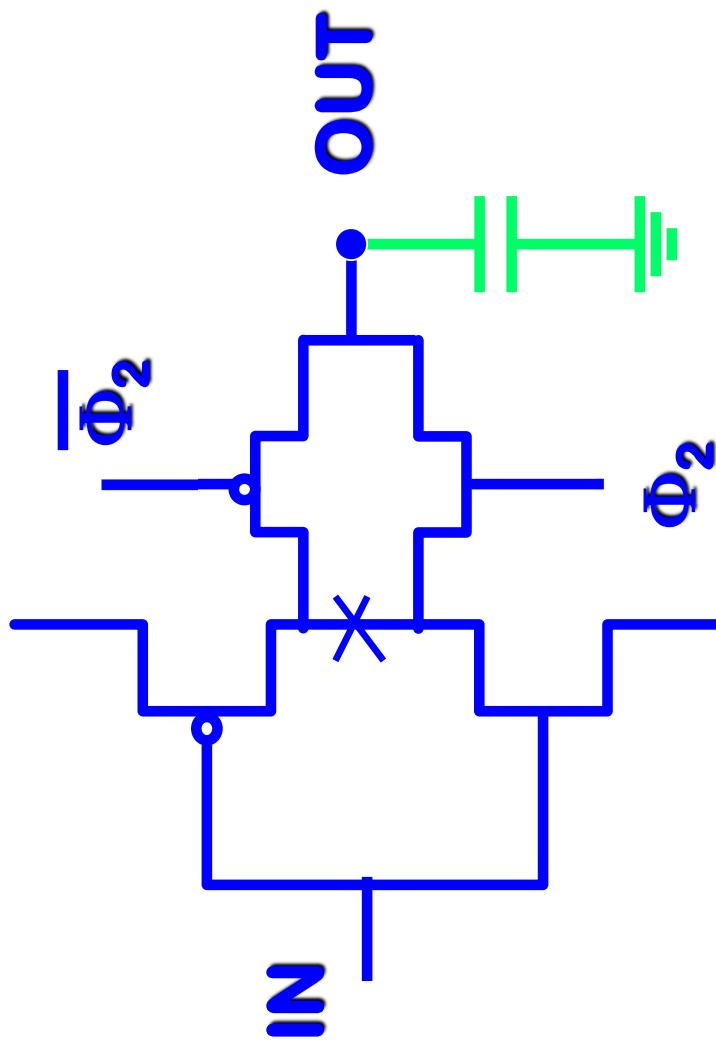
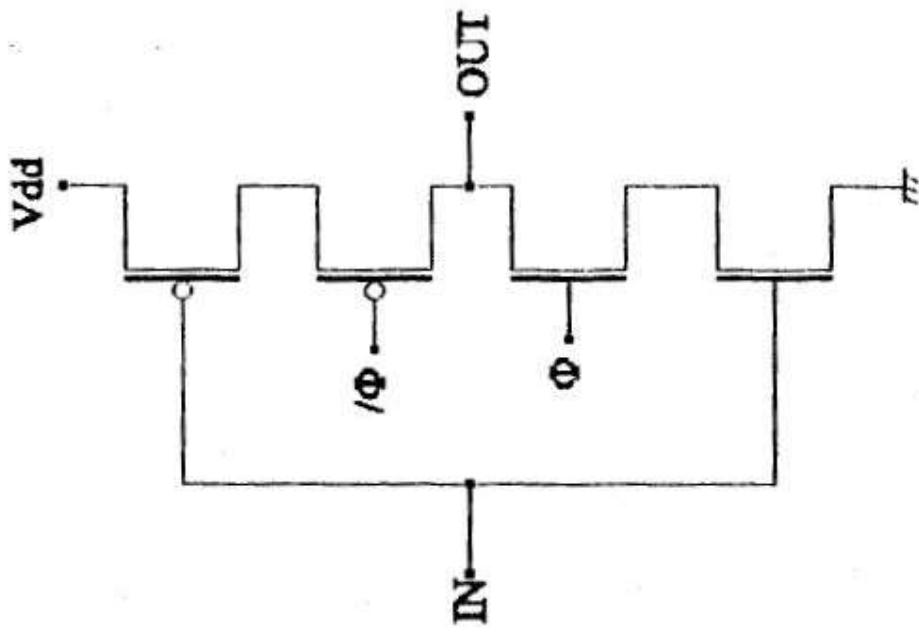
# Notes on Shift Register

- ❖ Wide spread used in digital designs
- ❖ Very simple structure
- ❖ Suitable for cell abutment
- ❖ Dynamic solution exploiting almost at the limit potential of selected silicon technology

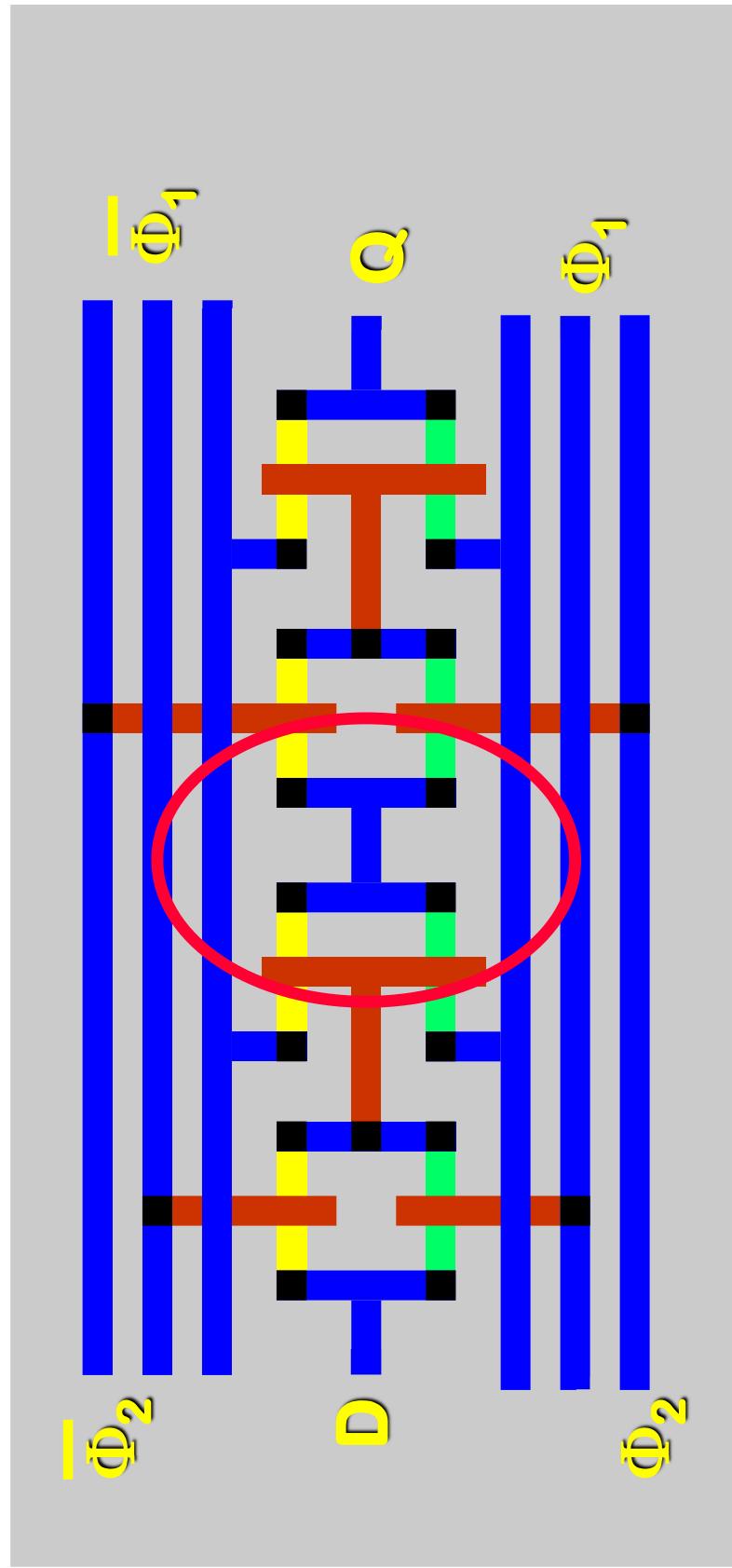
# Optimization: Clocked Inverter



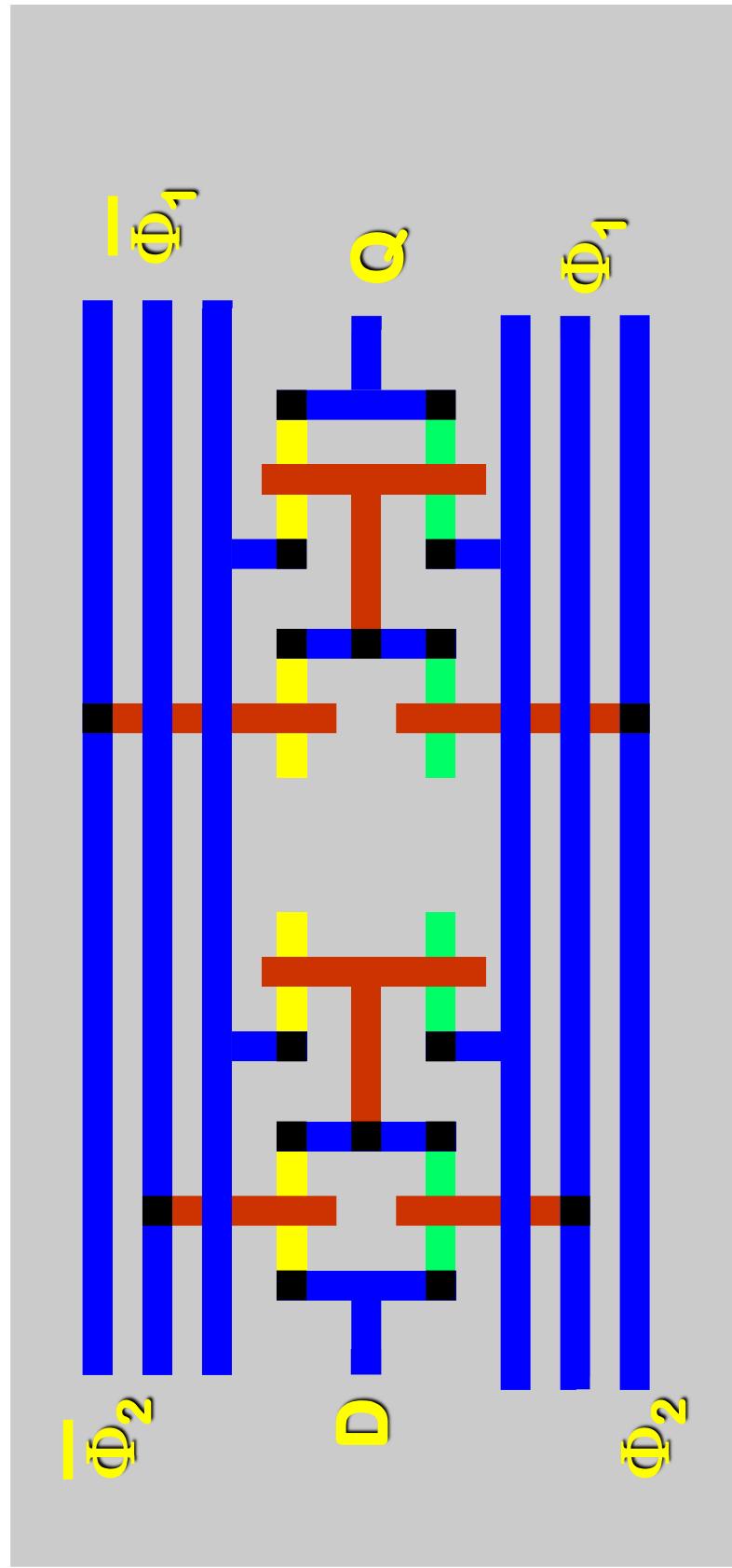
# Optimization: Clocked Inverter



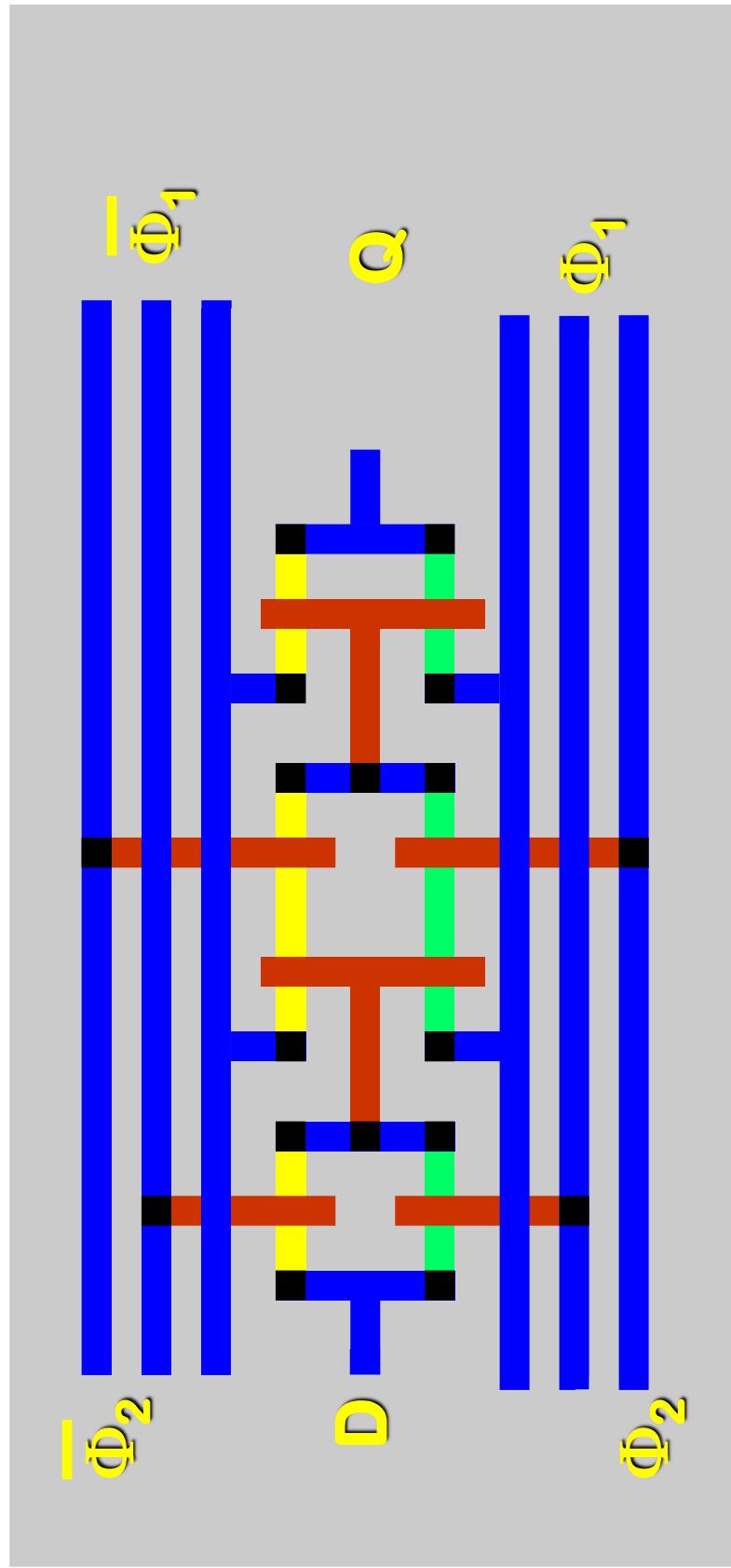
# Stick Diagram



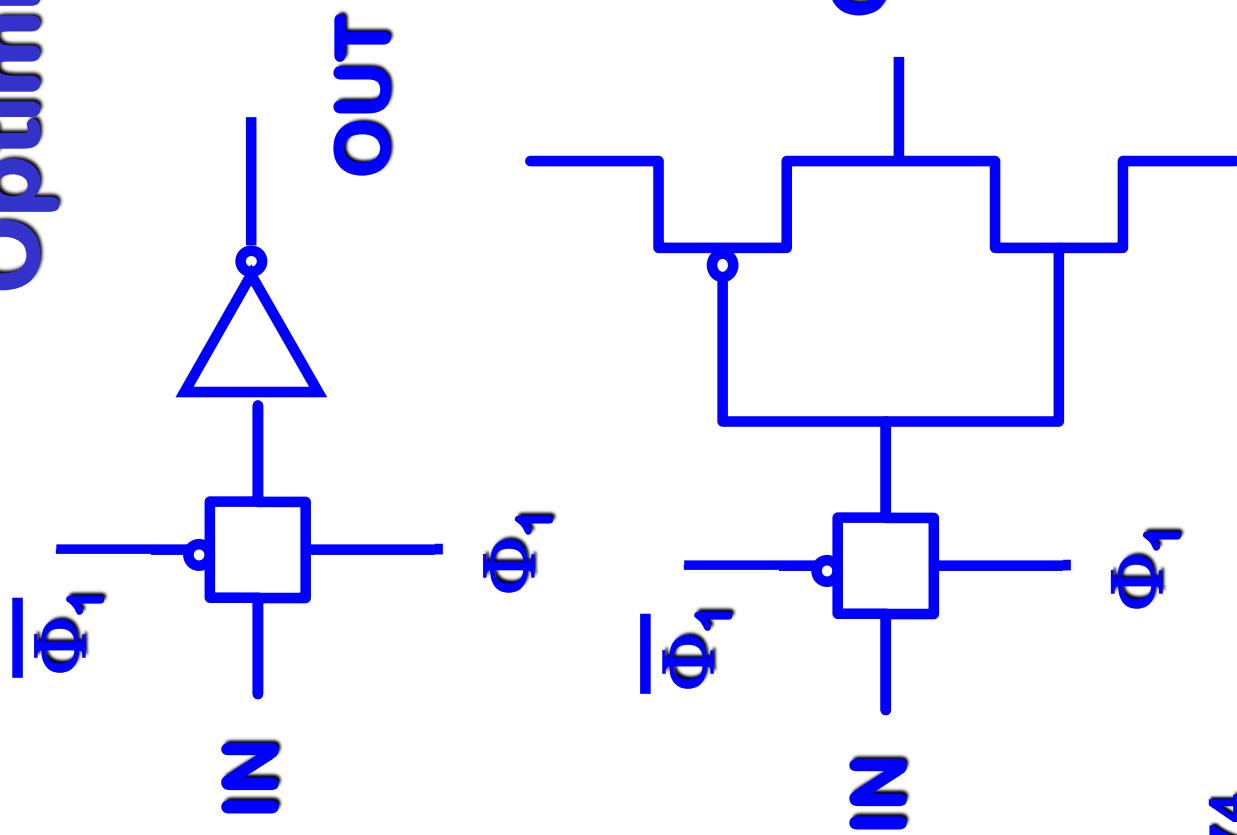
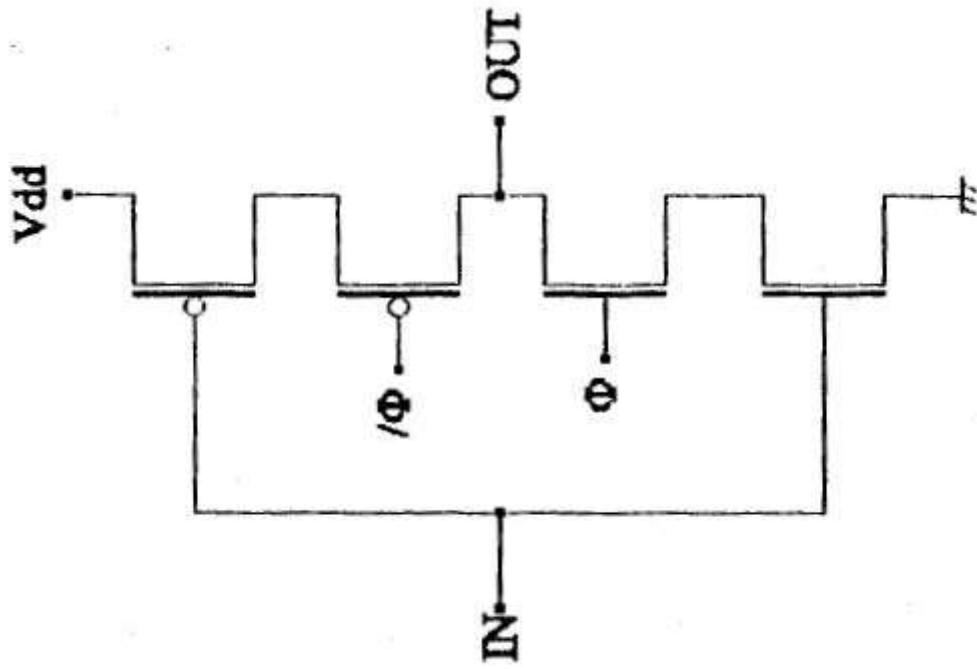
# Stick Diagram



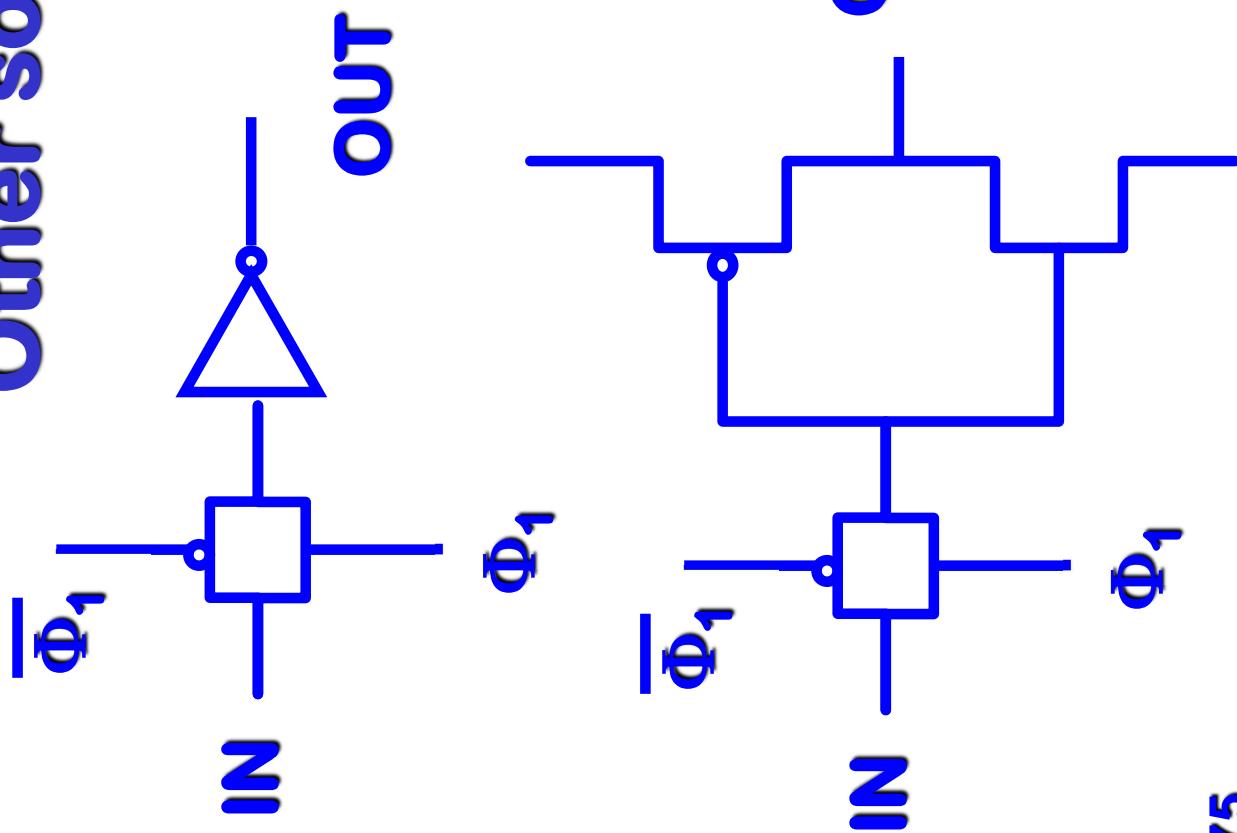
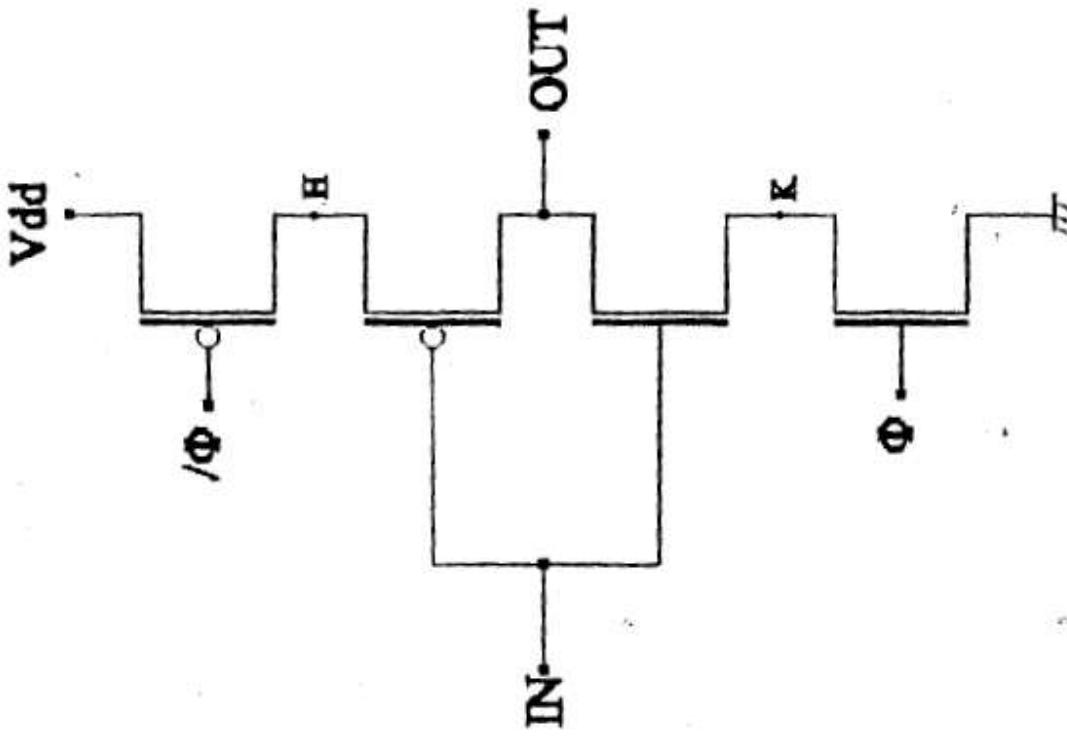
# Stick Diagram



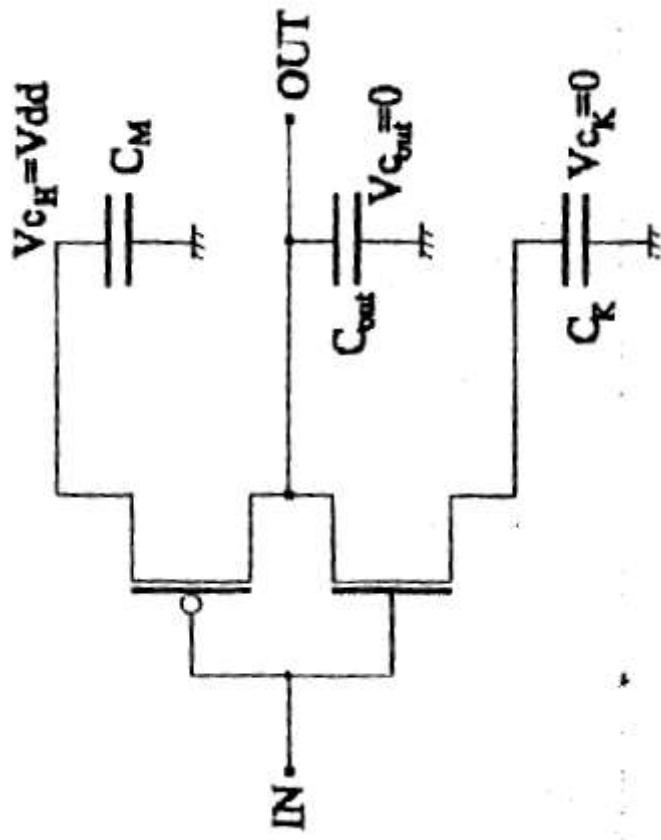
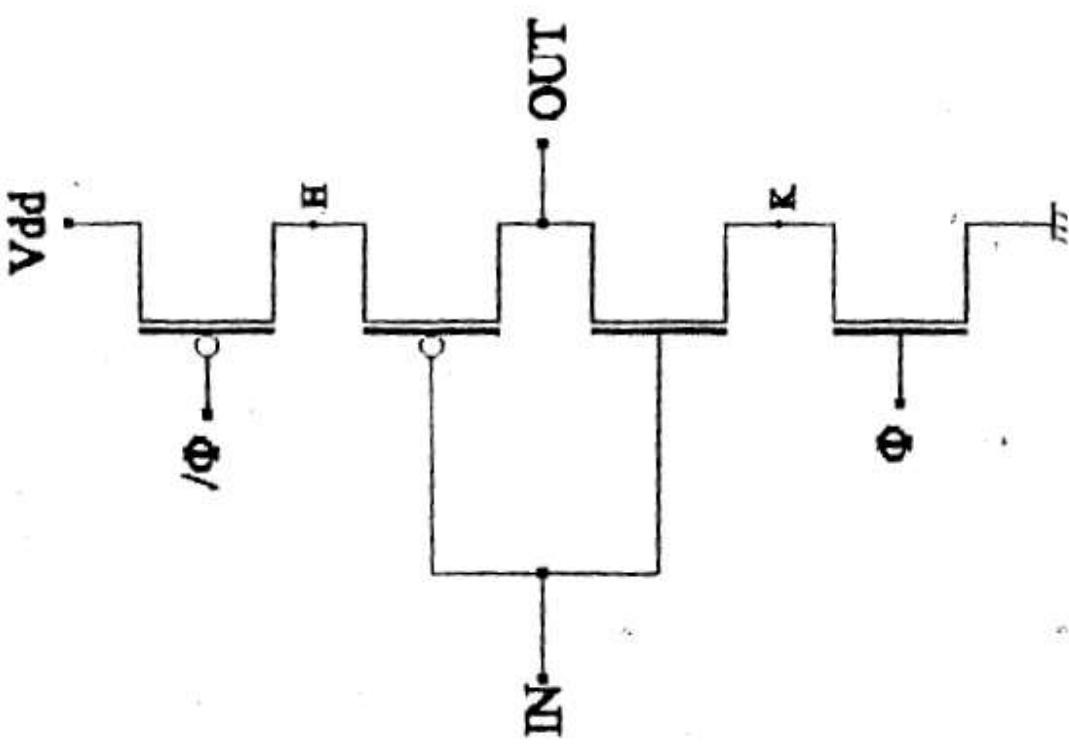
# Optimization



# Other solutions?



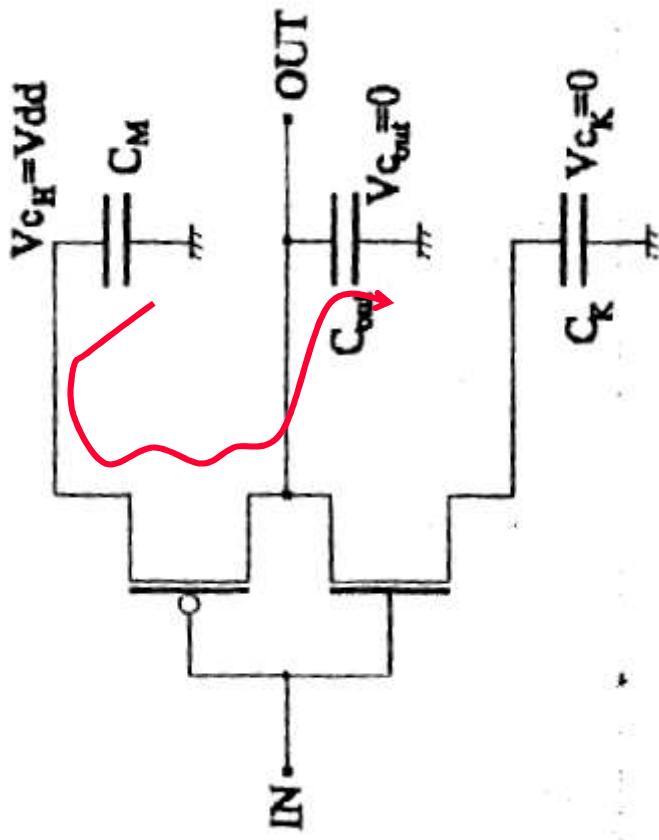
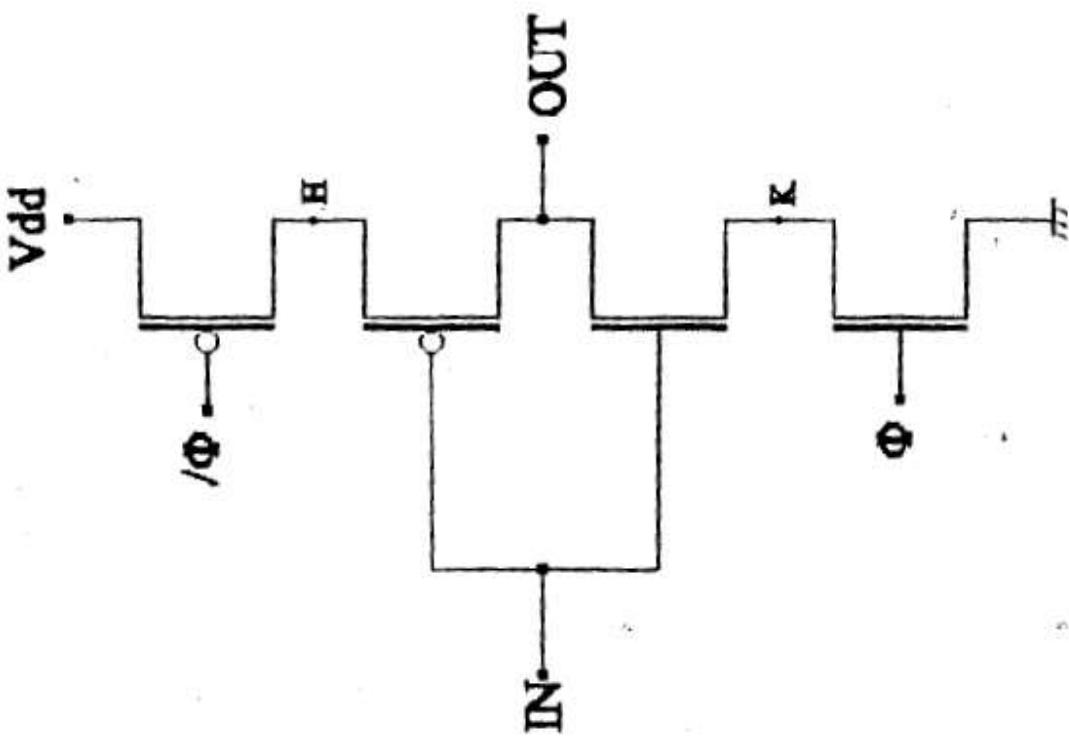
# Other solutions?



$\Phi_1 = 1 - \text{sensitive}$

$|N|=1$

# Other solutions? NO



$\Phi_1 = 0 \rightarrow \text{maintain}$

$\text{IN} = 1 \rightarrow 0$

# End, Questions ?

- **Flip Flop: Static Solution**
  - Flip- Flop S-R: NOR2 e NAND2
  - Flip-Flop S-R with enable
  - D -Latch
  - Flip Flop S-R Edge Triggered: NOR2, NAND2
  - Flip Flop D Edge Triggered: NOR2, NAND2, MUX
  - Flip Flop D Edge Triggered based on pass gate
- **Flip Flop: Dynamic Solution**
  - Flip Flop D Edge Triggered
  - Shift Register

