

Electronics and Communication Systems

Electronics Systems

Master Degree in Computer Engineering
<https://computer.ing.unipi.it/ce-lm>

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Outline

- **Electronic Abstraction Level Design**
- Integrated Circuit Design Styles
- Design Methodologies and Flows
- Cost-Performance Trade-off
- Field Programmable Gate Array
- Design Productivity
- Evolution of EDA Industry
- How to map a system/algoritm to a System on Chip

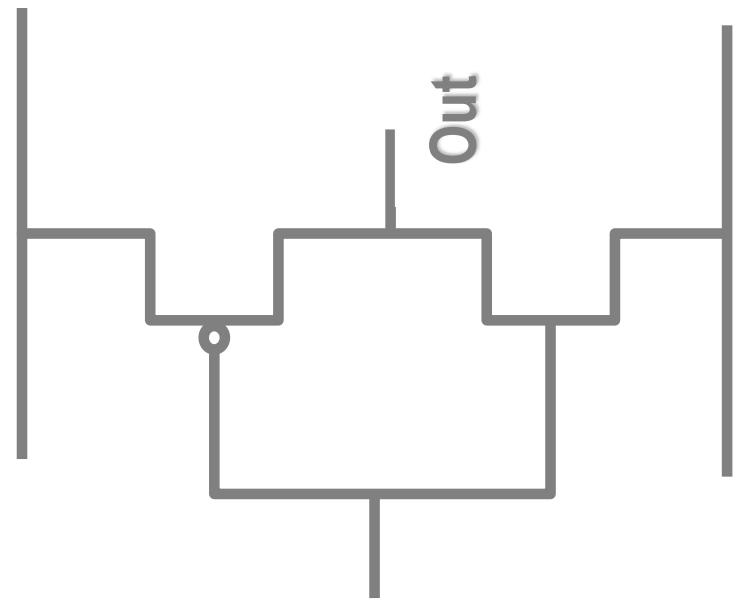
Inverter: Electronic Abstraction Levels

RTL

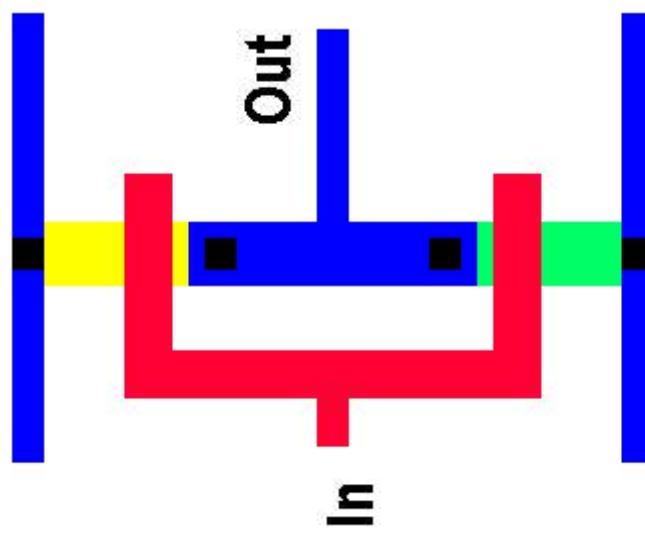
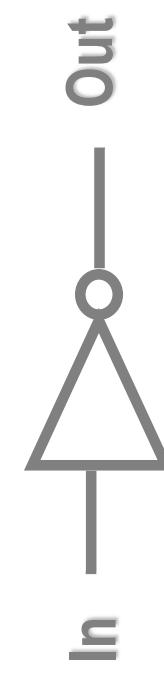
Transistor

Lay-out

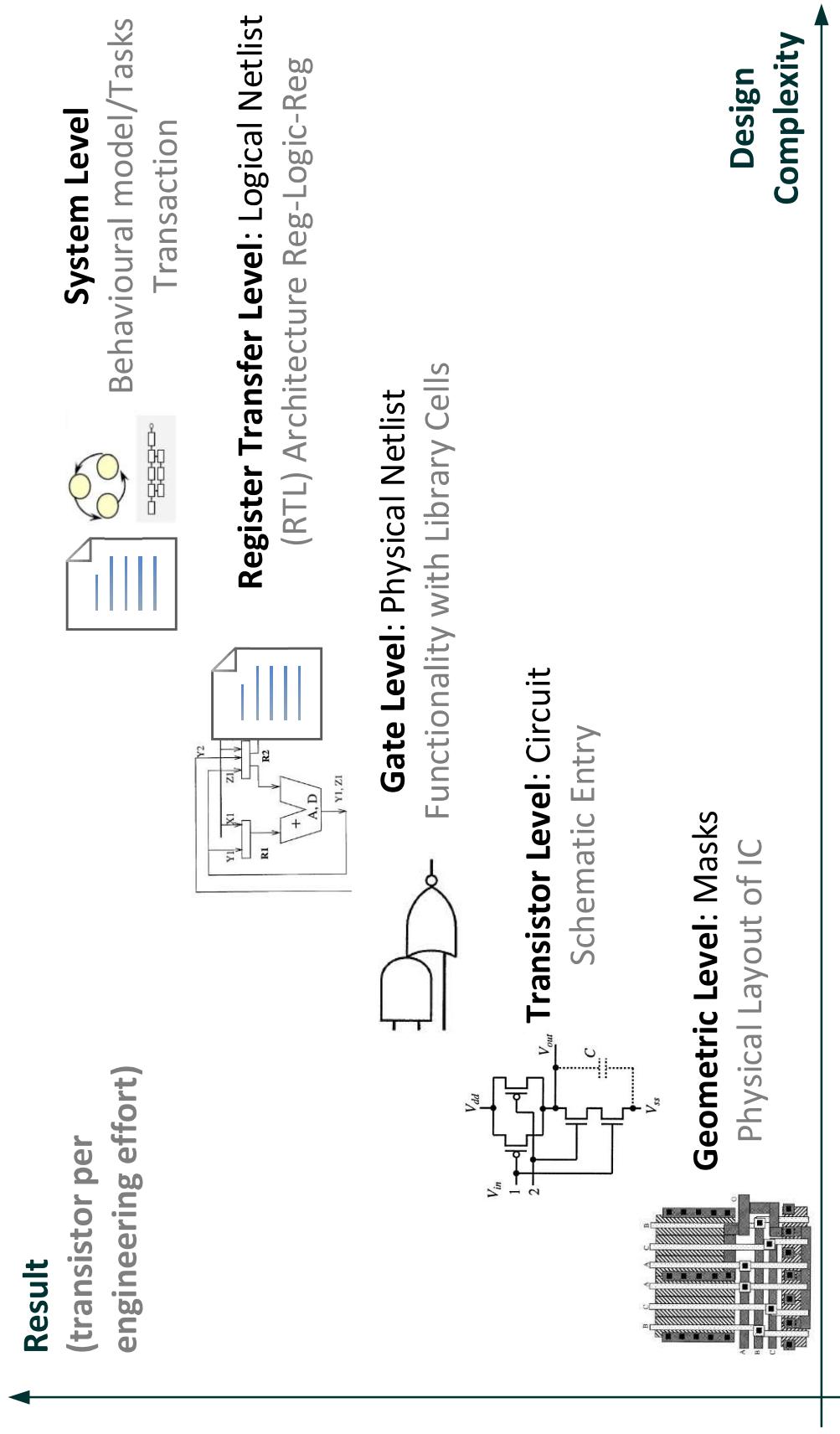
$$\text{Out} \leftarrow \text{NOT}(\text{In})$$



Gate



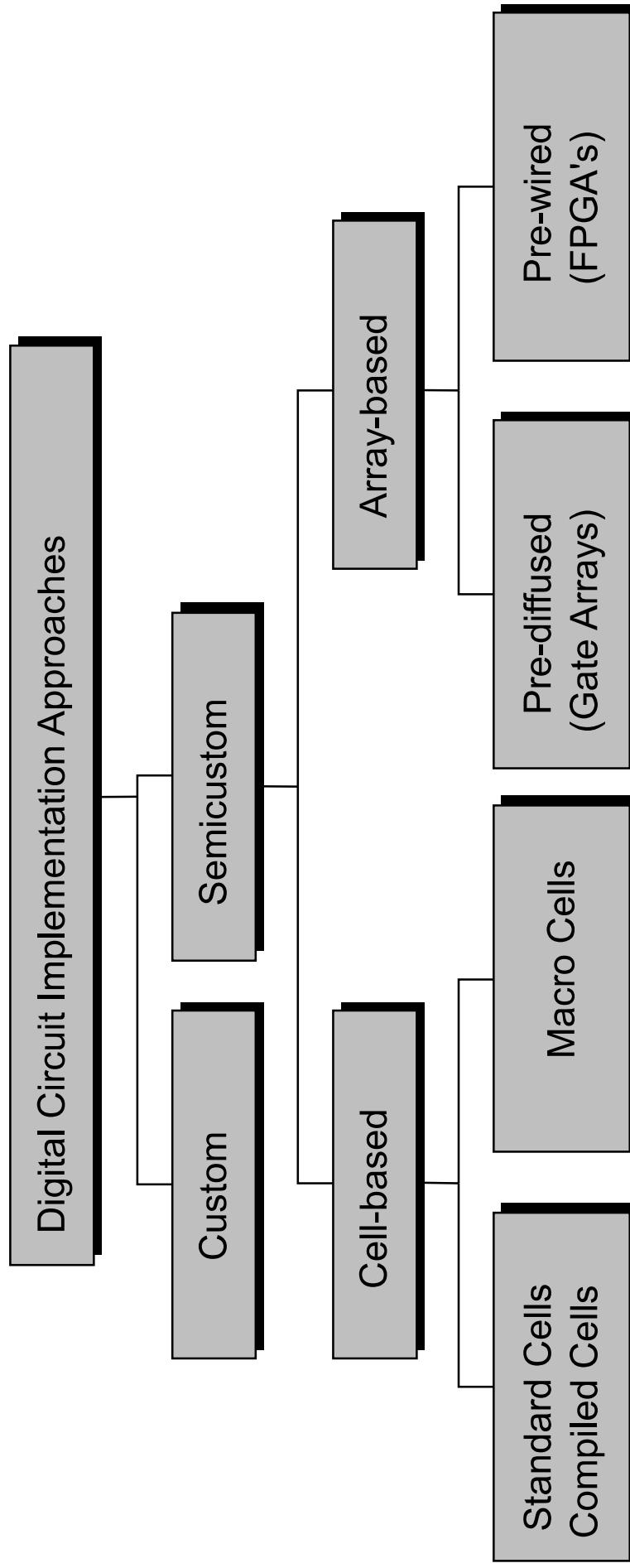
Electronic Abstraction Level Design



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- **Integrated Circuit Design Styles**
- **Design Methodologies and Flows**
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Integrated Circuit Design Styles



**Let's see the main difference among
these implementation approaches !!**

ASIC Design Approaches

- **full-custom**

- **Maximum Design Freedom:** sizing, placement and interconnection for each single transistor

- **semi-custom**

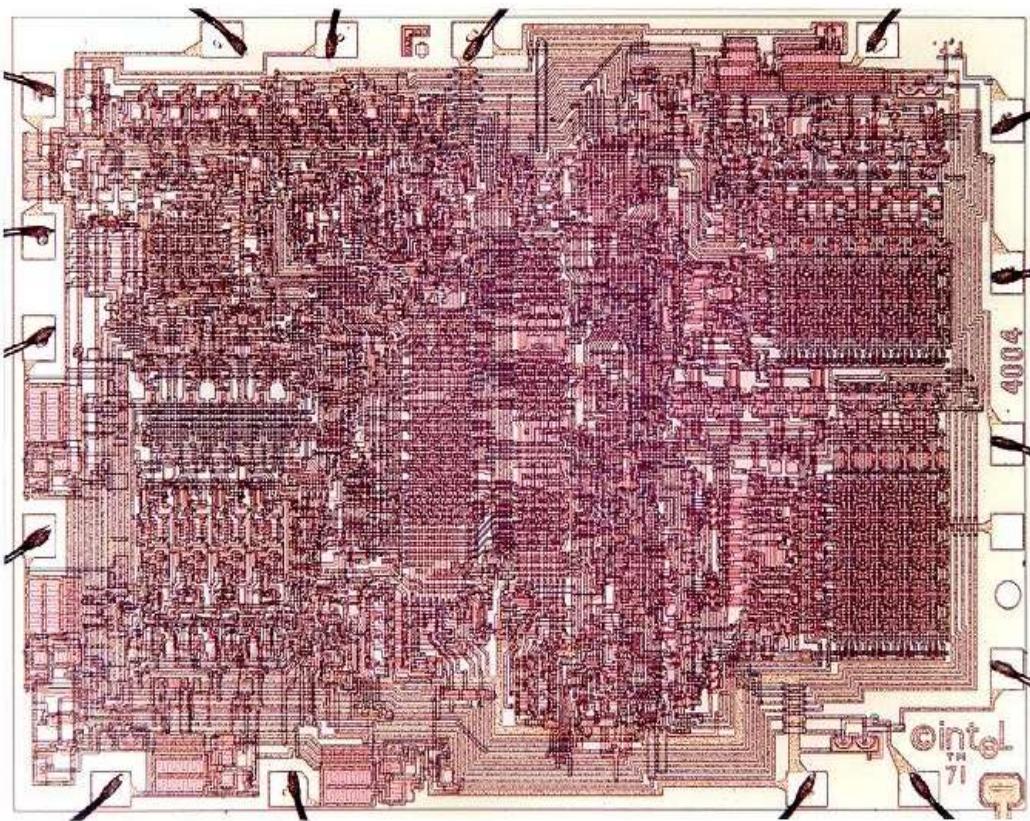
- **Reduction of some Design Freedom:** based on pre-designed and/or pre-manufactured logic structures (transistor, gate, logic cells) and defining only their interconnection

ASIC full-custom

- Maximum Design Freedom
- Maximum Potential of Optimization
 - speed
 - area complexity
- High Cost and Development time
- High skills required on ASIC technology, Electronic Circuit and Architecture

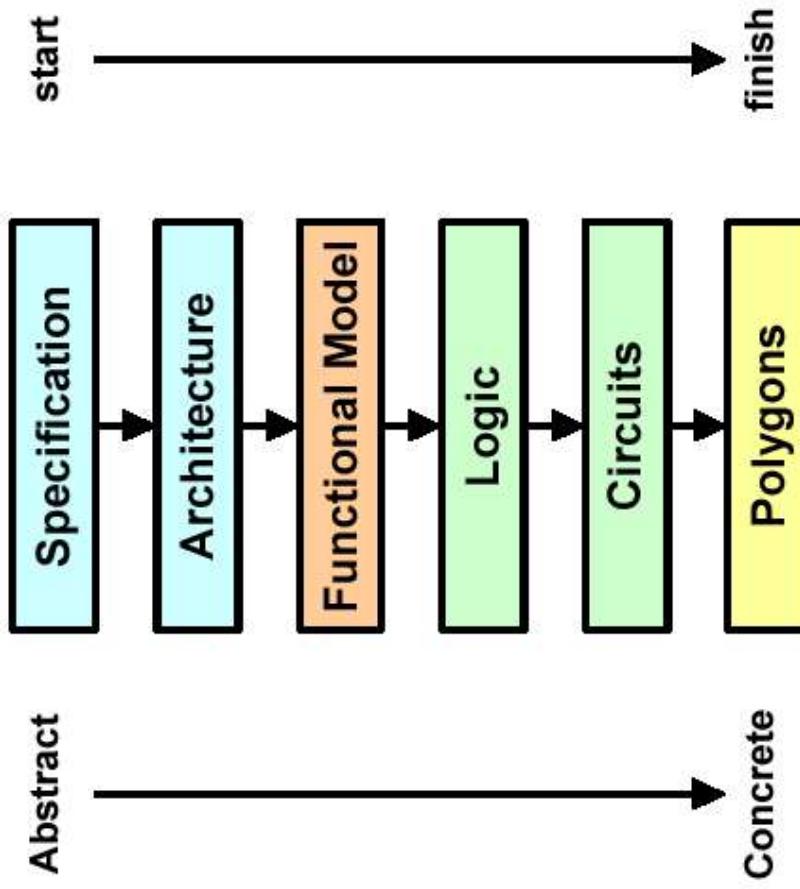
The Custom Approach

Intel 4004



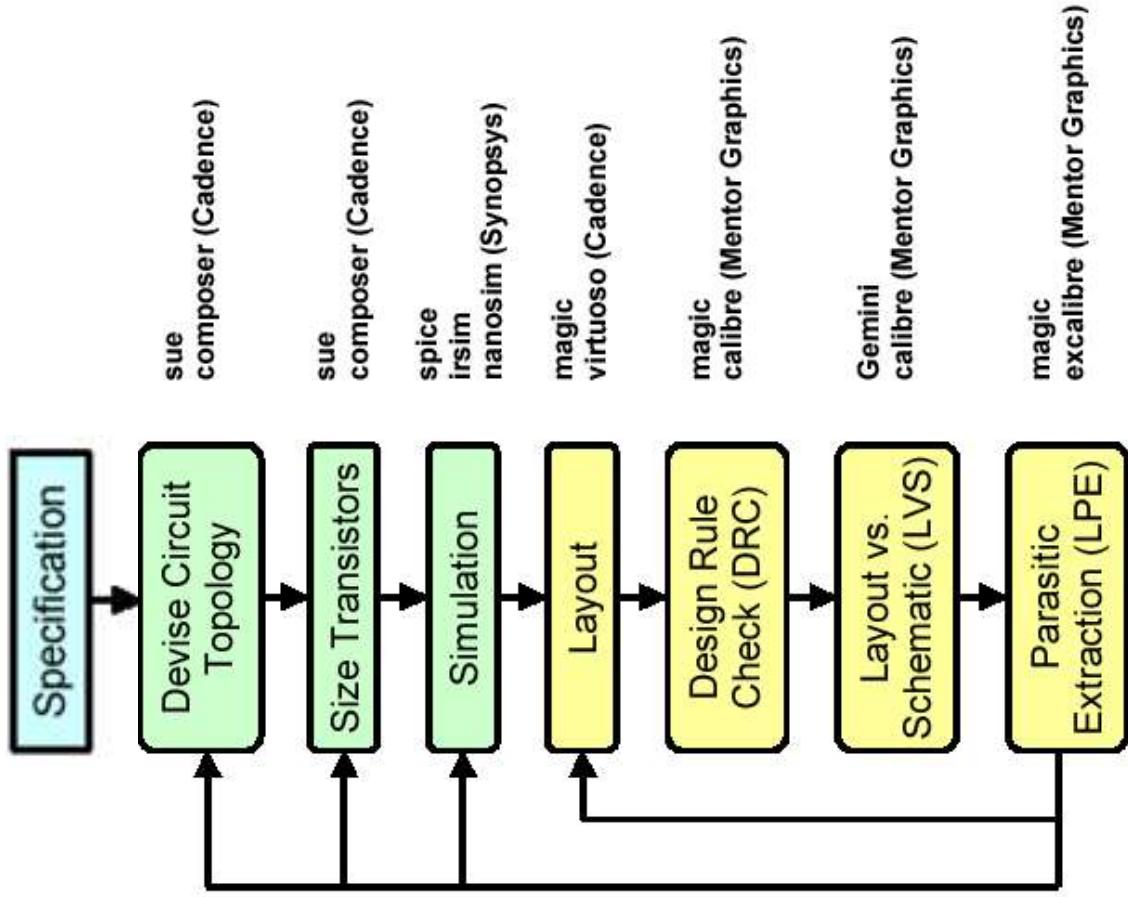
Levels of Design Abstraction

- Consider entire design at top levels only
 - Increasing amounts of automation possible further down the stack

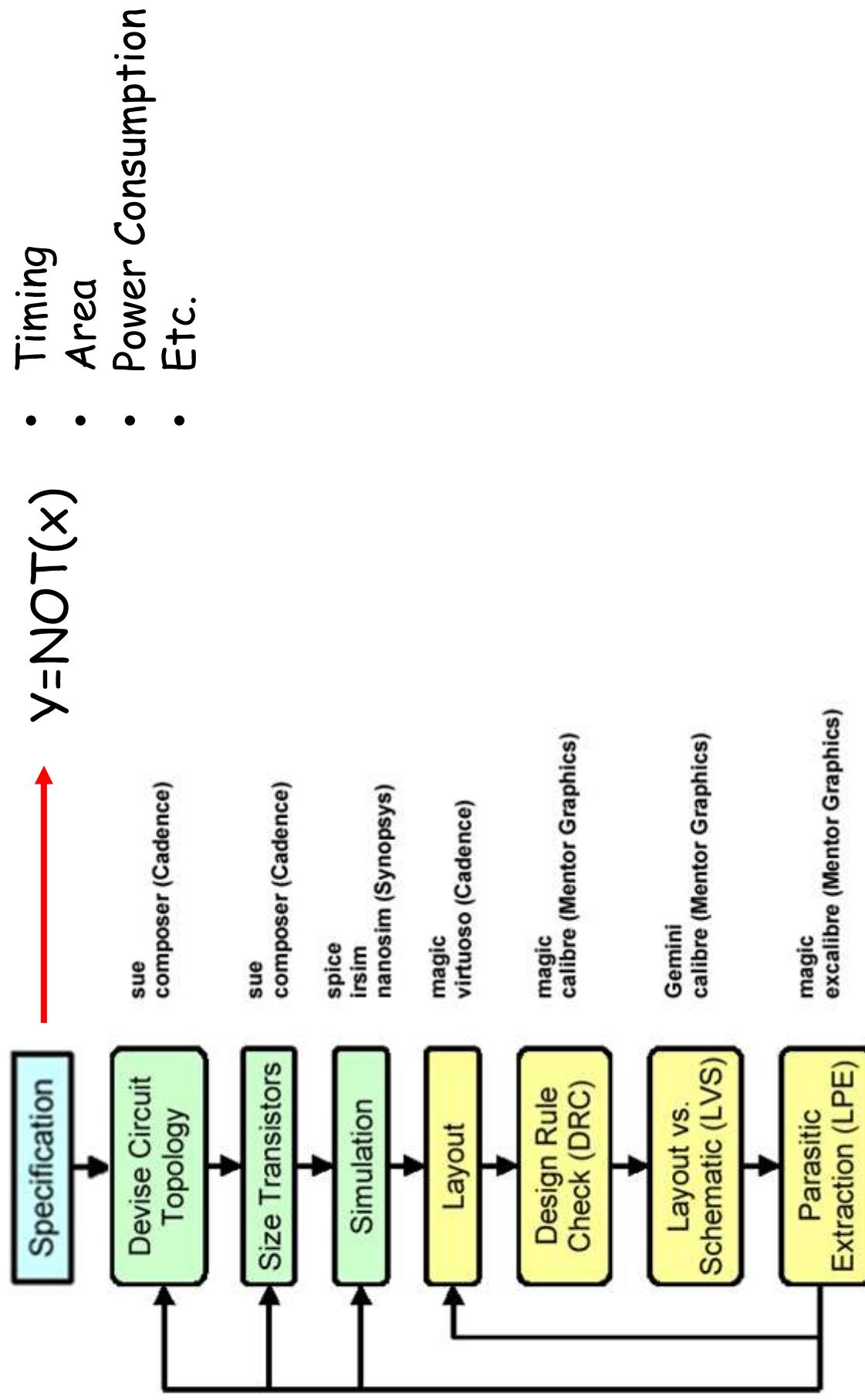


Full Custom Design Flow

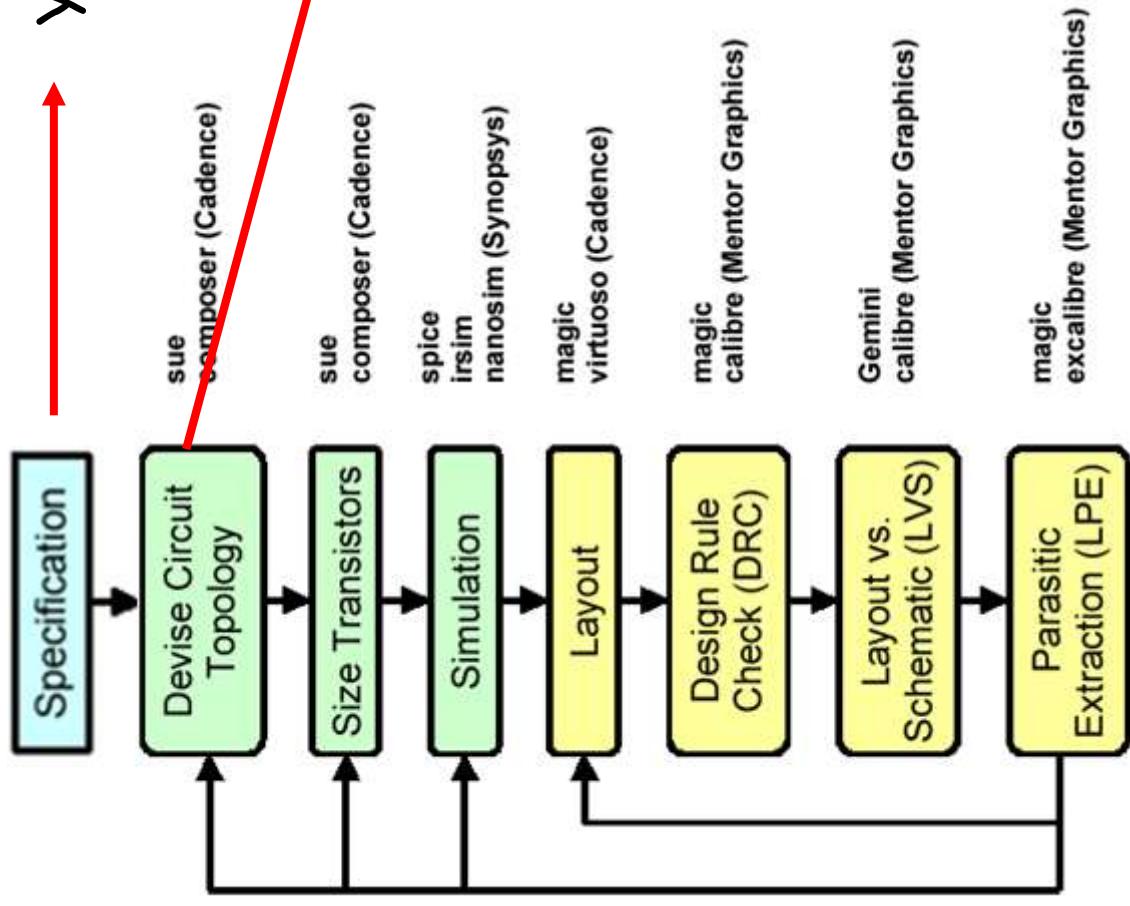
- Has the best performance
- Is the most labor intensive



Full Custom Design Flow

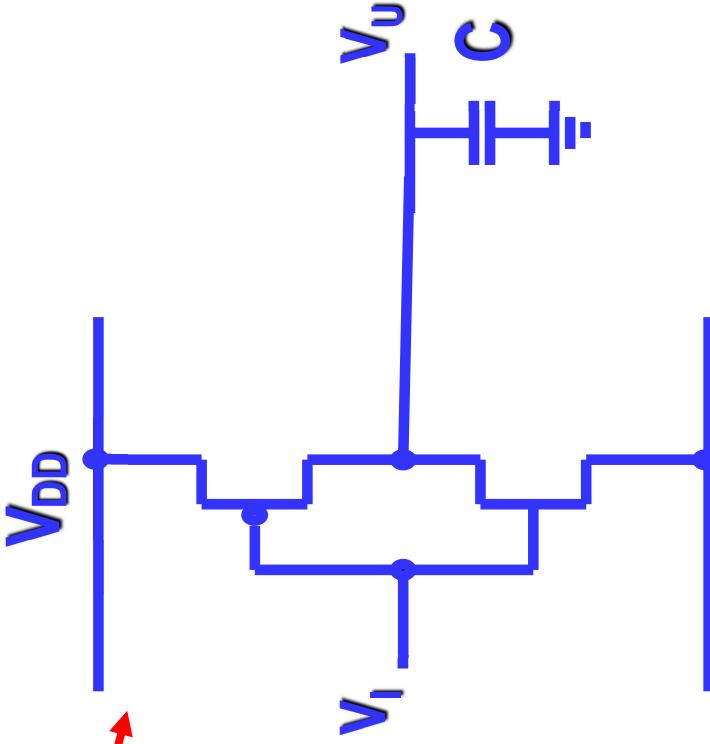


Full Custom Design Flow

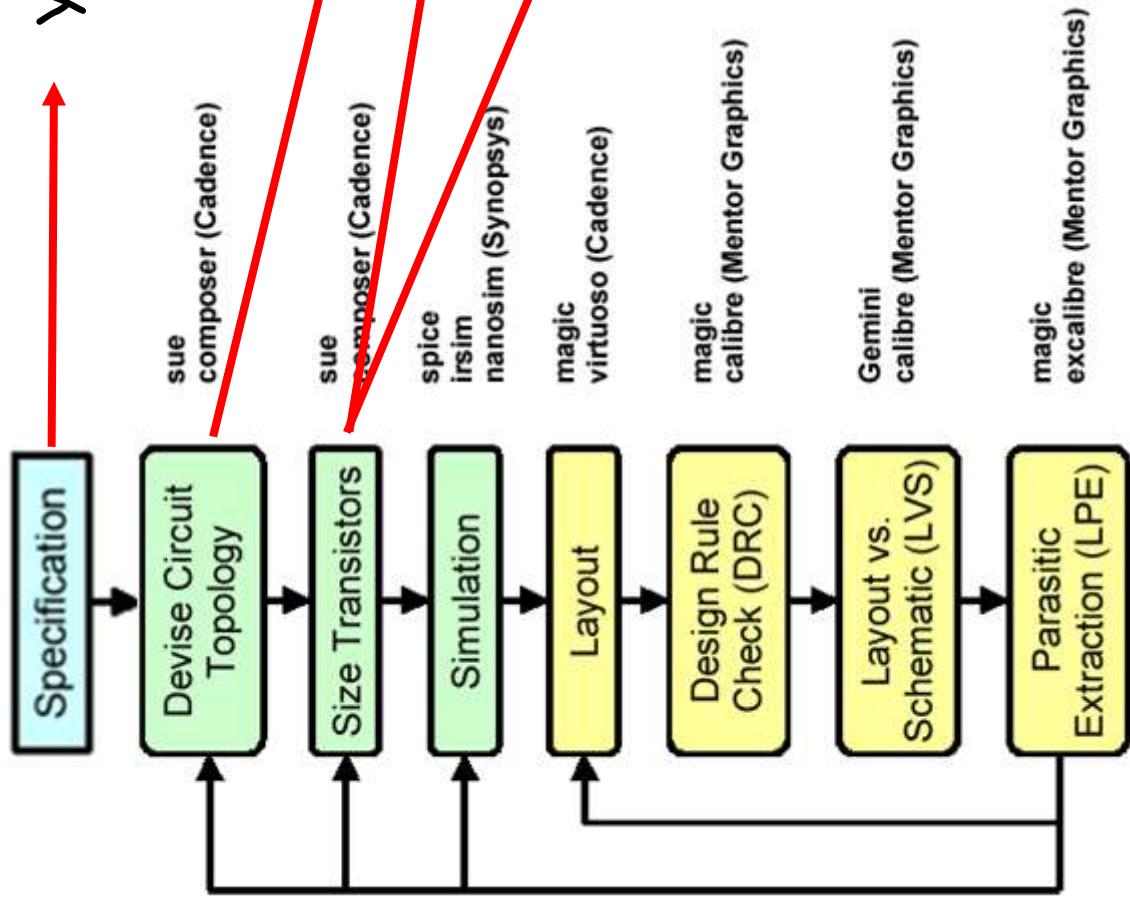


- $y = \text{NOT}(x)$
- Timing
- Area
- Power Consumption
- Etc.

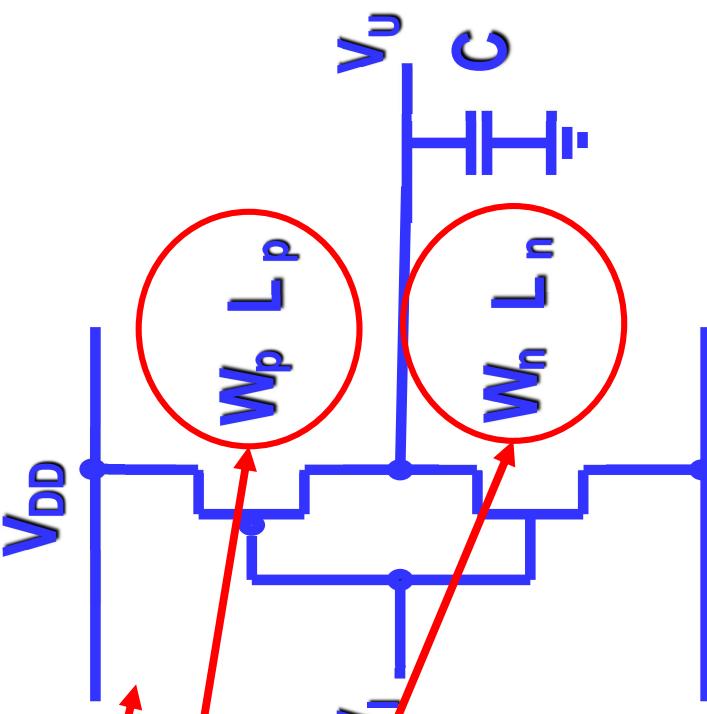
Red arrow pointing to the first item in the list: $y = \text{NOT}(x)$



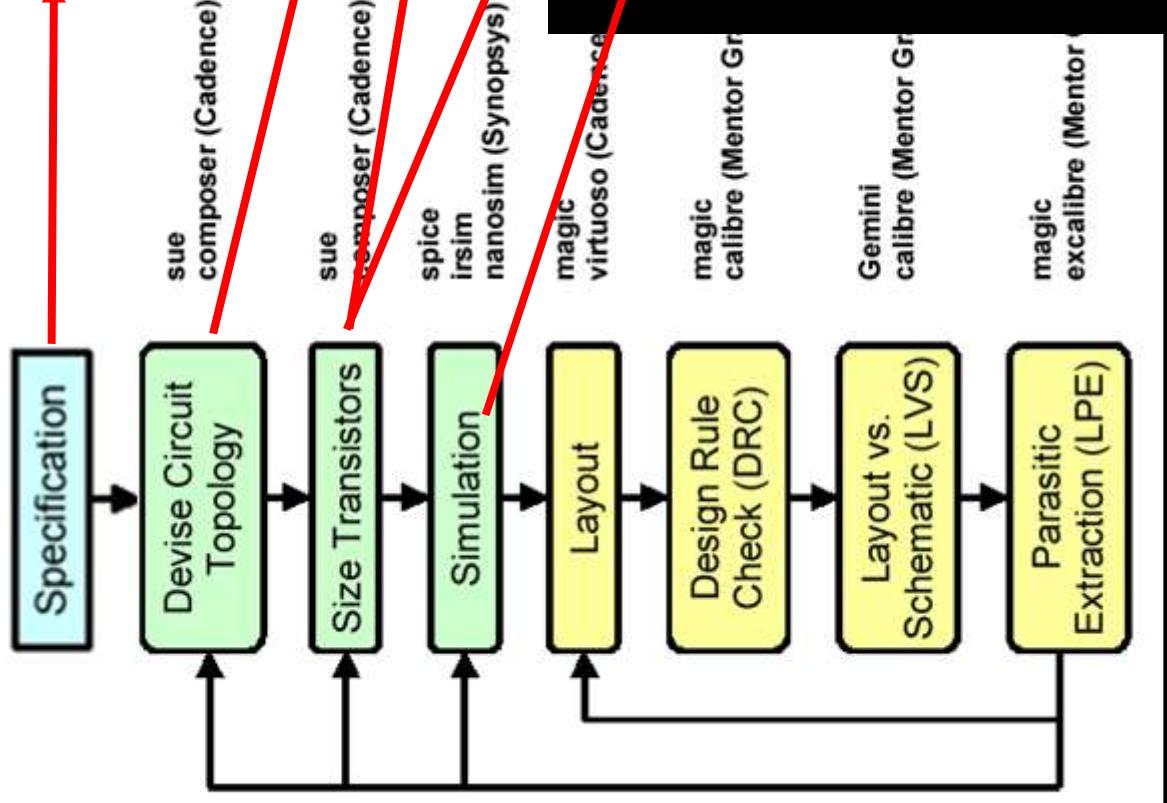
Full Custom Design Flow



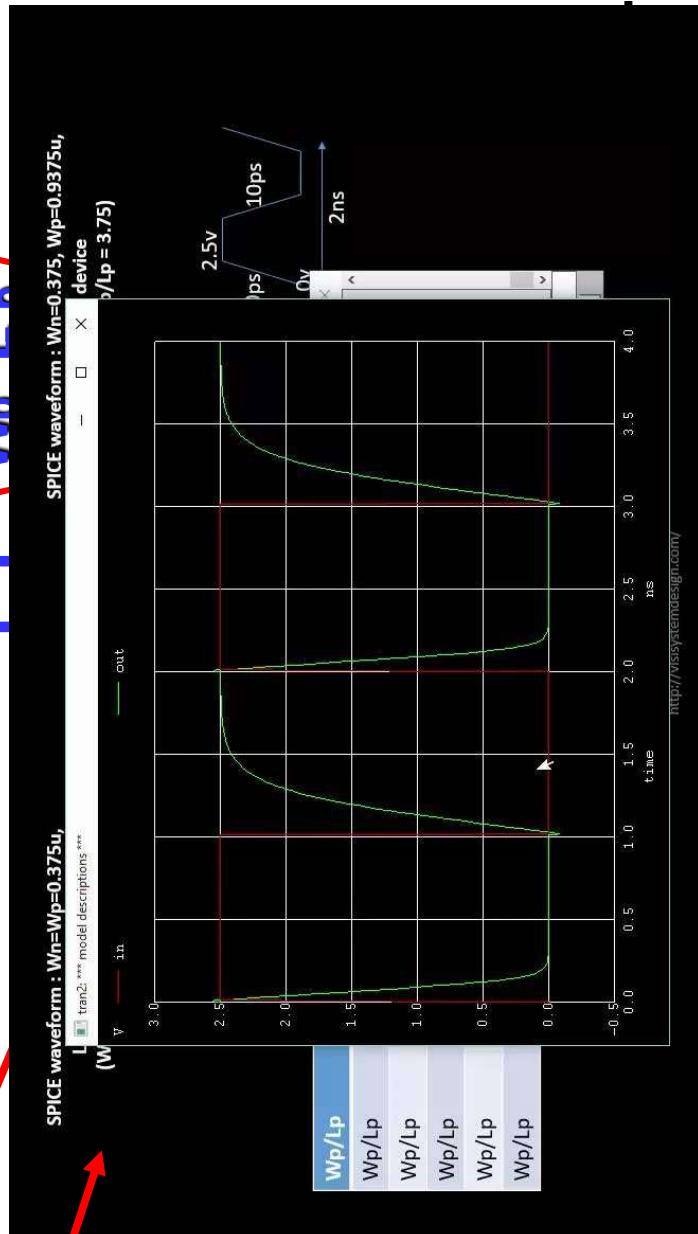
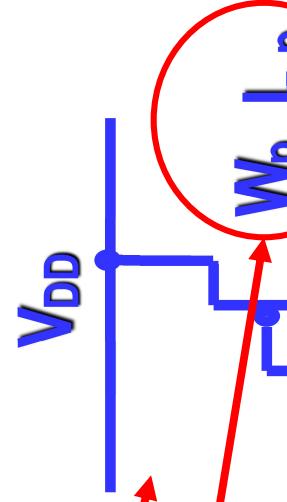
- Timing
- Area
- Power Consumption
- Etc.



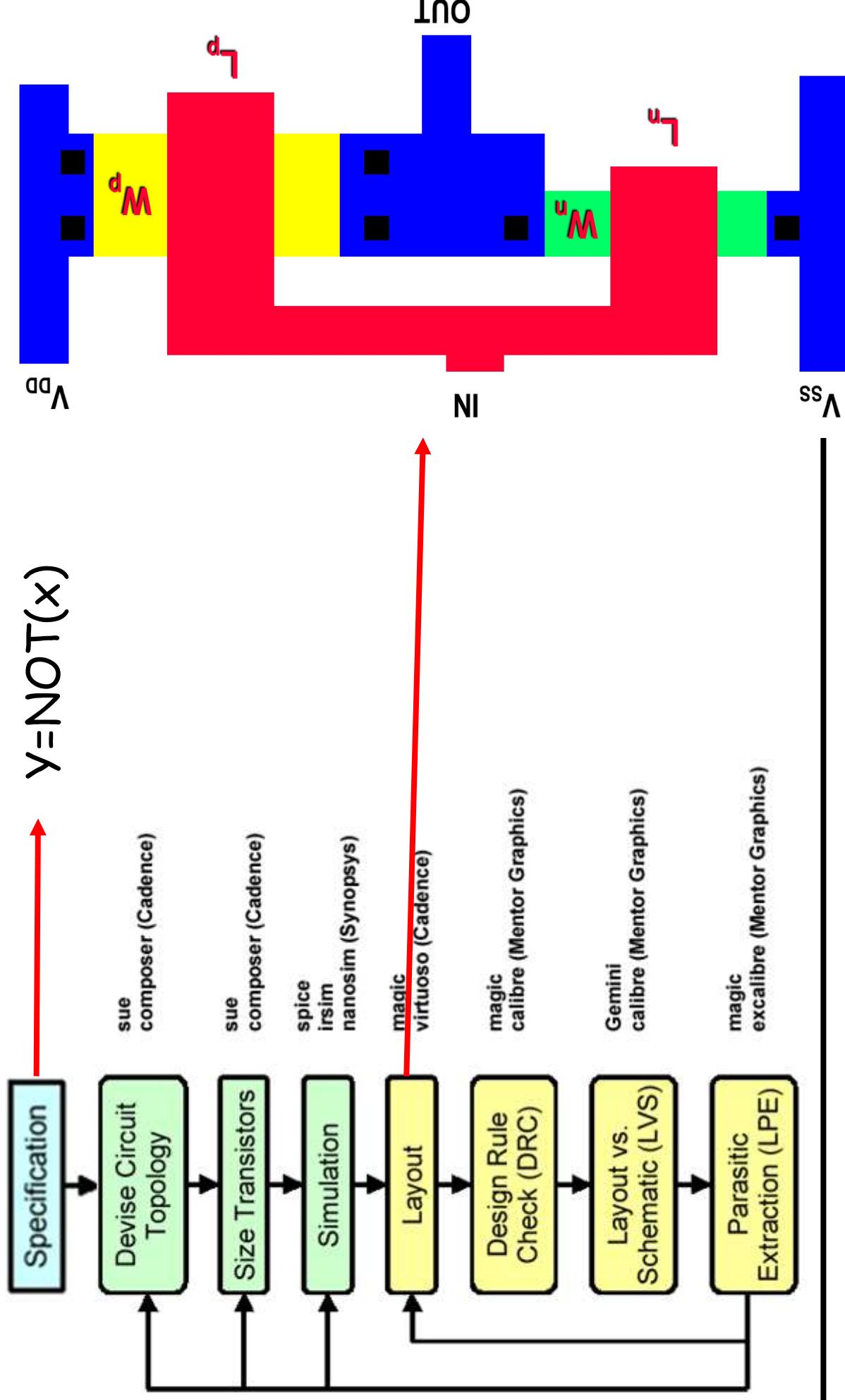
Full Custom Design Flow



$$y = \text{NOT}(x) \quad \begin{array}{l} \bullet \text{ Timing} \\ \bullet \text{ Area} \\ \bullet \text{ Power Consumption} \\ \bullet \text{ Etc.} \end{array}$$

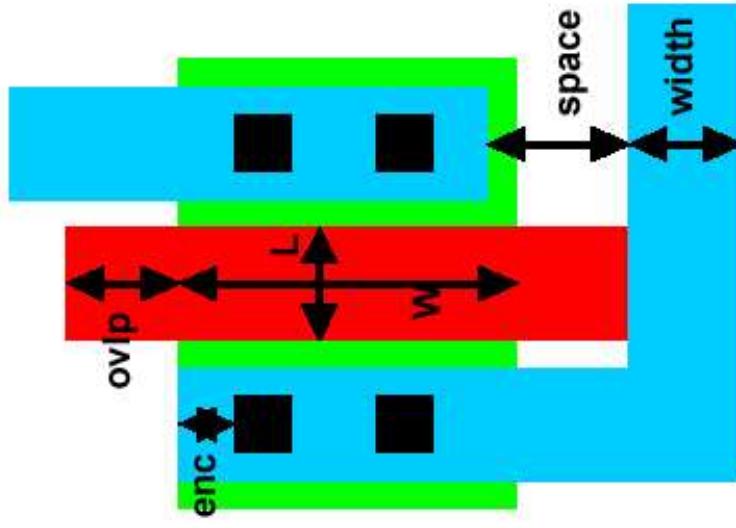


Full Custom Design Flow



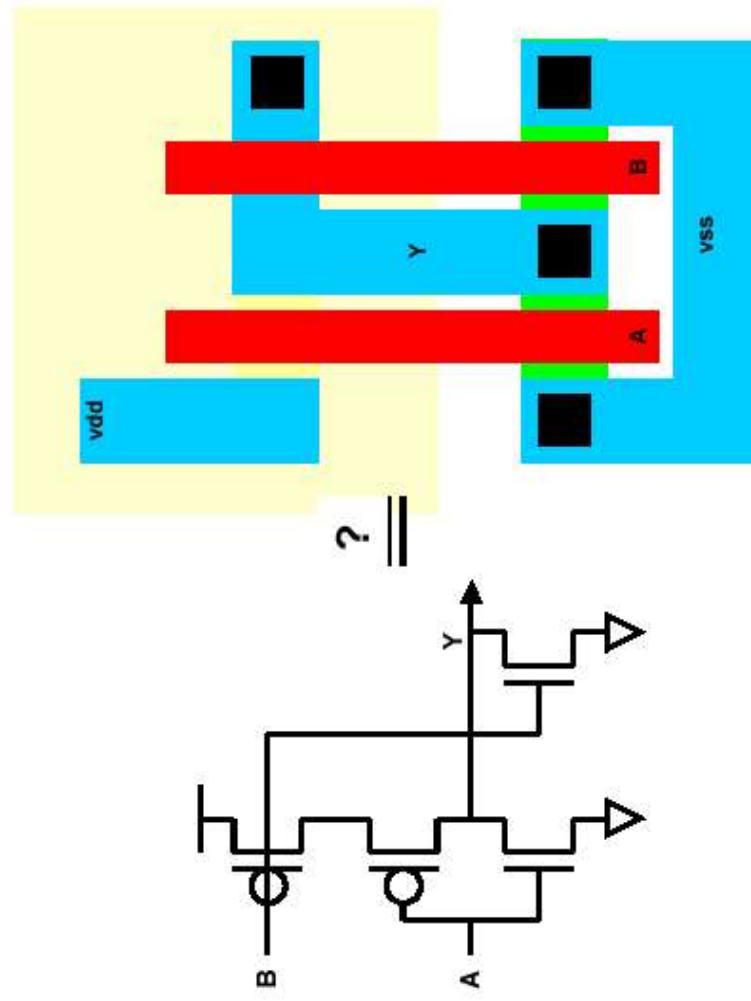
Design Rule Checking (DRC)

- Fab has rules for relationships between polygons in layout
 - Required for manufacturability
- DRC checker looks for errors
 - width
 - space
 - enclosure
 - overlap
 - Violations flagged for later fixup

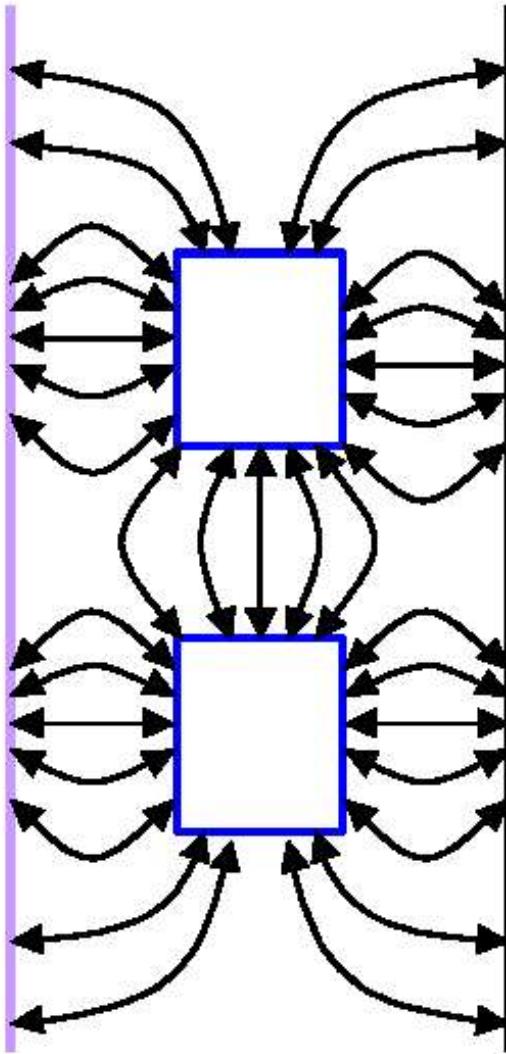


Layout Versus Schematic (LVS)

- Extracts netlist from layout by analyzing polygon overlaps
- Compares extracted netlist with original schematic netlist
- When discrepancies occur, tries to narrow down location

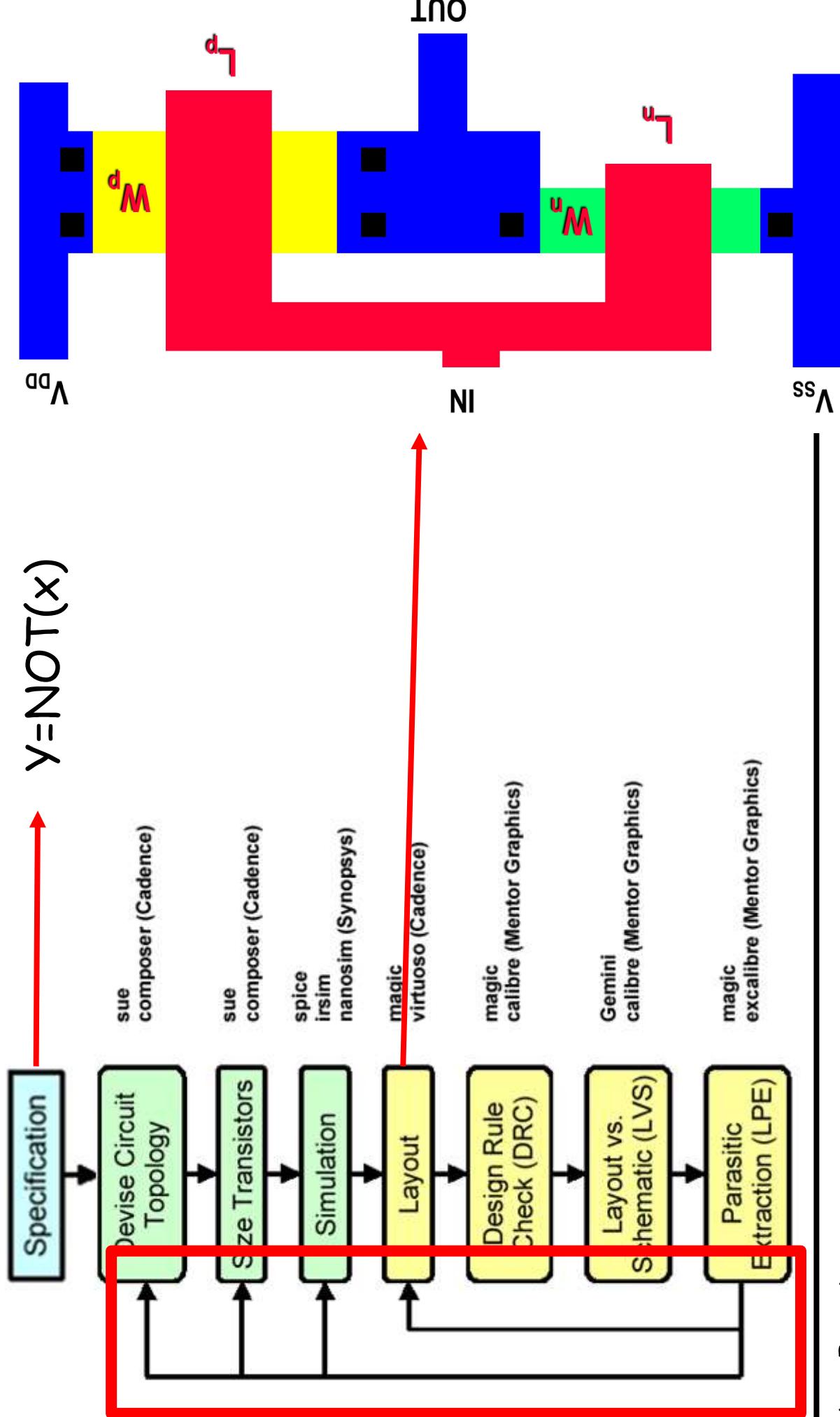


Layout Parasitic Extraction (LPE)



- Estimates capacitance between structures in the layout
- Calculates resistance of wires
- Output is either a simulation netlist or a file of interblock delays

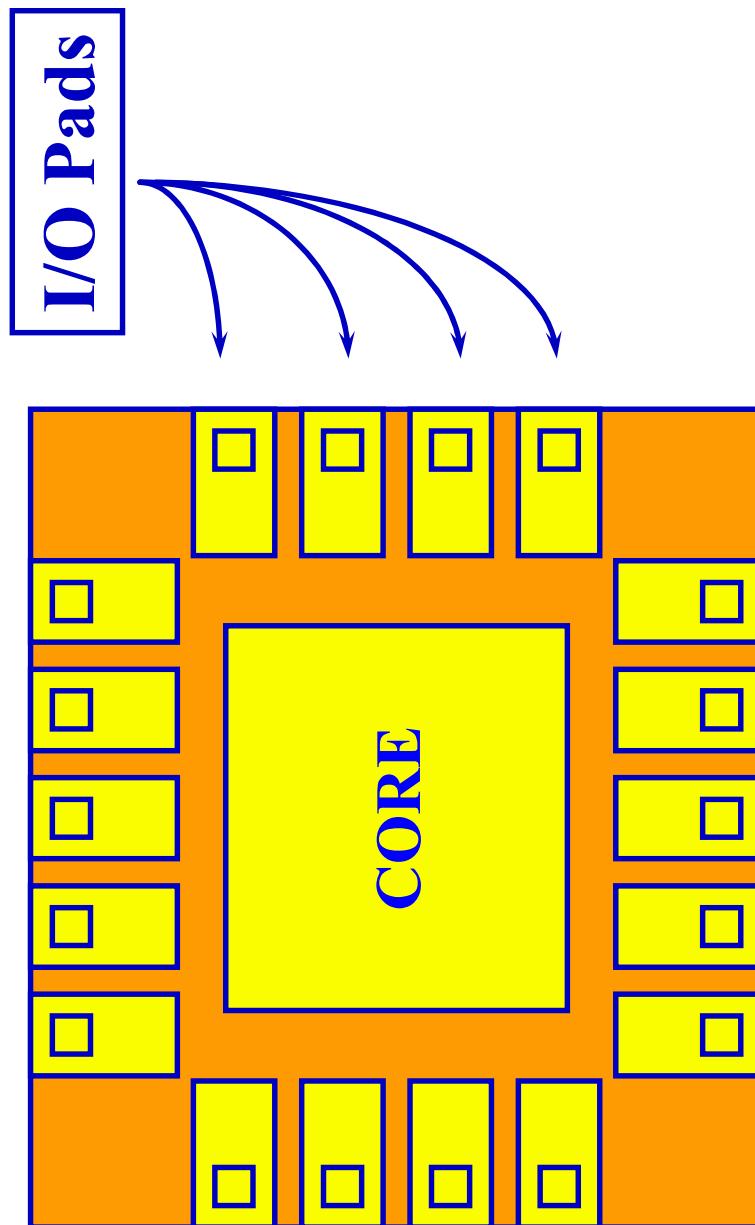
Full Custom Design Flow



ASIC semi-custom

- Designer defines interconnection among pre-designed and/or pre-manufactured logic blocks
- No global optimization
- Reduced cost and development time
- Not high skill required on technology and electronics circuits

ASIC Structure



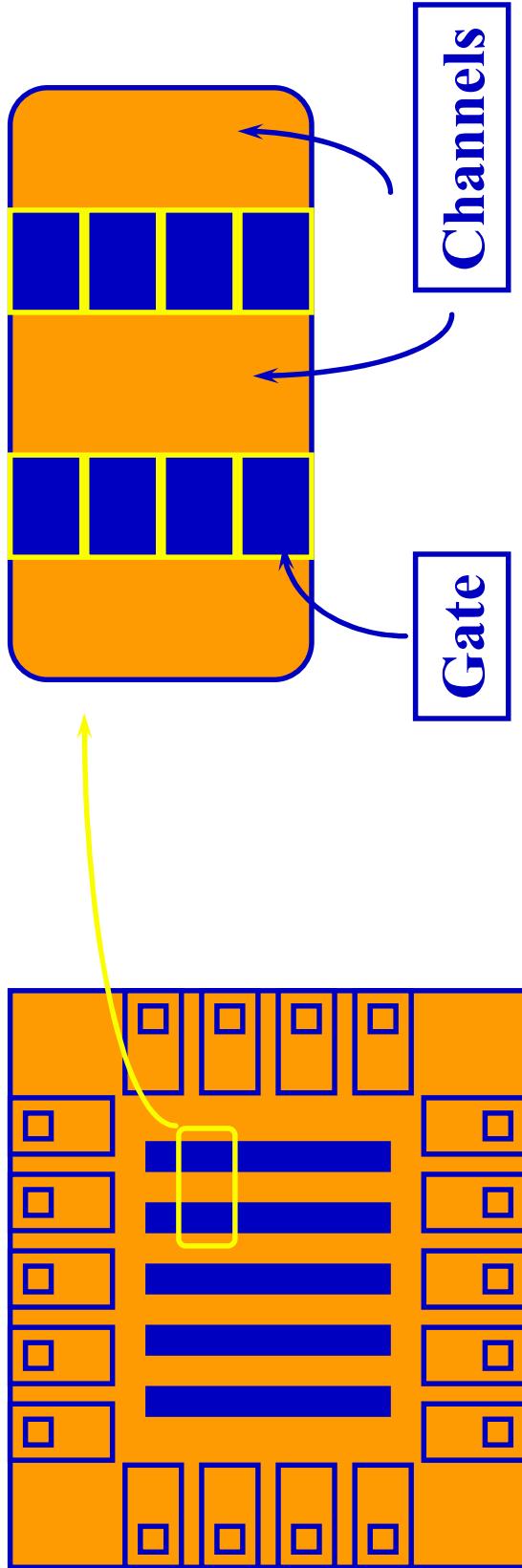
semi-custom technologies

- Gate array o channelled gate-array
- Sea of gate o channelless gate-array
- Standard cell

Gate arrays

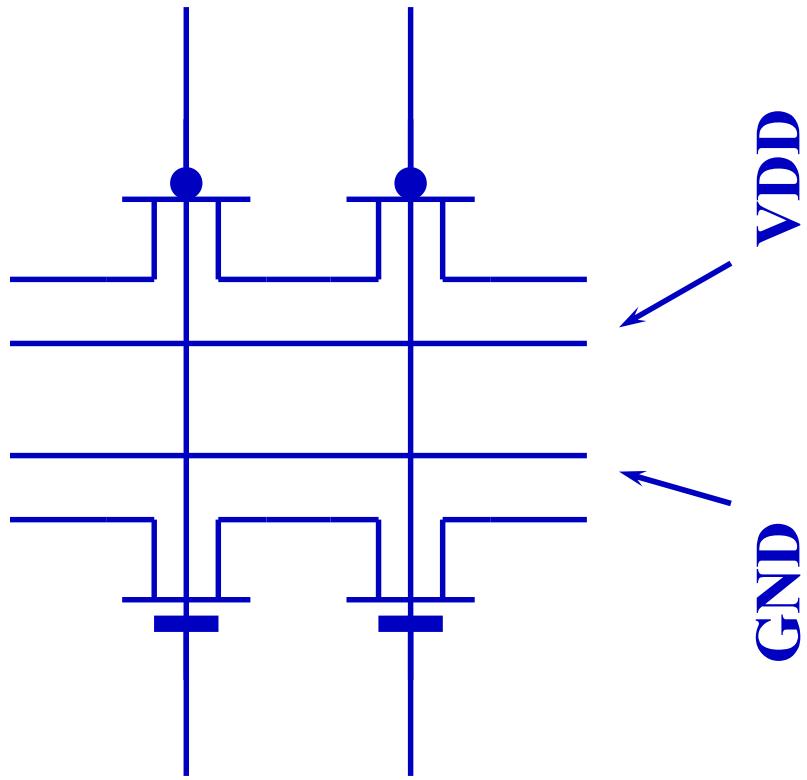
- Integrated circuits based on pre-manufactured transistors organized as a matrix
- Customization for the Specific Function is performed via metal layers (last steps of the semiconductor process)
- Size of the circuits are fixed
- I/O pads number and position is fixed
- Incomplete used of the overall transistors (<80%)

Gate array Structure

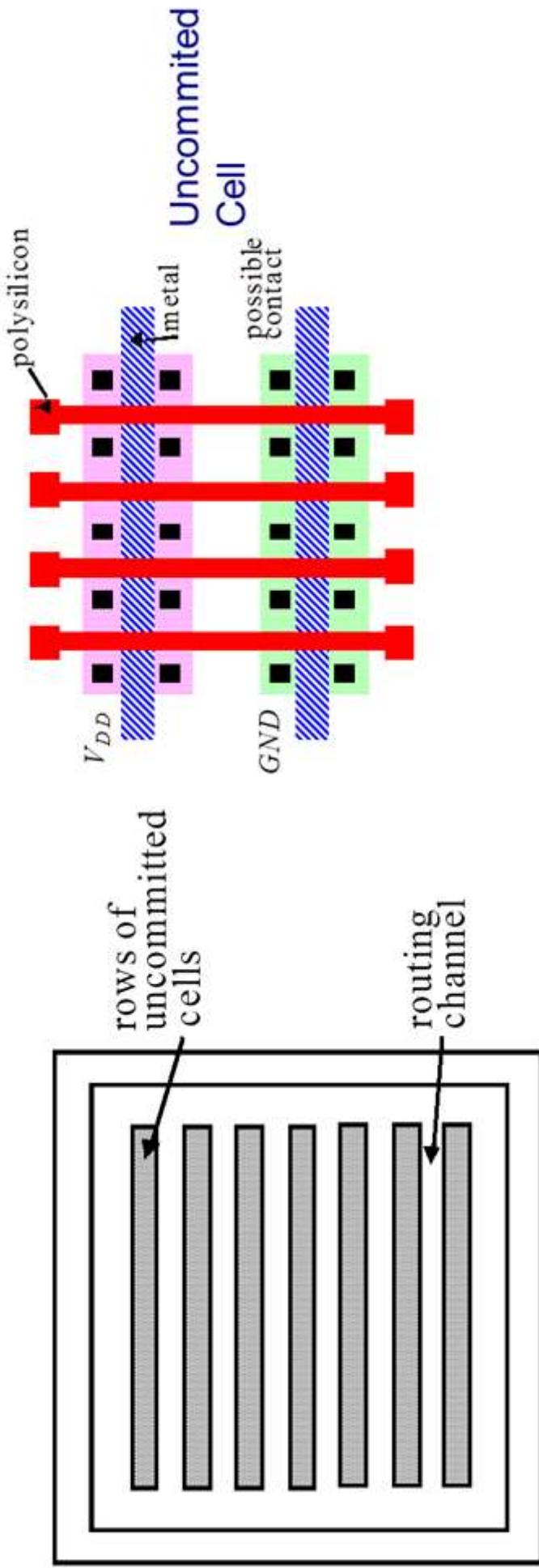


Single Gate Structure

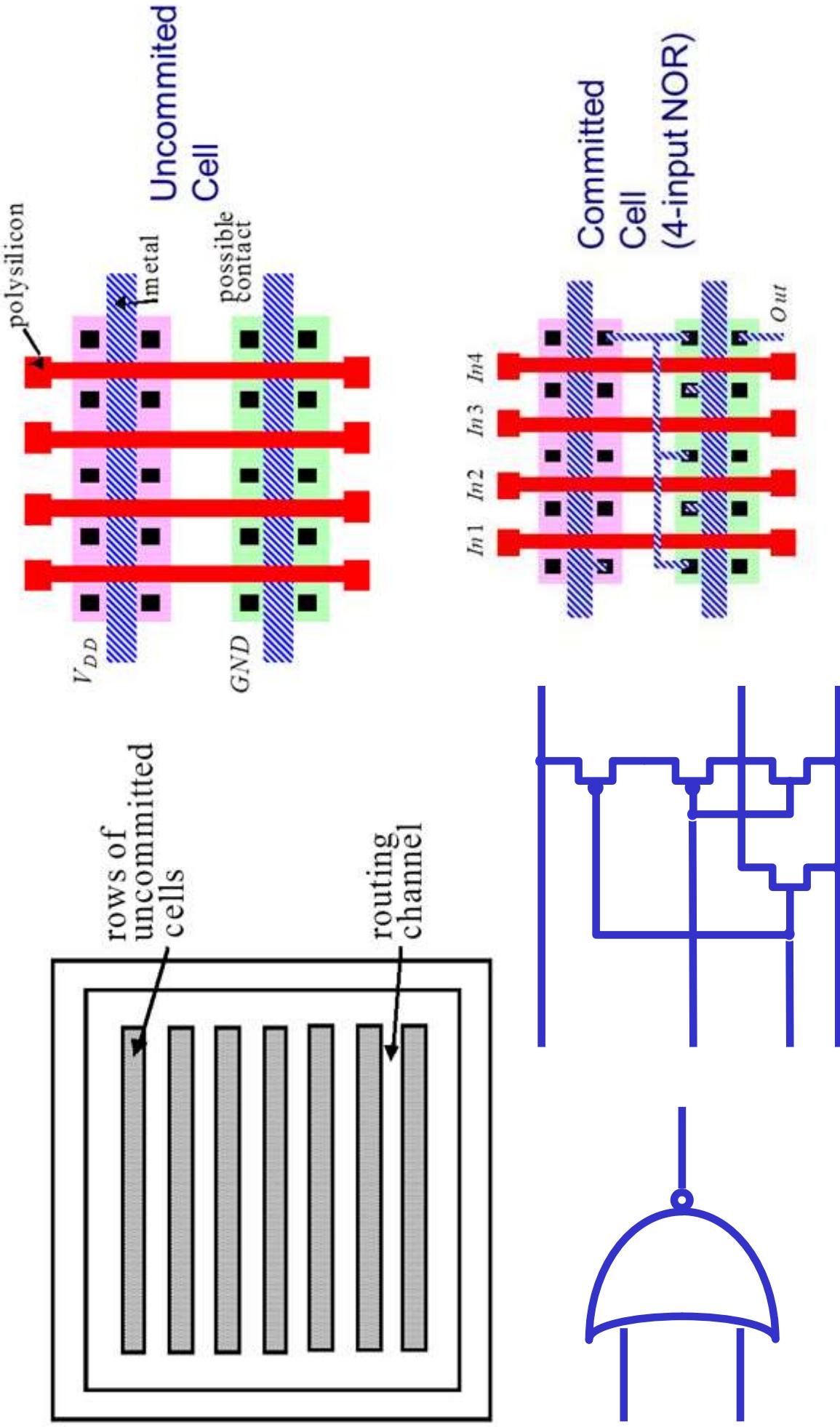
- 2 n-transistors and e 2 p-transistors per gate
- Possible interconnection from the channel to drain, source and gate terminal of the transistor



Single Gate Structure

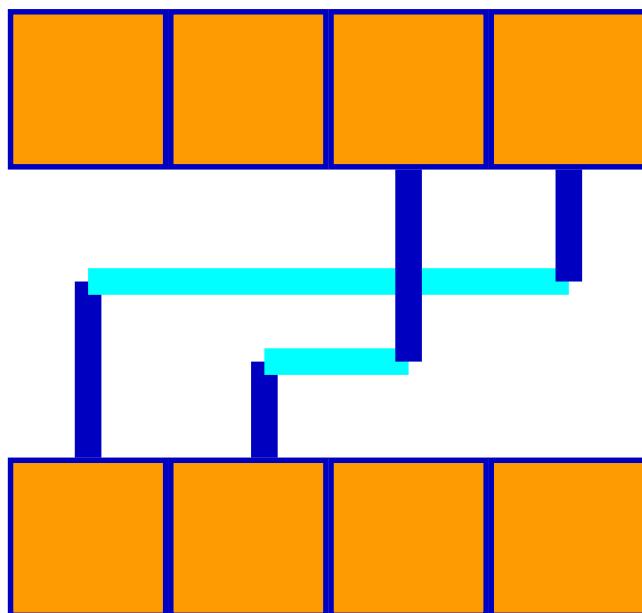


Single Gate Structure



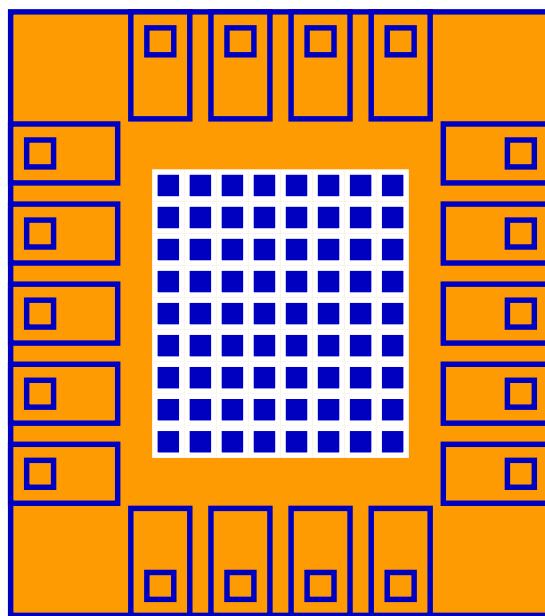
Gate-array Interconnection

- Example of a two metal layers interconnection
- Interconnection Channel (routing) of fixed size
- Sometime gate-array is not routable for channel congestion



Sea-of-gate structure

- No dedicated channels for routing
- Interconnections on top of gates, which are then not usable
- Greater flexibility



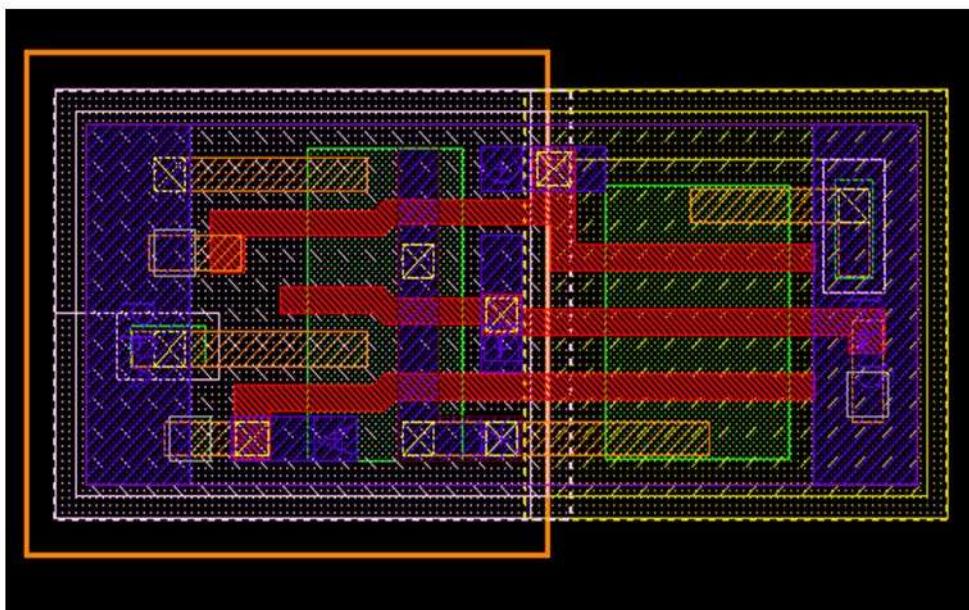
Standard cell

- Integrated Circuits manufactured *ex-novo*
- Based on standard cell, i.e. Circuit pre-designed and layout optimized with fixed height and variable width
- Organized as standard-cell rows separated by interconnection channels of variable sizes
- Possible to include macrocell such as DAC, ADC, ROM, RAM, etc.

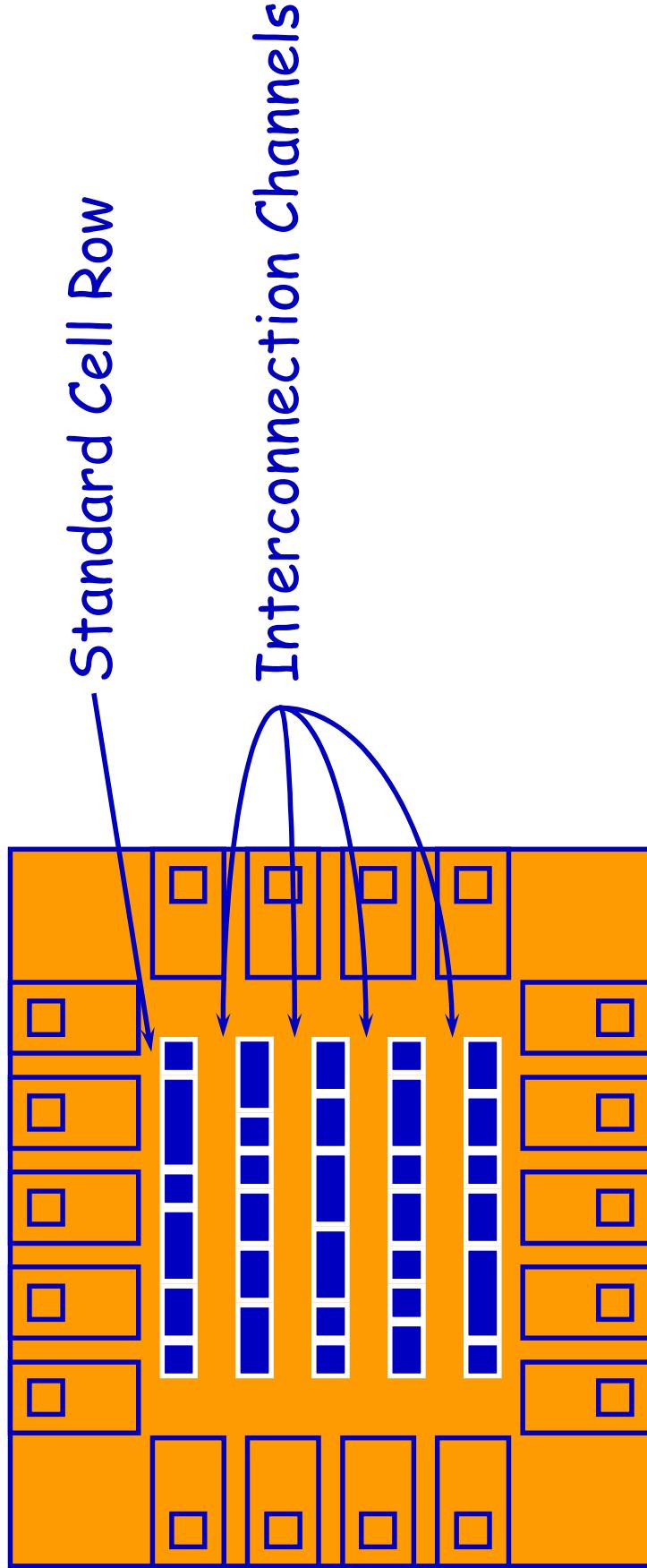
Standard cell

Path	1.2V - 125°C	1.6V - 40°C
$In1 \rightarrow t_{pLH}$	$0.073 + 7.98C + 0.317T$	$0.020 + 2.73C + 0.253T$
$In1 \rightarrow t_{pHL}$	$0.069 + 8.43C + 0.364T$	$0.018 + 2.14C + 0.292T$
$In2 \rightarrow t_{pLH}$	$0.101 + 7.97C + 0.318T$	$0.026 + 2.38C + 0.255T$
$In2 \rightarrow t_{pHL}$	$0.097 + 8.42C + 0.325T$	$0.023 + 2.14C + 0.269T$
$In3 \rightarrow t_{pLH}$	$0.120 + 8.00C + 0.318T$	$0.031 + 2.37C + 0.258T$
$In3 \rightarrow t_{pHL}$	$0.110 + 8.41C + 0.280T$	$0.027 + 2.15C + 0.223T$

3-input NAND cell
(from ST Microelectronics);
 C = Load capacitance
 T = input rise/fall time



Standard cell Structure

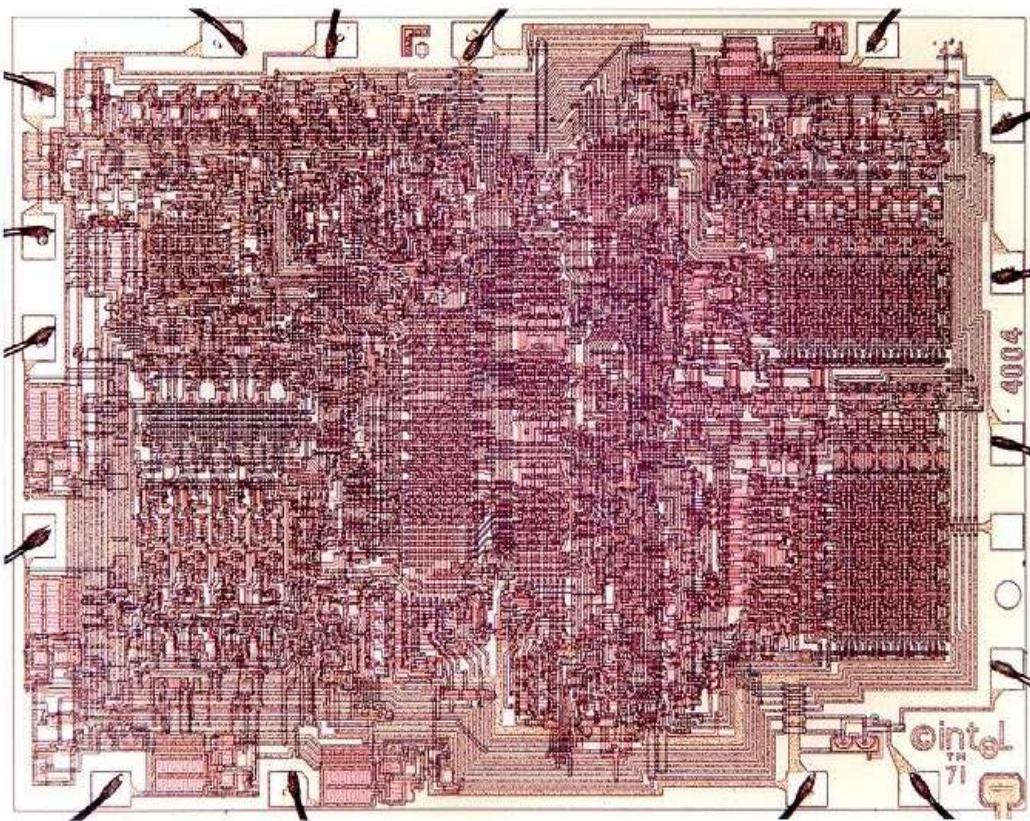


Standard cell Characteristics

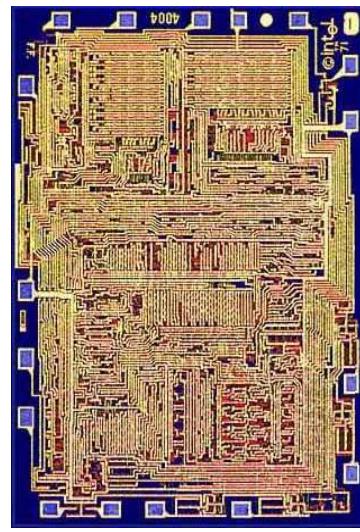
- Based on optimized cell in area and speed
- Availability of macrocells (RAM, ROM, ADC, DAC, OpAmp, etc.)
- I/O number and position decided by the designer
- Greater cost and development time w.r.t. gate array

The Custom Approach

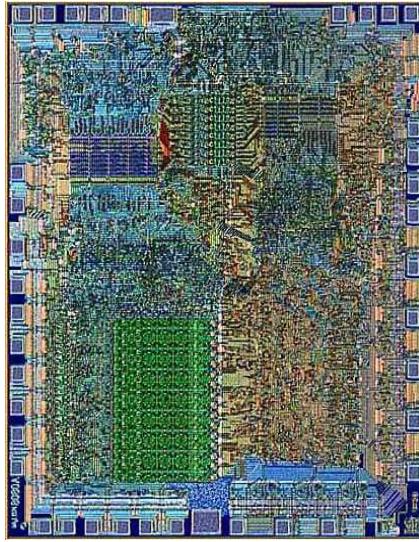
Intel 4004



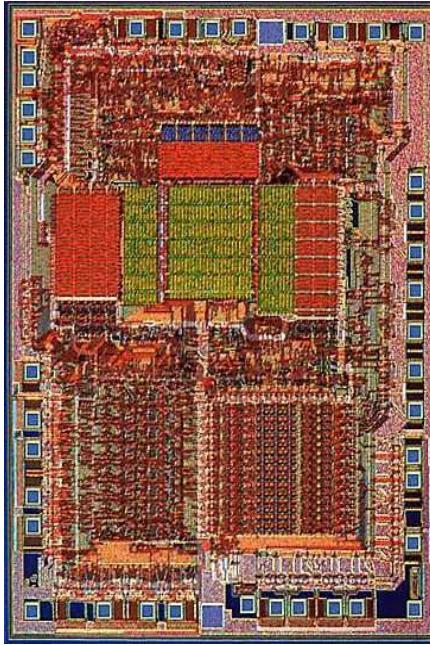
Transition to Automation and Regular Structures



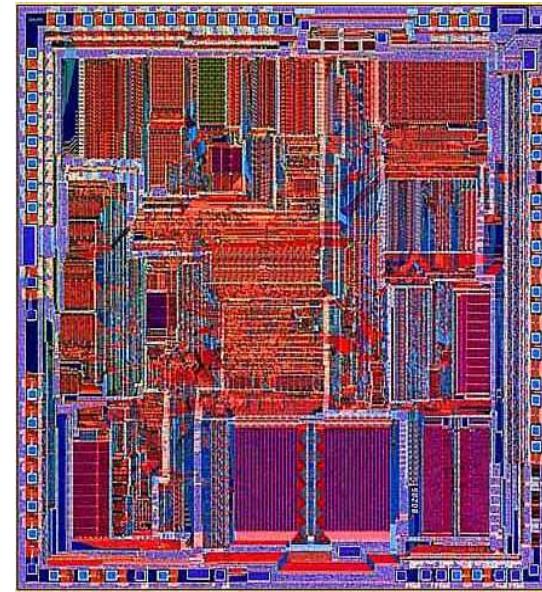
Intel 4004 ('71)



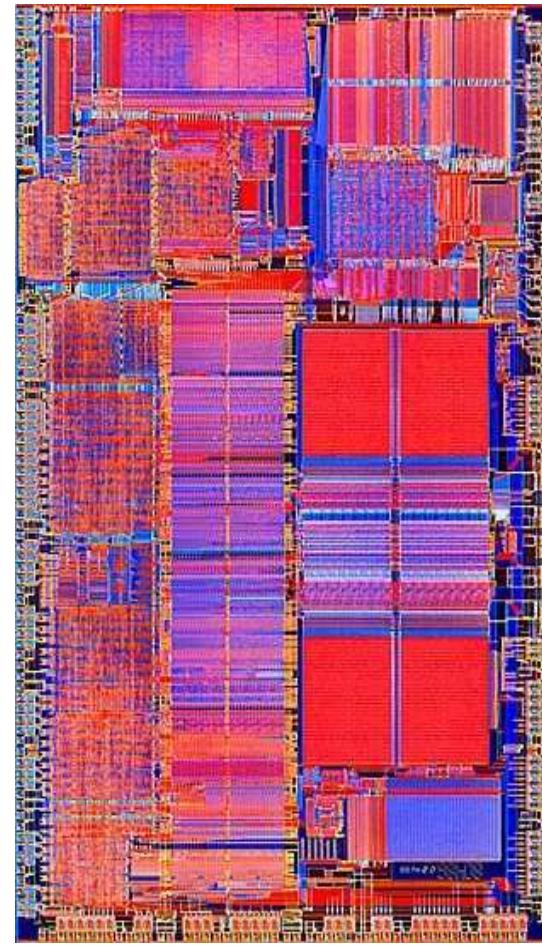
Intel 8080



Intel 8085



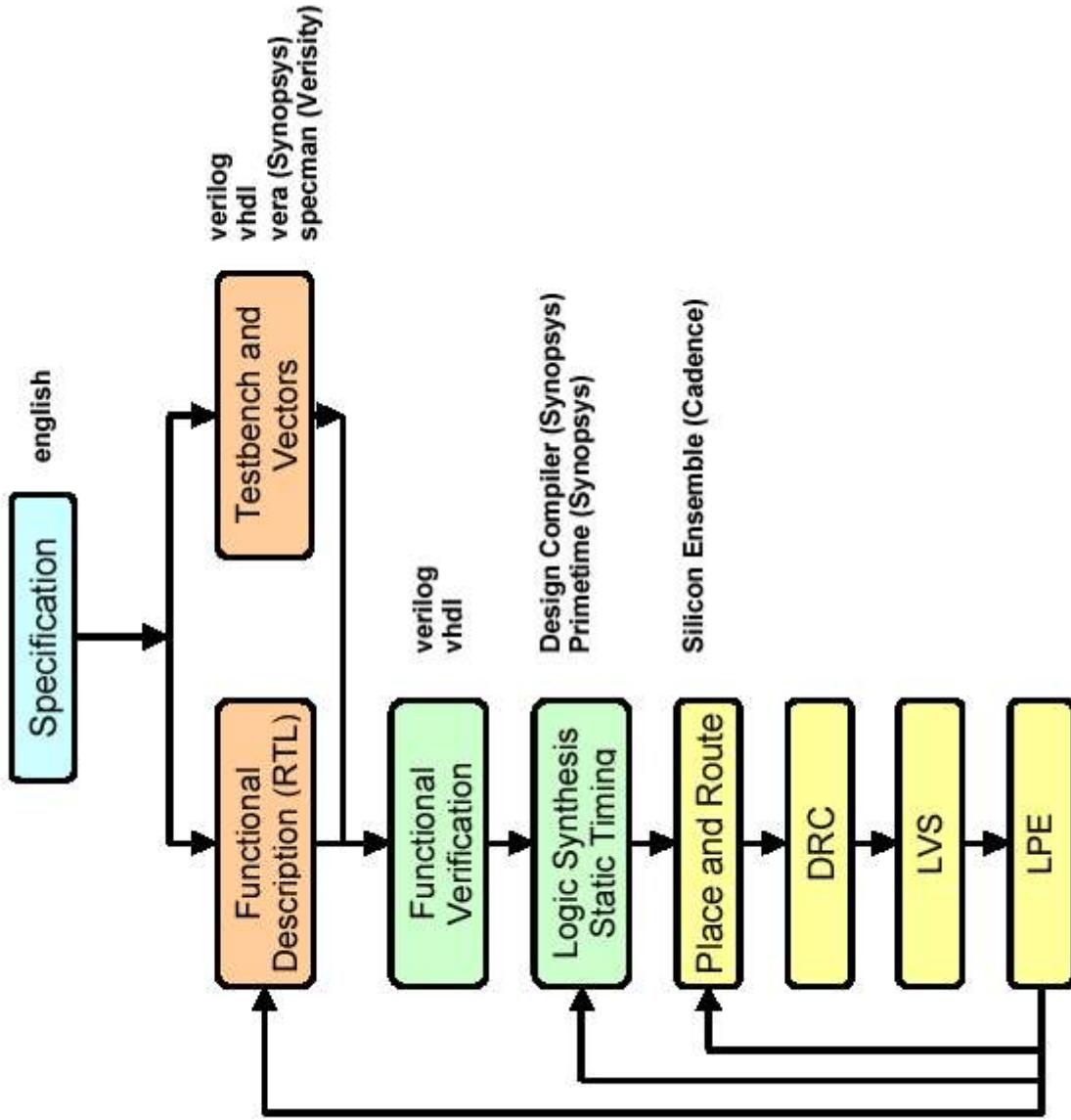
Intel 8286



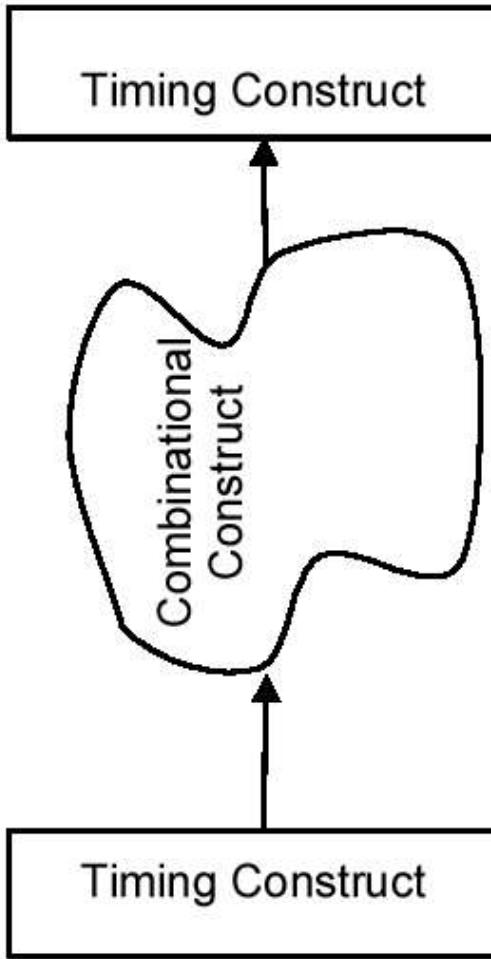
Intel 8486

"Semi-Custom" Design Flow

- Separate teams to design and verify
- Physical design is (semi-) automated
- Loops to get device operating frequency correct can be troubling



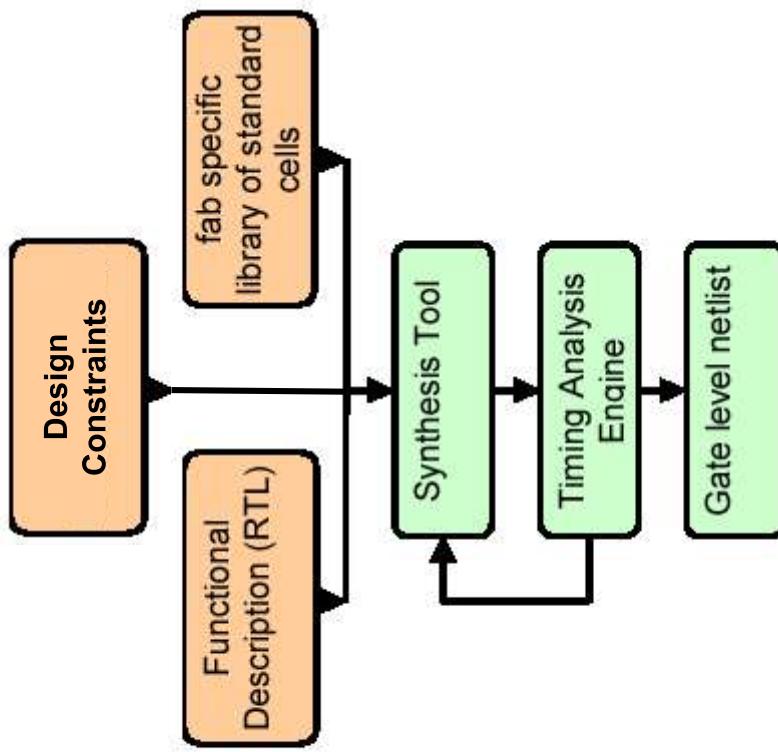
Register Transfer Level (RTL)



- Sections of combinational Constructs separated by timing statements
 - Defines behavior of part on every clock cycle boundary

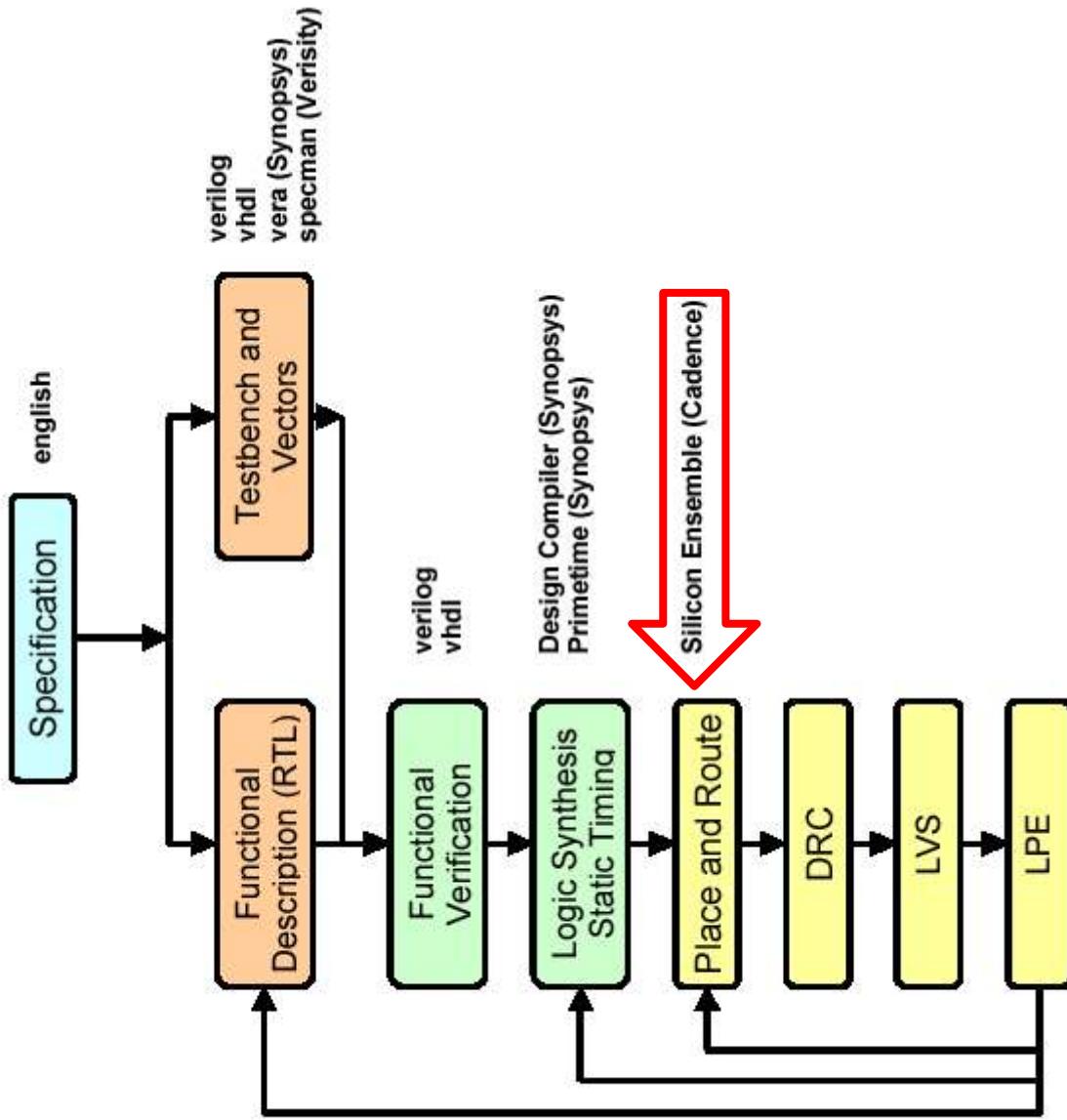
Logic Synthesis

- Changes cloud of combinational functionality into standard cells (gates) from fab-specific library
- Chooses standard cell flip-flop/latches for timing statements
- Attempts to minimize delay and area of resulting logic



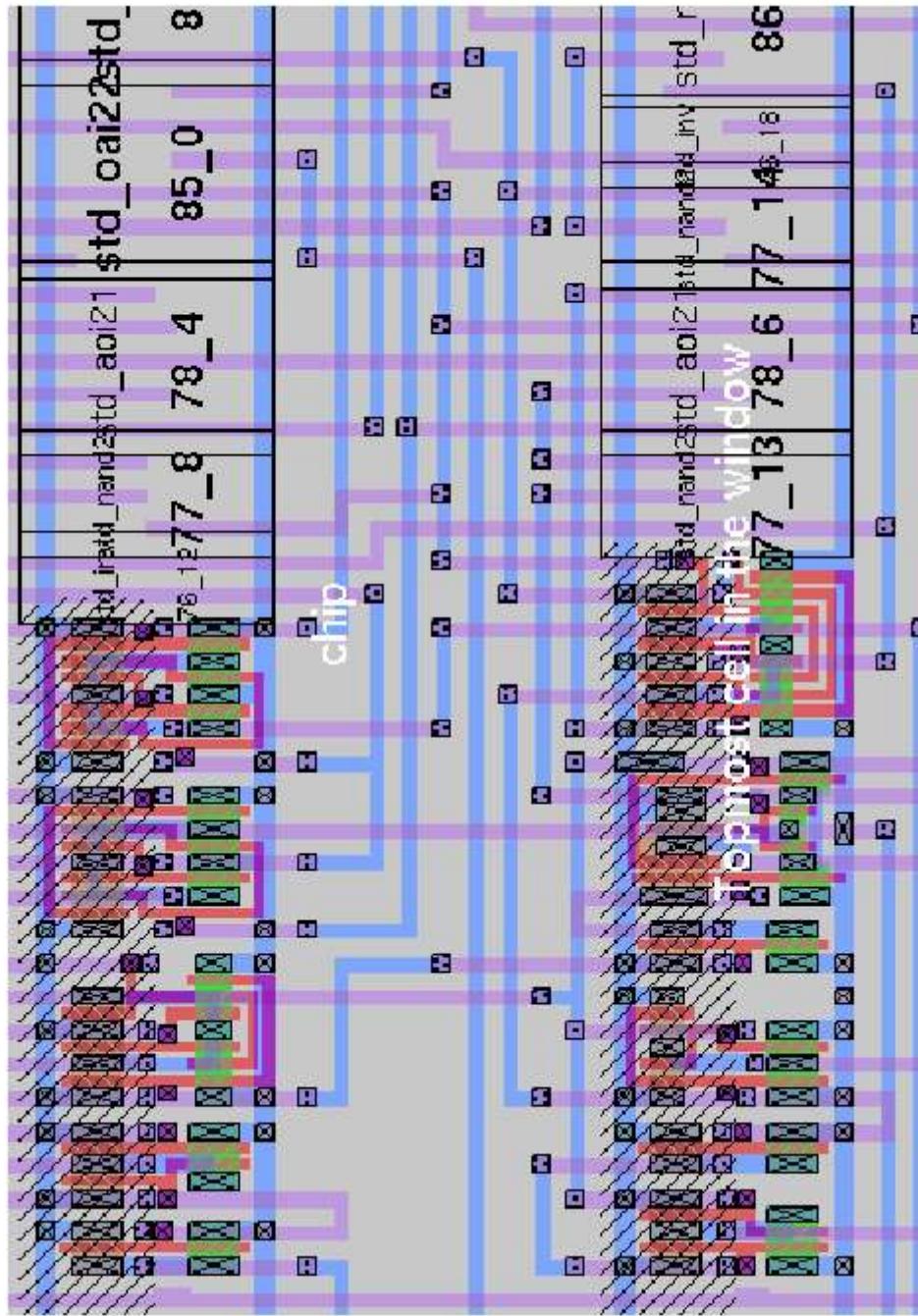
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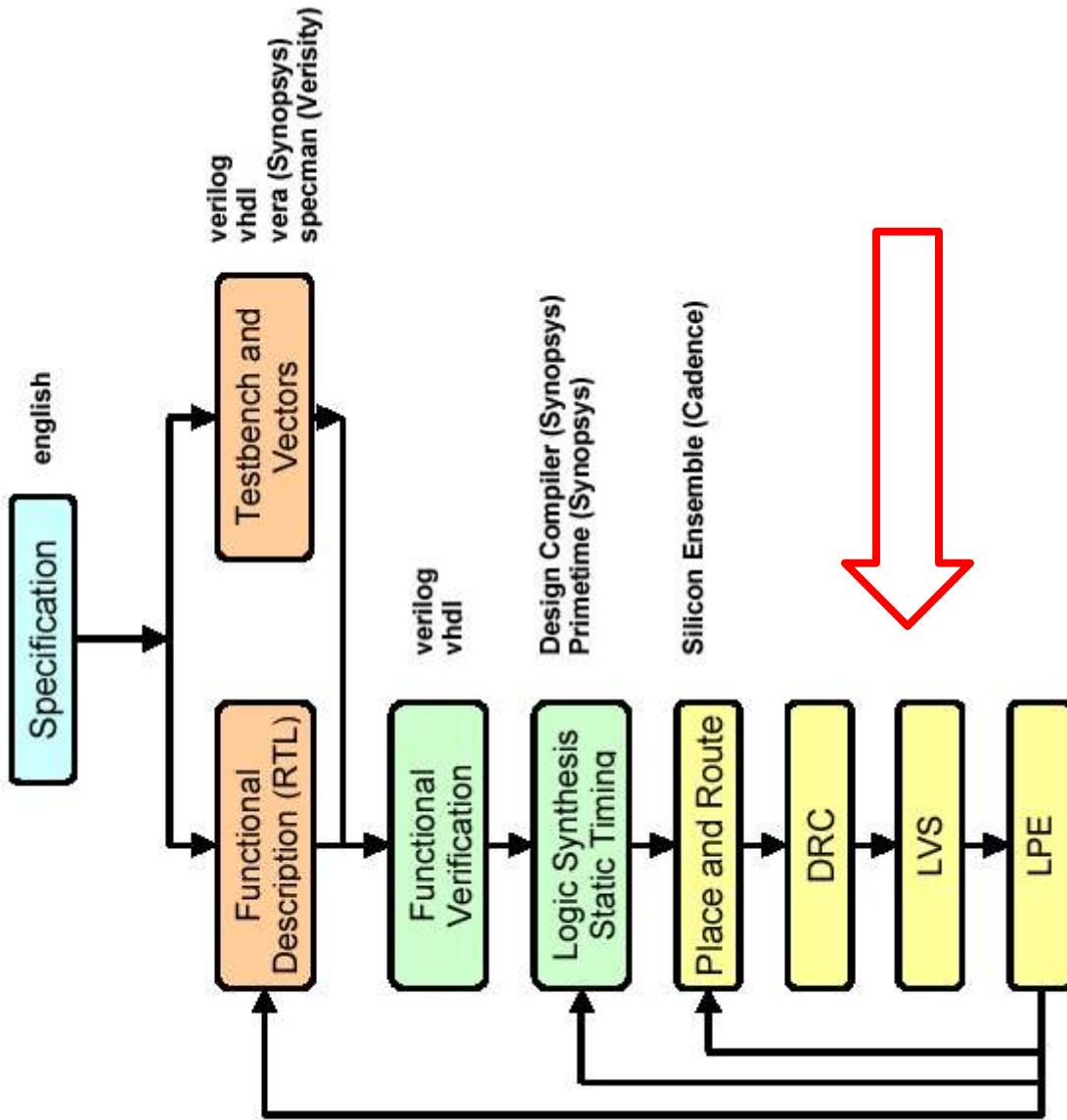
Standard Cell Placement and Routing

- Place layout for each gate (“cell”) in design into block
- Rearrange cell layouts to minimize routing
- Connect up cells



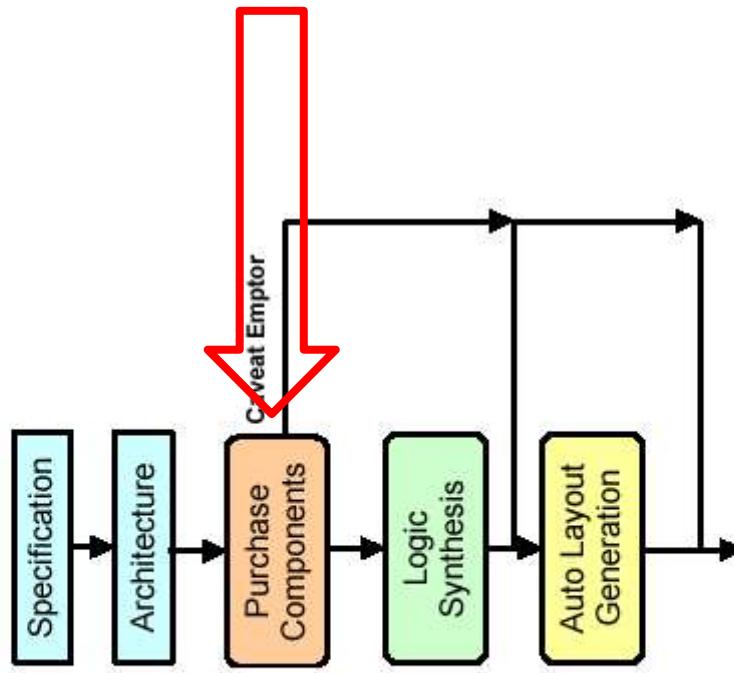
"Semi-Custom" Design Flow

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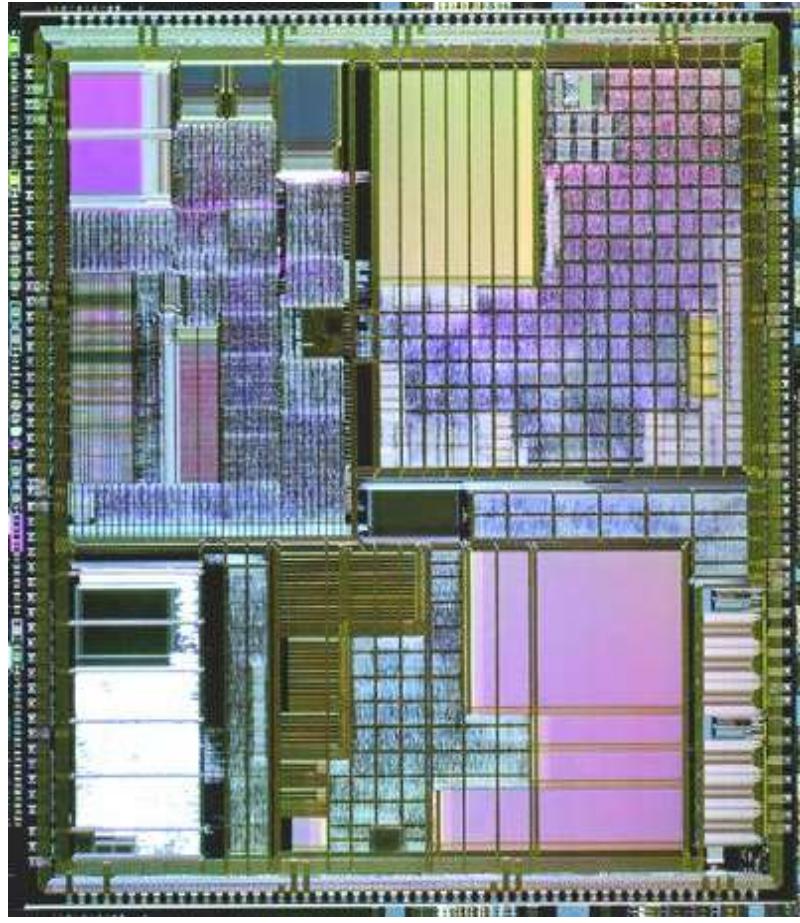
System On Chip Design Flow

- Can Buy “Intellectual Property” (IP) from various vendors
- “Soft IP”: RTL or gate level description
 - Synthesize and Place and Route for your process.
 - Examples: Ethernet MAC, USB
 - “Hard IP”: Polygon level description
 - Just hook it up
 - Examples: micro/DSP cores embedded DRAM
- Also: Standard cell libraries for ASIC flow



Chip Assembly System

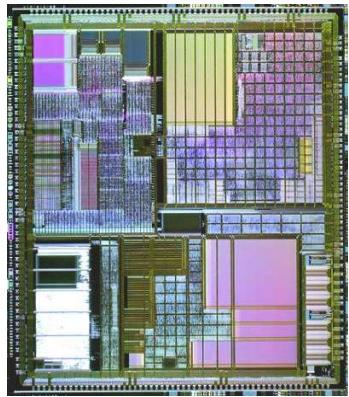
- Integrate blocks from previous steps into final layout
- Early Floorplanning is key



Tapeout

- Used to write 9-track computer tapes for mask making
 - Now, Transfer polygons to fabrication company via ftp
 - You're done! (Except for documentation, test vector generation, device bringup, skew lots, reliability tests, burnin...)

Foundry

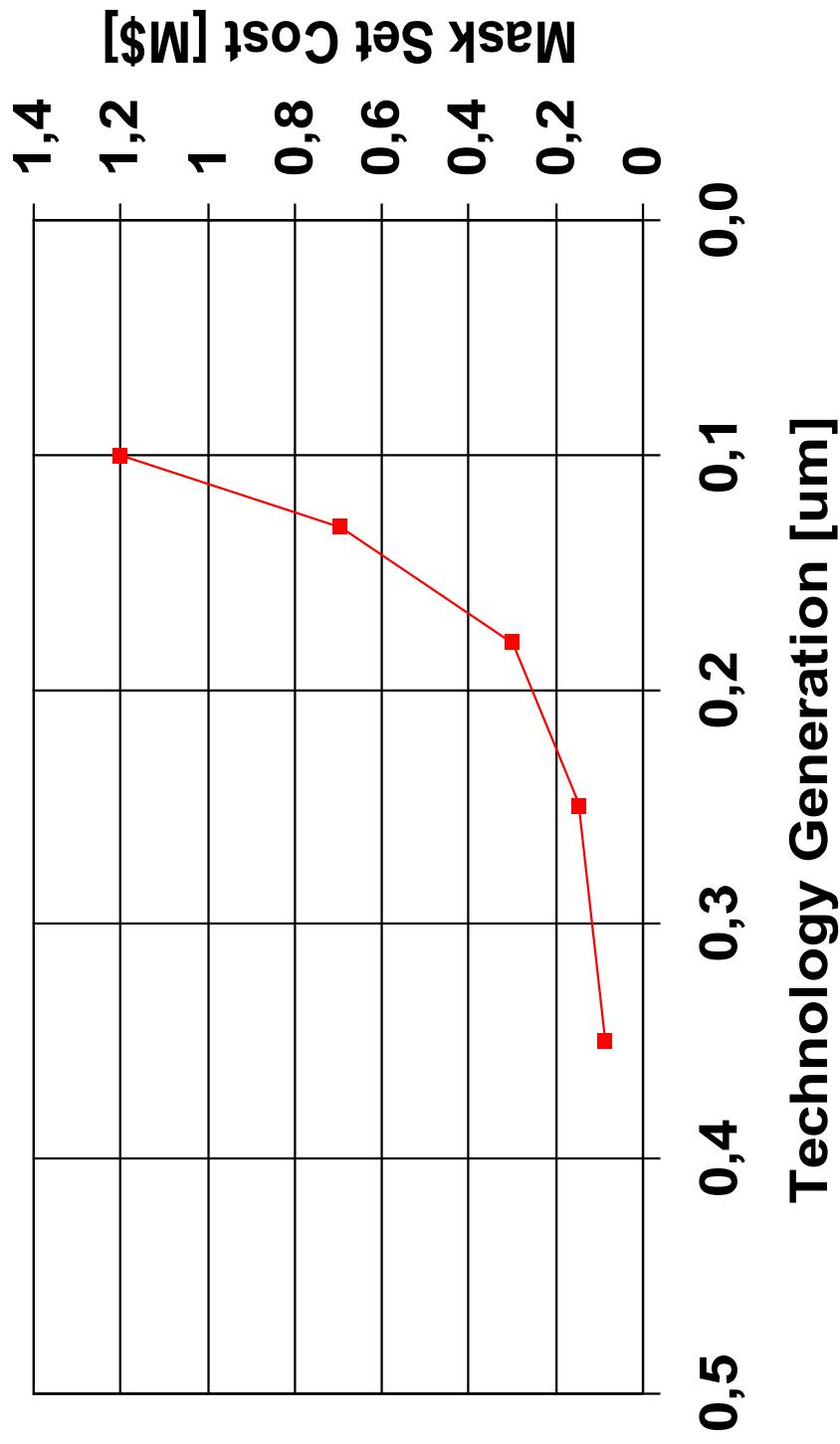


AMS 200 mm Production Line - (0,35 up to 0,18 μm)

Production Capacity: 3.000 Wafer Starts Per Week

Clean room Area: 2.600 m^2

Mask Costs



Foundry Costs: Example (2001)

AMS 200 mm Production Line - (0,35 up to 0,18 μ m)

305,2 Millioni di Euro

(building. equipment and support)

....the equivalent cost of a long queue of Ferrari 575 Maranello....



Cost: 176.783 Euro

Sizes: 455/194/128 cm

$305.200.000 / 176.783 = 1726$ auto
 $1726 \times 455 \text{ cm} = \text{nearly } 8 \text{ Km!}$

Testing the manufactured ASIC



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ASIC solution costs

- Major drawback is the **overall cost** for development and manufacturing
- Requires significant investment and risks
- High barrier especially for small-medium enterprise in the use of ASIC technology
- Requires a detailed cost estimation

Costs

- Fixed cost for investment, design and manufacturing
- Recurrent cost for each product unit

Number of product units

$$\text{Total Cost} = \text{Fixed Cost} + n \times \text{Recurrent Cost}$$

NRE Costs

- Fixed cost or NRE (non-recurrent engineering)
 - Design Costs
 - » Designer man months
 - » CAD tool machine time
 - » hardware and software amortization
 - » ...
 - Manufacturing and Testing Fixed Costs
 - » Masks for the semiconductor process
 - » Board and tool for ASIC testing

RE Costs

- Cost repeated for each unit or RE (*recurrent engineering*)
 - Manufacturing Process Cost
 - » Manufacturing cost for the single component
 - » Proportional to the circuit area (wafer cost divided by number of dies per wafers)
 - » package
 - Testing costs
 - » Tester Machine usage time for the single circuit

Unit Cost: C_1

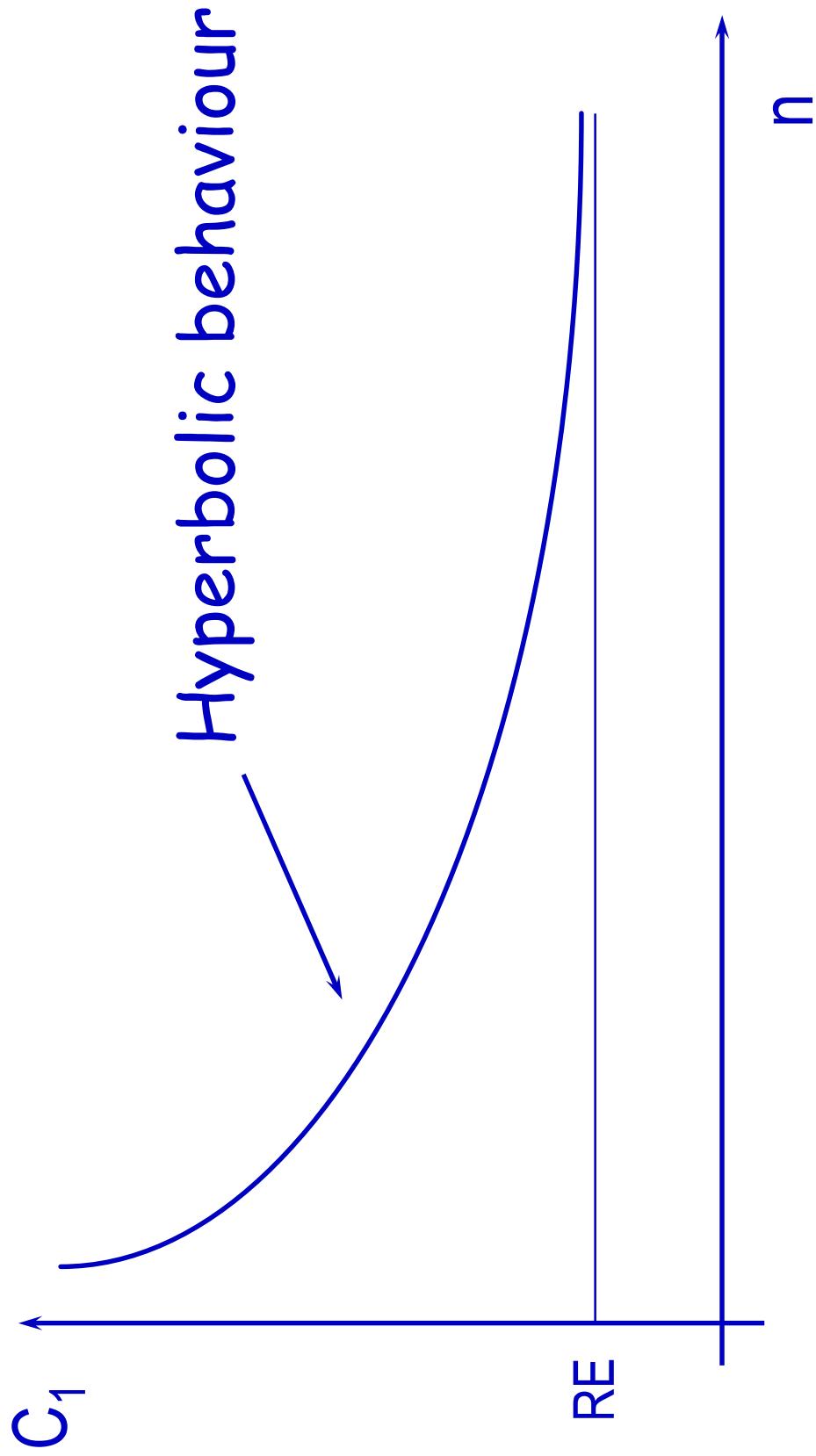
Total Cost = Fixed Cost + $n \times$ Recurrent Cost

$$C_T = NRE + n \times RE$$

Dividing by n we have the final cost for single unit

$$C_1 = NRE / n + RE$$

Cost Curve



Example

- Value for n in order to have an unit cost of 2,00 € in case $NRE=200 \text{ k€}$ and $RE=0,75 \text{ €}$?
 - $C_1 = NRE / n + RE \rightarrow C_1 - RE = NRE / n$
 - $n = NRE / (C_1 - RE) = 200 \cdot 10^3 / (2,00 - 0,75) = 160 \text{ K}$

Comparison of NRE Costs

- **Design Time**
 - full-custom involves the greatest design time
 - Different semi-custom have similar design time
- **Fixed Manufacturing costs**
 - full-custom and standard-cell are similar, since both are manufactured from scratch (**ex-novo**)
 - gate-array is smaller (most masks are shared among many users, only metal layers are application specific)

Comparison of NRE Costs

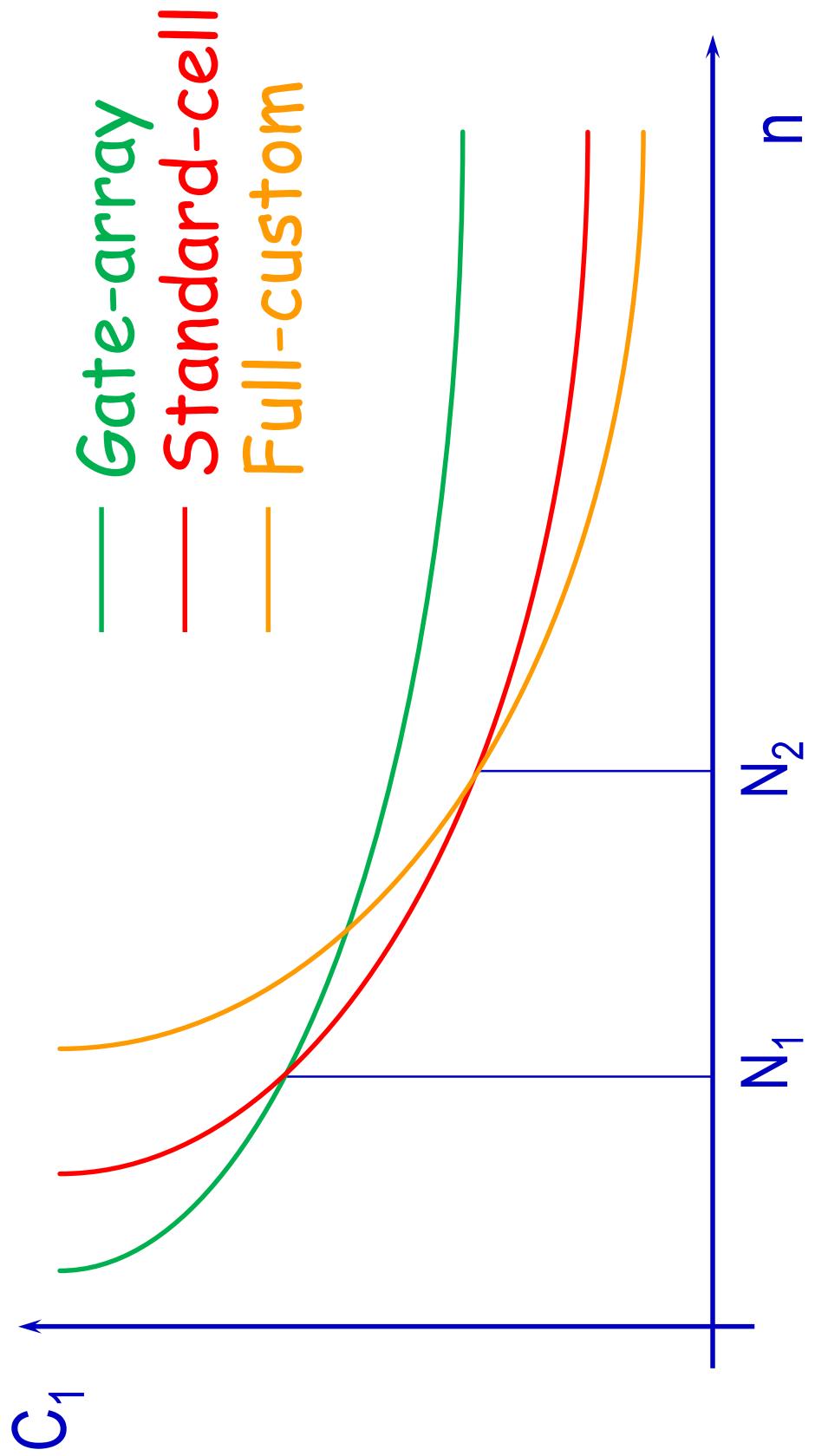
AREA

- Manufacturing costs is proportional to area

- **Full-custom:** optimized area
- **Standard-cell:** greater than full-custom but still with maximum freedom in the interconnection and complete used of all implemented resources
- **Gate array:** fixed sizes with partial use of implemented resources, greater are than the other approaches



Cost curves



Notes (1/2)

- Three zones for three most convenient solution
 - $n < N_1$
gate-array
 - $N_1 < n < N_2$
standard-cell
 - $n > N_2$
full-custom

Notes (2/2)

- Unit cost is not all. Other metrics could be important such as speed performance, size, power consumption, etc.
- For application with low or medium volume it is important to keep NRE costs to a minimum
- Time-to-market: full-custom and standard-cell technologies have a great impact on time-to-market

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FPGA technologies

- Characteristics of Field Programmable Gate-Array (FPGA)
 - Comparison with full-custom and semi-custom ASIC
- FPGA Architectures available on the market
 - Logic Cell Array
 - Gate Array

FPGA

- **Field Programmable Gate Array (FPGA)**
 - Internal logic is programmable
 - Interconnections are programmable
- **FPGA Architecture**
 - *Gate-array type*
 - *Logic Cell Array type*

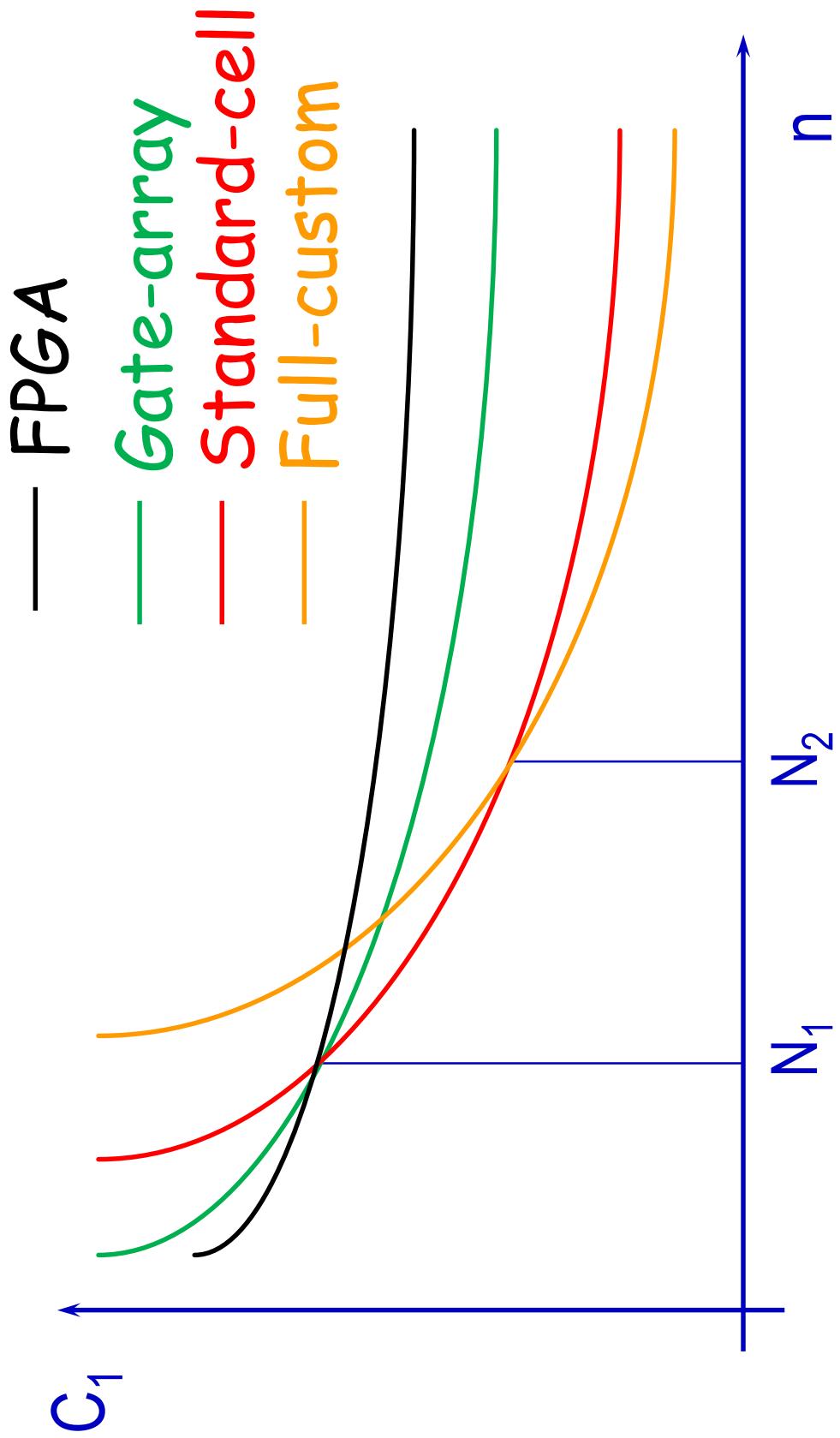
FPGA pro

- Programmable
 - Design Flexibility
 - Design updatable
- Zero turn-around time
- NRE costs smaller than ASIC

FPGA contra

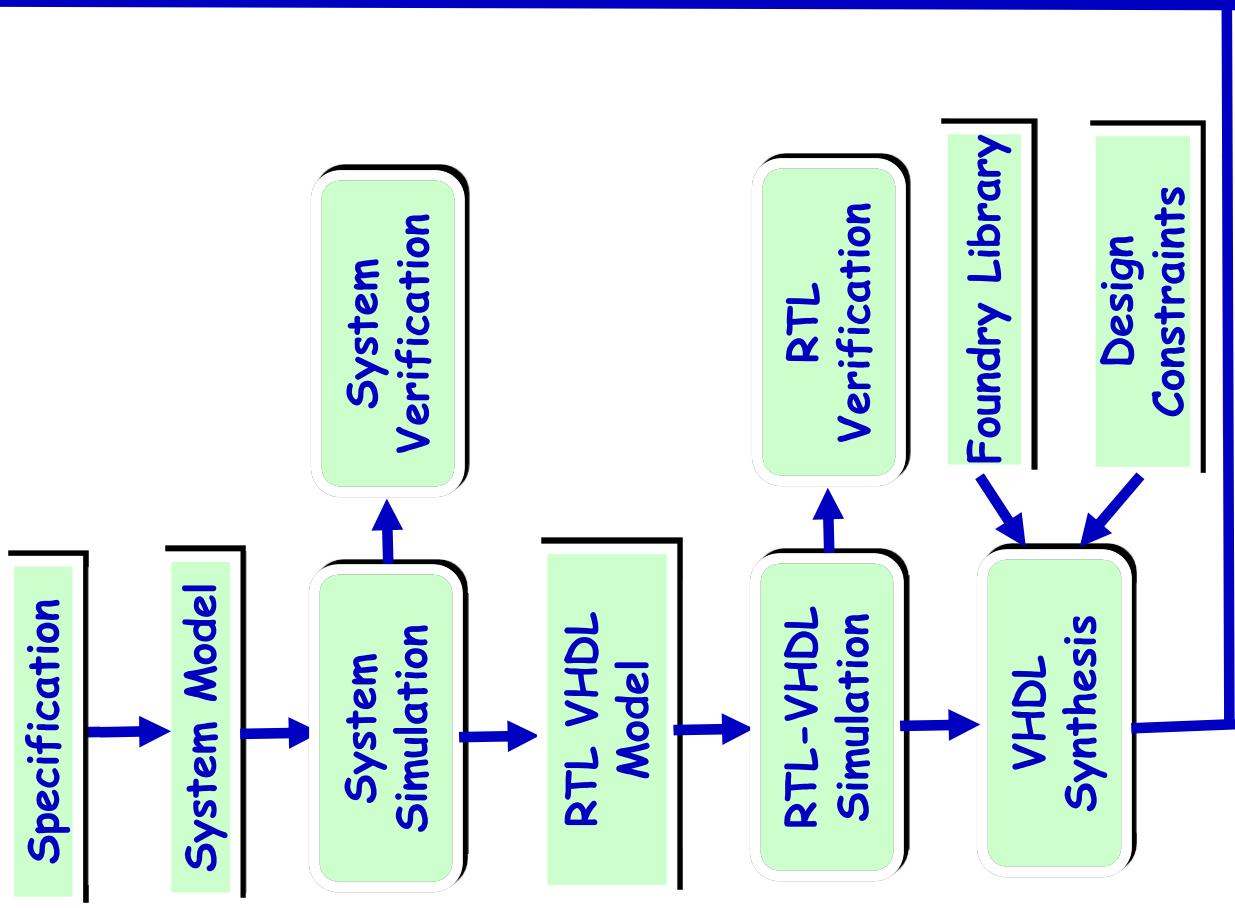
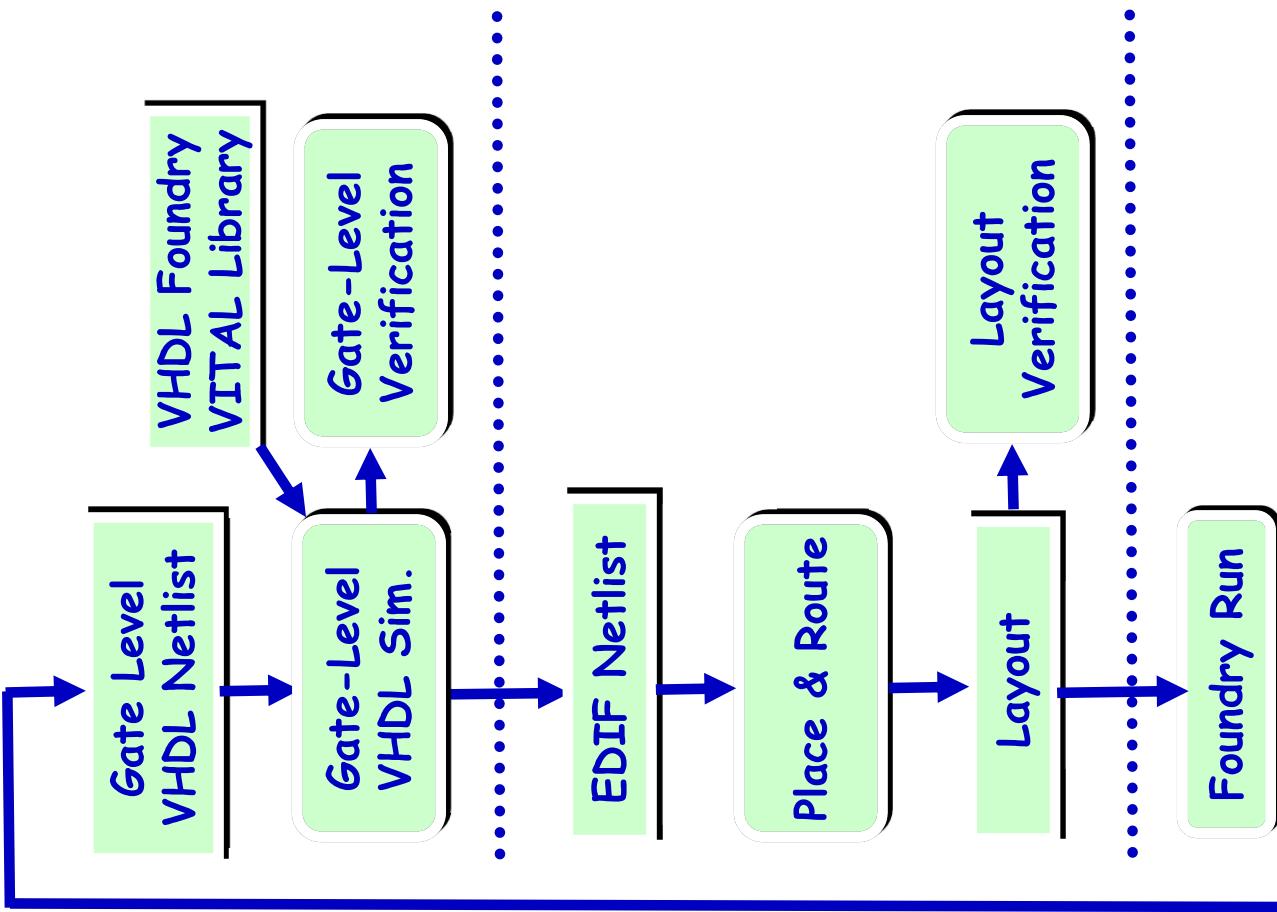
- No optimized Device
 - Manufactured in fixed size (area are not fully used)
 - No optimized performance (collegamenti e logica interna ridondanti)
- RE costs greater than ASIC
 - No convenient for huge volume

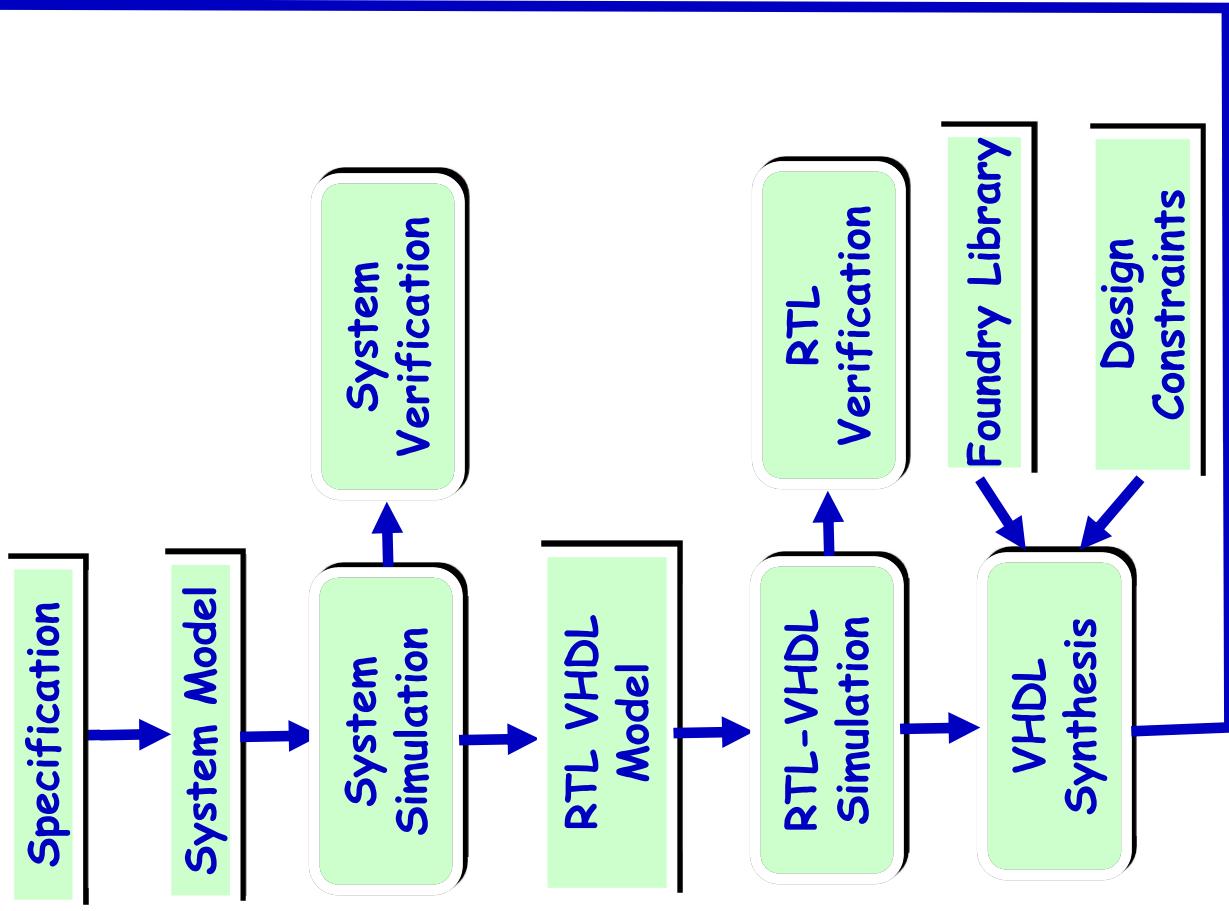
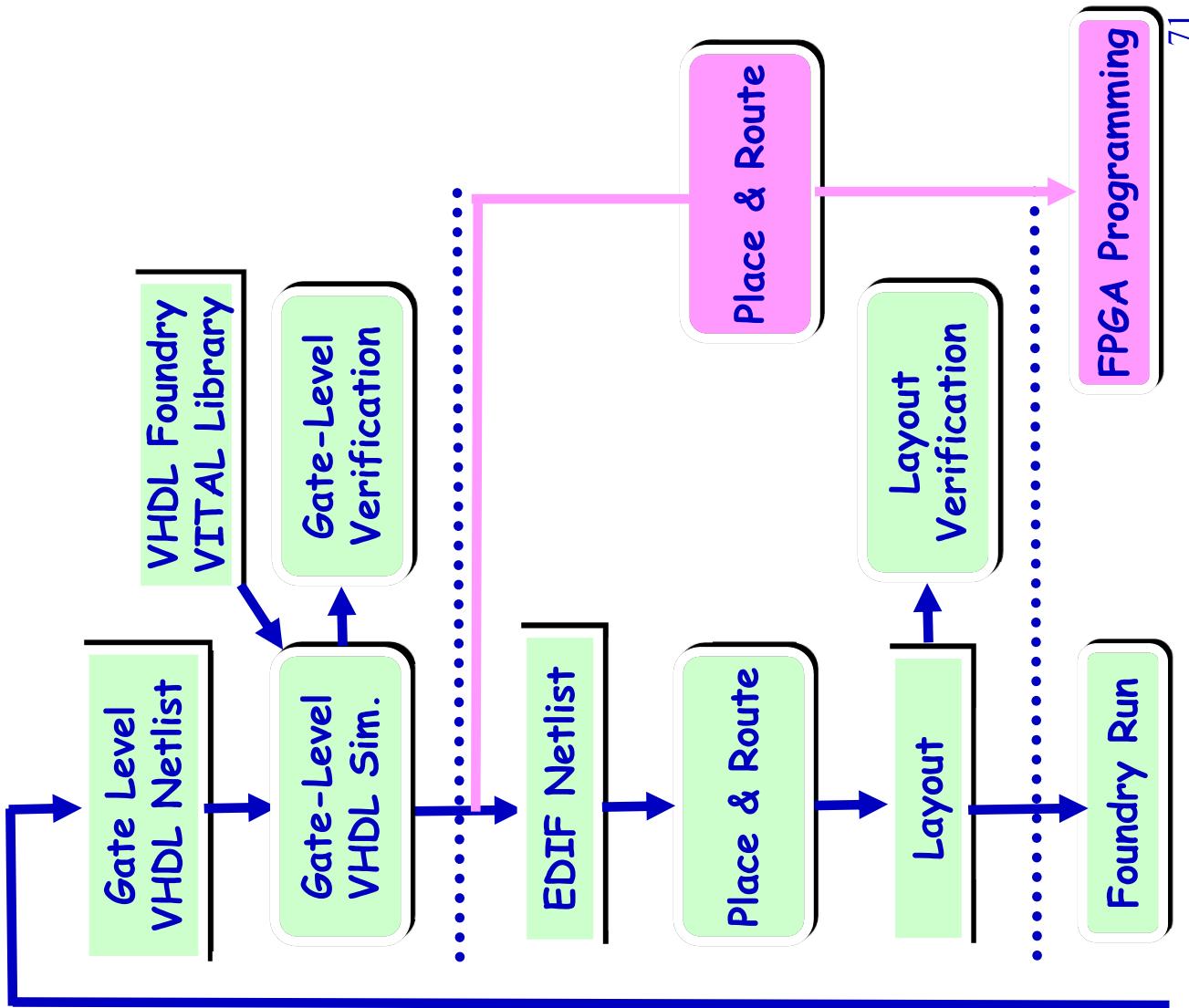
Comparison with ASIC



When **FPGA** are **advisable**

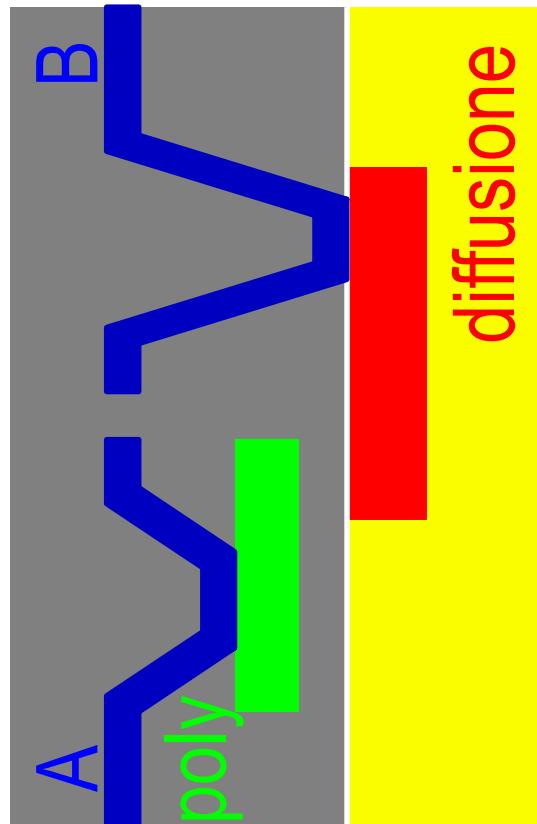
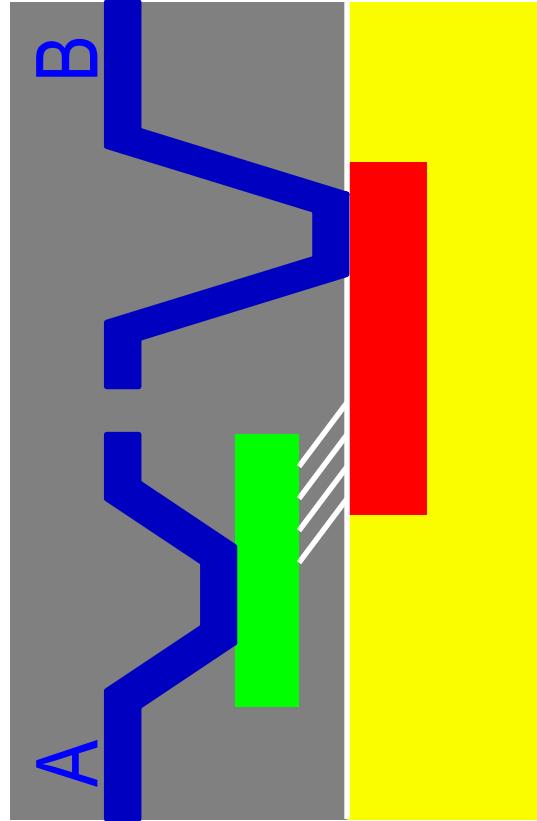
- Insufficient budget to cover ASIC NRE costs
- Small and Medium production volume
- System spec not completely frozen
- Prototyping
 - FPGA prototype for proof-of-concept
 - Easy and fast modification
 - Technology re-targeting to ASIC technology for volume production





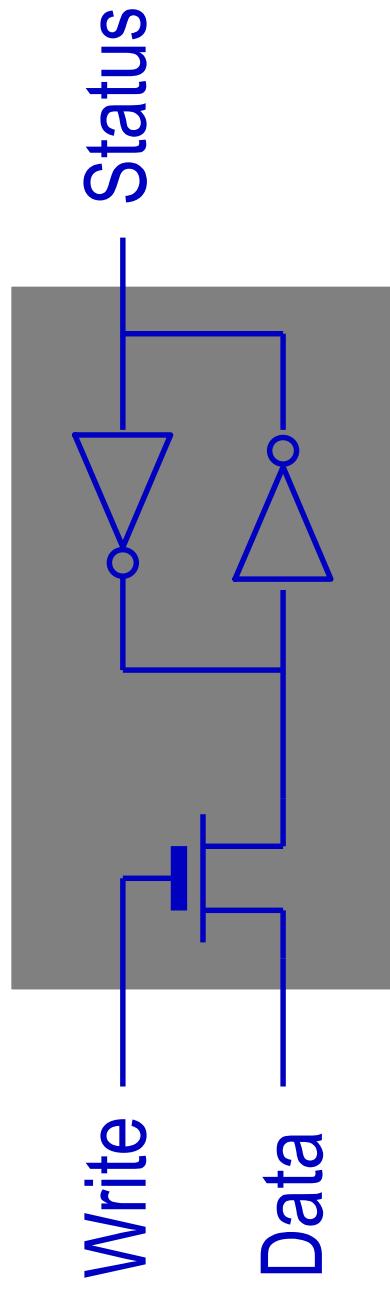
Programming Method: Anti-Fuse

- **Anti-fuse programming**
 - Two nodes are electrically isolated
 - When programmed two nodes are closed



Programming Method: SRAM based

- Programming with SRAM memory cell
 - Status of programmable unit depend on the data stored in the memory cell



FPGA SRAM-based

- Volatile Static Memory
 - ⌚ Configuration Load at power-on
 - ⌚ Sensibility on external noise (soft errors)
 - ⌚ Re-programmable
 - Easy and fast modification to the design
 - ⌚ Run time Re-programmability
 - Part of the FPGA can be re-programmed on the fly

FPGA Architectures

- Matrix of Logic Cell with different complexity/granularity
 - Row of logic cells
 - » ACTEL (www.actel.com) → www.microsemi.com (a microchip company)
 - Matrix of logic cells
 - » XILINX (www.xilinx.com)

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» Handbooks						
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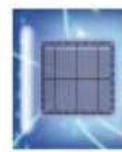
Xilinx offers the broadest lineup of FPGA, CPLD and EPP solutions that set the industry standard for the lowest cost, highest performance, and lowest power.

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Boards & Kits

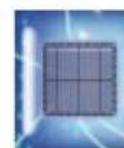
Xilinx development kits provide out-of-the box design solutions that help you cut your development time by up to 50%.



Design Tools

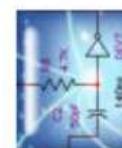
The ISE Design Suite unlocks the full potential of Xilinx Targeted Design Platforms with configurations for logic, embedded, and DSP designs – all available with tightly integrated design flows.

[Show Design Tools](#)



Intellectual Property

Xilinx Intellectual Property (IP) are key building blocks of Xilinx Targeted Design Platforms. An extensive catalog of base-level cores is available to address the general needs of FPGA designers, as well as robust domain- and market-specific cores to address requirements found in DSP, Embedded, and Connectivity



Technology

Xilinx offers the most complete suite of technology solutions available in the industry including Embedded Processing, DSP, Connectivity and more.

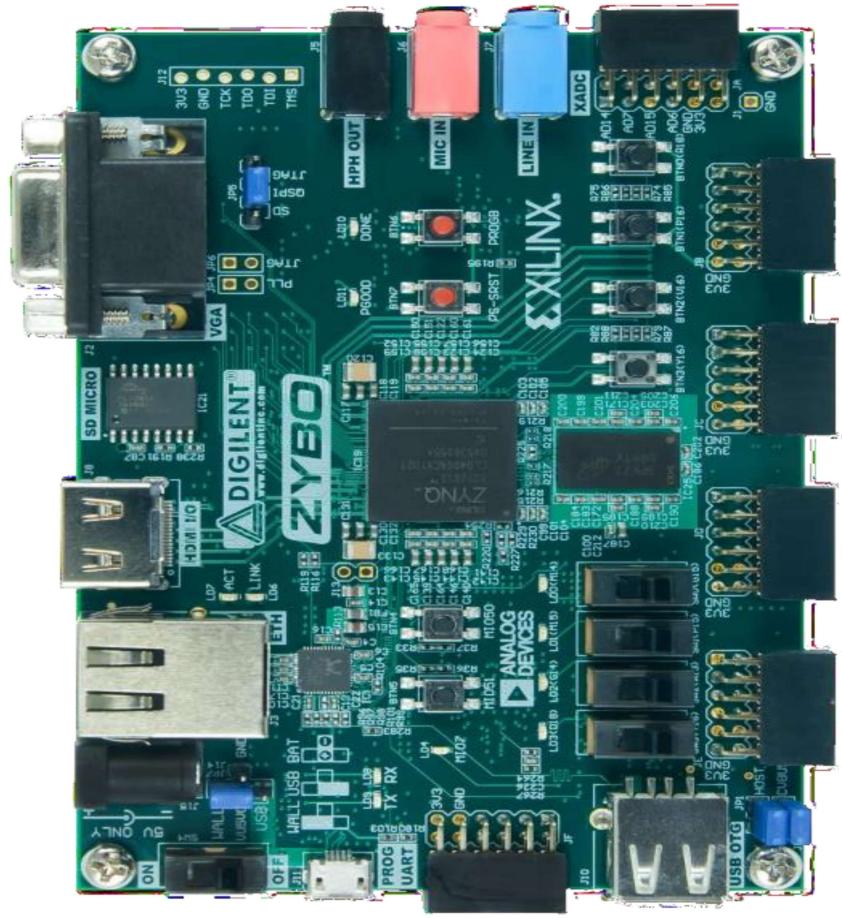
[Show Technologies](#)



Zybo Development Board



The ZyBO (Zynq BOard) is a feature-rich, entry-level embedded software and digital circuit development platform built around the smallest member of the Xilinx Zynq-7000 family, the Z-7010.

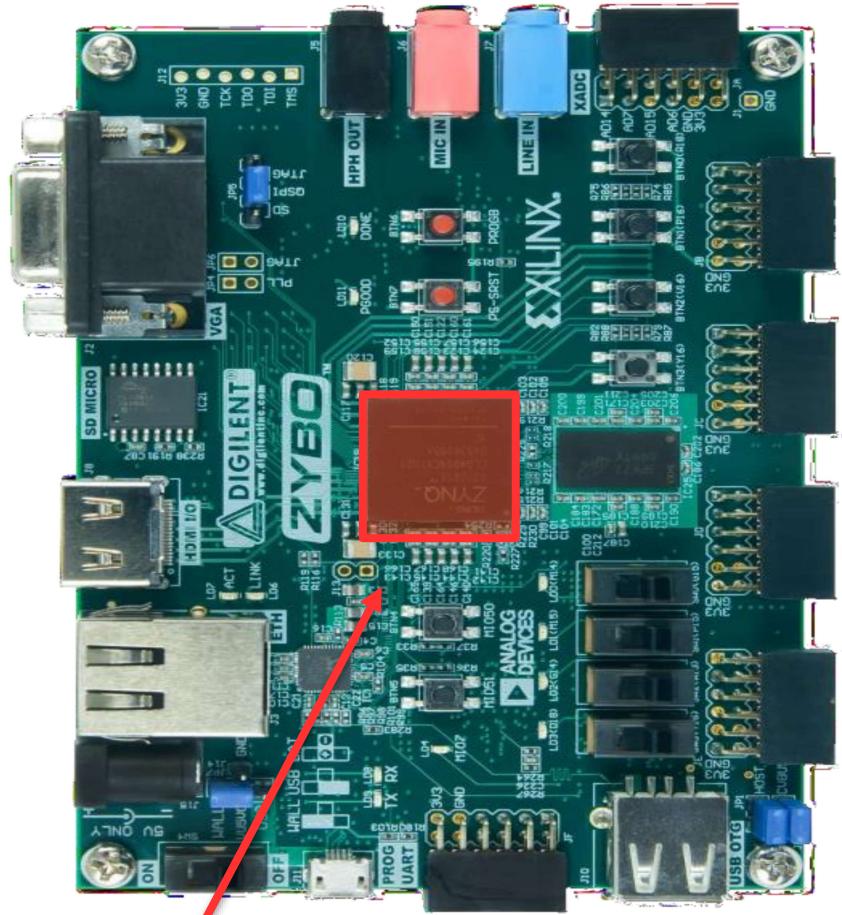


The Z-7010 is based on the Xilinx All Programmable System-on-Chip (AP SoC) architecture, which tightly integrates a dual-core ARM Cortex-A9 processor with Xilinx 7-series Field Programmable Gate Array (FPGA) logic.

Zybo Development Board

The Board

- **ZYNQ XC7Z010-1CLG400C**
- 512MB x32 DDR3 w/ 1050Mbps bandwidth
- Dual-role (Source/Sink) HDMI port
- 16-bits per pixel VGA source port
- Tremode (1Gbit/100Mbit/10Mbit) Ethernet PHY
- MicroSD slot (supports Linux file system)
- OTG USB 2.0 PHY (supports host and device)
- External EEPROM (programmed with 48-bit globally unique EUI-48/64™ compatible identifier)
- Audio codec with headphone out, microphone and line in jacks
- 128Mb Serial Flash w/ QSPI interface
- On-board JTAG programming and UART to USB converter
- GPIO: 6 pushbuttons, 4 slide switches, 5 LEDs
- Six Pmod connectors (1 processor-dedicated, 1 dual analog/digital, 3 high-speed differential, 1 logic-dedicated)

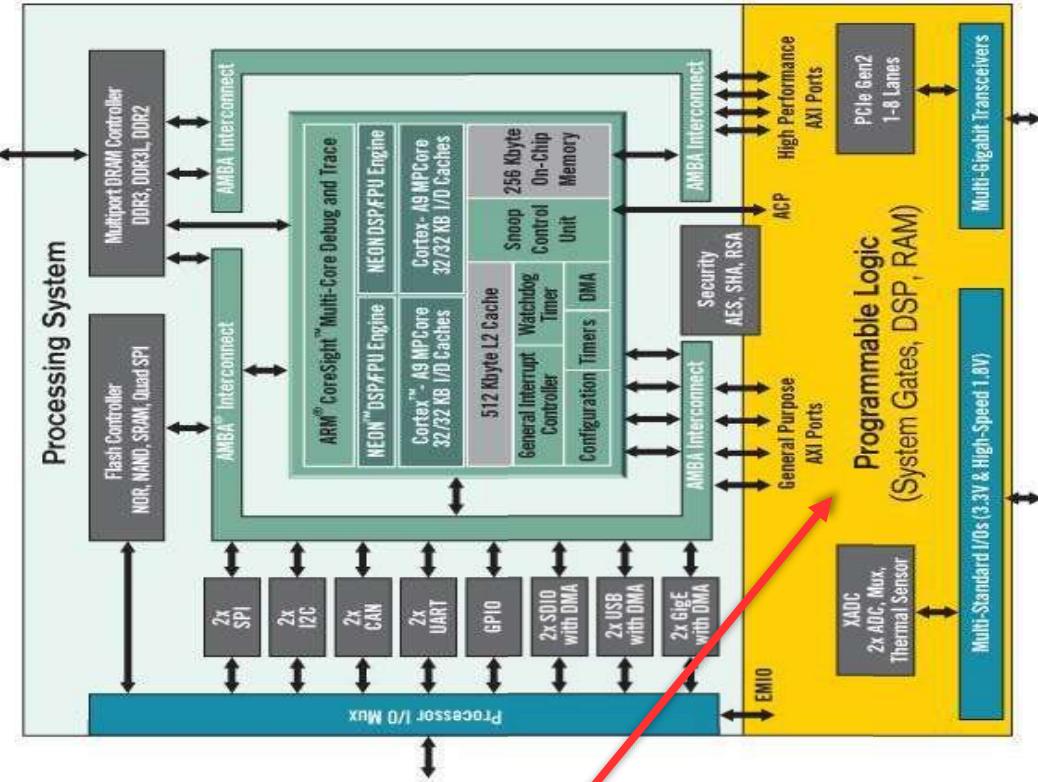


Zybo Development Board

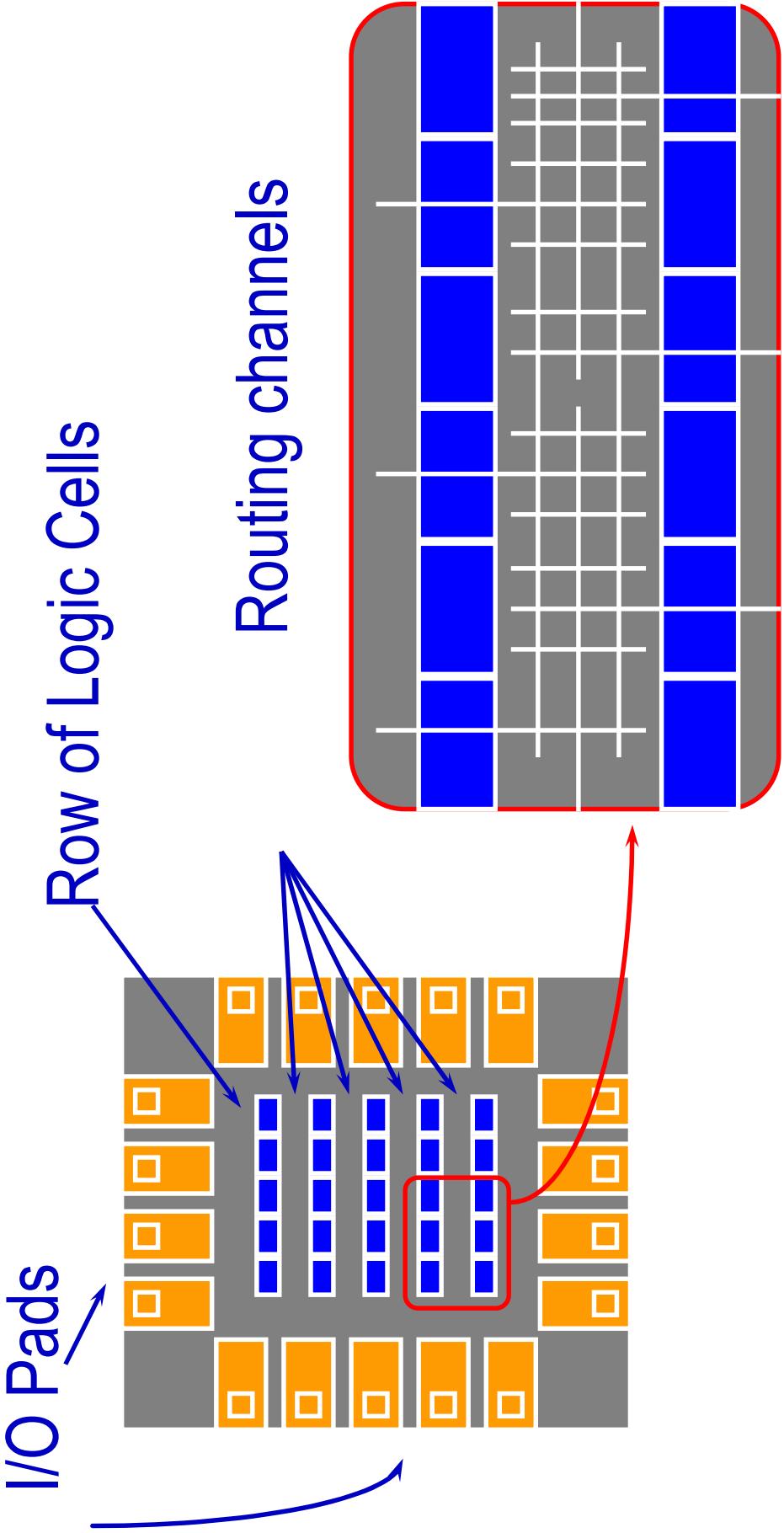


The ZYNQ Z-7010 AP SoC

- 650Mhz dual-core Cortex-A9 processor
- DDR3 memory controller with 8 DMA channels
- High-bandwidth peripheral controllers: 1G Ethernet, I2C
- Low-bandwidth peripheral controller: SPI, UART, CAN, I2C
- Reprogrammable logic equivalent to Artix-7 FPGA
 - 4,400 logic slices, each with four 6-input LUTs and 8 flip-flops
 - 240 KB of fast block RAM
 - Two clock management tiles, each with a phase-locked loop (PLL) and mixed-mode clock manager (MMCM)
 - 80 DSP slices
 - Internal clock speeds exceeding 450MHz
 - On-chip analog-to-digital converter (XADC)

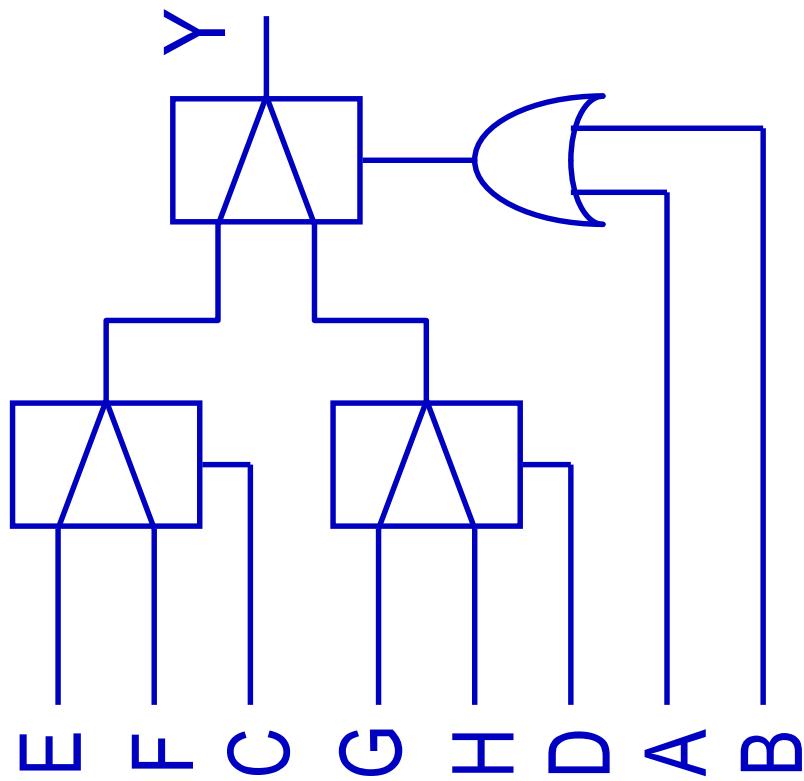


FPGA Actel

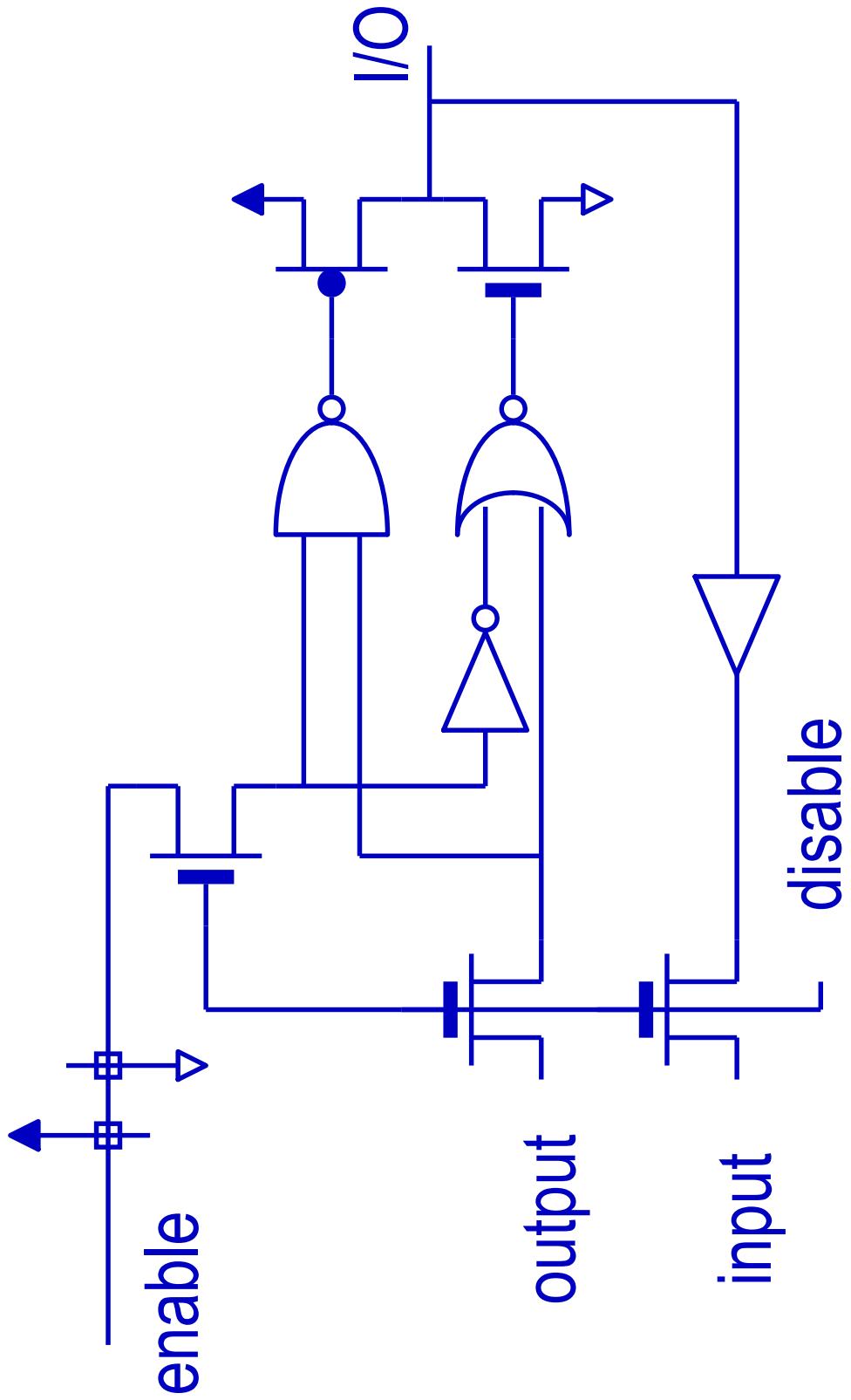


FPGA Actel: Basic Logic Cell

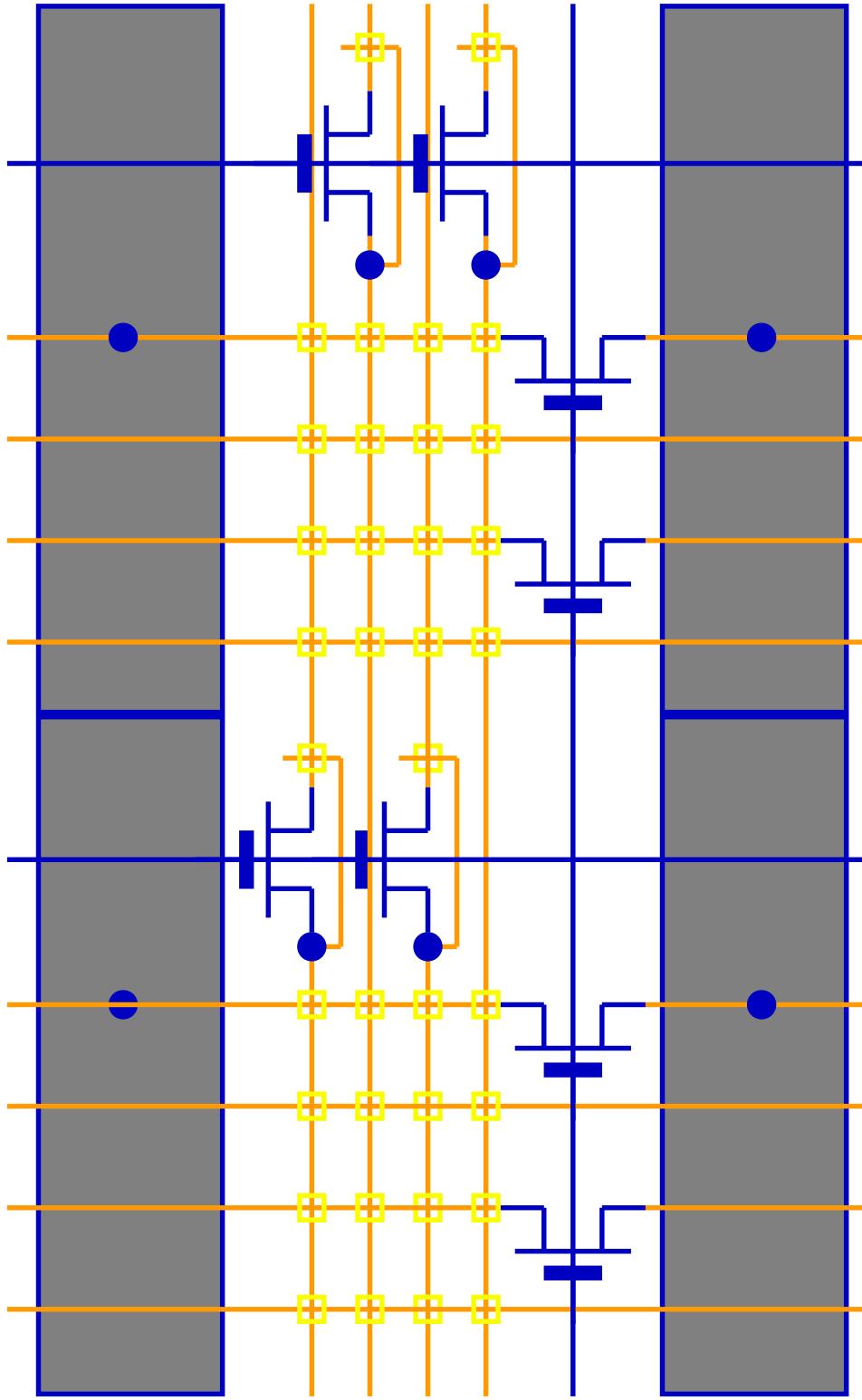
- 8 inputs
- Implements all functions with 2 or 3 inputs and many with 4 inputs
- Sequential Functions are obtained with two logic cells in feedback



FPGA Actel: I/O Pads



FPGA Actel: Interconnection

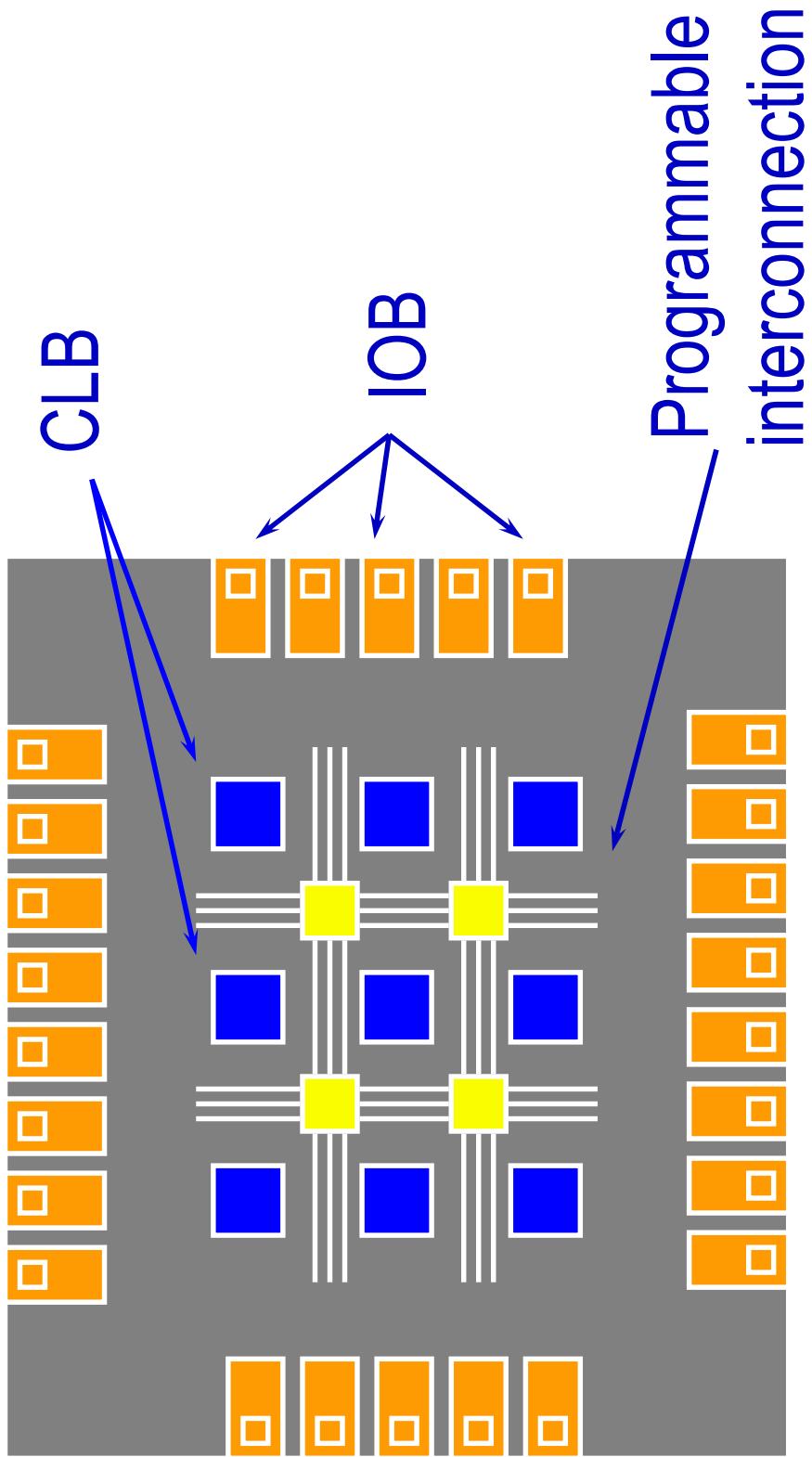


FPGA SRAM-based
(Xilinx)

Properties of **FPGA SRAM**-based

- Volatile Static Memory
 - ⌚ Configuration Load at power-on
 - ⌚ Required an External Memory
 - ⌚ Sensibility on external noise (soft errors)
 - ⌚ Re-programmable
 - ⌚ Technology CMOS standard
 - ⌚ Anti-fuse technology is not required

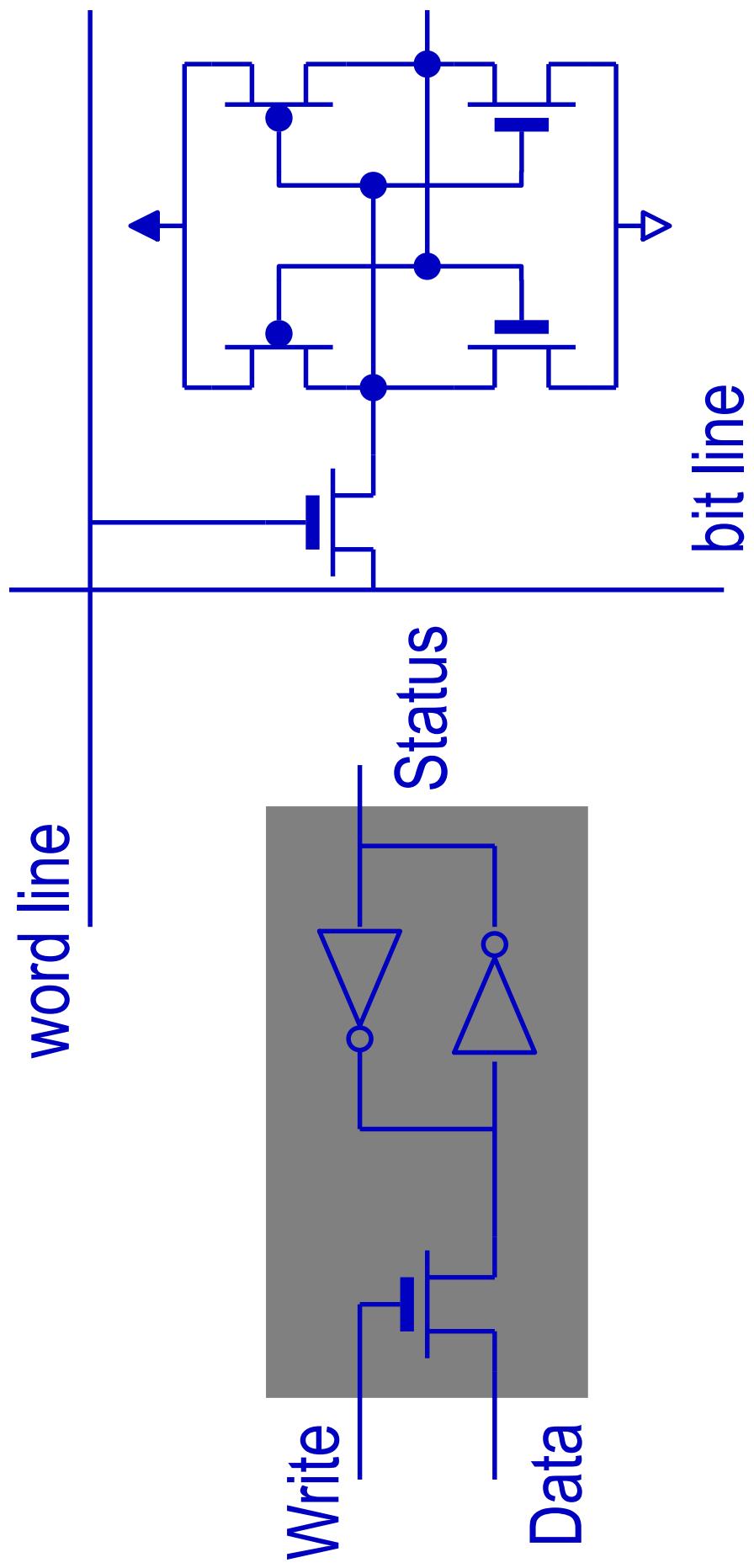
FPGA Xilinx Architecture



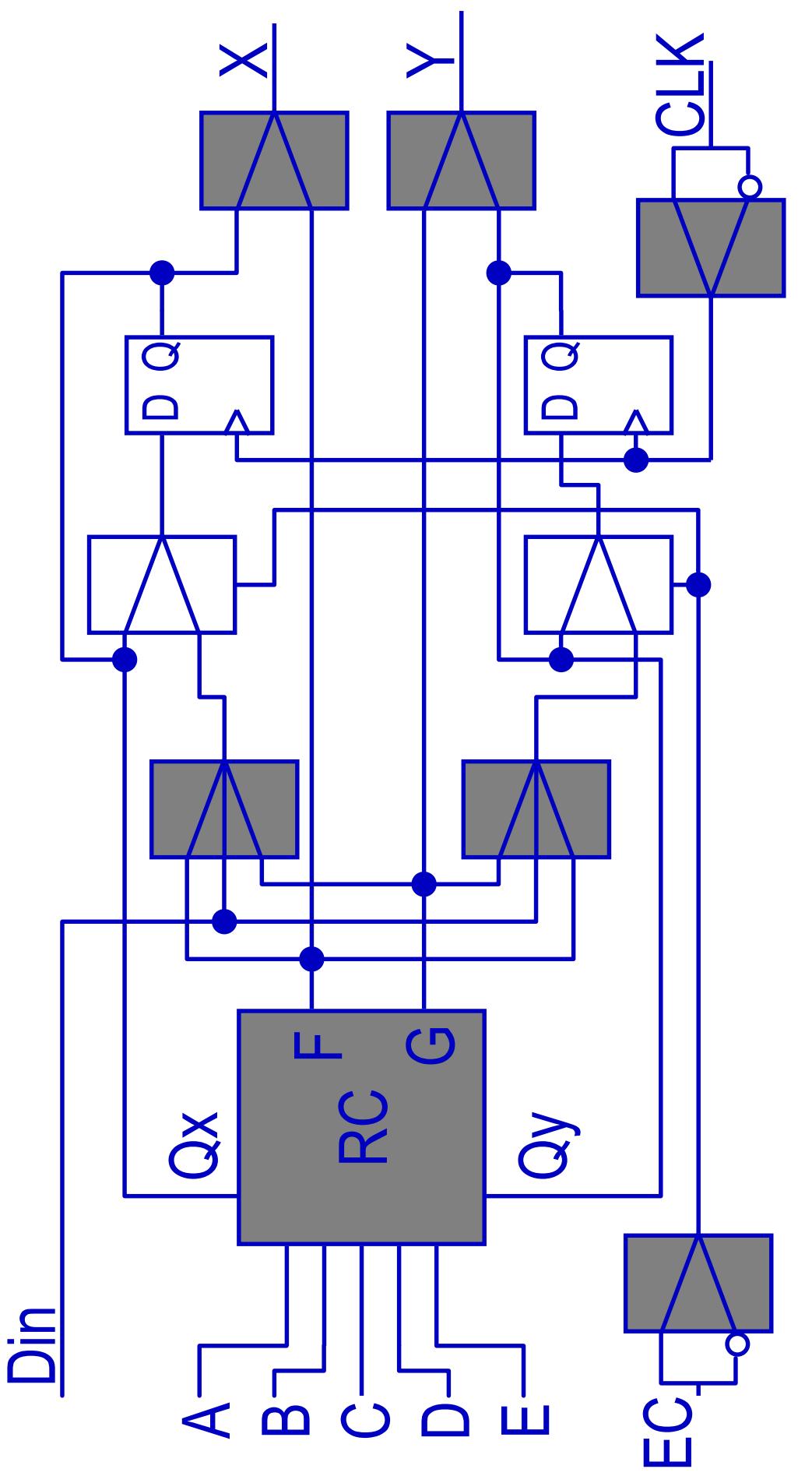
Building blocks

- Configurable Logic Blocks (CLB)
 - Where logic functions are implemented
- Input-output circuits (IOB)
 - Programmability of functionality and direction
- Routing Channels horizontal and vertical
- Memory Cell and Routing Cell are spread along the entire matrix

Memory Cell



CLB Structure



CLB properties (1/2)

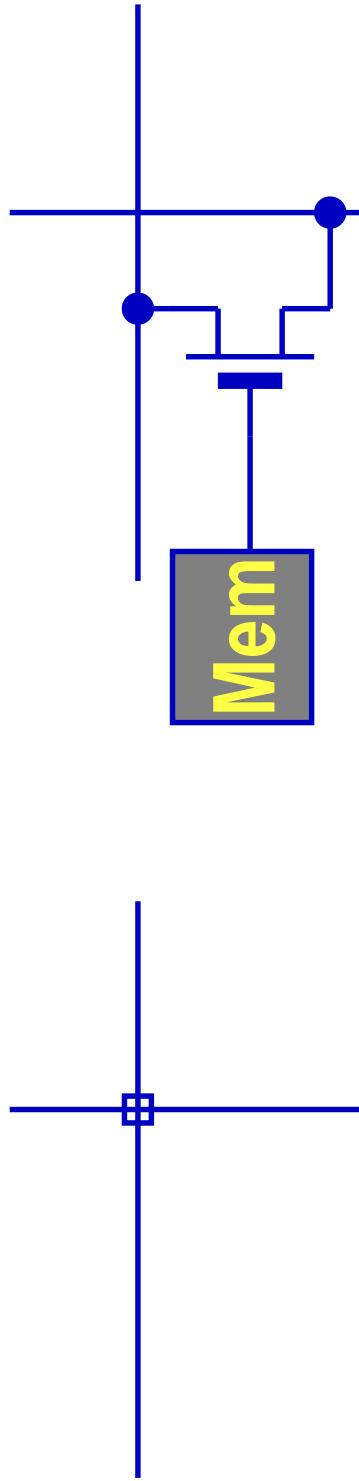
- 5 inputs, data in, clock and enable
- 2 symmetric outputs ($X \neq Y$)
- Logic Function Generator (PROM)
 - 32 cells (all functions with 5 inputs)
 - 2 splitted outputs ($F \neq G$) or a common one ($F = G$)
- 2 flip-flop D per logic block
 - positive or negative edge-triggered with enable clock

CLB properties (2/2)

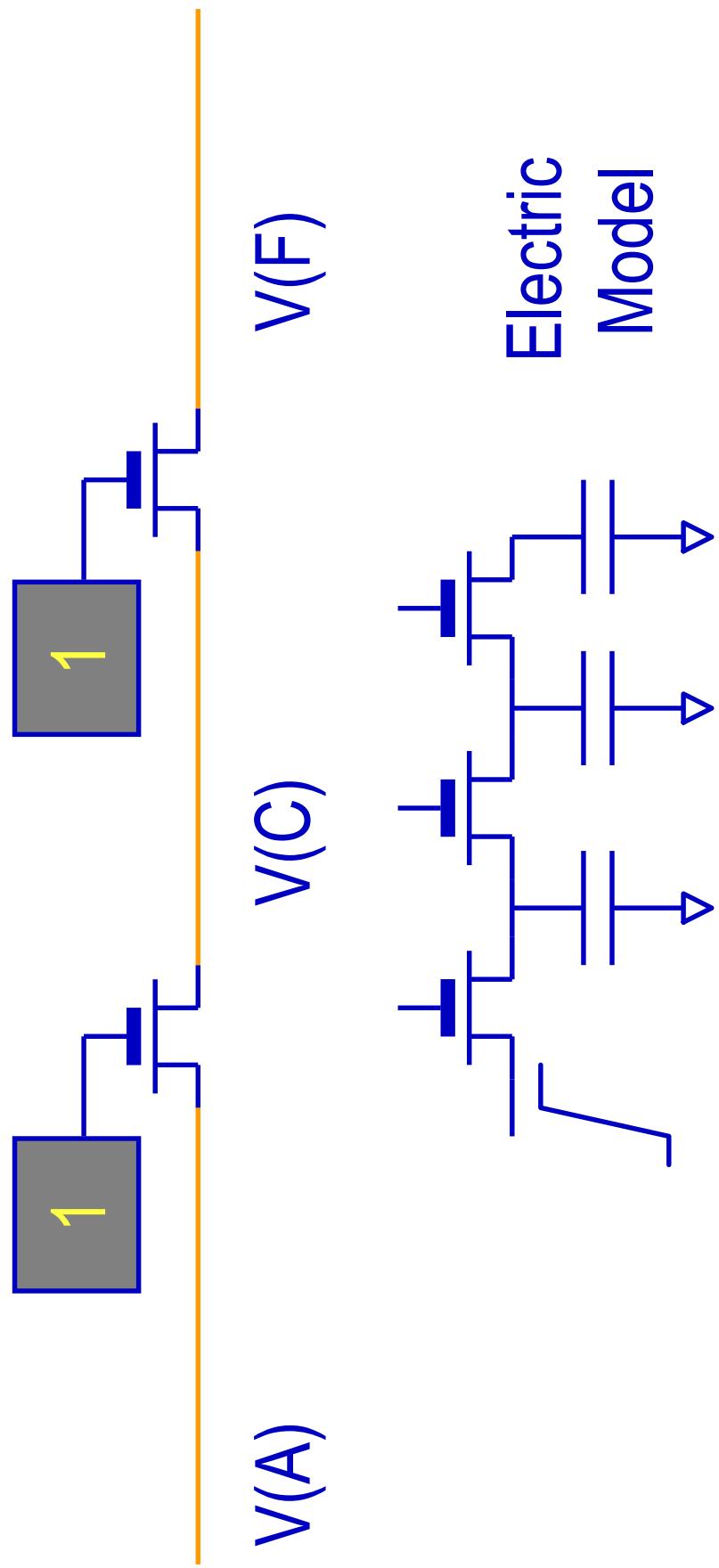
- Sequential functions with internal feedback ($Q_x \in Q_y$)
 - To implement Finite state machine
 - Synchronous Design Style
- DIN input avoiding the combinatory network
 - CLB as a building element of a CLB
 - Reduction of the propagation delay

Programmable interconnection

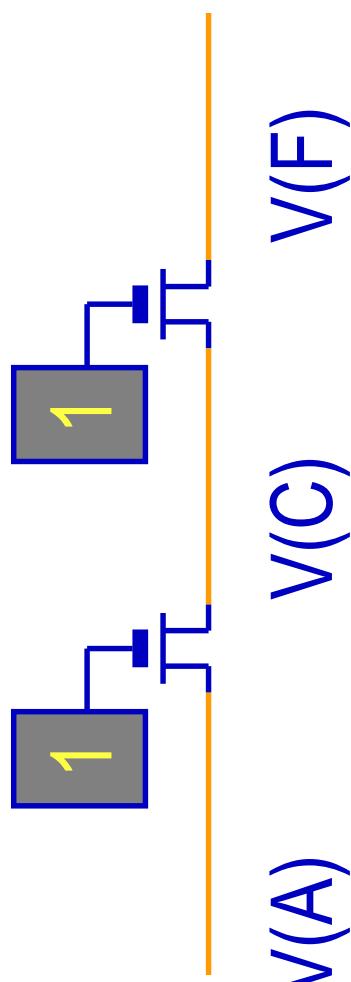
- Programmable interconnections are obtained through a pass transistor driven by a memory cell
 - Programmable Interconnect Point (PIP)



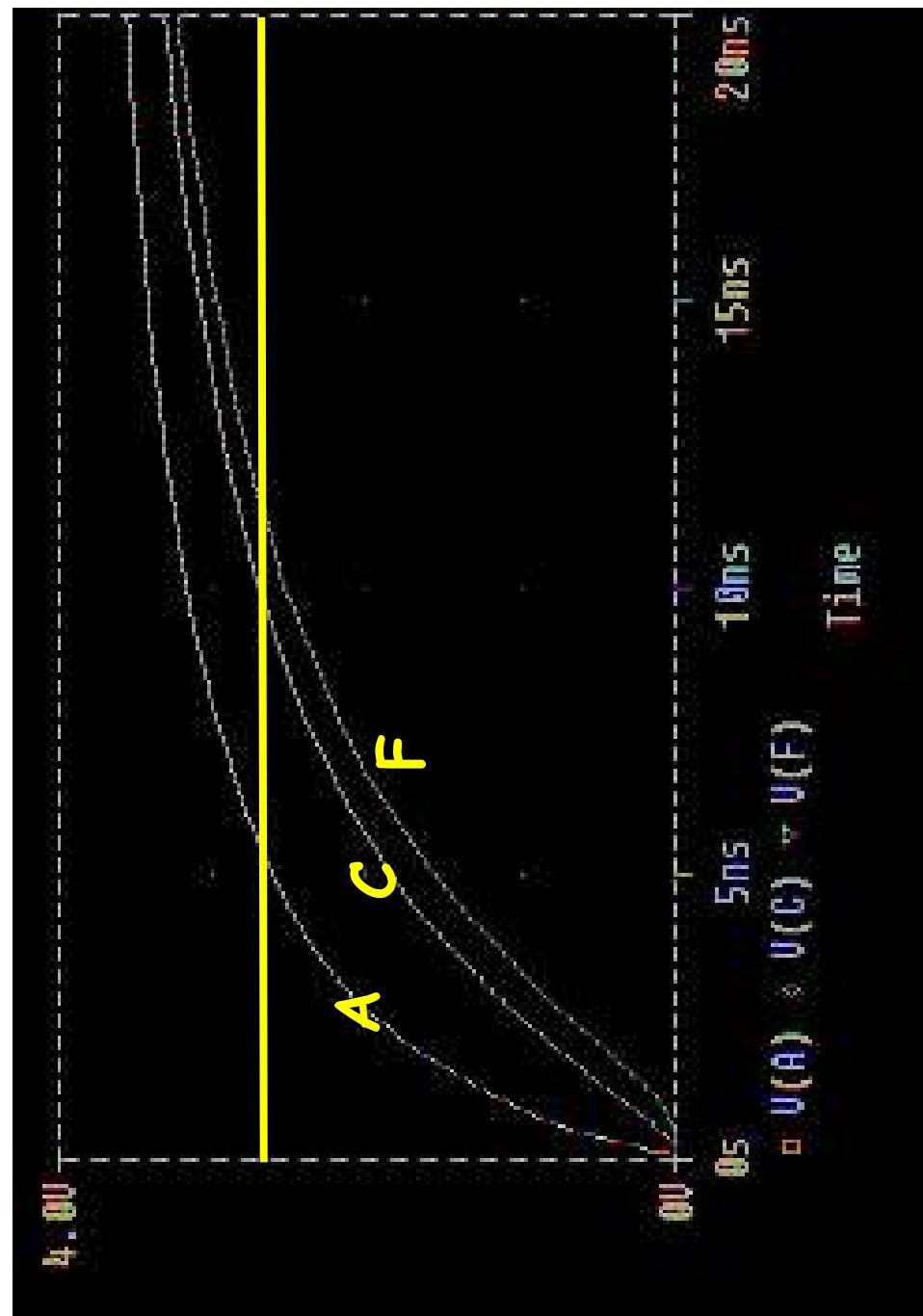
Interconnection



Simulation Waveforms



$V(A)$ $V(C)$ $V(F)$



Routing Problem

- Many short segments (high flexibility) determine long delay (many transistors in series)
- Few long segment (smaller propagation delay) makes connectivity more difficult

Required routing resources with different characteristics:

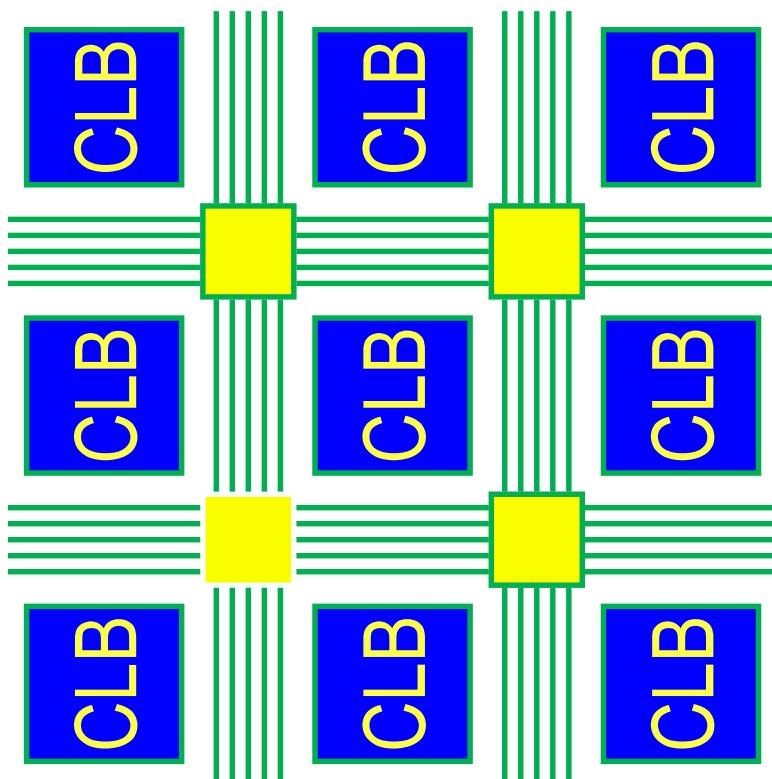
Short and long segments

Possible Interconnection

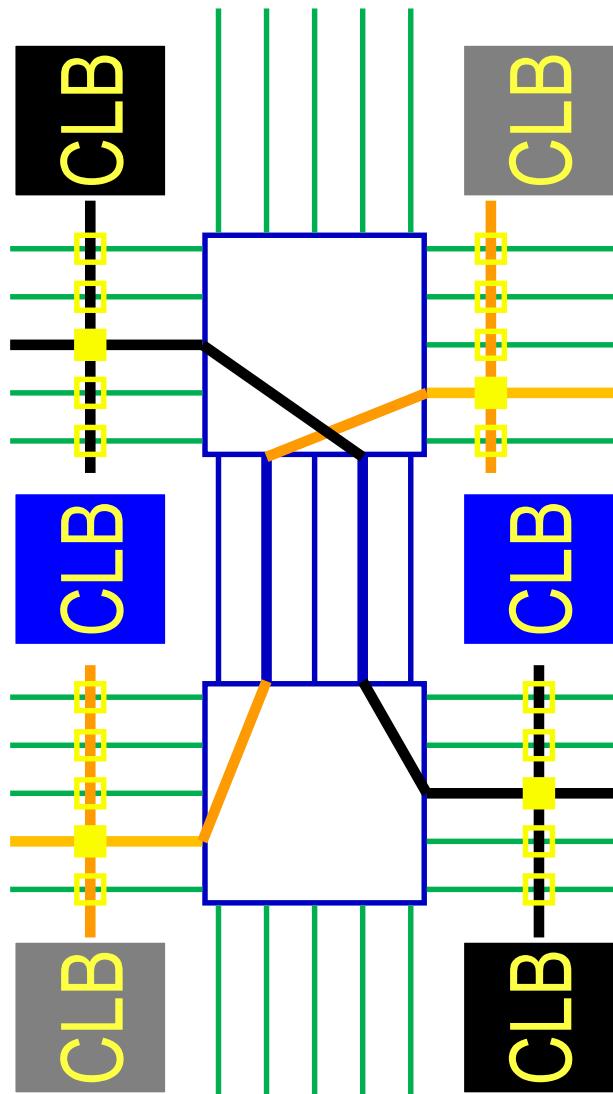
- **General**
 - Segment routed through small exchange matrix (magic box)
- **Direct or Local**
 - To link the output of a block to the input of a neighborhood one
- **Global**
 - Long interconnection lines for global use

General Interconnection

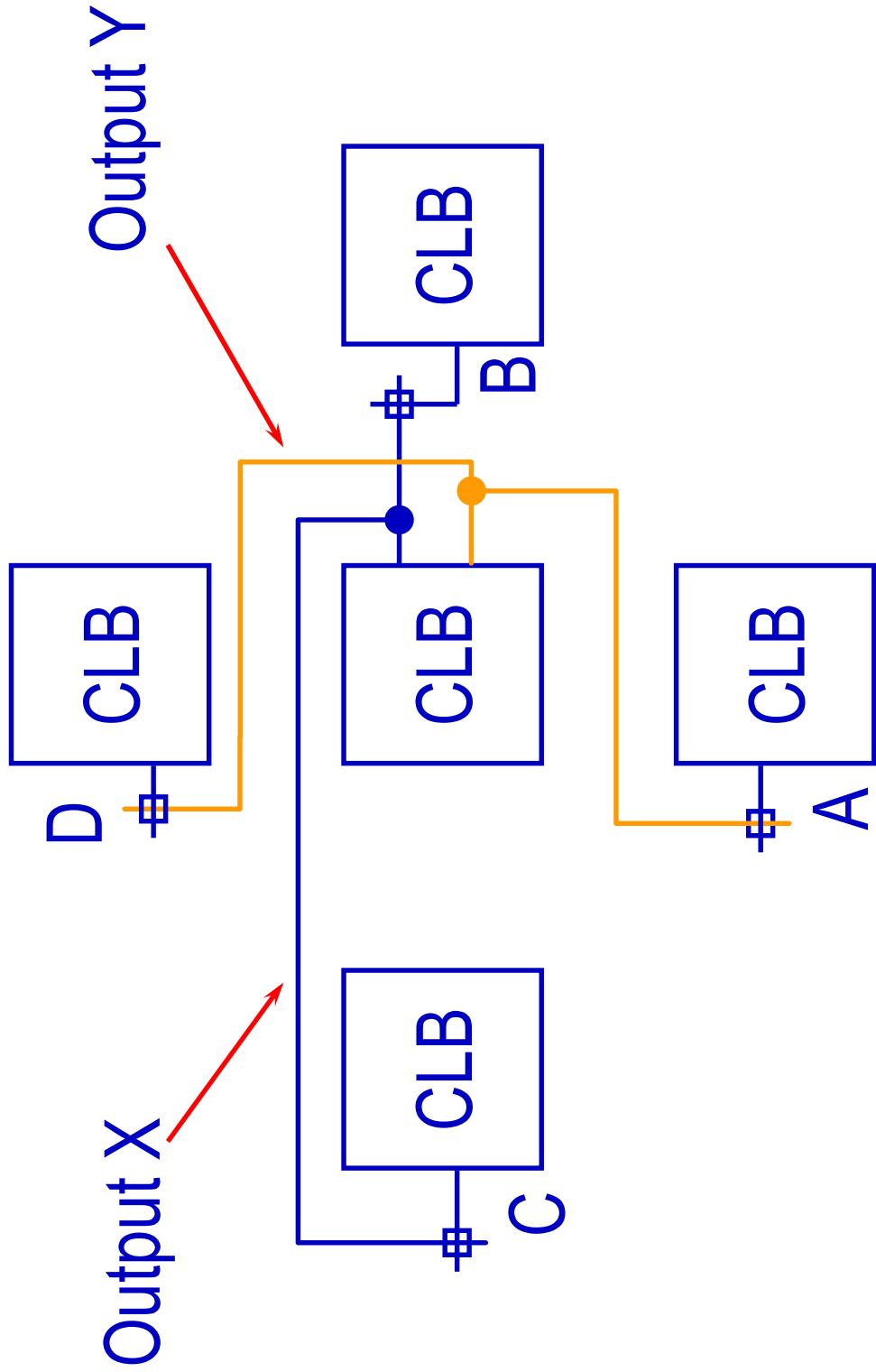
- 5 horizontal and Vertical Segments
- Exchange Matrix (5×5)
- CLB inputs and outputs are available on the channels through PIP



Example of a General Interconnection



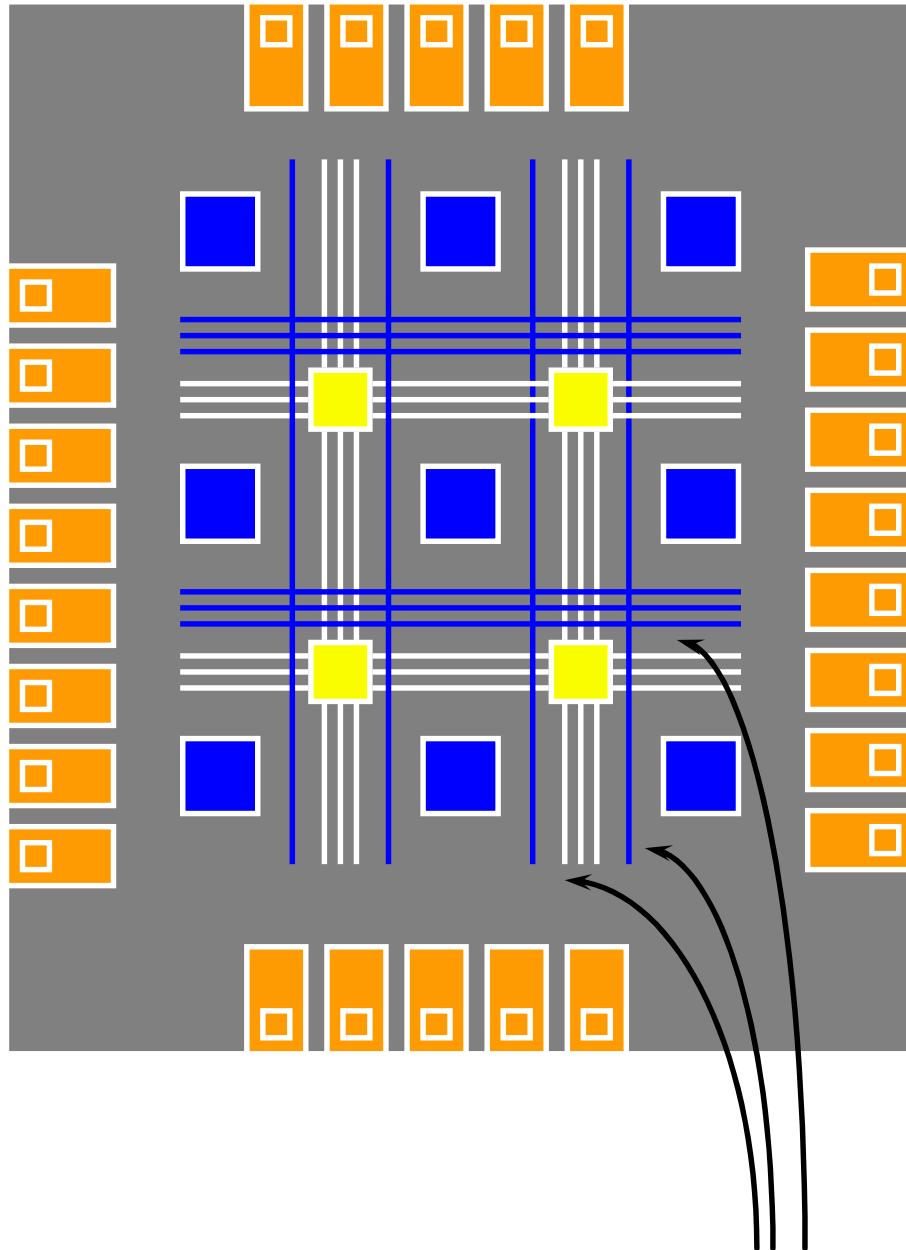
Direct Interconnections



Direct Interconnections

- Dedicated Local Connection among adjacent blocks
 - Very likelihood to happen
- Minimum and Defined Propagation Delay
- No use of general resources
- Output X is propagated to CLB on both right and left sides
- Output Y is propagated to CLB on upper and lower sides

Global Interconnections (long lines)

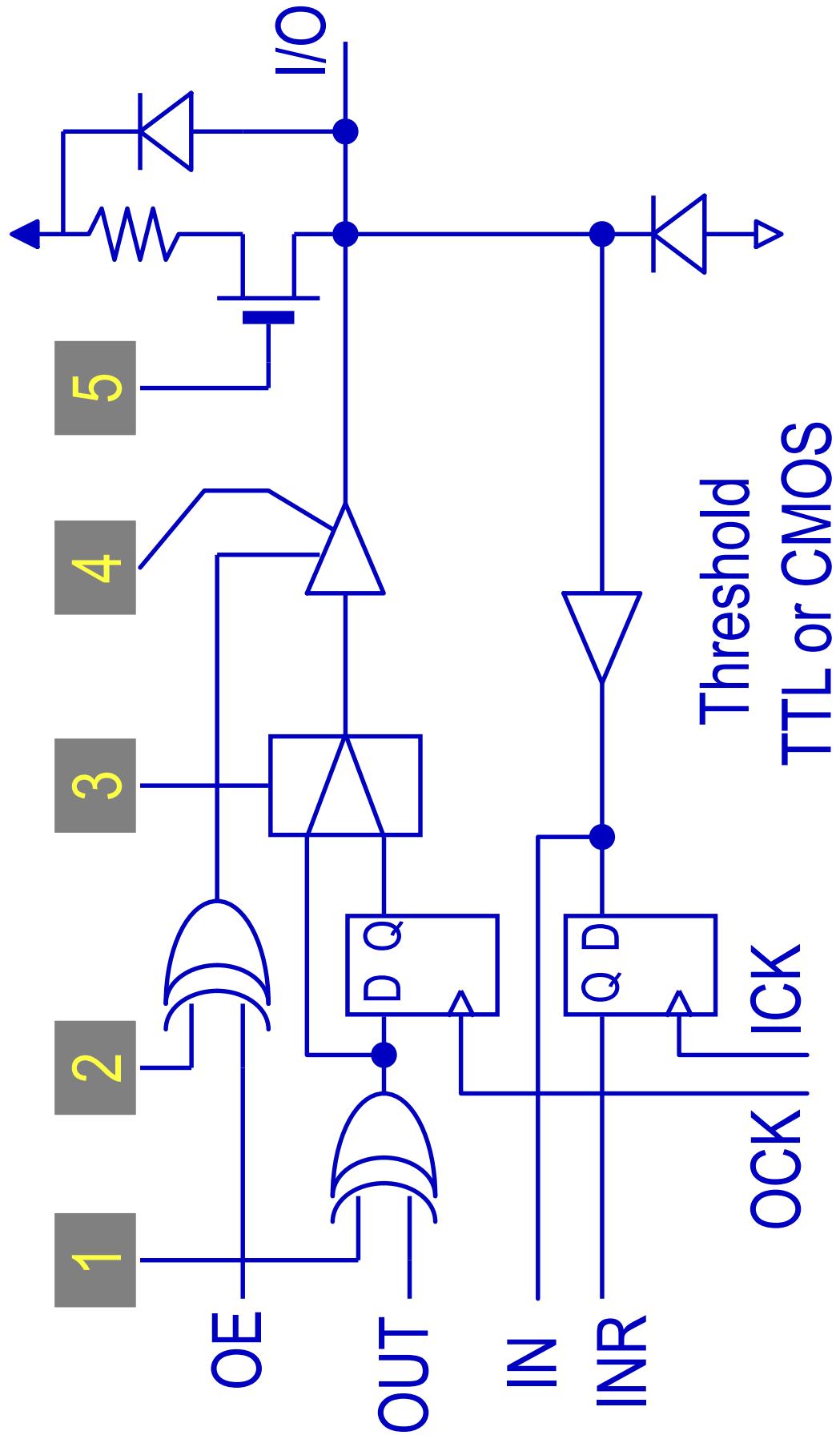


long
lines

Global Interconnections

- Long lines across the entire circuit vertically (3) and horizontally (2) without using exchange matrix
- Used for global signal (clock) or with long distance
 - Minimum clock skew
 - Possibly to be used as *FPGA* internal buses

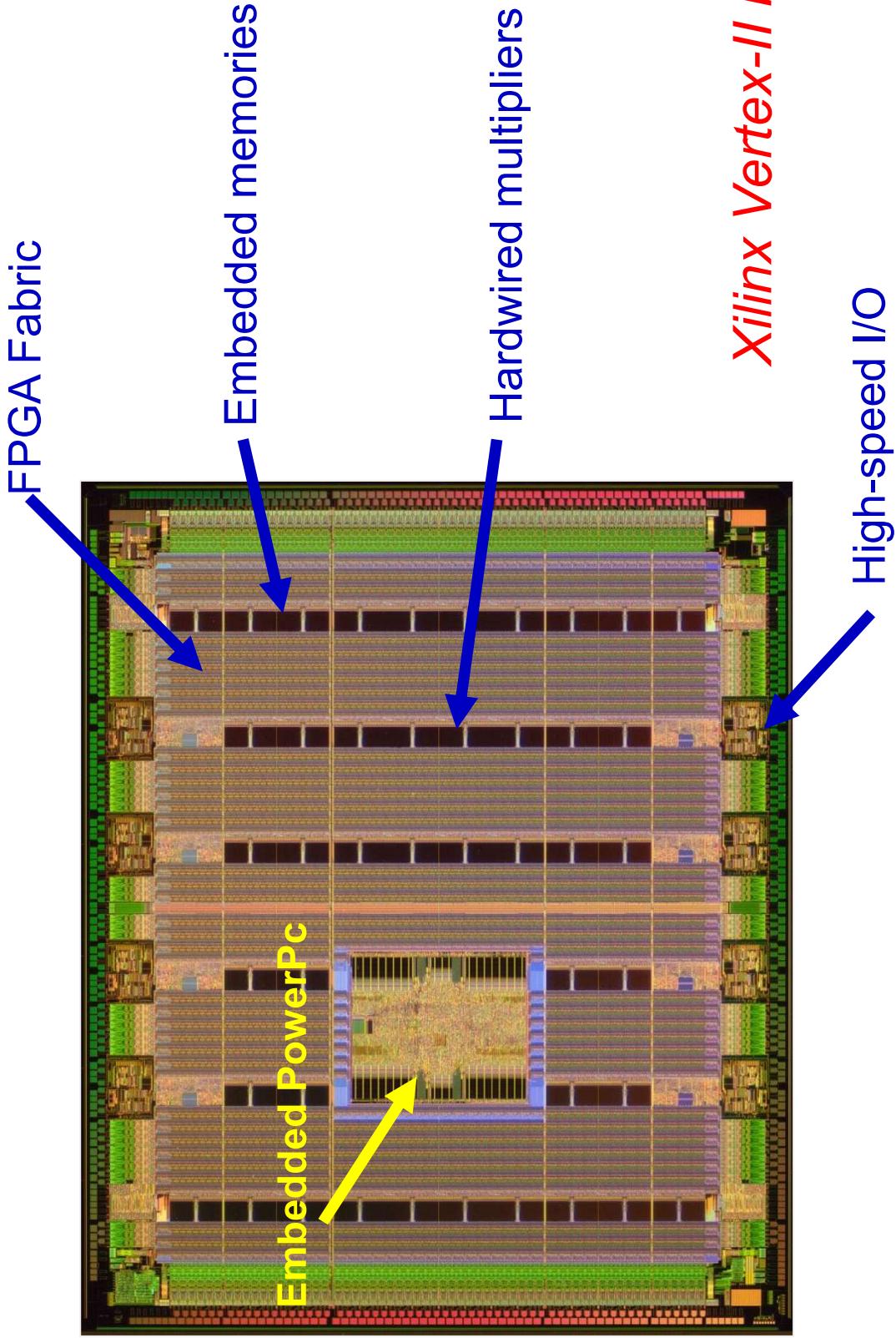
IOB Structure



IOB Functionalities

- Input-Output Terminal
- Possible to select:
 - 1 Output signal polarity
 - 2 Output enable signal polarity
 - 3 Output registered or Direct
 - 4 Output Buffer slew-rate
 - 5 Resistive pull-up
 - Registered input data (synchronization)

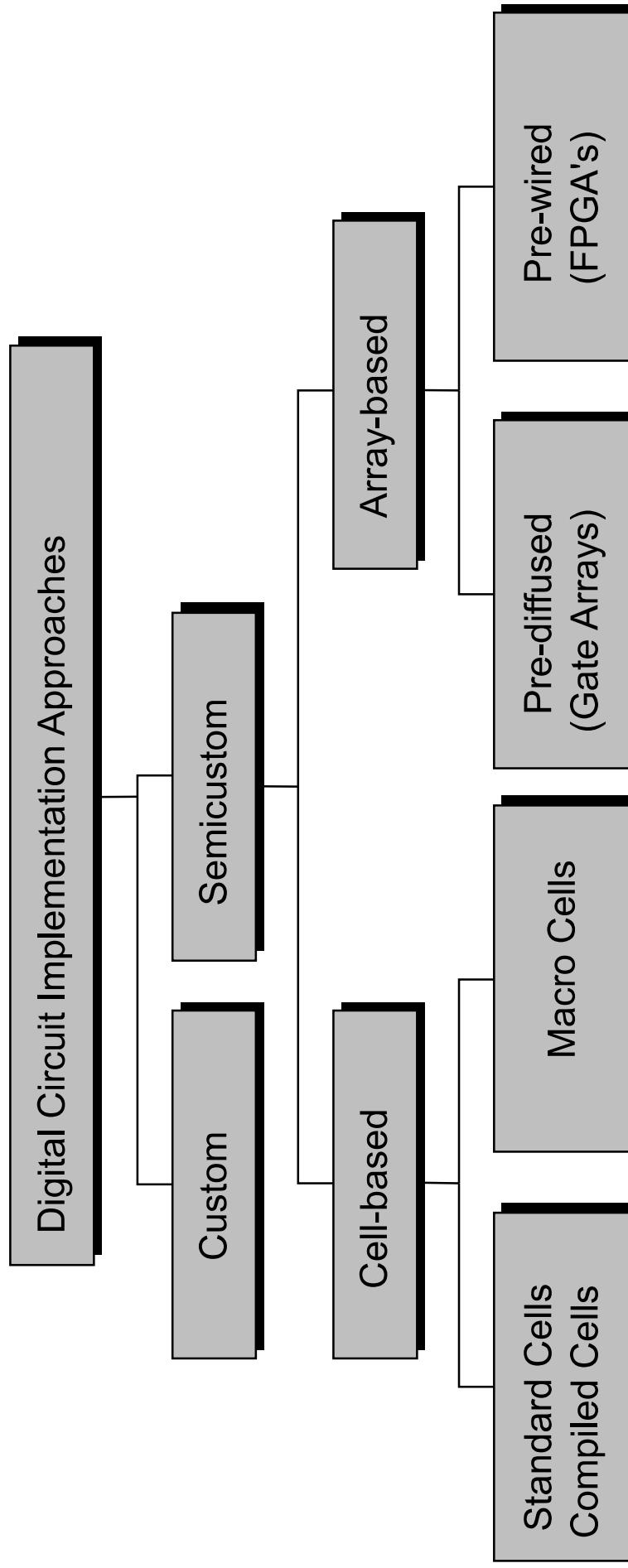
Heterogeneous Programmable Platforms



Outline

- Electronic Abstraction Level Design
- Integrated Circuit Design Styles
- Design Methodologies and Flows
- Cost-Performance Trade-off
- Field Programmable Gate Array
- **Design Productivity**
- **Evolution of EDA Industry**
- How to map a system/algoritm to a System on Chip

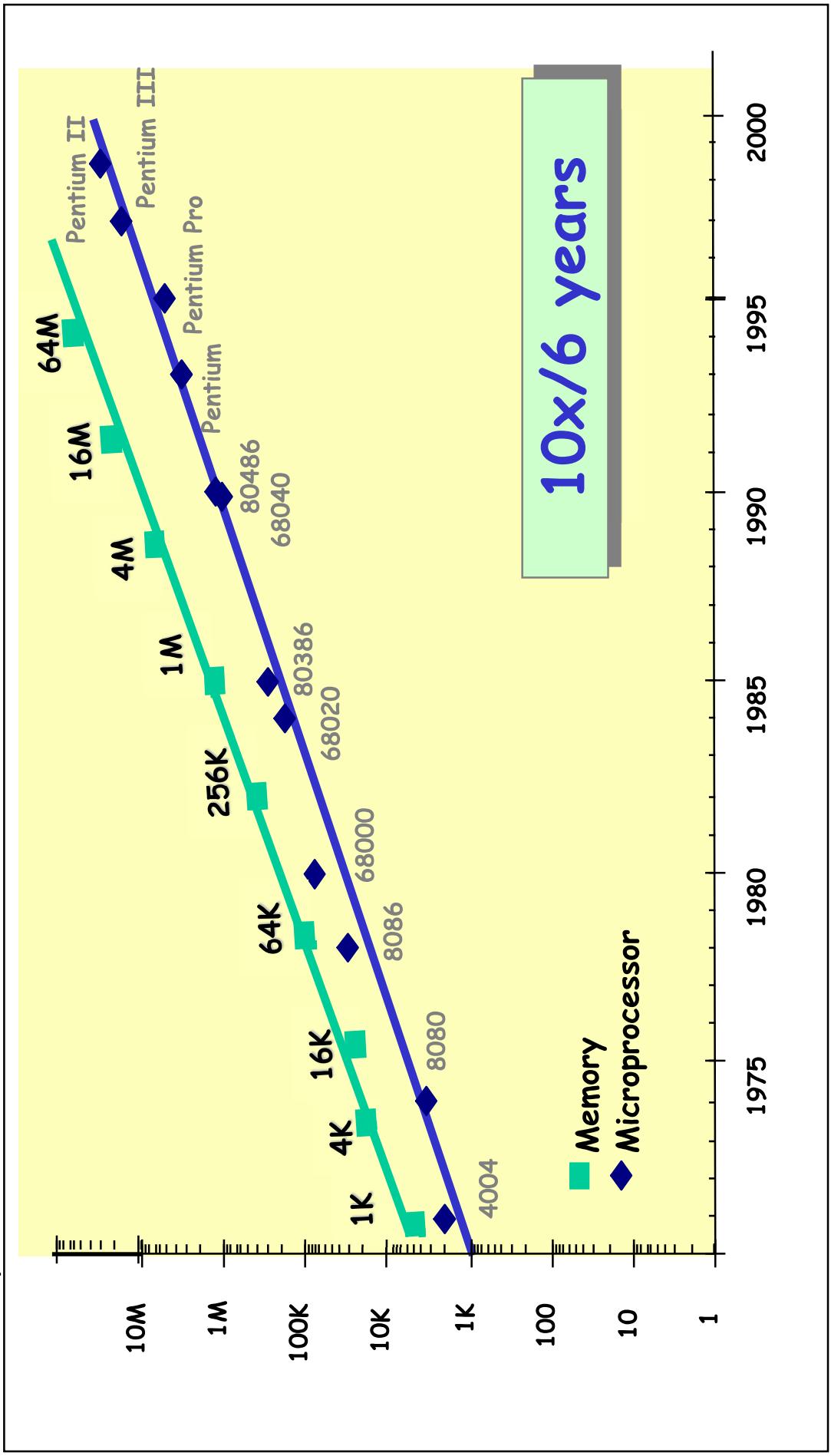
Integrated Circuit Design Styles



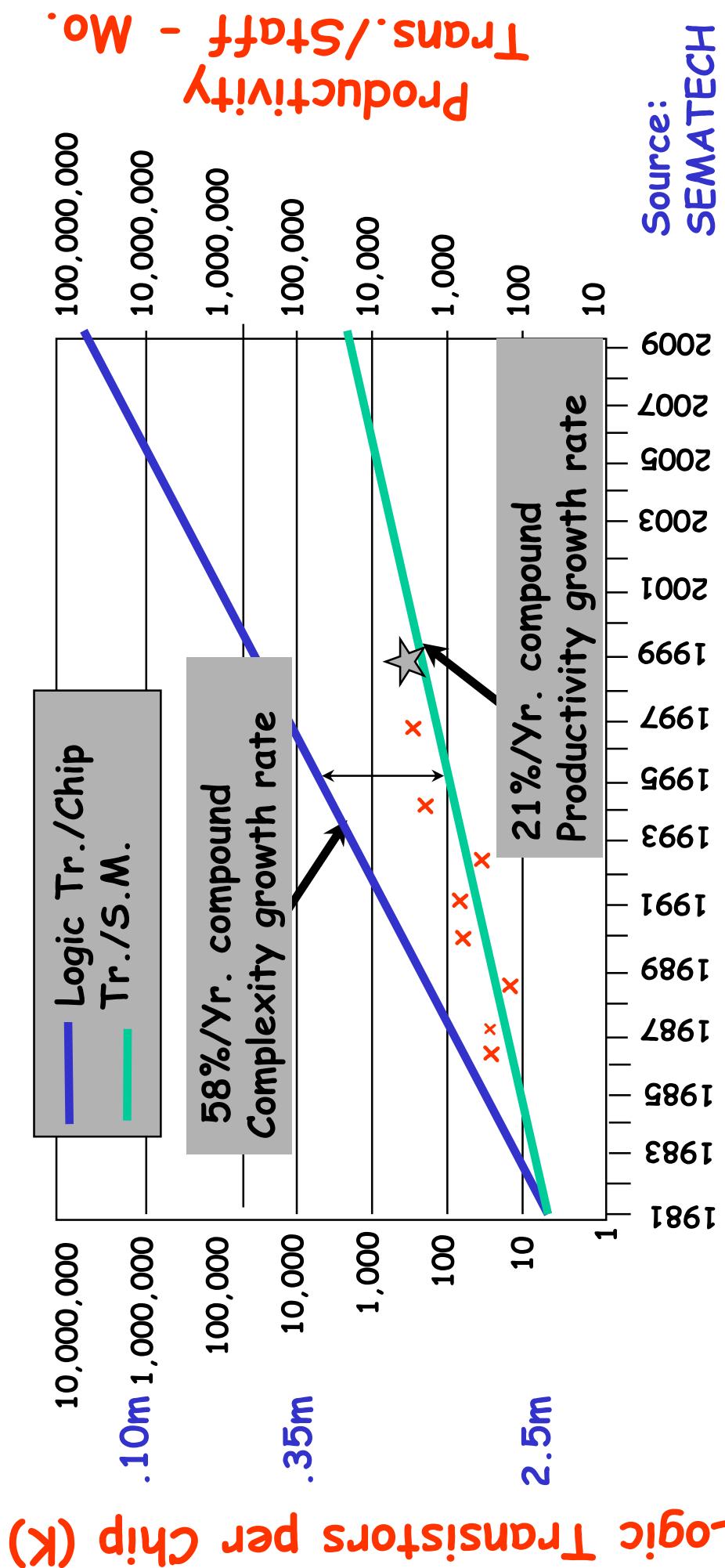
Let's compare the Design Productivity !!

VLSI Technology: Moore's Law

Transistors per die

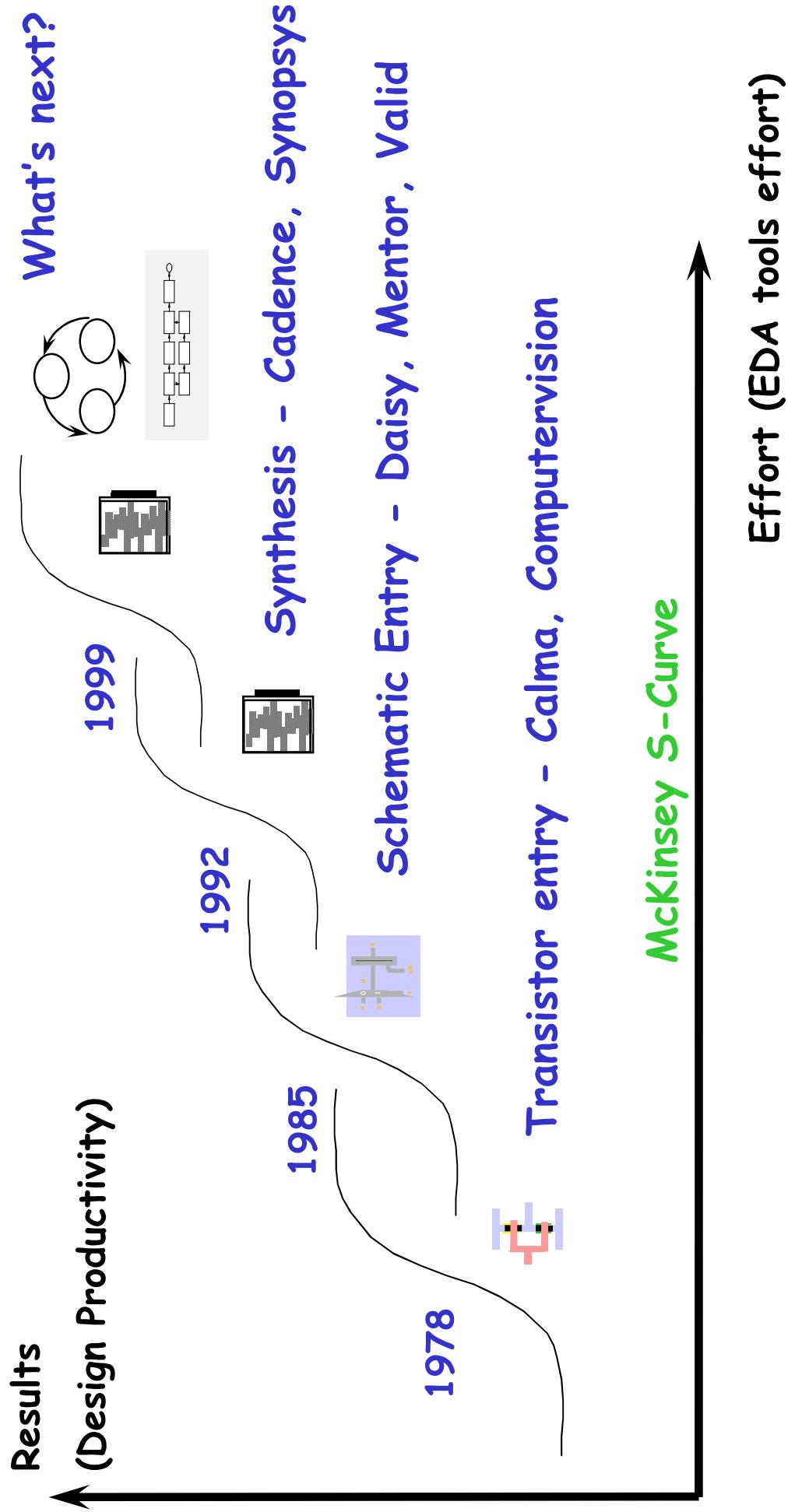


Design Productivity Gap

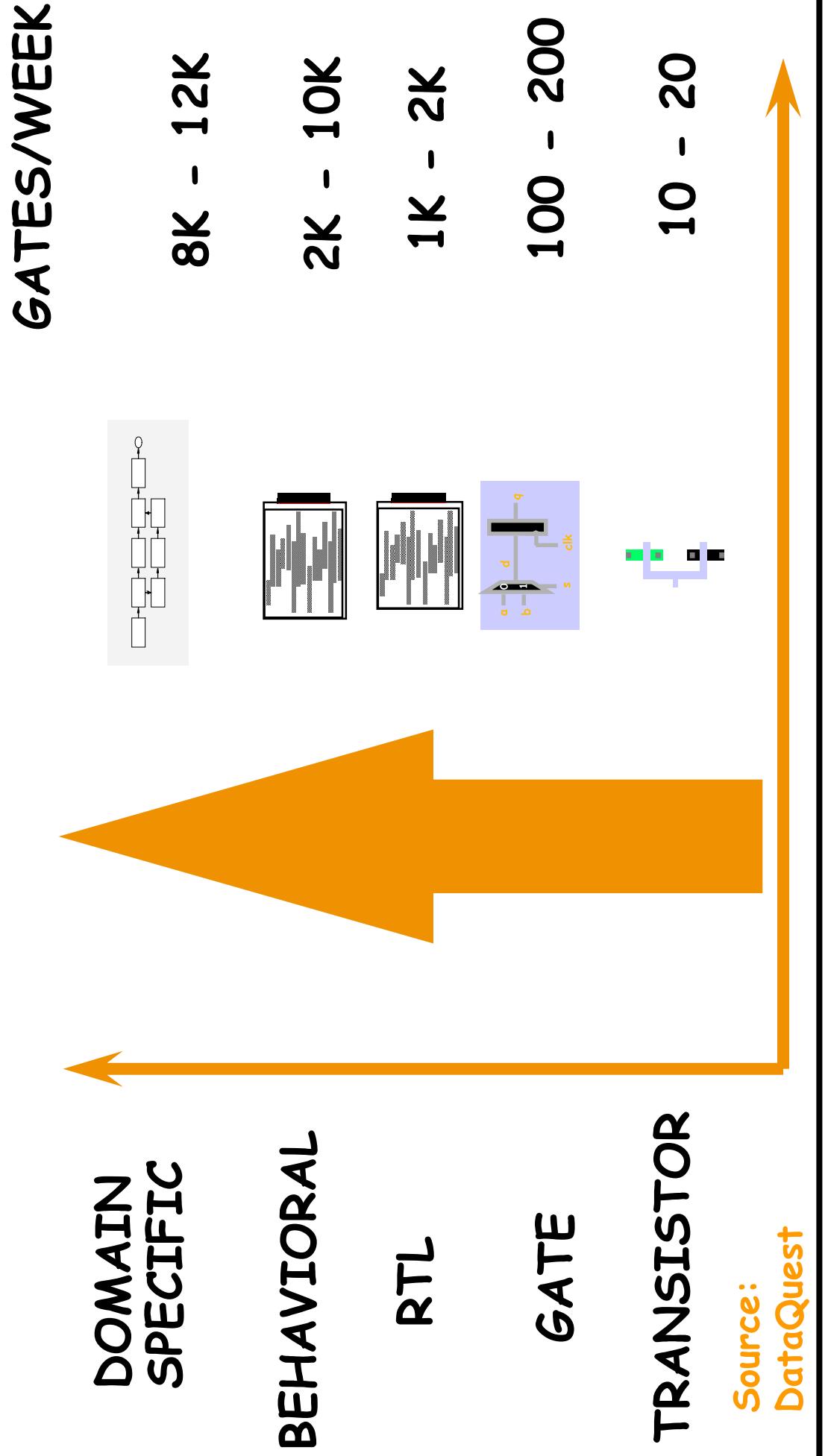


Logic Transistors per Chip (K)

Evolution of the EDA Industry



Design Productivity by Approach



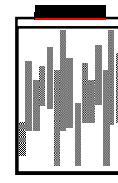
To Design, Implement, Verify 10M transistors

Staff Months

62.5

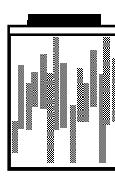
Implementations here are often not good enough

Behav.

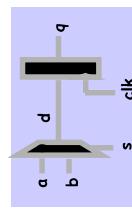


625

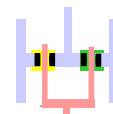
RTL



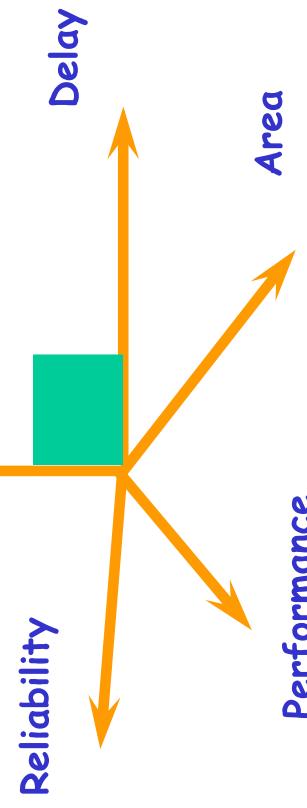
Gate



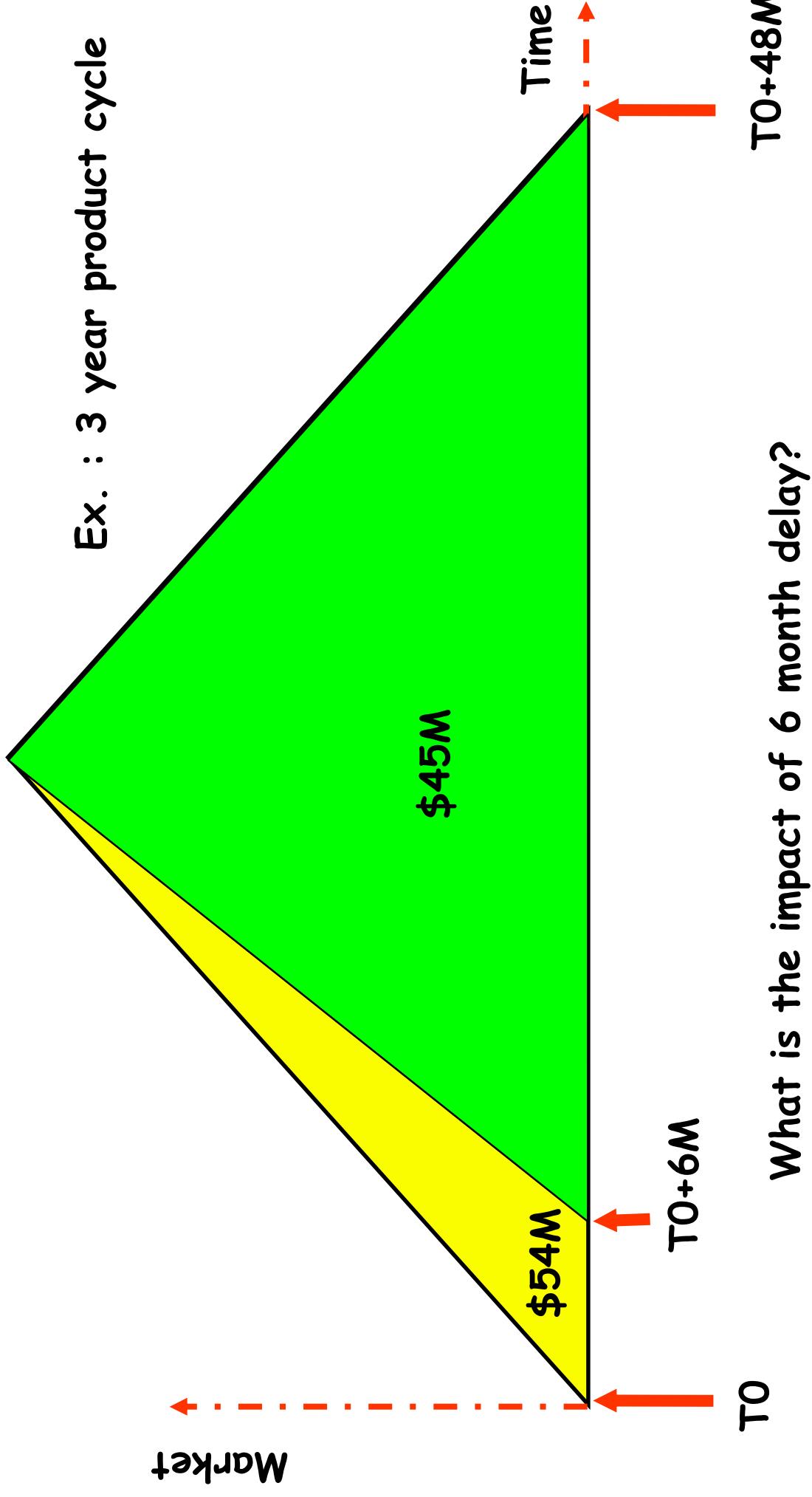
Trans.



62,500

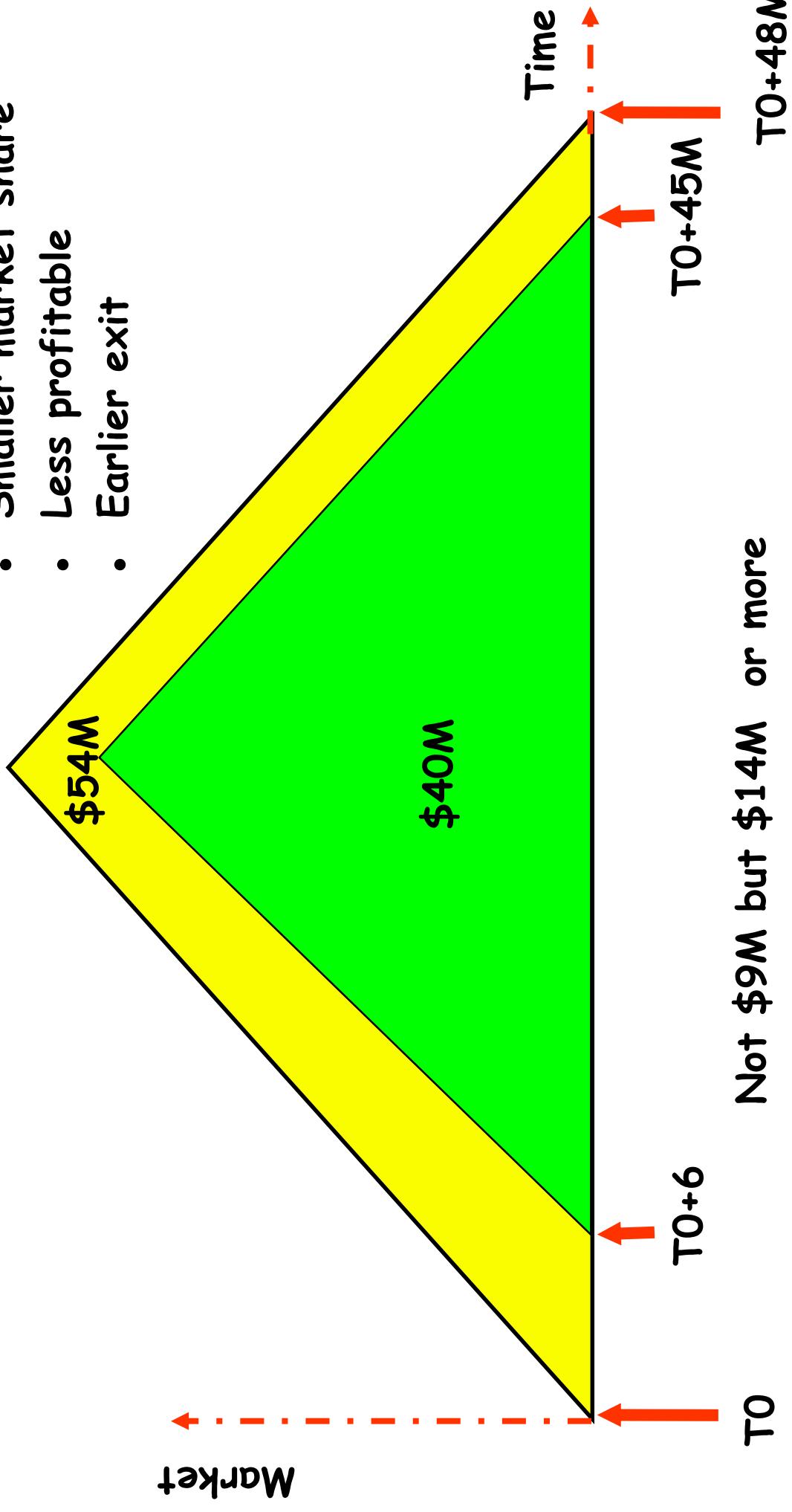


Time to Market (1/2)



Time to Market (2 / 2)

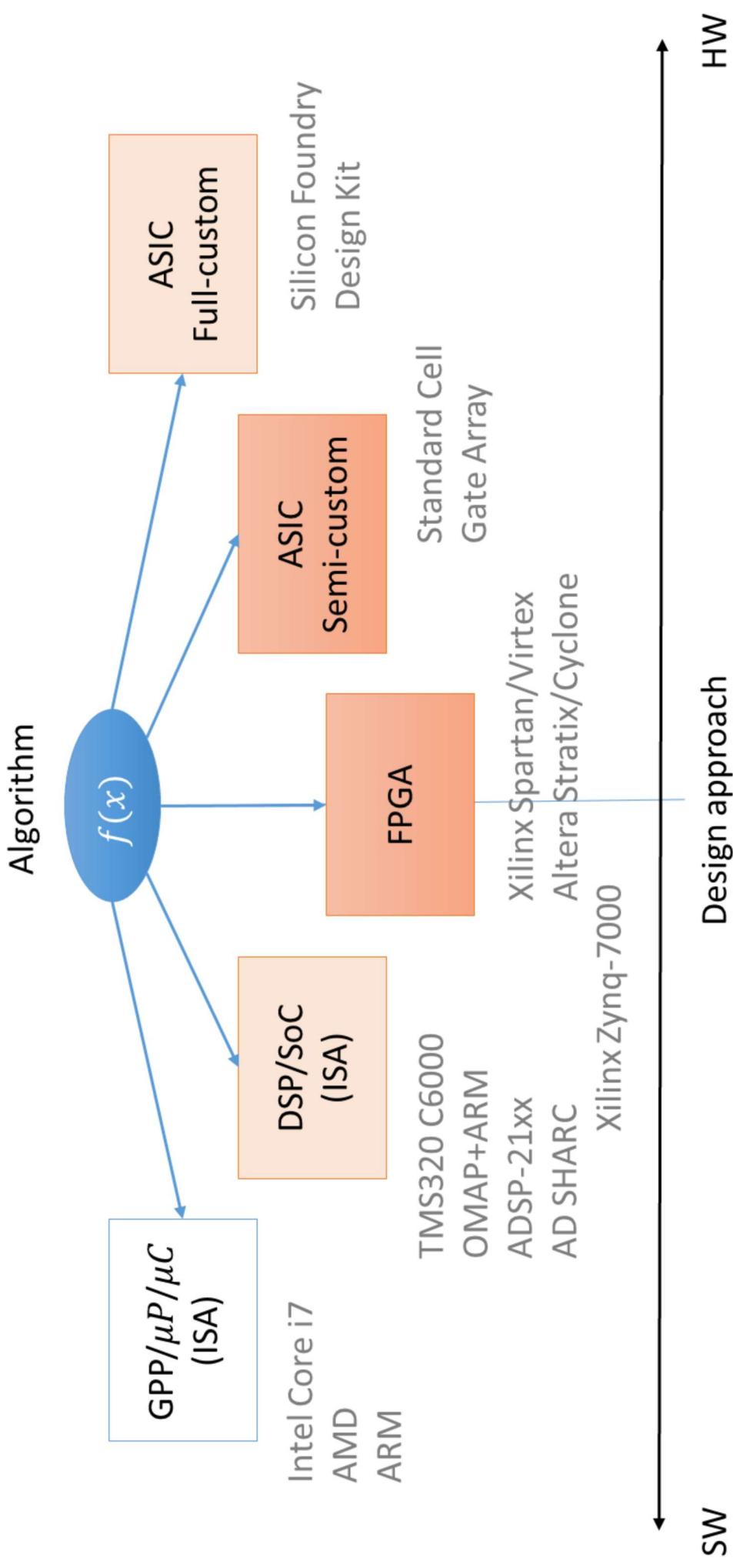
- Smaller market share
- Less profitable
- Earlier exit



Outline

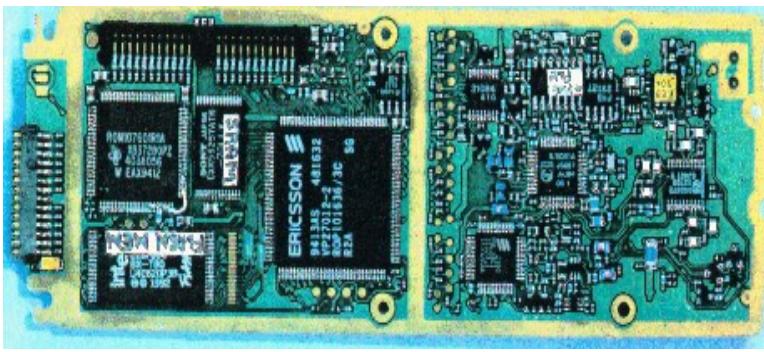
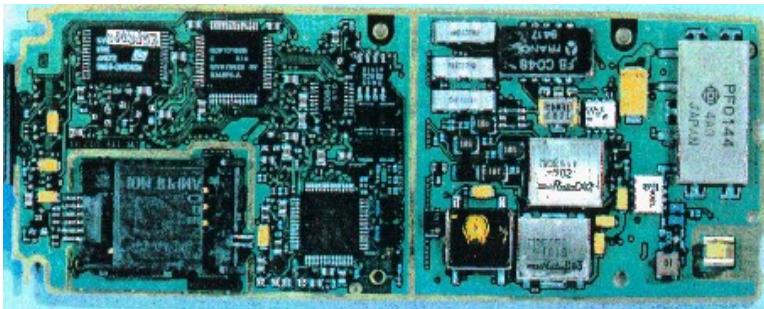
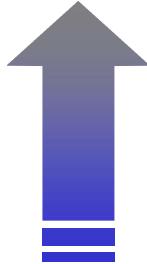
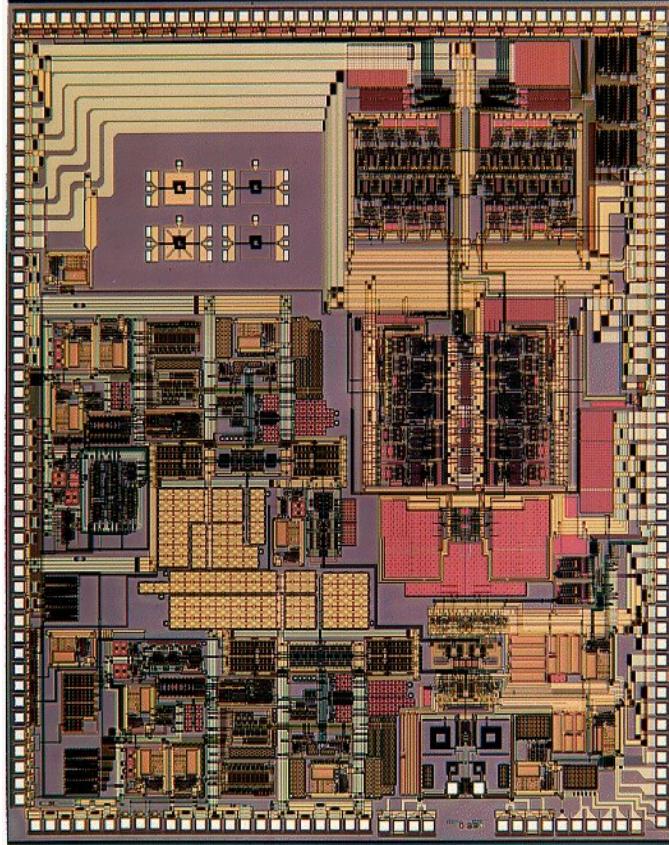
- Electronic Abstraction Level Design
- Integrated Circuit Design Styles
- Design Methodologies and Flows
- Cost-Performance Trade-off
- Field Programmable Gate Array
- Design Productivity
- Evolution of EDA Industry
- **How to map a system/algoritm to a System on Chip**

How to map a system/algoritm to hw/sw design



System on a Chip: GSM System

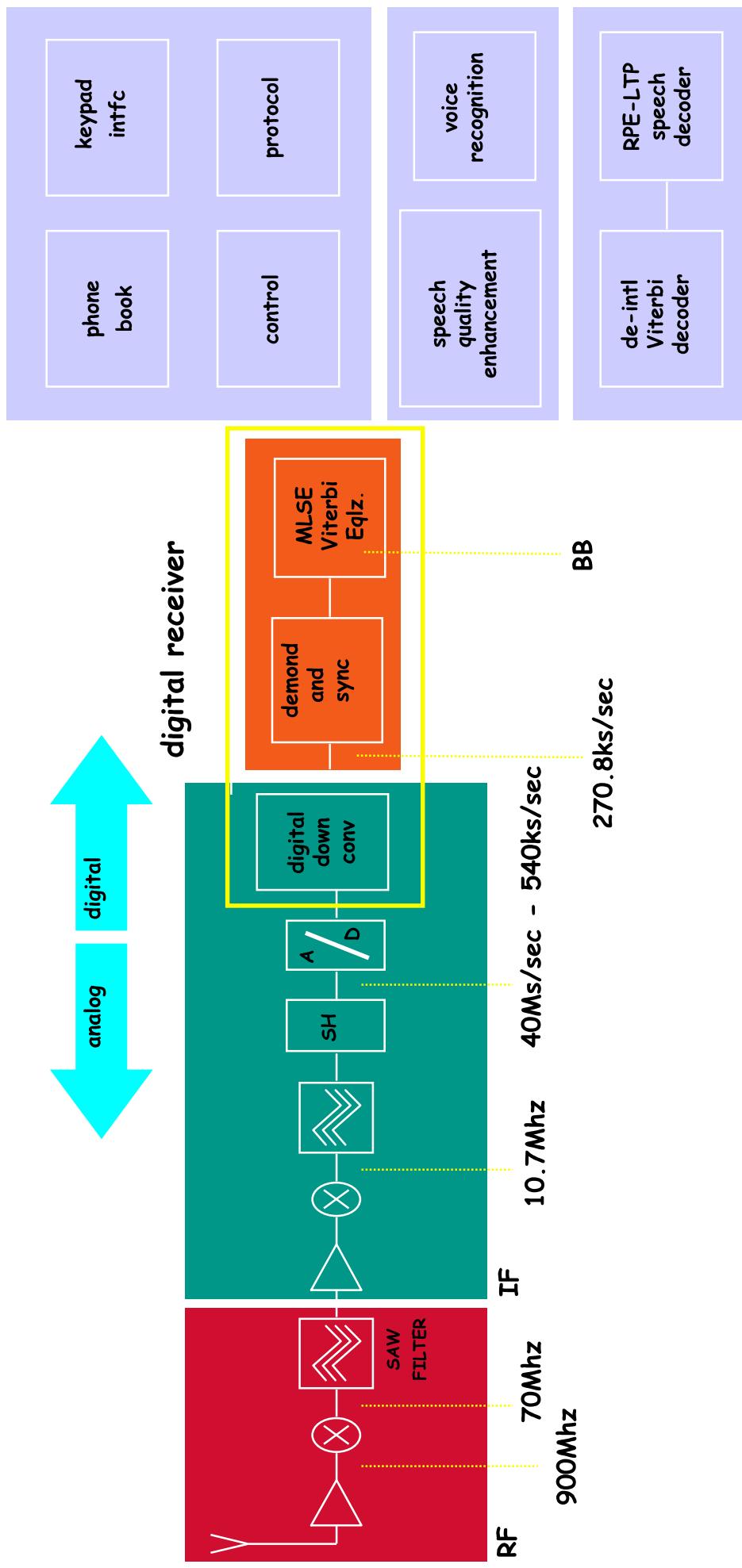
Source:
BWRC



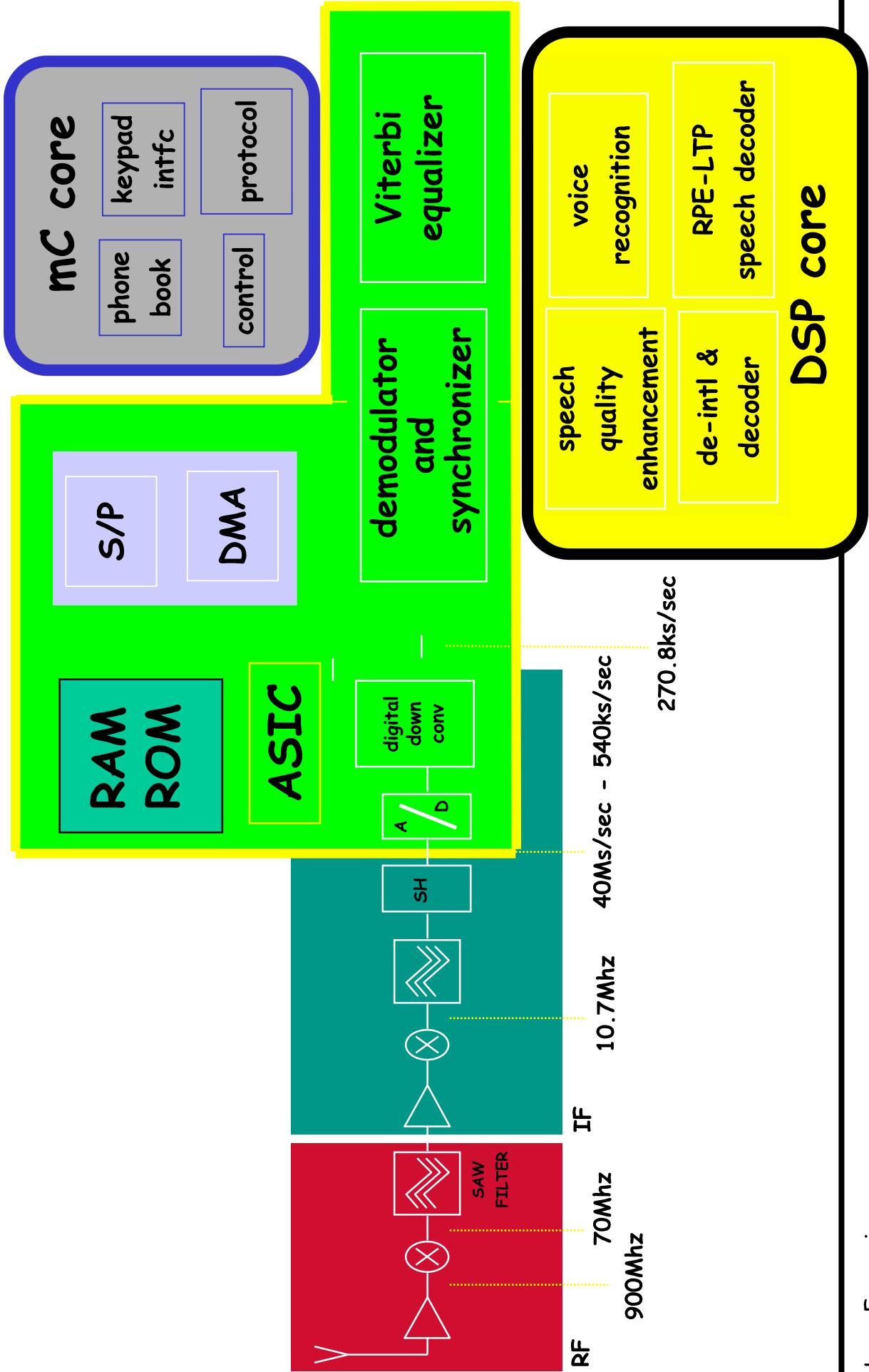
Research into technology and
design methodologies for
CMOS single chip radios

Conventional cellular
phone solution

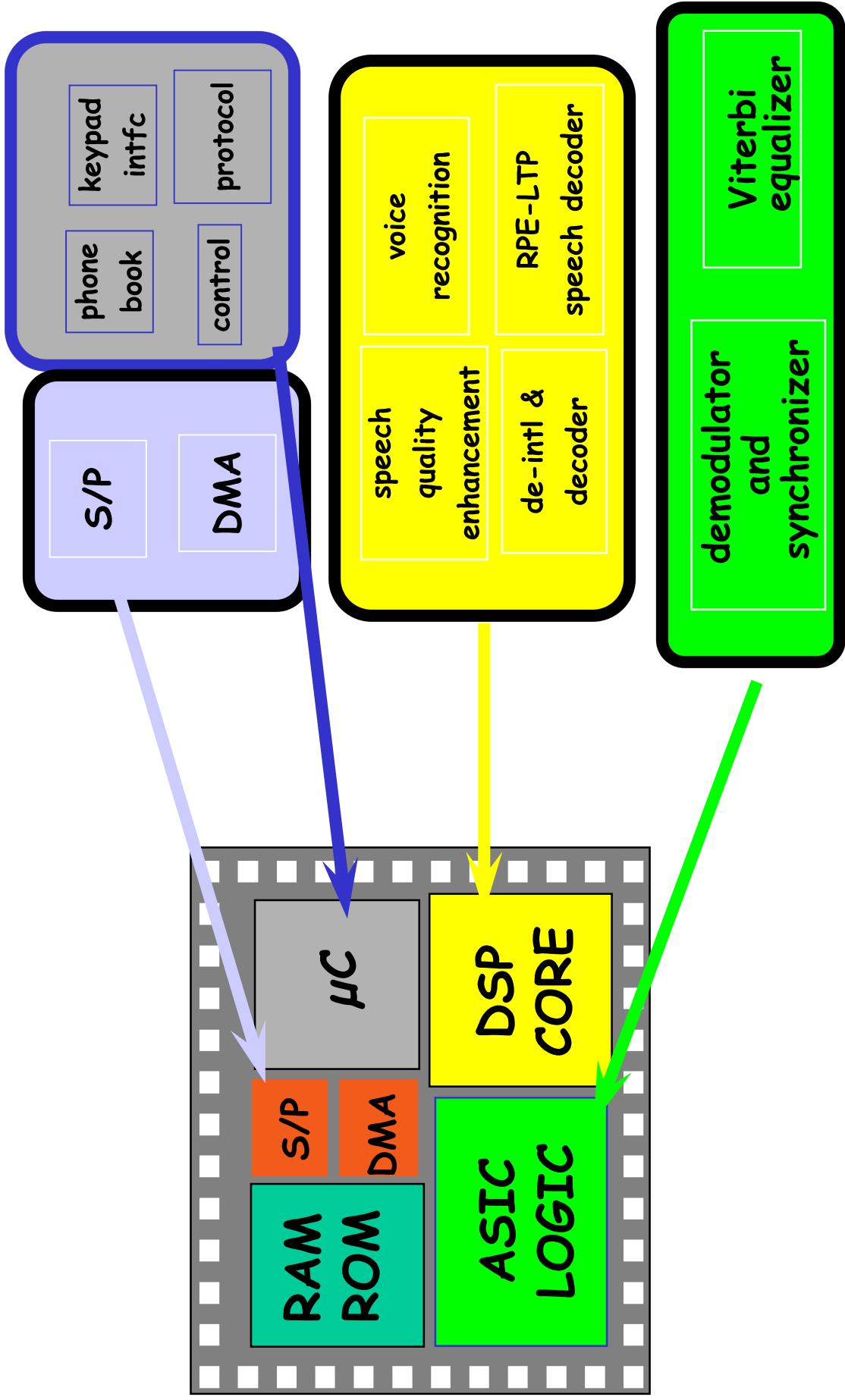
System level Modeling



Targeting an IC Implementation

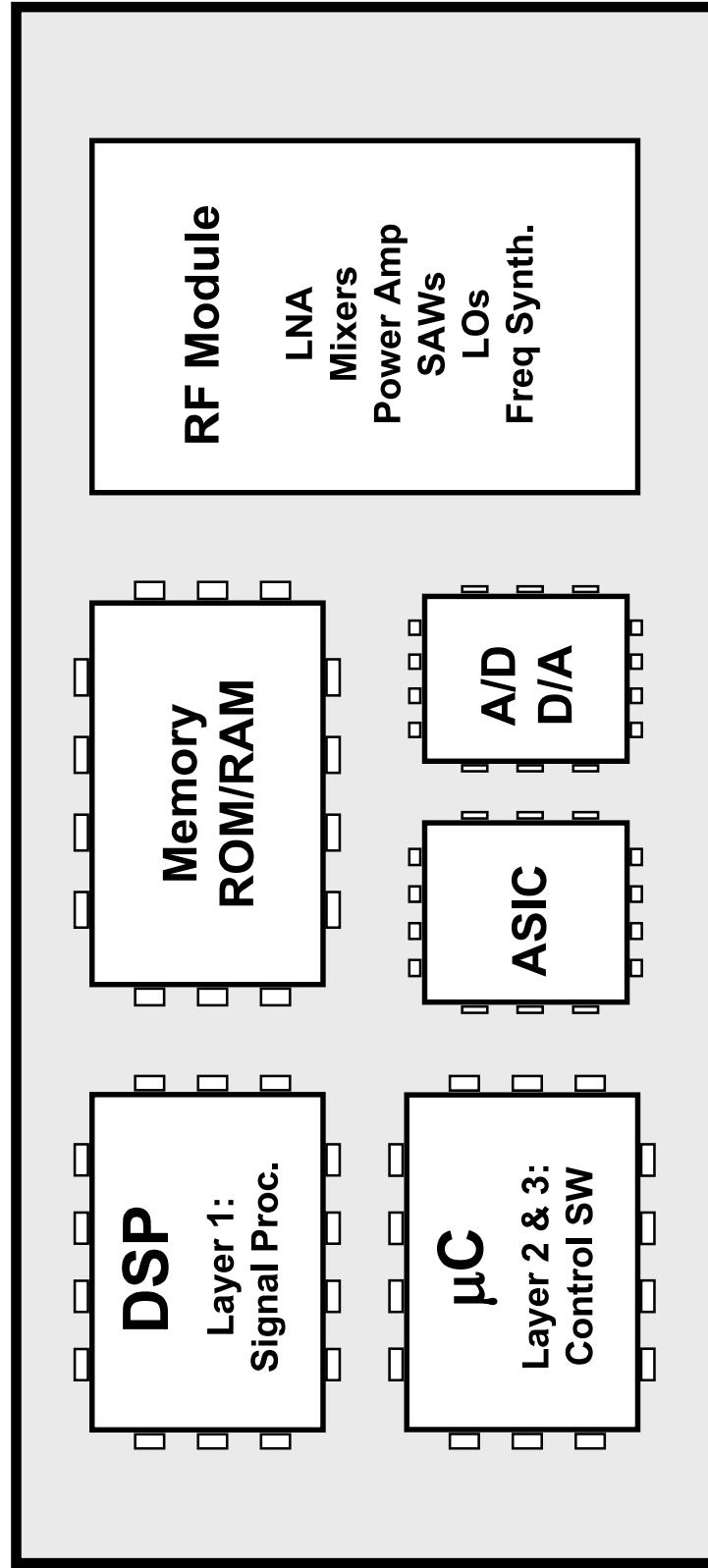


Mapping onto a system on a chip



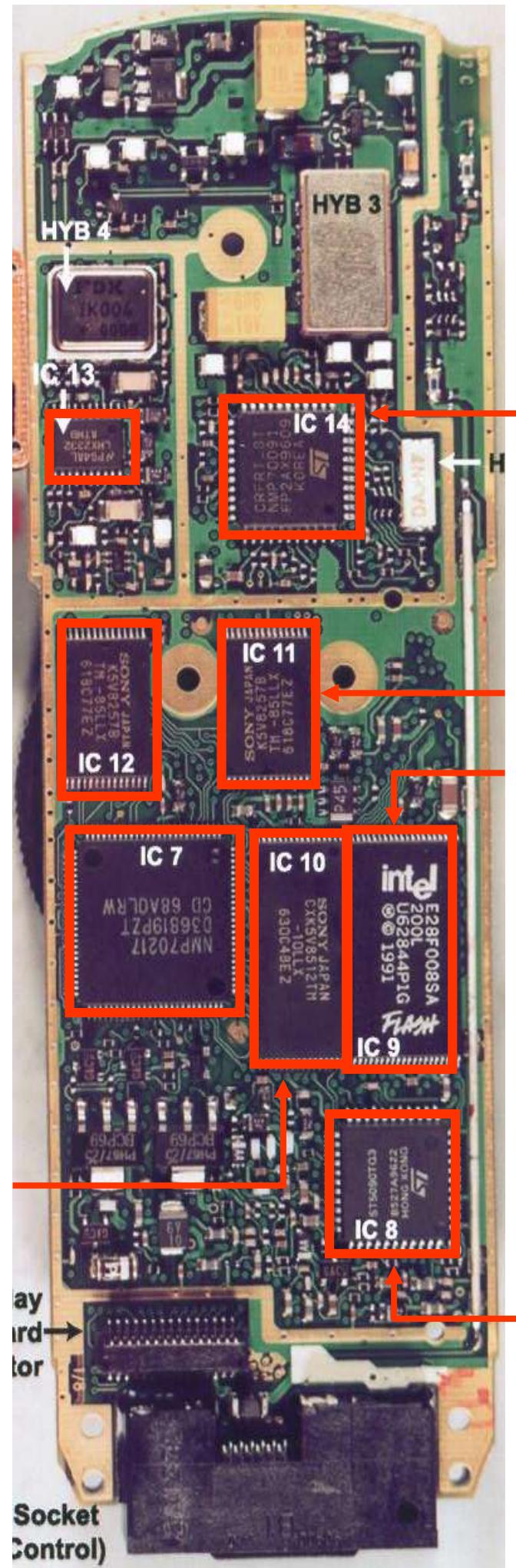
GSM Receiver Implementation (2/3)

DSP - centric Solution



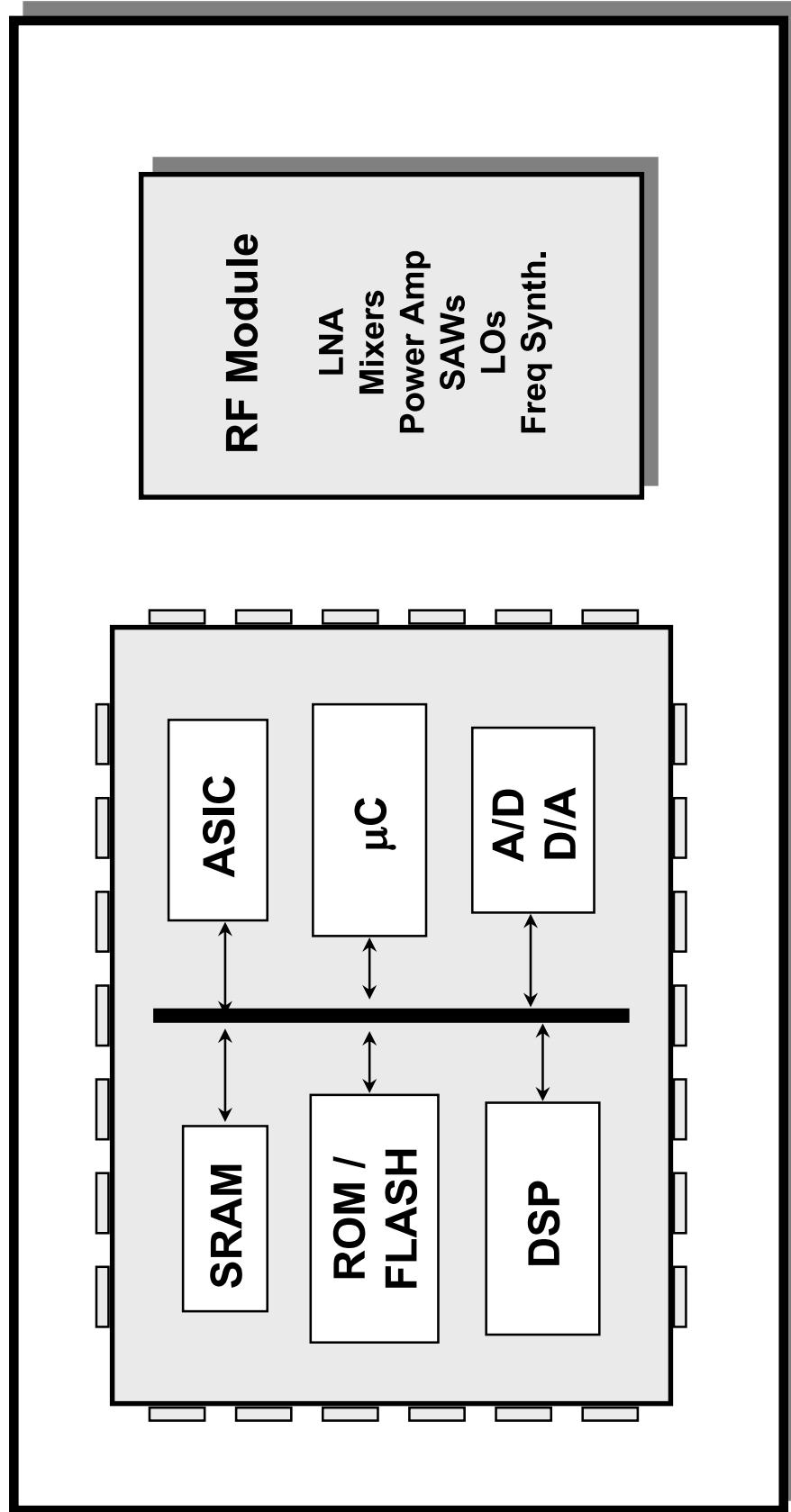
GSM Receiver Implementation (3/3)

RAM DSP RAM Frequency Synthesizer

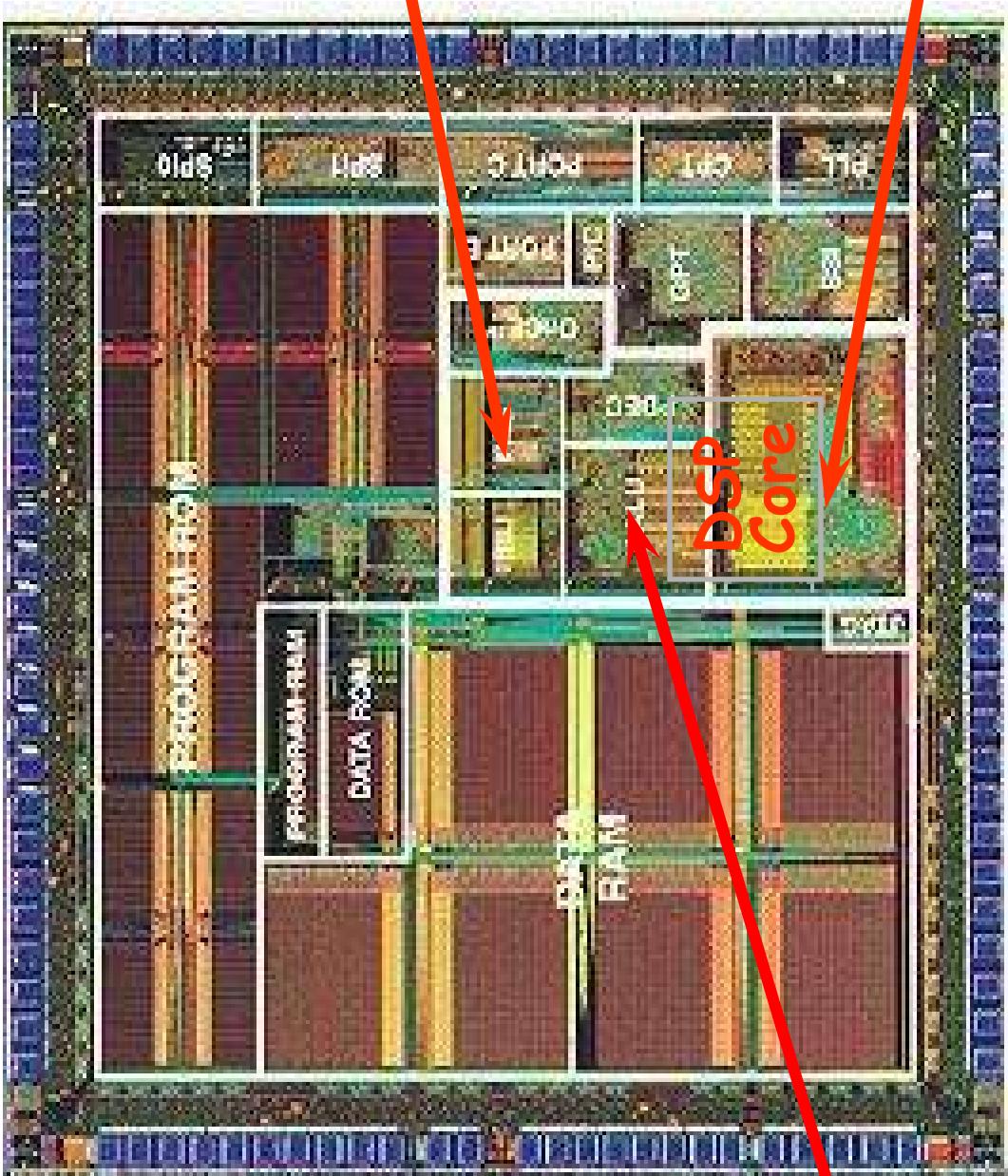


ROM RAM CODEC RAM ROM ASIC

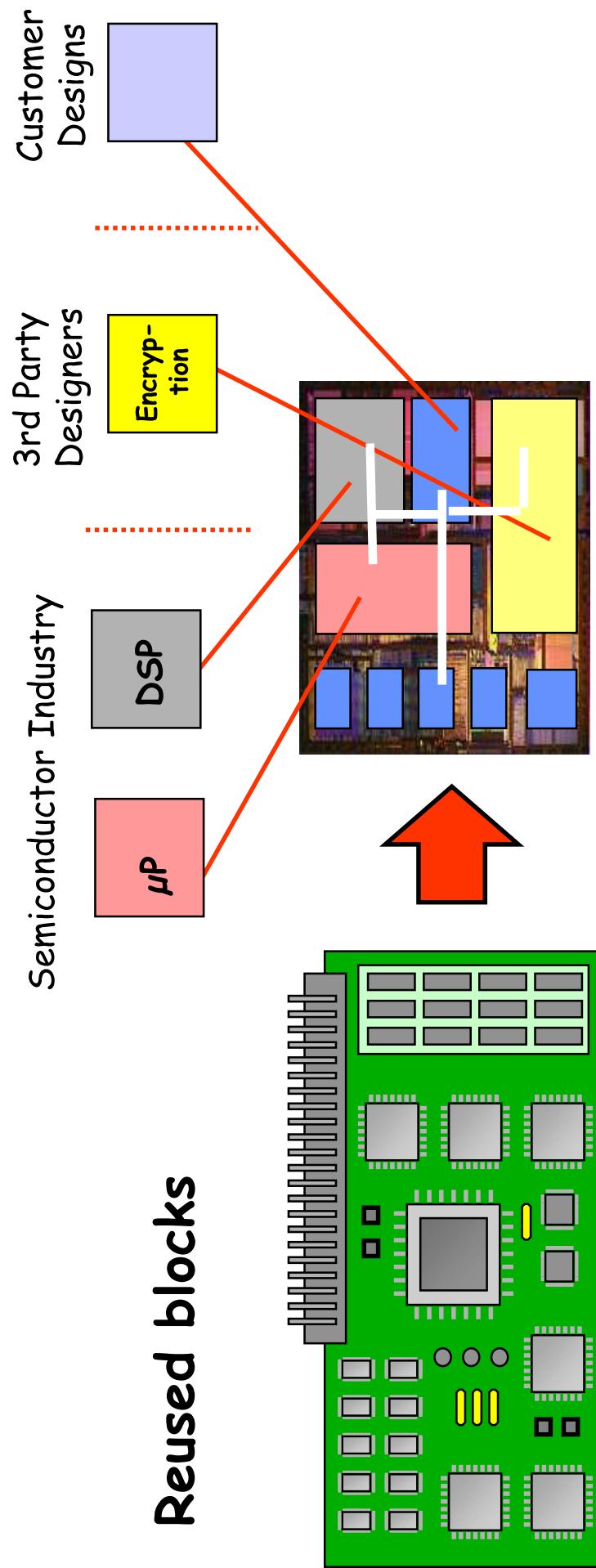
GSM SoC Receiver (1/2)



GSM Soc Receiver (2/2)



Re-useable IP



Achieve required design productivity by assembling
re-useable blocks of *intellectual property (IP)*

Source: **BWRC**

Growing list of IP Blocks

- Video: **MPEG**, DVD, HDTV
 - Power PC core: **3.1mm²** in **0.35μ**
 - ARM Core: **3.8 mm²** in **0.35μ**
- Audio: **MP3**, voice recognition
- Processors: **CPUs**, **DSPs**, Java
- Networking: **ATM**, **Ethernet**,
ISDN, **FibreChannel**, **SONET**
- Bus: **PCI**, **USB**, **IEEE 1394**
- Memory: **SRAM**, **ROM**, **CAM**
- Wireless: **CDMA**, **TDMA**
- Communication: **modems**, **transceivers**
 - Coding: speech, Viterbi, Reed-Solomon
 - Display drivers/controllers: TFT
- Other: **sensors**, **encryption/decryption**, **GPS**

Re-useable IP: Limiting factors

- Company Culture: from design for *one use* to design for *multiple reuse*.
 - Legal Protection
 - Contract Delays
 - IP/VC Availability
 - IP/VC Quality
 - Mix & Match
-
- The diagram consists of three orange arrows. One arrow points upwards from the 'IP/VC Availability' item to the text 'Virtual Component Exchange'. Another arrow points upwards from the 'IP/VC Quality' item to the same text. A third arrow points downwards from the 'Mix & Match' item to the text 'to organize a marketplace for the buying and selling of semiconductor IP/VC.'
- Virtual Component Exchange**
to organize a marketplace
for the buying and selling
of semiconductor IP/VC.

Virtual Socket Interface Alliance (VSIa) addresses the mix and match of IP/VC facilitating reuse for SoC designs. From 1996 to 2008 (<http://www.vsi.org/>).

Now refers to the Spirit Consortium (<http://www.spiritconsortium.org>)



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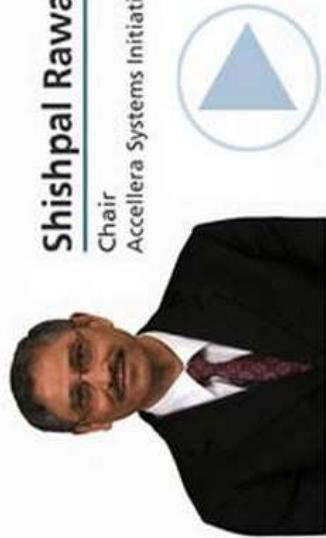
About Us

Who We Are

Accellera Systems Initiative is an independent, not-for-profit organization dedicated to create, support, promote, and advance system-level design, modeling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other "smart" electronic devices. Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission

Shishpal Rawat
Chair
Accellera Systems Initiative



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Accellera Systems Initiative Chair gives an update on
Accellera activities at DAC 2014.

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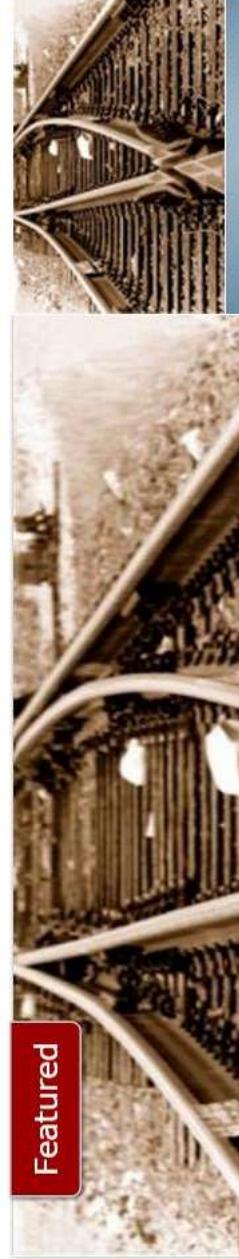
Silicon IP Verification IP Highlight

**12,000 IP Cores
from 400 Vendors**

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► You need more than an IP ?

Featured



synopsys®
Digital PLL 0.1-2 Ghz
TSMC40LP



Motion-adaptive Video
Deinterlacer

DVB-T2 Modulator

flexlogix
FPGA core in TSMC 28HPM

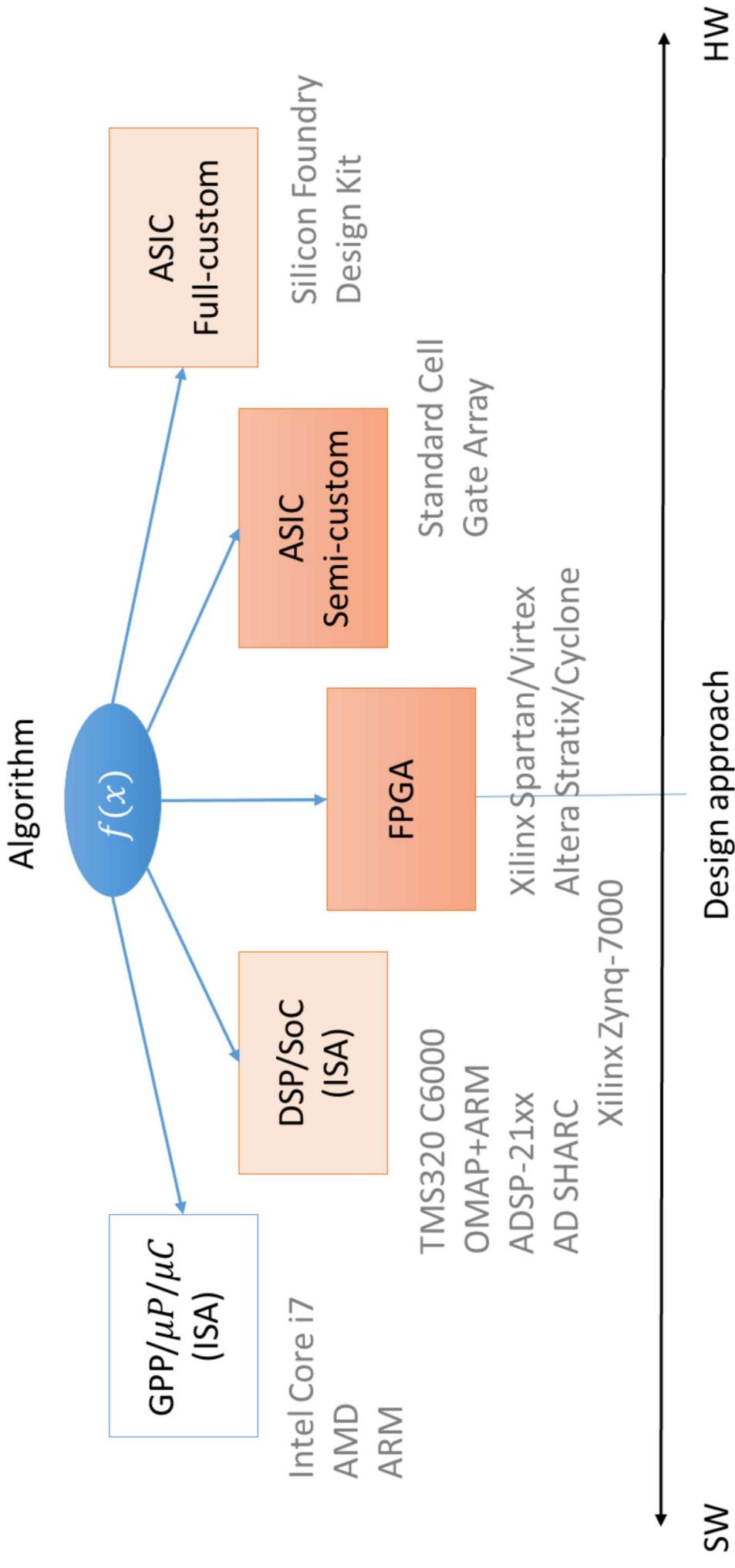
M....mpg
min. ri...

► Mostra tutti !

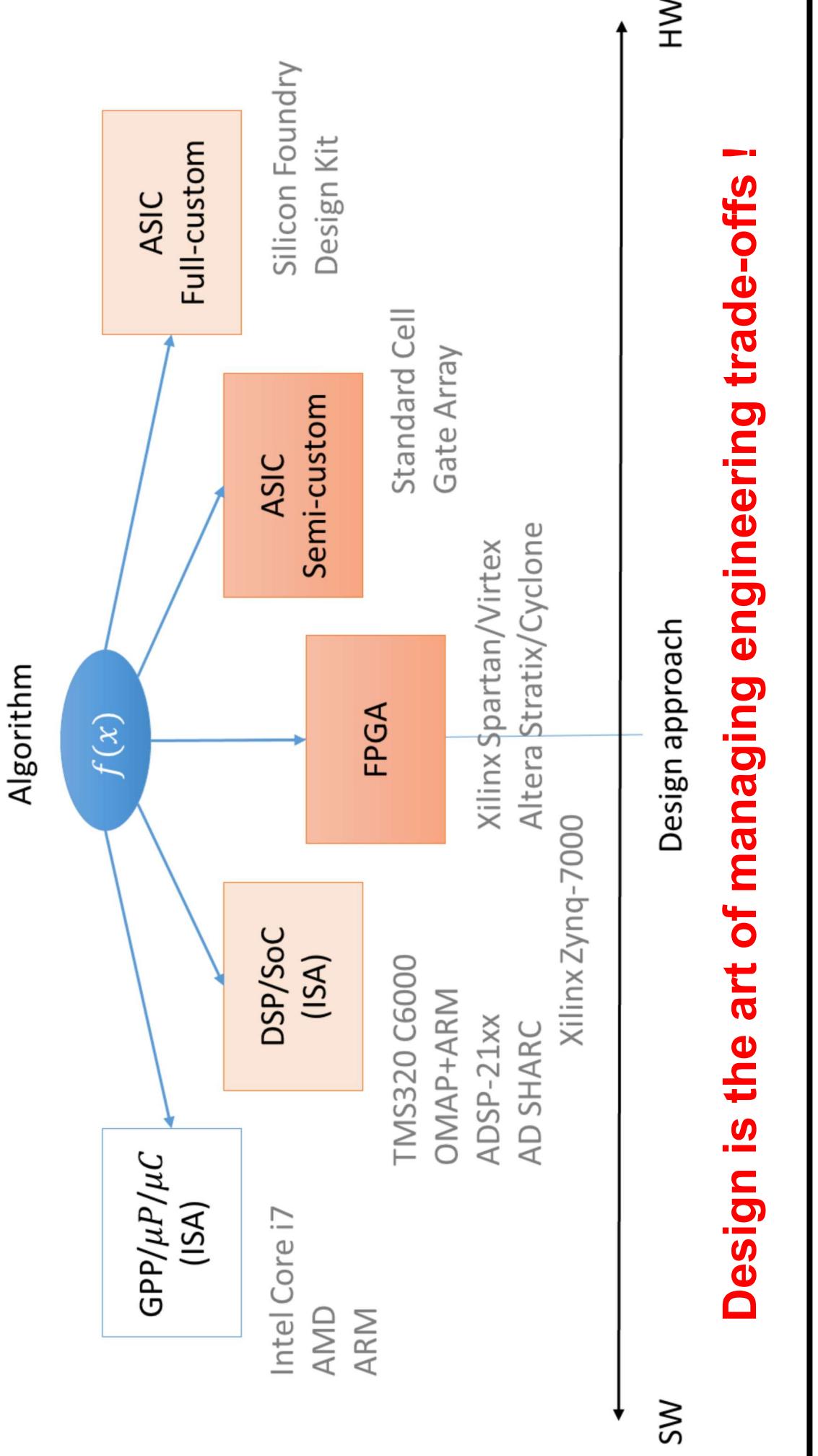
Requirements for re-use

- In order to be re-usable, I.P.'s must be properly validated:
 - Documented
 - Compliant with design tools
 - Fully debugged
 - Testable
 - Manufacturable
 - Possibly verified on silicon
- Re-use in place of re-development can reduce costs, but:
 - There is an additional cost in making the IP re-usable
 - Who pays the cost is not always the same who profits from re-use
- An I.P. risks being obsolete before is completely validated
- Two main trends:
 - Design blocks for re-use (e.g. ARM)
 - High level I.P.'s (algorithms, software blocks, synthesizable blocks have a better chance to pay their cost

How to map a system/algoritm to hw/sw design

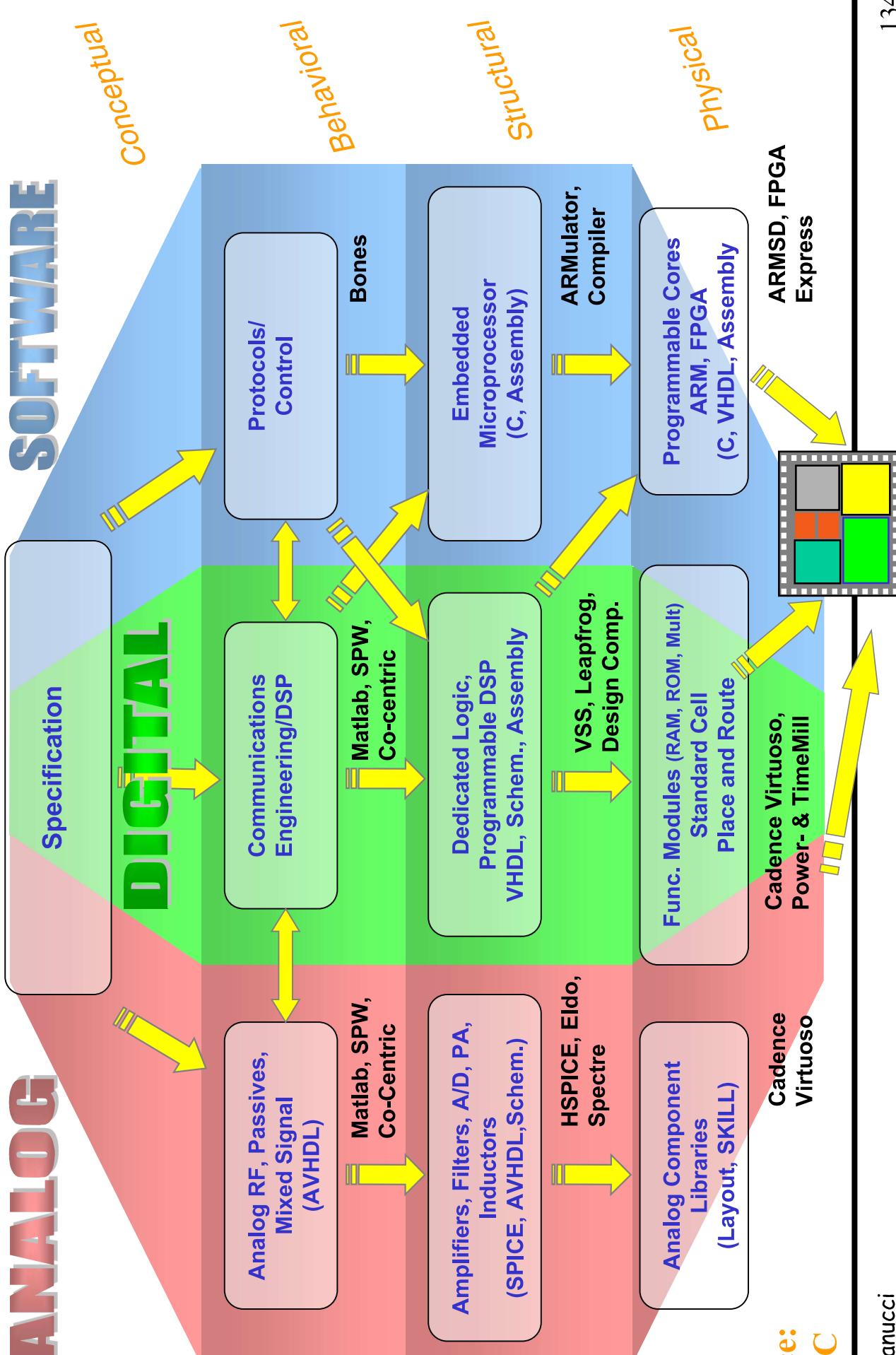


How to map a system/algoritm to hw/sw design



Design is the art of managing engineering trade-offs !

System on a Chip: Design Flow Example



Source:
BWRC

Luca Fanucci

Summary

- The capabilities of CMOS technology have now reached a threshold which allows System Level Integration
- The development of proper design methodology and CAD tools are fundamental for future System On a Chip :
 - Efficient management of design complexity
 - Reduced design cycle (time to market)
 - Efficient exploration of the solution space
 - Re-usability of whole designs or part of them
 - Technology independence

End, Questions ?

- Electronic Abstraction Level Design
- Integrated Circuit Design Styles
- Design Methodologies and Flows
- Cost-Performance Trade-off
- Field Programmable Gate Array
- Design Productivity
- Evolution of EDA Industry
- How to map a system/algorithim to a System on Chip

