

Electronics and Communication Systems

Electronics Systems

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Outline

- ❖ CMOS Logic
 - Static Logic (hard node)
 - Dynamic Logic (soft node)
- ❖ Example: NAND4 Area-Speed trade-off

Hard-Node (Static Logic)

- ❖ **Have positive feedback (regeneration) with an internal connection between the output and the input. Storage is performed through circuit topology**
- ❖ **Preserve state as long as the power is on**
- ❖ **Useful when updates are infrequent**

Soft Node (Dynamic Logic)

- ❖ **Store state on parasitic capacitors**
- ❖ **Only hold state for short periods of time**
- ❖ **Require periodic refresh**
- ❖ **Usually simpler, so higher speed and lower power**

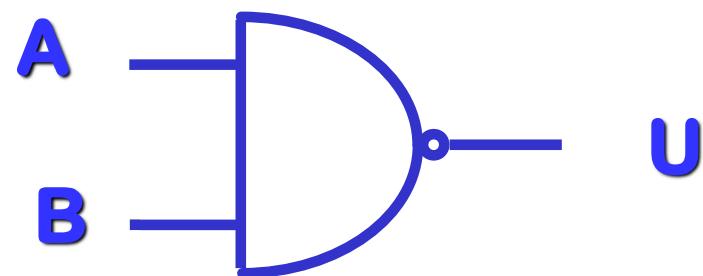
NAND

Truth Table

A	B	U
0	0	1
0	1	1
1	0	1
1	1	0

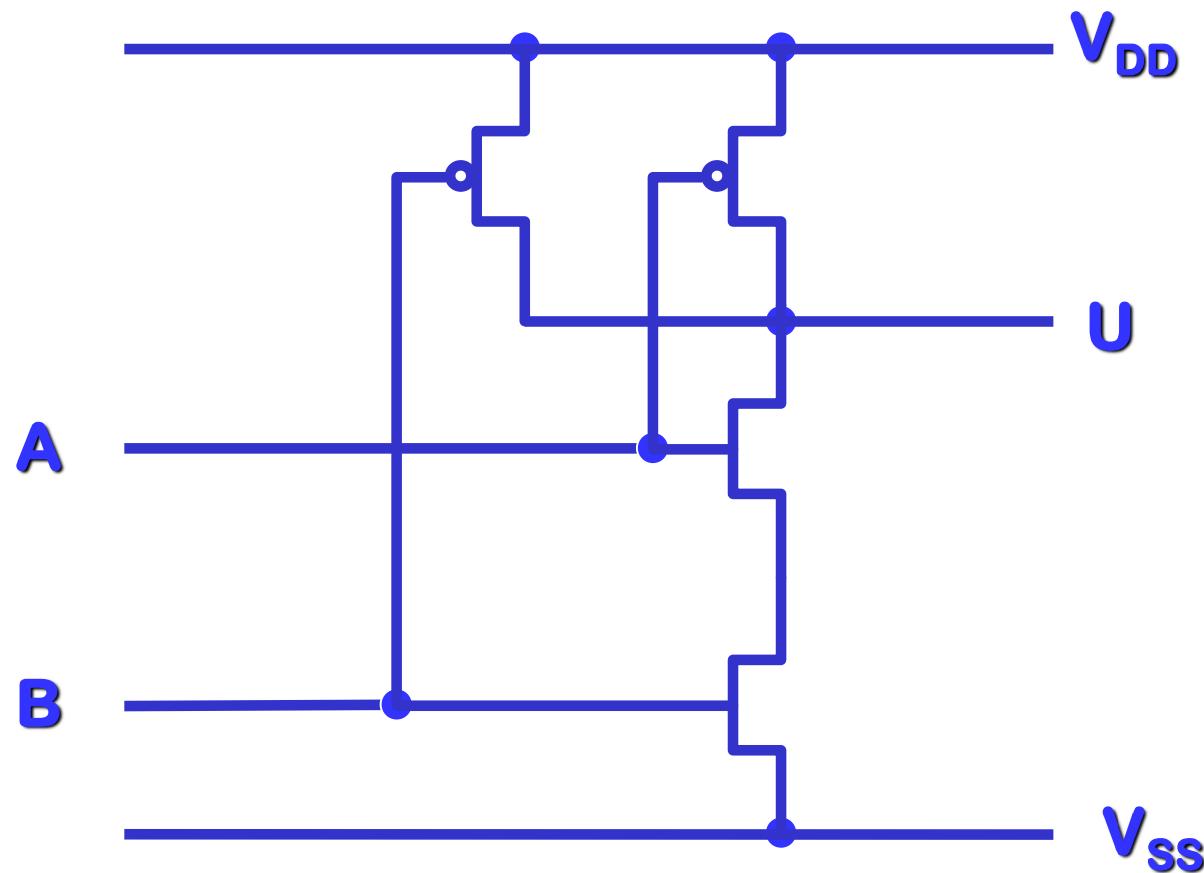
Logic Symbol

$$U = \overline{A * B}$$



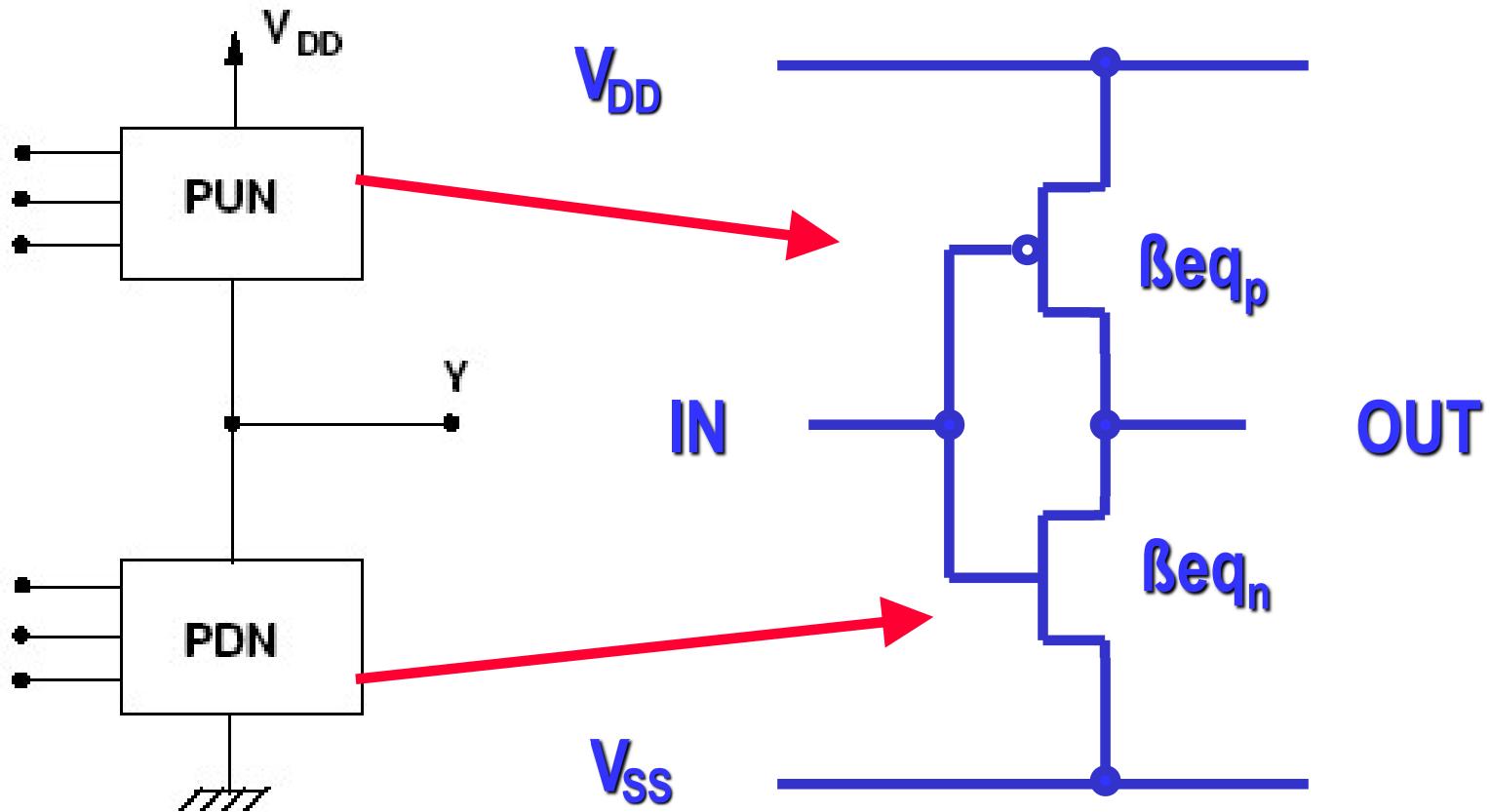
CMOS Implementation

✧ Electric Circuit



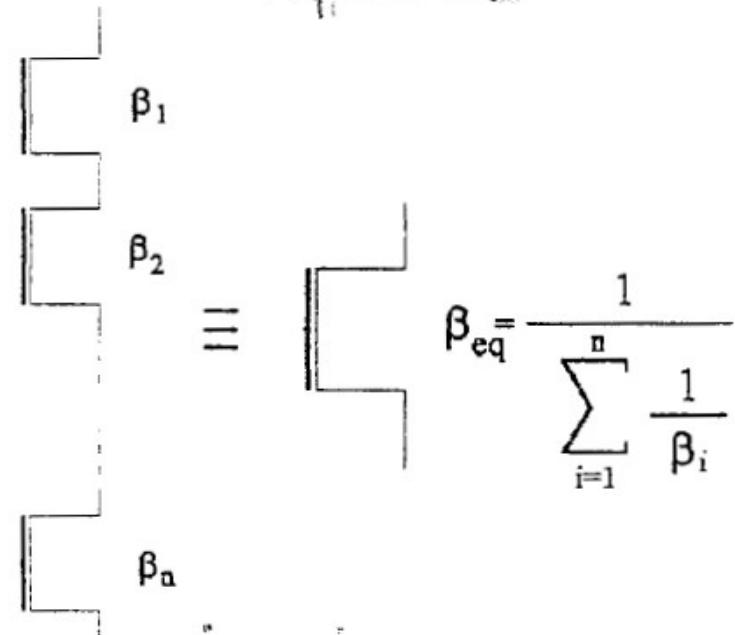
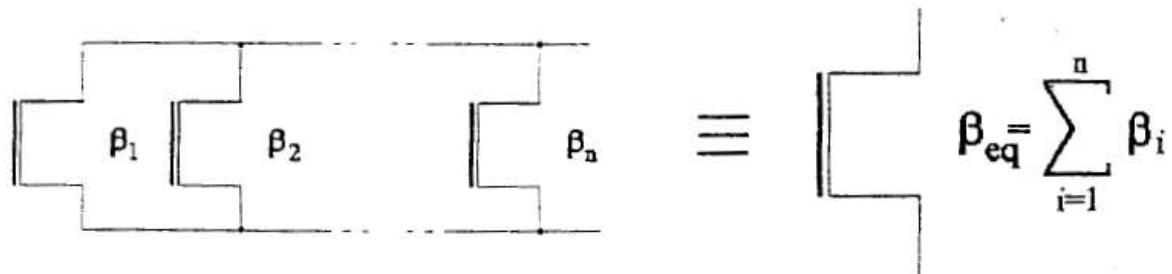
Dynamic A

$$t_{pHL} \propto \frac{KC}{\beta_n} \frac{1}{V_{DD} - V_{Tn}}$$

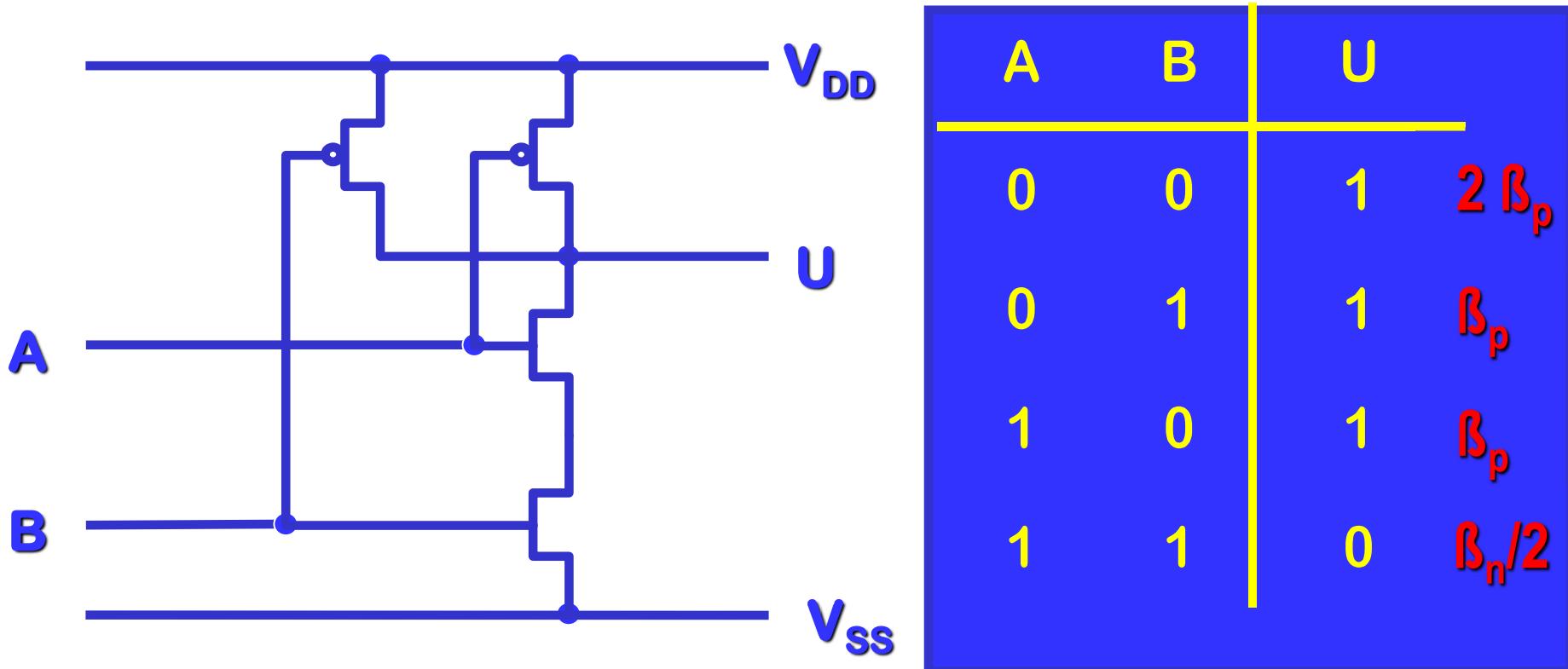


$$t_{pLH} \propto \frac{KC}{\beta_p} \frac{1}{V_{DD} + V_{Tp}}$$

Dynamic Analysis



Dynamic Analysis



$$t_{pLH} \propto \frac{KC}{\beta_{eqp}} = \frac{KC}{\beta_p}$$

$$t_{pHL} \propto \frac{KC}{\beta_{eqn}} = \frac{2KC}{\beta_n}$$

Dynamic Analysis

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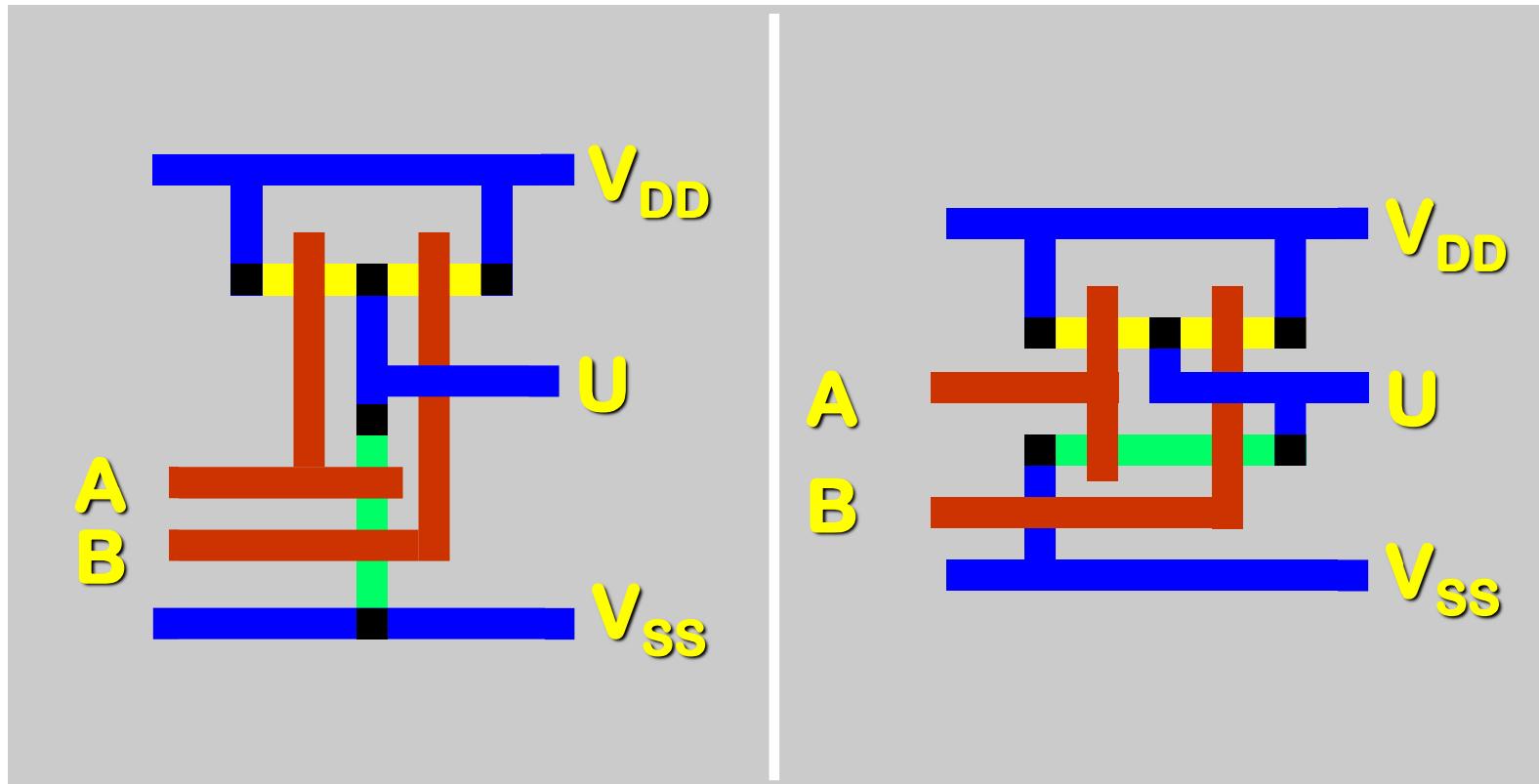
✧ **tp_{HL} = tp_{LH} in the worst case**

$$\beta_p = \frac{\beta_n}{2} \rightarrow \beta_n = 2\beta_p \rightarrow \mu_n \frac{W_n}{L_n} = 2\mu_p \frac{W_p}{L_p}$$

If $\mu_p = \frac{\mu_n}{2}$ $L_n = L_p = L_{\min}$ \longrightarrow $W_n = W_p$

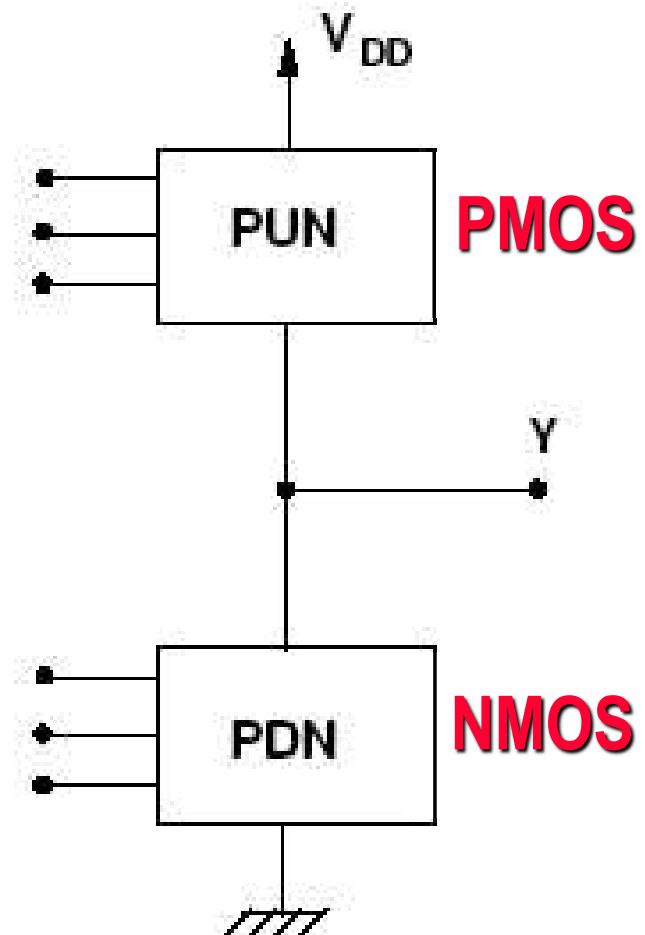
Stick Diagram

❖ Different topological solutions



Complementary CMOS

- ❖ Static Logic
- ❖ No Threshold Drop
- ❖ Maximum Noise Margin
- ❖ No Static Power Cons. (VDD-GND)
- ❖ Possible TR sizing for $tp_{HL} = tp_{LH}$
- ❖ Flexible Layout
- ❖ Transistor Complexity for a logic function with N input: **2 N MOS**

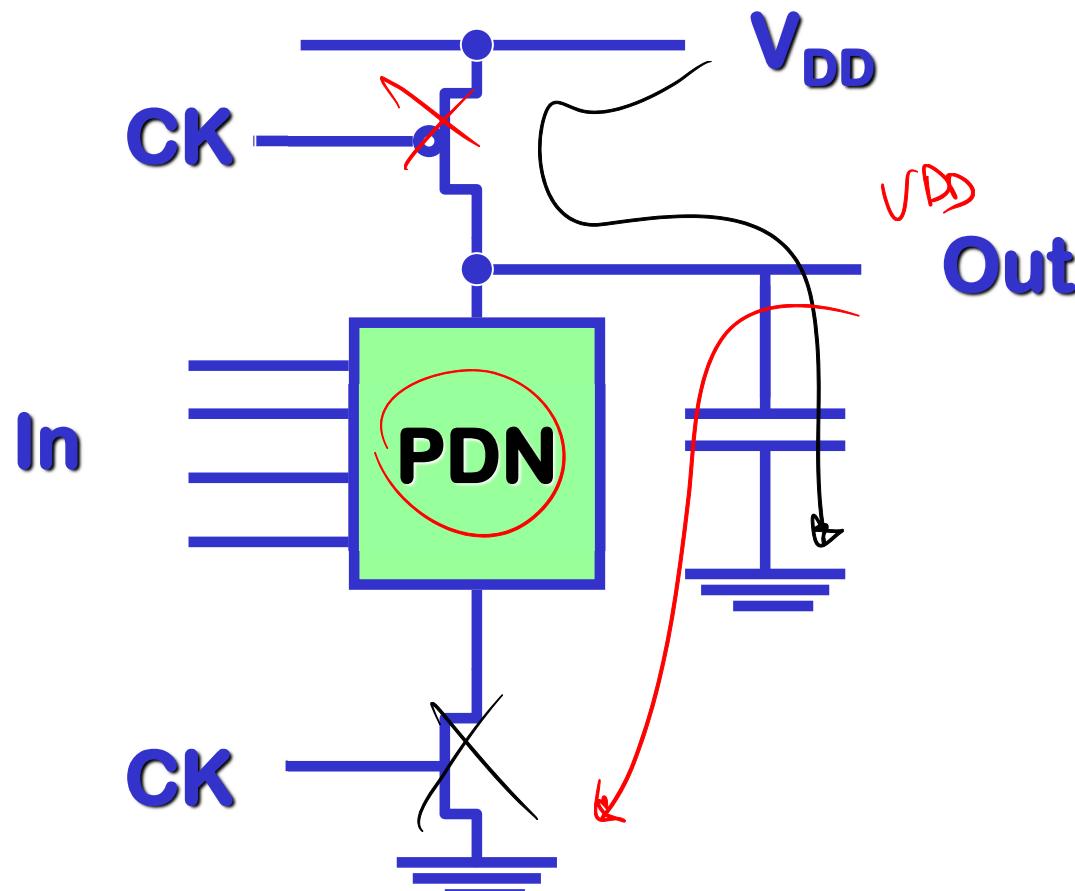


PDN and PUN are dual

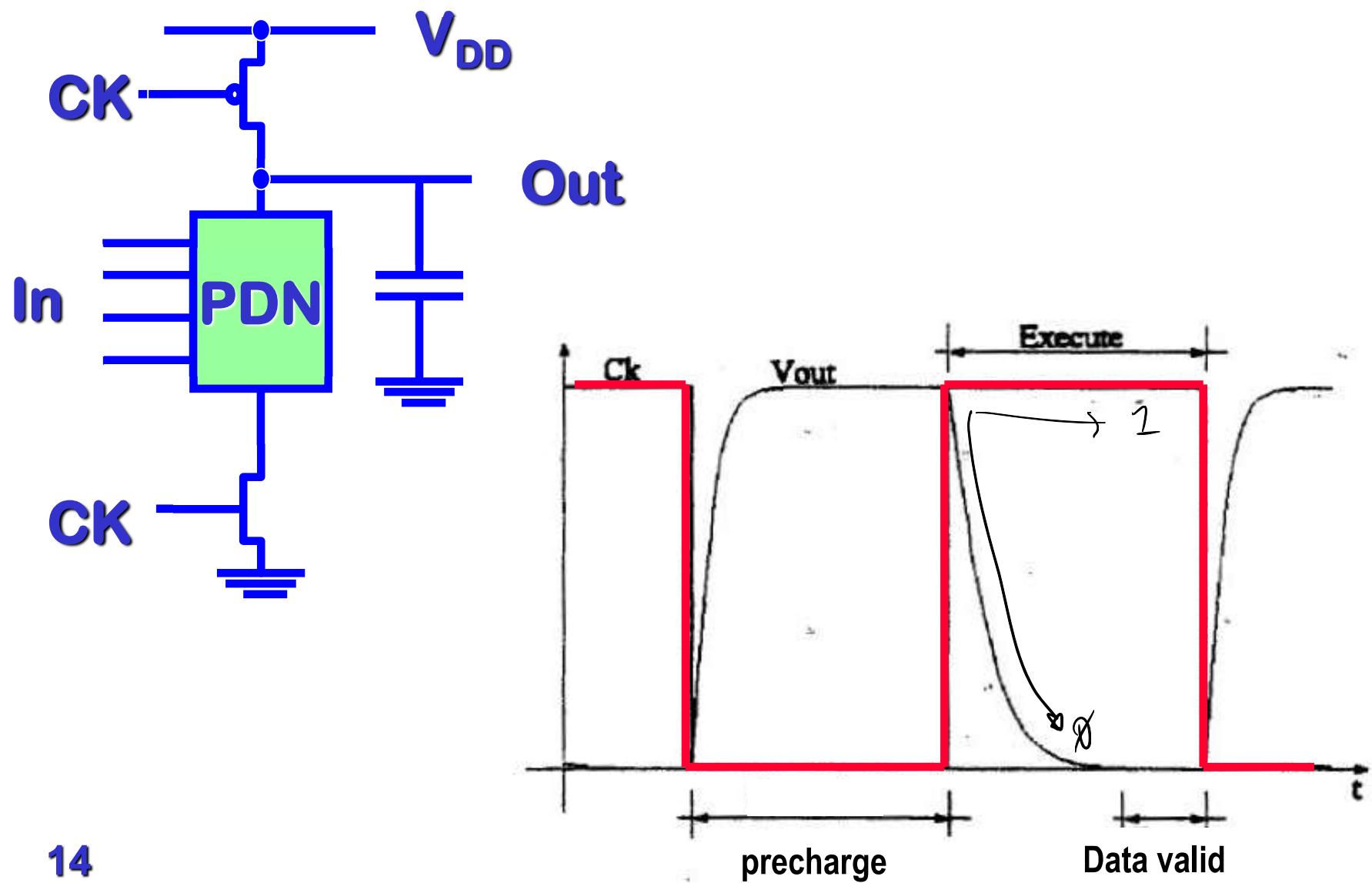
Dynamic Logic

$C_L = \emptyset$ "Präsentations"

$C_L = 2$



Dynamic Logic



Dynamic Logic

PRO

N MOS + 2

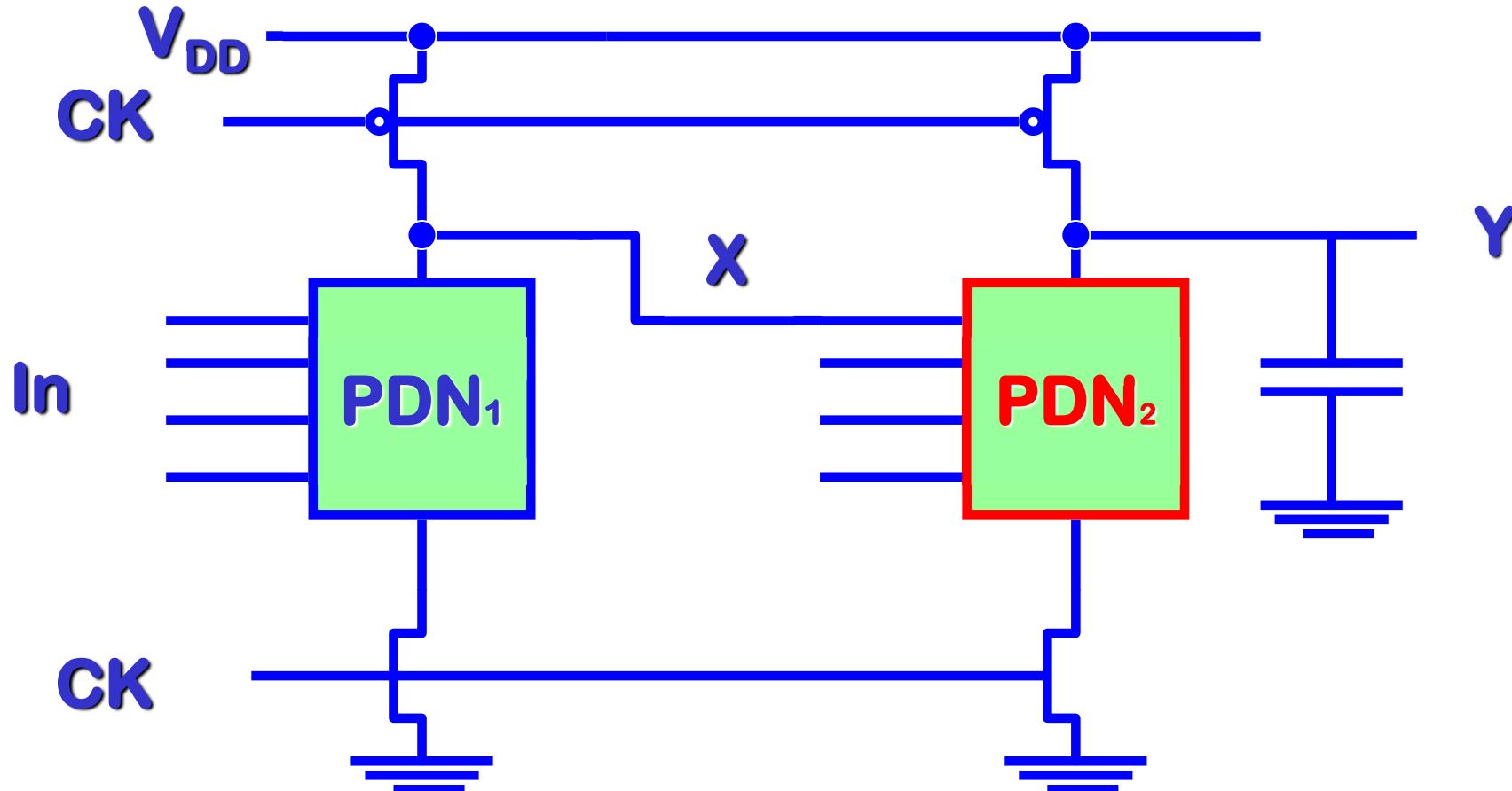
Reduced C_{in}

CONTRA

**Output is valid only for
 $CK=1$ (fraction of)
input have to be stable
when $CK=1$**

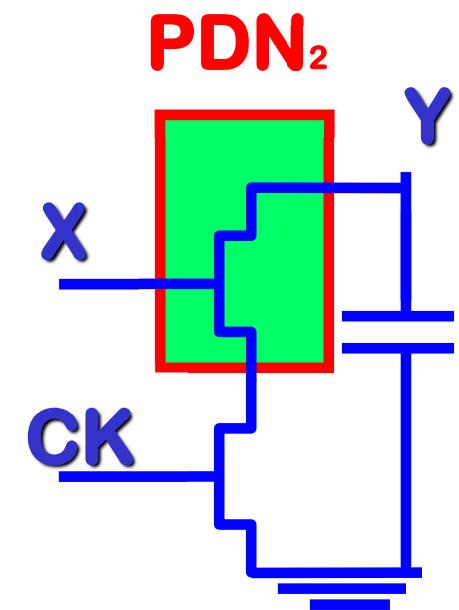
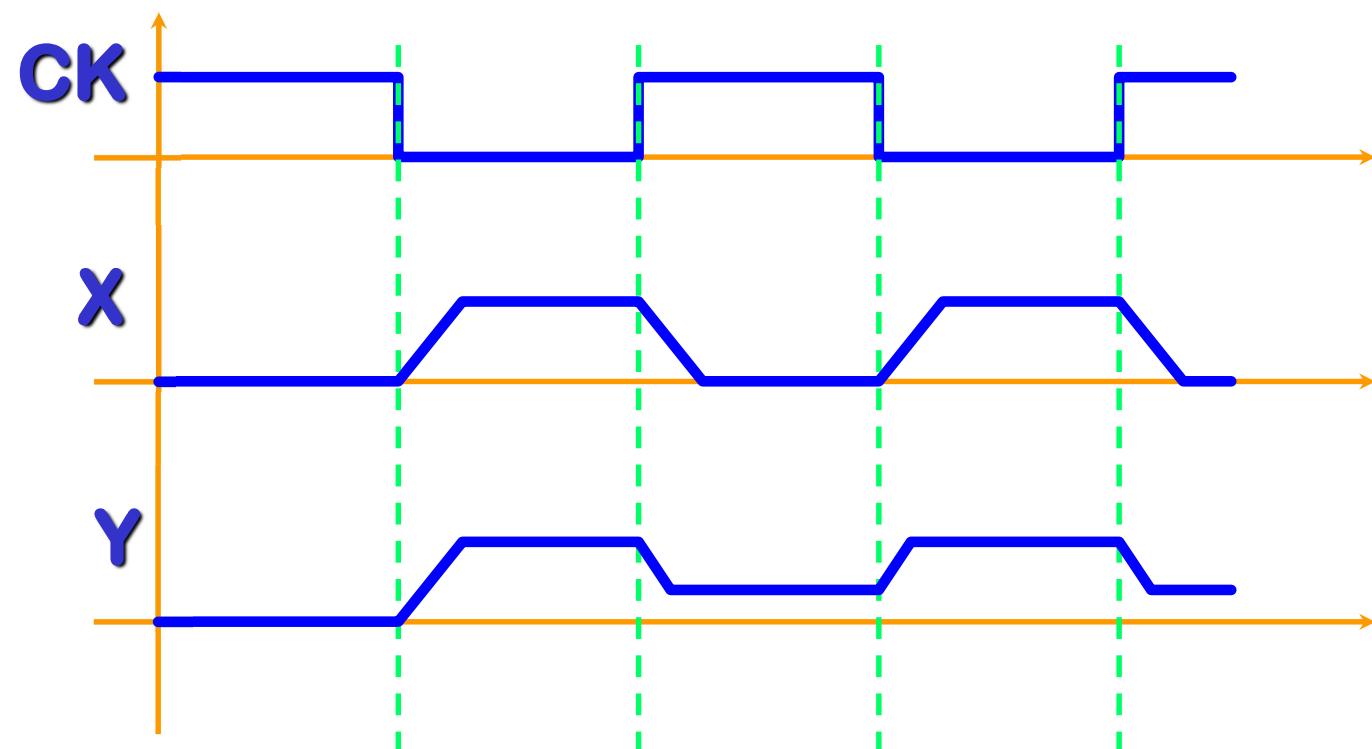
Cascaded of Dynamic Logic

❖ Descharge problem



Forme d'Onda

✿ Y state is not defined



Domino Logic

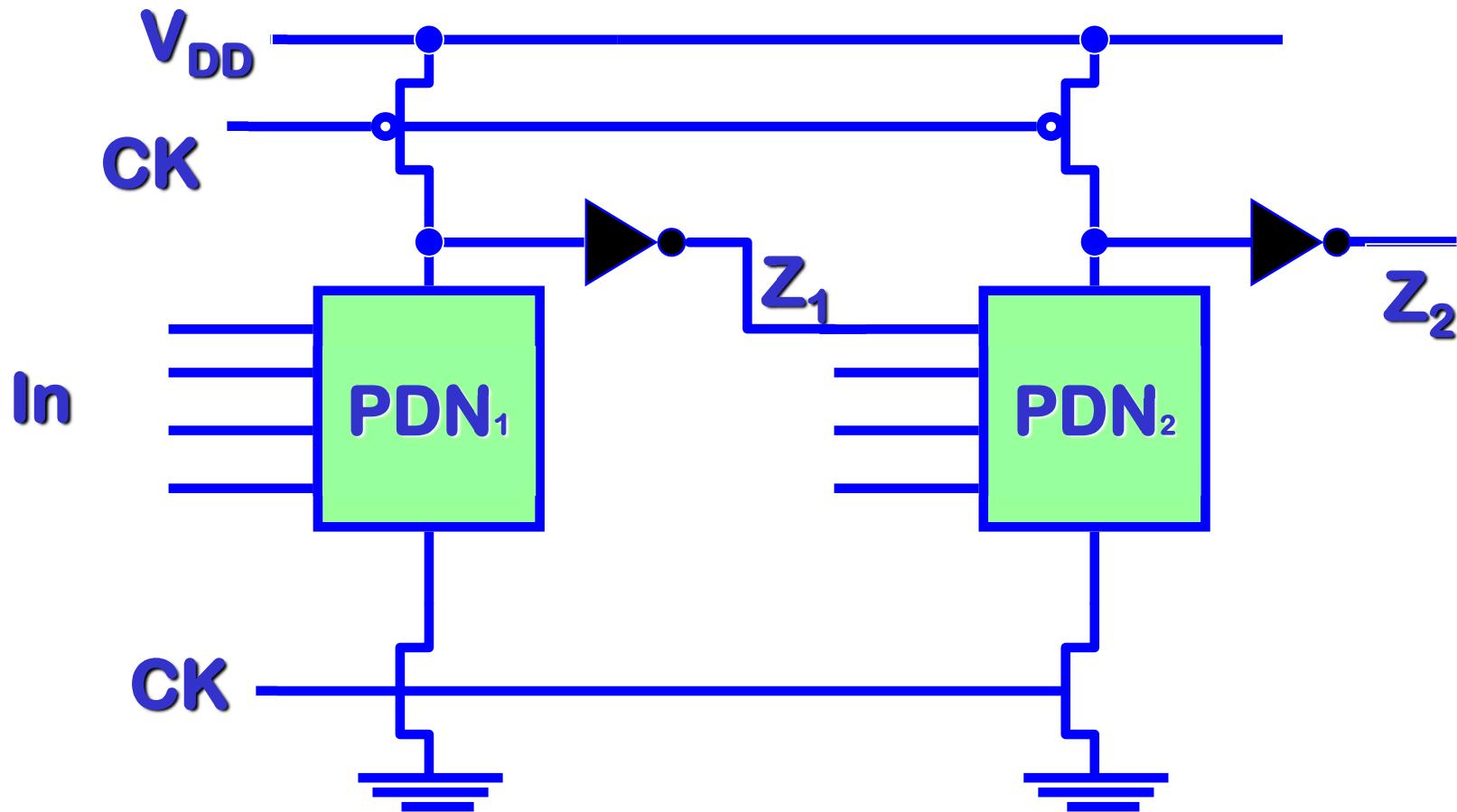
❖ Note

– Descharge is due to the precharge to “1”

❖ Solution

– precharge to “0”

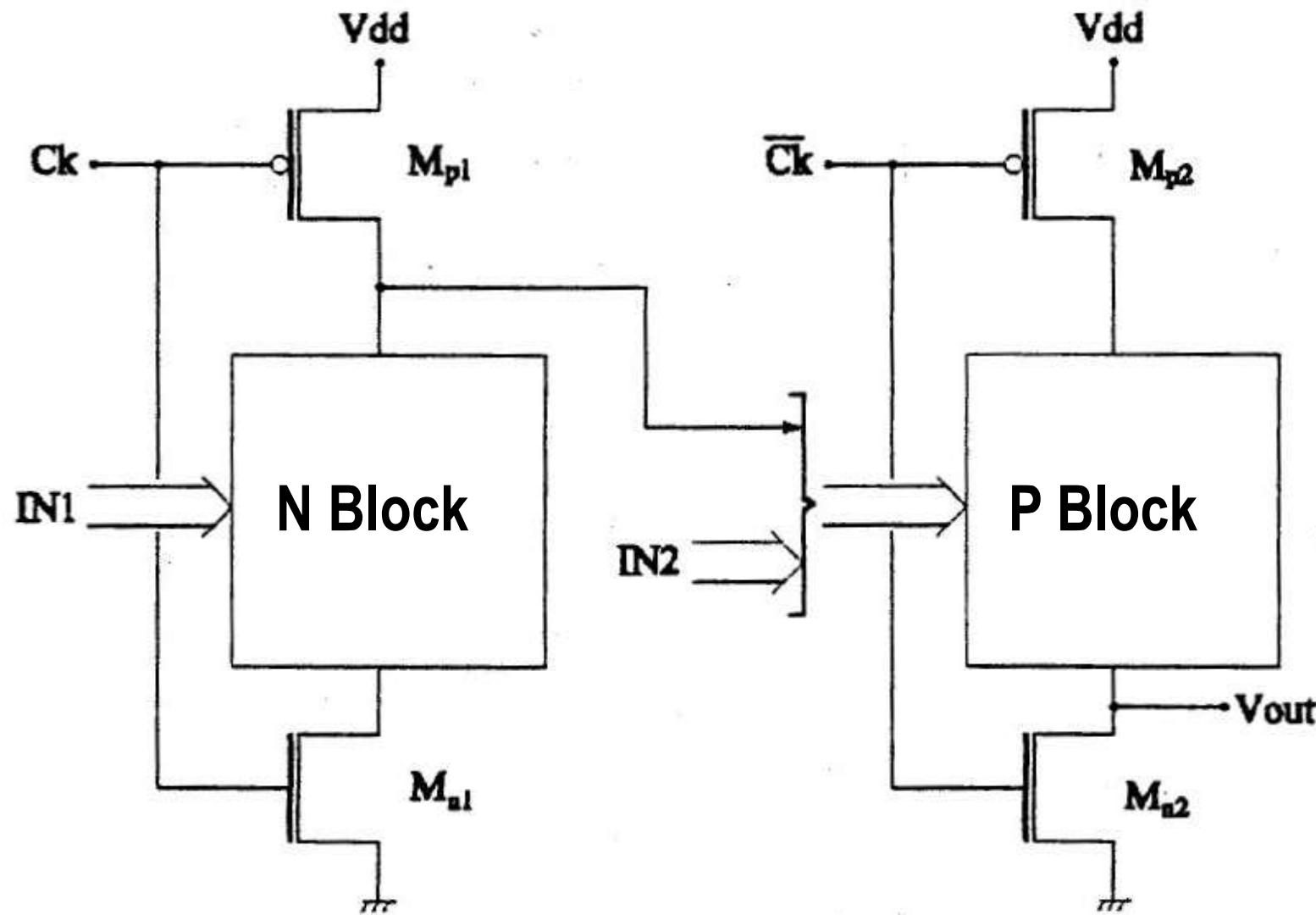
Domino Logic Scheme



Note on Domino Logic

- ❖ The name of Domino Logic derived from the fact that output “fall” one after the other as in the “DOMINO” game !!
- ❖ Negative Function cannot be implemented

Domino P-N

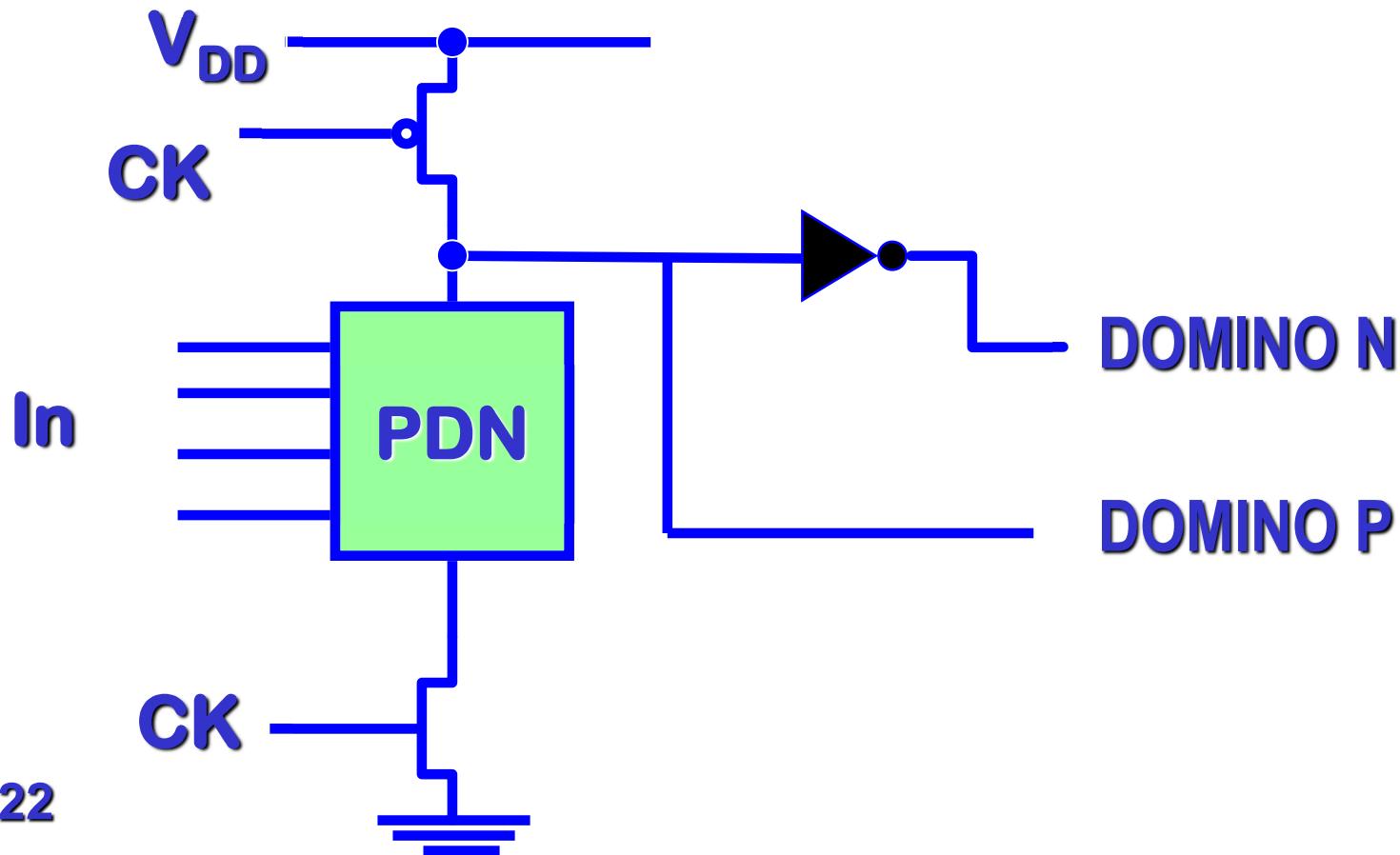


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Also negative function can be implemented

Domino P-N

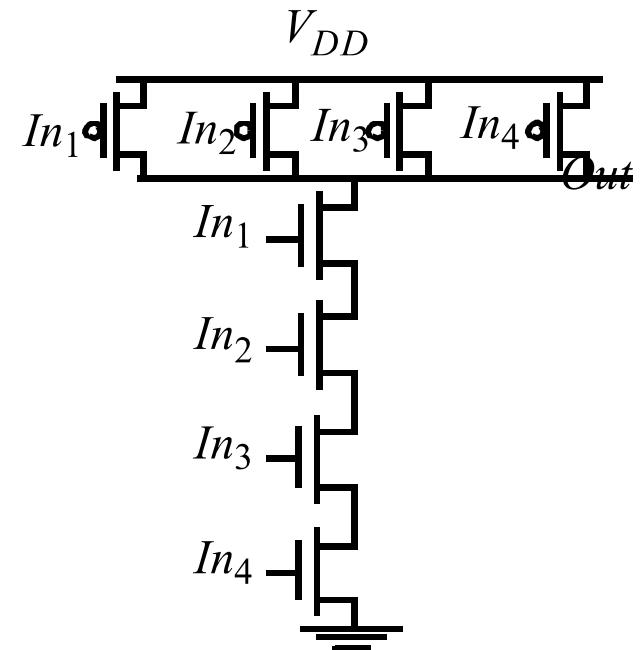
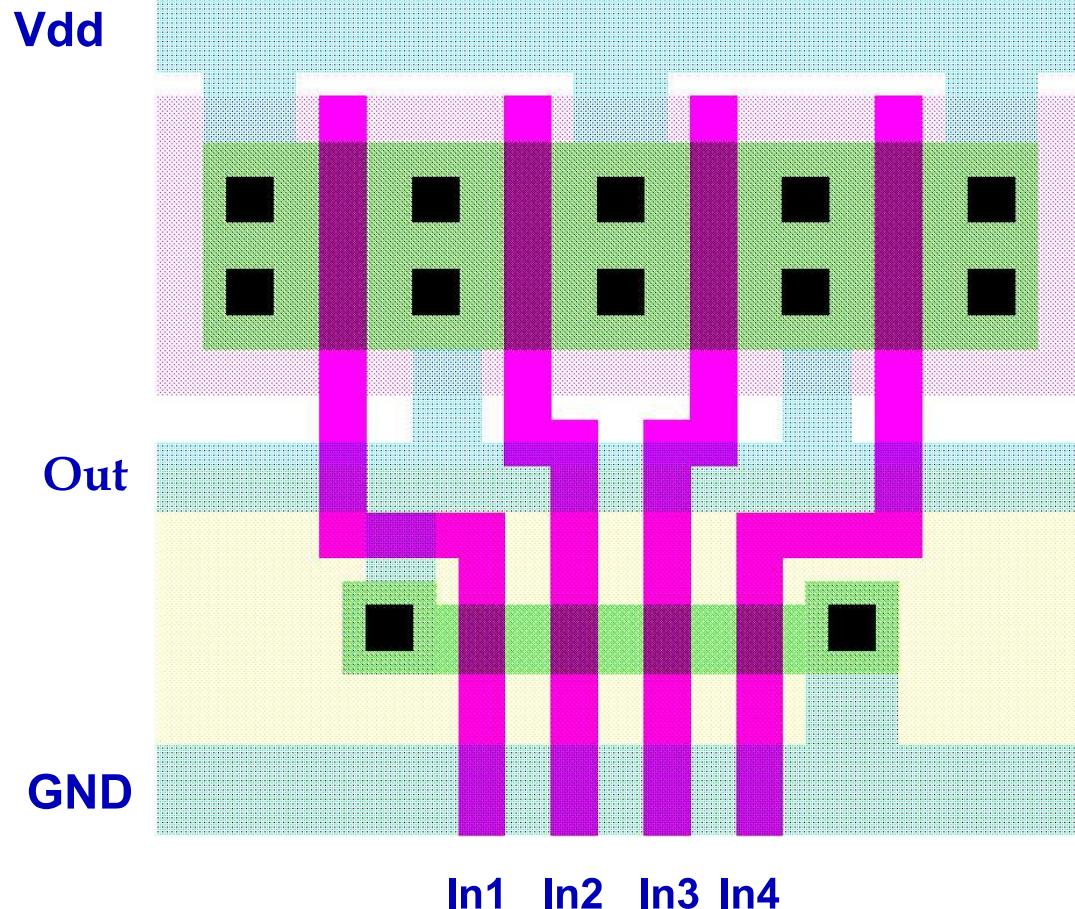
★ A DOMINO N gate can drive :



NAND 4 comparison

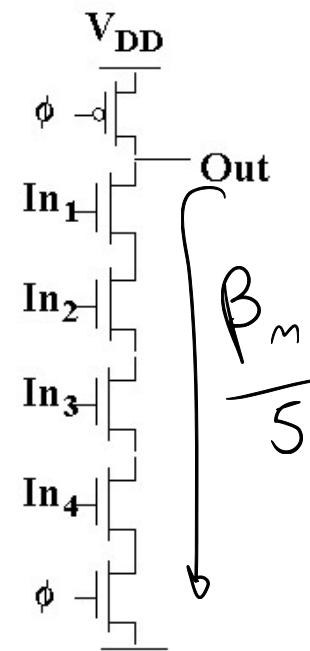
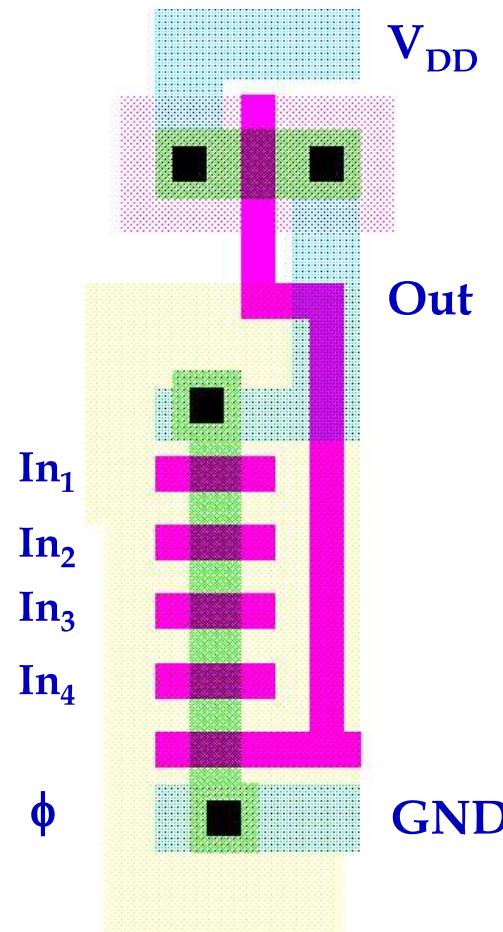
- ❖ Complementary CMOS
- ❖ Dynamic Logic

NAND 4 – Complementary CMOS



$$\omega_p > \omega_n$$

NAND 4 – Dynamic Logic

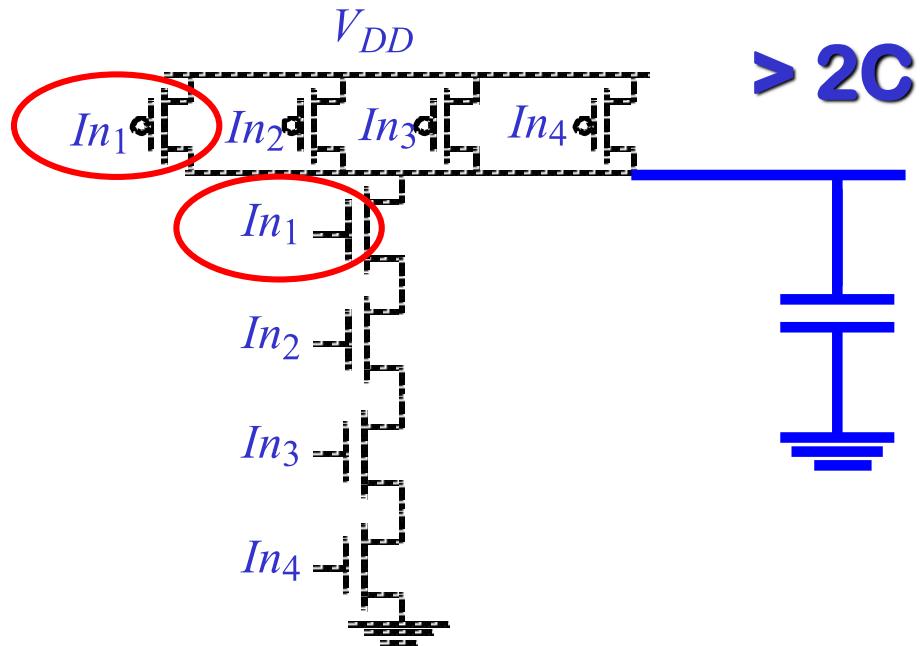
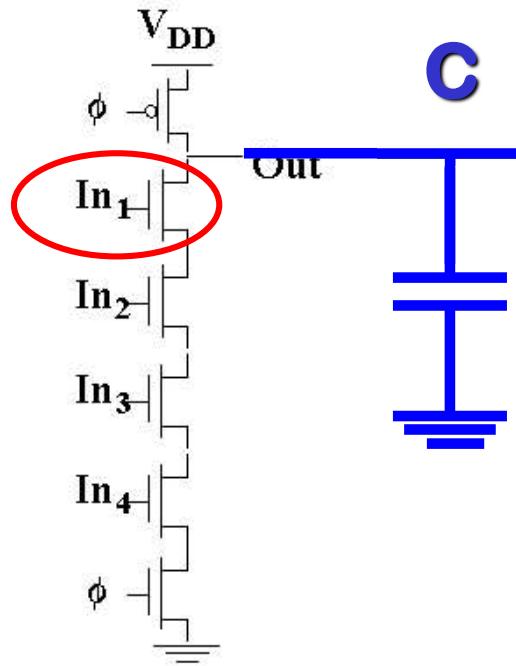


Are there two phases!

NAND 4 – Comparison

Style	# Transistor	Area (μm^2)	Propagation Delay (ns)
Complementary	8	533	0.61
Dynamic	6	212	0.37

NAND 4 – Comparison



$$t_{pHL} \propto \frac{KC}{\beta_n} \frac{1}{V_{DD} - V_{Tn}}$$

$$C_G = C_{ox} W^* L$$