

Electronics and Communication Systems

Electronics Systems

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Outline

✧ Flip Flop: Static Solution

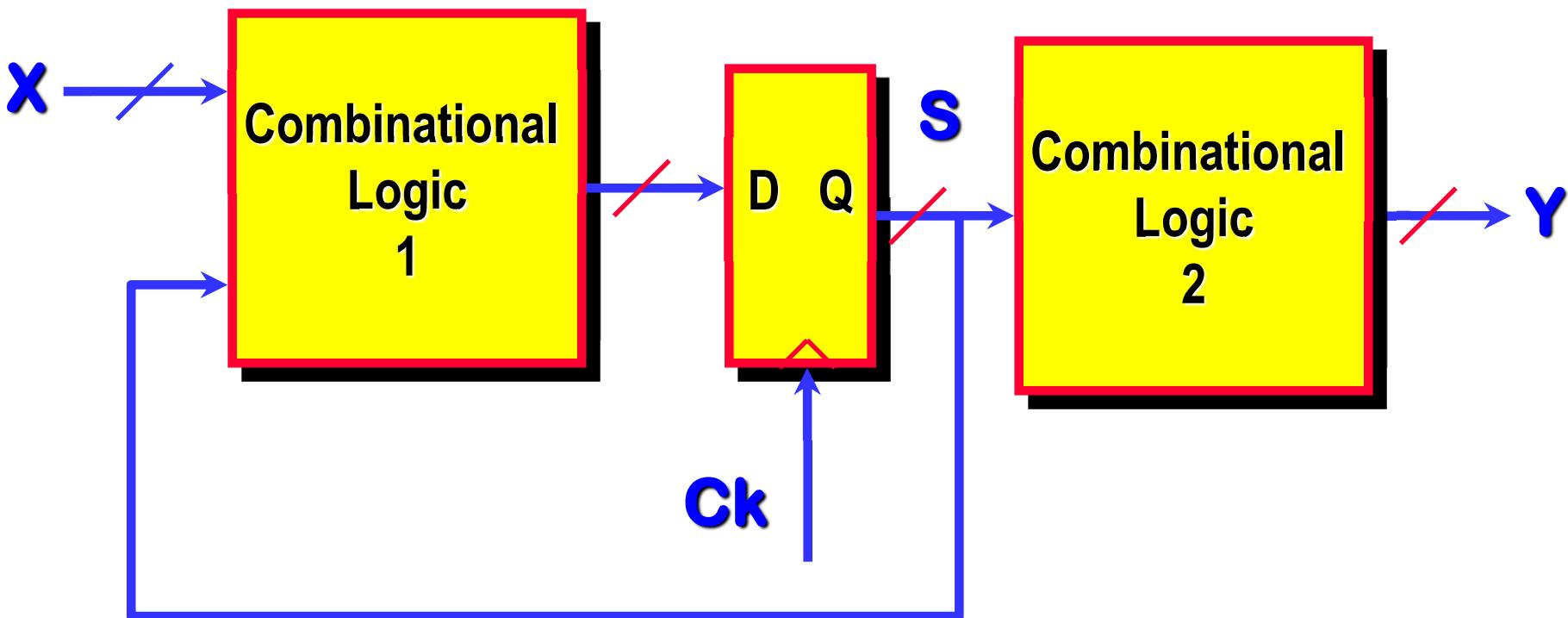
- Flip- Flop S-R: NOR2 e NAND2
- Flip-Flop S-R with enable
- D -Latch
- Flip Flop S-R Edge Triggered: NOR2, NAND2
- Flip Flop D Edge Triggered: NOR2, NAND2, MUX
- Flip Flop D Edge Triggered based on pass gate

✧ Flip Flop: Dynamic Solution

- Flip Flop D Edge Triggered
- Shift Register

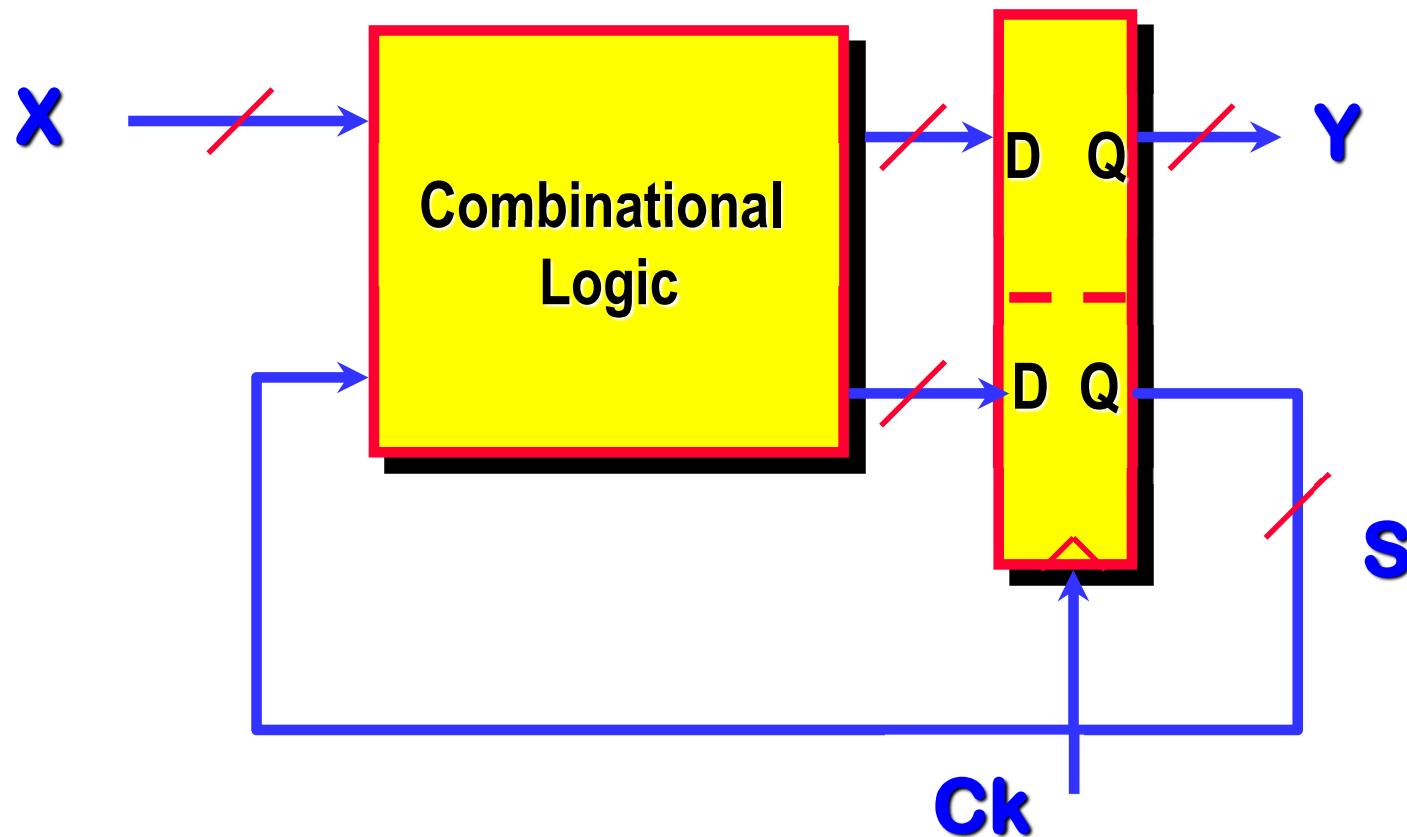
MOORE Machine

❖ Block diagram



Modified MEALY machine

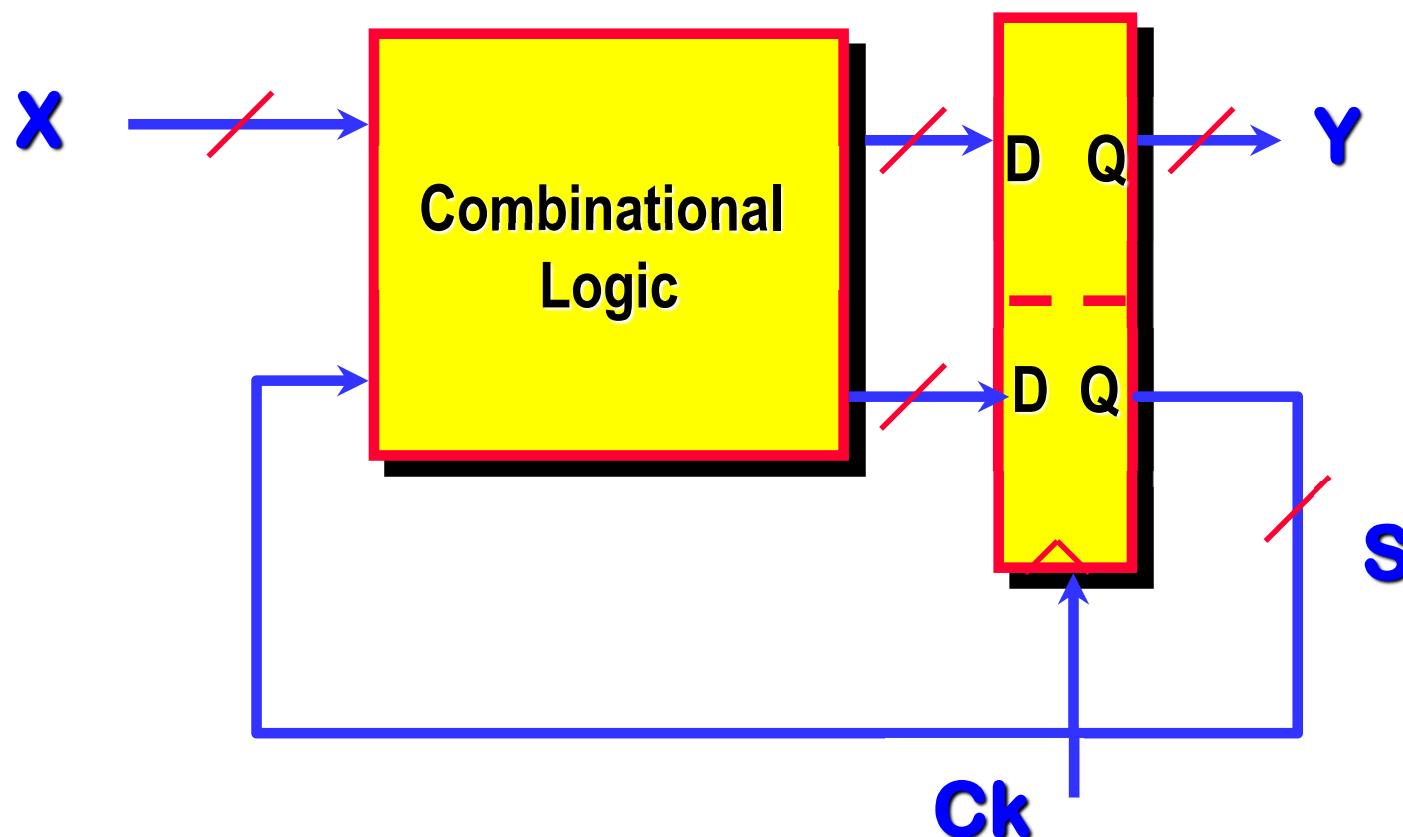
Block Diagram



Finite State Machine: Basic Elements

Combinational Logic

Memory Element (Flip Flop D edge triggered)

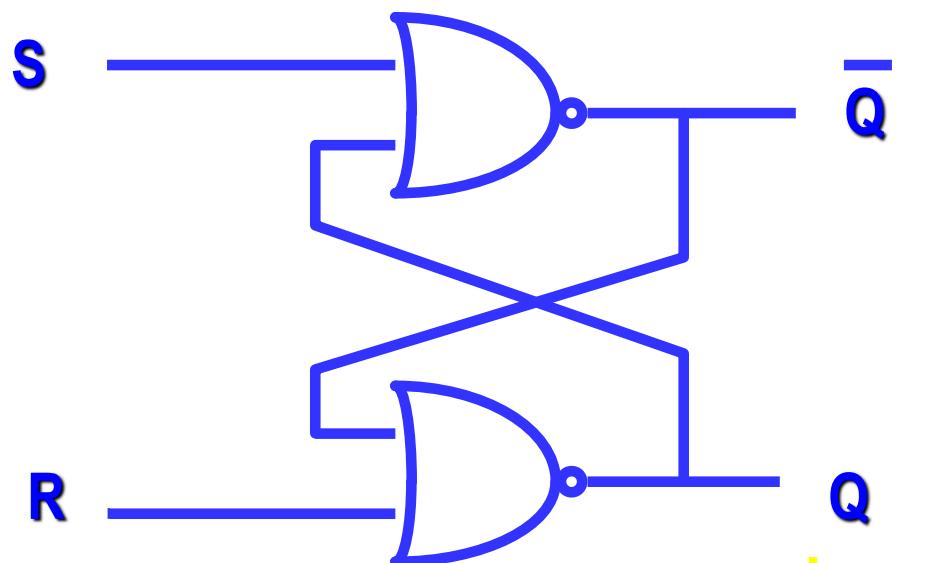


Flip - Flop S - R NOR2 BASED

Truth Table

R	S	Q	\bar{Q}
0	0	Q	\bar{Q}
1	0	0	1
0	1	1	0
1	1

Logic Scheme



A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

Flip - Flop

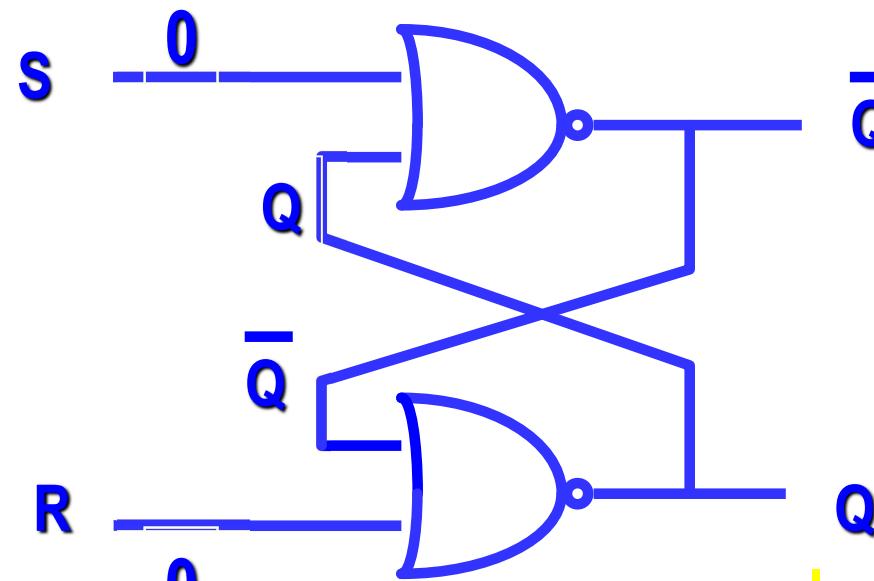
S – R

NOR2 BASED

Truth Table

R	S	Q	\bar{Q}
0	0	Q	\bar{Q}
1	0	0	1
0	1	1	0
1	1	-----	-----

Logic Scheme



A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

Flip - Flop

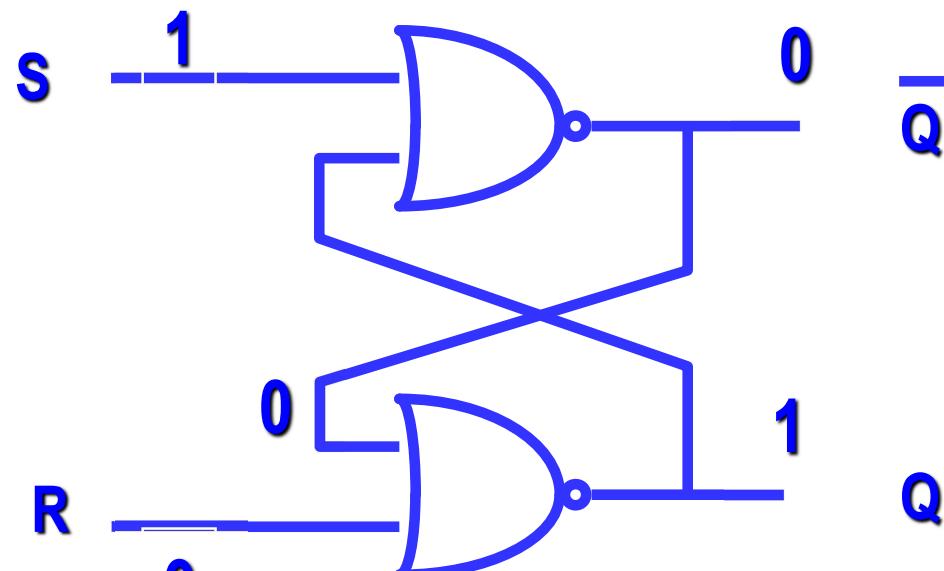
S - R

NOR2 BASED

Truth Table

R	S	Q	\bar{Q}
0	0	Q	\bar{Q}
1	0	0	1
0	1	1	0
1	1

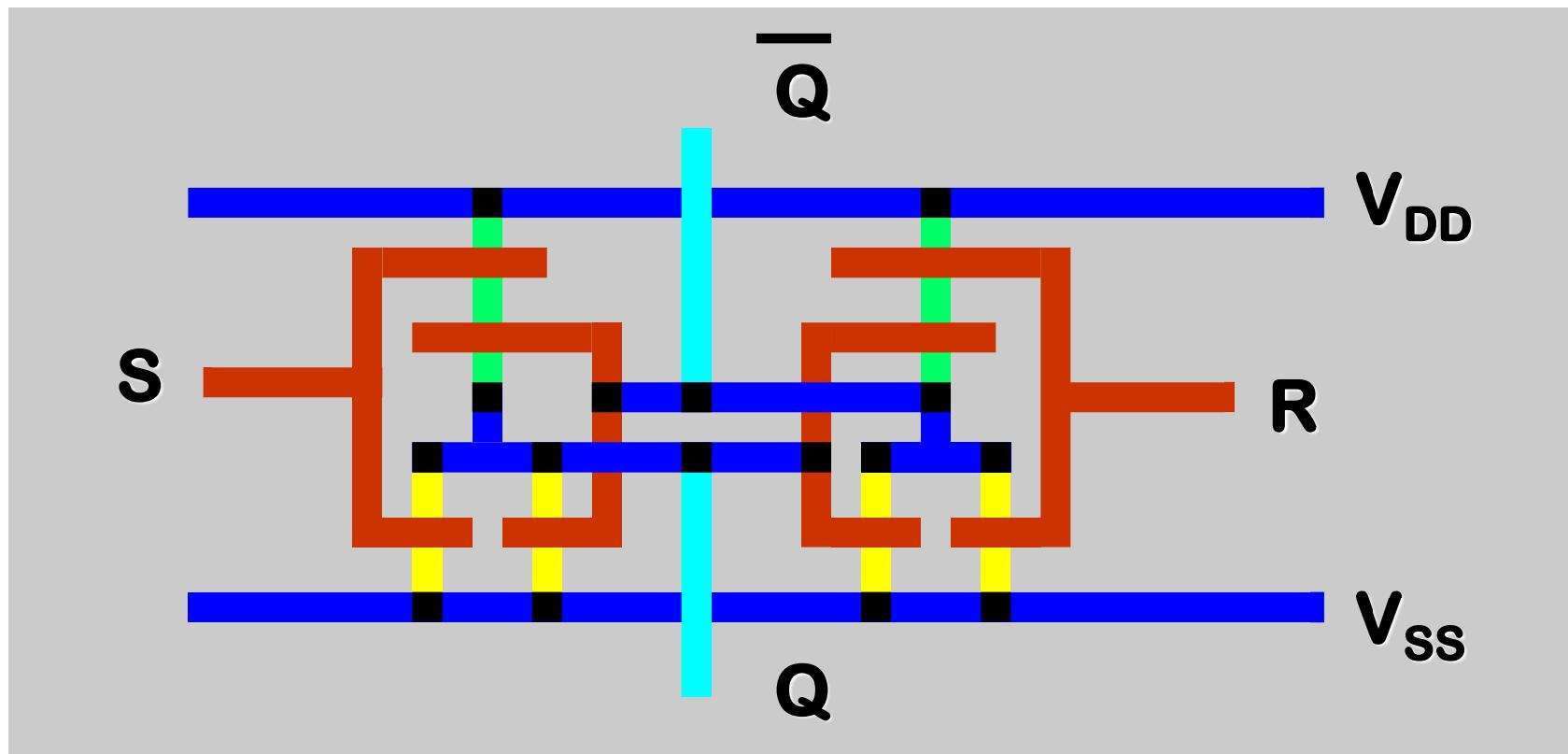
Logic Scheme



A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

Stick Diagram FF SR (NOR2)

❖ Number of Transistors = 8



Flip - Flop

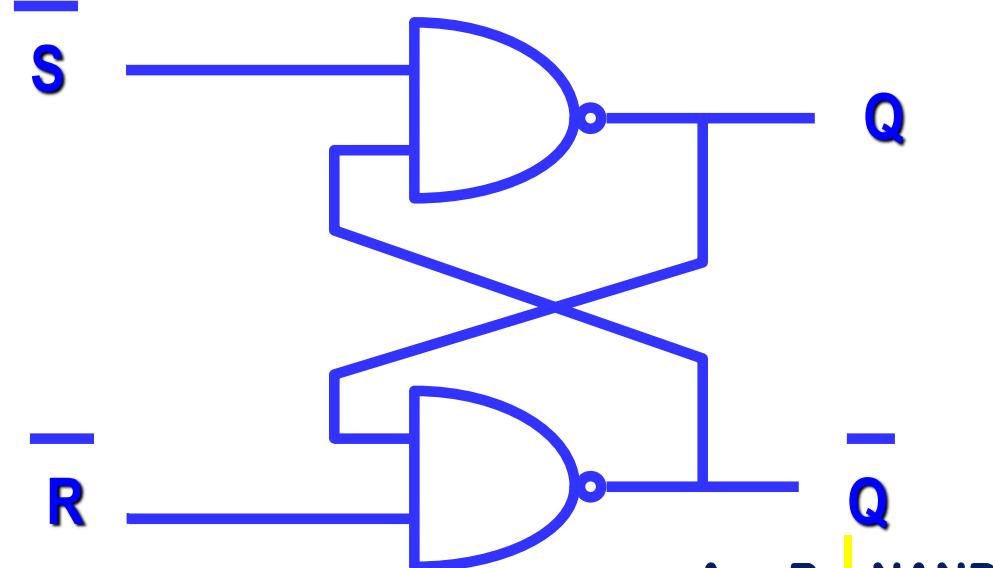
S - R

NAND2 BASED

Truth Table

S	R	\bar{S}	\bar{R}	Q	\bar{Q}	
1	1	0	0	---	---	
1	0	0	1	1	0	
0	1	1	0	0	1	
0	0	1	1	Q	\bar{Q}	

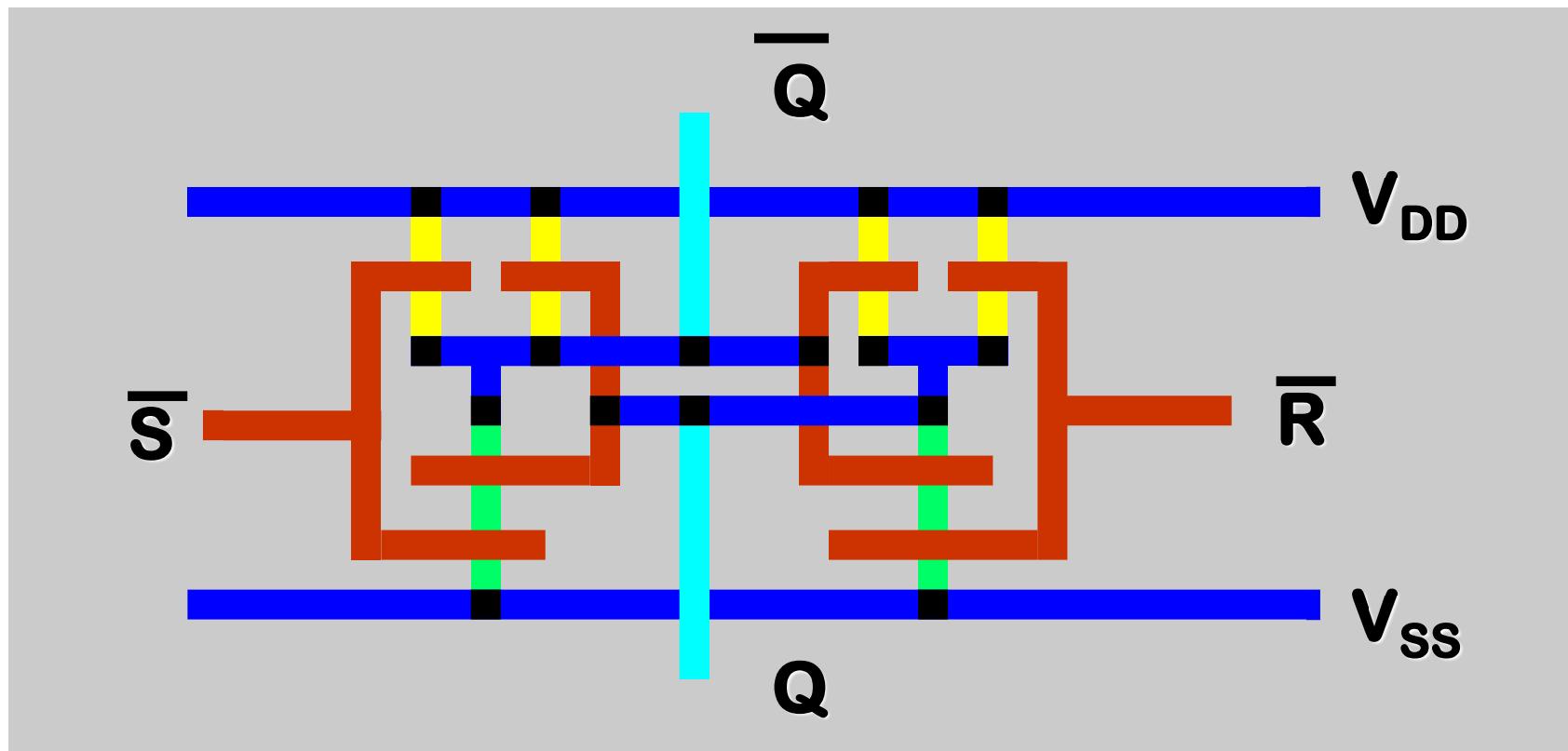
Logic Scheme



A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

Lay-Out simbolico FF SR (NAND2)

❖ Number of Transistors = 8 + 4 (for \bar{S} and \bar{R})



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✧ Flip Flop: Dynamic Solution

- Flip Flop D Edge Triggered
- Shift Register

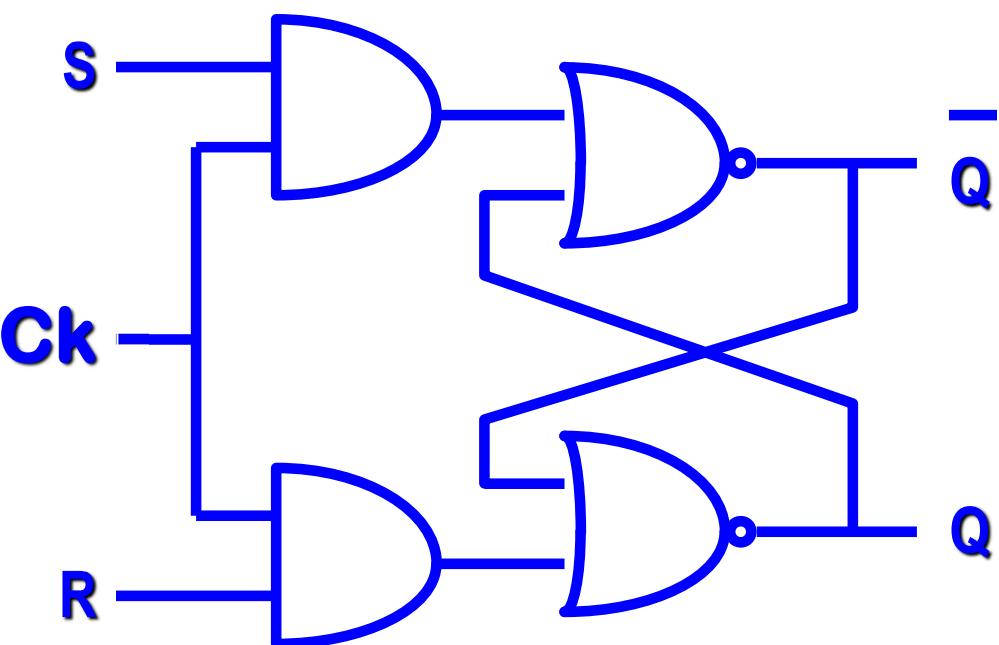
FLIP - FLOP

S - R with clock

Truth Table

S	R	Ck	Q	\bar{Q}
x	x	0	Q	\bar{Q}
0	0	1	Q	\bar{Q}
0	1	1	0	1
1	0	1	1	0
1	1	1	---	---

Logic Scheme



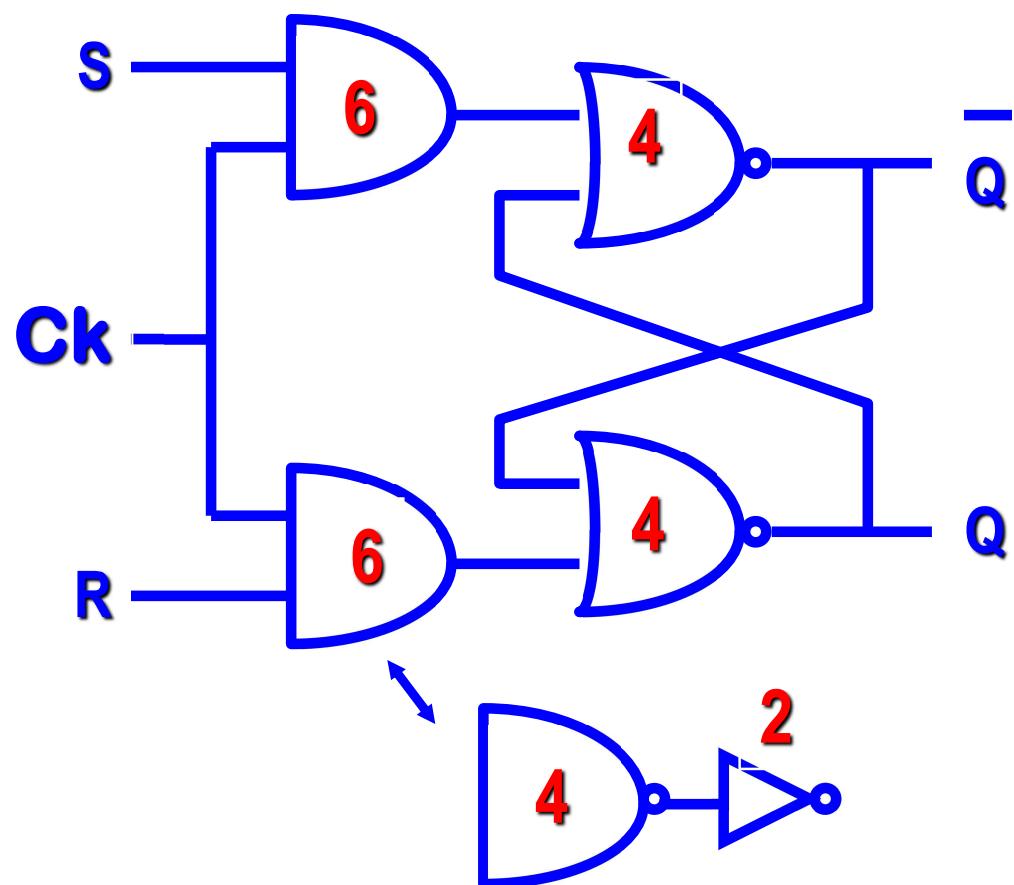
FLIP - FLOP

S - R with clock

Truth Table

S	R	Ck	Q	\bar{Q}
x	x	0	Q	\bar{Q}
0	0	1	Q	Q
0	1	1	0	1
1	0	1	1	0
1	1	1

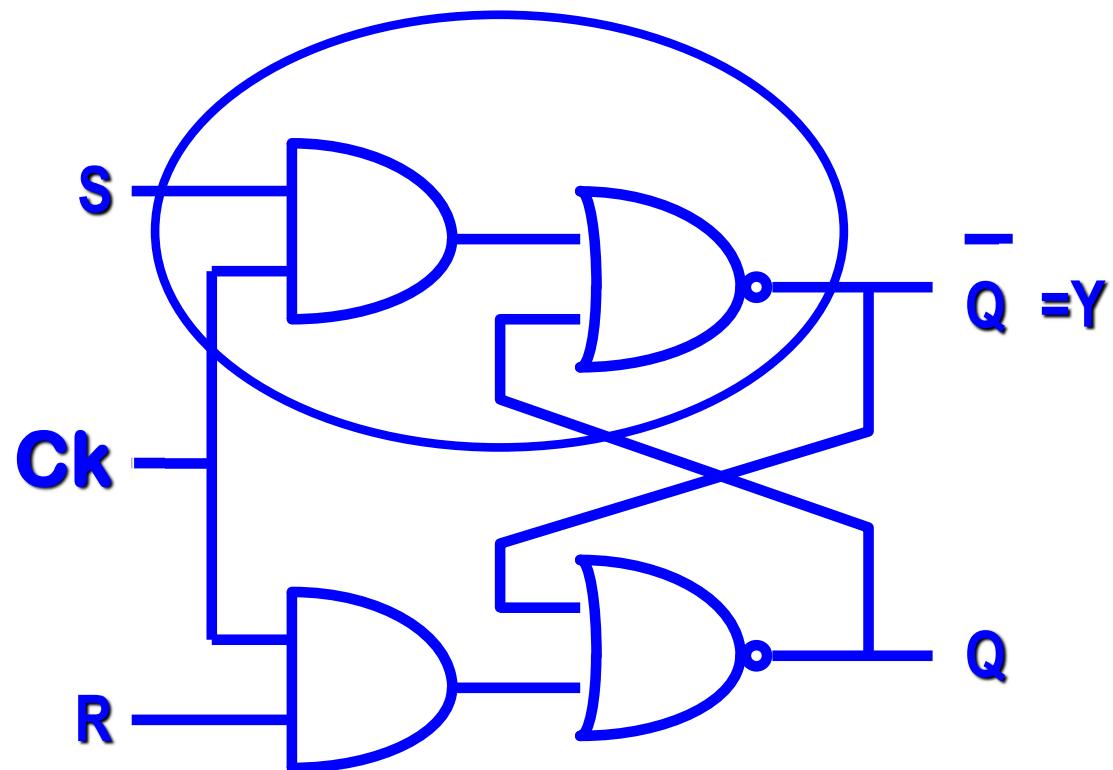
Logic Scheme



20 TR

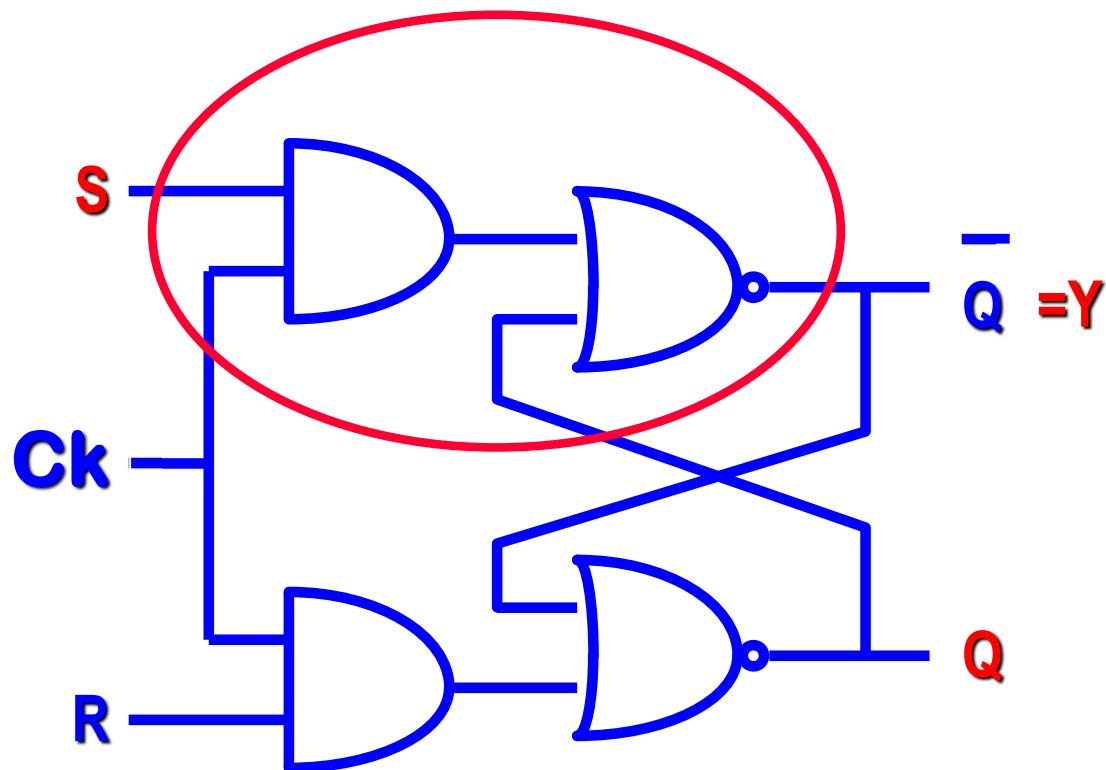
FLIP - FLOP

S - R con clock



$$Y = \bar{Q} = \overline{S \cdot CK + Q}$$

FLIP - FLOP

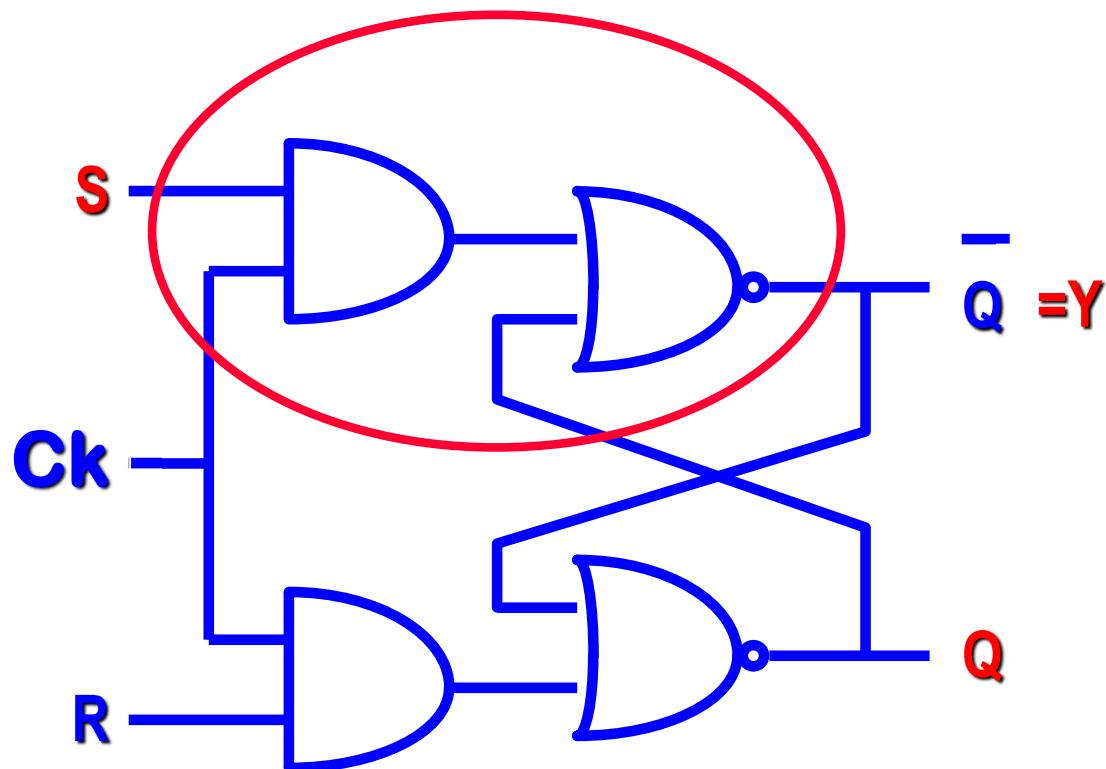


$$Y = \bar{Q} = S \cdot \overline{CK} + Q$$

S - R con clock

Q	CK	S	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0

FLIP - FLOP



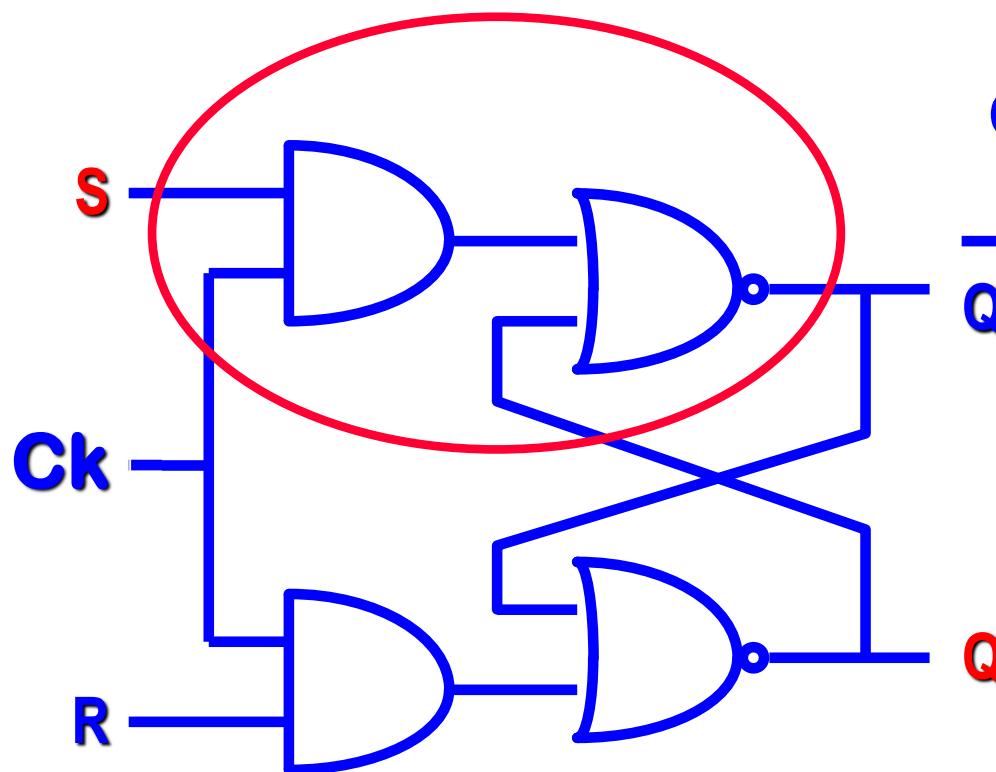
$$Y = \bar{Q} = \overline{S \cdot CK + Q}$$

$$\bar{Y}_{PDN} = S \cdot CK + Q$$

S - R con clock

Q	CK	S	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0

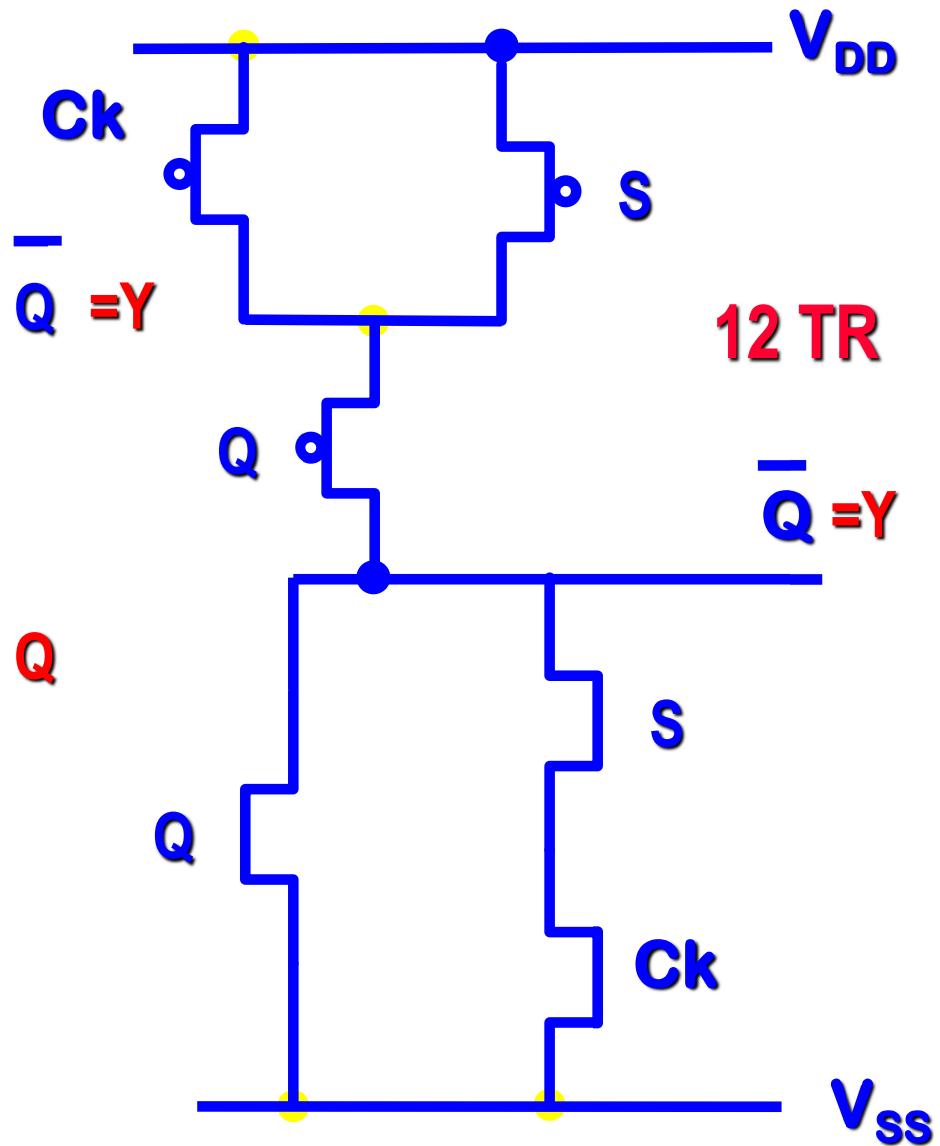
FLIP - FLOP



$$Y = \bar{Q} = \overline{S \cdot CK + Q}$$

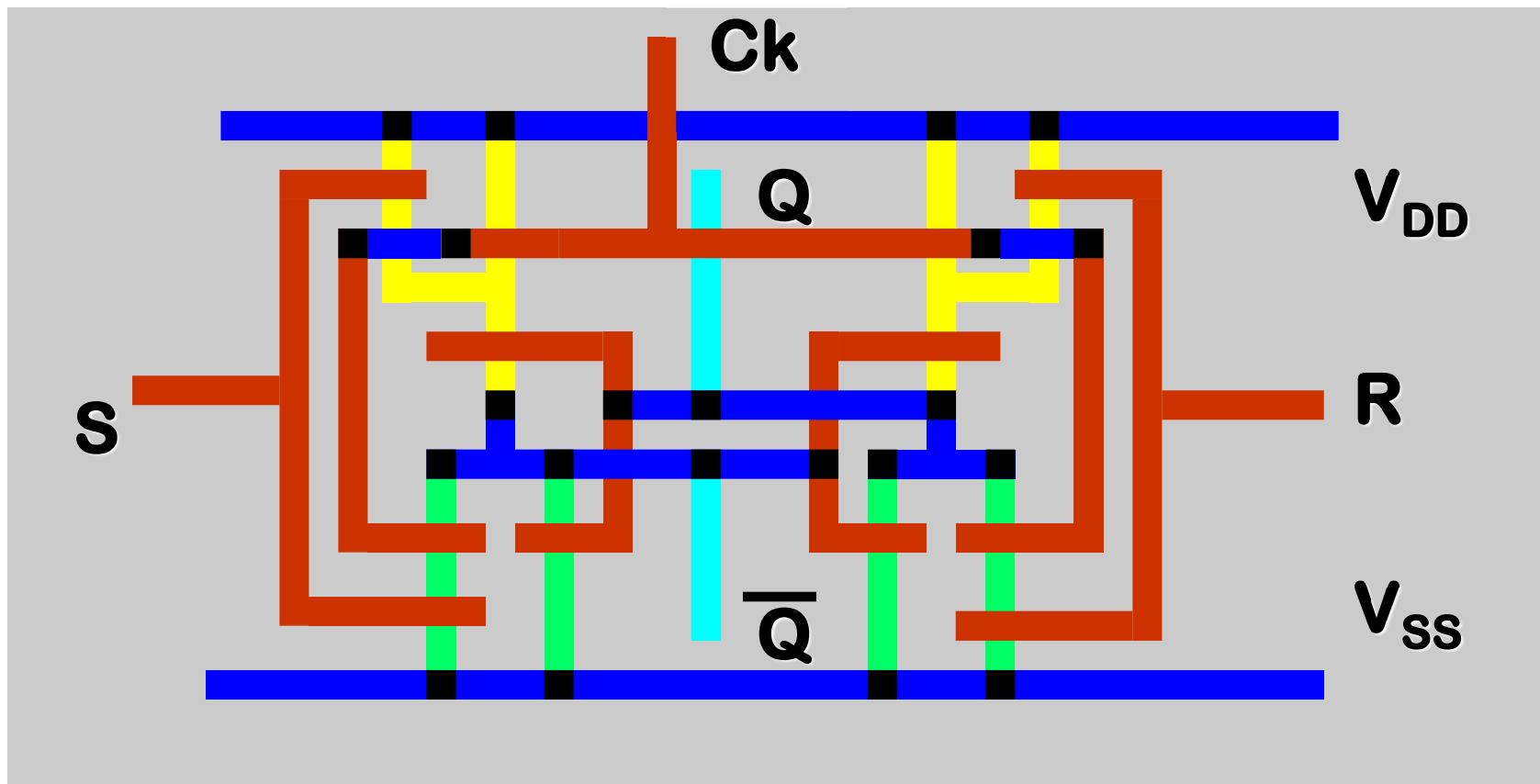
$$\bar{Y}_{PDN} = S \cdot CK + Q$$

S - R con clock



Stick Diagram

✿ Number of Transistors = 12



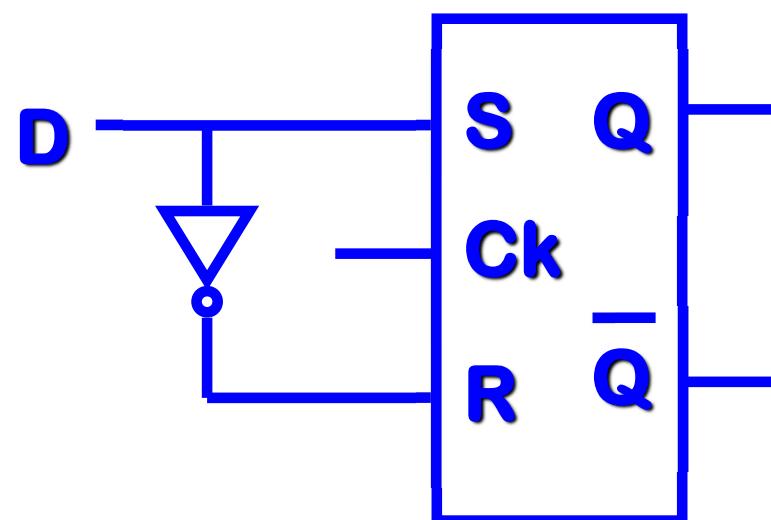
Latch

Truth Table

D	Ck	Q
X	1	Q
0	0	0
1	0	1

Logic Scheme

14 transistors

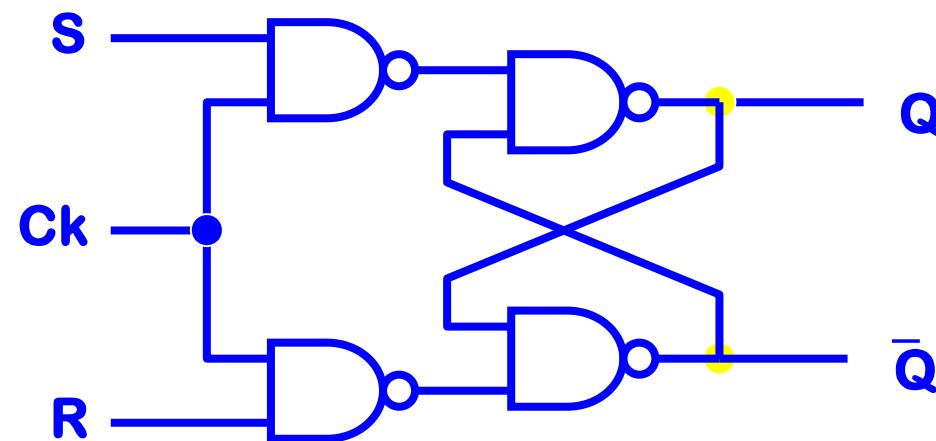


FF SR (NAND2) with clock

❖ Truth Table

Ck	S	R	Q
0	x	x	Q
1	0	0	Q
1	0	1	0
1	1	0	1
1	1	1	-

Logic Scheme



A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

Number of Transistors = 16

Outline

✧ Flip Flop: Static Solution

- Flip- Flop S-R: NOR2 e NAND2
- Flip-Flop S-R with enable
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- Flip Flop S-R Edge Triggered: NOR2, NAND2
- Flip Flop D Edge Triggered: NOR2, NAND2, MUX
- Flip Flop D Edge Triggered based on pass gate

✧ Flip Flop: Dynamic Solution

- Flip Flop D Edge Triggered
- Shift Register

Flip – Flop D

❖ $Ck = 1$

– Output Q follows input D

❖ $Ck = 0$

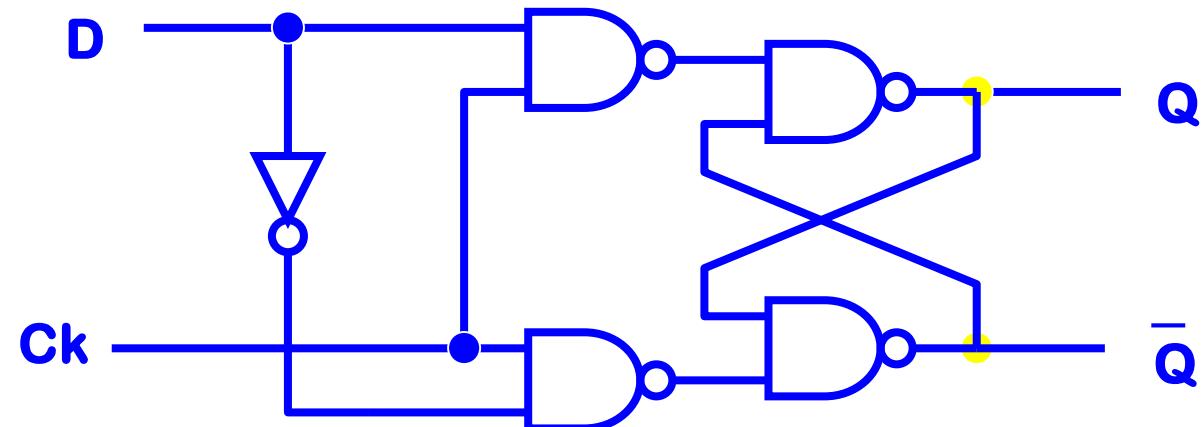
Number of Transistors= 18

– Output maintains previous value

❖ Truth Table

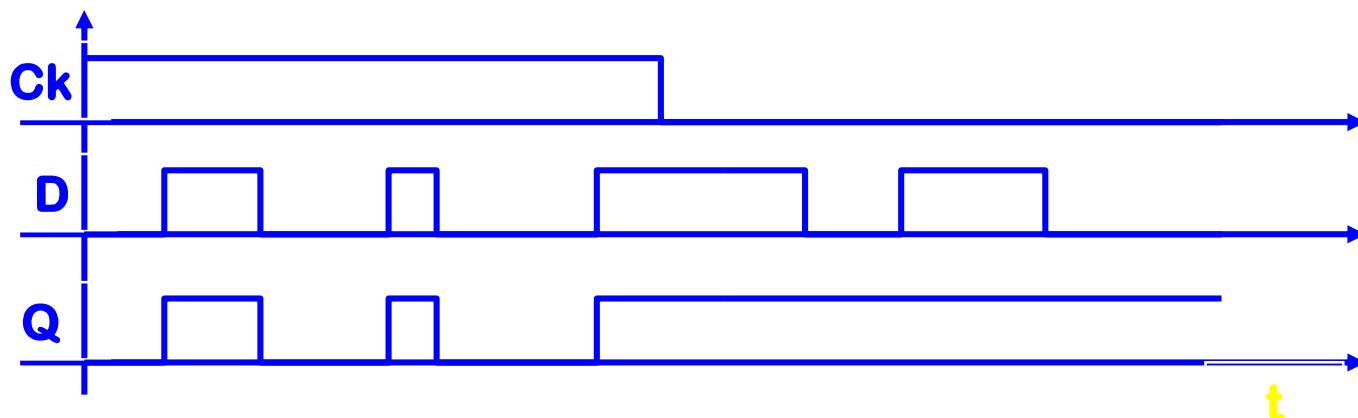
Logic Scheme

Ck	D	Q
0	x	Q
1	0	0
1	1	1



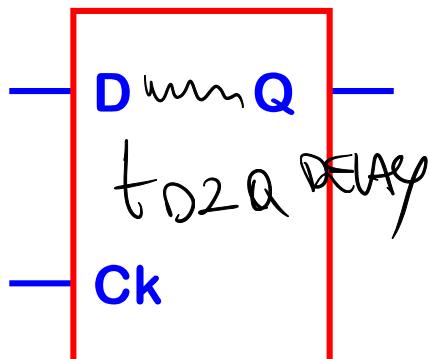
Notes

- ❖ When Clock is 1 Output Q follows input D



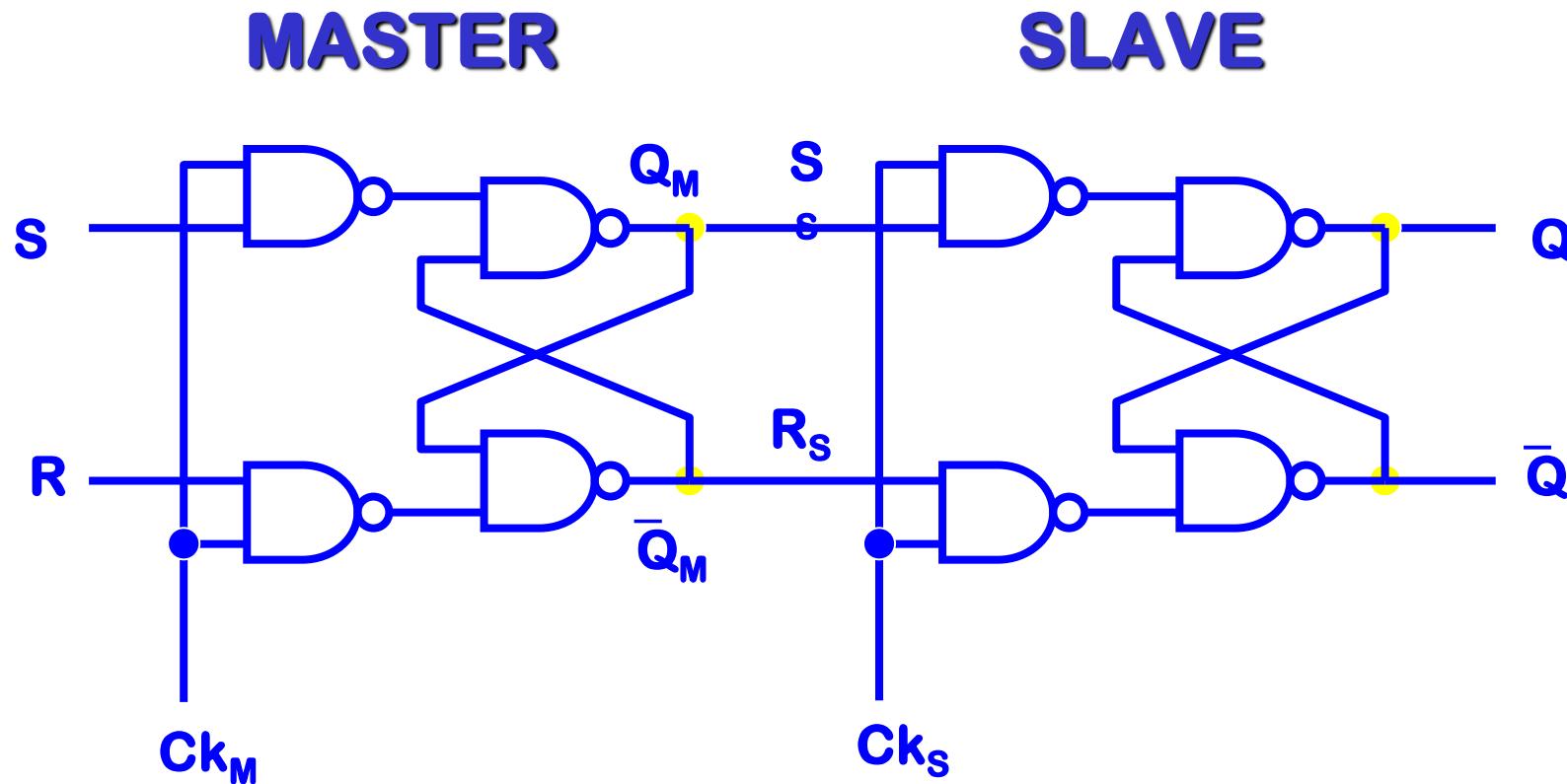
- ❖ Flip- Flop is “TRANSPARENT”

- ❖ Symbol



- Sensitive to high CK level !!
- Data is stored when CK changes from 1 to 0

MASTER – SLAVE Architecture

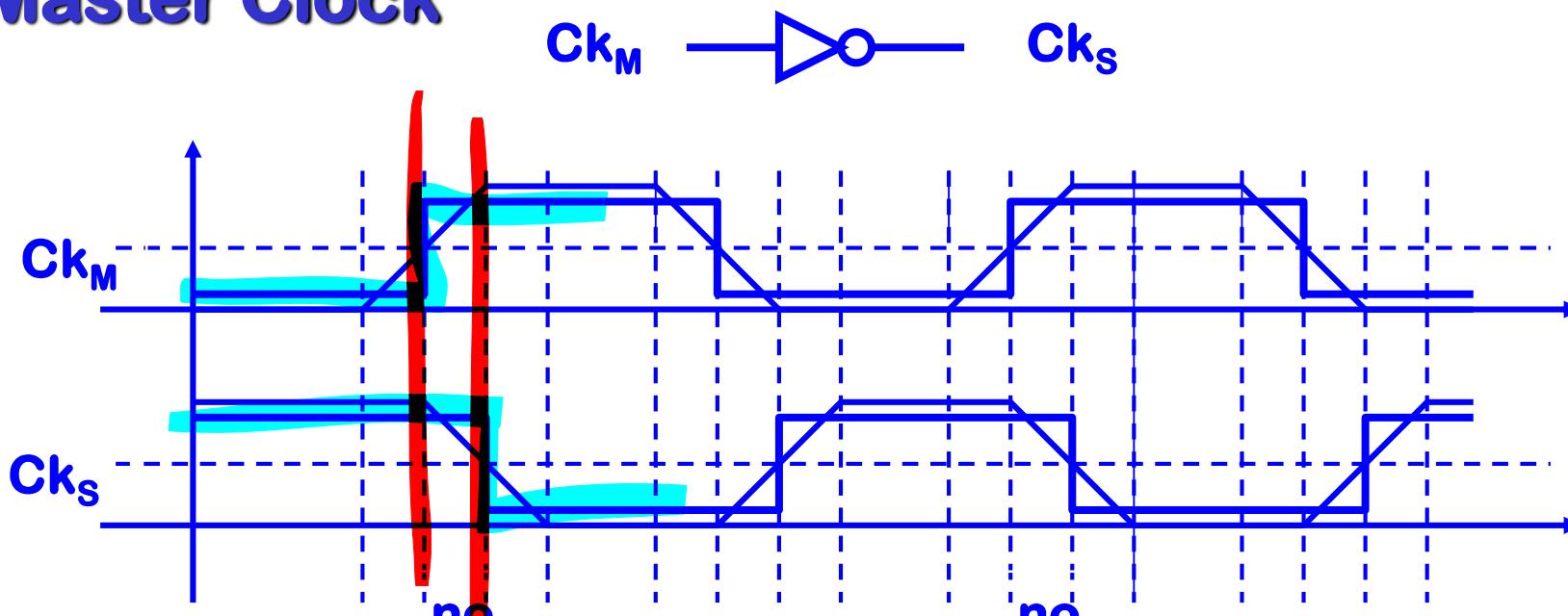


Number of Transistors = 32

Not overlapped Clock

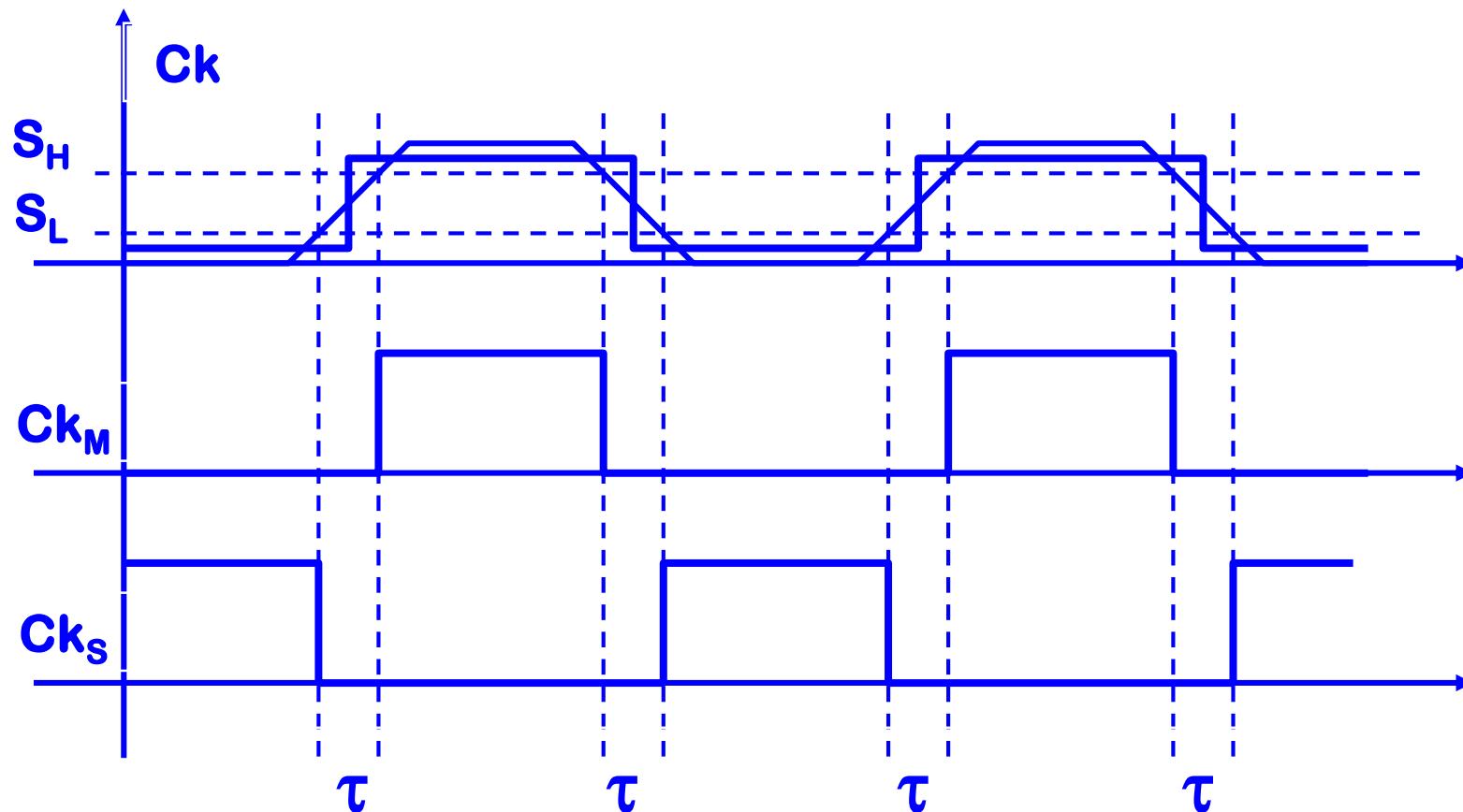
- master clock and slave clock never equal to 1 at the same time
- Slave Clock cannot be generated by inverting Master Clock

Master Clock

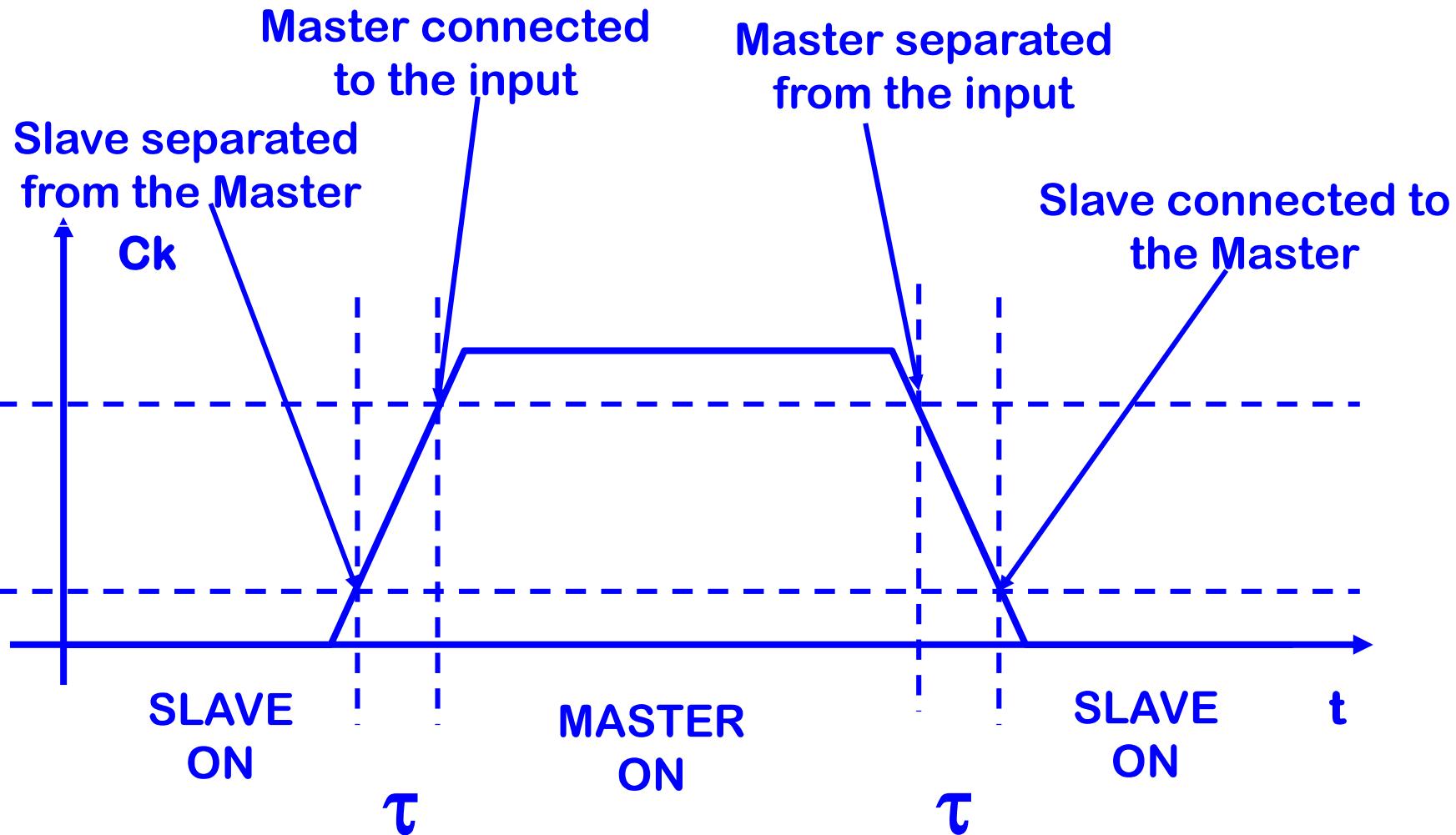


Not Overlapped Clock

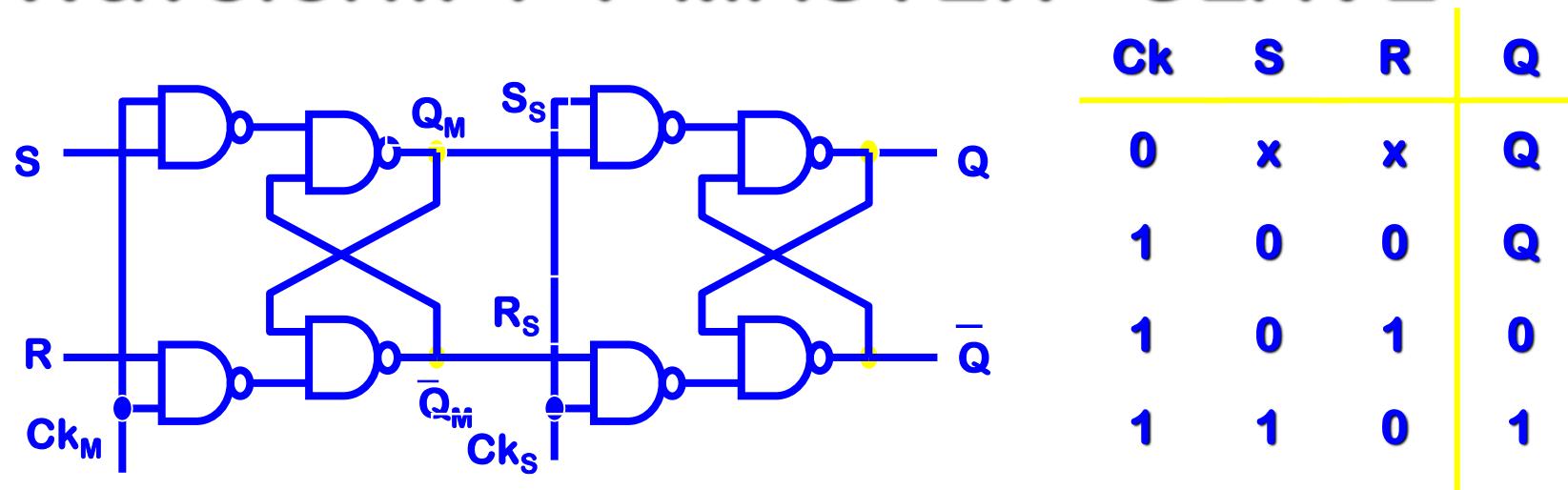
❖ Threshold Techniques



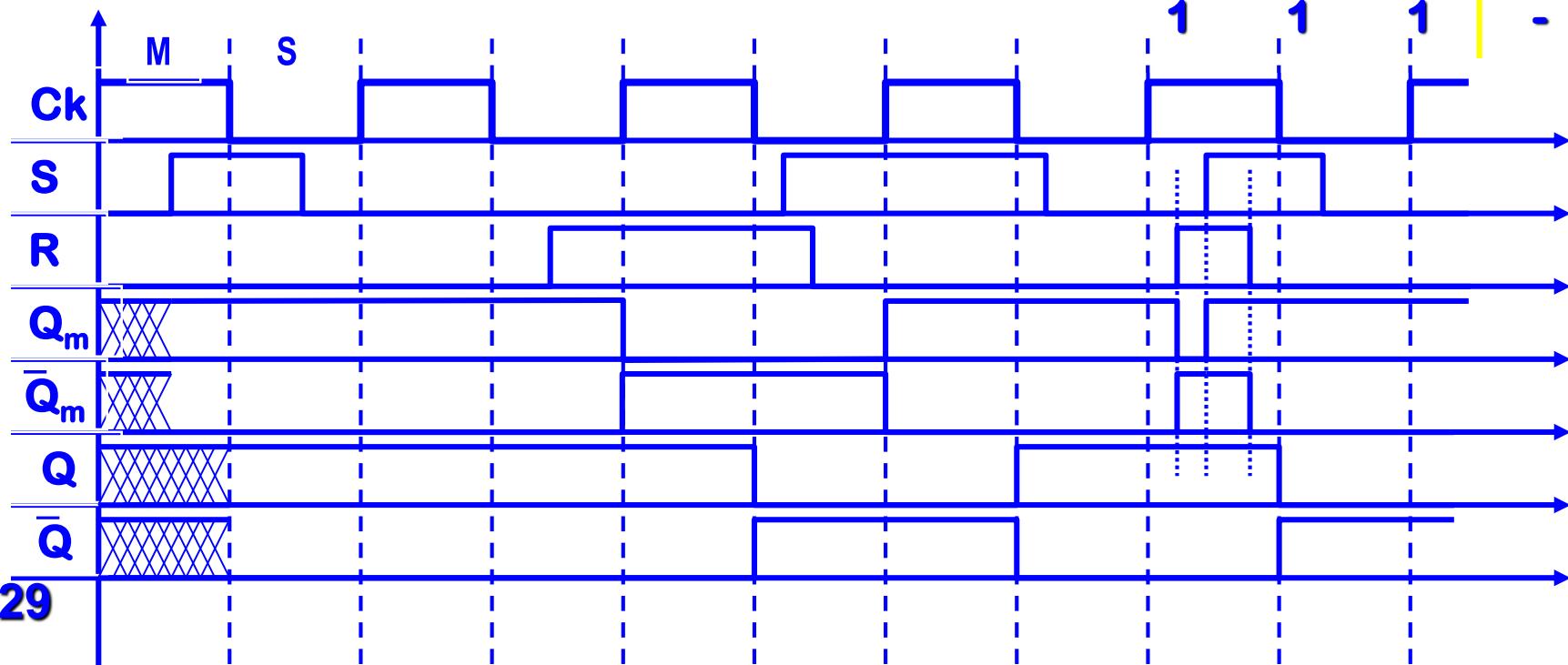
Working Sequence



Waveform F-F MASTER - SLAVE

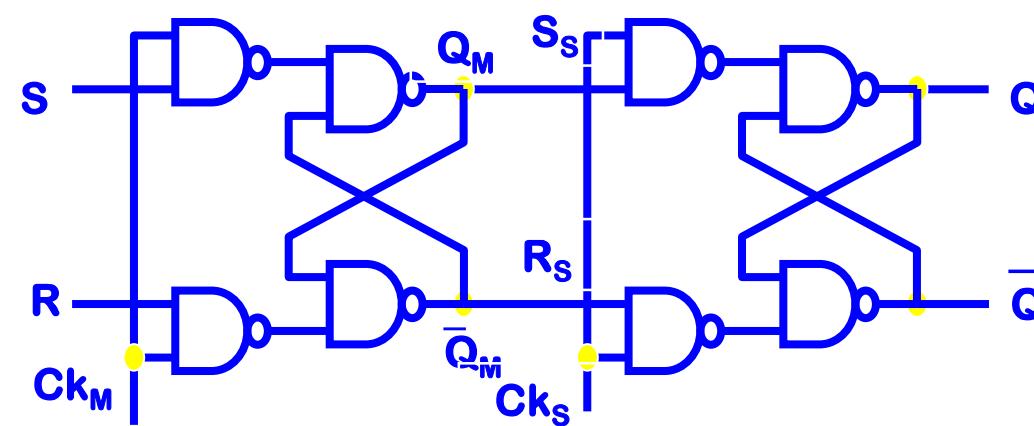


Ck	S	R	Q
0	x	x	Q
1	0	0	Q
1	0	1	0
1	1	0	1
1	1	1	-



Truth Table

Ck	S	R	Q
0	x	x	Q
1	x	x	Q
-	x	x	Q
0	0	Q	Q
-	0	1	0
1	0	1	1
1	1	-	-

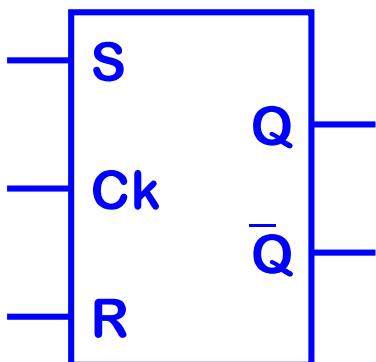


FF S-R edge-triggered

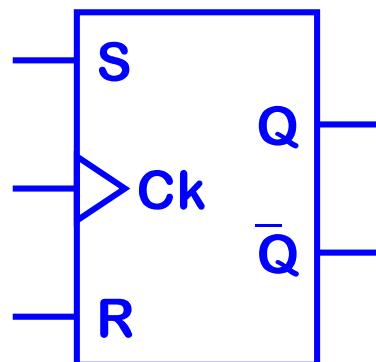
✿ Notes

- Flip-Flop S-R Master Slave changes the output when Clock falling edge
- Negative EDGE-TRIGGERED

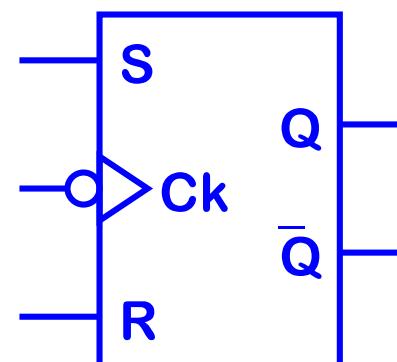
✿ Symbols



FF S-R
With clock

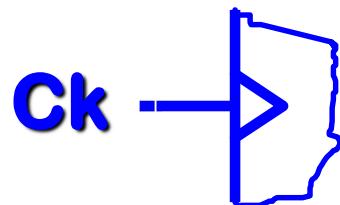


FF S-R
Positive
Edge-Triggered

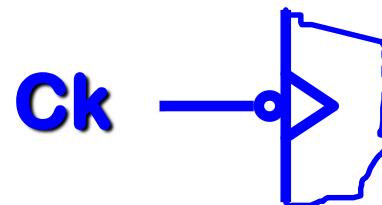


FF S-R
Negative
Edge-Triggered

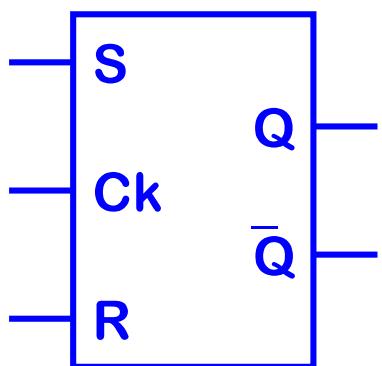
FF S-R edge-triggered



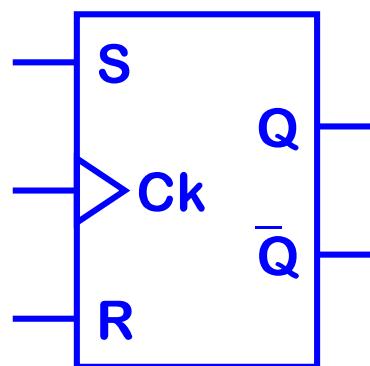
Rising Edge



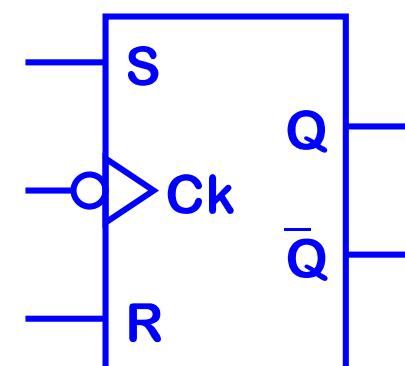
Falling Edge



FF S-R
With Clock



FF S-R
Positive
Edge-Triggered

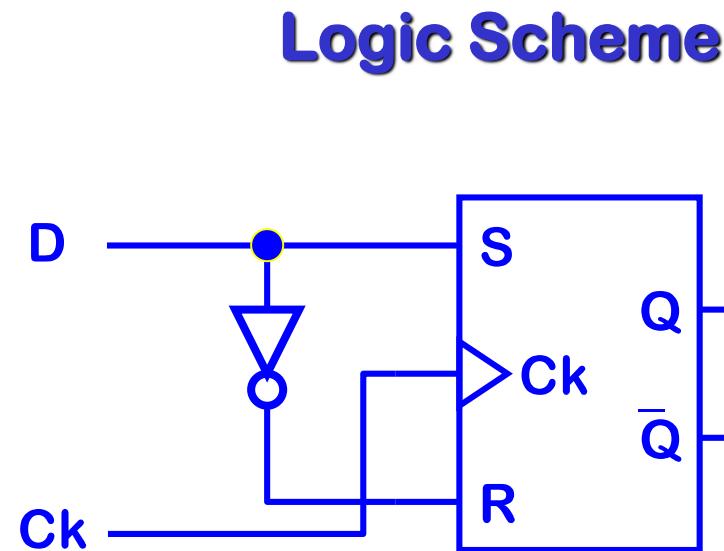


FF S-R
Negative
Edge-Triggered

Flip- Flop D Edge Triggered

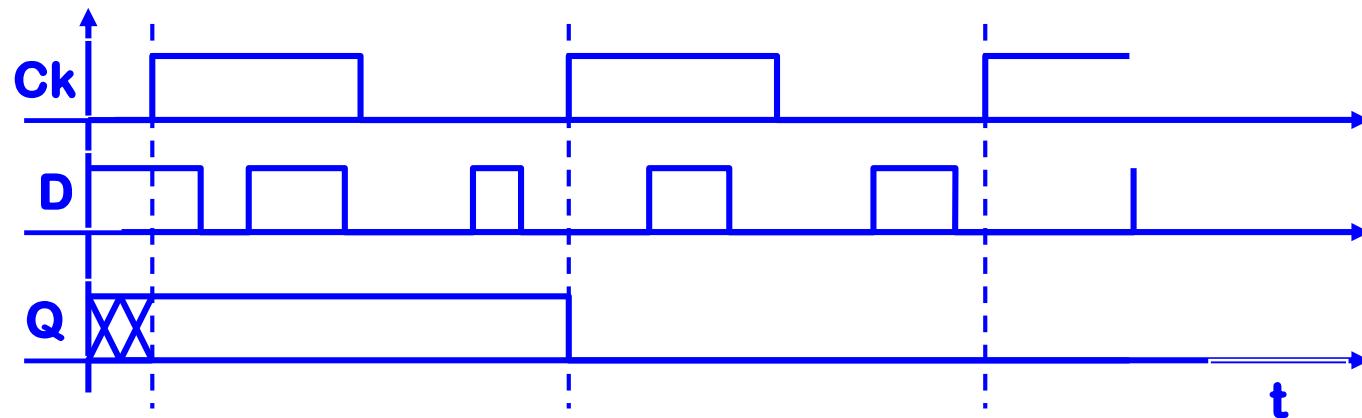
- ❖ Data is transferred to the output when clock rising (falling) edge occurs
- ❖ Truth Table

Ck	D	Q
0	X	Q
1	X	Q
{	X	Q
{	0	0
{	1	1



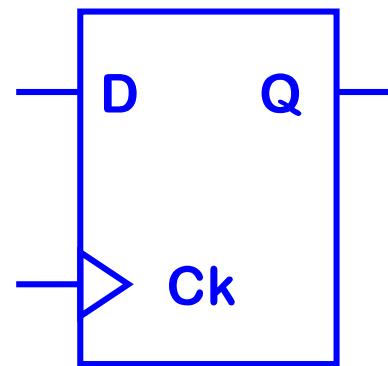
Number of Transistors= 34

Notes

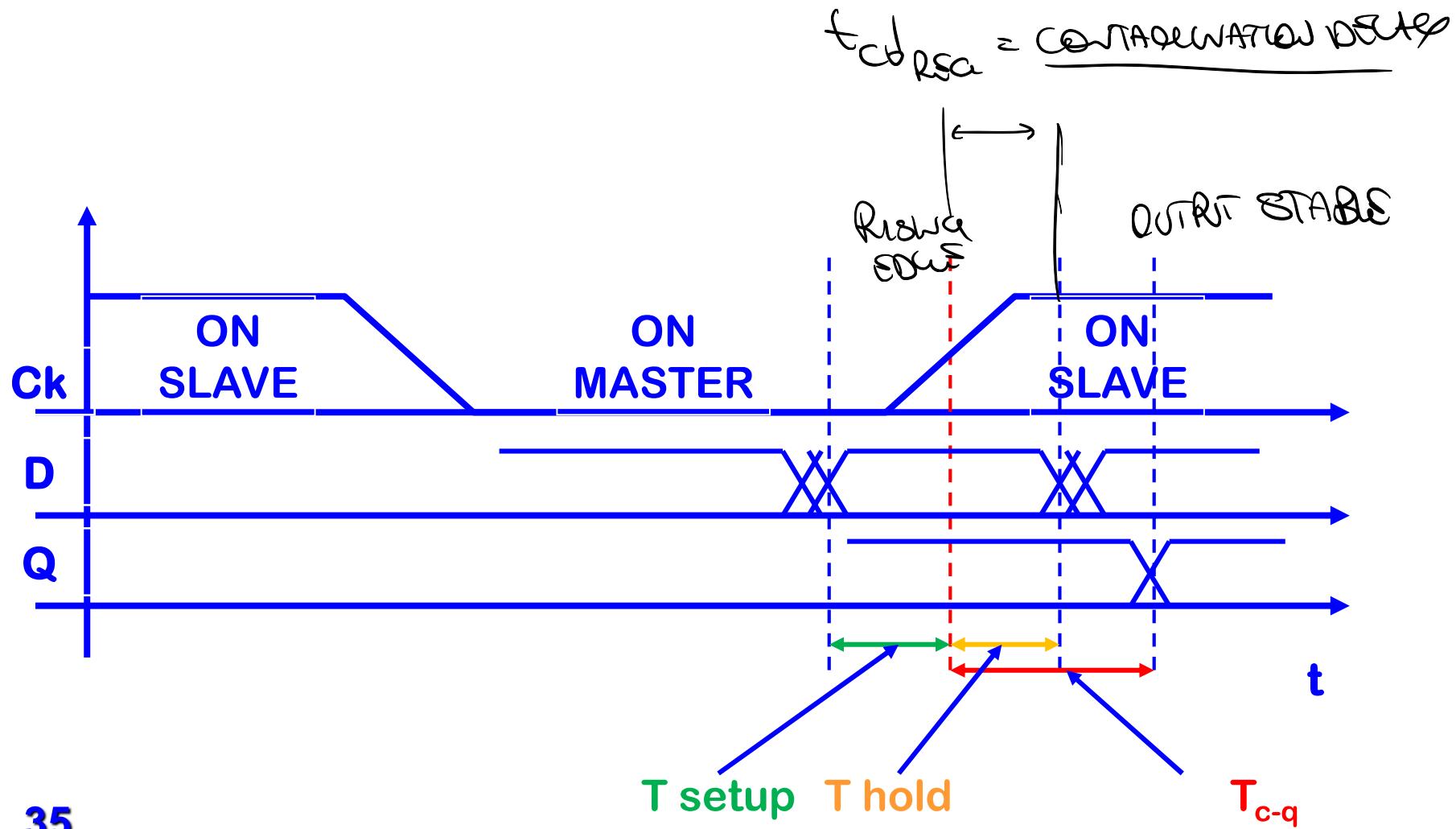


❖ Output is updated synchronously with the Clock

❖ Symbol

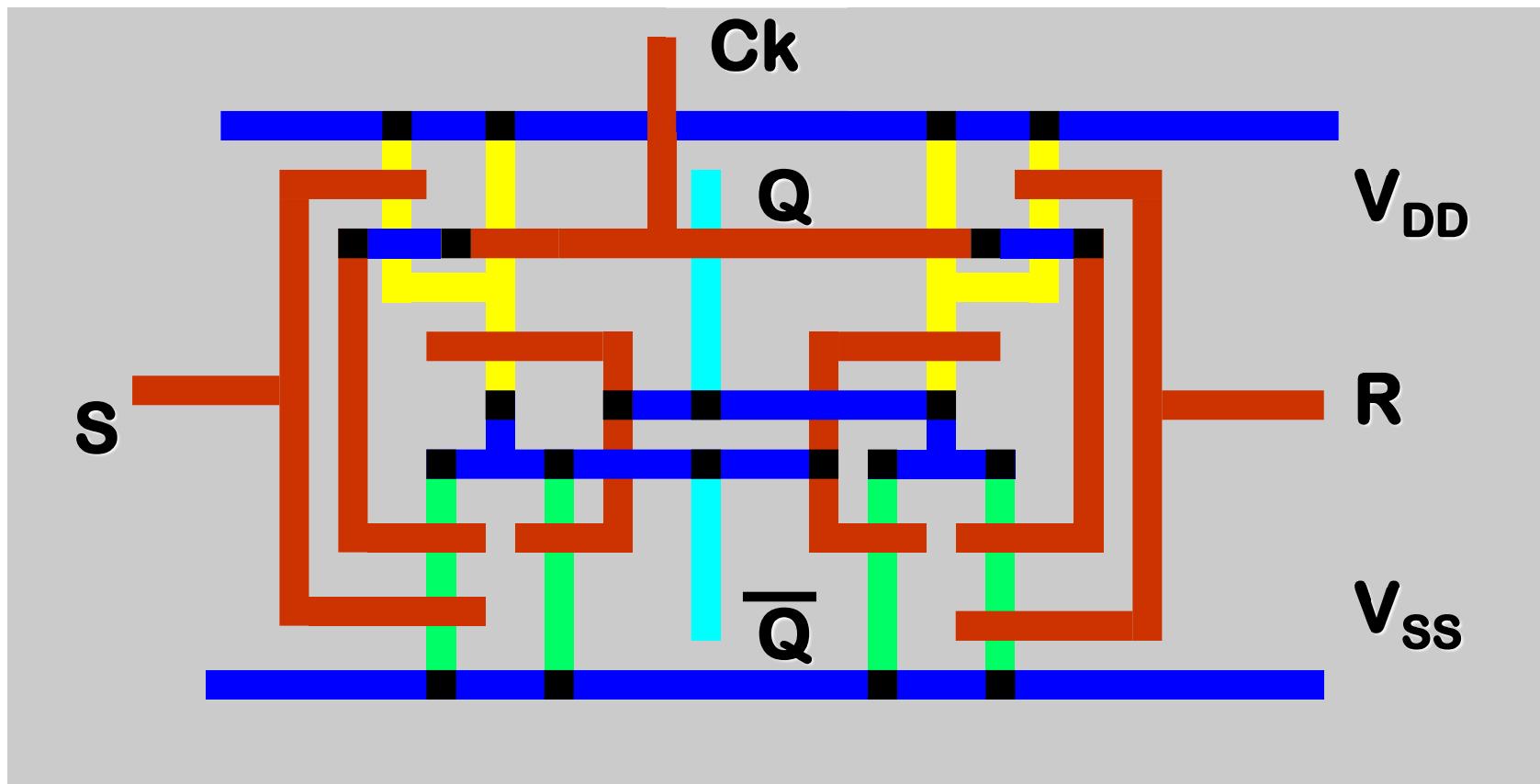


Timing Rules



Stick Diagram FFSR (NOR2)

◆ Number of Transistors = 12



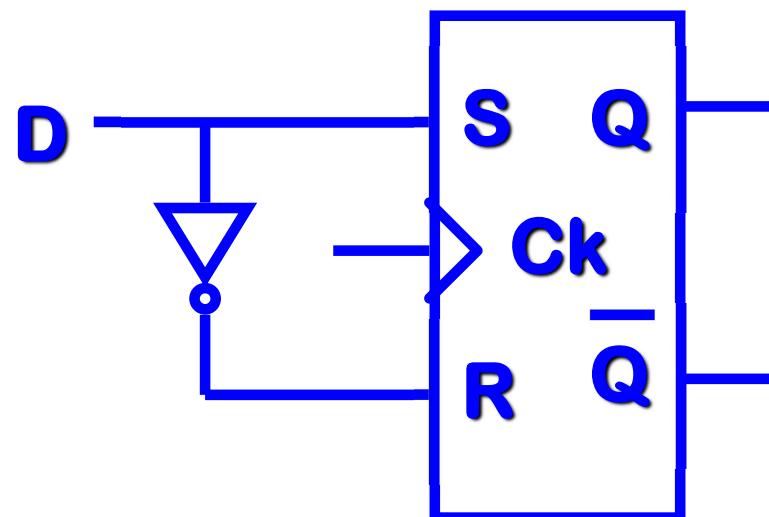
FF D edge triggered on FFSR(NOR2)

Truth Table

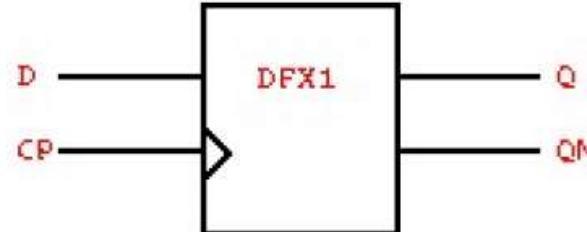
D	Ck	Q
X	1	Q
X	0	Q
X	L	Q
0	L	0
1	L	1

Logic Scheme

12+12+2=26 transistors



Description	F03. Edge Flip Flop with drive strength X1			
Strength	1			
Cell Area	232.960 μm^2			
Equation	$Q = "D"$ $QN = "!(D)"$			
Clock	CP			
Type	Sequential			
Input	D			
Output	Q, QN			



State Table					
CP	D	$IQ_{(int)}$	$IQN_{(int)}$	Q	QN
R	L	-	-	L	H
R	H	-	-	H	L
F	-	L	H	L	H
F	-	H	L	H	L

Propagation Delay [ns]					
Input Transition [ns]		0.01		4.00	
Load Capacitance [fF]	5.00	100.00	5.00	100.00	
CP to Q	fall	0.30	0.68	0.18	0.55
	rise	0.26	0.87	0.14	0.75
CP to QN	fall	0.30	0.67	0.18	0.55
	rise	0.37	0.99	0.25	0.86

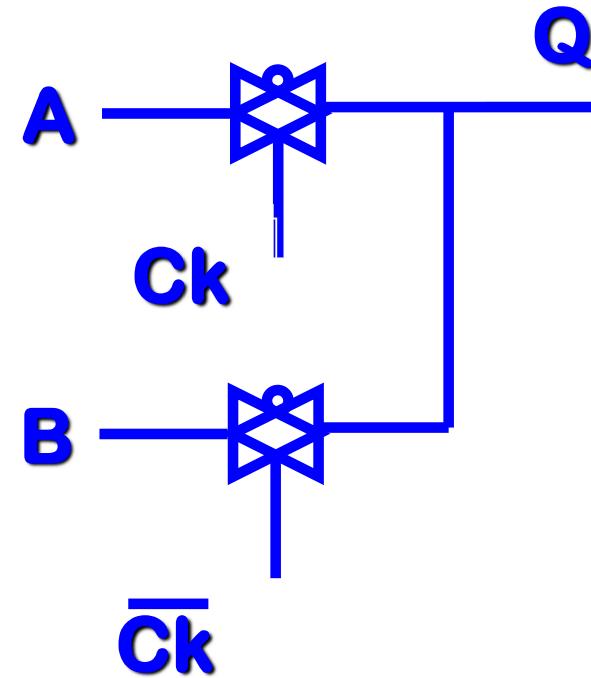
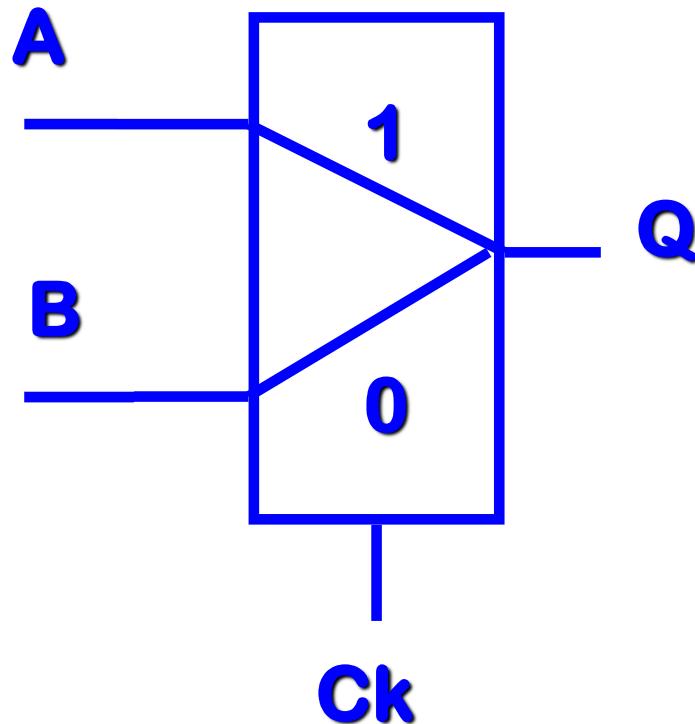
Output Transition [ns]					
Input Transition [ns]		0.01		4.00	
Load Capacitance [fF]	5.00	100.00	5.00	100.00	
CP to Q	fall	0.06	0.54	0.06	0.54
	rise	0.09	1.04	0.09	1.04
CP to QN	fall	0.06	0.53	0.06	0.53
	rise	0.09	1.04	0.09	1.04

Dynamic Power Consumption [nW/MHz]					
Input Transition [ns]		0.01		4.00	
Load Capacitance [fF]	5.00	100.00	5.00	100.00	
CP to Q	fall	244.10	241.45	711.72	841.11
	rise	219.04	222.00	700.53	856.69
CP to QN	fall	219.04	222.00	700.53	856.69
	rise	244.10	241.45	711.72	841.11

Capacitance [fF]	Leakage [pW]
CP	3.5800
D	3.4160

Constraints Time [ns]			
Setup CP to D		fall	1.06
		rise	0.48
Hold CP to D		fall	0.67
		rise	0.68

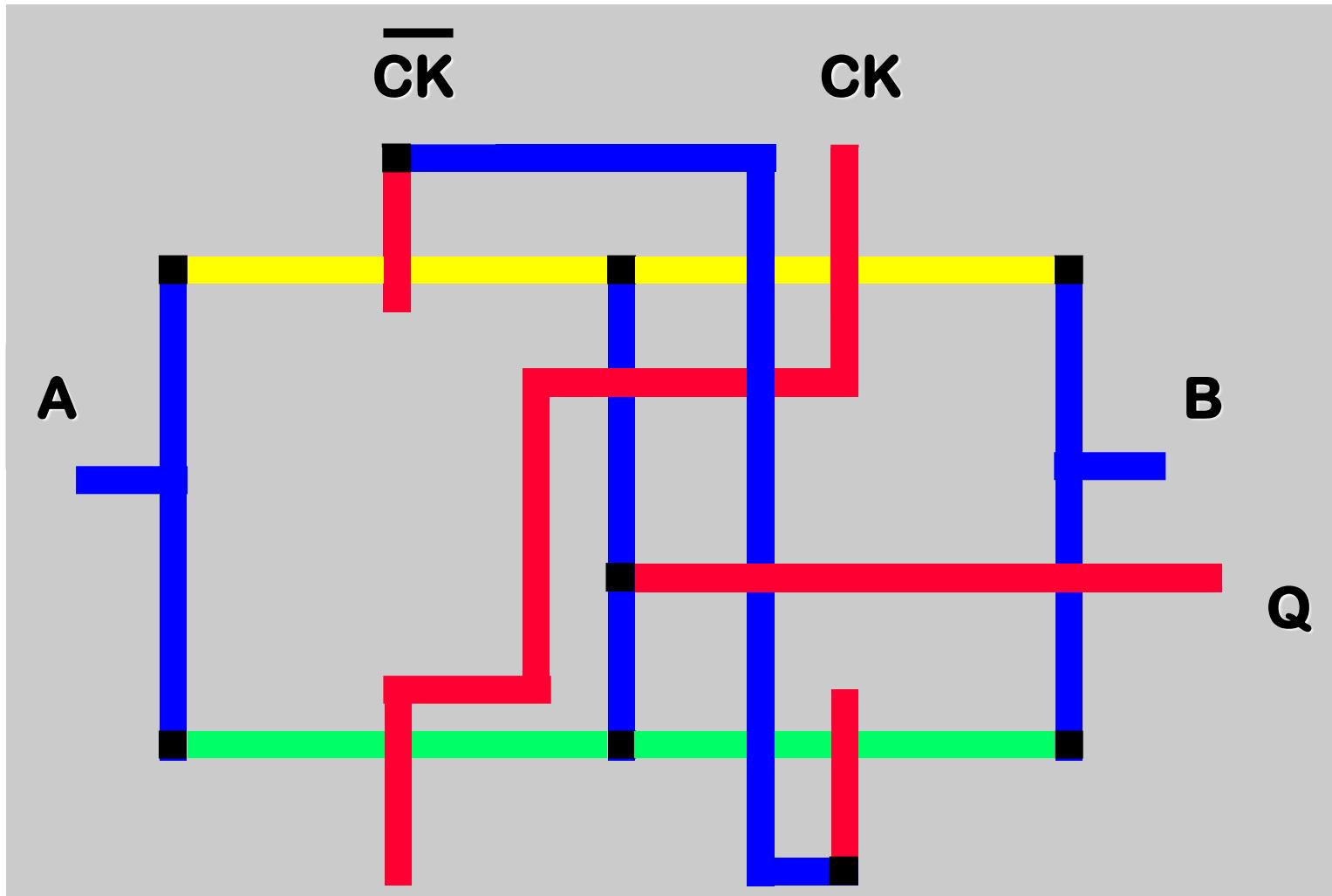
Two-ways Multiplexer



$$Q = A \cdot Ck + B \cdot \bar{Ck}$$

6 TR

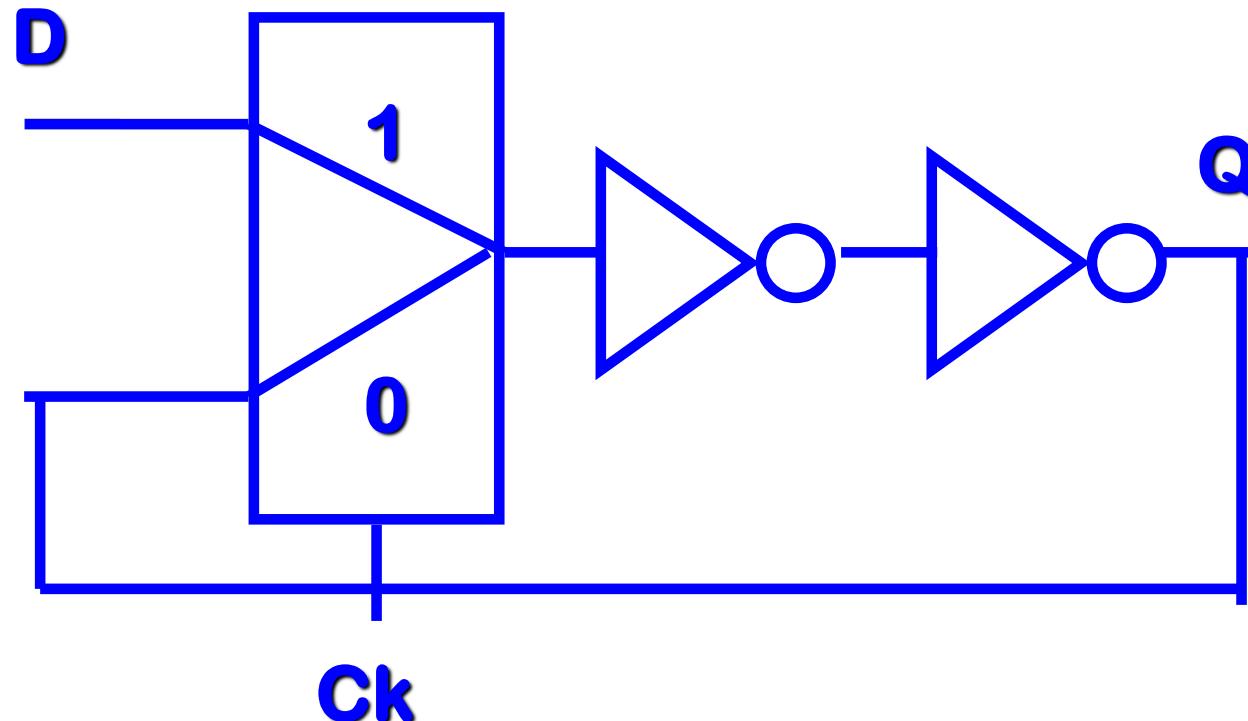
Two-ways Multiplexer



D- Latch

Positive

10 TR

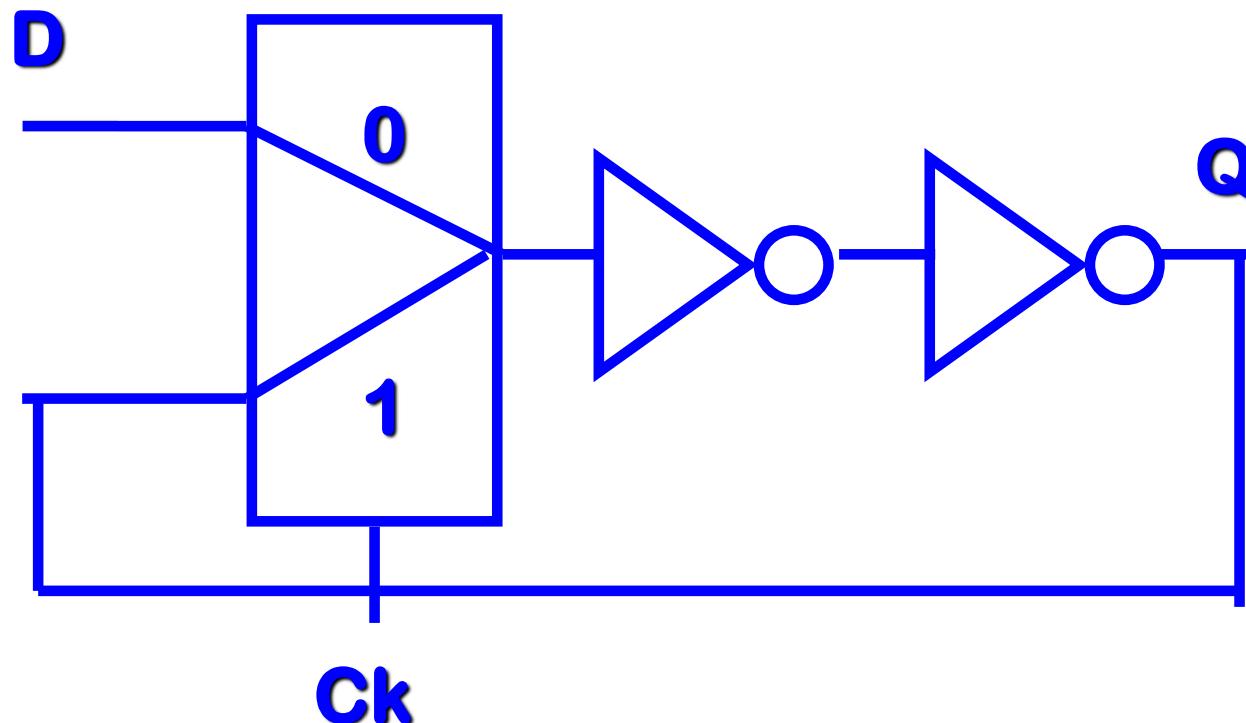


Ck=1 : Output follows the input

D- Latch

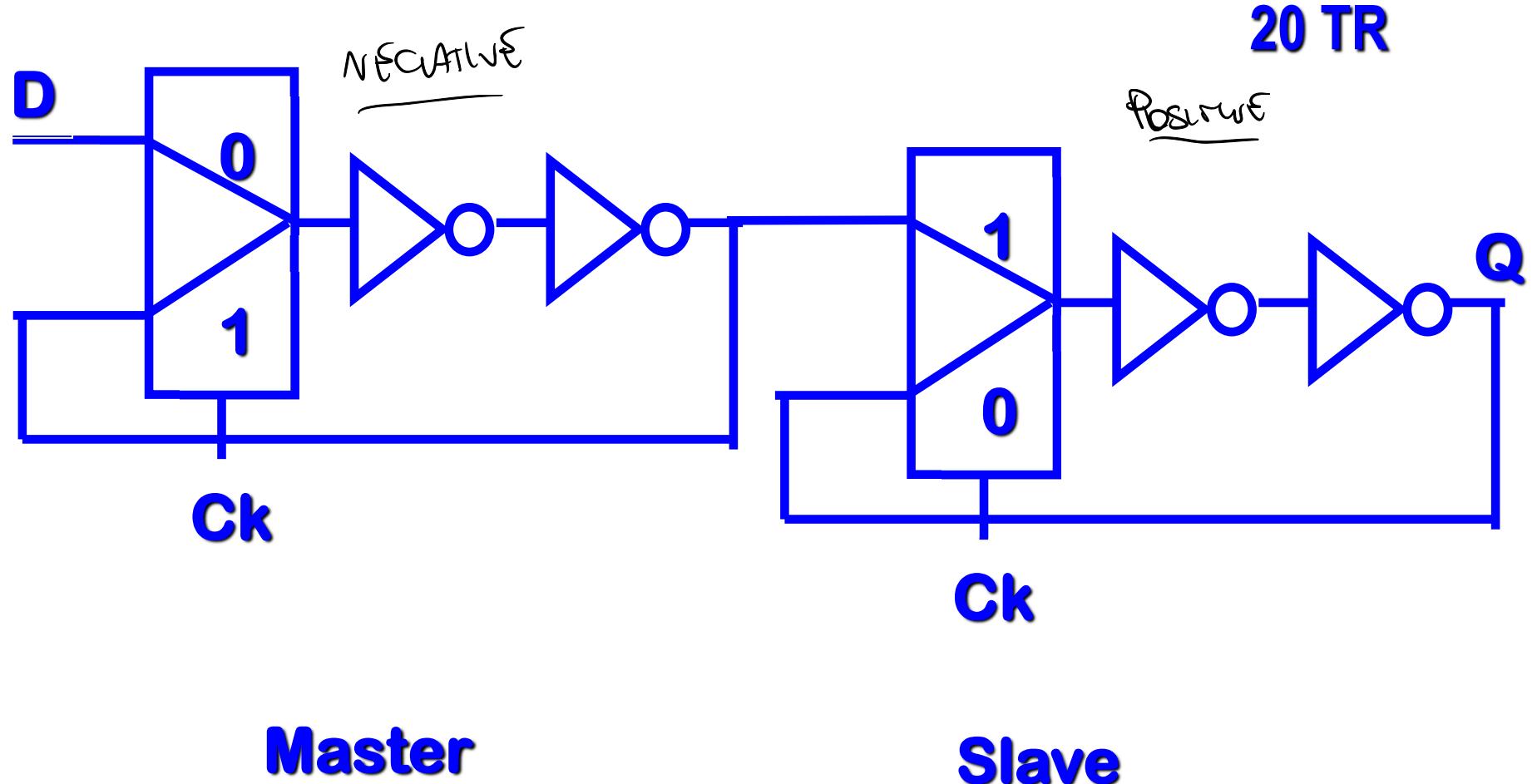
Negative

10 TR

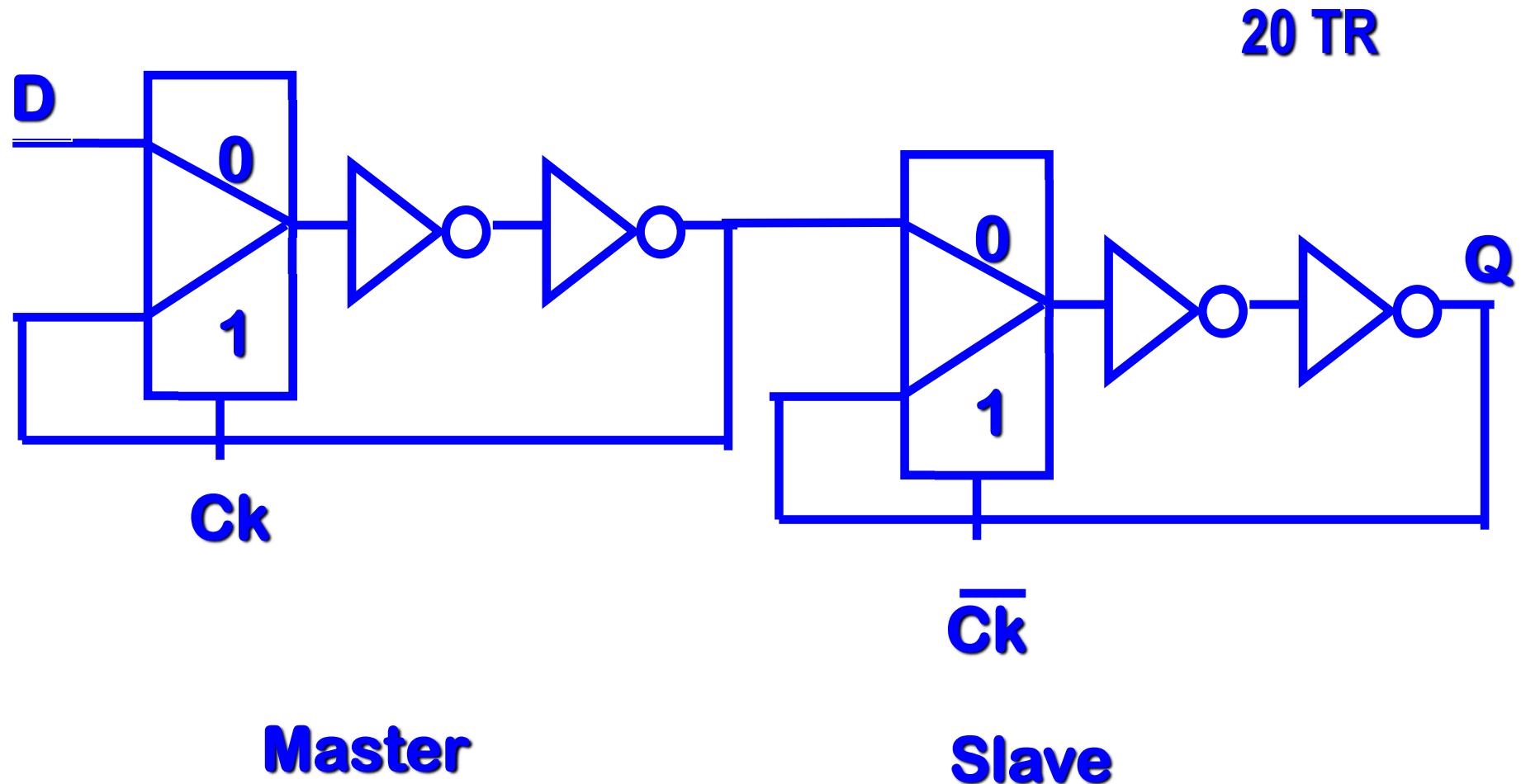


Ck=0 : Output follows the input

Positive D- edge triggered



Positive D- edge triggered



Positive D- edge triggered

Complexity trade-off (# of transistors)

FF SR (NAND2)

FF SR (NOR2)

MUX

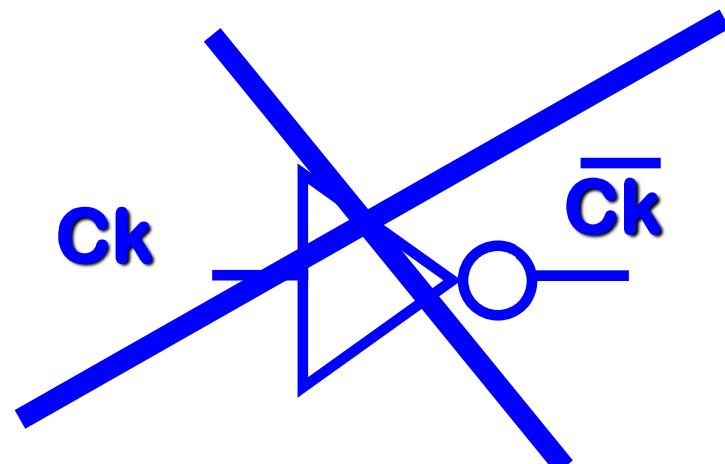
34

26

20

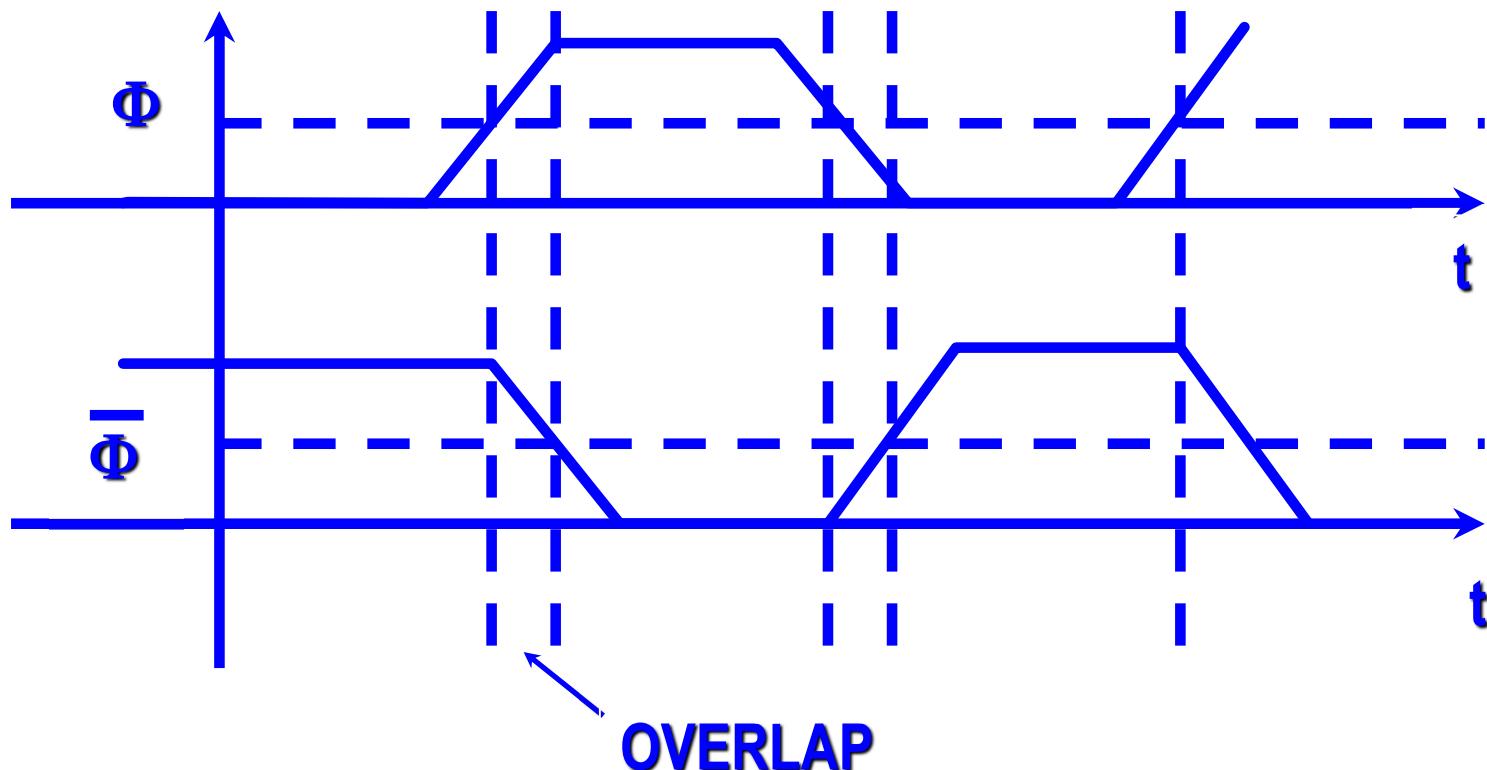
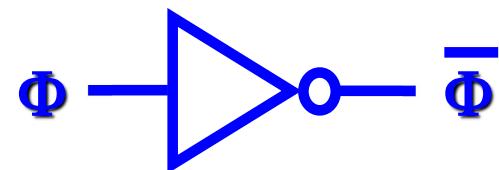
Clock Signal

- ❖ Non transparent conditions has to be guaranteed
- ❖ CK and \bar{CK} never equal to logic 1 at the same time
- ❖ inverter Solution is not valid
- ❖ Let's see with a linear delay model for the inverter



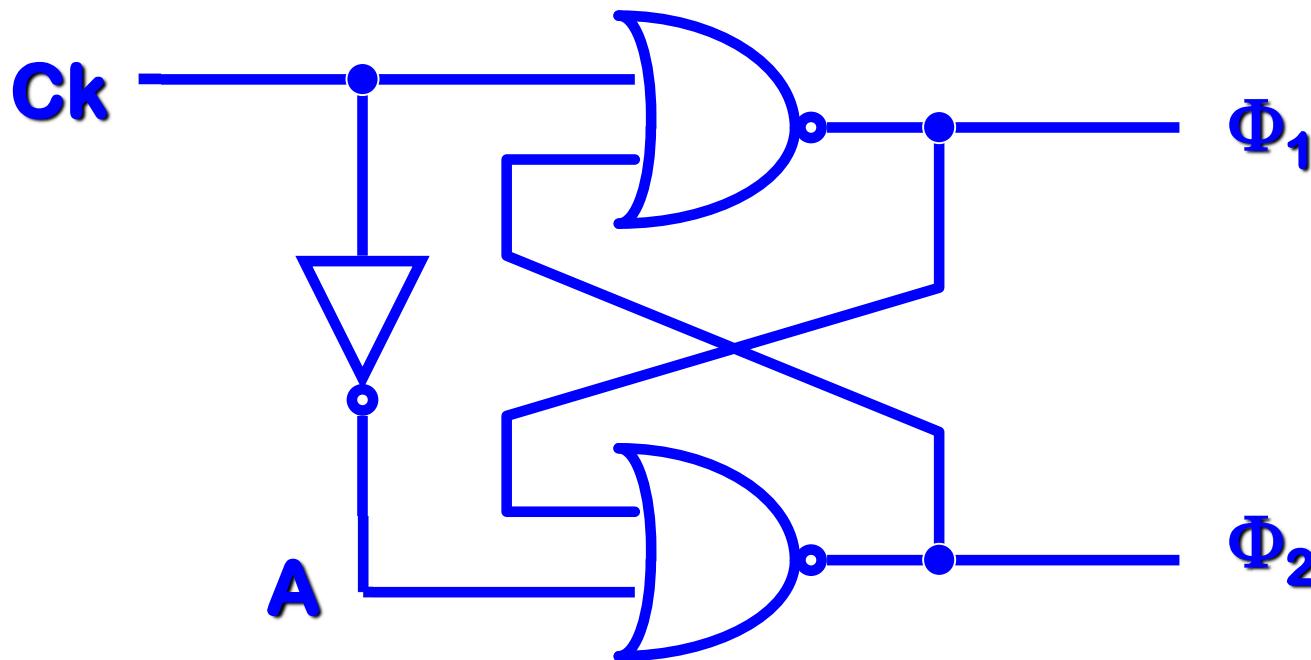
Clock Generator with an inverter

❖ Not valid solution



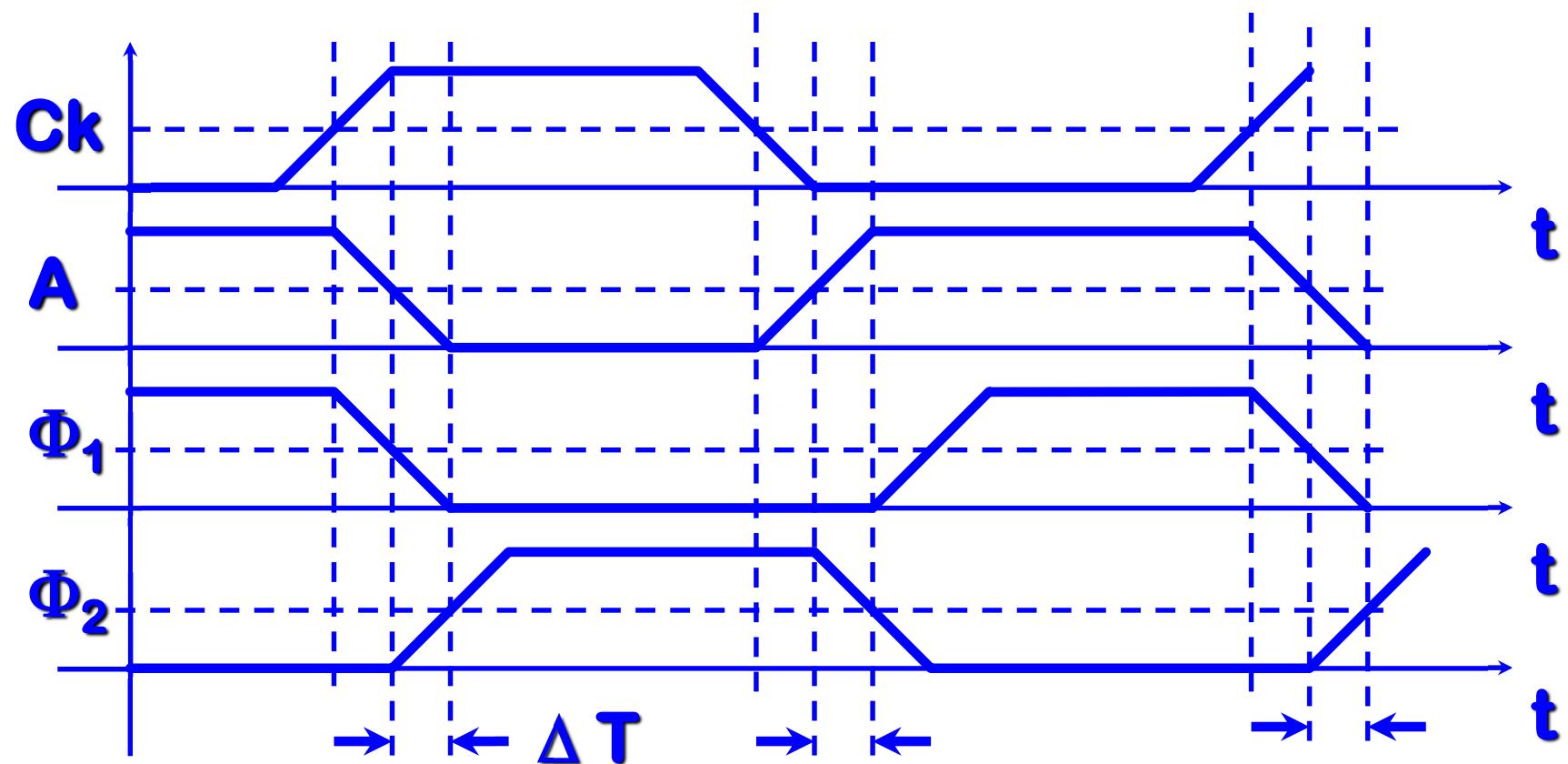
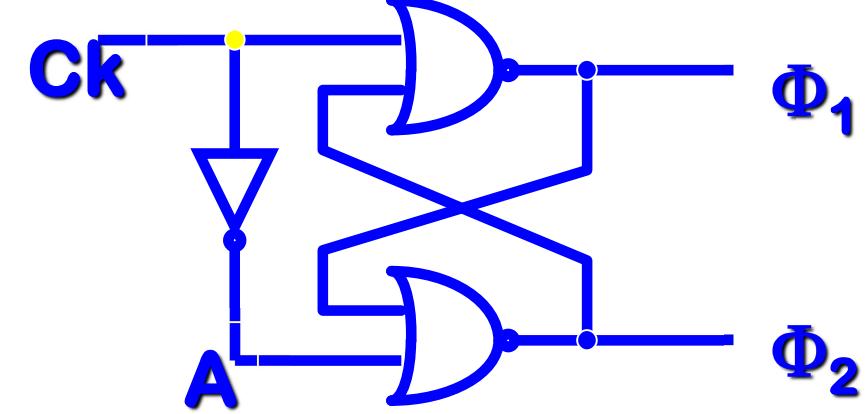
Two-phases Clock Generation

- ❖ Φ and $\bar{\Phi}$ are not derived from an inverter
- ❖ Two signals are defined: Φ_1 and Φ_2



A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

Waveforms

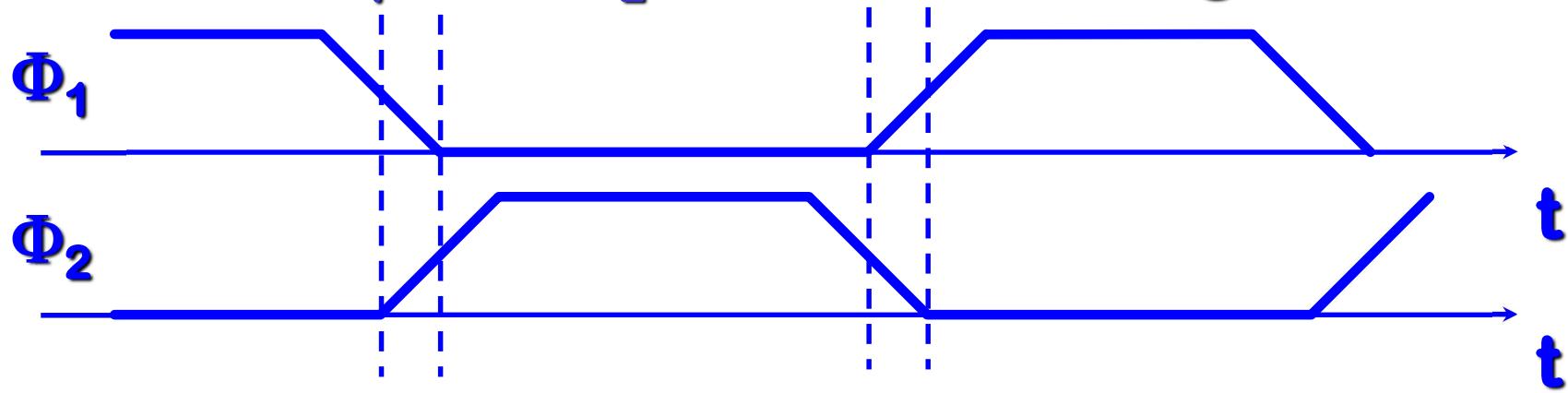


Notes on Clock Generation

- ❖ **Not overlapped condition is maintained also when driving high value capacitance**
- ❖ **NOR gates could be sized in order to provide the required buffering**

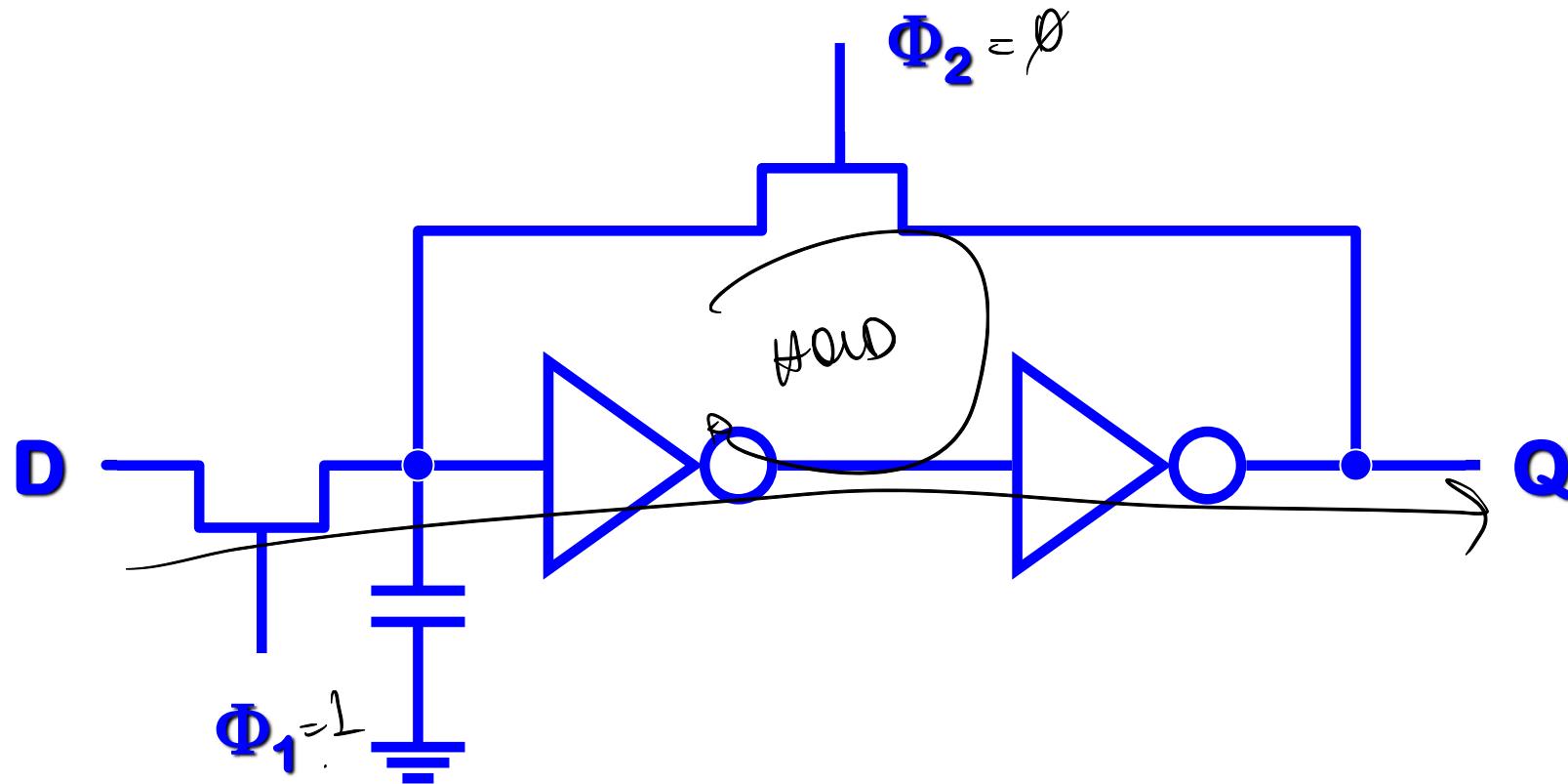
Static Flip - Flop

- ✧ Analyzed Flip – Flop solution are complex
- ✧ They do not rely on high impedance of MOS input
- ✧ There is an interval when both Φ_1 and Φ_2 are at the low logic level
- ✧ MOS input capacitance could store the data when both Φ_1 and Φ_2 are at the low logic level

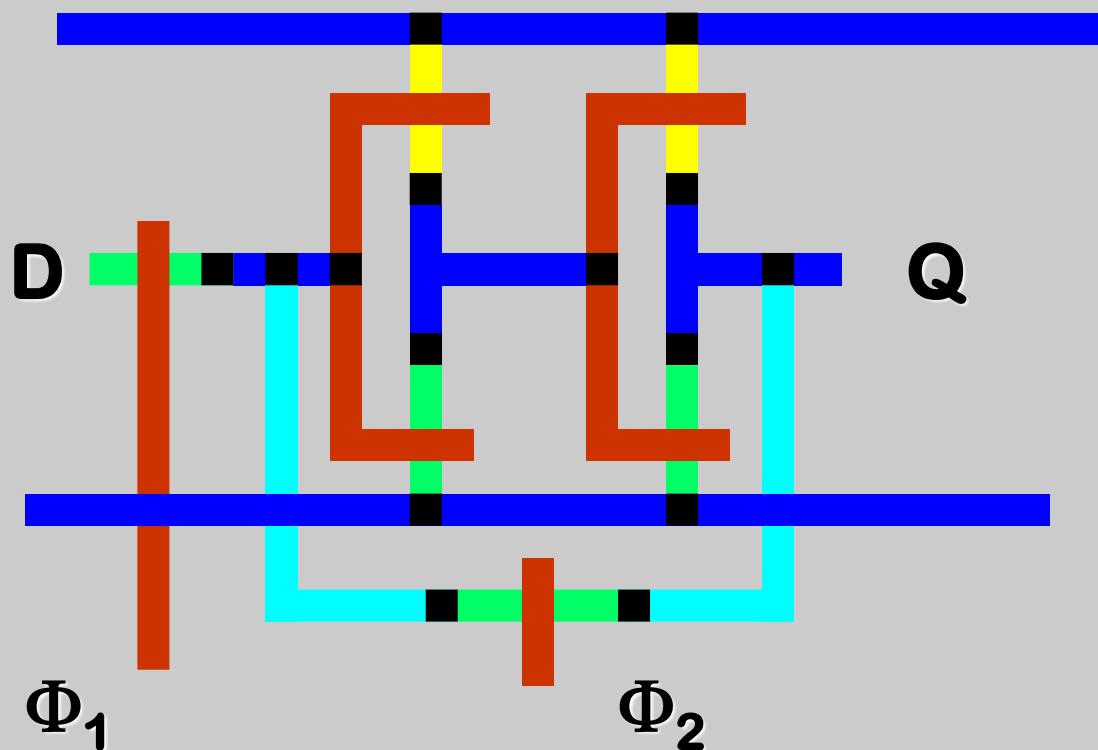


Transparent D-Latch

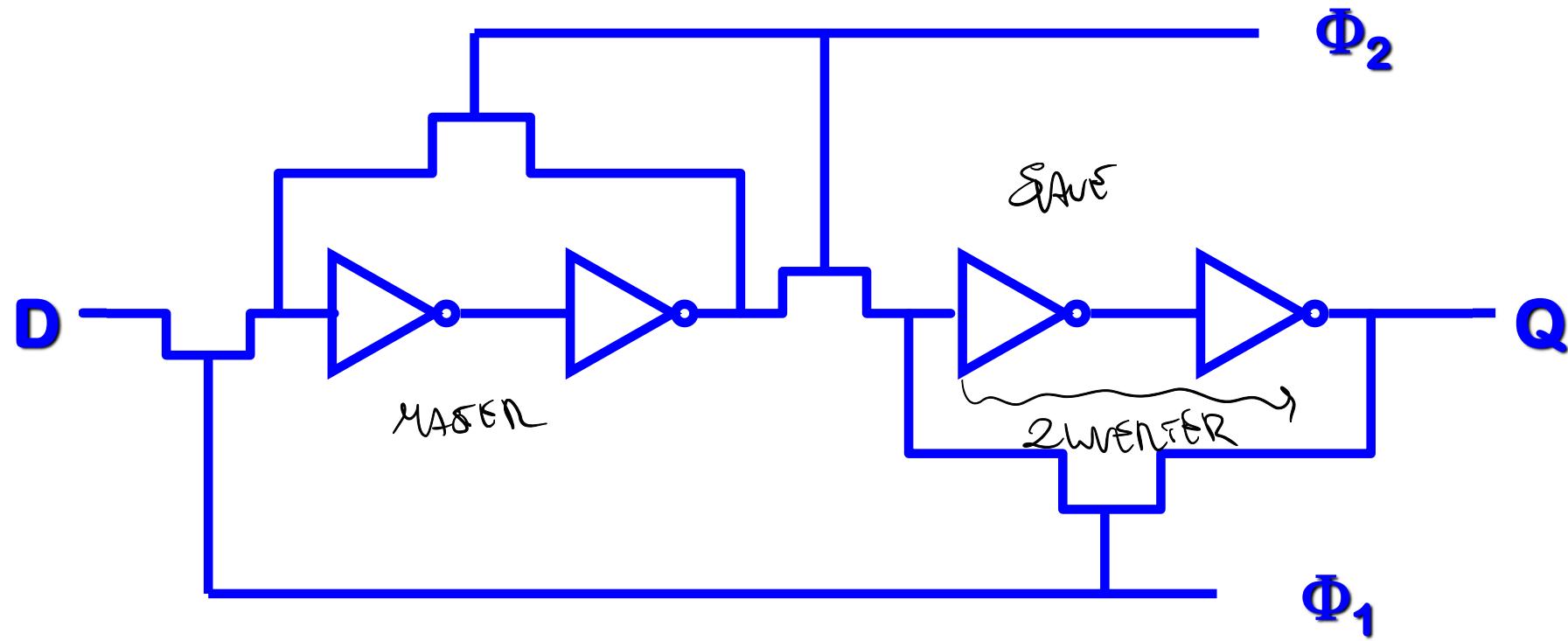
★ Pass Transistor based



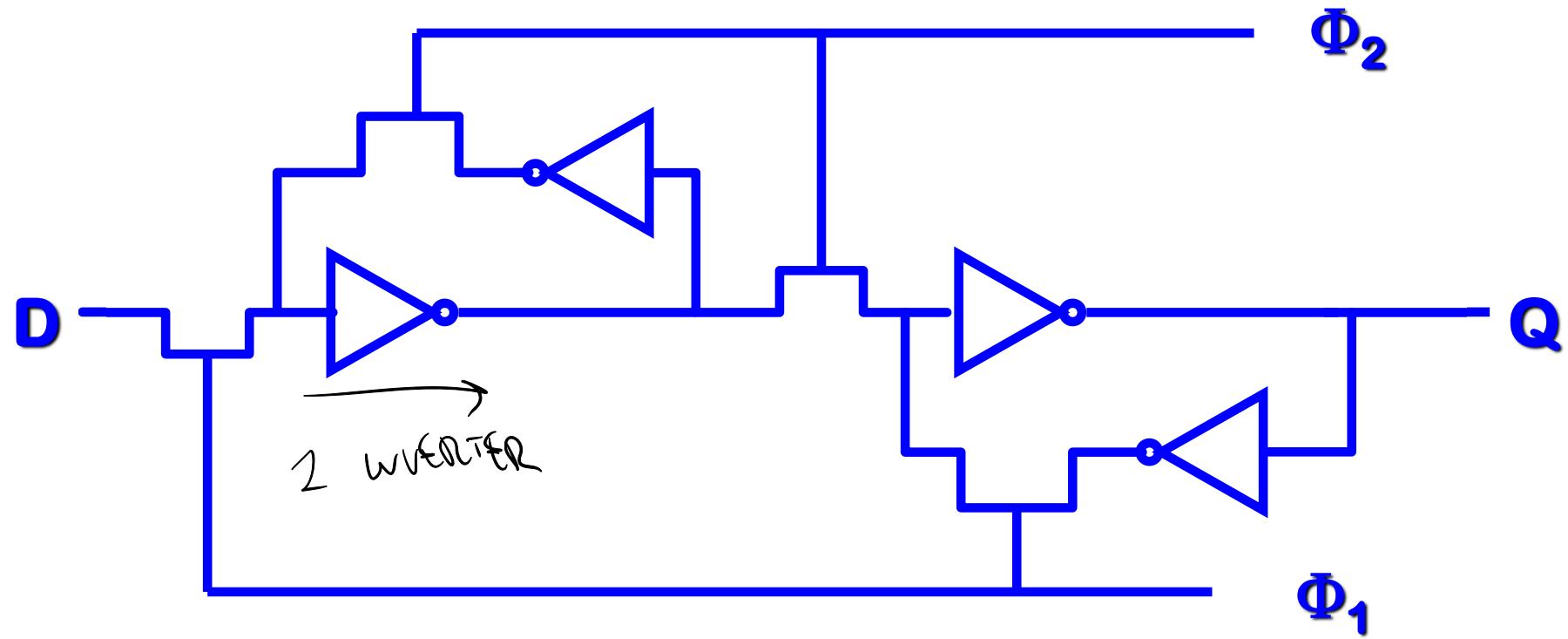
Stick diagram



Flip - Flop D Edge Triggered

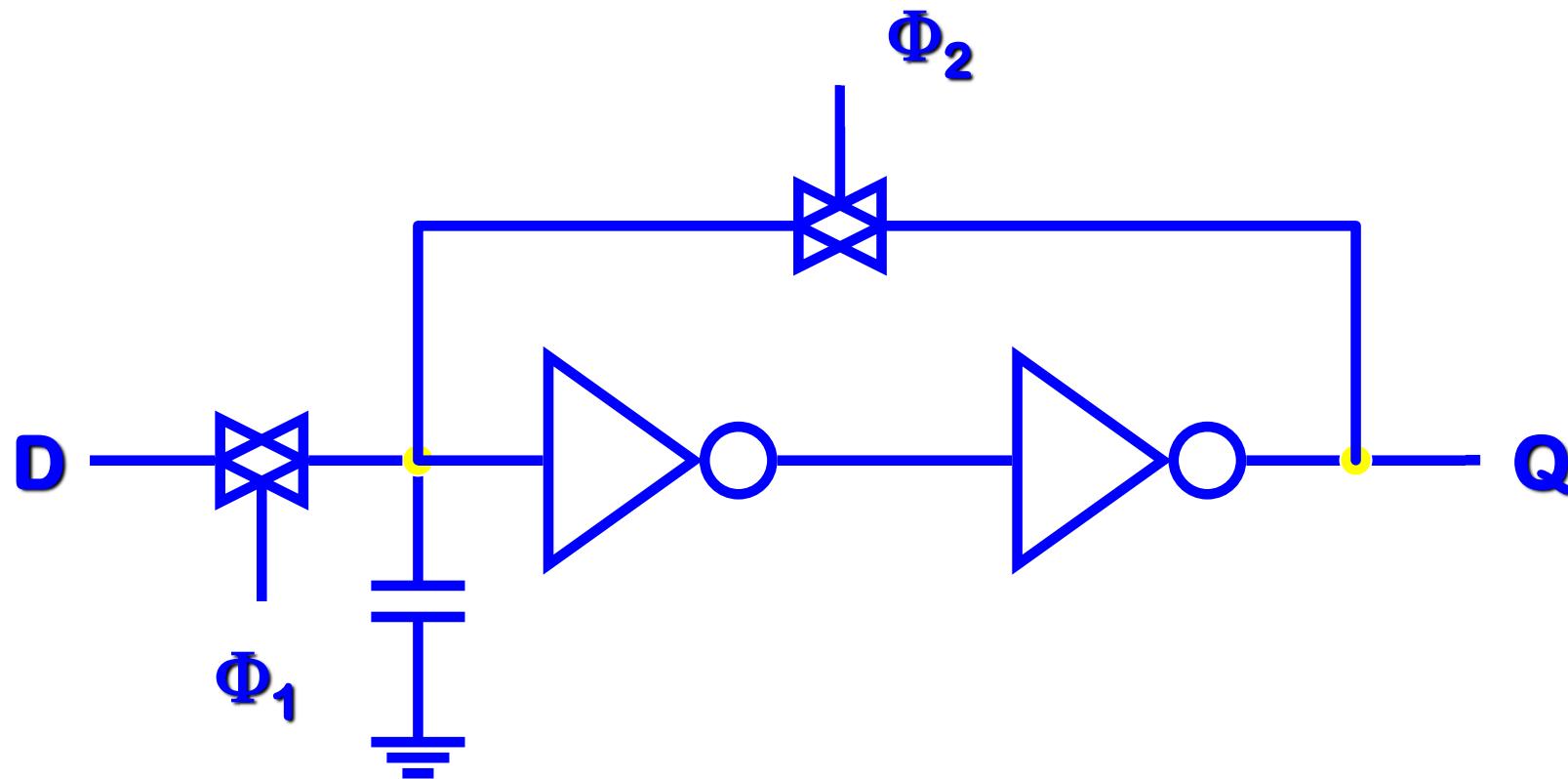


Delay Optimization



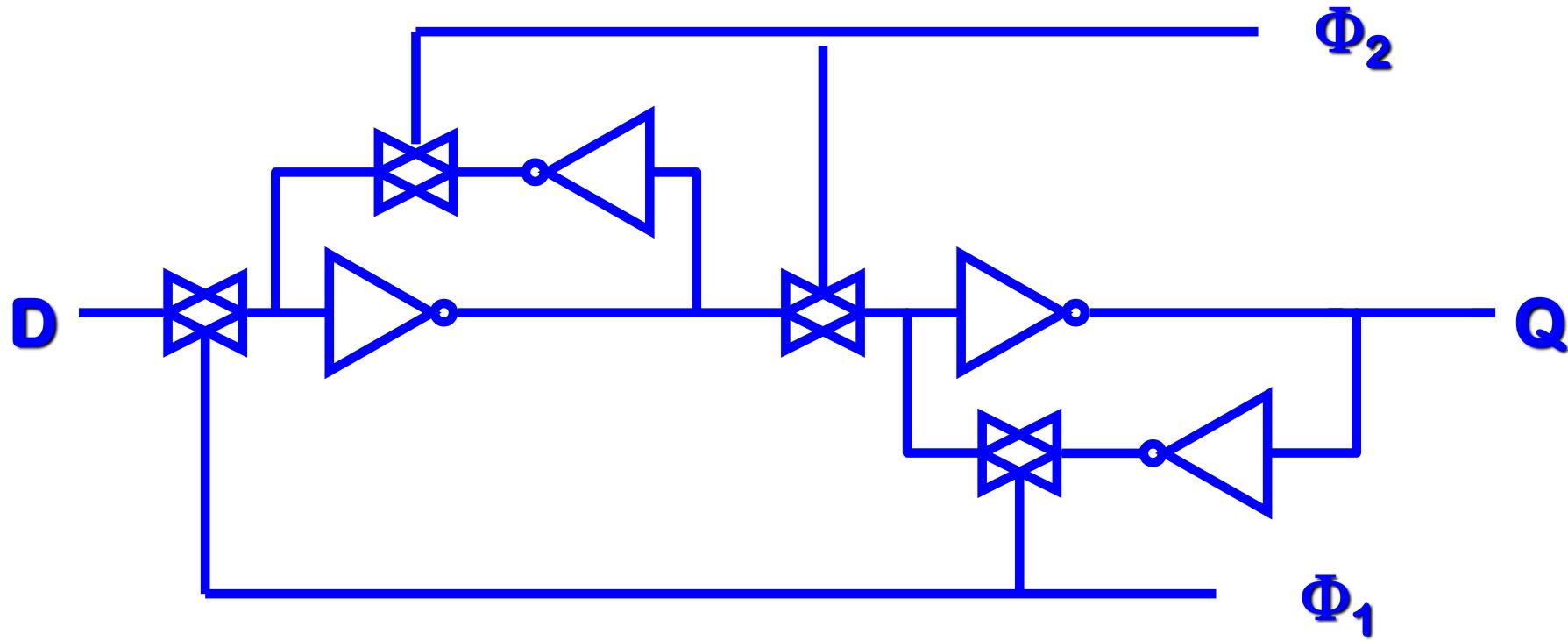
Transparent D-Latch with Pass Gate

❖ Only positive signals are shown



Flip - Flop D Edge Triggered with Pass Gate

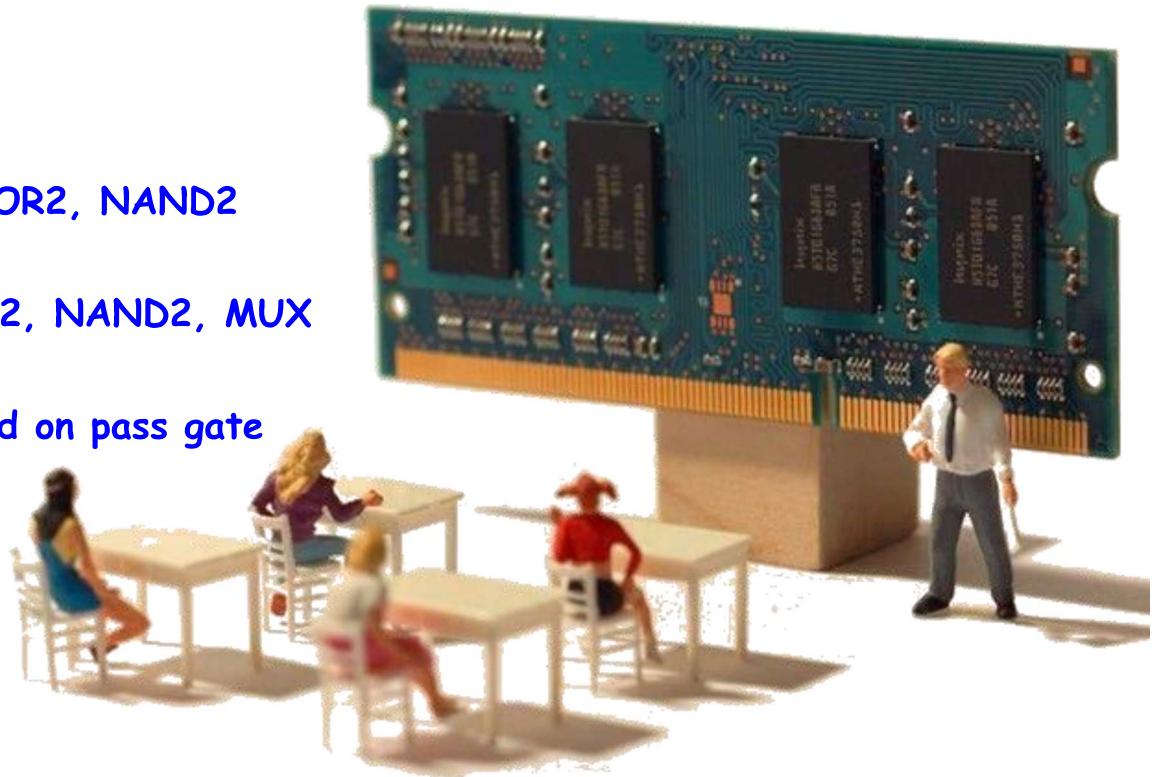
❖ 16 transistors



End, Questions ?

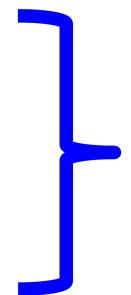
- Flip Flop: Static Solution

- Flip- Flop S-R: NOR2 e NAND2
- Flip-Flop S-R with enable
- D -Latch
- Flip Flop S-R Edge Triggered: NOR2, NAND2
- Flip Flop D Edge Triggered: NOR2, NAND2, MUX
- Flip Flop D Edge Triggered based on pass gate



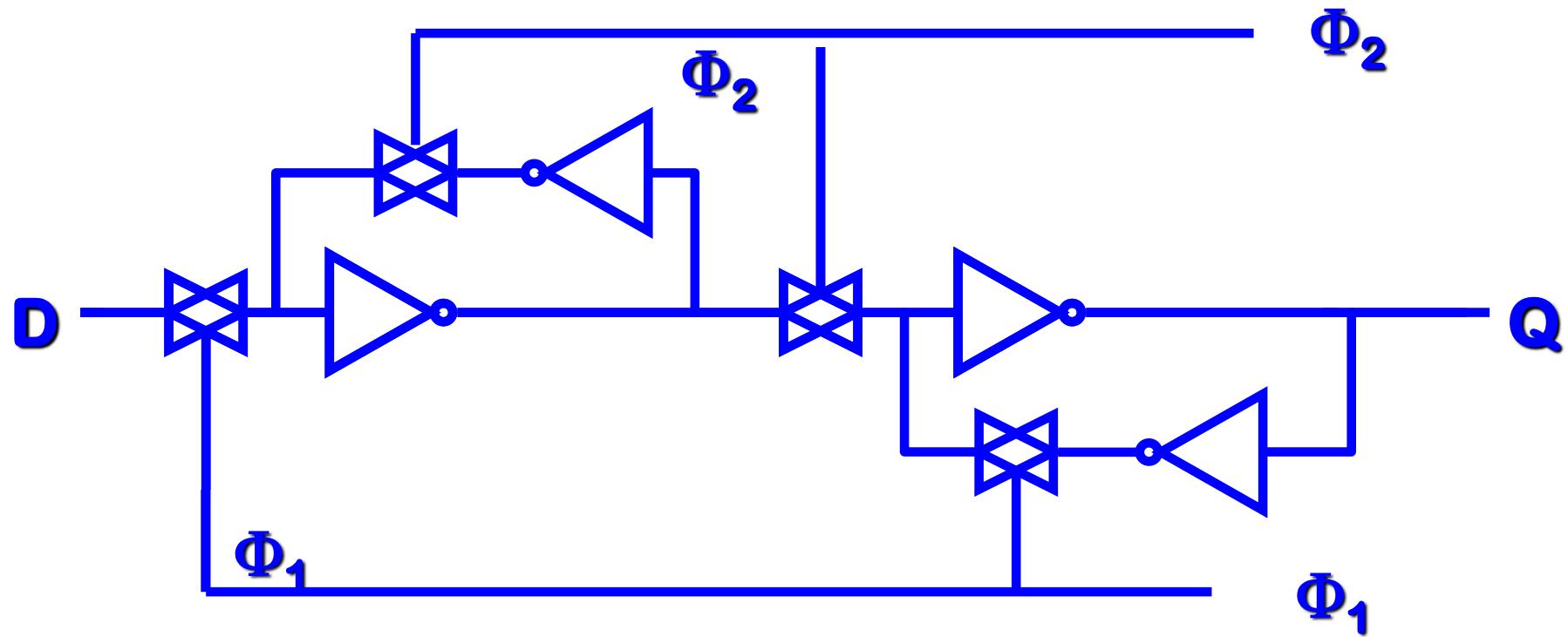
Dynamic Flip - Flop

- ❖ **Clock is always running**
- ❖ **Reduced MOS Sizes**
- ❖ **Reduced net lenght**



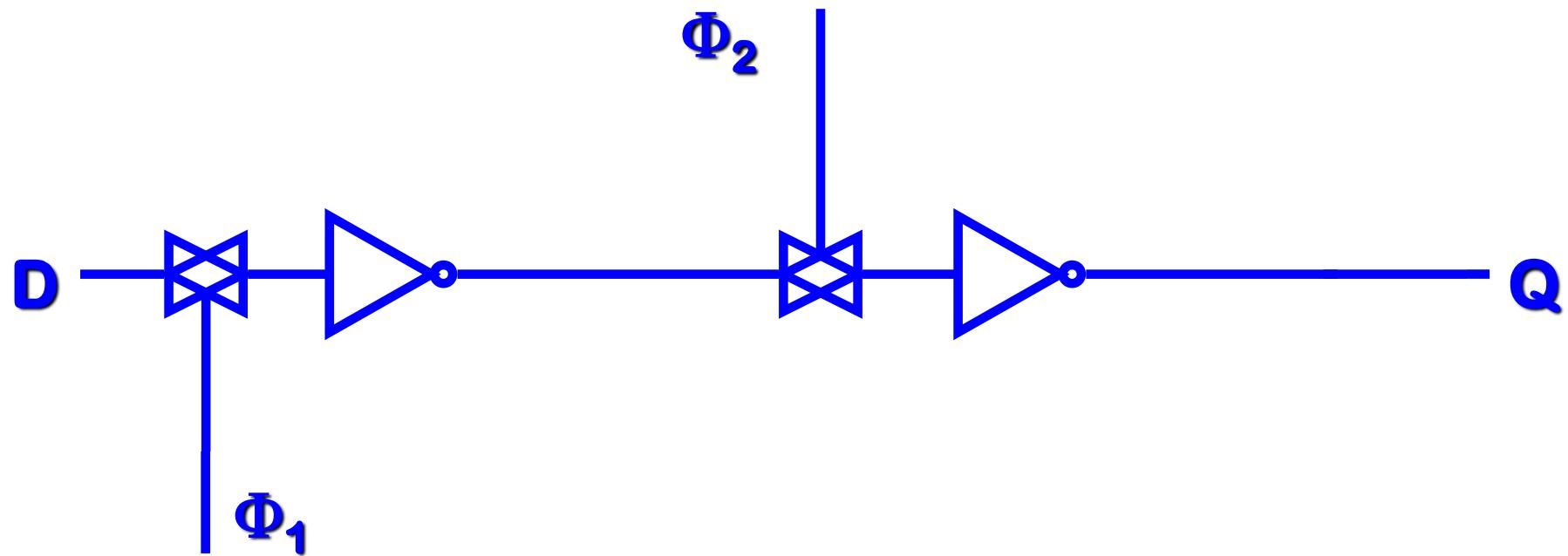
Greater Speed

Flip - Flop D Edge Triggered

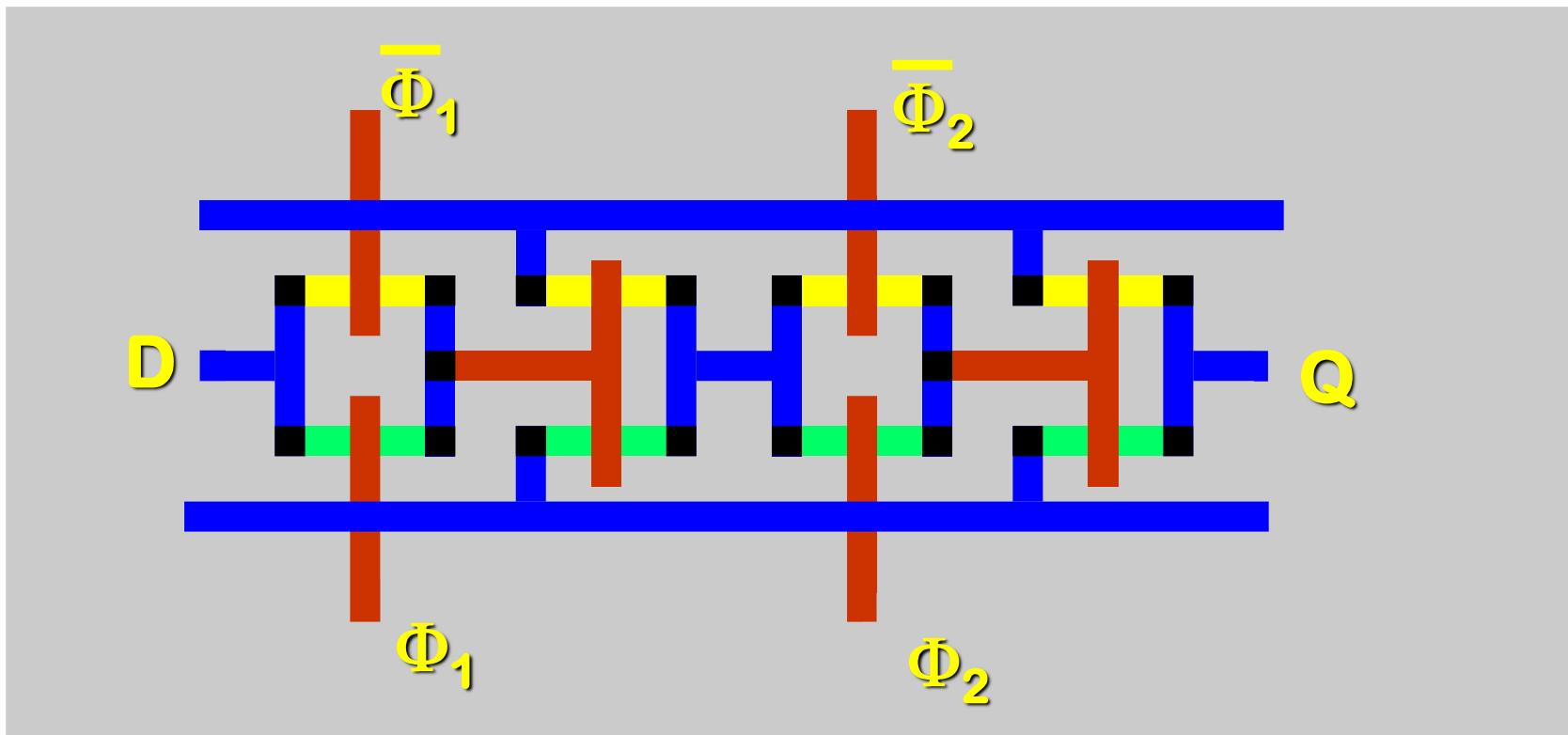


Flip - Flop D Edge Triggered

✧ 8 transistors !

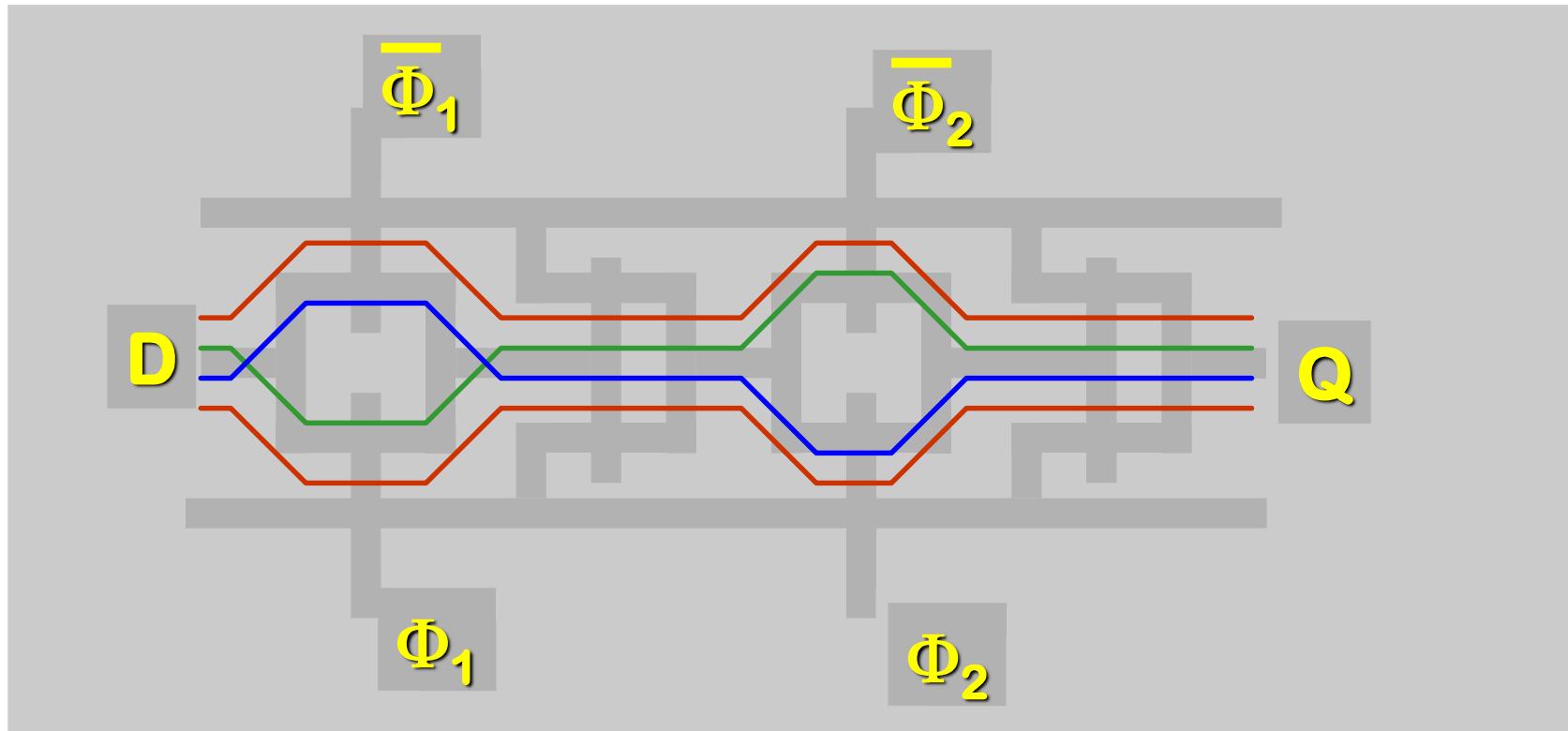


Stick Diagram



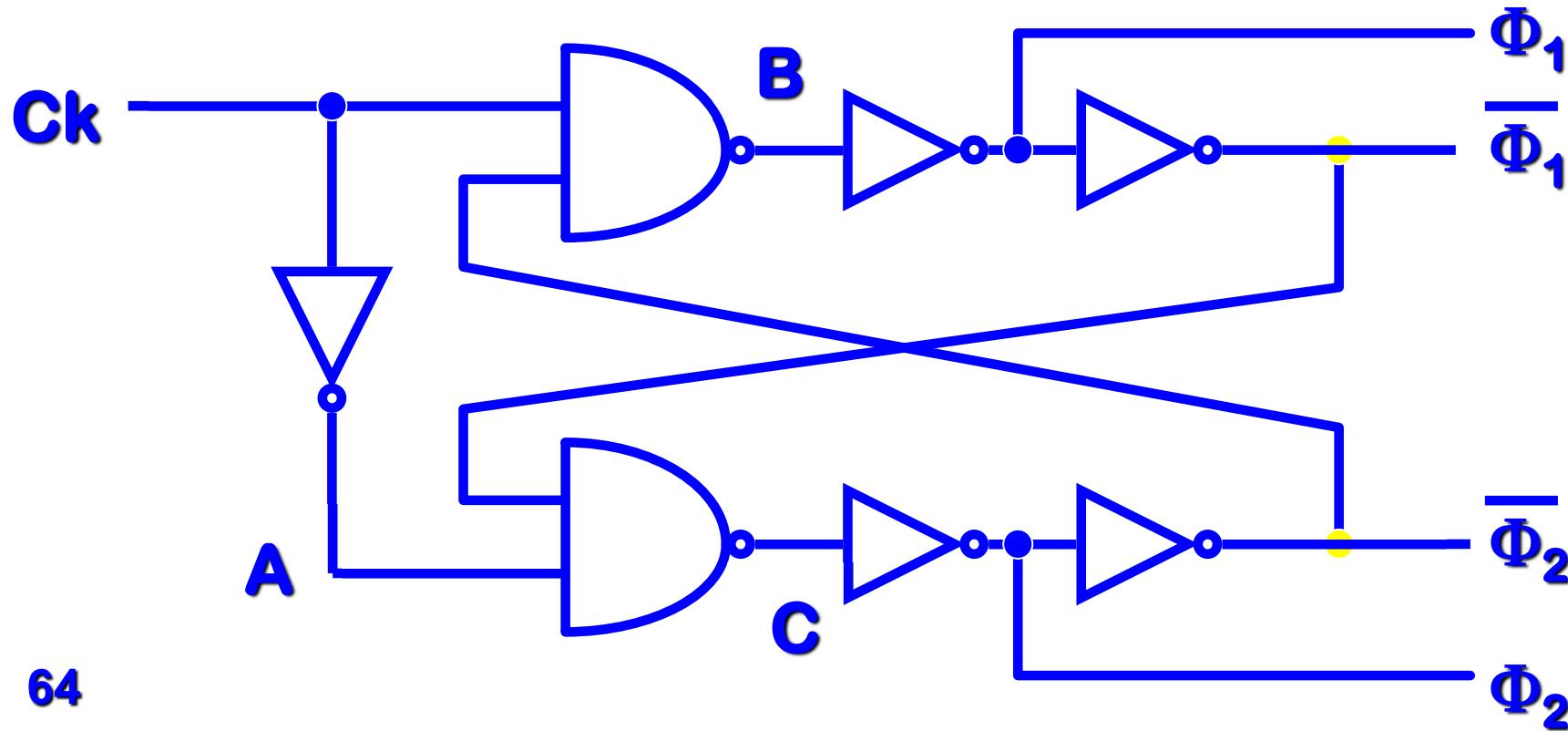
Clock Generation

❖ Possible Transparent Paths

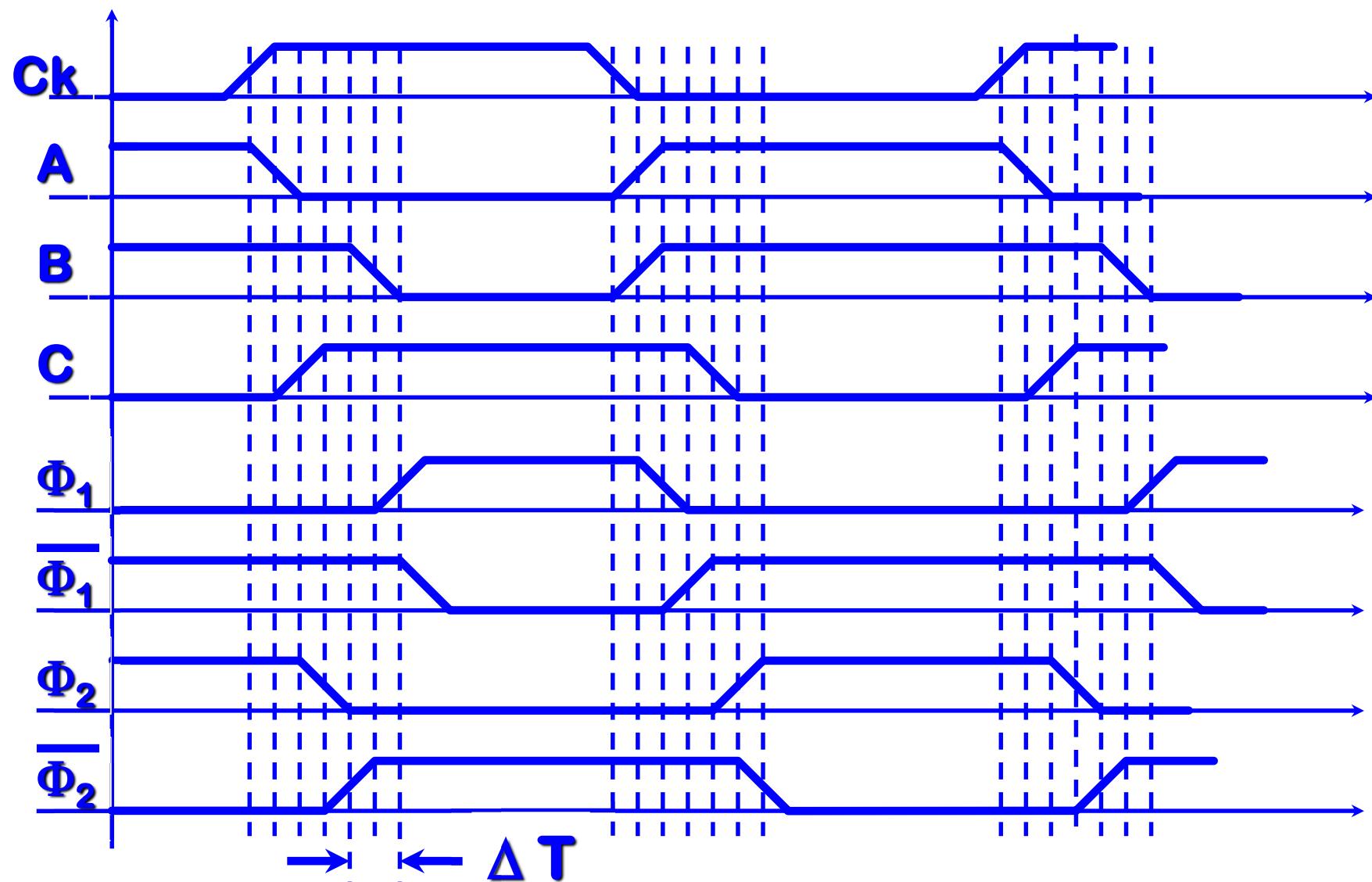


Two Phases Clock Generation for CMOS (pseudo 4 phases clock)

- ❖ Φ and $\bar{\Phi}$ are not derived by an inverter
- ❖ Two phases Clock even if 4 signals are present

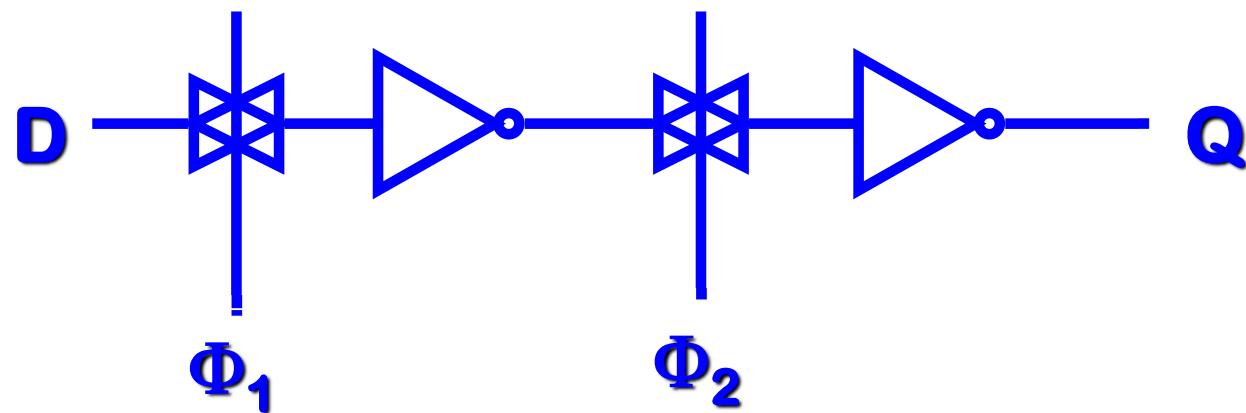


Waveforms

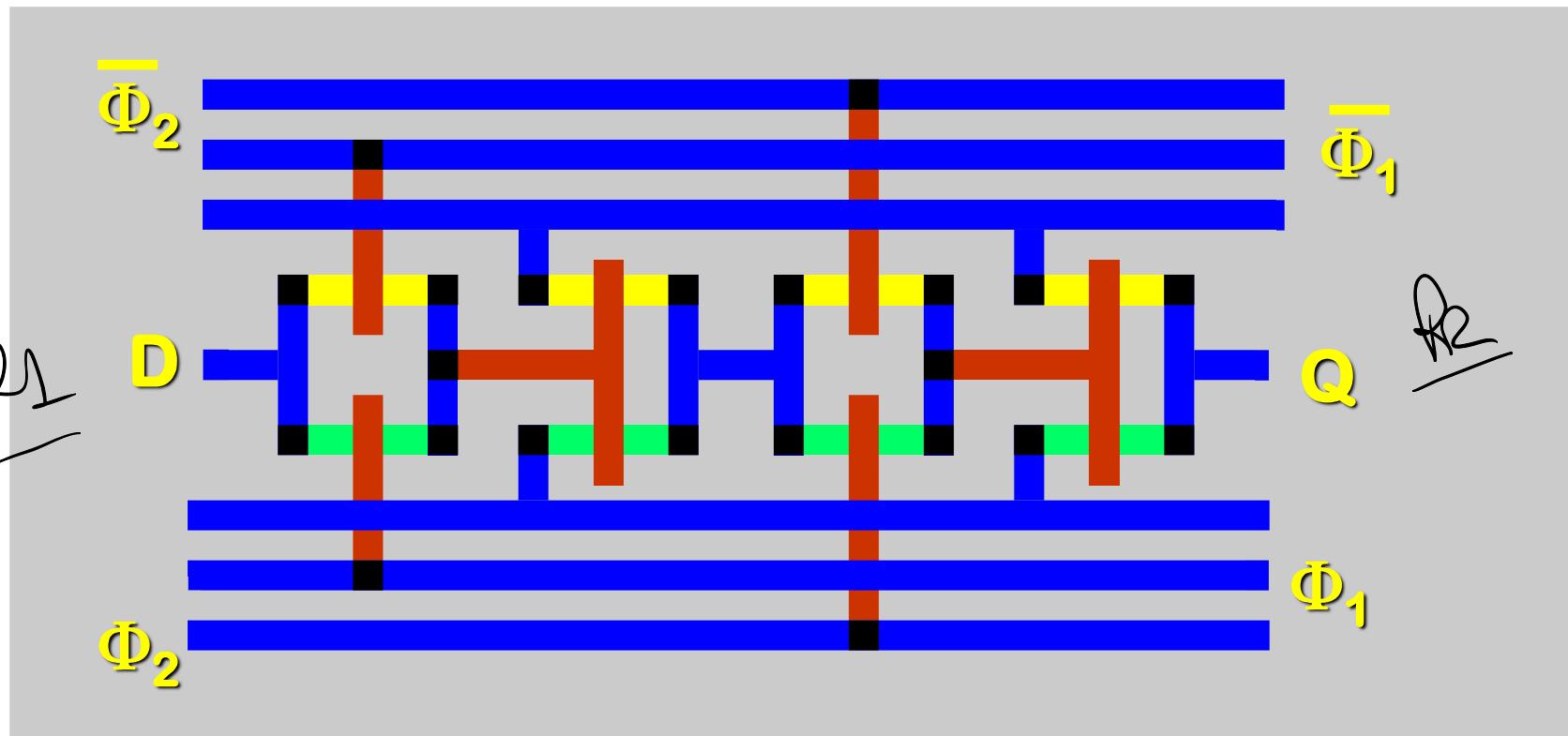


Shift Register Basic Cell

- ❖ Shift register is the basic cell in digital delay line
- ❖ It is based on a dynamic flip flop D edge-triggered



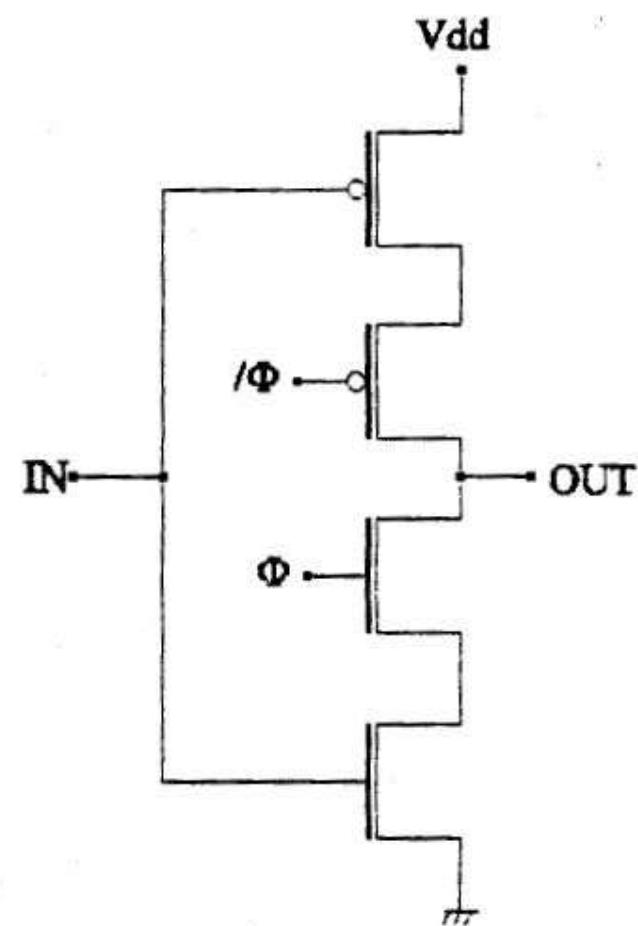
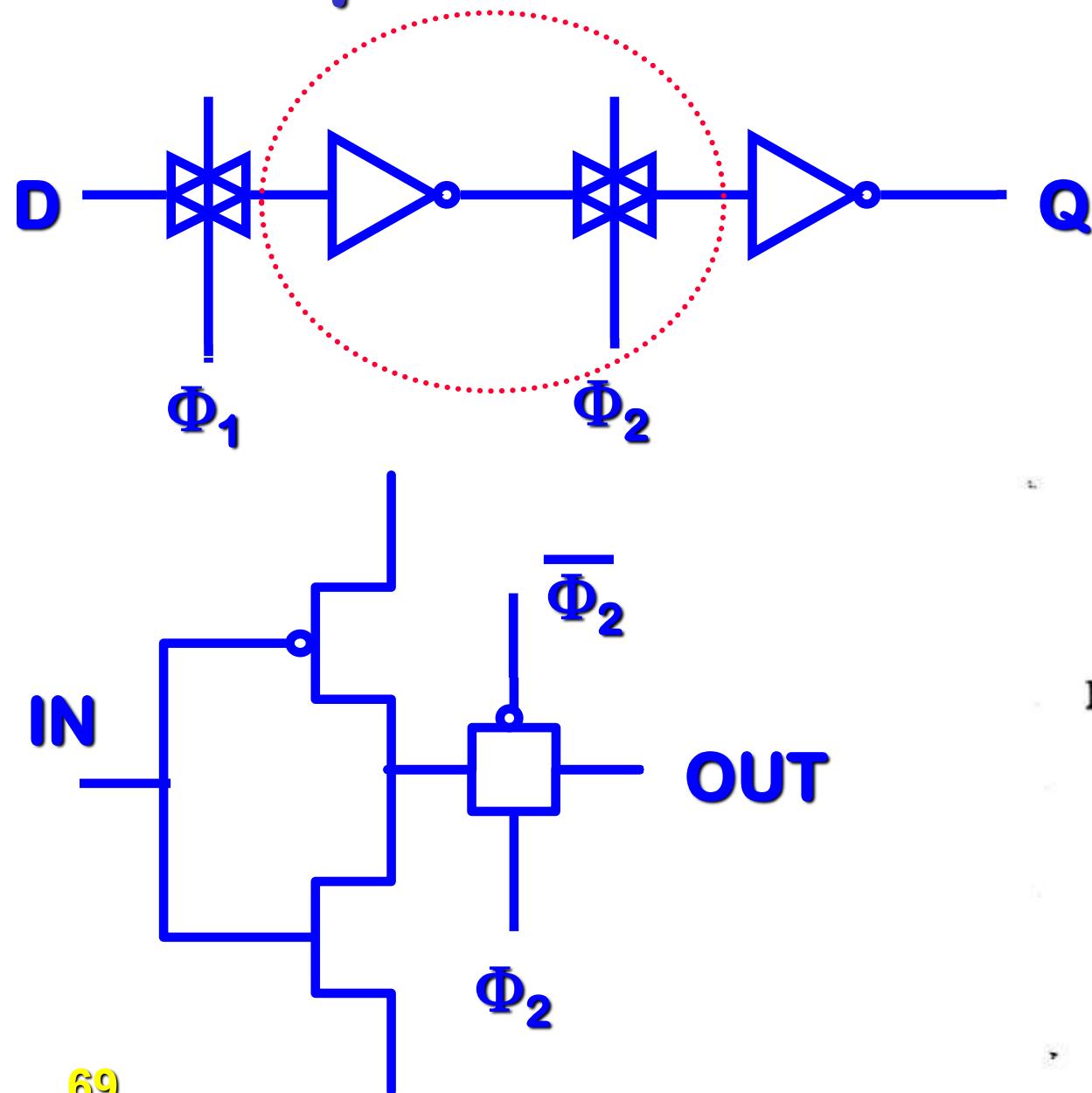
Stick Diagram



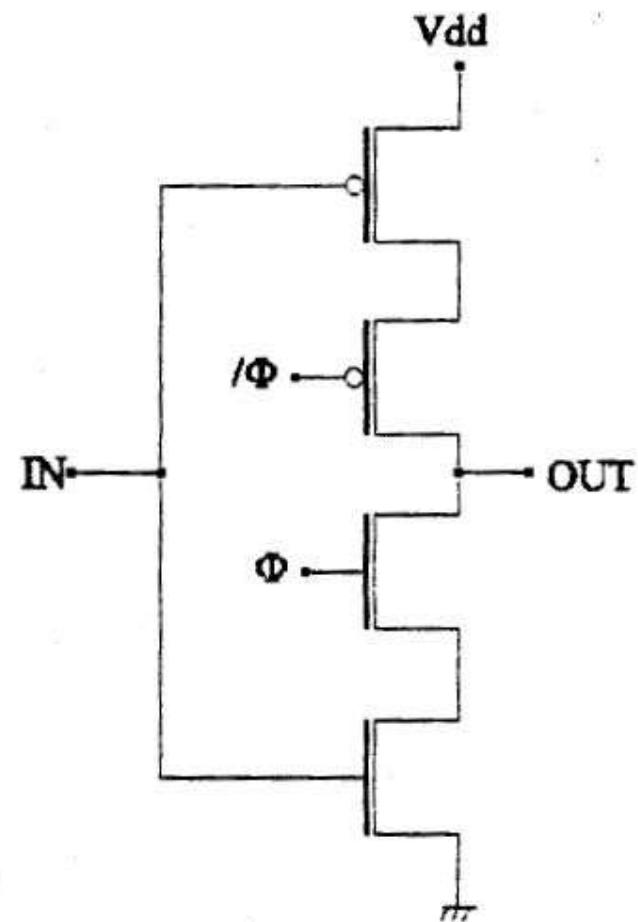
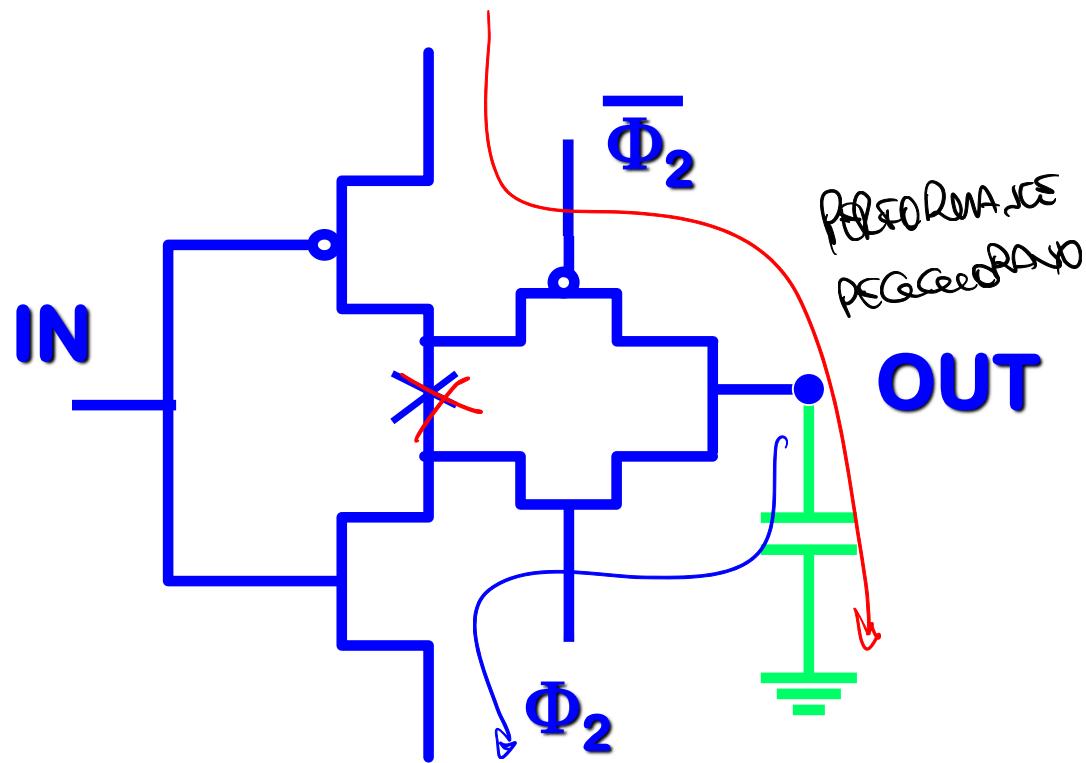
Notes on Shift Register

- ❖ **Wide spread used in digital designs**
- ❖ **Very simple structure**
- ❖ **Suitable for cell abutment**
- ❖ **Dynamic solution exploiting almost at the limit potential of selected silicon technology**

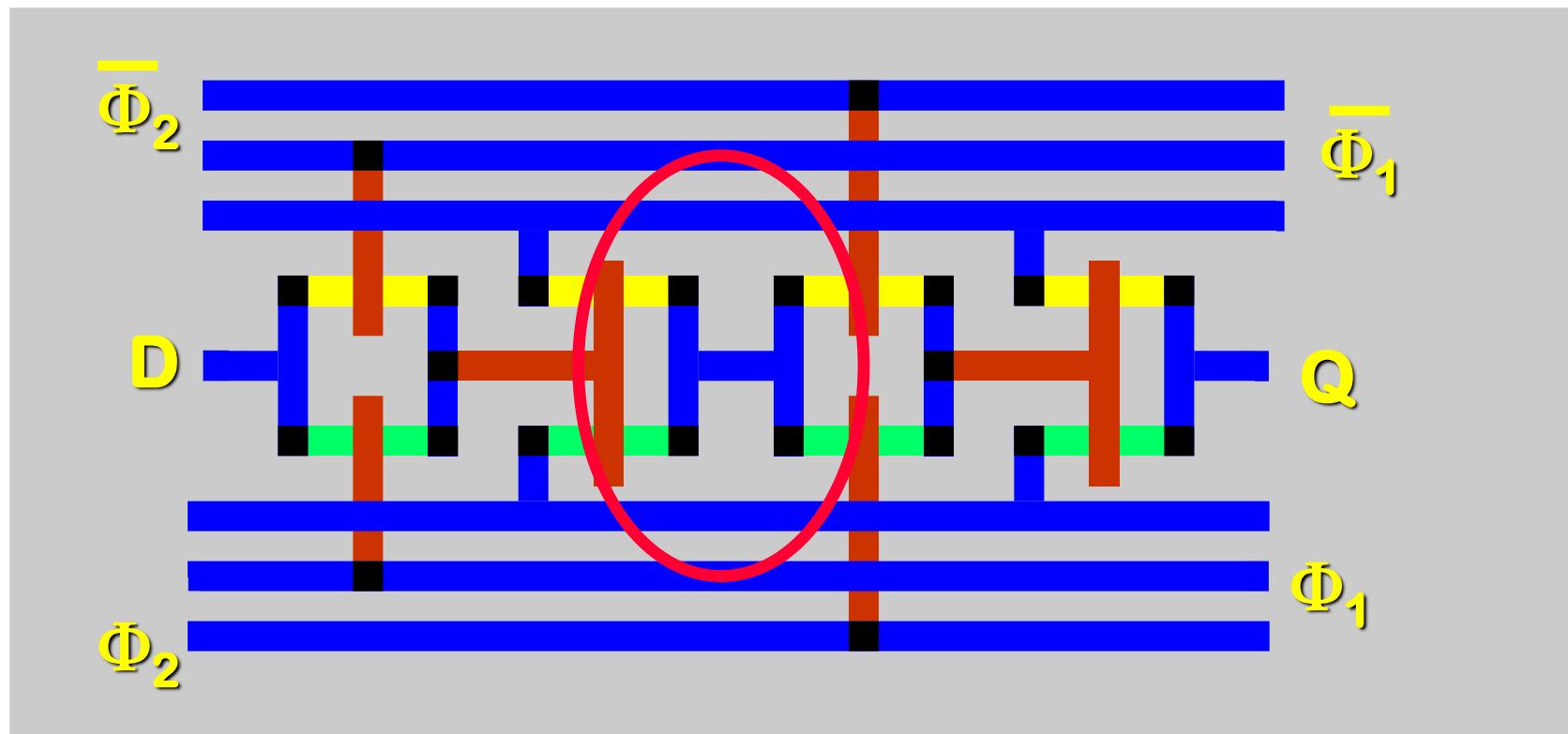
Optimization: Clocked Inverter



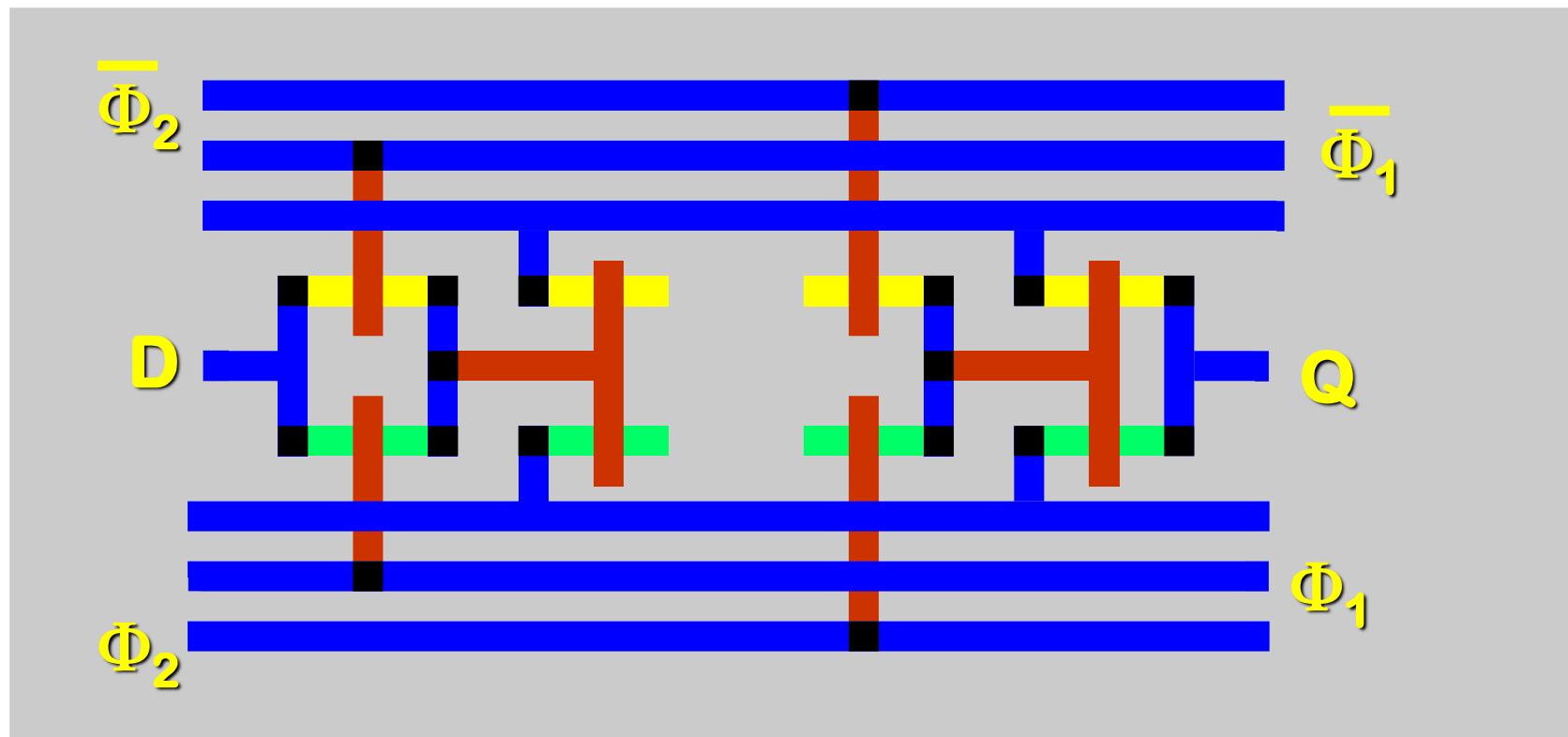
Optimization: Clocked Inverter



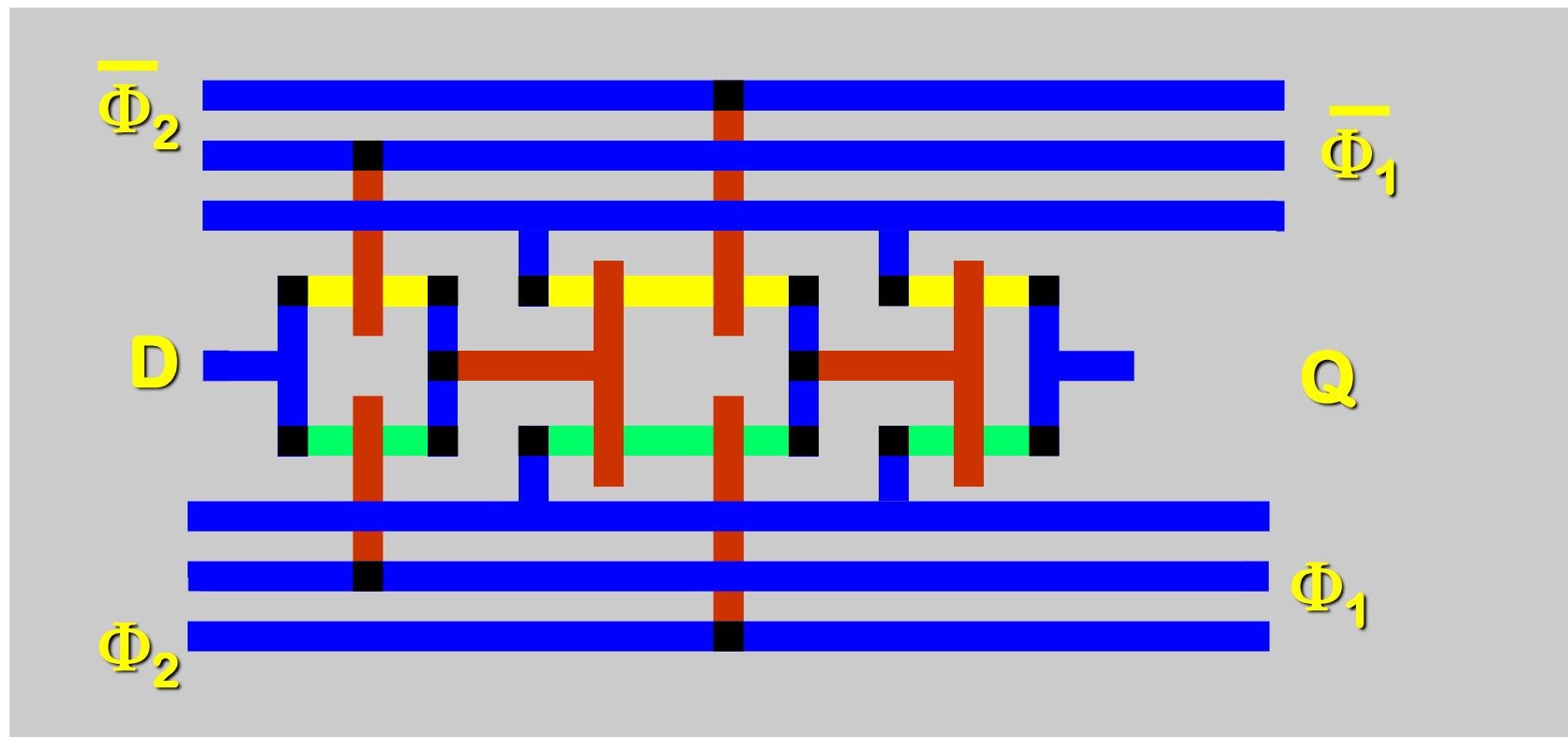
Stick Diagram



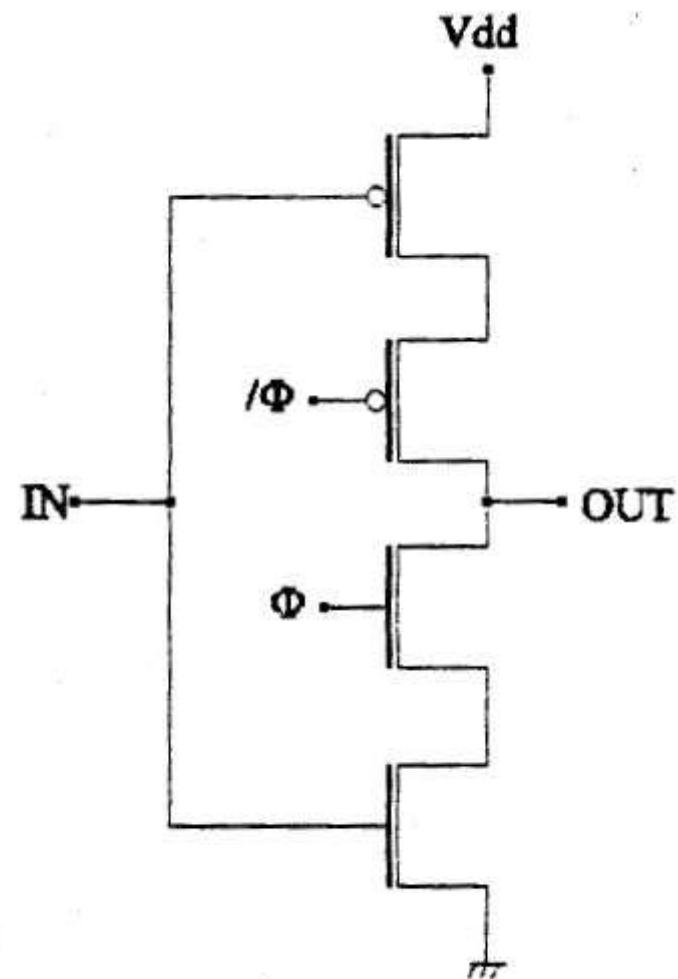
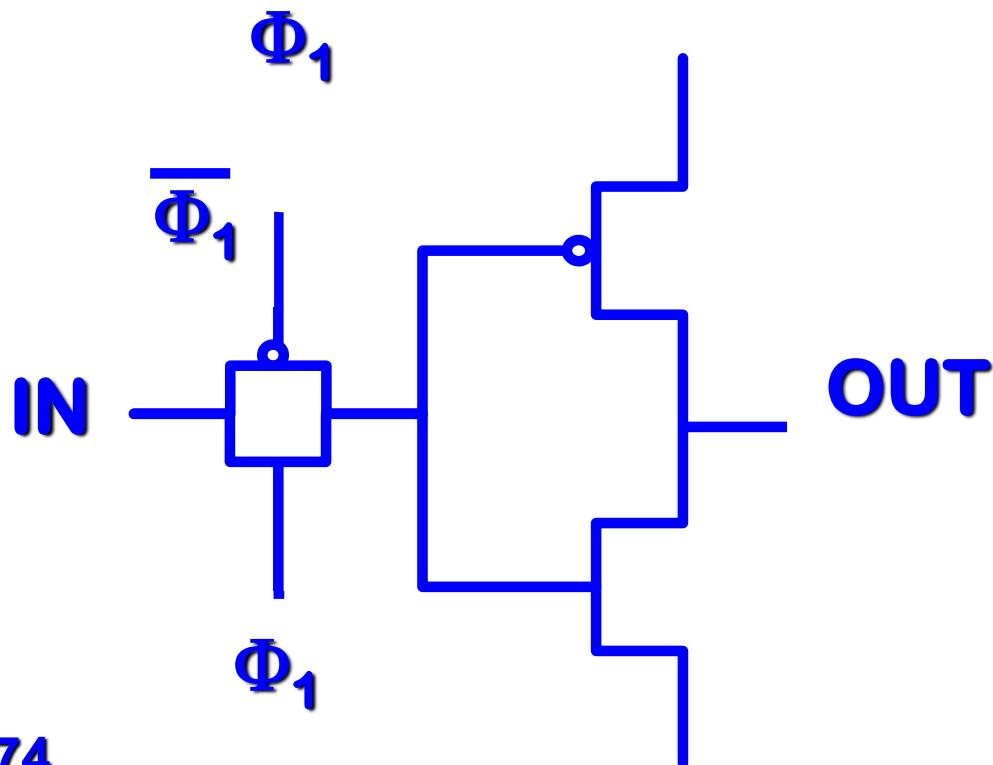
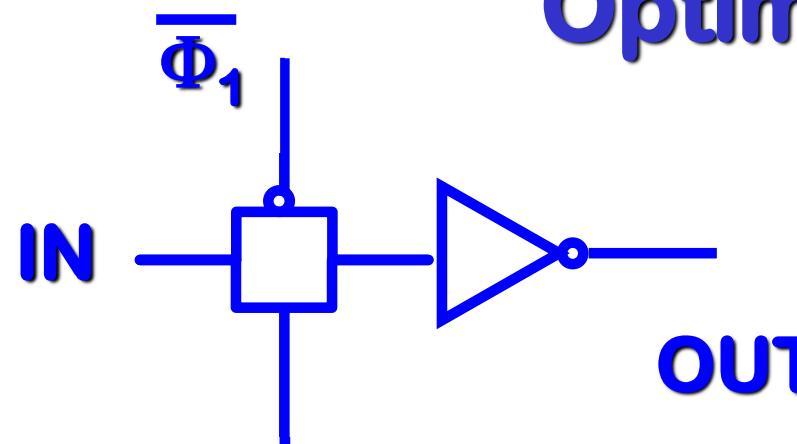
Stick Diagram



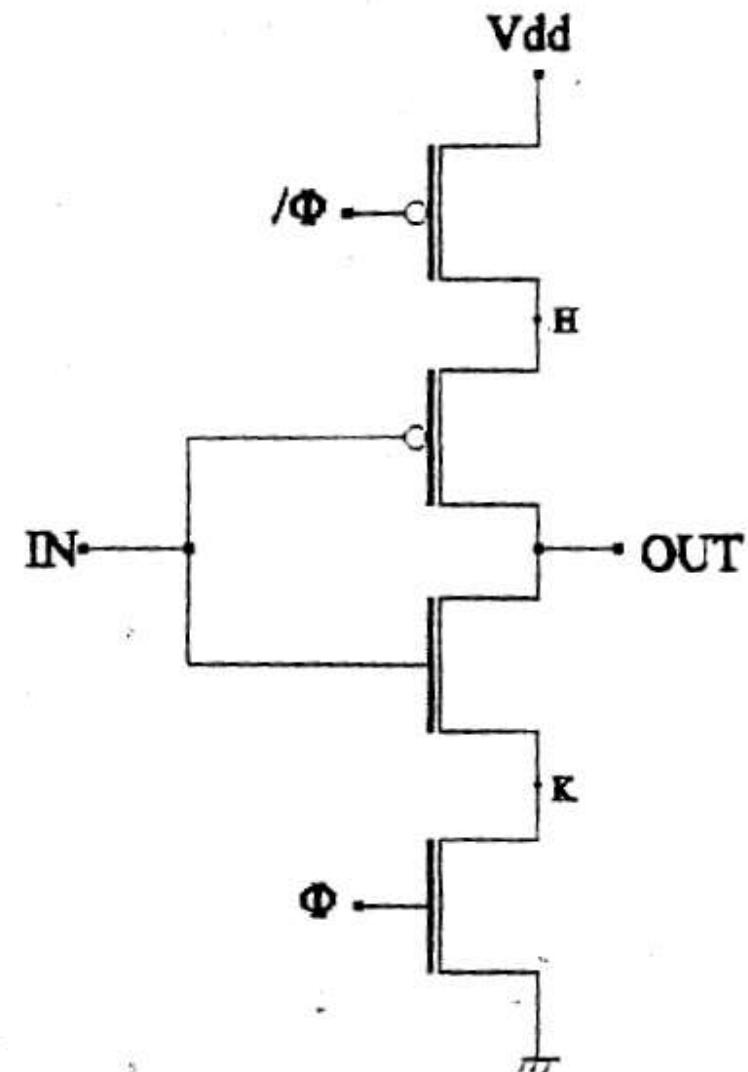
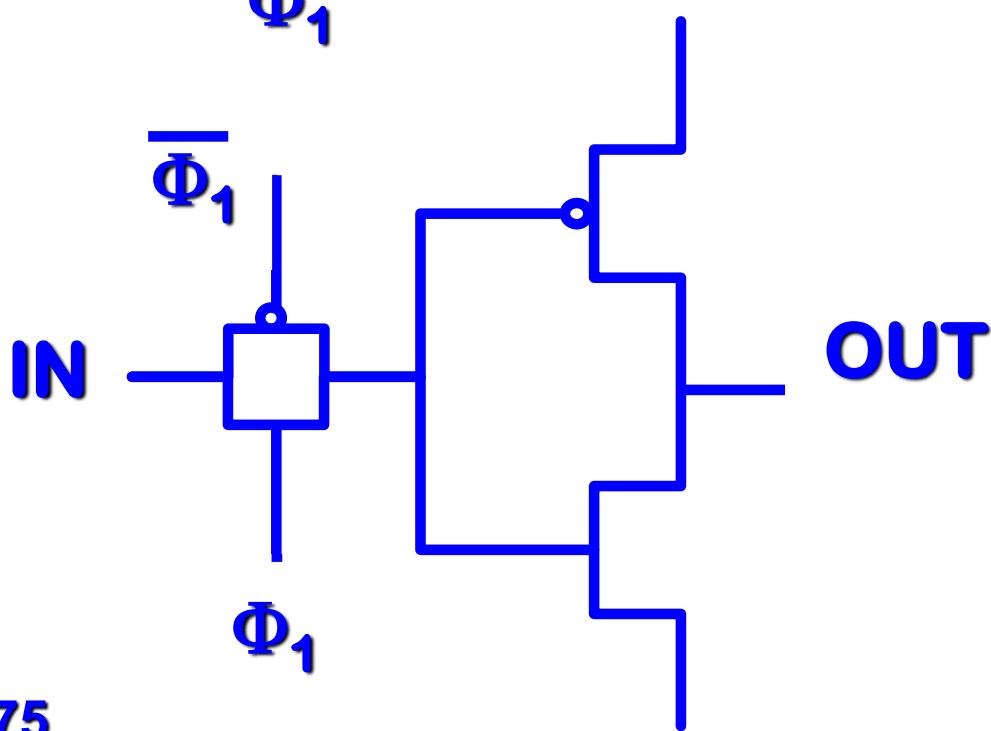
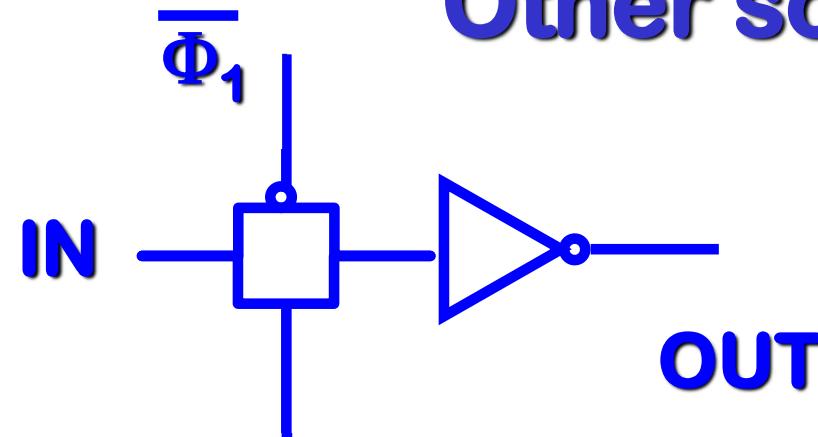
Stick Diagram



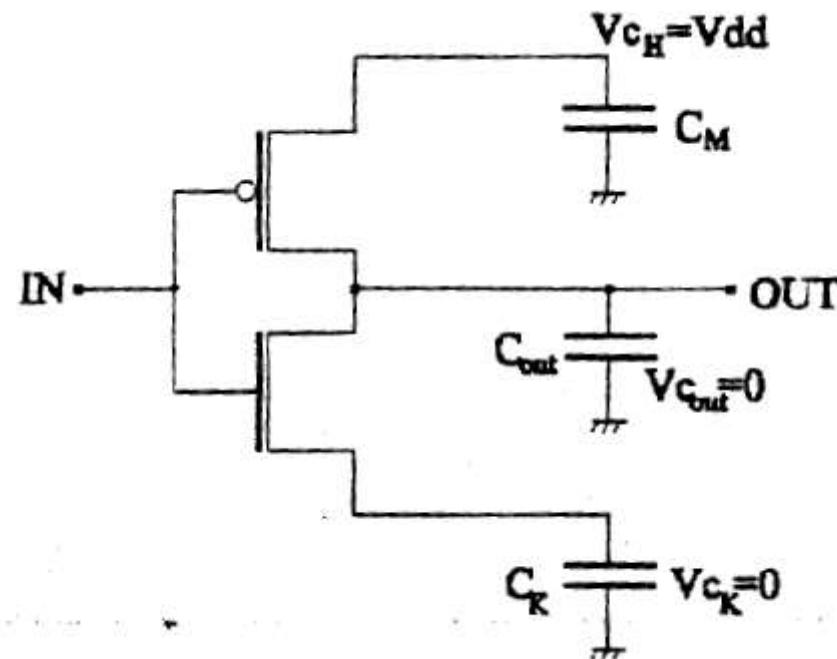
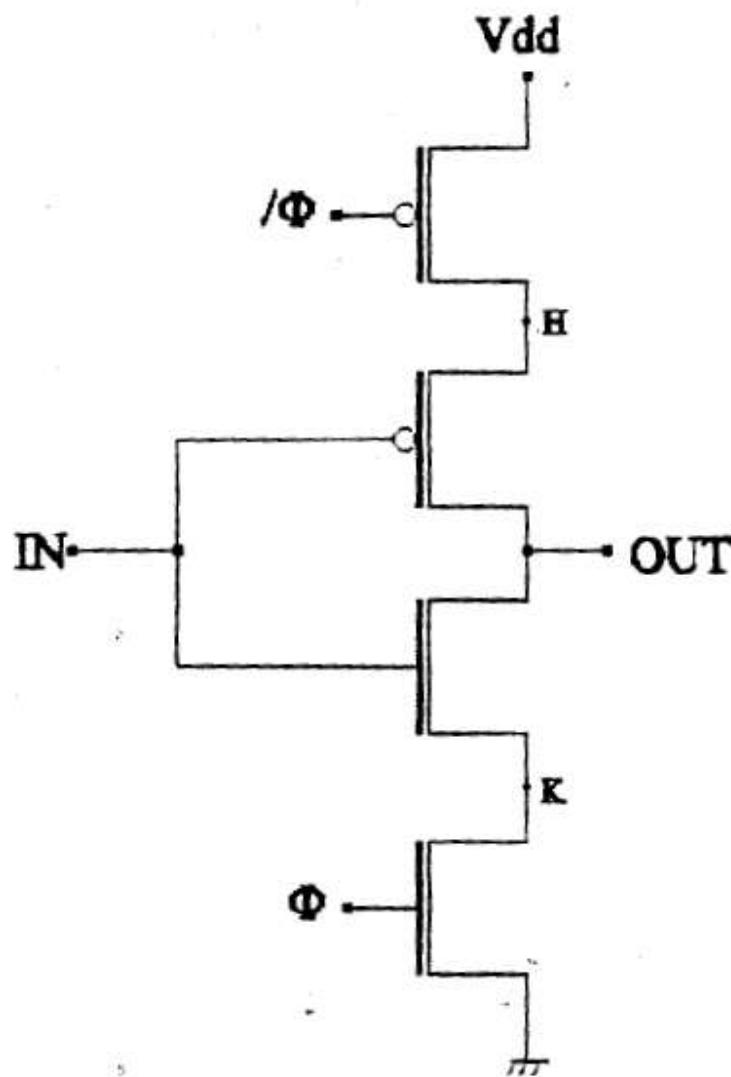
Optimization



Other solutions ?



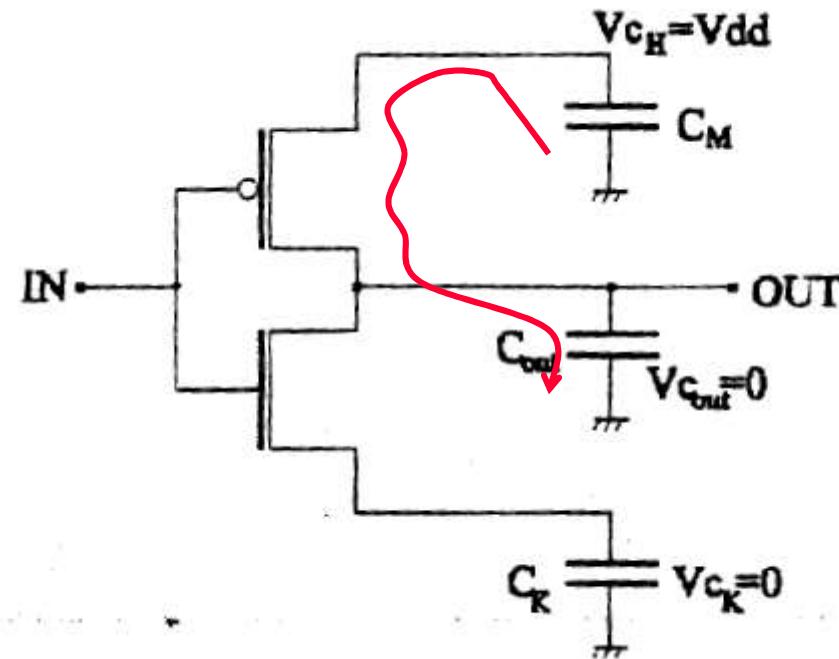
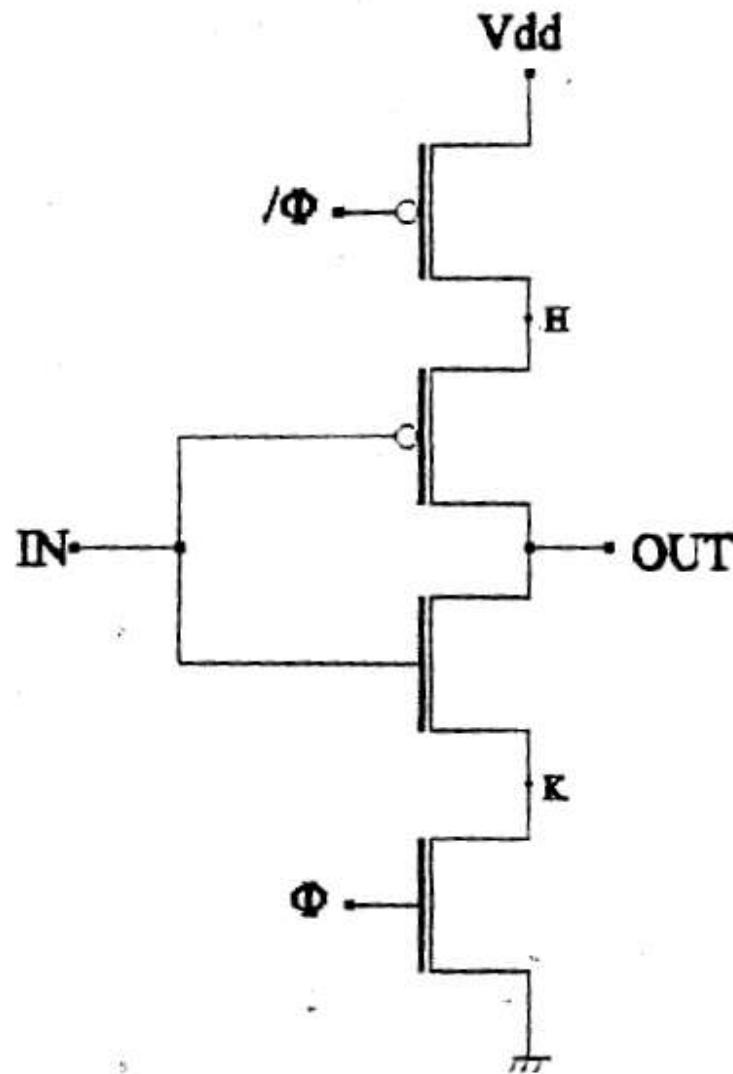
Other solutions?



$\Phi_1=1$ - sensitive

$|N=1$

Other solutions? NO



$\Phi_1=0 \rightarrow$ maintain

$IN=1 \rightarrow 0$

End, Questions ?

- **Flip Flop: Static Solution**

- Flip- Flop S-R: NOR2 e NAND2
- Flip-Flop S-R with enable
- D -Latch
- Flip Flop S-R Edge Triggered: NOR2, NAND2
- Flip Flop D Edge Triggered: NOR2, NAND2, MUX
- Flip Flop D Edge Triggered based on pass gate

- **Flip Flop: Dynamic Solution**

- Flip Flop D Edge Triggered
- Shift Register

