December 11, 2008

C8051F336/7/8/9 Revision A Errata

Errata Status Summary

Errata #	Title	Impact	Status	
			Affected Revisions	Fixed Revision
1	SMBus Hardware ACK behavior	Major	Revision A	Not Fixed

Impact Definition: Each erratum is marked with an impact, as defined below:

- Minor—Workaround exists.
- Major—Errata that do not conform to the data sheet or standard.
- Information—The device behavior is not ideal but acceptable. Typically, the data sheet will be changed to match the device behavior.

Errata Details

1. **Description**: The Address Hardware Acknowledge mechanism of the SMBus peripheral can cause an unexpected SMBus interrupt or cause an incorrect SMBus state transition. The behavior depends on the EXTHOLD bit in the SMB0CF register.

   a) When Hardware Acknowledge is enabled (EHACK = 1b, SMB0ADM) and SDA setup and hold times are not extended (EXTHOLD = 0, SMB0CF), the SMBus hardware will generate an SMBus interrupt, whether or not the address on the bus matches the hardware address match conditions. The expected behavior is that an interrupt is only generated when the address matches. When the MCU enters the interrupt service routine, the SMBus peripheral will be in the appropriate state and indicate the reception of a slave address.

   b) When Hardware Acknowledge is enabled (EHACK = 1b, SMB0ADM) and SDA setup and hold times are extended (EXTHOLD = 1, SMB0CF) the SMBus hardware will incorrectly clear the Start bit (STA) on reception of a slave address, which causes the firmware to interpret the state as the "Slave Receiver -- Data Byte received" state. This will only happen when the address match conditions determined by the SMB0ADR and SMB0MASK registers are met by the address presented on the bus.

   Impacts:

   a) Once the CPU enters the interrupt service routine, SCL will be asserted low until SI is cleared. Incompliant SMBus masters that do not support SCL clock stretching will not recognize that the clock is being stretched. If the received address does not match the conditions of SMB0ADR and SMB0MASK, the slave will generate a NACK. If the CPU issues a write to SMB0DAT, it will have no effect on the bus. No data collisions will occur.

b) Once the hardware has matched an address and entered the interrupt service routine, the firmware will not be able to use the Start bit to distinguish between the reception of an address byte versus the reception of a data byte. However, the hardware will still correctly acknowledge the address byte (SLA+R/W).

Workarounds:

a) The SMBus interrupt service routine should verify an address when it is received and clear SI as soon as possible if the address does not match.

b) It is recommended that setup and hold times should not be extended when Hardware Acknowledge is enabled. Contact mcuapps@silabs.com for alternate workarounds if these two features are required.