SILICON LABORATORIES

AN116

Power Management Techniques and Calculation

Relevant Devices

This application note applies to the following devices:

C8051F000, C8051F001, C8051F002, C8051F005, C8051F006, C8051F010, C8051F011, C8051F012, C8051F012, C8051F015, C8051F016, C8051F017, C8051F018, and C8051F019.

Introduction

This application note discusses power management techniques and methods of calculating power in a Silicon Labs C8051F00x and C8051F01x SoC. Many applications will have strict power requirements, and there are several methods of lowering the rate of power consumption without sacrificing performance. Calculating the predicted power use is important to characterize the system's power supply requirements.

Key Points

- Supply voltage and system clock frequency strongly affect power consumption.
- Silicon Lab's SoC's feature power management modes: IDLE and STOP.
- Power use can be calculated as a function of system clock frequency, supply voltage, and enabled peripherals.

Power Saving Methods

CMOS digital logic device power consumption is affected by supply voltage and system clock (SYSCLK) frequency. These parameters can be adjusted to realize power savings, and are readily controlled by the designer. This section discusses these parameters and how they affect power usage.

Reducing System Clock Frequency

In CMOS digital logic devices, power consumption is directly proportional to system clock (SYSCLK) frequency:

$$power = CV^2f$$

where: *C* is CMOS load capacitance, *V* is supply voltage, and *f* is SYSCLK frequency.

Equation 1. CMOS Power Equation

The system clock on the C8051Fxxx family of devices can be derived from an internal oscillator or an external source. External sources may be a CMOS clock, RC circuit, capacitor, or crystal oscillator. For information on configuring oscillators, see application note: "AN02 - Configuring the Internal and External Oscillators." The internal oscillator can provide four SYSCLK frequencies: 2, 4, 8, and 16 MHz. Many different frequencies can be achieved using the external oscillator.

To conserve power, a designer must decide what the fastest needed SYSCLK frequency and required accuracy is for a given application. A design may require a constant SYSCLK frequency during all device operations. In this case, the designer will choose the lowest possible frequency required, and use the oscillator configuration that consumes the least power. Typical applications include serial communications, and periodic sampling with an ADC that must be performed.

Some operations may require high speed operation, but only in short, intermittent intervals. This is sometimes referred to as "burst" operation. In the C8051Fxxx, the SYSCLK frequency can be changed at anytime. Thus, the device can operate at low frequency until a condition occurs that requires high frequency operation.

Two examples of alternating between SYSCLK sources are (1) an internal oscillator/external crystal configuration, and (2) an external crystal/RC oscillator configuration. If the device is used for occasional high speed data conversion, and a real-time clock is used for time-stamping the data, a combination internal oscillator and external crystal would be ideal. During sampling operations, the high speed internal oscillator would be used. When sampling is complete, the device could then use an external 32 kHz crystal to maintain the real-time clock. Once high speed operations are required again, the device switches to the internal oscillator as necessary (see Figure 1 below). An example of this procedure is illustrated in application note "AN008 - Implementing a Real-Time Clock".

The crystal oscillator and internal oscillator may be operated simultaneously and each selected as the SYSCLK source in software as desired. To reduce supply current, the crystal may also be shutdown when using the internal oscillator. In this case, when switching from the internal to external oscillator the designer must consider the start-up delay when switching the SYSCLK source. The C8051F0xx devices have a flag that is set when the external clock signal is valid (XTLVLD bit in the OSCXCN register) to indicate the oscillator is running and stable. This flag is polled before switching to the external oscillator. Note that other operations can continue using the internal oscillator during the crystal start-up time.

Some applications require intermittent high speed and accuracy (e.g., ADC sampling and data processing), but have lower frequency and accuracy requirements at other times (e.g., waiting for sampling interval), a combination of an external oscillator and RC circuit can be useful. In this case, the external RC oscillator is used to derive the lower frequency SYSCLK source, and the crystal is used for high frequency operations. The RC circuit requires a connection to VDD (voltage source) to operate. Because this connection could load the crystal oscillator circuit while the crystal is in operation, we connect the RC circuit to a general purpose port pin (see Figure 2 below). When the RC circuit is in use, the port pin connection is driven high (to VDD) by selecting its output mode to "push-pull" and writing a '1' to the port latch. When the crystal oscillator is being used, the port pin is placed in a 'hi-Z' condition by configuring the output mode of the port to "open-drain" and writing a '1' to the port latch. Note the RC circuit

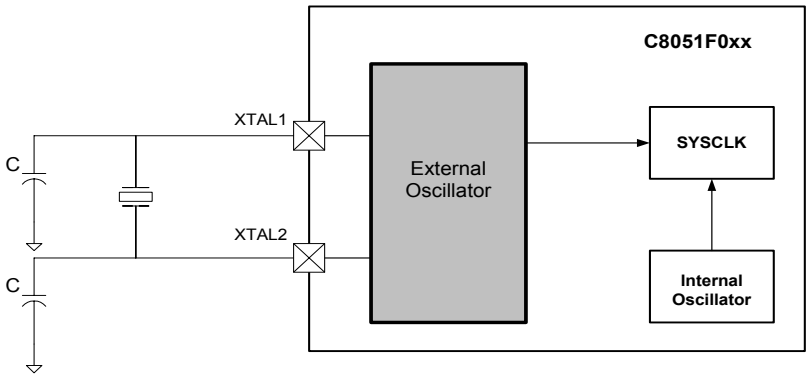

Figure 1. Internal Oscillator and an External Crystal Source Configuration

may take advantage of the existing capacitors used for the crystal oscillator.

The start-up of the RC-circuit oscillator is nearly instantaneous. However, there is a notable start-up time for the crystal. Therefore, switching from the RC oscillator to the external crystal oscillator using the following procedure:

1. Switch to the internal oscillator.
2. Configure the port pin used for the RC circuit voltage supply as open-drain and write a '1' to the port pin (Hi-Z condition).
3. Start the crystal (Set the XFCN bits).
4. Wait for 1 ms.
5. Poll for the External Crystal Valid Bit (XTLVLD --> '1').
6. Switch to the external oscillator.

Switch from the external crystal oscillator to the the RC oscillator as follows:

1. Switch to the internal oscillator.
2. Shutdown the crystal (clear the XFCN bits).
3. Drive the voltage supply port pin high (to VDD) by putting the port pin in "push-pull" mode and writing a '1' to its port latch.
4. Switch back to the external oscillator.

Supply Voltage

The amount of current used in CMOS logic is directly proportional to the voltage of the power supply. The power consumed by CMOS logic is proportional the power supply voltage squared (See Equation 1). Thus, power consumption may be reduced by lowering the supply voltage to the device. The C8051Fxxx family of devices require a supply voltage of 2.7-3.6 Volts. Thus, to save power, it is recommended to use a 3.0 volt regulator instead of a 3.3 volt regulator for power savings.

CIP-51 Processor Power Management Modes

The C8051 processor has two modes which can be used for power management. These modes are IDLE and STOP.

IDLE Mode

In IDLE Mode, the CPU and FLASH memory are taken off-line. All peripherals external to the CPU remain active, including the internal clocks. The CPU exits IDLE Mode when an enabled interrupt

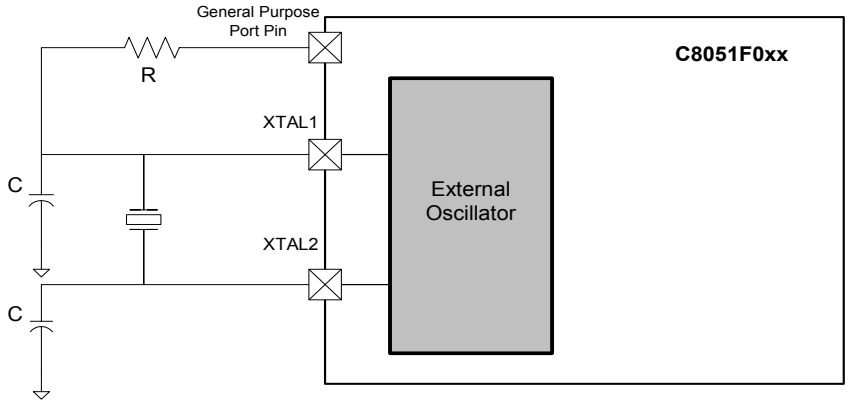

Figure 2. External RC and Crystal Oscillator Configuration

or reset occurs. The CPU is placed in IDLE Mode by setting the Idle Mode Select Bit (PCON.0) to '1'.

When the IDLE Mode Select Bit is set to '1', the CPU enters IDLE Mode once the instruction that sets the bit has executed. An asserted interrupt will clear the IDLE Mode Select Bit and the CPU will vector to service the interrupt. After a return from interrupt (RETI), the CPU will return to the next instruction following the one that had set the IDLE Mode Select Bit. If a reset occurs while in IDLE Mode, the normal reset sequence will occur and the CPU will begin executing code at memory location 0x0000.

As an example, the CPU can be placed in IDLE while waiting for a Timer 2 overflow to initiate a sample/conversion in the ADC. Once the conversion and sample processing is complete, the ADC end-of-conversion interrupt wakes the CPU from IDLE Mode and processes the sample. After the sample processing is complete, the CPU is placed back into IDLE Mode to save power while waiting for the next interrupt.

As another example, the CPU may wait in IDLE Mode to save power until an external interrupt signal is used to "wake up" the CPU as needed. Upon receiving an external interrupt, the CPU will exit IDLE Mode and vector to the corresponding interrupt vector (e.g., /INT0 or /INT1).

STOP Mode

The C8051 STOP Mode is used to shut down the CPU and oscillators. This will effectively shut down all digital peripherals as well. All analog peripherals must be shutdown by software prior to entering STOP Mode. The processor exits STOP Mode only by an internal or external reset. Thus, STOP Mode saves power by reducing the SYSCLK frequency to zero.

Note that the Missing Clock Detector will cause an internal reset (if enabled) that will terminate STOP Mode. Thus, the Missing Clock Detector should be disabled prior to entering STOP Mode if the CPU is to be in STOP Mode longer than the Missing Clock Detector time-out (100 μs).

The C8051 processor is placed in STOP Mode by setting the STOP Mode Select Bit (PCON.1) to '1'. Upon reset, the CPU performs the normal reset sequence and begins executing code at 0x0000. Any valid RESET source will exit STOP Mode. Sources of reset to exit STOP Mode are External Reset (/RST), Missing Clock Detector, Comparator 0, and the External ADC Convert Start (/CNVSTR).

As an example, the CPU may be placed in STOP Mode for a period to save power when no device operation is required. When the device is needed, Comparator 0 reset could be used to "wake up" the device.

Generally, a power conscious design will use the lowest voltage supply, lowest SYSCLK frequency, and will use Power Management Modes when possible to maximize power savings. Most of these can be implemented or controlled in software.

Calculating Power Consumption

There are two components of power consumption in Silicon Lab's C8051F00x and C8051F01x family of devices: analog and digital. The analog component of power consumption is nearly constant for all SYSCLK frequencies. The digital component of power consumption changes considerably with SYSCLK frequency. The digital and analog components are added to determine the total power consumption.

The current use calculations presented in this application note apply to the C8051F00x and C8051F01x ('F000, 01, 02, 03, 05, 06, 10, 11, 12, 15, and 16) family of Silicon Labs devices.

The data sheet section, "Global DC Electrical Characteristics" contains various supply current values for different device conditions. The current values are separated into digital (at three example frequencies) and analog components. The analog numbers presented are values with *all* analog peripherals active. Supply current values for each analog peripheral can be found in the data sheet section for the peripheral.

For convenience, the Global DC Electrical Characteristics for the C8051F00x and C8051F01x family of devices are presented in the table below.

Table 1. C8051F0xx Global DC Electrical Characteristics

PARAMETER	CONDITIONS	Min	Typ	Max	UNITS
Analog Supply Voltage		2.7	3.0	3.6	V
Analog Supply Current	Internal REF, ADC, DAC, Comparators all active		1	2	mA
Analog Supply Current with Analog Subsystems inactive	Internal REF, ADC, DAC, Comparators all inactive; oscillator disabled		6	20	μA
Analog-to-Digital supply delta (|VDD - AV+|)				0.5	V
Digital Supply Voltage		2.7	3.0	3.6	V
Digital Supply Current with CPU active	VDD=2.7V; CLK=20 MHz VDD=2.7V; CLK=1 MHz VDD=2.7V; CLK=32 kHz		10 90 10		mA μA μA
Digital Supply Current with CPU inactive (IDLE Mode)	VDD=2.7V; CLK=20 MHz VDD=2.7V; CLK=1 MHz VDD=2.7V; CLK=32 kHz		9 0.6 10		mA mA μA
Digital Supply Current (STOP Mode)	Oscillator not running		5		μA
Digital Supply RAM Data Retention Voltage			1.5		V
Specified Operating Temp Range		-40		+85	degrees C

Internal vs. External Oscillator

Besides using lower SYSCLK frequencies, the designer can realize power savings by making smart SYSCLK source choices. The internal oscillator will typically consume 200 μA of current supplied from the digital power supply. The current used to drive an external oscillator can vary. The drive current (supplied from the analog power supply) for an external source, such as a crystal, is set in software by configuring the XFCN bits in the External Oscillator Control Register (OSCXCN). Thus, at higher drive currents the user may save power by using the internal oscillator. However, at the lowest XFCN setting the external oscillator will use less than 1 μA which is less current than used by the internal oscillator. Some typical measured current values are listed below. These measurements may vary from device to device. This drive level is kept as low as possible to minimize power consumption, but must be high enough to start the external oscillator. The following table lists the cur-

rent vs. External Oscillator Frequency Control Bit settings.

Table 2. Typical Current Use vs. External Oscillator Frequency Control Bit Settings

XFCN	Current (μA)
000	0.6
001	2.0
010	5.8
011	17
100	50
101	140
110	630
111	2900

Digital Peripherals

For rough calculations, a good rule of thumb is to assume a 1 mA/MHz of operating current (digital) + 1 mA if the analog components (ADC, comparators, DAC, VREF, etc.) are enabled. This rule of thumb assumes a 3.6 V supply voltage. A lower supply voltage will reduce power consumption. At 2.7 V, the rule of thumb is 0.5 mA/MHz (in NORMAL mode). The rules of thumb for rough calculations are presented in the table below:

Table 3. Digital Current Consumption (typical)

Power Mode	VDD=2.7 V	VDD=3.6 V
NORMAL	0.5 mA/MHz	1.0 mA/MHz
IDLE	0.33 mA/ MHz	0.65 mA/MHz

Note that digital supply current is independent of how many digital peripherals are in use. Supply current is proportional to SYSCLK frequency and power supply voltage.

Analog Peripherals

The individual supply current values for each analog peripheral are posted in the data sheet section for that component (typically near the end of the section). It is recommended to disable all peripherals not in use to save power. For convenience, the C8051F00x and C8051F10x analog peripherals supply current values are listed below:

Table 4. C8051F0xx Analog Supply Current Use by Component

Analog Peripheral	Current (Typical) in μA
VDD monitor (always enabled)	8 (VDD=2.7 V) 15 (VDD=3.6 V)
ADC	450
VREF (internal)	50 (bandgap ref. and driver)
Temp Sensor	10
Comparators	1.5 (each)
DAC	110 (each)
Internal Oscillator (uses digital power supply)	200

Note the analog power consumption is relatively independent of by SYSCLK frequency.

Calculating Total Current

When the required SYSCLK frequency, supply voltage, and peripherals have been determined, the total supply current can be estimated. To calculate the total supply current, the analog peripheral current use (found by adding the currents of each of the enabled analog peripherals) is added to the digital current use (calculated for a given frequency, power mode, and supply voltage). If all of the analog peripherals are enabled, analog current use is about 1 mA.

Example Calculations

The following are examples of supply current calculations. Each application may use different

power modes, SYSCLK frequencies, and peripherals at different times. Thus, power management specifications may require several different supply current calculations. The digital component and analog components of current use are found separately, and then added together for the total.

Example 1

The C8051F000 device is being used in a system with VDD=3.6 V. An ADC is sampling a parameter and processing the sample for an output to one DAC. Because of the sampling and processing requirements of the application, SYSCLK frequency is 16 MHz using the internal oscillator.

Table 5. Analog Components

Peripheral	Supply Current (µA)
ADC	450
VREF (internal)	50
Internal Osc.	200
one DAC	110
VDD monitor	15
Total Analog	825

Table 6. Digital Component
Table 7.

In NORMAL Mode @ 16 MHz;
1 mA/MHz * 16 MHz = 16 mA

Table 8. Total
Table 9.
825 µA (analog) + 16 mA (digital)= 16.8 mA

Example 2

Assume we are still estimating the supply current in the same application in Example 1. If the sample processing is a burst operation (i.e., intermittent need for sampling and conversions), we may choose to place the CIP-51 in IDLE Mode to allow a Timer to wake-up the CIP-51 after a specified interval. In this case, the average supply current can be calculated in order to estimate power requirements. The device will switch between NORMAL Mode (for sampling and data conversion) and IDLE Mode (between sample processing operations). The switch between IDLE and NORMAL Modes (and supply current values) will happen in a cycle with a period equal to the sampling rate. (See Figure 3 below). This will allow us to calculate average supply current, after we calculate the supply current in IDLE Mode.

Table 10. Analog Component
Table 11.

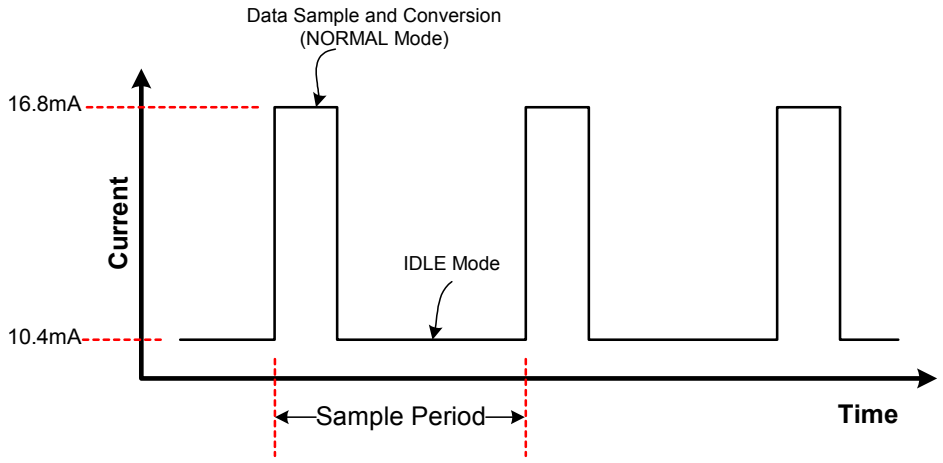

Figure 3. Supply Current Modulation to Lower Average Power

Analog peripherals are disabled during the IDLE Mode period between sample processing and output. Thus, analog current consumption is just:

VDD monitor = 15 µA.

Table 12. Digital Component
Table 13.
In IDLE Mode @ 16 MHz;
0.65 mA/MHz * 16 MHz = 10.4 mA

Table 14. Total
Table 15.
The analog component would be considered negligible in most applications, thus, the total is just the digital component:

50 µA (analog) + 10.4 mA (digital) = 10.4 mA

Now that we have calculated IDLE Mode supply current and NORMAL Mode supply current (in Example 1), we must calculate the time we spend in each mode to find the average current the device will use.

Assuming the ADC is in low-power tracking mode and at the maximum SAR conversion clock of 2 MHz (ADC set for SAR clock = SYSCLK/8), and we desire a 10 kHz sampling rate. The period of the power cycle in Figure 3 is 1/10,000 (sample rate) = 100 µs.

The time in NORMAL Mode will be the ADC tracking/conversion time, and the time to store the value in memory. In low-power tracking mode, it will take 3 SAR clocks for tracking, and 16 SAR clocks for conversion. 19 SAR clocks at 2 MHz will take 9.5 µs. To store the number will take to system clock cycles, or 0.125 µs. To enter NORMAL Mode, a *mov* instruction is executed, taking 3 SYSCLK cycles which takes 0.188 µs. Thus, the total time in NORMAL Mode is 9.5 µs+0.125 µs+0.188 µs = 9.8 µs.

Because the ADC sample period is 100 µs, the time we may be in IDLE Mode during the power cycle is 100 µs - 9.8 µs (time in NORMAL Mode) = 90.2 µs. By integrating the area under the curve in Figure 3 for one period (100 µs), and dividing that number by the period, the average supply current is 11 mA.

Example 3

If the oscillator frequency were lowered while in IDLE Mode (in Example 2) to 32 kHz using an external crystal for additional power savings, the current use would be:

The external oscillator control bits will be set to XFCN = 000. This uses 0.6 µA of analog current.

(0.65 mA *.032 MHz) + 0.6 µA = 21 µA

This is a dramatic difference from Example 2's IDLE Mode at 16 MHz, by simply reducing oscillator frequency.

Continuing with the average supply current calculation in Example 2 (with 6 extra SYSCLK cycles in NORMAL Mode to lower the frequency), the average supply current would be 1.7 mA!

Example 4

In this application, the C8051F000 is being used to sample a parameter using the ADC and store samples in memory, with high accuracy timing of samples required. For more accurate timing, the SYSCLK is derived from an external 18.432 MHz crystal oscillator. To save power, the designer has decided to use a supply voltage of 3.0 V. Timer 2 is used to time the ADC sampling intervals.

Table 16. Analog Components

Peripheral	Current (µA)
ADC	450
External Osc Driver (XFCN=111)	2900

Table 16. Analog Components

Peripheral	Current (μA)
VDD Monitor	11
Total Analog	3361

Table 17. Digital Component
Table 18.
In NORMAL Mode @ 18.432 MHz;
0.8 mA/MHz * 18.432 MHz = 14.7 mA

Table 19. Total Current Use
Table 20.
3.4 mA (analog)+14.7 mA (digital)= 18.1 mA

Example 4 in IDLE Mode

Placing the application in IDLE Mode with the ADC disabled during intervals that sampling is not required (no CIP-51 operations are needed; digital peripherals continue to operate) will save power if the sampling operation is a burst operation. In IDLE Mode, the digital current consumption is only 0.6 mA/MHz, with no ADC, thus the current consumption at 18.432 MHz =11.1 mA.

Calculating the average supply current for one sample period (similarly to Example 2, assuming a 10 kHz sampling rate and low-power tracking mode), the average current is estimated to be 11.9 mA.

Contact Information

Silicon Laboratories Inc.
4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032
Email: productinfo@silabs.com
Internet: www.silabs.com

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