SILICON LABS

Analog Peripherals

Comparator
- – Programmable hysteresis and response time
- – Configurable as interrupt or reset source
- – Low current (< 0.5 µA)

Memory
- – 1280 bytes internal data RAM
- – 16 kB byte-programmable EPROM code memory

On-Chip Debug
- – C8051F310 can be used as in-system code development platform; complete development kit available
- – On-chip debug circuitry facilitates full speed, non-intrusive in-system debug

Supply Voltage 1.8 to 3.6 V
- – On-chip LDO regulator for core supply
- – On-chip voltage supply monitor

Temperature Range: –40 to +85 °C

High-Speed 8051 µC Core
- – Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- – 25 MIPS peak throughput with 25 MHz clock
- – Expanded interrupt handler

Digital Peripherals
- – 21 port I/O; All 5 V tolerant with high sink current
- – Hardware enhanced UART, SPI™, and SMBus™ serial ports
- – Four general purpose 16-bit counter/timers
- – 16-Bit programmable counter array (PCA) with five capture/compare modules
    - – PWM
    - – Rising/falling edge capture
    - – Frequency output
    - – Software timer

Clock Sources
- – Internal oscillator: 24.5 MHz with ±2% accuracy supports UART operation
- – External oscillator: CMOS clock or external capacitor
- – Can switch between clock sources on-the-fly; useful in power saving modes

Package
- – 24-pin QFN

Development Kit: C8051T610DK