USING THE Si3400 POE PD CONTROLLER IN ISOLATED AND NON-ISOLATED DESIGNS

1. Introduction

Power over Ethernet or PoE is an IEEE standard (IEEE 802.3af) for delivering power through Ethernet cables. 802.3af specifies two options for this as shown in Figure 1 and Figure 2.

The option shown in Figure 1 must be used for "midspan equipment", which injects power on the Ethernet connection of an existing Ethernet link. Endpoint equipment, such as an Ethernet switch, can use either option.

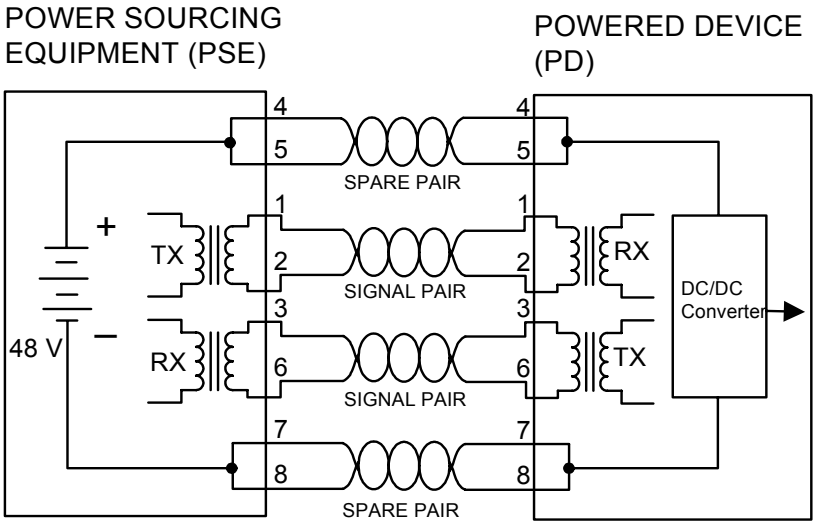

Figure 1. Power Delivered over Spare Pair

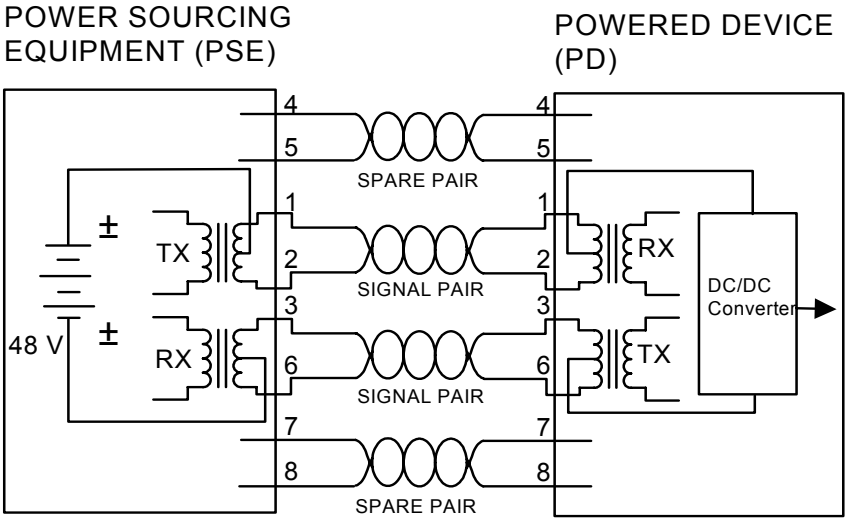

Figure 2. Power Delivered over Signal Pair

The Power Sourcing Equipment (PSE) supplies 44 to 57 VDC and must be isolated from earth ground. The PD must not consume more than 12.95 W which translates to no more than 350 mA of steady state input current allowing for 20 Ω of cabling resistance between the PSE and PD. This means that, with practical conversion efficiencies, approximately 10 W of regulated power is available to PD devices, making Power over Ethernet or PoE a preferred alternative for powering devices, such as VoIP phones, wireless routers, security devices, etc. as it eliminates the need for a power source, greatly simplifies installation, and allows easy power backup through a UPS (Uninterruptible Power Source) on the PSE end.

The advantages of IEEE 802.3af-compliant equipment include:

- This standard provides a standard way for the PSE to recognize that the PD side is PoE enabled and not supply power unless a valid signature is detected, thus eliminating the possibility of damaging equipment that is not PoE enabled.
- This standard provides a method of allowing the 802.3af PD device to supply classification information to the PSE so that the PSE can determine the load requirements of the multiple PD equipment it is powering.
- This standard ensures interoperability of PSE and PD devices from different manufacturers.

The Si3400 is a highly-integrated and efficient PD signature and dc-to-dc converter integrated circuit. It is fully compatible with 802.3af and has a two-step inrush current limiting feature to allow PD designs that are compatible with pre-standard PSE equipment. It supports PD designs that require isolation between the Ethernet cables and powered equipment as well as the lower cost option without isolation for fully-enclosed devices.

This application note will cover the basic operation of the Si3400 as well as design equations and selection criteria for signature resistors and capacitors, dc-to-dc converter power train, input filter, output filter, feedback and compensation, soft-start, duty cycle limits, and switcher current limit. The Si3400 also has integrated surge protection, which will be discussed in the final section of this application note.

2. Typical Application Schematics

Basic application circuits for the two Si3400 evaluation boards are shown in Figure 3 and Figure 4.

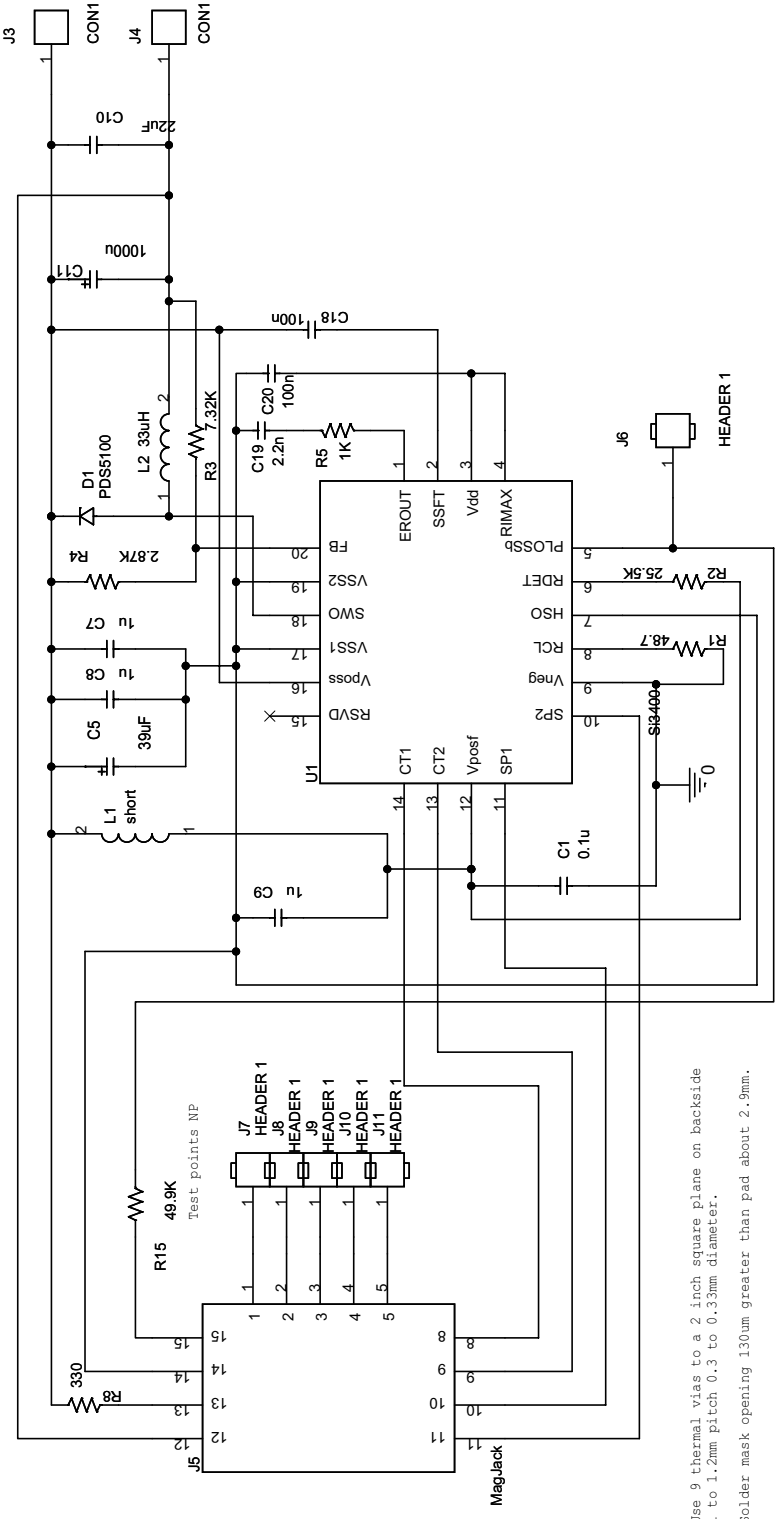

Figure 3. Non-Isolated Buck Configuration for Si3400-EVB

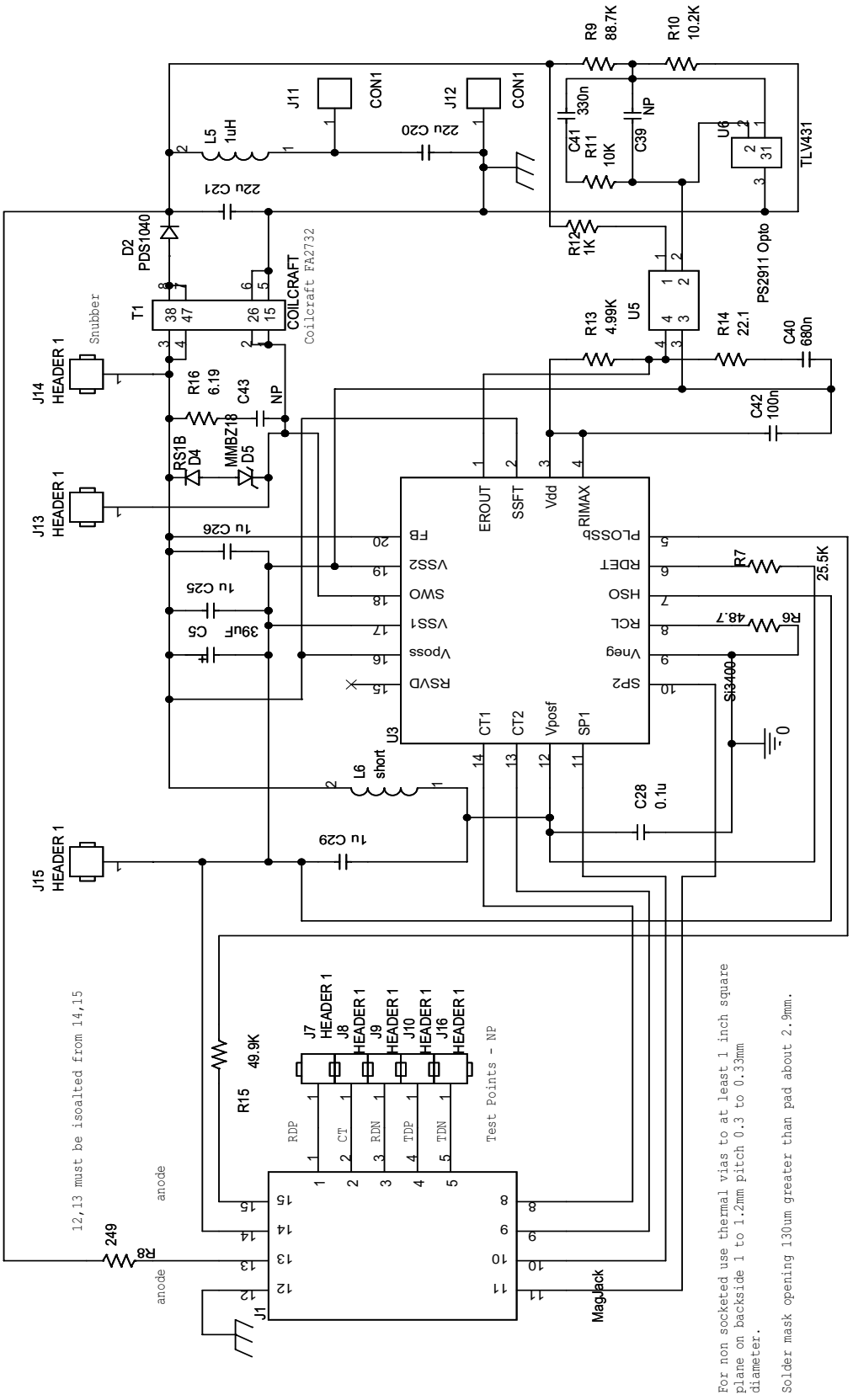

Figure 4. Isolated Flyback Configuration for Si3400ISO-EVB

3. Basic Detection, Classification, and Power Sequencing

Both of the circuit configurations in Figure 3 and Figure 4 have the same operation during detection, classification and power sequencing. A full power cycle is shown in Figure 5.

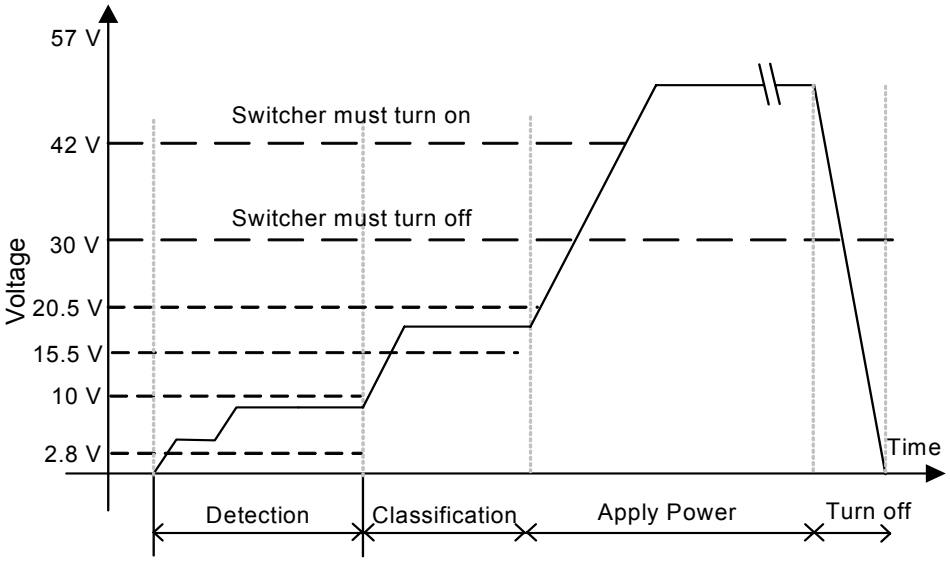

Figure 5. Full Power Cycle

As will be described in more detail below, a low voltage is used to detect a valid PD; a higher voltage is used to classify the power level of the PD, and full power operation starts at a voltage of 42 to 57 V.

3.1. Detection

During the detection phase the PSE applies two voltages between 2.8 and 10 VDC and measures the current (with a current limit of 5 mA). The slope of the I-V characteristic of the PD must be between 23.75 and 26.25 kΩ. This slope is set by the resistor, Rdet (R2 in Figure 3 or R7 in Figure 4). Additionally, the input capacitance must be between 50 and 120 nF, which is set by the capacitor, Cdet (C1 in Figure 3 or C28 in Figure 4).

The low voltage and current applied in the detect phase as well as the requirement of such specific resistance and capacitance makes it unlikely that non-PoE enabled equipment will be recognized if plugged into PSE equipment that supports PoE.

3.2. Classification

During the classification phase, the PSE applies a voltage between 15.5 and 20.5 V, current-limited to 100 mA, and determines the maximum output power requirement.

Class	Power level that the PSE Must Support
0	15.4 W
1	4.0 W
2	7 W
3	15.4 W
4	Reserved (Treat as Class 0)

Over the range of 14.5 to 20.5 V, the PD current during the classification stage must be:

Class	Minimum Current	Maximum Current	Units
0	0	4	mA
1	9	12	mA
2	17	20	mA
3	26	30	mA
4	36	44	mA

The classification current for the Si3400 is set by the resistor, Rclass (R1 in Figure 3 or R6 in Figure 4).

3.3. Powerup

During detection and classification, the PD must isolate the switcher input filter and not apply power to the load. After completion of this phase, the PSE ramps up to between 44 and 57 V, and PD turns on by closing the internal hot swap switch.

The PD must turn on at an input voltage of 42 V. After turning on, this voltage can droop to 37 V due to cabling resistance.

The Si3400 hot swap switch has a two-step current limit. The input filter capacitor is first charged to within about 1.3 V of its final value at a typical current of 150 mA. Once the filter input capacitor is almost charged, the current limit is increased to over 400 mA, and the switcher is allowed to turn on. The hot swap switch operates at the higher current limit as long as the input filter is charged to about 30 V to allow for any switcher startup transients.

The Si3400 is designed so that the hot swap switch current limit is generally not the limitation in terms of the amount of power the PD can draw. This limit is intended to be set by the switching regulator and load or by the Power Sourcing Equipment.

However, to limit inrush current as the switcher turns on, the switcher design supports soft-start operation, which is described in more detail in the detailed switcher descriptions of this application note.

Figure 6 shows the input current and output voltage vs time when 48 V dc is suddenly applied to the PD circuit. The initial current spike is due to the charging of the 0.1 µF input capacitor. For this particular device, the filter capacitor charges up with a current limit of 108 mA in 17 msec. At this point, the current limit increases, and the capacitor is allowed to fully charge the last 1.3 V resulting in a very brief current spike.

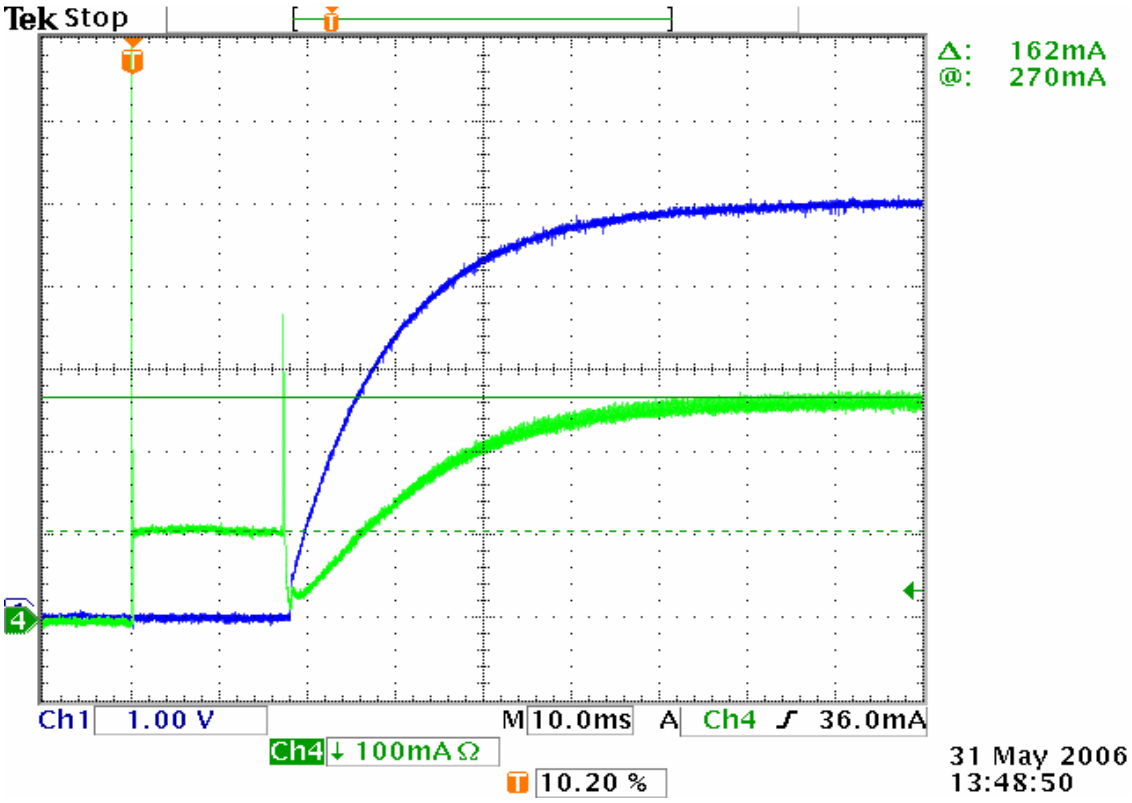

Figure 6. Typical Startup Waveform with 2.5 Ω Load

3.4. Maintain Power Signature

The PSE detects the dc current to the PD by either looking for the low ac impedance of the input filter or making sure that it is drawing current.

For this reason, the input filter capacitor must be >5 µF, and the load must be such that the input current is >10 mA. Since the Si3400 is designed to be very efficient and dissipates very little power, there is a minimal load current requirement of 250 mW (50 mA at 5 V output) so as to draw >10 mA from the input supply. It has also been observed that if the switcher is operated with no load, the switcher tends to pulse on and off, which may be undesirable. For this reason, it is recommended that a 250 mW load always be present. In "4.2. Isolated flyback design" on page 11, the snubber circuit provides a load, and the minimum load requirement changes depending on the snubber value.

3.5. Turn Off

As the PSE reduces input voltage, the PD is required to turn off at 30 V. Failure to maintain power signature or a system initiated denial of power to the PD will result in the system cycling back through the detection and classification phases.

The Si3400 has approximately 6 V of hysteresis between turn-on and turn-off with respect to the voltage across the switcher input filter capacitor so that inrush current at startup will not cause the part to turn off.

Additionally, the Si3400 has an early power loss feature where the voltage on the cable side of the diode bridge is sensed. If this voltage drops to between 25 and 30 V, the power loss signal (PLOSSb) is asserted. This allows for early detection of power removal while the switcher input capacitor is still charged.

3.6. Signature Resistors and Capacitors and Component Selection Criteria

The Si3400 is designed to meet 802.3af signature requirements with R_{det} (connected to pin R_{det}) = 25.5 kΩ ±1%. Recommended resistor values for Rclass (connected to pin R_{CL}) are listed in the following table.

Class	Power level that the PSE must support	Rclass +/- 1%	Class
0	15.4 W	Open circuit (>1.33 kΩ)	0
1	4.0 W	140 ohms	1
2	7 W	75 ohms	2
3	15.4 W	48.7 ohms	3
4	Reserved – treat as Class 0	34 ohms	4

The voltage across these resistors is limited so that 0603 or larger surface mount resistors may be used.

Csig should be a 100 V X7R type surface mount with tolerance of ±10%. While these type of capacitors exhibit a strong voltage and temperature dependence, the 50–120 nF requirement of 802.3af will be met.

3.7. Input Filter

802.3af requires that the input filter capacitor be greater than 5 µF. Additionally, the ripple at the RJ-45 input at the switching frequency of approximately 350 kHz must be less than 150 mV. To reduce the chance of conducted or radiated emissions due to induced common mode voltage on the Ethernet cable pairs, it may be desirable to further reduce the input ripple.

To maintain the >5 µF input capacitance, an aluminum electrolytic capacitor, such as Sanyo 100ME39AX, is used. This capacitor has an ESR of up to 0.4 Ω and would result in much too large an input ripple because of the ripple current from the switcher, which can be as much as 3 A. To keep input ripple down, it is recommended that additional X7R surface mount capacitors be used in parallel (for example, a 1 µF 100 V X7R 1210 capacitor is available from several vendors with an ESR of less than 0.6 Ω).

In some cases, it is desirable to further reduce input ripple voltage. In this case, it is possible to use an additional inductor to form a “pi section” filter at the input.

As will be explained in the section about surge protection, the input filter capacitor also helps to absorb surge current. For this reason, it is recommended that the input filter capacitor be a minimum of 15 µF.

4. DC to DC Converter Operation

There are two basic configurations for the dc to dc converter: buck and flyback. Additionally, the converter may be designed so that its power output is electrically isolated from the power input. Isolation is required per IEEE 802.3af when the case of the PD does not provide the isolation.

In the non-isolated case, the buck topology is generally used, and, in the isolated case, the flyback topology is generally used. It is possible to use the flyback topology in the non-isolated case, although this is not described in detail in this application note.

The equations used for determining all of the components surrounding the switching converter are described briefly below. A spreadsheet utility has also been developed to enable easy calculation of component values.

4.1. Non-Isolated Buck Design

Under most conditions the current through the inductor (L2 in Figure 3) is continuous, and the voltage across the inductor switches from positive to negative as in Figure 7.

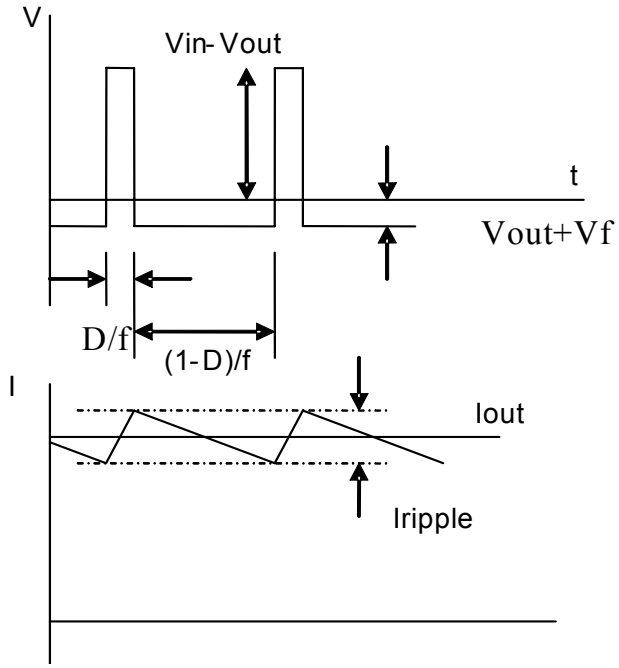

Figure 7.

The average voltage across the inductor must be zero; so, the duty cycle is:

$$D \times (V_{in} - V_{out}) = (1 - D) \times (V_{out} + V_f)$$

Where V_{out} is the desired output voltage; V_f is the forward drop of the diode (D1 in Figure 3), and V_{in} varies with the PD input voltage, which is generally 42–55 V. Solving:

$$D = \frac{(V_{out} + V_f)}{(V_{in} + V_f)}$$

The ripple current that has to be supported in the output filter is:

$$I_{ripple} = \frac{(V_{in} - V_{out}) \times (V_{out} + V_f)}{((V_{in} + V_f) \times L \times F)}$$

Where L is the inductance. L = 33 µH, Vout = 3.3 V, V_{in} = 55 V, V_f = 0.7 V

F is the internally-set switch frequency of approximately 350 kHz.

I_{ripple} = 321 mA

This is the ripple current into the output filter. The peak-to-peak ripple current that must be handled by the input filter is equal to the average current delivered to the output plus half of the ripple current in the inductor.

The rectifier diode in the non-isolated design must be rated for at least the input voltage. Generally, a 100 V diode is chosen for margin. A Schottky diode is preferred to avoid a large voltage drop and excess power associated with stored charge. Typical part numbers are PDS5100 from diodes incorporated or the equivalent UPS5100 from Microsemi. Note that these 100 V diodes have a larger forward drop than the lower voltage diodes that will be used for the non-isolated design below.

The overall efficiency is determined by dividing the output power by the input power including conduction losses in the inductor, rectifier, switching FET, input bridge, and hot swap switch as well as bias and switching losses.

4.1.1. Output Voltage Non- Isolated Design

The output voltage in the isolated case is determined by R3 and R4 according to the following equation:

$$V_{out} = 1.415 \times \left(1 + \frac{R3}{R4}\right)$$

For example, for a 5 V output, values of 7.32 kΩ for R3 and 2.87 kΩ for R4 are recommended.

For lower current, the output impedance increases, and output voltage can increase up to 4% under no load. This is related to the finite gain of the error amplifier and the need to modulate pulse width as the circuit goes into the discontinuous conduction mode. The load current at which this occurs may be reduced by increasing the inductor; contact Silicon Laboratories, Inc. for more details if this is a concern.

4.1.2. Output filter and loop stability - non-isolated design

Generally, the current in the output inductor is continuous (it does not return to zero). The current does become discontinuous for very light loads, but the continuous mode of operation is most difficult to stabilize due to the LC filter resonance that occurs in this case.

The output filter section has a resonant frequency of:

$$\frac{1}{2 \times \pi \times \sqrt{LC}}$$

The circuit will be critically damped with a resistance of:

$$2 \times \sqrt{\frac{L}{C}}$$

For a typical 33 µH inductor and 1000 µF filter cap, the resonant frequency is 876 Hz, and the resistance for critical damping is 0.36 Ω.

The damping resistance is a combination of capacitor ESR, inductor series resistance, and switch and diode resistance. It has been found that the combination of switcher FET resistance and Schottky diode effective series resistance results in an effective 0.5–1 Ω in series with the inductance for the recommended applications circuit. This damps the output resonance and allows for the use of low ESR filter capacitors without stability concerns.

The network of Rc and Cc stabilizes the feedback loop by introducing a pole zero pair in the feedback loop. It has been found that values of 2.2 nF (C19 in Figure 3) and 1000 Ω (R5 in Figure 3) work well; this translates to a pole at 120 Hz and a zero at 72 kHz.

With these values, a typical Bode plot is shown in Figure 8.

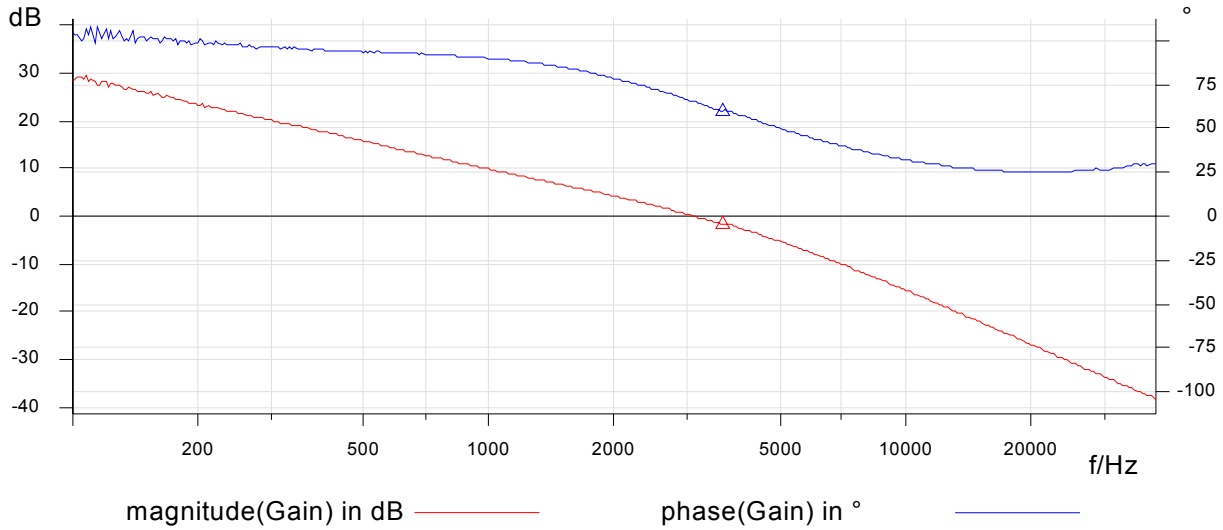

Figure 8. Typical Bode Plot

While this is a very conservative design, there is quite a bit of variation in the low-frequency gain with process and input voltage as well as in the dominant pole location and output filter effects. If it is desired to change filter and loop stabilization components, it is recommended that you check the actual Bode plots or consult with Silicon Laboratories, Inc.

4.1.3. Soft Start Non Isolated Case

In the non-isolated case, capacitor Css (C18 in Figure 3) acts to allow the duty cycle of the switcher FET to gradually increase.

There is an internal impedance of 100 kΩ in the Si3400 that works in combination with Css to slowly ramp the reference voltage to the error amplifier.

A typical Css of 100 nF gives a soft-start time constant of 10 ms, which is a good value for a 1000 µF output filter capacitor.

A typical startup waveform with a 2.5 Ω load is shown in Figure 5.

4.2. Isolated flyback design

For the isolated design, a flyback transformer approach is used. For the case of a flyback transformer, the primary inductance is "charged" when the main switcher FET turns on, and the energy stored in this inductance is delivered to the secondary when the switcher FET turns off. This type of circuit may be designed to operate in either the continuous mode or discontinuous mode. In the continuous mode, current always flows in either the transformer primary or secondary. In the discontinuous mode, the secondary current drops to zero before the next cycle of primary current. Typical waveforms are shown in Figure 9.

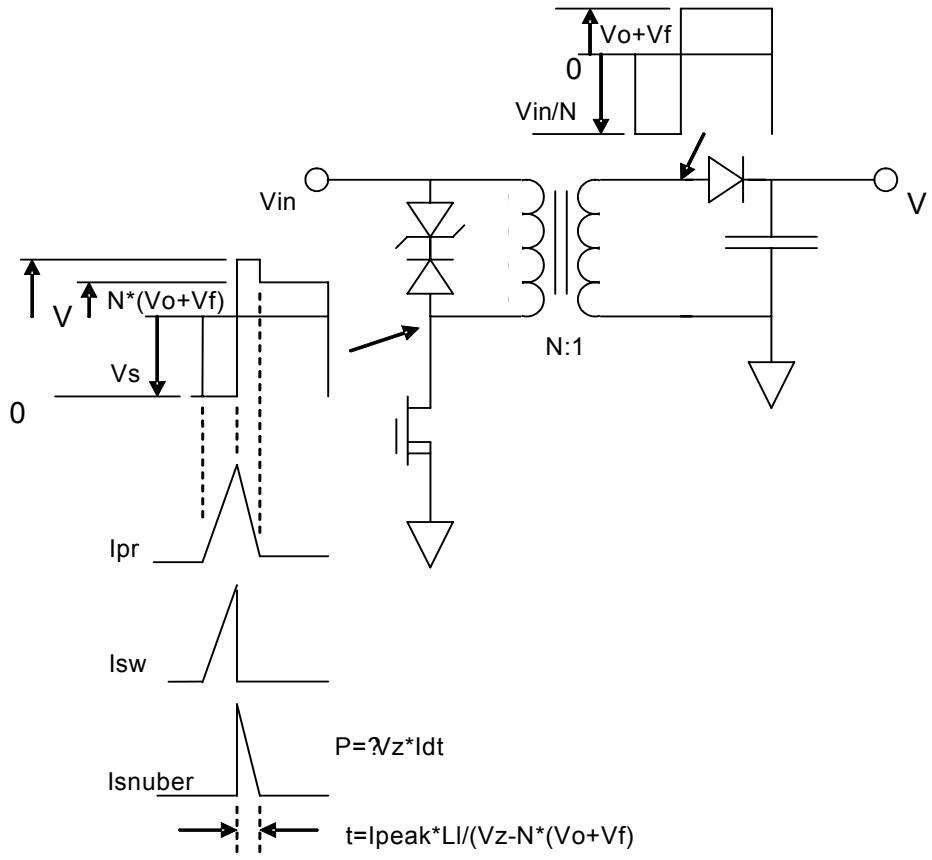

Figure 9. Typical Waveforms

A transformer with a turns ratio of N:1 is used to help reduce peak currents.

In the discontinuous mode, the output power I_0 x V_0 must be supplied by the ½ x LI^2 energy stored in the transformer with some margin for switching losses. If ε is the margin for switching losses (typically 90%), then:

$$P_0 = I_0 \times V_0 = \frac{1}{2} \times I_p^{\,2} \times L_m \times f \times \varepsilon$$

Where P_0, I_0, and V_0 are output power, current and voltage and I_p, L_m and f are transformer primary peak current, magnetizing inductance, and operating frequency.

The portion of the switching waveform where the FET is on d_1 is:

$$d_1 = I_p \times L_m \times \frac{f}{V_p}$$

Where V_p is the input voltage.

The time, d_2, where current flows in the secondary is:

$$d_2 = V_p \times \frac{d1}{(N \times (V_0 + V_f))}$$

Where V_o is the output voltage (plus diode drop), and N is the transformer turns ratio.

Solving with the constraint that $d_1+d_2 = 1$ gives:

$$I_0 = \left[\varepsilon \times \frac{V_0 + V_f}{(2 \times f \times L_m)}\right] \times \left[\frac{N}{\left(1 + N \times \frac{(V_0 + V_f)}{V_p}\right)}\right]^2$$

For a given power transformer magnetizing inductance, turns ratio, output voltage, frequency, and input voltage, this gives the output current at which the current becomes continuous and always flows in either the transformer primary or secondary.

Lm = 40 µH gives a good compromise between transformer size (larger Lm gives a larger transformer) and peak current (larger Lm gives smaller peak current at the input and output).

Plugging in $V_0 + V_f = 4$ V, $V_p = 48$ V, N = 4, Lm = 40 µH, $\varepsilon = 0.9$, and f = 380 kHz gives:

$I_0 = 0.68$ A

Above this current, the transformer current becomes continuous in that there is always current flow in either the transformer primary or secondary.

For larger output current, the duty cycle stays fairly constant at:

$$D = N \times \frac{(V_o + V_f)}{(V_p + N(V_o + V_f))}$$

In the continuous mode, the average current while the switcher FET is on is determined by setting the average input power after an efficiency, ε, to equal the average output power:

$$I_{avg} \times V_p \times \varepsilon \times D = I_O \times (V_o + V_f)$$

In this mode of operation, there is a change in primary current while the FET is on of:

$$\Delta I = \frac{V_p \times D}{(L_m \times f)}$$

The peak current that the transformer must handle is:

$$I_{peak} = I_{avg} + \frac{\Delta I}{2}$$

For the same transformer above with Io = 3 A, the peak transformer current is 1.85 A.

Increasing the turns ratio decreases peak current, particularly on the primary side. However, the secondary voltage is reflected back to the primary, and the increased turns ratio also increases the voltage on the switcher FET. Additionally, transformer leakage inductance causes an additional spike of voltage on the switcher FET, which must be clamped by a snubber.

The Si3400 has a built-in snubber that clamps the FET starting at a voltage, Vz, of 19 V above Vss with a series resistance, Rsn, of approximately 5 Ω.

The FET maximum drain voltage is 80 V, and the maximum voltage at Vpos is about 55 V; so, the snubber must clamp to 25 V. For high transformer peak current, the built-in snubber of the Si3400 requires an additional RC snubber and/or Zener clamp in parallel.

For medium-power operation, 560 pF (C43 in Figure 4) in series with 6.2 Ω (R16 in Figure 4) has been found to be effective. For full-power applications, an additional Zener diode and fast recovery diode are recommended to clamp the output at less than 25 V above V_{POS}.

Increasing the turns ratio will increase snubber power. Therefore, there is an optimal turns ratio that compromises

between high peak current at a low turns ratio and high snubber power at a high turns ratio.

Silicon Laboratories, Inc. has partnered with Coilcraft to develop flyback transformers that are optimized for maximum efficiency of the Si3400 at 3.3 and 5 V output. Recommended part numbers are FA2571-AL for 3.3 V (40 µH and 1:0.3 turns ratio) and FA2572-AL for 5 V (40 µH and 1:0.4 turns ratio). For other output supply configurations, please contact Silicon Laboratories for recommendations.

The rectifier in this case does not need as high a voltage rating because the transformer turns ratio limits the reverse voltage to (1/N) x Vin. The PDS1040 from diodes incorporated or the equivalent UPS1040 from Microsemi can be used, and these parts have much lower forward drop and overall loss due to their lower voltage rating of 40 V.

4.2.1. Output Voltage—Isolated Design

In the isolated design, a TLV431 (U5 in Figure 4) is used as an isolated reference voltage. The TLV431 is available from many suppliers and regulates at a reference voltage of 1.24 V; so, the output voltage is:

V_{out} = 1.24 x (1+R9/R10)

An opto-isolator, such as PS2911 (U6 in Figure 4), which is also available from many suppliers, is used to couple the error signal back to the Si3400.

4.2.2. Output Filter and Loop Stability—Isolated Design

In the flyback design, even if the current in the transformer is continuous in that it always flows in the transformer primary or secondary, the secondary current does not flow during the time that primary current flows, and thus there is always a large ripple current in the output which must be filtered. For the isolated design, it is recommended that a pi-section filter be used with 6.3 V, 100 µF 1210 capacitors and a 1.0 µH inductor, such as Coilcraft D01608-102ML.

Due to the operation of the flyback transformer in both the discontinuous and continuous modes as well as the output pi section filter, the overall feedback loop has large variations in frequency response, which, in general, must be compensated by a very low pole frequency. A pole of 0.5 Hz has been found to work over the entire load range. For applications where the power does not vary as much and the flyback transformer operates in only one mode, it should be possible to further optimize this.

The primary compensation consists of a pole zero pair consisting of C41 and R11.

The pole frequency is determined by the Miller multiplied capacitance of C41 working against the Thevin equivalent resistance of the voltage sense divider R9//R10.

Pole = 1/(2 x π xC41 x TLV431 gain x (R9 + R10)/R10)

Typical values of R9 / R10 = 9.16 kΩ, TLV431 gain = 700 and C41 = 330 nF set this at about 0.1 Hz.

The zero is determined by C41 and R41.

The R-C at the ERout node consisting of C40 and R14 is used for soft start. The overall design is that the C41, R11 zero is used to compensate the C40 R13 pole so:

C41 x R11 approximately = C40 x R13

Typical values are C41 = 330 nF, R11 = 10 kΩ, C40 = 680 nF, R13 = 4.99 kΩ.

The final zero used to give phase margin is determined by C40 and R14.

Typical values of C40 = 680 n and R14 = 22.1 Ω give the final zero at 10.6 kHz.

Typical Bode plots are shown in Figure 10 for the discontinuous case and Figure 11 for the continuous case.

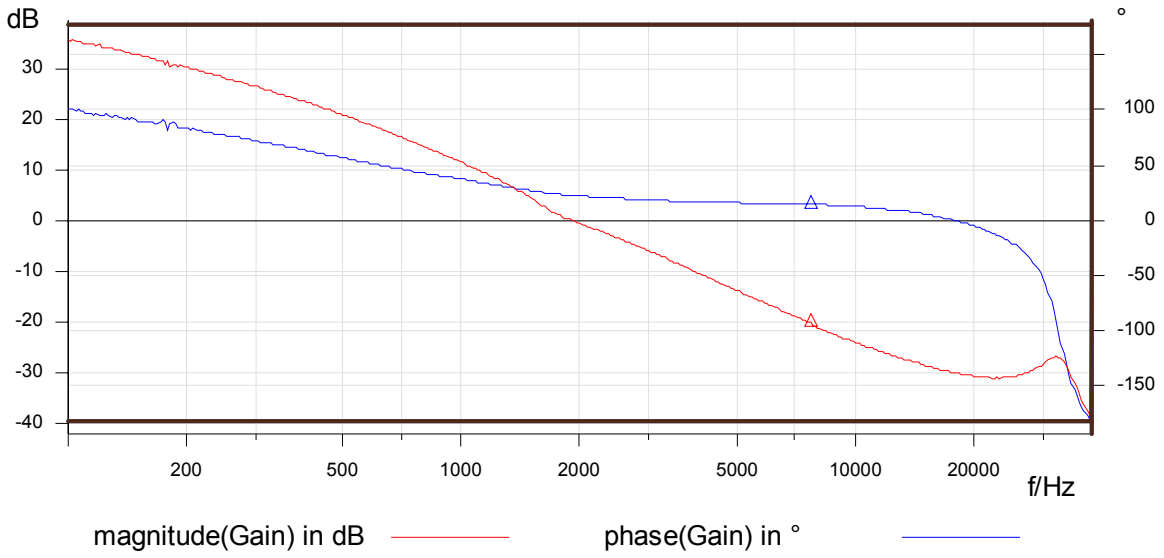

Figure 10. Discontinuous Case Bode Plot

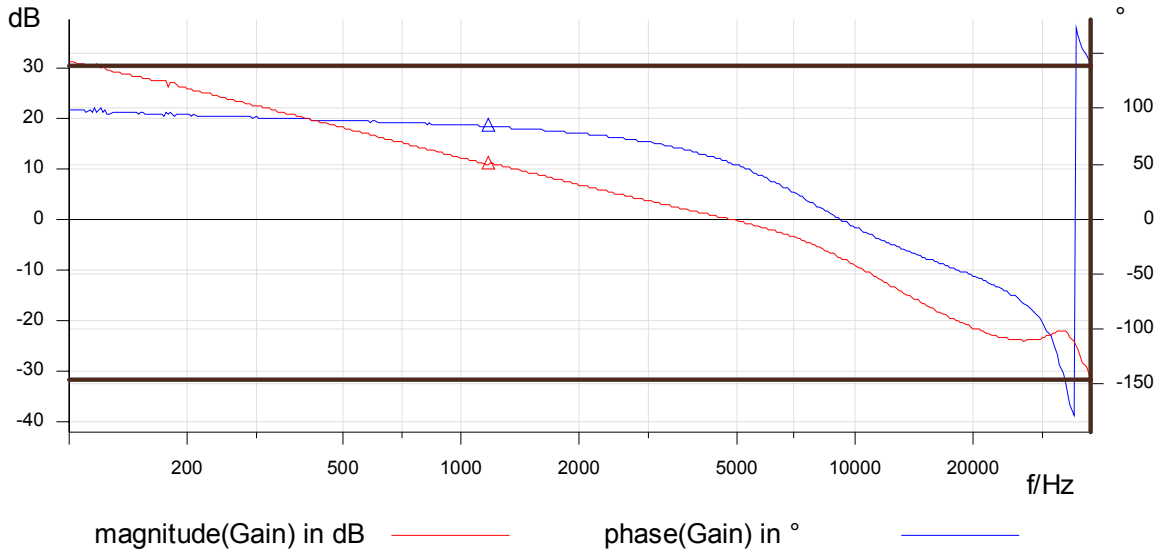

Figure 11. Continuous Case Bode Plot

This compensation is optimized for a design that can operate in both the continuous and discontinuous mode. The load transient response is optimized for the continuous mode as shown in Figure 12.

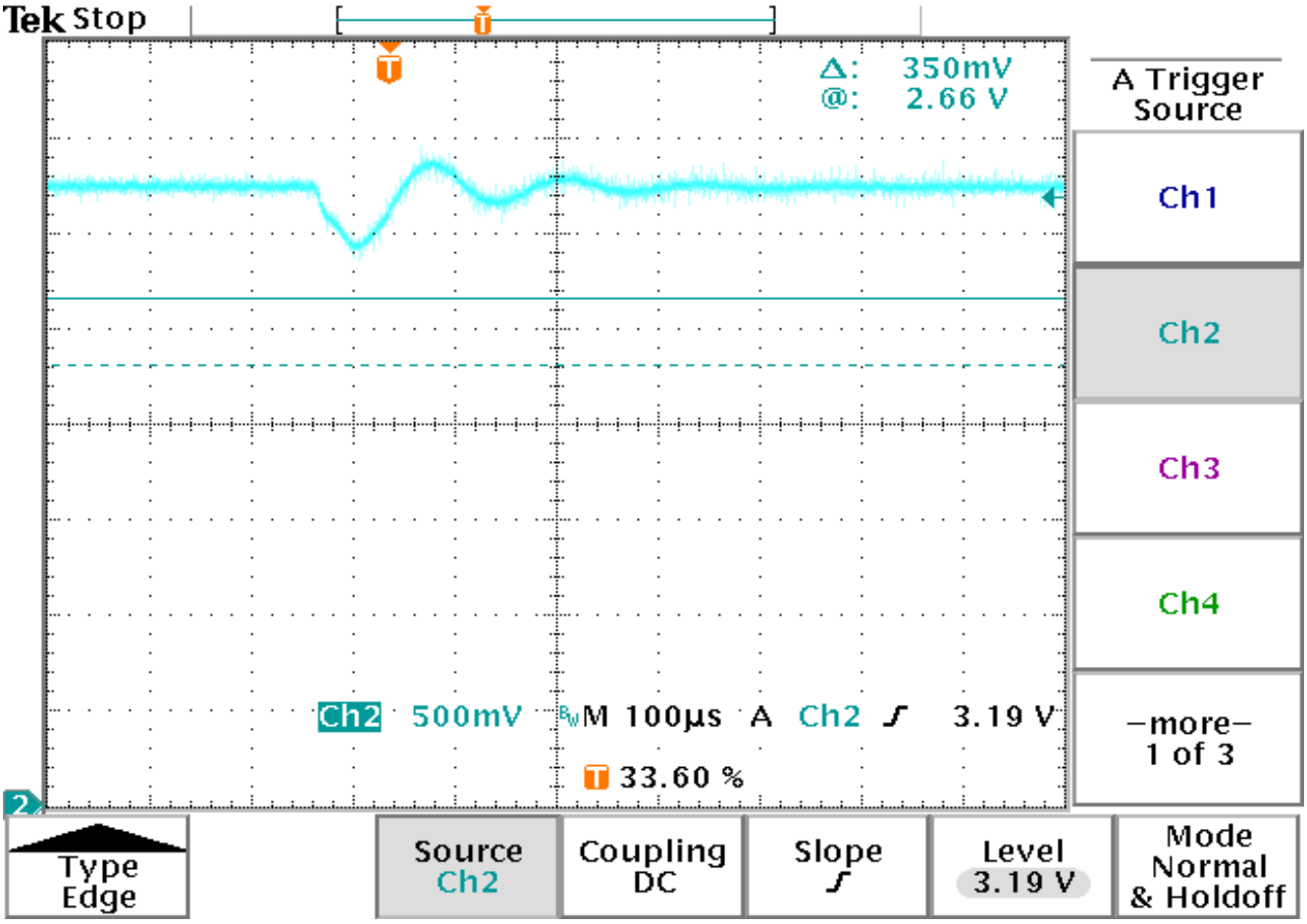

Figure 12. Load Transient Response in Continuous Mode for Load Change from 2.5 to 1.5 Ω and 3.3 V Output

4.2.3. Soft Start—Isolated Case

In the isolated topology, the soft-start feature of the Si3400 is not used. For this case, C40 in the compensation network provides soft-start operation.

The choice of C40 is also critical to the overall feedback loop compensation as described above. It is required that C40 holds the input to the ERout pin to about 1 V at start up to prevent the switcher from turning on.

Practical values of R13 = 5 kΩ and R14 of 100 Ω will insure this, with C40 determined by the position of the final zero in the compensation network as above.

5. Surge

The Si3400 has an input clamp that will protect it against surges as spelled out in 802.3af.

802.3af specifies a 1000 V surge with 0.3 µsec rise time and 50 µsec fall time applied to each conductor through a series resistance of 402 Ω. Because this pulse is generally applied to all conductors, the differential current at the input is generally very limited. The Zener clamp itself can withstand about a 1 A surge for 50 µsec.

The Si3400 is designed to handle a 50 µsec 5 A pulse that would result from applying the surge to either both Tx or Rx pairs and grounding the other pair. This is accomplished by turning on the hot swap switch while disabling the switcher if current flows in the input clamp. During the 50 µs transient, a large portion of the input energy is redirected to the switcher input capacitor. For this reason, a 15 µF minimum input capacitor is recommended.

The Si3400 is also required to survive the application of telephony ringing voltage. 802.3af specifies 56 V dc + 175 V peak ringing applied through 400 Ω source impedance at a frequency of 20 to 60 Hz. In this case, the switcher could turn on during the ringing application, which would be very undesirable and could cause damage to the switcher FET. To prevent this from happening, the switcher is actively shut down when there is any current of >1 mA flowing through the clamp.

Application of this large of a ringing signal continuously would damage the Si3400 (although it would not cause a safety hazard). However, this large of a ringing signal should also cause a "ring trip" or apparent off hook indication at the central office within 200 msec. It has been found that the Si3400 can withstand application of telephony ringing for over 1 second before damage occurs, so in general telephony ringing will not cause damage.

6. Use with an Auxiliary Power Supply

In some applications, it is desirable to be able to use either the power from the RJ45 Power over Ethernet or from a low-cost auxiliary power supply.

This is very easy to do with the Si3400, and a 48 V auxiliary supply is shown in Figure 13.

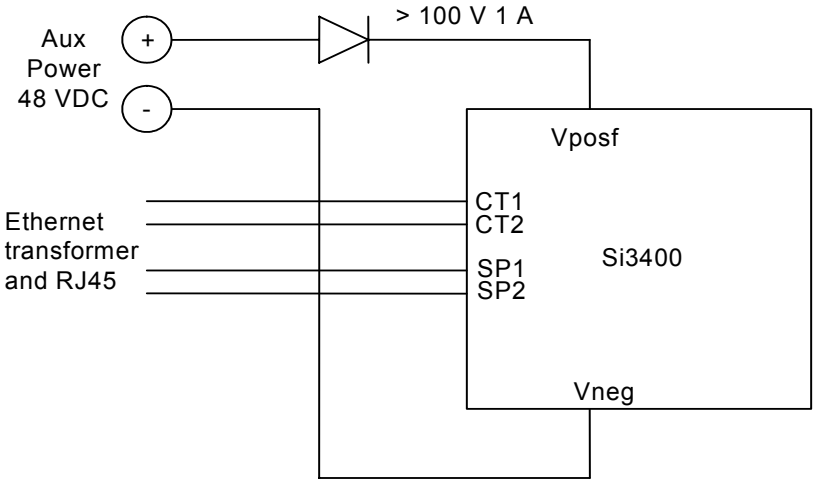

Figure 13. 48 V Auxiliary Supply

The auxiliary power source must supply between 41 and 56 V and power of at least 15 W for class 0 or 3 equipment (less if the equipment is class 1 or 2). It must also have output that is isolated from earth ground.

This provides a very simple and inexpensive means of providing auxiliary power. The diode bridges in the Si3400 ensure that no power is fed back to the PSE.

The auxiliary power source always provides the power if it is plugged in first because the PSE will not successfully complete the detection and classification cycle. If the PSE is plugged in first, the auxiliary power or the auxiliary power source could provide the power - whichever has the greater output voltage. If the auxiliary power source provides the power, the PSE will generally sense a disconnect.

The Si3400 $\overline{\text{PLOSS}}$ signal will indicate if the power is being provided from the auxiliary power source.

It is also possible to use a lower-voltage auxiliary power source, such as 12 V by diode OR at the output of the switching converter, as shown in Figure 14.

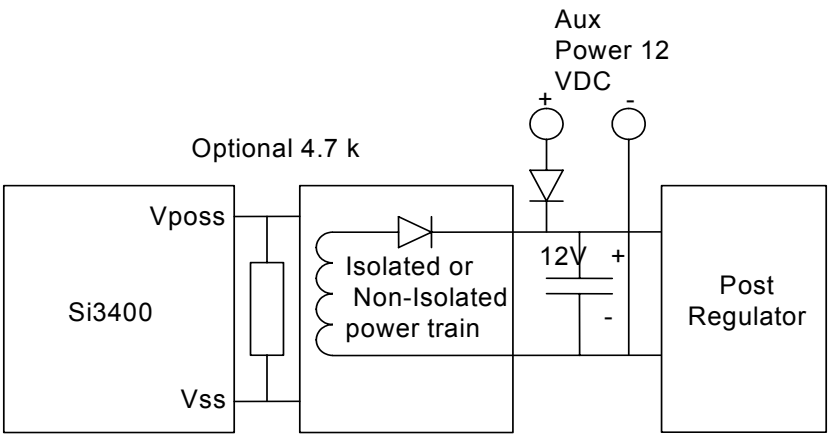

Figure 14. 12 V Auxiliary Supply

This option may be preferable when a post regulator is required for generation of very low voltages, such as 1.8 V, or when the post regulator is required for low noise.

With the post regulator option, the larger output voltage will again supply the power. In this case, the Si3400 will attempt to go through the detection and classification cycle, but if the AUX supply is providing the power, the Si3400 will not draw enough dc current, and the PSE may disconnect and continuously cycle. To prevent this, it is possible to add a 4.7 kΩ, 1 W resistor from Vposf to Vss of the Si3400 to ensure >10 mA power drain from the PSE. If this resistor is added, the PSE will always have >10 mA power drain and will stay connected even if the auxiliary power source is providing the load current.

In this option, the $\overline{\text{PLOSS}}$ indicator will not be active when the auxiliary power source is providing the power and the PSE is not present.

7. Conclusion

This application note has covered the basic operation and design equations for the Si3400 allowing the design of highly-integrated and efficient PD for PoE applications.

As mentioned, reference designs and design spreadsheets are also available to assist in the easy design-in process for the Si3400. The spreadsheets should be used in conjunction with this application note, and additional documentation is included within the spreadsheet.

The evaluation boards and reference designs are documented separately and include example layouts and BOM lists.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Updated schematics and BOM with optimized values for Rev C, Si3400
- Updated performance information with measured results for Rev C Si3400
- Added new section, "6. Use with an Auxiliary Power Supply" on page 18.

NOTES:

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