December 10, 2008

# C8051T630/1/2/3/4/5 Revision A Errata

## Errata Status Summary

| Errata # | Title | Impact | Status | |
|---|---|---|---|---|
| | | | Affected Revisions | Fixed Revision |
| 1 | Weak Pull-up Pin Voltage | Minor | Revision A | Not Fixed |
| 2 | P0.0 Analog Mode Leakage Current | Minor | Revision A | Not Fixed |
| 3 | SMBus Hardware ACK behavior | Major | Revision A | Not Fixed |
| 4 | $V_{PP}$ Programming Voltage Change | Information | Revision A | Revision A |

Impact Definition: Each erratum is marked with an impact, as defined below:

- Minor—Workaround exists.
- Major—Errata that do not conform to the data sheet or standard.
- Information—The device behavior is not ideal but acceptable. Typically, the data sheet will be changed to match the device behavior.

## Errata Details

1. **Description**: The weak pull-ups on the port I/O pins have a voltage drop between the pad (internal to the device) and the pin (external to the device), of approximately 0.9 V.

   **Impact**: Systems using port I/O pins as open-drain output will see a drop in the logic-high level at the pin. This does not affect pins used as push-pull outputs or pins used in open-drain mode which are driven by external circuitry. No additional supply current or pin leakage current is associated with this voltage drop.

   **Workaround**: For systems using an open-drain pin as an output which require higher logic levels at the pins, external pull-up resistors should be used to ensure the logic level at the pin reaches the desired logic high level.

2. **Description:** When configured for analog mode, port pin P0.0 will exhibit an additional leakage current of approximately 10 µA to ground, when bit REFBGS (REF0CN.7) is set to logic 0.

   **Impact:** Any system using port pin P0.0 as an analog input function may be affected by this extra current. Systems using the P0.0 pin as an analog output, digital input, or digital output are not affected.

   **Workaround:** If P0.0 is used as an analog input for the device (ADC, comparator, or external voltage reference), the REFBGS bit in register REF0CN should be set to “1” by firmware.

3. **Description**: The Address Hardware Acknowledge mechanism of the SMBus peripheral can cause an unexpected SMBus interrupt or cause an incorrect SMBus state transition. The behavior depends on the EXTHOLD bit in the SMB0CF register.

   a) When Hardware Acknowledge is enabled (EHACK = 1b, SMB0ADM) and SDA setup and hold times are not extended (EXTHOLD = 0, SMB0CF), the SMBus hardware will generate an SMBus interrupt, whether or not the address on the bus matches the hardware address match conditions. The expected behavior is that an interrupt is only generated when the address matches. When the MCU enters the interrupt service routine, the SMBus peripheral will be in the appropriate state and indicate the reception of a slave address.

   b) When Hardware Acknowledge is enabled (EHACK = 1b, SMB0ADM) and SDA setup and hold times are extended (EXTHOLD = 1, SMB0CF) the SMBus hardware will incorrectly clear the Start bit (STA) on reception of a slave address, which causes the firmware to interpret the state as the "Slave Receiver -- Data Byte received" state. This will only happen when the address match conditions determined by the SMB0ADR and SMB0MASK registers are met by the address presented on the bus.

   **Impacts**:

   a) Once the CPU enters the interrupt service routine, SCL will be asserted low until SI is cleared. Incompliant SMBus masters that do not support SCL clock stretching will not recognize that the clock is being stretched. If the received address does not match the conditions of SMB0ADR and SMB0MASK, the slave will generate a NACK. If the CPU issues a write to SMB0DAT, it will have no effect on the bus. No data collisions will occur.

   b) Once the hardware has matched an address and entered the interrupt service routine, the firmware will not be able to use the Start bit to distinguish between the reception of an address byte versus the reception of a data byte. However, the hardware will still correctly acknowledge the address byte (SLA+R/W).

   **Workarounds**:

   a) The SMBus interrupt service routine should verify an address when it is received and clear SI as soon as possible if the address does not match.

   b) It is recommended that setup and hold times should not be extended when Hardware Acknowledge is enabled. Contact mcuapps@silabs.com for alternate workarounds if these two features are required.

4. **Description:** A change is being made to the specified programming voltage ($V_{PP}$) for the device, in order to improve the effectiveness of programming operations. At higher $V_{PP}$ voltages, there is a possibility that programming a byte in the EPROM memory will also unintentionally program other bytes in the memory. To eliminate the possibility of this happening, the specifications for minimum, typical, and maximum $V_{PP}$ voltage are all being reduced by 0.5 V. We are implementing this change in two stages.

   Stage 1) For devices with date code prior to 0935, the maximum $V_{PP}$ voltage specification is being reduced from 6.75 V to 6.5 V and the typical specification for this parameter is being reduced from 6.5 V to 6.375. The minimum specification of 6.25 V is not changed for these devices.

   Stage 2) For devices with date code 0935 and later, the maximum $V_{PP}$ voltage is being reduced to 6.25 V minimum $V_{PP}$ voltage is being reduced to 5.75 V, the typical $V_{PP}$ voltage is being reduced to 6.0 V, and the minimum $V_{PP}$ voltage is being reduced to 5.75 V.

   **Impact:** A small percentage of devices programmed with $V_{PP}$ voltages above the specifications may exhibit programming failures. These will be easily detectable by performing a read-verify operation of the

EPROM contents. It is very important that the minimum $V_{PP}$ specification is observed for all devices. Devices are screened for EPROM data retention down to the specified levels (6.25 V for date codes before 0935, and 5.75 V for date codes 0935 and later). EPROM data retention cannot be guaranteed if devices are programmed with lower voltages.

**Workaround:** It is recommended that any existing programming hardware using the previous $V_{PP}$ specification be modified to apply between 6.25 V and 6.5 V to $V_{PP}$ during programming operations. Devices with date code 0935 and later can safely be programmed at the lower $V_{PP}$ specification.