C8051F9XX PRODUCT FAMILY

FREQUENTLY ASKED QUESTIONS

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Customer and Market Specific Questions

Q1: What is the target market for the C8051F9xx family of products? What is a real world application that will use the part?

The primary target applications for the C8051F9xx product family are products that operate from user-replaceable batteries. These devices are expected to have typical battery lives in excess of 3-5 years, and in some cases as long as 15 years. The devices you would expect to find the C8051F9xx family of MCUs in will spend the majority of their time in an ultra-low current sleep mode, awaking periodically to make a measurement, and then quickly returning to their low power sleep mode.

Some typical applications include:

1. Wireless sensors such as door or window contacts in an alarm system. In this case, the sensors are in a sleep mode, only awaking to report the opening or closing of the contact switches. At all other times, these sensors are sleeping to preserve battery life.
2. Portable personal medical equipment, such as a blood glucose meter. These types of devices are battery operated and are in a low power sleep mode except for when making measurements, which can be as infrequent as once a day.
3. Remote controls, wireless mice, and keyboards. In each of these cases the internal MCU is only active when a button on the device is depressed. At all other times, the MCU is in a low power sleep mode. Extending battery life is a key objective for product manufacturers.

In addition to low voltage/low power applications, the C8051F9xx is also ideally suited for applications that require a high level of functional density. A common goal in today's electronic product design is to pack as many functions as possible into the device. The C8051F9xx product family integrates up to 64 kB of Flash and 4 kB of RAM into a 4 x 4 mm package. This is the smallest 64 kB Flash device available in the market today.

Q2: What are the customer benefits?

Depending upon the customers' requirements, the C8051F9xx product family can result in design solutions that are more power efficient, resulting in longer battery life, lower cost, or smaller form factor. In many cases, the benefit to the customer may encompass more than one of these items.

- **Lowest Cost/Long Battery Life**—By moving from an existing product design that utilizes two AA or AAA batteries to a new design based upon the C8051F9xx and one AA or AAA battery, the customer can realize the lowest cost product. In some cases the C8051F9xx based solution could provide up to equivalent battery life of their original product based upon two batteries.
- **Smaller Form Factor/Long Battery Life**—By moving from an existing product design that utilizes two AAA batteries to a new design based upon the C8051F9xx and one AA battery, the customer can realize a smaller form factor product while providing longer battery life than their original design based upon two batteries.
- **Low Cost/Longer Battery Life**—By moving from an existing product design that utilizes two batteries in series to one that incorporates the C8051F9xx and uses the two batteries in parallel, a customer can extend the product's battery life by more than two times.
- **Small Form Factor**—By utilizing the functionally dense C8051F9x family, which is the smallest 64 kB Flash device available in the market today, a customer can free up valuable board space for other features or to simply reduce the product cost.

Q3: Why do you say that you are the world's first 0.9 V MCU? There are other MCU products out there that claim 0.9 V operation.

There are a number of products that include a microcontroller core and that operate in some fashion down to 0.9 V. Outside of the C8051F9xx family, they fall into one of two categories:

- High-end ASICs or ASIC-like MCUs, such as MP3 player chips. Other products are the NXP/Philips LPC2888 and LPC3180, $8 devices that have feature sets tailored specifically for portable products having large memory and processing requirements, and which provide very limited functionality at 0.9 V. No possible applications exist for which the C8051F9xx family and any of these devices would both be considered.
- Very low-end, low performance MCUs. Most of these are small-company ASICs, such as the ones found in hearing aids, pagers, watches, etc. One MCU that fits this description is the EM6682 from the Swiss company, EM Microelectronic. This is an 8-pin MCU with 4-bit ADC, 40 bytes of RAM, 3 kB bytes of mask ROM, and 0.4 MIPS max performance—hardly a device that would ever compete with the C8051F9xx.

The distinction of the C8051F9xx family is that it is the first general-purpose Flash MCU that achieves 0.9 V operation WITH NO PERFORMANCE COMPROMISES. Unlike the other devices in this category, the C8051F9xx is a competitive MCU even if you are using a 3 V power supply. In the broad "middle ground" of MCU requirements—1 MIP to 25 MIPs, 8 kB to 64 kB Flash, full complement of analog and digital peripherals, $1 to $4 price—the C8051F9xx stands alone as the only family to offer operation down to 0.9 V

Product Specific Questions

Q4: What differentiates the C8051F9xx Low Voltage/Low Power MCU product family from other MCU solutions on the market?

The C8051F9xx family of products is the first MCU capable of operating from a one-cell battery (0.9–1.8 V). The integrated dc-dc converter can supply enough current to power other external devices such as RF transceivers to create a true one-cell system solution. Additionally, the C8051F9xx family of devices integrates up to 64 kB of Flash and 4 kB of RAM into the smallest footprint available in the market today, a 4 x 4 mm QFN24 package.

Q5: What differentiates the six new products?

All of the C8051F9xx products include 25 MIPS 8051 CPU, integrated dc-dc converter, 4352 bytes of RAM, smaRTClock oscillator, and a 10-bit successive approximation (SAR) ADC. Memory, package, and I/Os differentiate the six devices:

Device	Package	Flash	RAM	GPIOs
C8051F930-GQ	32-pin LQFP	64 kB	4 kB	24
C8051F930-GM	32-pin QFN	64 kB	4 kB	24
C8051F931-GM	24-pin QFN	64 kB	4 kB	16
C8051F920-GQ	32-pin LQFP	32 kB	4 kB	24
C8051F920-GM	32-pin QFN	32 kB	4 kB	24
C8051F921-GM	24-pin QFN	32 kB	4 kB	16

Q6: Timing and availability?

The C8051F9xx product family is available now starting at $2.02 in quantities of 10 k. Samples of development kits are available now, with production beginning in July 2008.

Q7: Can you quantify what you mean by low power and explain how you achieved it?

The C8051F9xx family was designed to minimize energy usage. Energy is equal to V*I*t, and all three were addressed in the C8051F9xx design:

1. Low voltage operation.
2. Low active current and very low leakage sleep modes.
3. High-speed operation (core and peripherals) in the active states and fast transition between sleep and active modes.

Q8: Can this device work from 0.9–3.6 V? Why do you mention two specific operating ranges: 0.9–1.8 V and 1.8–3.6 V?

The C8051F9xx devices were designed to be powered from unregulated batteries, and no commonly used battery cells or combinations of cells provide voltages between 1.6 V and 1.8 V at any point during their useful operating life. The C8051F9xx devices are designed to provide full analog and digital performance and minimum power consumption at an internal supply voltage of 1.8 V, so we provide two distinct operating modes with different pin connections and external components, based on whether the battery voltage is above or below 1.8 V.

Most of today's low-power products use alkaline, carbon-zinc, silver oxide, NiCd, or NiMH battery chemistries, all of which have cell voltages that range from 1.2–1.6 V when fresh, and from 0.9–1.0 V at the end of their useful life. Two of these cells in series will provide a supply voltage between 1.8 V and 3.2 V; therefore, the C8051F9xx "Two-Cell Mode" supply voltage range of 1.8 V to 3.6 V can accommodate two standard battery cells, a single lithium coin cell (having an operating voltage range of 3.0–2.0 V), and regulated supplies ranging from 2–3.3 V, ±10 %.

One feature that separates the C8051F9xx family from all other general-purpose, 8-bit microcontrollers is the ability to operate from a single-cell battery at voltages down to 0.9 V. In one-cell mode, some circuit blocks operate directly from the battery; however, the digital core and most analog peripherals are powered from an inductor-based dc-dc converter that generates a supply voltage above 1.8 V. Since the one-cell and two-cell modes require different pin connections and different external components, we specify separate supply voltage ranges for each.

Q9: How can a low dropout (LDO) regulator be efficient for the system design? It is consuming current without doing any useful work.

It is a minor penalty to substantially decrease power consumption. Digital power is proportional to voltage squared. For example, if you operate from a 3.6 V supply and you do not have an LDO regulator, your digital power is proportional to V^2, which is 12.96 V. If you have an LDO that provides 1.8 V, your digital power is proportional to V^2 = 3.24 V. The digital power is lower by a factor of four, though now you also have power dissipated in the LDO. The LDO power is about the same as the power consumed in the core, since they have the same current flowing through them and each has 1.8 V across it; therefore, the net result is an improvement in the overall power consumption by a factor of two.

Think of buying a year's supply of laundry detergent. You could pay $1000 at the supermarket. An alternative would be to buy a card for Sam's Club for $250 and spend another $250 for the same amount of detergent. You save half the original amount, but it cost you something to make the savings. (For those of you not familiar with Sam's Club, it is a membership-required discount store where you can purchase items in bulk to save money.)

Q10: I notice that there is an internal dc-dc converter on board. Why is the dc-dc converter needed? Isn't it typically very inefficient?

The internal digital circuits of the C8051F9xx family require a supply voltage of 1.8 V, ±10 %, and the internal analog circuits require a minimum of 1.8 V in active operation. When the device is in one-cell mode, an inductor-based dc-dc converter is used to boost the battery voltage. The highly integrated converter needs only an external 0.68 µH inductor, plus decoupling capacitors on the VBAT and VDD pins. The converter's output voltage is programmable from 1.8–3.3 V, and it is able to supply a total of 65 mW of output power. The C8051F9xx devices themselves never require this much power, so the additional power is available to drive high-current loads (such as LEDs) from the GPIO pins or to supply sensors or other chips in the system.

The efficiency of the C8051F9xx dc-dc converter varies as a function of input voltage, output power, and other variables, but efficiencies of 80–90% are achieved under many conditions. While it is true that some power is dissipated in the converter, in many situations the overall power efficiency is actually higher when using the C8051F9xx dc-dc converter than it would be in a competing two-cell implementation.

Q11: How is an on-chip dc-dc converter more efficient than an external dc-dc converter?

The dc-dc converter is sized exactly for the MCU, which improves efficiency by providing the correct voltage and current that the MCU needs. Integrating the dc-dc converter with the power management unit (PMU) is a big advantage because it allows the MCU to control the dc-dc converter directly—putting it to sleep and waking it up. The PMU runs directly from a 0.9–3.6 V supply, so it operates even when the dc-dc converter is switched off.

The disadvantage of using an external dc-dc converter to power a typical 1.8 V MCU is that you can never put the dc-dc converter to sleep. However, for applications that require more output power than the C8051F9xx dc-dc converter can provide, an external dc-dc converter can be used with the C8051F9xx, in which case the C8051F9xx can completely shut down the external converter to achieve sub 1 µA sleep current.

Q12: How did you go about achieving lower active mode current?

The C8051F9xx series of devices are fabricated using an advanced 0.18 µm CMOS processing technology. Compared to the 0.25 µm and 0.35 µm technologies used by most competing 8-bit MCUs, the 0.18 µm technology enables operation at higher speeds with a lower operating voltage and lower active mode current. It also allows an unprecedented amount of functionality to be packed into tiny 5 x 5 mm and 4 x 4 mm QFN packages.

Q13: A current consumption of 170 µA/MHz looks fantastic compared to competitors. How do you do this?

We use 0.18 µm geometry, which gives better active-mode current consumption.

Q14: Conventional wisdom says that larger processing geometries are better for lower power consumption. Why have you selected 0.18 µm technology?

Conventional wisdom applies only to non-active modes. We have chosen a technology that provides better active-mode current and we use innovative circuit design to achieve class-leading sleep mode current.

Q15: What are the disadvantages of using the 0.18 µm technology?

Because the 0.18 µm mosfets can tolerate a maximum internal supply voltage of 2.0 V, an internal LDO voltage regulator must be used whenever the external supply voltage exceeds 2 V, which is usually the case when operating in two-cell mode. This LDO regulator and its associated bandgap reference circuit will always consume some static current (approximately 70 µA), but the lower dynamic power consumption more than makes up for this small fixed current. The C8051F9xx devices have a typical active current metric of 170 µA/MHz at 25 MHz, including the static current from the LDO regulator and precision oscillator. Because of the static current, the "µA/MHz" metric is best at fast clock frequencies; therefore, the highest overall power efficiency is obtained by operating the C8051F9xx devices for short bursts of activity interspersed with sleep mode, rather than operating at a constant low clock frequency.

Q16: What was tough about the design? Why will it not be easy to copy?

The biggest challenge was getting low leakage with 0.18 µm technology—every 0.18 µm transistor had to be disconnected from the supply in Sleep Mode. Further complicating the leakage problem was our fast wake-up goal. Although we are disconnecting every 0.18 µm transistor from power during Sleep Mode, the internal registers need to retain state so that when they wake up, they can immediately operate in active mode. Our design can wake up from Sleep Mode in 2 us, which allows the chip to wake up on a port match interrupt from a UART (at 115.2 kbps) fast enough to receive the message. Achieving both low leakage and fast wake up required us to rethink the design of nearly every part of the chip. A competitor could not obtain the same performance by reusing their existing technology or by simply shrinking their existing designs.

Q17: How can the C8051F9xx devices achieve low sleep-mode current if they require an LDO in two-cell mode and a dc-dc converter in one-cell mode, both of which require current to operate?

All circuits that need to operate in sleep mode have been designed to operate over the full 0.9–3.6 V supply voltage range, so they require neither the LDO nor the dc-dc converter. As a result, the typical sleep-mode current of the C8051F9xx devices is 50 nA.

Q18: What can the C8051F9xx devices do in sleep mode? Which circuits work, and how much current do they use?

In sleep mode, the C8051F9xx enters a very low current state while preserving the contents of all registers and SRAM. In the deepest sleep mode, the registers, SRAM, PMU, and GPIO are operating and the supply current is typically less than 100 nA. The PMU includes a low-voltage brownout detector that resets the part if the supply voltage drops below ~0.8 V to ensure that register and SRAM contents are not corrupted. The device can exit sleep mode via a customer-triggered Port Match event. If the smaRTClock peripheral remains enabled in sleep mode, the current increases by about 500 nA at 1.8 V. The Alarm and Oscillator Fail functions can be configured to wake the device. Finally, Comparator0 can be enabled and used as a wakeup source if the supply voltage remains above 1.8 V. In its lowest power mode, Comparator0 consumes about 400 nA.

Because the state of the MCU is preserved in sleep mode, the user code will resume execution with the instruction immediately following the sleep instruction as soon as the device wakes up, which takes about 2 us in 2-cell mode and usually less than 10 us in 1-cell mode.

Q19: How do the C8051F9xx devices reduce the "time" portion of the battery energy relationship E = V*I*t?

The pipelined architecture of the C8051F9xx CPU executes most instructions in one or two clock cycles with a 25 MHz maximum clock frequency. This clock frequency enables the device to execute a lot of code quickly, which in turn minimizes the amount of time that the device must remain in active mode to perform a given task. Furthermore, the C8051F9xx devices can transition very quickly between sleep and active operating modes so that they spend the maximum amount of time in the sleep state. Finally, the analog peripherals also have fast wakeup times; therefore, they can be enabled just long enough to perform their tasks.

Q20: How does the internal IREF compare to a conventional IDAC?

A conventional IDAC is designed with high resolution (typically 8 to 12 bits) and low integral and differential nonlinearities to allow it to reproduce AC waveforms with low distortion. However, the high resolution adds to the size and cost of the chip and is unnecessary for most DC biasing applications. Furthermore, the IDAC typically does not have high absolute accuracy. The C8051F9xx Programmable Current Reference (IREF) block was designed to provide DC biasing performance superior to that of a conventional IDAC while occupying much less chip area. It is a 6-bit IDAC with two ranges: 0 to 63 µA in 1 µA steps and 0 to 504 µA in 8 µA steps. It is also a bipolar IDAC, meaning that it can be used to source or sink current, and it is factory calibrated to provide high absolute accuracy.

Although intended mainly for biasing applications, the C8051F9xx IREF can operate at frequencies up to 1 MHz.

Q21: What additional components are required to implement capacitive touch sense switches when using the C8051F9xx product family?

The C8051F9xx Capacitive Touch Sense feature allows direct monitoring of up to 23 capacitive touch switches (on 32-pin devices) without any additional external components.

Q22: How does the cap touch interface differ from your existing products?

We have optimized the C8051F9xx such that it does not need external resistors or an external analog multiplexer. In addition, the timers have capacitive touch inputs, so the device uses fewer pins (one per switch).

Q23: Why are there so many different integrated oscillators on this product? When would you typically use each of them?

The C8051F9xx devices have four different oscillators that may be used to derive the system clock.

The precision internal oscillator allows for increased integration and external component elimination. This 24.5 MHz oscillator eliminates the need for an external crystal oscillator or resonator. With a spec of ±2 % across all voltage and temperature conditions, it is accurate enough to generate the communication clock for the standard UART baud rates. It consumes approximately 300 µA of current. A spread spectrum mode is provided to minimize electromagnetic interference (EMI).

For applications that do not require ±2 % accuracy, the low-power internal oscillator may be used. It is a 20 MHz oscillator with ±10 % accuracy across all voltage and temperature conditions, and it consumes less than 1000 µA.

The C8051F9xx external oscillator provides four modes of operation—external crystal, capacitor, RC network, or external CMOS clock source—that allow the user to set a clock frequency between 20 kHz and 25 MHz.

Finally, the smaRTClock peripheral includes a very low power 32.768 KHz crystal oscillator that can be used both as the clocking source for the real time clock and as the system clock. The smaRTClock oscillator has a self-oscillate mode (with provision for internal digital calibration of the oscillation frequency) for low-cost timekeeping applications that do not require the accuracy of a crystal.

Q24: Can you explain the spread spectrum mode and EMI enhancements in general?

The precision internal oscillator includes a user-selectable mode that dithers the oscillation frequency by ±0.75%. The dithering is small enough that UART operation and most other timing-critical functions are not compromised, but is large enough to reduce radiated emissions by approximately 10 dB when a 24.5 MHz system clock is driven out from a GPIO pin. The C8051F9xx devices have several additional features that minimize EMI. First, the use of 0.18 µm process technology means that the digital circuits operate at lower power and occupy a smaller area, thereby minimizing emissions. The on-chip LDO confines digital switching current to the chip itself. The dc-dc converter has some design features to minimize EMI. Finally, the GPIO pads have two programmable drive strengths: high drive for static loads, such as LEDs, and a low-drive-strength mode that minimizes signal slew rates and provides an additional 10 dB attenuation of EMI from digital output signals.

Q25: How does the spread spectrum mode work?

By dithering the clock, we can lower the peak energy. The energy is spread across frequency so that the spectral components have lower amplitude but are slightly wider. This lowered amplitude helps a design to be compliant with radiated emission standards. The clock frequency is tightly controlled—the modulating waveform is a stepped triangle wave with maximum frequency deviation of ±0.75 %. Thus, we still maintain 2 % accuracy.

Q26: How fast does your ADC wake-up?

The ADC wakes up in 1.7 uS. It uses an internal Vref. The MSP430 ADC also has an internal Vref but takes 17mS to wake-up (it needs an external capacitor). You can use an external Vref, but they tend to be expensive. Stand-alone Vrefs also tend to emphasize precision rather than settling time. The other option on a TI product is to use VDD as a Vref; this is problematic, however, as VDD is the battery voltage and its value is unknown.

Q27: This product has an integrated 10-bit SAR ADC, whereas some of the other Silicon Labs product families have 12-bit SAR ADCs. Are there ways to improve the performance if higher resolution is needed? How is this accomplished?

The burst-mode feature of the C8051F9xx SAR ADC allows the user to automatically accumulate the results of multiple conversions. In situations wherein the ADC performance is limited by random noise, accumulating the results from multiple conversions averages the noise and effectively increases the resolution. The increase in resolution is 1-bit for each fourfold increase in the number of samples, so using the maximum repeat count of 64 will result in a 16-bit accumulator value with an effective resolution of 13 bits.

Q28: What kind of development tools are available?

The C8051F930DK development platform, available for $99, provides everything needed to develop applications using the C8051F9xx product family. Included in the kit is the Silicon Labs Battery Life Estimator, which is a GUI based tool that provides details on typical battery discharge characteristics, as well as a user-editable spreadsheet to optimize the customer's low voltage/low power MCU design.

A ToolStick daughter card, part number ToolStick931DC, is available for $17.90. The daughter card is used together with the ToolStick Base Adapter, available separately or as part of the ToolStick Starter Kit, to connect the daughter card to a PC to provide a full development environment. ToolStick Programming adapters for each of the three package types offered are also available for $69.

The C8051F9xx products and development kits are available for purchase directly from Silicon Laboratories at www.silabs.com/Point9.

Operational Questions

Q29: Why do I see higher current consumption than your data sheet claims when I operate the device from the 24.5 MHz precision oscillator?

There are two common reasons for this. First, check to make sure that you are not driving the system clock (or any other clock) out on a GPIO pin. A 15 pF load that is switched at 24.5 MHz will consume more than 1 mA from a 3-volt supply. Second, make sure that the Flash one-shot timer is disabled whenever the sysclk frequency is greater than 10 MHz; failing to do so can add between 1 and 2 mA to the chip consumption.

Q30: I am seeing a reduction in SAR10 ADC performance when the device is operating in one-cell mode. What can I do to prevent this degradation?

Any system that puts large switching activity in close proximity to sensitive analog circuitry has the potential for interference issues, and systems using the C8051F9xx devices are no exception. The switching currents of the dc-dc converter can cause interference with external signals that are used as inputs to the SAR10 ADC. Conversions performed on internal signals (such as the integrated temperature sensor) are usually not affected. In addition to following good engineering practices such as careful board layout of the sensitive signals and the use of an appropriate anti-aliasing filter, there are other steps that can reduce or eliminate the interference. First, we recommend the use of the external ground reference option available on the P0.1/AGND pin. Second, you can use the SYNC bit in the DC0CN register to synchronize the ADC sampling to the dc-dc converter when running the dc-dc converter from its local oscillator. Applying averaging to the signal using the SAR10's burst mode accumulator feature is effective at eliminating any residual noise using this method. Finally, you can manually synchronize the dc-dc converter and SAR10 clocks by ensuring that both clocks are derived from SYSCLK and the SAR10 clock frequency is an integer multiple of the dc-dc clock frequency. In this method, adjustment of the phase relationship between the start-of-conversion signal and the dc-dc clock can prevent the interference. Contact MCUapps@silabs.com for more information on this topic.

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