C8051T605

25 MIPS, 2 kB OTP, Mixed-Signal MCU

Analog Peripherals

Comparator

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current (< 0.5 µA)

Memory

- 256 bytes internal data RAM
- 2 kB one time programmable code memory

On-Chip Debug

- C8051F300 can be used as in-system code development platform; complete development kit available
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug

Supply Voltage 1.8 to 3.6 V

- On-chip LDO regulator for core supply
- Typical operating current: TBD mA @ TBD MHz:
  TBD µA @ TBD kHz
- Typical stop mode current (regulator off): TBD µA
- Built-in brown-out detector

Temperature Range: –40 to +85 °C

Development Kit: C8051T600DK

High-Speed 8051 µC Core

- Pipe-lined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- 25 MIPS peak throughput with 25 MHz clock
- Expanded interrupt handler

Digital Peripherals

- 8 port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART and SMBus™ serial ports
- Three general purpose 16-bit counter/timers
- 16-Bit programmable counter array (PCA) with three capture/compare modules
  - 8 or 16-bit PWM
  - Rising / falling edge capture
  - Frequency output
  - Software timer

Clock Sources

- Internal oscillator: 24.5 MHz with ±2% accuracy supports UART operation
- External oscillator: CMOS clock or external capacitor
- Can switch between clock sources on-the-fly; useful in power saving modes

Package

- 11-pin QFN or 14-pin SOIC
- QFN size = 3x3 mm