



2.4 GHz 802.15.4/ZIGBEE™ DEVELOPMENT BOARD HARDWARE USER'S GUIDE

1. Introduction

The Silicon Laboratories 2.4 GHz 802.15.4 Development Board provides a hardware platform for the development of 802.15.4 and ZigBee™ Wireless Personal Area Networks. The 2.4 GHz 802.15.4 Development Board features the following key components:

- Silicon Laboratories C8051F121 MCU
- Chipcon CC2420 RF Transceiver
- Silicon Laboratories CP2101 USB-to-UART bridge

This development platform can be used with an 802.15.4 Media Access Controller (MAC), with a complete ZigBee stack, or it can be used to develop application-specific firmware. This document describes the hardware features and details of operation.

2. Features

The controller on the 802.15.4 Development board is the Silicon Labs C8051F121 Precision Mixed Signal MCU.

C8051F121 Features:

- 100 MIPS 8051 CPU
- 128 kB Flash memory
- 8448 bytes RAM
- 12-bit 100 ksps SAR ADC
- 8-bit 500 ksps SAR ADC
- Two 12-bit DACs
- Two analog comparators
- Voltage reference
- Temperature sensor
- Five 16-bit timers
- 6-channel PCA
- 48 digital I/O pins
- 16 x 16 MAC
- 64-pin TQFP64 package

The C8051F121 has ample resources for 802.15.4 MAC and ZigBee network firmware development. The large Flash memory and RAM size provide enough space to develop and debug networking software.

The C8051F121 features a JTAG connection on-chip debug module. Wireless networking code can be developed using this hardware platform with a simple

USB Debug Adapter and Silicon Laboratories IDE. An expensive emulator is not needed. The 2.4 GHz 802.15.4 Development Board, USB Debug Adapter, and IDE provide a complete development environment for wireless networking firmware.

The C8051F121 also features a full complement of high precision analog peripherals. The high precision ADC and DAC can be used for wireless sensor networks.

Wireless connectivity is provided using the Chipcon CC2420 802.15.4 RF Transceiver.

Chipcon CC2420 Features:

- 2.4 GHz IEEE 802.15.4 RF transceiver
- 8051-compatible high-speed SPI interface
- Dual 128-byte FIFOs for RX and TX
- Automatic CRC checking
- Automatic PAN and address filtering
- Automatic acknowledgement transmission
- Low current consumption (RX: 19.7 mA, TX: 17.4 mA)
- Integrated voltage regulator
- QLP-48 package, 7 x 7 mm

The C8051F121 communicates with the CC2420 via SPI peripheral and a full implementation of hardware control signals.

The CP2101 provides USB connectivity and a Virtual COM Port (VCP) connection to a PC.

CP2101 Features:

- USB 2.0 compliant function controller
- Full-featured UART interface
- On-chip voltage regulator
- Virtual COM port drives
- 28-pin QFN package (5 x 5 mm)

After installing the CP2101 Virtual COM Port drivers, the 802.15.4 Development Board appears as a conventional COM port on the PC. The PC software can communicate with the development board using a standard COM port interface. The MCU firmware communicates with the CP2101 using either one of the integrated UARTs.

The 2.4 GHz 802.15.4 Development Board is capable of operating from multiple power sources. A 2.1 mm power jack is provided for use with a 9 V dc wall transformer. The 2.4 GHz 802.15.4 Development Board may also be

powered from the USB port when connected. A 9 V battery holder is also provided for battery operation. A switch is provided to disconnect the battery when not in use.

The board includes five push button switches. Switch SW1 is a reset switch provided for resetting the MCU. Four user-programmable switches are provided for the application firmware user interface (SW 2–5).

The 2.4 GHz 802.15.4 Development Board has a total of eleven LEDs. Two red LEDs are used for power status indicators for the 2.1 mm jack and USB power. These LEDs are located adjacent to the 2.1 mm jack and USB receptacle. The 9 V battery power source does not have a power status indicator LED since the battery is intended for low-power operation.

Eight LEDs are available for user-programmable indicators. These LEDs are grouped into two sets of four LEDs with four different colors in each group: green, yellow, amber, and red. The LEDs are connected to port P2 on the 'F121 and may be activated collectively using byte access, or individually using bit access. These LEDs are adjacent to the four switches so that the LEDs may also be used for tactile feedback or mode indicators.

An extra red LED is provided connected to P1.1. This LED may be used as a dimmer, using the PCA in 8-bit PWM mode to drive the LED. This LED may also be used as a heartbeat indicator for a periodic interrupt timer. The heartbeat monitor will toggle the LED at a imperceptible high frequency if the timer is getting serviced properly and will blink at a perceptible low frequency if the timer is not getting serviced.

The 2.4 GHz 802.15.4 Development Board also includes a thumb wheel potentiometer to demonstrate ADC input capability. The C8051F121 contains a internal temperature sensor that is also used with the ADC. The board also has test points available for one analog input and one analog output. A twisted pair of wires can be used to connect the analog input and output to an external system. The analog input is also connected to an analog comparator. The analog comparator can be used to generate an alarm interrupt when the input voltage exceeds the reference voltage.

The RF SMA connector may be used with the supplied antenna or may be connected to test equipment using standard 50 Ω SMA coax cable.

3. Hardware Details

A detailed schematic of the 2.4 GHz 802.15.4 Development Board is provided in Section 4. The silk screen and top side components are shown in Figure 1. The remaining figures are images of the other PCB layers.

The power supply circuit uses a 3.3 V low drop out regulator (U3). The LM2936 was selected for its low quiescent current to enable low power operation. A high-current low drop out regulator, such as the LM2937, is recommended for continuous 100 MIPS operation. Three schottky diodes are connected from regulator input to the three possible power sources: power jack, USB, and 9 V battery. In this configuration, the current will be supplied by the input source with the highest voltage. Note that the supplied wall transformer voltage is normally higher than both the USB bus voltage and the 9 V battery. However, the battery voltage is normally higher than the USB bus voltage. So the battery power switch should be turned off to conserve the battery. A tantalum capacitor C21 is provided on the regulator output to minimize the ripple voltage. This capacitor may be safely removed for ultra-low power operation. A ceramic capacitor with a resistor in series is provided to ensure regulator stability with the tantalum capacitor removed.

The CP2101 provides a USB connection for the 2.4 GHz 802.15.4 Development Board. The CP2101 is always powered from the USB bus. The CP2101 is unpowered when the USB is not connected. The TX and RX lines of the CP2101 are connected to both UART0 and UART1. UART0 is used in many simple 8051 code examples. UART1 provides more flexibility in setting baud rates, especially with lower system clock frequencies. Both UART0 and UART1 should be enabled in the crossbar. However, the TX output should be enabled only on the UART actually in use. The $\overline{\text{SSPND}}$ signal is connected to P3.7 of the C8051F121. This can be used to accommodate the USB suspend mode. When the $\overline{\text{SSPND}}$ signal is asserted, a bus powered USB device should switch to a low power state, drawing less than 500 μA . This feature may not be implemented in the development firmware.

A 10-pin JTAG connector is provided for in-circuit programming and debug. This connector is configured to work with the Silicon Laboratories USB Debug Adapter. The USB Debug Adapter can be powered from V_{DD} on pin 1 of the connector. The 2.4 GHz 802.15.4 Development Board is also compatible with the USB Debug Adapter. However, the board cannot be powered by the USB Debug Adapter.

The 2.4 GHz 802.15.4 Development Board comes with an 8 MHz crystal for the C8051F121. This crystal was selected for compatibility with existing 802.15.4 MAC firmware. The C8051F121 draws about 1 mA per MHz while executing code from Flash memory. Typical current consumption for the C8051F121 using an 8 MHz crystal is 8 mA running directly off the crystal, 24 mA running at 24 MHz off the PLL, and about 2 mA with the crystal running and the CPU in IDLE mode.

The 8 MHz crystal can be replaced with a low frequency crystal for ultra-low power operation. The current consumption of the C8051F121 is about 30 μ A using a 32 kHz crystal with the MCU in IDLE mode. The internal oscillator of the C8051F121 can then be used with or without the PLL when executing code.

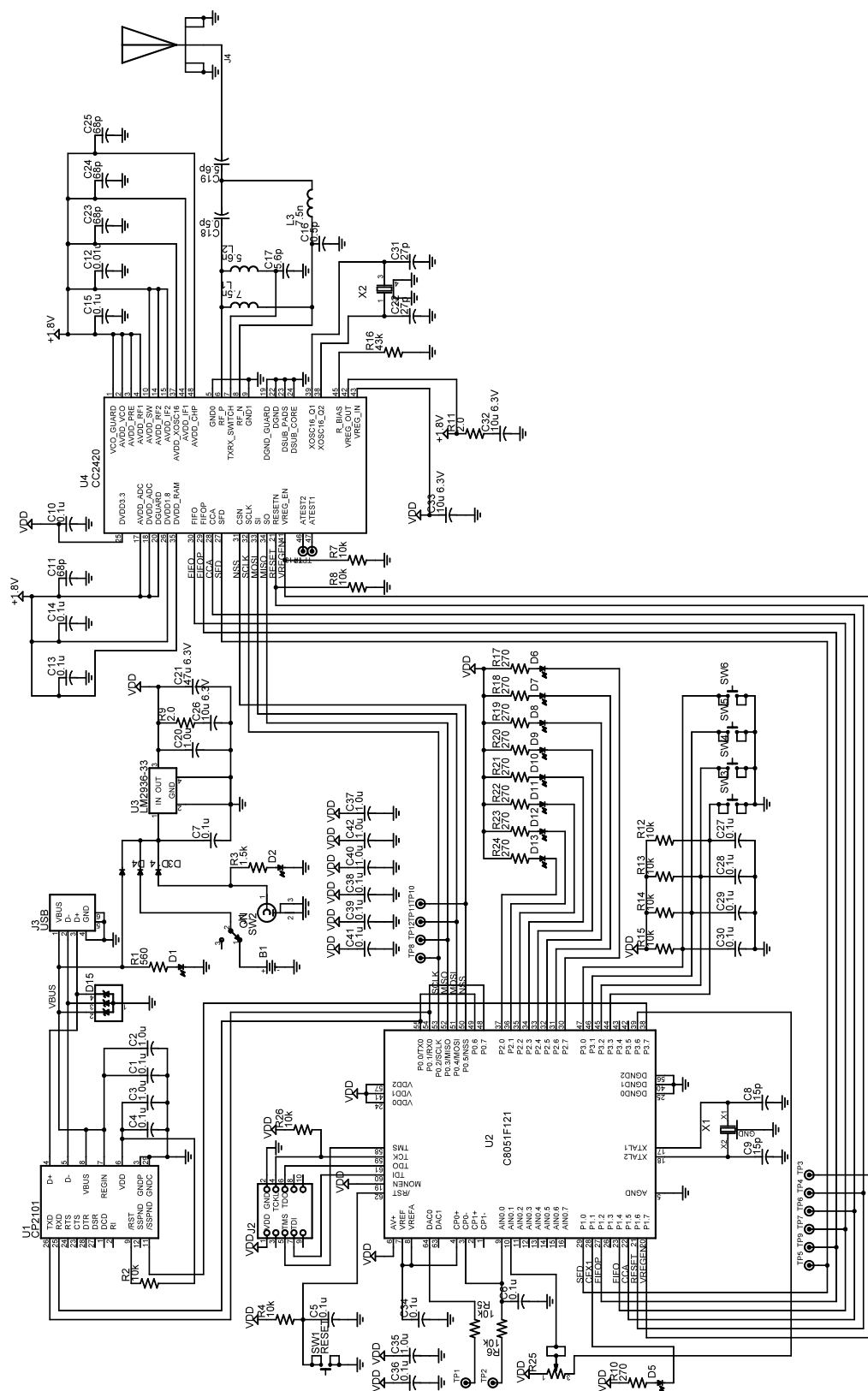
The 2.4 GHz 802.15.4 Development Board CC2420 interface provides complete interface for the CC2420 transceiver. The SPI peripheral of the C8051F121 is connected to the SPI port of the CC2420. The C8051F121 is configured as the SPI master and the CC2420 is configured as a slave. The SPI peripheral of the C8051F121 must be configured for four-wire mode to skip the NSS pin in the crossbar. The SCLK, MOSI, and NSS are configured as outputs. The SPI bus operates reliably up to about 4 MHz. While the C8051F121 and CC2420 are specified to operate at higher clock rates, the bus capacitance limits the data rate. Test points are provided and labeled for observing the SPI data with an oscilloscope.

The start-of-frame delimiter (SFD) signal from the CC2420 is connected to P1.0 of the C8051F121. This port pin may be configured as an input capture pin, such as CEX0, using the PCA in input capture mode. This

feature may be used to time-stamp an incoming frame and synchronize with a beacon frame. The FIFO threshold signal FIFOP is connected to P1.2 of the C8051F121. This port pin may be configured as an external interrupt, INT0. This signal is typically used to interrupt the CPU and initiate the reception of an incoming data frame.

The PCB layout is designed to provide good RF performance and isolation between the RF and CPU. The PCB uses a cost-effective construction with a standard 0.062 inch nominal thickness and FR4 dielectric thicknesses of 0.012/0.028/0.012 inches. Layer 3 is a solid ground plane layer over the entire board. Layer 2 has a V_{DD} plane under the MCU section and carefully routed supply traces for the RF section. The top and bottom layers are used for routing with unused areas flooded with ground plane. Via stitching is used in the RF section. The RF layout is closely duplicated from the CC2420EM reference design from Chipcon (www.chipcom.com). The RF output 50 Ω traces are adjusted slightly for a FR4 dielectric thickness of 0.036 inches between the top layer and the ground plane layer 3.

4. Schematic



5. Bill of Materials

| Qty. | Parts | Description | Value | Package | Part Number | Manufacturer |
|---|---|-----------------|--------------------|---------|----------------|--------------|
| 1 | U4 | RF Transceiver | | QFP48 | CC2420* | Chipcon |
| 1 | U1 | USB-UART Bridge | | QFN28 | CP2101* | Silicon Labs |
| 1 | U2 | 8-Bit MCU | | QFP64 | C8051F121* | Silicon Labs |
| 4 | C10, C13, C14, C15 | Chip Capacitor | 0.1 μ F, 6.3 V | 402 | 490-1318-1-ND | |
| 4 | C11, C23, C24, C25 | Chip Capacitor | 68 pF | 402 | 490-1289-1-ND | |
| 2 | C16, C18 | Chip Capacitor | 0.5 pF | 402 | 399-1000-1-ND | |
| 2 | C17, C19 | Chip Capacitor | 5.6 pF | 402 | 399-1008-1-ND | |
| 2 | L1, L3 | Chip Inductor | 7.5 nF | 402 | 490-1143-1-ND | |
| 1 | C12 | Chip Capacitor | 0.01 μ F, 25 V | 402 | 399-3066-1-ND | |
| 1 | L2 | Chip Inductor | 5.6 nF | 402 | 490-1081-1-ND | |
| 1 | R11 | Chip Resistor | 2.0 | 402 | 311-2.0JCT-ND | |
| 1 | R16 | Chip Resistor | 43 k | 402 | RHM43.0KLCT-ND | |
| 14 | C1, C4, C5, C6, C7, C27, C28, C29, C30, C34, C36, C38, C39, C41 | Chip Capacitor | 0.1 μ F, 25 V | 603 | 399-1282-1-ND | |
| 11 | R2, R4, R5, R6, R7, R8, R12, R13, R14, R15, R26 | Chip Resistor | 10 k | 603 | RHM10.0KHCT | |
| 9 | R10, R17, R18, R19, R20, R21, R22, R23, R24 | Chip Resistor | 270 | 603 | RHM270GCT-ND | |
| 7 | C2, C3, C20, C35, C37, C40, C42 | Chip Capacitor | 1.0 μ F, 16 V | 805 | 399-1284-1-ND | |
| 3 | C26, C32, C33 | Chip Capacitor | 10 μ F, 6.3 V | 805 | 399-3138-1-ND | |
| 5 | D1,D2,D5,D9,D13 | SM LED | Red | 805 | 160-1176-1-ND | |
| 2 | D8,D12 | SM LED | Amber | 805 | 160-1177-1-ND | |
| 2 | D7,D11 | SM LED | Yellow | 805 | 160-1175-1-ND | |
| 2 | D6,D10 | SM LED | Green | 805 | 160-1179-1-ND | |
| 2 | C8, C9 | Chip Capacitor | 33 pF | 603 | 399-1055-1-ND | |
| 2 | C22, C31 | Chip Capacitor | 27 pF | 603 | 399-1054-1-ND | |
| 1 | R3 | Chip Resistor | 1.5 k | 603 | 311-1.50KHCT | |
| 1 | R9 | Chip Resistor | 2.0 | 603 | 311.2.0HCT-ND | |
| 1 | R1 | Chip Resistor | 560 | 603 | P560CGCT-ND | |
| *Note: Manufacturer's Part Number. All other part numbers listed are Digi-Key part numbers. | | | | | | |

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| Qty. | Parts | Description | Value | Package | Part Number | Manufacturer |
|--|--------------------------|------------------------|-------------------|------------|-------------------|--------------|
| 1 | D15 | USB OVP | | SP0503BAHT | SP0503BAHT* | Littlefuse |
| 3 | "D3, D4, D14" | Schottky Diode | | SOD123 | MBR0520LCT-ND | |
| 1 | X1 | Crystal | 8 MHz | | SE3414-ND | |
| 1 | C21 | Tantalum Capacitor | 47 μ F, 6.3 V | Case B | 478-1692-1-ND | |
| 1 | U3 | Micro-power LDO | | SOT-223 | LM2936MP-3.3CT-ND | |
| 1 | X2 | Crystal | 16 MHz | TSX10A | TSX-10A 16MHz* | Toyocom |
| 5 | "SW1,SW3, SW4, SW5, SW6" | 6 mm Push-Button | | SW_PB_6MM | P8007-ND | |
| 1 | J4 | Vertical SMA | | SMA | ARFX1231-ND | |
| 1 | SW2 | SPDT Switch | | | SS12DP2* | NKK |
| 1 | B1 | Battery Holder | 9 V | | 1294K-ND | |
| 1 | J2 | Shrouded 10 pin header | JTAG | | MHB10K-ND | |
| 1 | J3 | USB Connector | USB | | ED9003-ND | |
| 1 | J1 | 2.1 mm Jack | RAPC722 | | SC1153-ND | |
| 1 | R25 | Thumb-Wheel Pot | 10 k | | P4A9103-ND | |
| 1 | | Antenna | 2.4 GHz | SMA | 2010B4844-01* | GigaAnt |
| *Note: Manufacturer's Part Number. All other part numbers listed are Digi-Key part numbers. | | | | | | |

6. PCB Layout

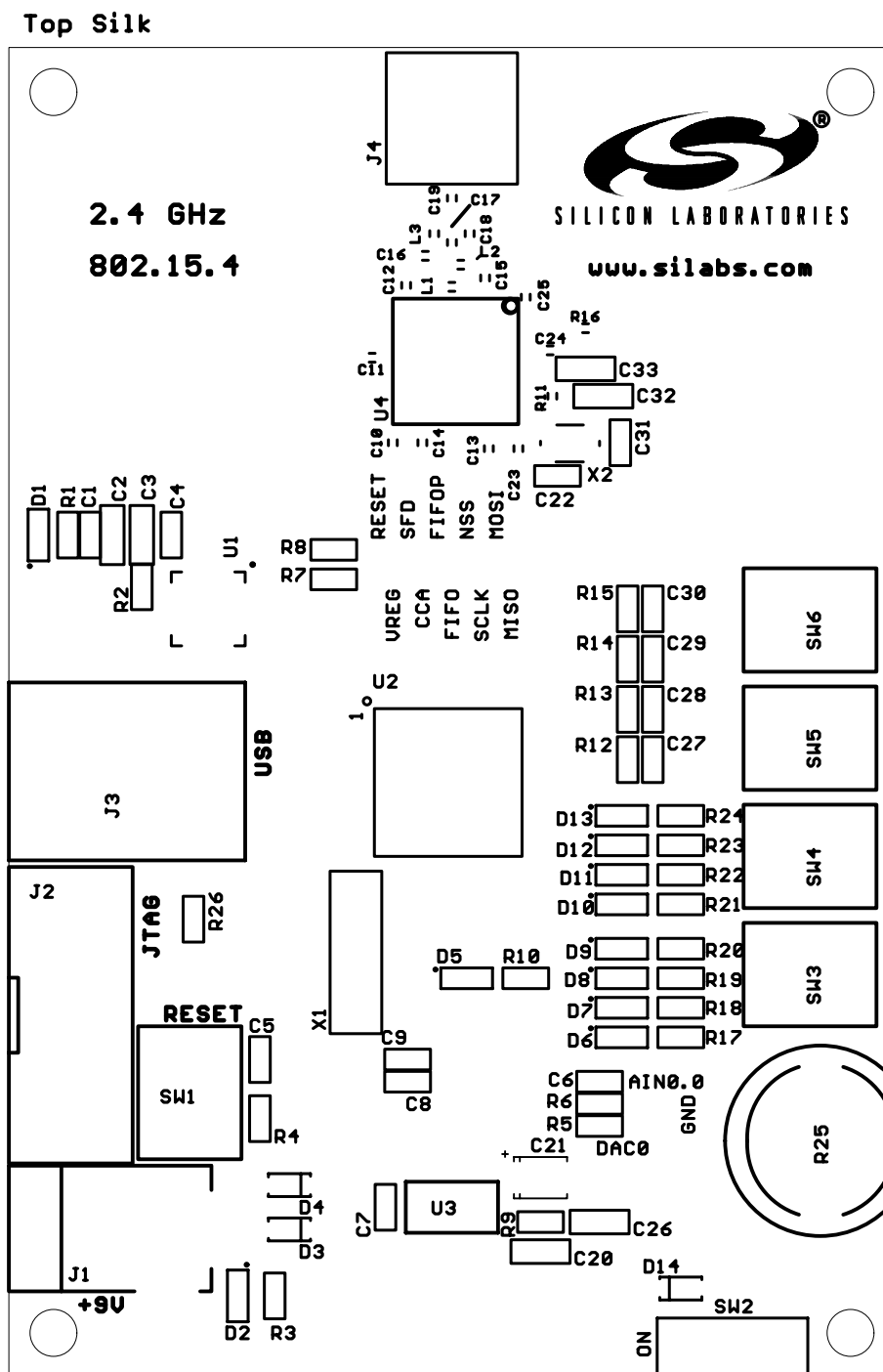


Figure 1. Top Silk Screen

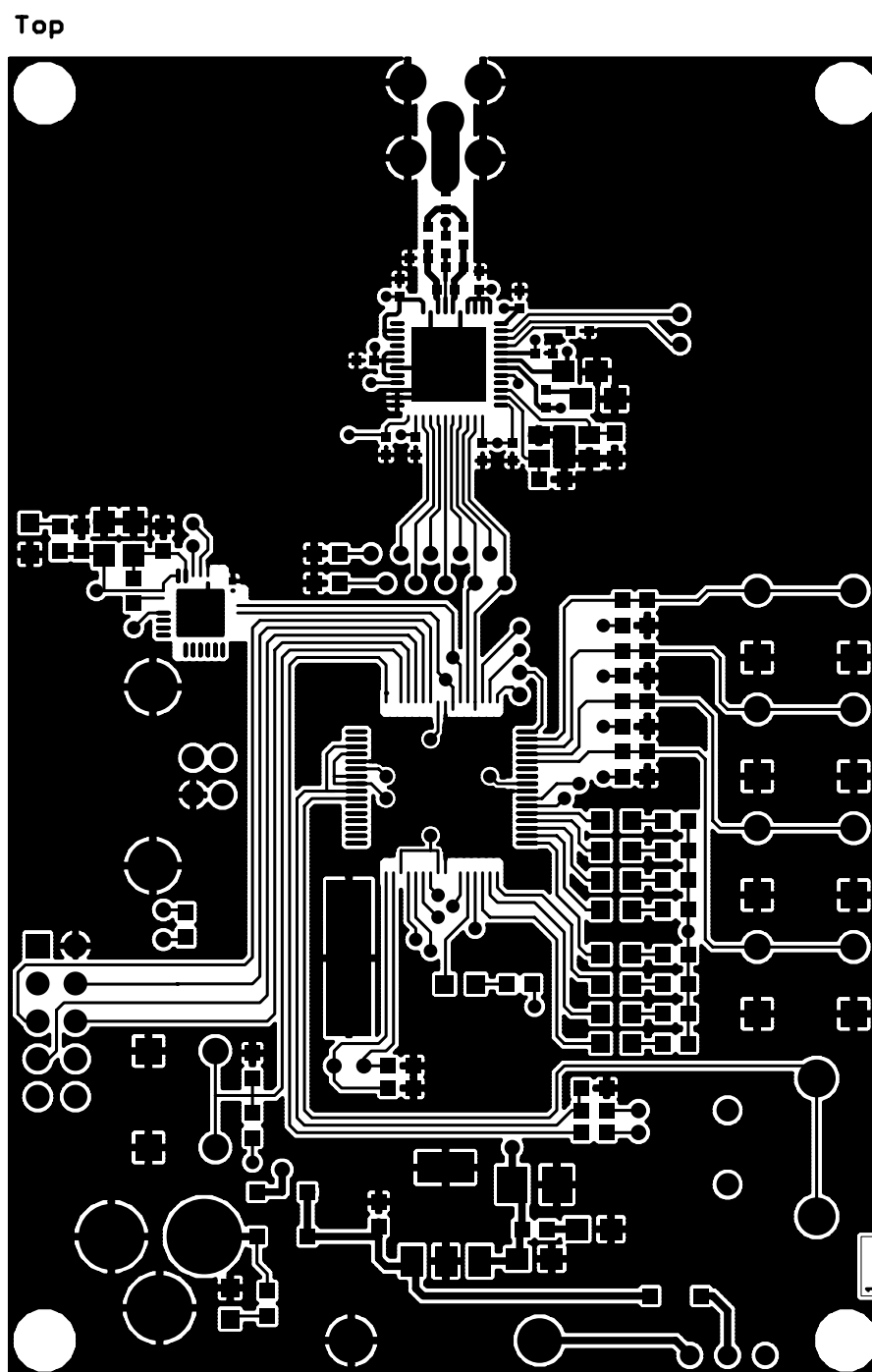


Figure 2. Layer 1 (Top)

Layer 2 (Inner Top)

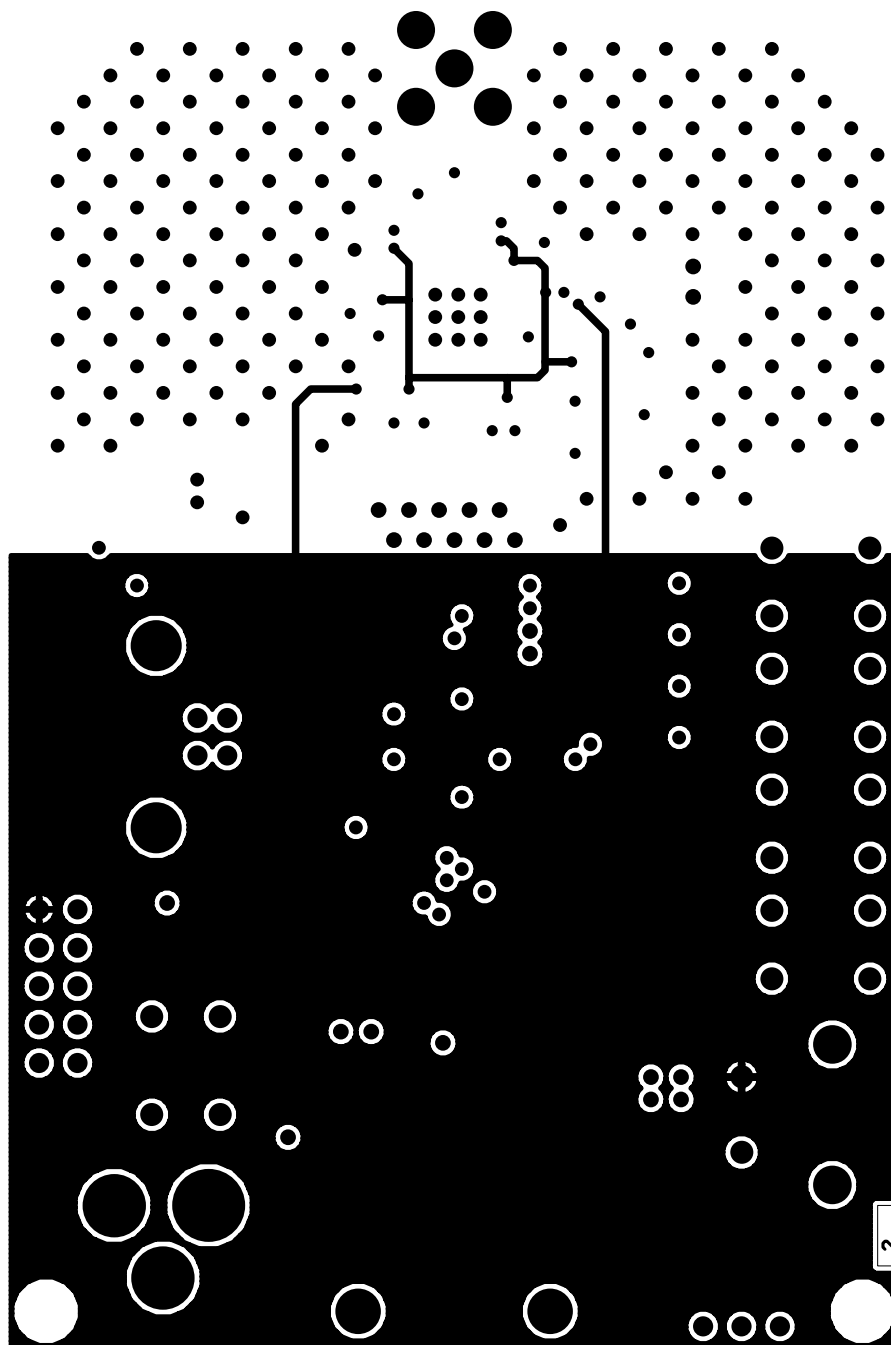


Figure 3. Layer 2 (Inner Top)

Layer3 (Inner Bottom)

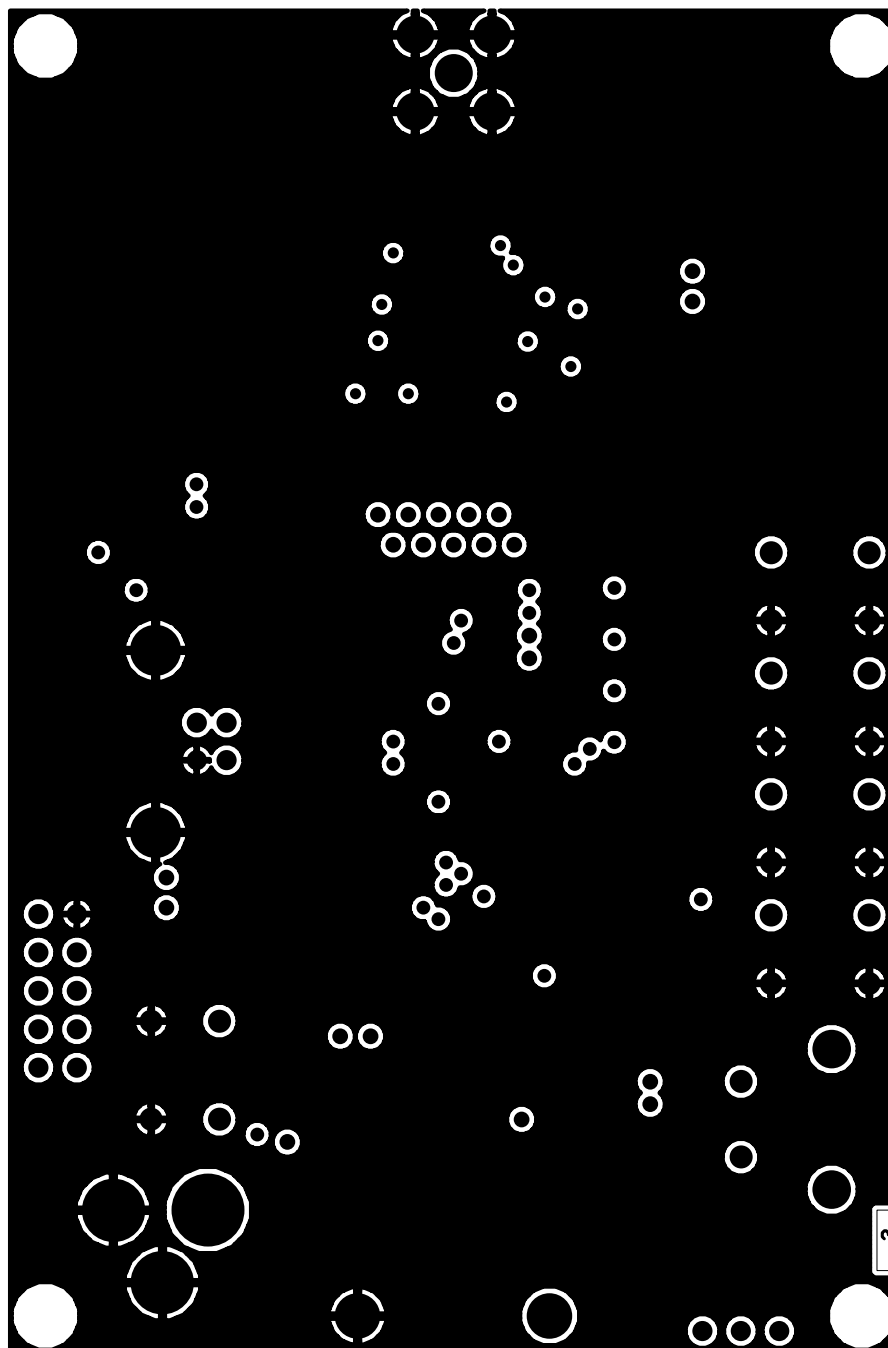


Figure 4. Layer 3 (Inner Bottom)

Bottom

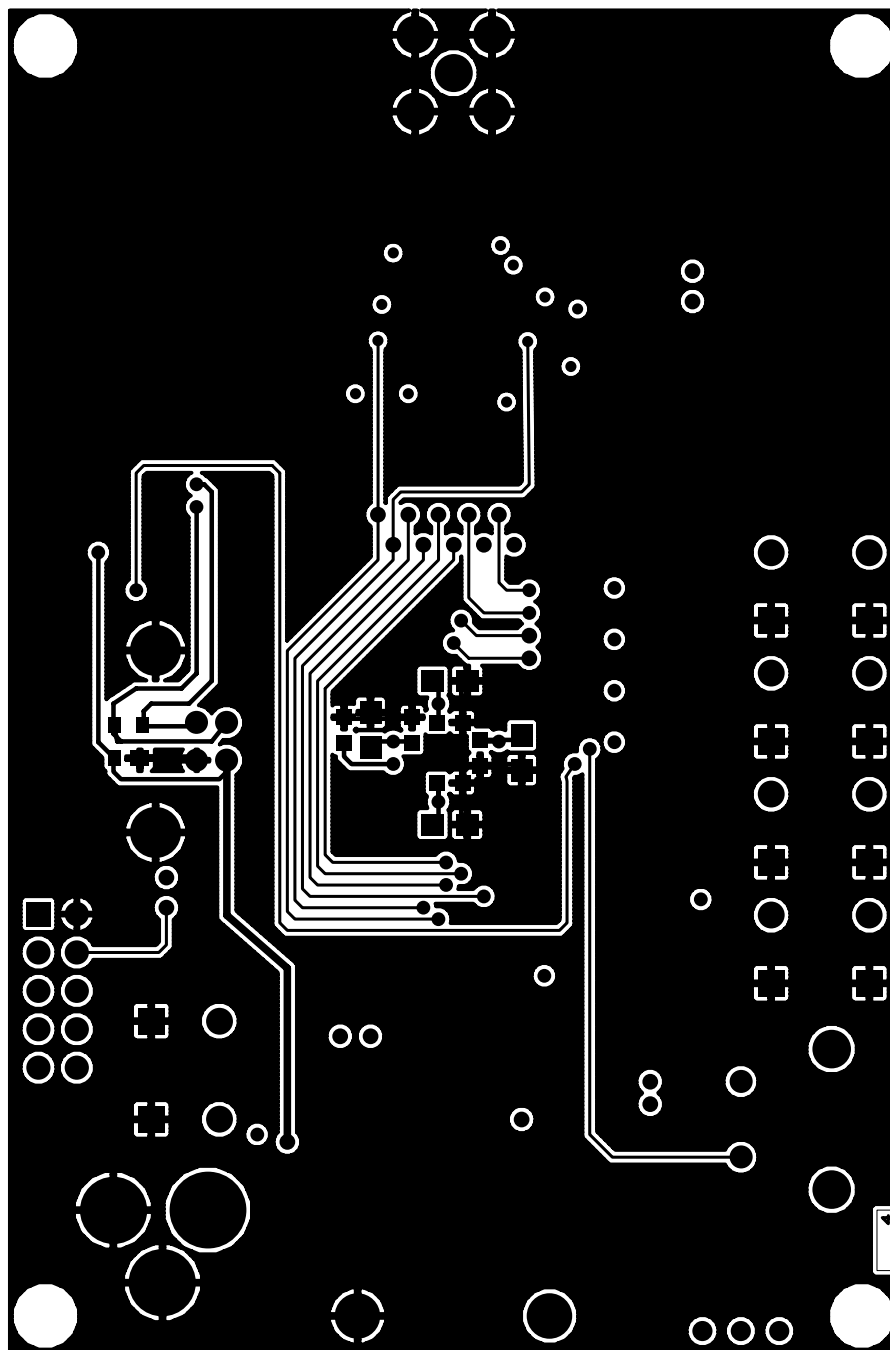


Figure 5. Layer 4 (Bottom)

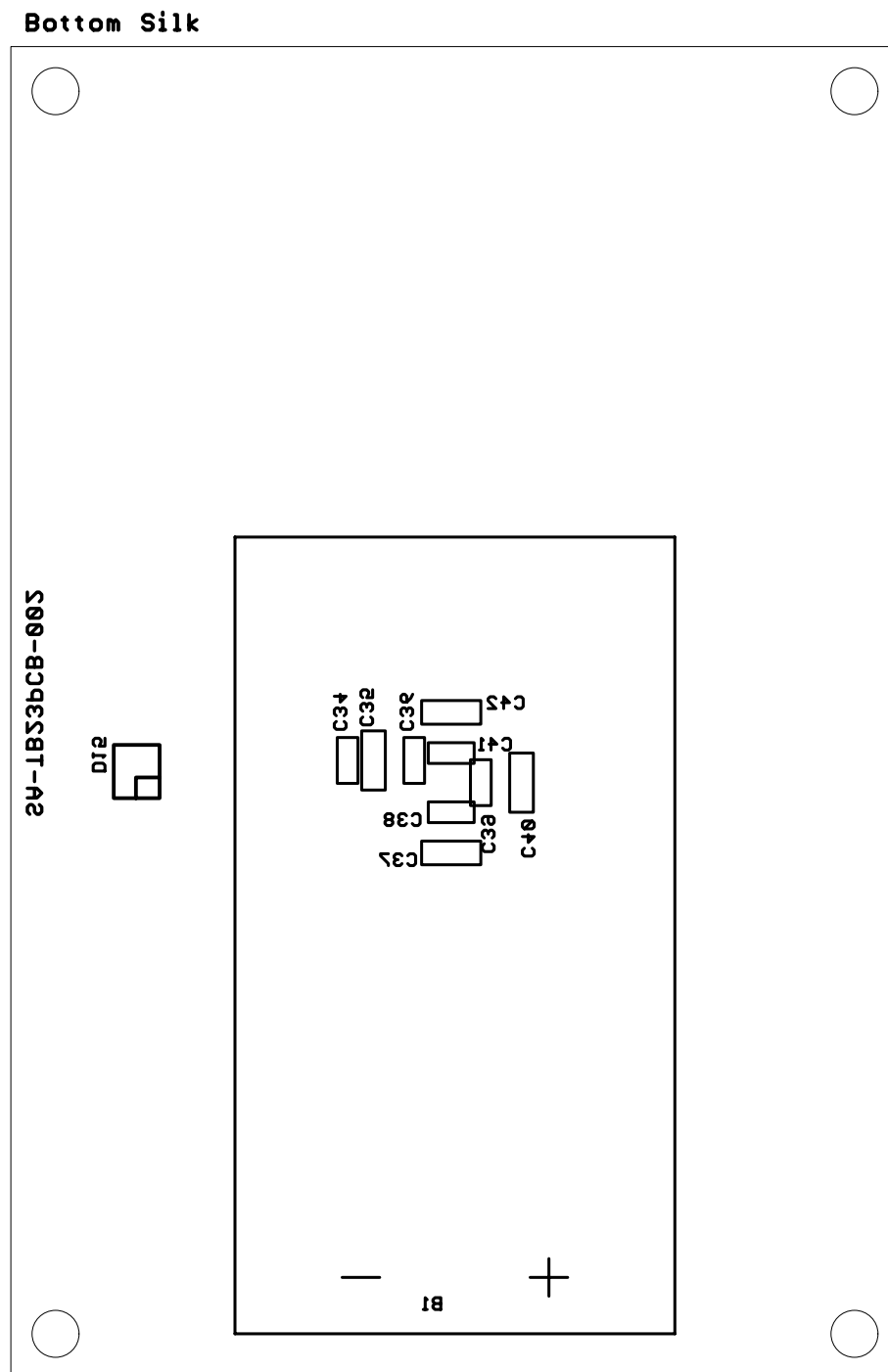


Figure 6. Bottom Silk Screen

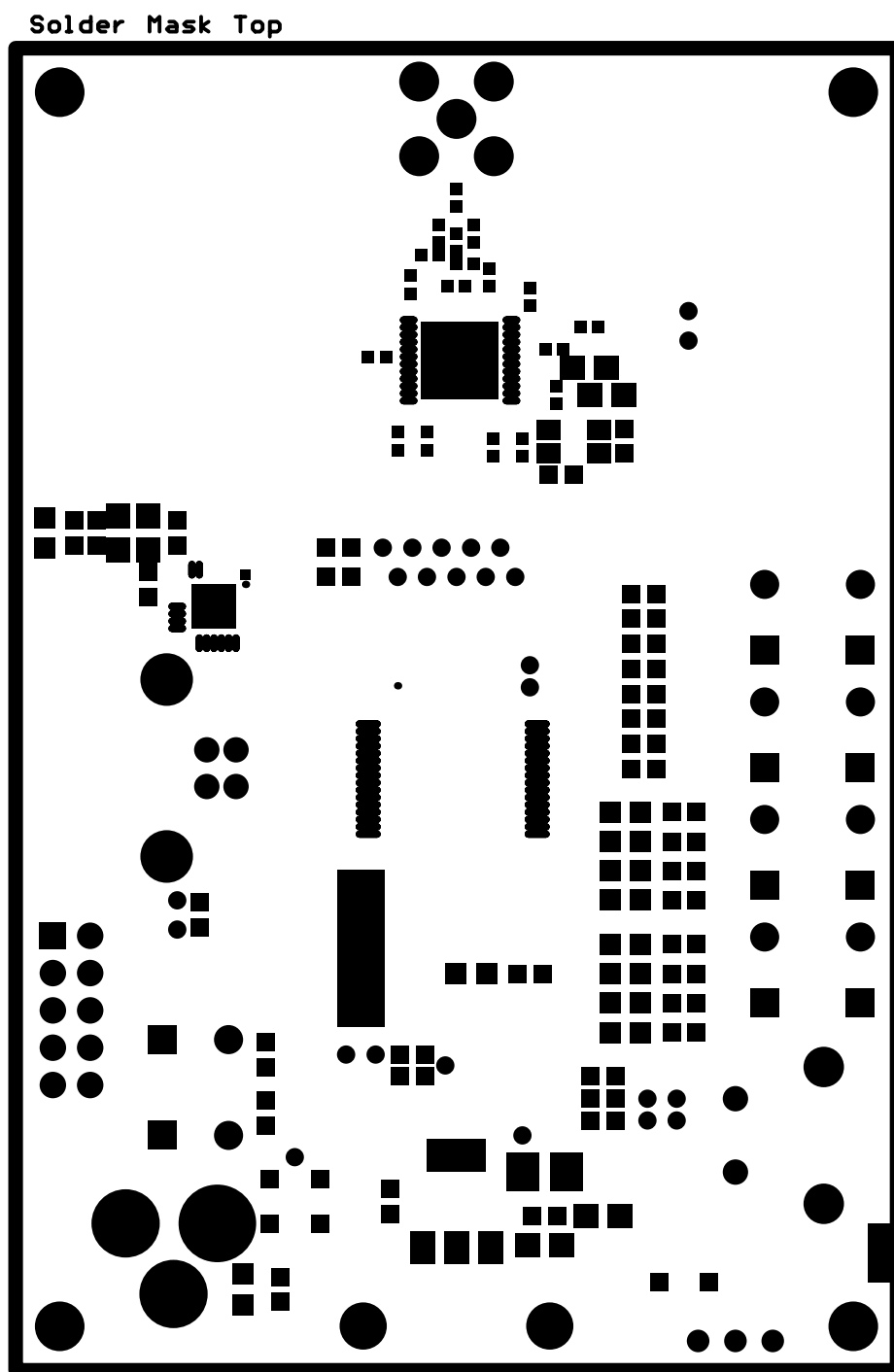


Figure 7. Top Solder Mask

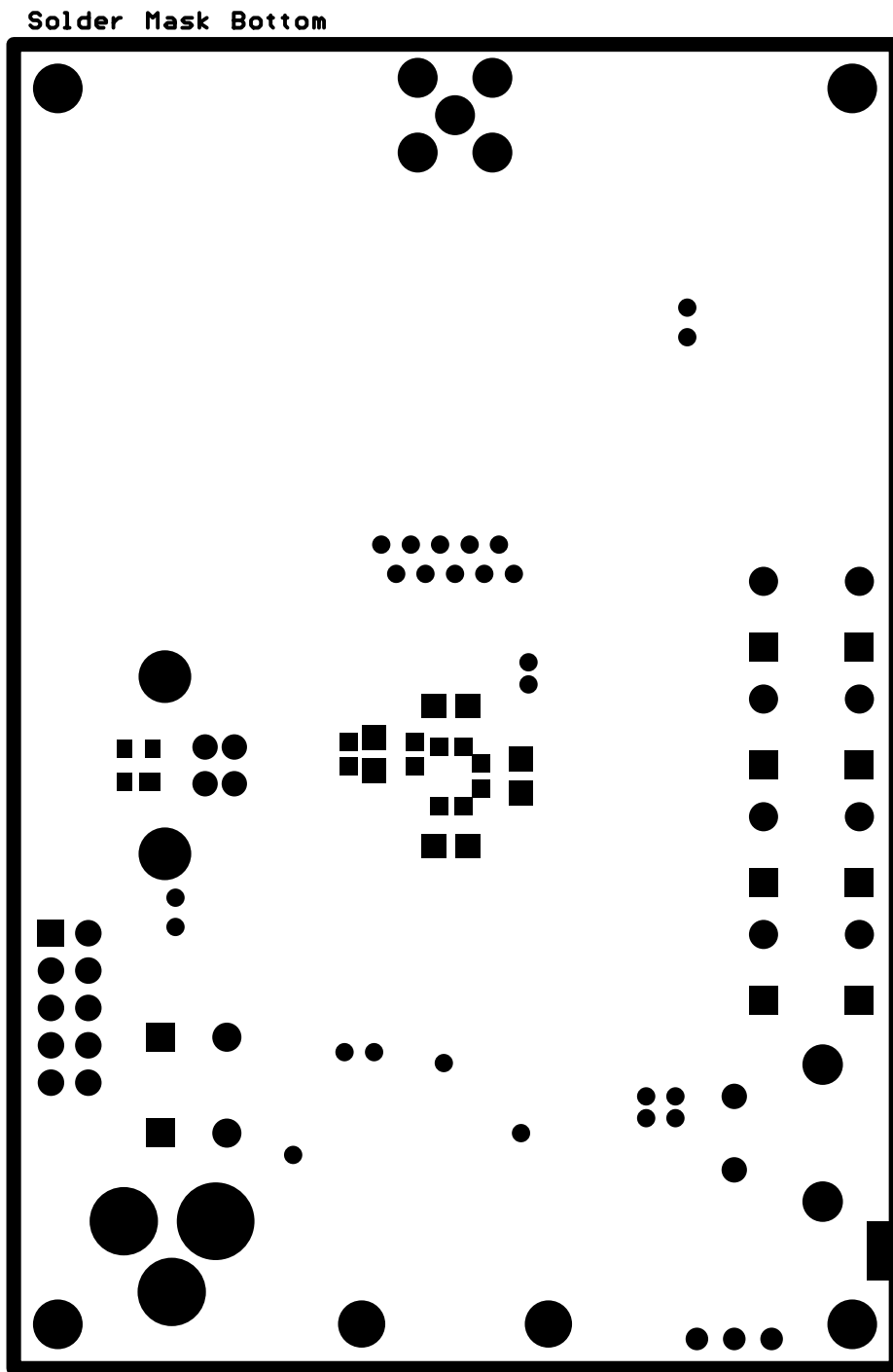


Figure 8. Bottom Solder Mask

NOTES:

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