Final Exam Report Template (ver 1.0)

Live URL: https://docs.google.com/document/d/1betiXh_42RHGMyzHDpVCAALihf4BIKYW2BVRw-4wTdk

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(if done as team)
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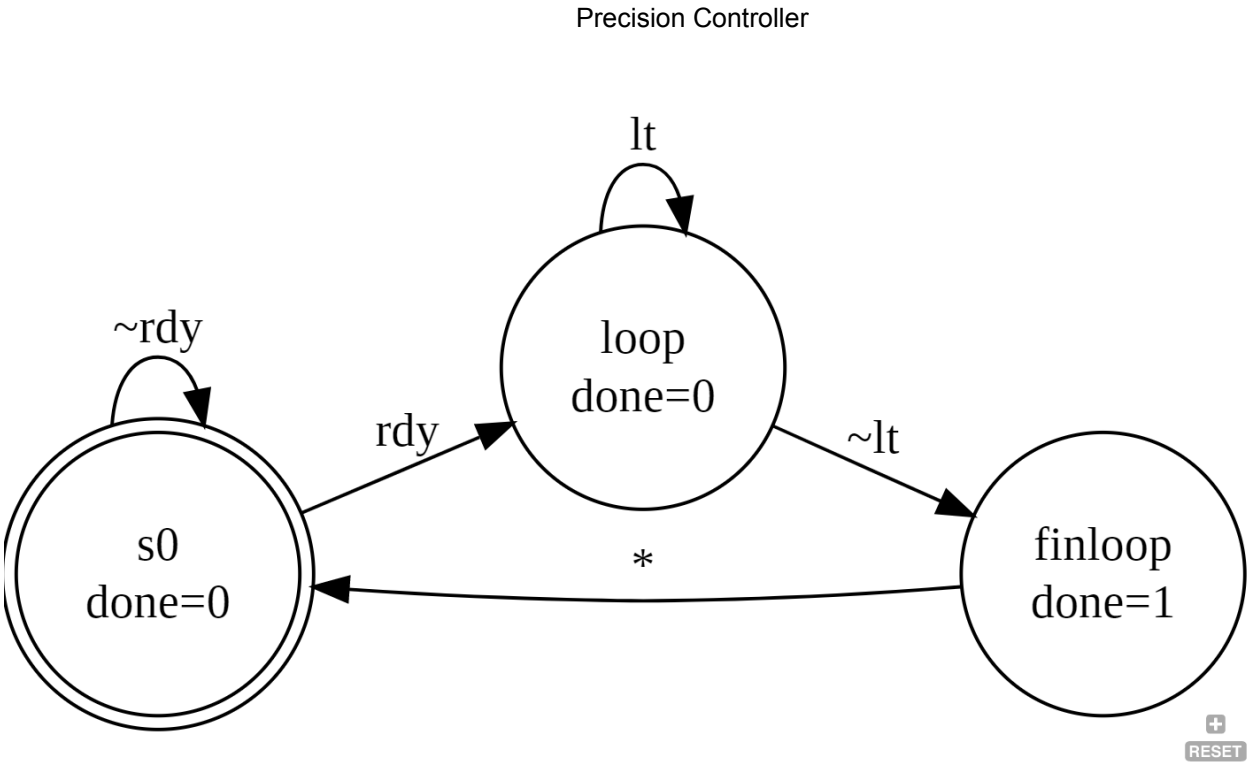
Task 1: Euclidean Distance Computer

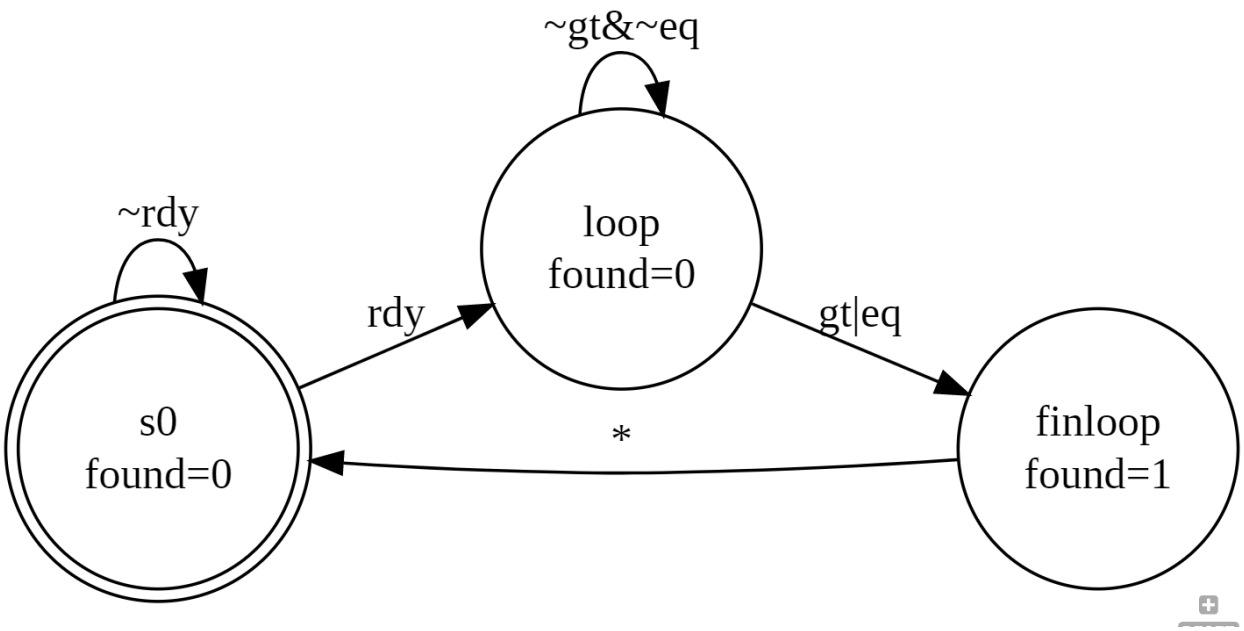
Architecture showing Datapath, Controller, and Main Signals

<one or more images showing the datapath structure and how it interacts with the controller FSM(s)>

State Transition Diagram (for every FSM in Controller)



Square Root Controller



State Transition Tables (for every FSM)

Square Root FSM:

```
#Automatic compact state assignment: {'s0': 0, 'loop': 1, 'finloop': 2} using 2 bits
# State Assignment: {'s0': 0, 'loop': 1, 'finloop': 2}
eq rdy gt curstate[1..0] | found nxtstate[1..0]
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
 -   0  -             00 |     0             00
 -   1  -             00 |     0             01
 0   -  0             01 |     0             01
 1   -  1             01 |     0             10
 1   -  0             01 |     0             10
 0   -  1             01 |     0             10
 -   -  -             10 |     1             00
```

Precision FSM:

```
#Automatic compact state assignment: {'s0': 0, 'loop': 1, 'finloop': 2} using 2 bits
# State Assignment: {'s0': 0, 'loop': 1, 'finloop': 2}
lt rdy curstate[1..0] | done nxtstate[1..0]
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
 -   0             00 |     0             00
 -   1             00 |     0             01
 1   -             01 |     0             01
 0   -             01 |     0             10
 -   -             10 |     1             00
```

State Encoding

For every FSM describe how you encoded the states into bit vectors and why you picked this encoding.

Square Root fsm - gray code, it was a small amount of states so I did this
Precision fsm - again, small amount of states

Circuit Area

Total Circuit Area = *42562*

Distance Computation Delay (in clock cycles)

The "delay" of your circuit is the # of clock cycles between both points being available to the system (i.e., the clock edge at which your system sees the latter of $GO1 = 1$ and $GO2 = 1)$ and when the result is seen by the external work (i.e., the clock edge at which is sees $DONE = 1$). Note that we will validate what you write below using the Autogtader

Fill the table below for the 10 test cases with the $DIST$ that your system computer and the delay it had.

$X1$	$Y1$	$X2$	$Y2$	$DIST$	DELAY (# of cycles)
-128	-128	-128	-128	0	
-128	-128	127	127		
-128	-128	0	0		
-128	-128	127	-128		
-96	-96	-128	127		
0	0	127	127		
-63	-63	63	63		
-10	10	10	-10		
96	-96	63	63		
33	-33	050	50		

Average Delay for Distance Computation =
Median Delay for Distance Computation =
Best Case Delay for Distance Computation =
Worst Case Delay for Distance Computation =

Area-Delay Product

$Area \times Median\ Delay =$ <fill the product of you design's area and the median delay in # of clock cycles>

Design Approach

Give a brief description of your controller + datapath design approach, including how you split between the two, what is the information exchange between them, how are the two coordinated, and how did you try to optimize for area and delay.

The controller waits until all of the go's are asserted, then it tells the square root calculator datapath to begin. When the square root datapath finishes, it tells the controller that it is finished, and then the square root controller tells the precision controller to begin. The precision fsm works by adding 0.0001 to the square root calculated by the square root datapath until the value of this to the power of 2 is greater than or equal to the actual value that we took the square root of. Then, it subtracts 0.0001 and asserts DONE=1.

Testing Approach

Give a brief description of how you tested your design, including description or screenshots of any testing circuit that you created.

I tested different number combinations by hand, making sure each one worked.

Additional Remarks

Reset is implemented synchronously, but it is not an input/part of the truth table for the controller fsm's.