Dual Channel Output LCD Bias Power

General Description

The LP6280S boost converter is designed to supple bias power positive/negative output source driver application. It has wide input voltage range of 2.5V to 5.5V and output currents up to 150mA.

The LP6280S is a high efficiency synchronous boost converter, which is based on current mode topology, fixed frequency to regulate output voltage. Other features include under-voltage lockout (UVLO), internal soft start, current limit protection, thermal shutdown protection.

The LP6280S is available in a space saving WLCSP 15-ball (0.4mm pitch) package.

Order Information

LP6280S □□ □

- F: Pb-Free
- Package Type
  HV: WLCSP-15

Features

- 2.5V to 5.5V Input Supply Voltage Range
- Output Current up to 150mA
- Up to 85% Efficiency
- Programmable Output Voltages
  - VOP Output Voltage : 4V to 6V with 0.1V step
  - VON Output Voltage :-4V to -6V with 0.1V step
- ENP/ENN Power on Sequence Control.
- Built-in Soft Start
- Over-Current Protection
- Over-Temperature Protection
- WLCSP 15-ball (1.17mm x 1.94mm) Package
- RoHS Compliant and Halogen Free
- Pb-Free Package

Applications

- TFT LCD Smartphone and Tablets
- White Brand MID
- DAC Supply
- OLED Displays

Marking Information

Device	Marking	Package	Shipping
LP6280S	LPS LP6280S YWXXX	WLCSP-15	3K/REEL
Y is year code. W is week code. XXX is series number.			

Typical Application Circuit

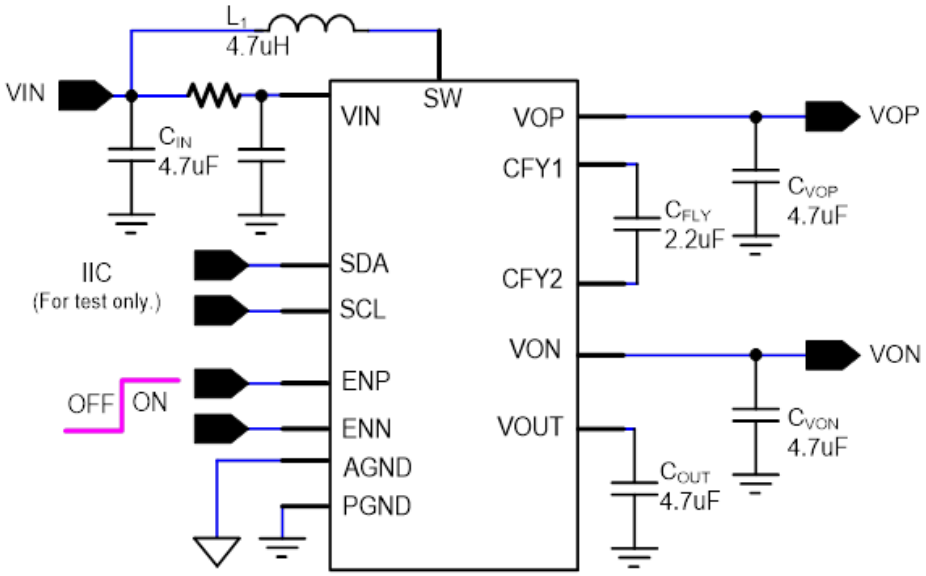

Figure 1. Typical Application Circuit of LP6280S

Function Block Diagram

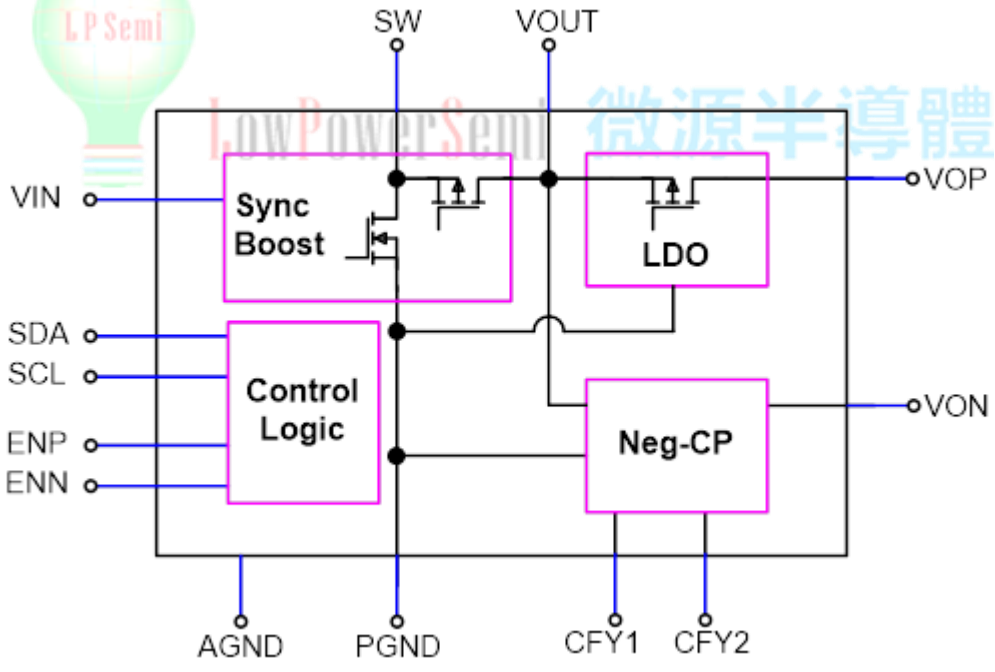

Figure 2. Internal Function Block Diagram

Pin Configuration

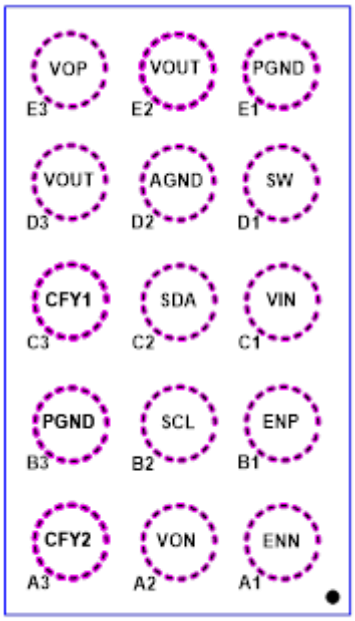

Figure 3. WLCS-15-Ball (1.17mm x 1.94mm) Top View

Functional Pin Description

Pin No.	Pin Name	Description
A1	ENN	Logic control shutdown input for VON power control.
A2	VON	Negative voltage output.
A3	CFY2	Negative input for the external flying capacitor. Connect a ceramic 2.2μF capacitor close to the pins of the IC
B1	ENP	Logic controlled shutdown input for VOP power control.
B2	SCL	IIC interface clock signal. (This pin is for production test only, no connection)
B3,E1	PGND	Boost converter power ground.
C1	VIN	Input supply pin. Decouple with 4.7μF ceramic capacitor close to the pin.
C2	SDA	IIC interface data signal. (This pin is for production test only, no connection)
C3	CFY1	Positive input for the external flying capacitor. Connect a ceramic 2.2μF capacitor close to the pins of the IC
D1	SW	Power switching output. Connect an external inductor to this switching node.
D2	AGND	Analog ground. Control circuitry returns current to this pin.
D3,E2	VOUT	Output of the synchronous rectifier. Decouple with an external capacitor. At least 4.7μF is recommended. Higher capacitor values reduce output ripple.
E3	VOP	Positive voltage output.

Absolute Maximum Ratings Note 1

- ✧ Supply Voltage: VIN, VCFLY1 ---------- -0.3V to +7V
- ✧ Enable Voltage: VENN, VENP ---------- -0.3V to VIN+0.3V
- ✧ Positive Output Voltage: VOUT, VOP ---------- -0.3V to +7V
- ✧ Negative Output Voltage: VON, VCFY2 ---------- +0.3V to -7V
- ✧ SW Voltage: VSW ---------- -0.3V to +7V
- ✧ IIC Bus Voltage: VSDA, VSCL ---------- -0.3V to +7V
- ✧ Operating Junction Temperature Range (T_J) ---------- -40℃ to 150℃
- ✧ Operation Ambient Temperature Range ---------- -40℃ to +85℃
- ✧ Storage Temperature Range ---------- -65℃ to +150℃
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- +260℃

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Thermal Resistance

  WLCSP 15-ball (1.4mm x 2.3mm), θ_{JA} ---------- 95℃/W

  WLCSP 15-ball (1.4mm x 2.3mm), θ_{JC} ---------- 1℃/W

ESD Susceptibility

- ✧ HBM(Human Body Mode) Note 2 ---------- 2KV
- ✧ MM(Machine Mode) Note 3 ---------- 200V

Note 2. The Human body model (HBM) is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The testing is done according JEDEC.
Note 3. Machine Model (MM) is a 200pF capacitor discharged through a 500nH inductor with no series resistor into each pin. The testing is done according JEDEC.

Electrical Characteristics

(T_A=25℃, V_{IN}=3.7V, V_{OP}=5.5V, V_{ON}=–5.5V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
General						
Input UVLO Threshold	$V_{UVLO(VTH)}$	V_{IN} rising	2.1	2.3	2.5	V
Under Voltage Lockout Threshold Hysteresis	$V_{UVLO(HYS)}$	V_{IN} falling		200		mV
Quiescent Current	I_Q	No Load.		1	2	mA
		ENN=ENP=GND		5		uA
High-Side MOSFET Leakage Current	$I_{SW(leak)}$	V_{SW}=6.5V, V_{OUT}=0V			10	μA
Low-Side MOSFET Leakage Current		V_{SW}=6.5V			10	μA
Oscillator Frequency	F_{OSC}		0.96	1.2	1.44	MHz
Switch Current Limit	I_{LIM}			1.5		A
Maximum Duty Cycle	D_{MAX}			90		%
Thermal Shutdown Temperature	T_{SD}			140		℃
Thermal Shutdown Hysteresis				10		℃
Positive Output Voltage						
Positive Output Voltage Range	V_{OP}	21 steps, each step=100mV	4		6	V
Output Voltage Accuracy		No load	-1.5		+1.5	%
Positive Output Current	I_{OP}				150	mA
Dropout voltage	V_{DROP}	V_{OP}=5V, I_{OP}=120mA		160		mV
Load Regulation		I_{OP}=10mA to 40mA, V_{OP}=5V		1		%
Line Regulation		V_{IN}=2.5V~4.2V, I_{OP}=40mA		1		%
VOP Discharge Resistor	R_{DIS_P}			140		Ω
ENP Logic Low	$V_{ENP(L)}$				0.5	V
ENP Logic High	$V_{ENP(H)}$		1.5			V
ENP Pin Current	I_{ENP}	V_{ENP}=2V		10		μA
Negative Output Voltage						
Negative Output Voltage Range	V_{ON}	21 steps, each step=100mV	-6		-4	V
Output Voltage Accuracy		No load	-1.5		+1.5	%
Negative Output Current	I_{ON}				-150	mA
UVP Threshold Voltage on AVEE Pin		VOP falling under target percentage		60		%
Charge Pump Switching Frequency	F_{CP}		0.8	1	1.2	MHz
Load Regulation		I_{ON}=-10mA to -40mA, V_{ON}=-5V		1		%
Line Regulation		V_{IN}=2.5V~4.2V, I_{OP}=-40mA		1		%
VON Discharge resistor	R_{DIS_N}			10		Ω
ENN Logic Low	$V_{ENN\ (L)}$				0.5	V
ENN Logic High	$V_{ENN\ (H)}$		1.5			V
ENN Pin Current	I_{ENN}	V_{ENN}=2V		10		μA

Typical Performance Curves

T_A=+25℃, unless otherwise noted.

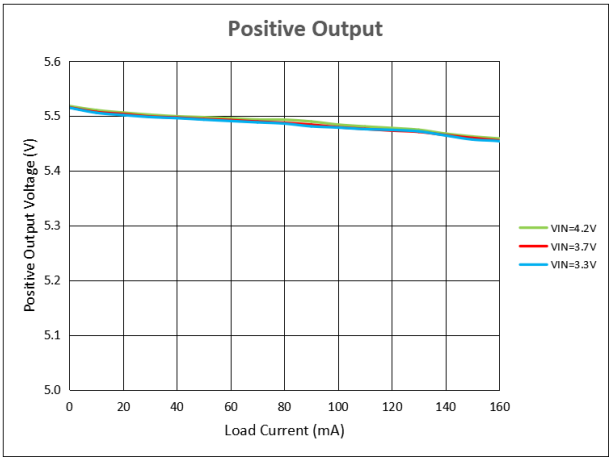

Figure 4. Positive Output Load Regulation

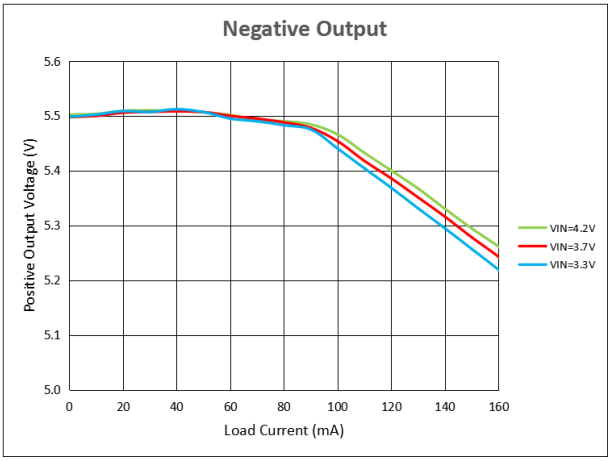

Figure 5. Negative Output Load Regulation

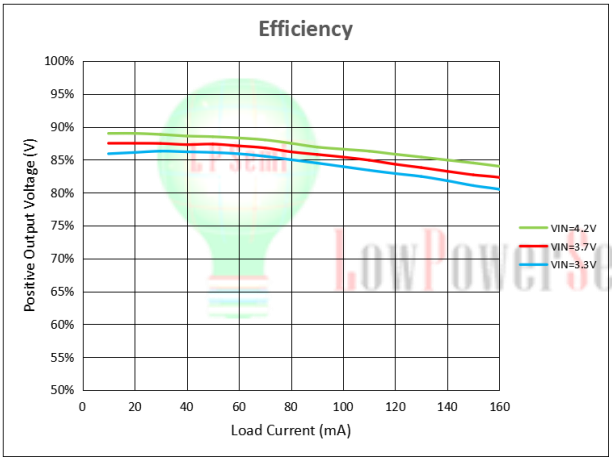

Figure 6. Output Efficiency

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Application Information

The LP6280S is a dual channel power sources for LCD panel. It contains a boost, a LDO and a negative charge pump. The output voltage of boost converter is VOUT. The LDO generates the positive voltage(VOP) and the negative charge pump generates the negative voltage(VON), both are regulating through VOUT.

Under Voltage Lockout (UVLO)

The LP6280S had an UVLO internal circuit that enable the device once the voltage on the VIN voltage exceeds the UVLO threshold voltage.

Power Sequencing

The LDO (VOP) and the negative charge pump (VON) are turn on/off by external signal. ENP is for VOP and ENN is for VON. Beside, any enable signal turn on, the boost will be power on.

Boost Converter

The LP6280S integrates a PWM synchronous boost converter operating with current mode control. Switching frequency is 1.2MHz (typ.). The device is designed for high efficiency over wide output current range.

VOP/N Discharge

When VIN falls below UVLO threshold or ENP/ENN becomes low, all converter will be turns off. Both ENP and ENN go low, VOP/VON will be actively discharged to GND.

Over Temperature Protection

The LP6280S device enters over temperature protection if its junction temperature exceeds 140℃ (typical). During over temperature protection none of the device's functions are available. To resume normal operation the junction temperature need cool down, and the outputs will restart.

Layout Consideration

The proper PCB layout and component placement are critical for all circuit. The careful attention should be prevent electromagnetic interference (EMI) problems. Here are some suggestions to the layout of LP6280S design.

1. Connected all ground together with one uninterrupted ground plane, which include power ground and analog ground.
2. The input capacitor should be located as closed as possible to the VIN and ground plane.
3. Minimize the distance of all traces connected to the LX node, that the traces short and wide route to obtain optimum efficiency.
4. All output capacitor should be located as closed as possible to the output and ground plane.
5. The CFLY should be placed close to IC's CFLY1 and CFLY2 pins.

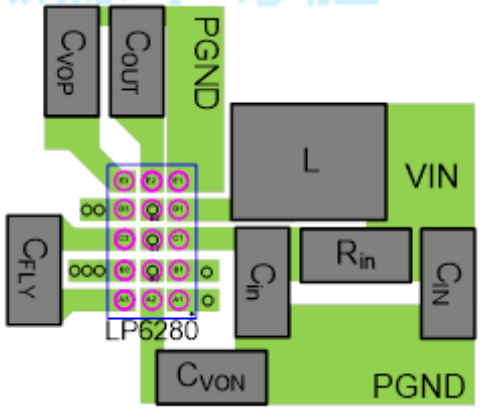


Figure 7. Recommended PCB Layout Diagram

Application Information (Continued)

1. IIC Interface Specification

The LP6280S can easily modify parameters by IIC bus, that slave address is 0x3EH.

IIC is a two wire serial interface developed, the bus consists of a clock line(SCL) and a data line(SDA) with pull-up structures. The LP6280S works as a slave mode, and address is 3E. The data transfer protocol is follow IIC-Bus Specification's standard mode(100kbps) and fast mode(400kbps).

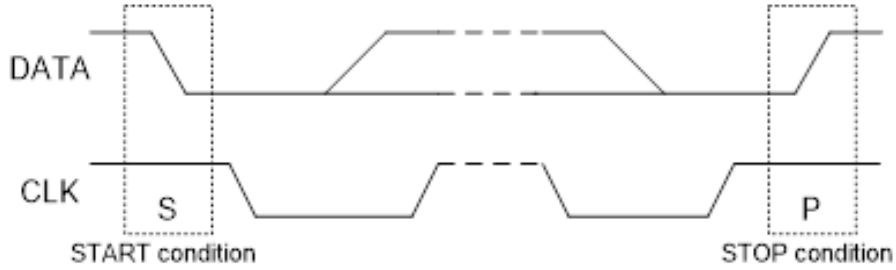


Figure 8. START and STOP Conditions

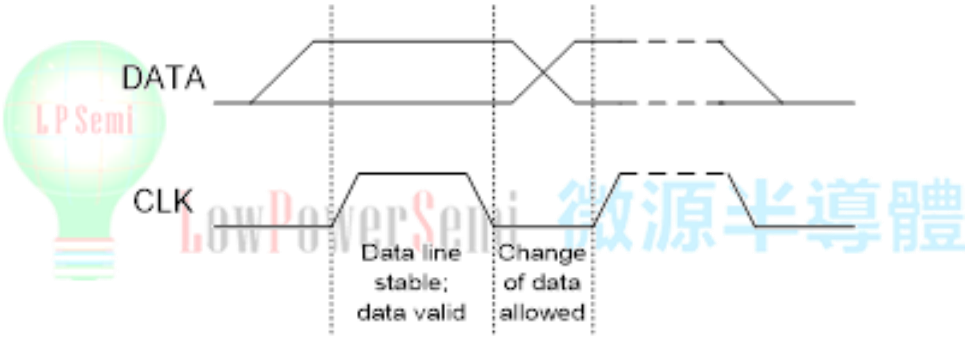


Figure 9. Bit Transfer on the Serial Interface

2. Write Data to Register

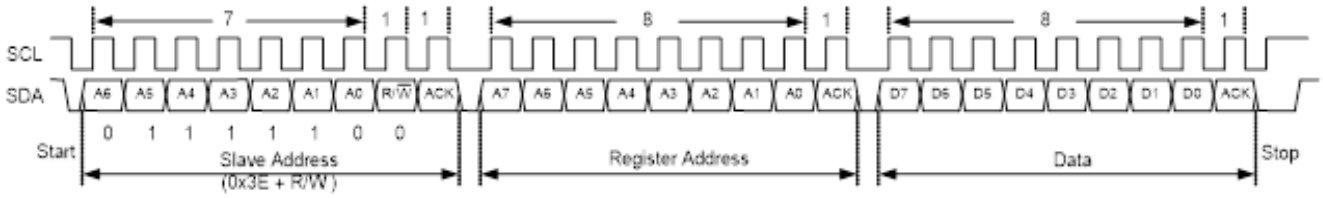


Figure 10. Write Single Byte Data to Register

3. Read Data to Register

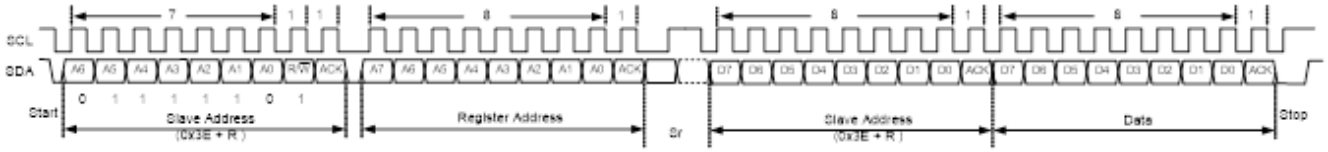


Figure 11. Read Single Byte Data from Register

Application Information (Continued)

4. IIC REGISTER MAP

The lowest bit number (0) represents the least bit, the highest bit number (7) represents the most bit, and R/W indicates whether the bit is read only (R), write only (W), or both read and write (R/W).

Address	Description	Default	D7	D6	D5	D4	D3	D2	D1	D0
00H	Positive Output VOP Voltage	0FH	--	--	--	**VOP [4:0]**				
01H	Negative Output VON Voltage	0FH	--	--	--	**VON [4:0]**				
03H	DIS_VOP:VOP Discharge Resistor Enable or Disable DIS_VON:VON Discharge Resistor Enable or Disable	03H	--	--	--	--	--	--	**DIS_ VOP**	**DIS_ VON**
FFH	Data registers write controller.	00H	**Wr**	--	--	--	--	--	--	--

Set VOP Output Voltage (Register Address – 00H)

VOP Voltage							
Addr: 00H	**Default Value : VOP(Register)=0x0FH, VOP =5.5V**						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	VOP[4]	VOP [3]	VOP [2]	VOP [1]	VOP [0]

VOP [4:0]			
Register	**Volt (V)**	**Register**	**Volt (V)**
00000	4.00	10000	5.60
00001	4.10	10001	5.70
00010	4.20	10010	5.80
00011	4.30	10011	5.90
00100	4.40	10100	6.00
00101	4.50	10101	6.00
00110	4.60	10110	6.00
00111	4.70	10111	6.00
01000	4.80	11000	6.00
01001	4.90	11001	6.00
01010	5.00	11010	6.00
01011	5.10	11011	6.00
01100	5.20	11100	6.00
01101	5.30	11101	6.00
01110	5.40	11110	6.00
01111	5.50	11111	6.00

Application Information (Continued)

Set VON Voltage (Register Address – 01H)

VON Voltage							
Addr: 01H	**Default Value : VON(Register)=0x0FH, VON =-5.5V**						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	VON[4]	VON [3]	VON [2]	VON [1]	VON [0]

VON [4:0]			
Register	**Volt (V)**	**Register**	**Volt (V)**
00000	-4.00	10000	-5.60
00001	-4.10	10001	-5.70
00010	-4.20	10010	-5.80
00011	-4.30	10011	-5.90
00100	-4.40	10100	-6.00
00101	-4.50	10101	-6.00
00110	-4.60	10110	-6.00
00111	-4.70	10111	-6.00
01000	-4.80	11000	-6.00
01001	-4.90	11001	-6.00
01010	-5.00	11010	-6.00
01011	-5.10	11011	-6.00
01100	-5.20	11100	-6.00
01101	-5.30	11101	-6.00
01110	-5.40	11110	-6.00
01111	-5.50	11111	-6.00

Set Discharge Resistor Enable (Register Address – 03H)

Discharged Resistor Enable/Disable							
Addr: 03H	**Default Value : DIS_VO(Register)=0x03H**						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	DIS_VOP	DIS_VON

DIS_VOP		DIS_VON	
Register	DIS_VOP	Register	DISP_VOP
0	Disable	0	Disable
1	Enable	1	Enable

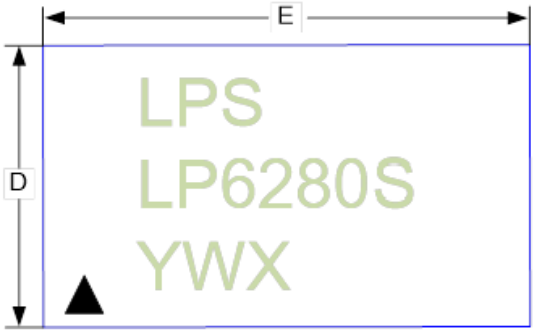
Set Control Register (Register Address – FFH)

Control Register							
Addr: FFH	**Write : Control(Register)=0x80H, Read : Control(Register)=0x00H**						
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R
W_EPROM	0	0	0	0	0	0	0

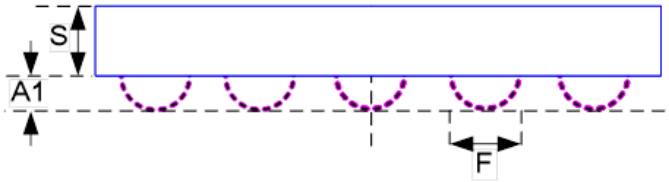
W_EPROM	
Register	Bit Description
0	Disable any registers data write into the EPROM
1	Enable all register's data to write into the EPROM

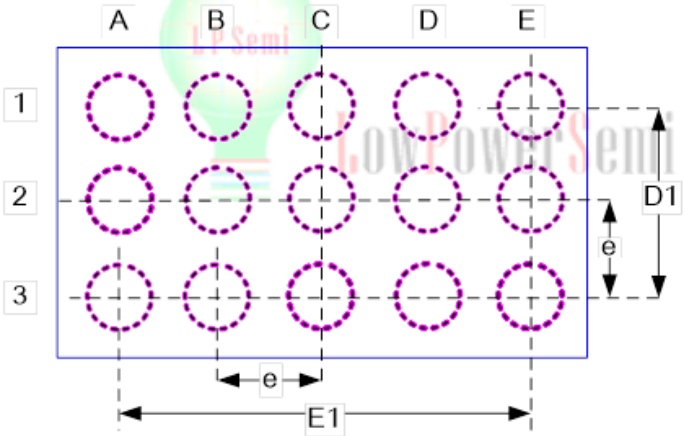
Packaging Information

WLCSP-15-ball Package (1.17×1.94) pitch 0.4 (Unit: mm)

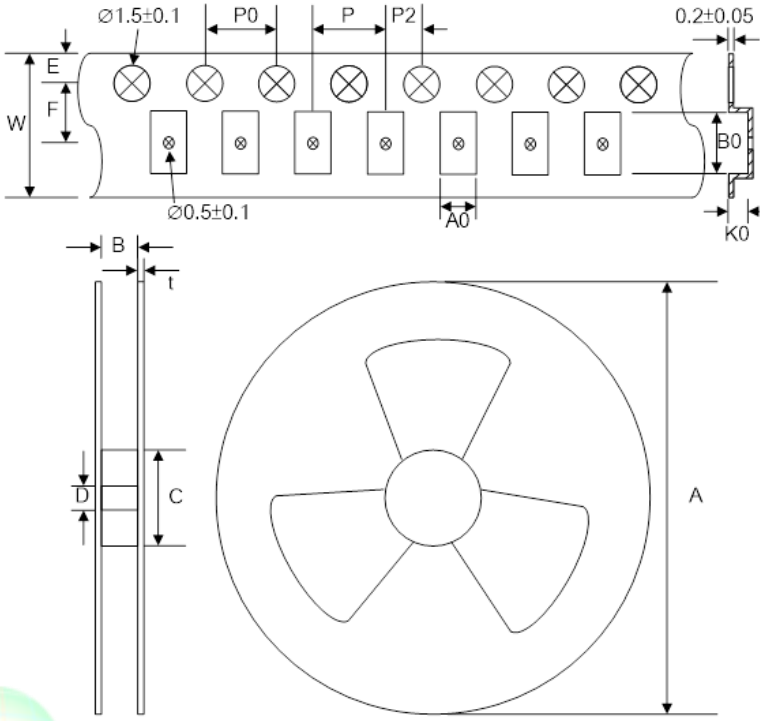


SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
D	1.145	1.185
E	1.915	1.955
S	0.402	0.428
D1	0.750	0.850
E1	1.550	1.650
A1	0.165	0.205
F	0.210	0.250
e	0.4	





Carrier Dimensions



Device	Package Type		Pins	SPQ	A (mm)	B (mm)	C (mm)	D (mm)	t (mm)
LP6280S	WLCSP		15	3000	ø180±1	9.5±0.5	ø60±1	ø13±0.2	1.1±0.25
	W (mm)	E (mm)	F (mm)	P (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P2 (mm)
	8±0.3	1.75±0.1	3.5±0.05	4	1.82±0.05	2.74±0.05	0.75±0.05	4	2