

### VND5160AJ-E

# Double channel high side driver with analog current sense for automotive applications

#### **Features**

Max supply voltage	$V_{CC}$	41 V
Operating voltage range	V <sub>CC</sub>	4.5 to 36V
Max on-state resistance (per ch.)	R <sub>ON</sub>	160 mΩ
Current limitation (typ)	I <sub>LIMH</sub>	5 A
Off state supply current	Is	2 μA <sup>(1)</sup>

- 1. Typical value with all loads connected.
- General features
  - Inrush current active management by power limitation
  - Very low stand-by current
  - 3.0V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/EC European directive
- Diagnostic functions
  - Proportional load current sense
  - High current sense precision for wide range currents
  - Current sense disable
  - Thermal shutdown indication
  - Very low current sense leakage
- Protection
  - Undervoltage shut-down
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V<sub>cc</sub>
  - Thermal shut down



- Reverse battery protection (see Application schematic)
- Electrostatic discharge protection

#### **Application**

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

#### **Description**

The VND5160AJ-E is a monolithic device made using STMicroelectronics VIPower technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS\_DIS is driven low or left open. When CS\_DIS is driven high, the CURRENT SENSE pin is in a high impedance condition. Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

#### Table 1. Device summary

Packago	Order codes		
Package	Tube	Tape and Reel	
PowerSSO-12	VND5160AJ-E	VND5160AJTR-E	

Contents VND5160AJ-E

## **Contents**

1	Block diagram and pin description				
2	Elec	trical specifications7			
	2.1	Absolute maximum ratings			
	2.2	Thermal data 8			
	2.3	Electrical characteristics			
	2.4	Electrical characteristics curves			
3	Арр	lication information			
	3.1	GND protection network against reverse battery			
		3.1.1 Solution 1 : resistor in the ground line (RGND only)21			
		3.1.2 Solution 2 : diode (DGND) in the ground line			
	3.2	Load dump protection			
	3.3	MCU I/Os protection			
	3.4	Maximum demagnetization energy (VCC = 13.5V)			
4	Pack	kage and PC board thermal data			
	4.1	PowerSSO-12 <sup>™</sup> thermal data			
5	Pack	kage and packing information			
	5.1	ECOPACK <sup>®</sup> packages			
	5.2	Package mechanical data			
	5.3	Packing information			
6	Revi	sion history			

VND5160AJ-E List of tables

# List of tables

Table 1.	Device summary	. 1
Table 2.	Pin function	. 5
Table 3.	Suggested connections for unused and N.C. pins	. 6
Table 4.	Absolute maximum ratings	. 7
Table 5.	Thermal data	. 8
Table 6.	Power section	. 9
Table 7.	Switching (VCC=13V, Tj=25°C)	. 9
Table 8.	Logic input	10
Table 9.	Protection and diagnostics	10
Table 10.	Current sense (8V <vcc<16v)< td=""><td>11</td></vcc<16v)<>	11
Table 11.	Truth table	
Table 12.	Electrical transient requirements	
Table 13.	Thermal parameters	26
Table 14.	PowerSSO-12™ mechanical data	
Table 15.	Document revision history	30

List of figures VND5160AJ-E

# **List of figures**

4/31

Figure 1.	Block diagram	
Figure 2.	Configuration diagram (top view)	. 6
Figure 3.	Current and voltage conventions	. 7
Figure 4.	Current sense delay characteristics	
Figure 5.	Delay response time between rising edge of ouput current and rising edge of current sen	se
	(CS enabled)	
Figure 6.	lout/isense vs. lout	14
Figure 7.	Maximum current sense ratio drift vs load current	14
Figure 8.	Switching characteristics	15
Figure 9.	Output voltage drop limitation	15
Figure 10.	Waveforms	17
Figure 11.	Off state output current	18
Figure 12.	High level input current	
Figure 13.	Input clamp voltage	18
Figure 14.	Input low level	18
Figure 15.	Input high level	18
Figure 16.	Input hysteresis voltage	
Figure 17.	On state resistance vs. T <sub>case</sub>	19
Figure 18.	On state resistance vs. V <sub>CC</sub>	19
Figure 19.	Undervoltage shutdown	19
Figure 20.	Turn-On voltage slope	19
Figure 21.	I <sub>LIMH</sub> vs. T <sub>case</sub>	19
Figure 22.	Turn-Off voltage slope	19
Figure 23.	CS_DIS high level voltage	
Figure 24.	CS_DIS clamp voltage	
Figure 25.	CS_DIS low level voltage	
Figure 26.	Application schematic	
Figure 27.	Maximum turn-Off current versus inductance (for each channel)	
Figure 28.	PowerSSO-12™ PC board	
Figure 29.	Rthj-amb vs. PCB copper area in open box free air condition (one channel ON)	
Figure 30.	PowerSSO-12™ thermal impedance junction ambient single pulse (one channel ON)	
Figure 31.	Thermal fitting model of a double channel HSD in PowerSSO- $12^{TM}$	
Figure 32.	PowerSSO-12™ package dimensions	
Figure 33.	PowerSSO-12™ tube shipment (no suffix)	
Figure 34.	PowerSSO-12 <sup>™</sup> tape and reel shipment (suffix "TR")	29

# 1 Block diagram and pin description

Figure 1. Block diagram

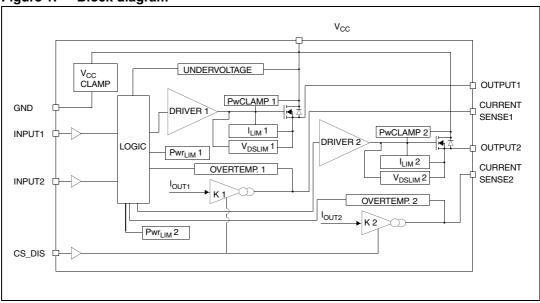


Table 2. Pin function

Name	Function				
V <sub>CC</sub>	Battery connection.				
OUTPUT <sub>n</sub>	Power output.				
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.				
INPUT <sub>n</sub>	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.				
CURRENT SENSE <sub>n</sub>	Analog current sense pin, delivers a current proportional to the load current.				
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.				

 $TAB = V_{cc}$ □ N.C. GND □ 2 11 OUTPUT2 INPUT2 == 3 ☐ OUTPUT2 INPUT1 10 **CURRENT SENSE1** 4 9 □ OUTPUT1 CURRENT SENSE2 □ 5 8 COUTPUT1 6 CS\_DIS □ 7 □ N.C. PowerSSO-12

Figure 2. Configuration diagram (top view)

Note:

The above pin configuration reflects the changes notified with PCN-APG-BOD/07/2886. The new pinout is backaward compatible with existing PCB layouts where pins #7 and 12 are connected to Vcc. For new PCB designs, these pins should be left unconnected.

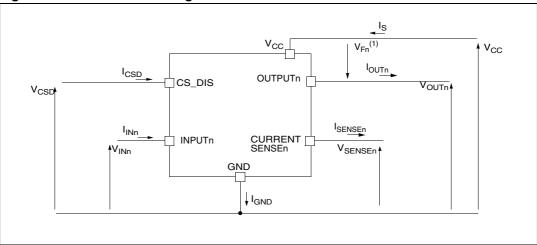
Table 3. Suggested connections for unused and N.C. pins

Connection / Pin	Current Sense	N.C.	Output	Input	CS_DIS
Floating	N.R. <sup>(1)</sup>	Х	Χ	Х	Х
To ground	Through 1kΩ resistor	Х	N.R. <sup>(1)</sup>	Through 10kΩ resistor	Through 10kΩ resistor

<sup>1.</sup> Not recommended.

### 2 Electrical specifications

Figure 3. Current and voltage conventions



Note:  $V_{Fn} = V_{OUTn} - V_{CC}$  during reverse battery condition.

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC supply voltage	41	٧
-V <sub>CC</sub>	Reverse DC supply voltage	0.3	٧
- I <sub>GND</sub>	DC reverse ground pin current	200	mA
I <sub>OUT</sub>	DC output current	Internally limited	Α
- I <sub>OUT</sub>	Reverse DC output current	6	Α
I <sub>IN</sub>	DC input current	-1 to 10	mA
I <sub>CSD</sub>	DC current sense disable input current	-1 to 10	mA
-I <sub>CSENSE</sub>	DC reverse CS pin current	200	mA
V <sub>CSENSE</sub>	Current sense maximum voltage	V <sub>CC</sub> -41 +V <sub>CC</sub>	V V
E <sub>MAX</sub>	Maximum switching energy (single pulse) (L=12mH; $R_L$ =0 $\Omega$ ; $V_{bat}$ =13.5V; $V_{jstart}$ =150 $^{o}$ C; $V_{jot}$ =1 $V_{limL}$ ( $V_{jot}$ )	34	mJ

 Table 4.
 Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
	Electrostatic discharge (Human Body Model: R=1.5KΩ; C=100pF)		
	- INPUT	4000	V
V <sub>ESD</sub>	- CURRENT SENSE	2000	V
	- CS_DIS	4000	٧
	- OUTPUT	5000	٧
	- V <sub>CC</sub>	5000	V
V <sub>ESD</sub>	Charge device model (CDM-AEC-Q100-011)	750	٧
T <sub>j</sub>	Junction operating temperature	-40 to 150	°C
T <sub>stg</sub>	Storage temperature	-55 to 150	°C

### 2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case (MAX) (With one channel ON)	8	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient (MAX)	See Figure 29	°C/W

### 2.3 Electrical characteristics

The values specified in this section are for 8V<V $_{CC}$ <36V; -40°C<T $_{j}$ <150°C, unless otherwise stated.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>CC</sub>	Operating supply voltage		4.5	13	36	V
V <sub>USD</sub>	Undervoltage shutdown			3.5	4.5	V
V <sub>USDhyst</sub>	Undervoltage shut-down hysteresis			0.5		V
R <sub>ON</sub>	On state resistance (1)	I <sub>OUT</sub> = 0.5A; T <sub>j</sub> = 25°C I <sub>OUT</sub> = 0.5A; T <sub>j</sub> = 150°C I <sub>OUT</sub> = 0.5A; V <sub>CC</sub> = 5V; T <sub>j</sub> = 25°C			160 320 210	$m\Omega$ $m\Omega$ $m\Omega$
V <sub>clamp</sub>	Clamp voltage	I <sub>S</sub> = 20 mA	41	46	52	V
I <sub>S</sub>	Supply current	Off State; $V_{CC}$ = 13V; $T_j$ = 25°C; $V_{IN}$ = $V_{OUT}$ = $V_{SENSE}$ = $V_{CSD}$ =0V On State; $V_{CC}$ =13V; $V_{IN}$ =5V; $I_{OUT}$ =0A		2 <sup>(2)</sup>	5 <sup>(2)</sup> 6	μA mA
I <sub>L(off)</sub>	Off state output current (1)	V <sub>IN</sub> =V <sub>OUT</sub> =0V; V <sub>CC</sub> =13V; T <sub>j</sub> =25°C V <sub>IN</sub> =V <sub>OUT</sub> =0V; V <sub>CC</sub> =13V; T <sub>j</sub> =125°C	0 0	0.01	3 5	μΑ
V <sub>F</sub>	Output - V <sub>CC</sub> diode voltage <sup>(1)</sup>	-l <sub>OUT</sub> = 0.6A; T <sub>j</sub> =150°C			0.7	V

<sup>1.</sup> For each channel.

Table 7. Switching ( $V_{CC}$ =13V,  $T_j$ =25°C)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn- On delay time	$R_L$ = 26 $\Omega$ (see <i>Figure 8.</i> )		10		μs
t <sub>d(off)</sub>	Turn- Off delay time	$R_L = 26\Omega$ (see <i>Figure 8.</i> )		15		μs
(dV <sub>OUT</sub> /dt) <sub>on</sub>	Turn- On voltage slope	R <sub>L</sub> = 26Ω		See Figure 20.		V/µs
(dV <sub>OUT</sub> /dt) <sub>off</sub>	Turn- Off voltage slope	$R_L = 26\Omega$		See Figure 22.		V/µs
W <sub>ON</sub>	Switching energy losses during twon	R <sub>L</sub> = 26Ω (see <i>Figure 8.</i> )		0.03		mJ
W <sub>OFF</sub>	Switching energy losses during twoff	$R_L$ = 26 $\Omega$ (see <i>Figure 8</i> .)		0.02		mJ

<sup>2.</sup> PowerMOS leakage included.

Table 8. Logic input

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>IL</sub>	Input low level voltage				0.9	V
I <sub>IL</sub>	Low level input current	V <sub>IN</sub> = 0.9V	1			μΑ
V <sub>IH</sub>	Input high level voltage		2.1			V
I <sub>IH</sub>	High level input current	V <sub>IN</sub> = 2.1V			10	μΑ
V <sub>I(hyst)</sub>	Input hysteresis voltage		0.25			V
V <sub>ICL</sub>	Input clamp voltage	I <sub>IN</sub> = 1mA I <sub>IN</sub> = -1mA	5.5	-0.7	7	V V
V <sub>CSDL</sub>	CS_DIS low level voltage				0.9	V
I <sub>CSDL</sub>	Low level CS_DIS current	V <sub>CSD</sub> = 0.9V	1			μΑ
V <sub>CSDH</sub>	CS_DIS high level voltage		2.1			V
I <sub>CSDH</sub>	High level CS_DIS current	V <sub>CSD</sub> = 2.1V			10	μΑ
V <sub>CSD(hyst)</sub>	CS_DIS hysteresis voltage		0.25			V
V <sub>CSCL</sub>	CS_DIS clamp voltage	I <sub>CSD</sub> = 1mA I <sub>CSD</sub> = -1mA	5.5	-0.7	7	V V

Table 9. Protection and diagnostics<sup>(1)</sup>

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>limH</sub>	DC short circuit current	V <sub>CC</sub> = 13V 5V <v<sub>CC&lt;36V</v<sub>	3.8	5	7.5 7.5	A A
I <sub>limL</sub>	Short circuit current during thermal cycling	$V_{CC}$ = 13V; $T_R < T_j < T_{TSD}$		2		Α
T <sub>TSD</sub>	Shutdown temperature		150	175	200	°C
T <sub>R</sub>	Reset temperature		T <sub>RS</sub> + 1	T <sub>RS</sub> + 5		°C
T <sub>RS</sub>	Thermal reset of STATUS		135			°C
T <sub>HYST</sub>	Thermal hysteresis (T <sub>TSD</sub> -T <sub>R</sub> )			7		°C
$V_{DEMAG}$	Turn-Off output voltage clamp	I <sub>OUT</sub> = 1A; V <sub>IN</sub> = 0; L= 20mH	V <sub>CC</sub> -41	V <sub>CC</sub> -46	V <sub>CC</sub> -52	V
V <sub>ON</sub>	Output voltage drop limitation	I <sub>OUT</sub> = 0.03A; T <sub>j</sub> = -40°C150°C (see <i>Figure 9</i> .)		25		mV

To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Current sense (8V<VCC<16V)

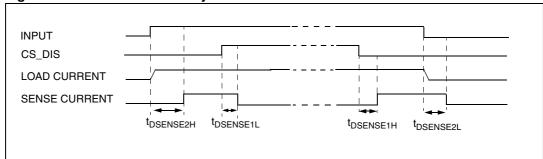
Table 10.	Current Sense (6v <vcc<16v)< th=""><th></th></vcc<16v)<>					
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
κ <sub>0</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 0.025A; V <sub>SENSE</sub> = 0.5V; V <sub>CSD</sub> =0V; T <sub>j</sub> = -40°C150°C	260	500	750	
К <sub>1</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	$I_{OUT}$ = 0.35A; $V_{SENSE}$ =0.5V; $V_{CSD}$ =0V; $T_{j}$ = -40°C150°C $I_{OUT}$ =0.35A; $V_{SENSE}$ =0.5V; $V_{CSD}$ =0V; $T_{j}$ = 25°C150°C	320 360	450 450	590 540	
dK <sub>1</sub> /K <sub>1</sub> <sup>(1)</sup>	Current sense ratio drift	I <sub>OUT</sub> = 0.35A; V <sub>SENSE</sub> = 0.5V; V <sub>CSD</sub> =0V; T <sub>J</sub> = -40 °C to 150 °C	-13		+13	%
K <sub>2</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 0.5A; V <sub>SENSE</sub> = 4V; V <sub>CSD</sub> = 0V; T <sub>j</sub> = -40°C150°C I <sub>OUT</sub> = 0.5A; V <sub>SENSE</sub> = 4V; V <sub>CSD</sub> = 0V; T <sub>i</sub> = 25°C150°C	360 380	440	540 510	
dK <sub>2</sub> /K <sub>2</sub> <sup>(1)</sup>	Current sense ratio drift	I <sub>OUT</sub> = 0.5 A; V <sub>SENSE</sub> = 4 V; V <sub>CSD</sub> = 0V; T <sub>J</sub> = -40 °C to 150 °C	-8	7.70	+8	%
К <sub>3</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 1.5A; V <sub>SENSE</sub> =4V; V <sub>CSD</sub> =0V; T <sub>j</sub> = -40°C150°C I <sub>OUT</sub> =1.5A; V <sub>SENSE</sub> =4V; V <sub>CSD</sub> =0V; T <sub>j</sub> = 25°C150°C	410 420	440 440	480 460	
$dK_3/K_3^{(1)}$	Current sense ratio drift	I <sub>OUT</sub> = 1.5 A; V <sub>SENSE</sub> = 4 V; V <sub>CSD</sub> =0V; T <sub>J</sub> = -40 °C to 150 °C	-4		+4	%
I <sub>SENSE0</sub>	Analog sense leakage current	$\begin{split} &I_{OUT}{=}0A; \ V_{SENSE}{=}0V; \\ &V_{CSD}{=}5V; \ V_{IN}{=}0V; \ T_{j}{=}{-}40^{\circ}C150^{\circ}C \\ &V_{CSD}{=}0V; \ V_{IN}{=}5V; \ T_{j}{=}{-}40^{\circ}C150^{\circ}C \\ \\ &I_{OUT}{=}0.6A; \ V_{SENSE}{=}0V; \\ &V_{CSD}{=}5V; \ V_{IN}{=}5V; \ T_{j}{=}{-}40^{\circ}C150^{\circ}C \end{split}$	0 0		1 2	μΑ μΑ μΑ
I <sub>OL</sub>	Openload ON state current detection threshold	$V_{IN} = 5V$ , $I_{SENSE} = 5 \mu A$	1		5	mA
V <sub>SENSE</sub>	Max analog senseoutput voltage	I <sub>OUT</sub> =1.5A; V <sub>CSD</sub> =0V;	5			V
V <sub>SENSEH</sub>	Analog sense output voltage in overtemperature condition	$V_{CC}$ =13V; $R_{SENSE}$ = 3.9KΩ;		9		V
I <sub>SENSEH</sub>	Analog sense output current in overtemperature condition	V <sub>CC</sub> =13V; V <sub>SENSE</sub> = 5V;		8		mA

Table 10. Current sense (8V<VCC<16V) (continued)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>DSENSE1H</sub>	Delay response time from falling edge of CS_DIS pin	V <sub>SENSE</sub> <4V, 0.08A <lout<1.5a I<sub>SENSE</sub>=90% of I<sub>SENSE max</sub> (see <i>Figure 4.</i>)</lout<1.5a 		50	100	μs
t <sub>DSENSE1L</sub>	Delay response time from rising edge of CS_DIS pin	V <sub>SENSE</sub> <4V, 0.08A <lout<1.5a I<sub>SENSE</sub>=10% of I<sub>SENSE max</sub> (see <i>Figure 4</i>.)</lout<1.5a 		5	20	μs
t <sub>DSENSE2H</sub>	Delay response time from rising edge of INPUT pin	V <sub>SENSE</sub> <4V, 0.08A <lout<1.5a I<sub>SENSE</sub>=90% of I<sub>SENSE max</sub> (see <i>Figure 4</i>.)</lout<1.5a 		80	150	μs
Δt <sub>DSENSE2H</sub>	Delay response time between rising edge of output current and rising edge of current sense	V <sub>SENSE</sub> < 4V, I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> , I <sub>OUT</sub> = 90% of I <sub>OUTMAX</sub> I <sub>OUTMAX</sub> =2A (see <i>Figure 5</i> )			20	μs
t <sub>DSENSE2L</sub>	Delay response time from falling edge of INPUT pin	V <sub>SENSE</sub> <4V, 0.08A <lout<1.5a I<sub>SENSE</sub>=10% of I<sub>SENSE max</sub> (see <i>Figure 4.</i>)</lout<1.5a 		100	250	μs

<sup>1.</sup> Parameter guaranteed by design; it is not tested.





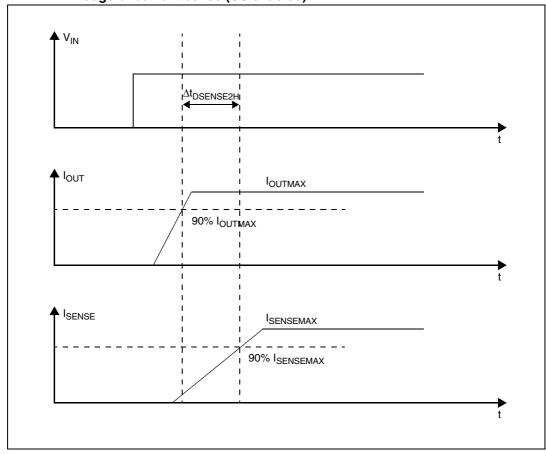


Figure 5. Delay response time between rising edge of ouput current and rising edge of current sense (CS enabled)

47/

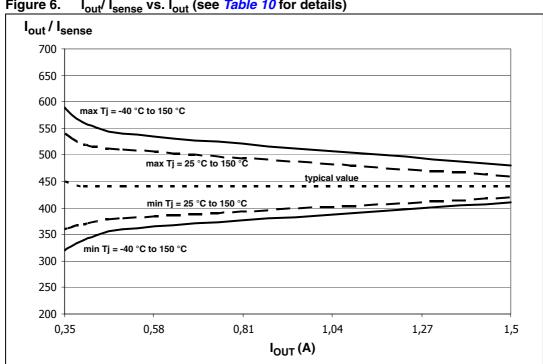
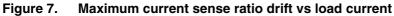
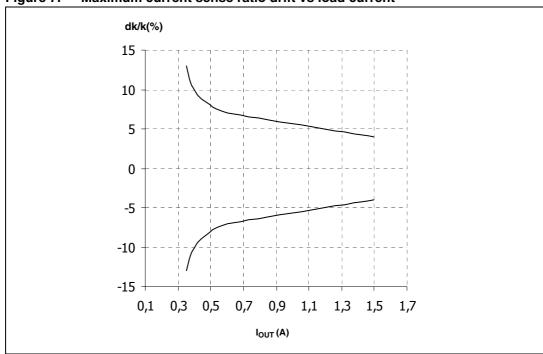


Figure 6. I<sub>out</sub>/ I<sub>sense</sub> vs. I<sub>out</sub> (see *Table 10* for details)





Note: Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	INPUT	ОИТРИТ	SENSE (V <sub>CSD</sub> =0V) <sup>(1)</sup>
Normal aparation	L	L	0
Normal operation	Н	Н	Nominal
Overtemperature	L	L	0
Overtemperature	Н	L	$V_{SENSEH}$
Lindawyoltogo	L	L	0
Undervoltage	Н	L	0
	L	L	0
Short circuit to GND	Н	L	0 if $T_j < T_{TSD}$
(R <sub>SC</sub> ≤10 mΩ)	Н	L	$V_{SENSEH}$ if $T_j > T_{TSD}$
Chart aircuit to V	L	Н	0
Short circuit to V <sub>CC</sub>	Н	Н	< Nominal
Negative output voltage clamp	L	L	0

If the V<sub>CSD</sub> is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Figure 8. Switching characteristics

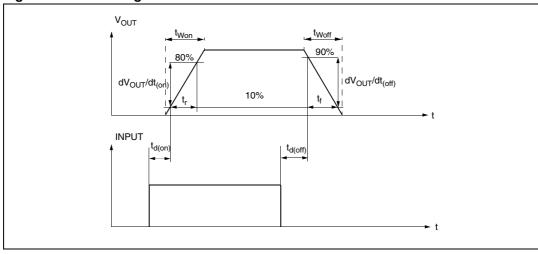


Figure 9. Output voltage drop limitation

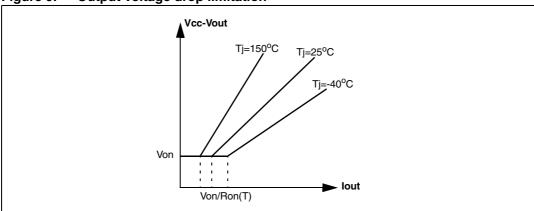


Table 12. Electrical transient requirements

ISO 7637-2: 2004(E)	Test le	vels <sup>(1)</sup>	Number of pulses or	Burst cy	cle/pulse	Delays and
Test pulse	III	IV	test times repetition time		repetition time i	
1	-75V	-100V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37V	+50V	5000 pulses	0.2 s	5 s	50 μs, 2 Ω
3a	-100V	-150V	1h	90 ms	100 ms	0.1 μs, 50 Ω
3b	+75V	+100V	1h	90 ms	100 ms	0.1 μs, 50 Ω
4	-6V	-7V	1 pulse		1	100 ms, 0.01 Ω
5b <sup>(2)</sup>	+65V	+87V	1 pulse			400 ms, 2 Ω

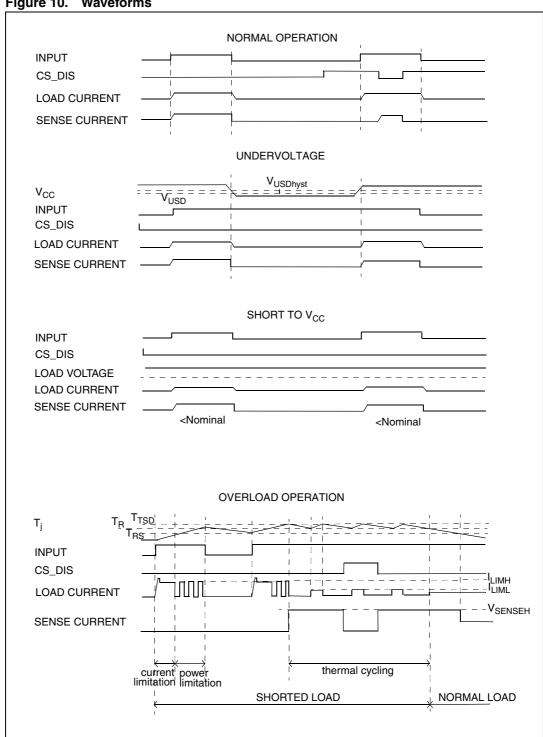
ISO 7637-2: 2004(E)	Test level	results <sup>(1)</sup>
Test pulse	III	IV
1	С	С
2a	С	С
3a	С	С
3b	С	С
4	С	С
5b <sup>(2)</sup>	С	С

<sup>1.</sup> The above test levels must be considered referred to Vcc = 13.5V except for pulse 5b.

<sup>2.</sup> Valid in case of external load dump clamp: 40V maximum referred to ground.

Class	Contents
С	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

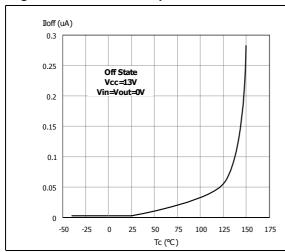
Figure 10. Waveforms



#### 2.4 Electrical characteristics curves

Figure 11. Off state output current

Figure 12. High level input current



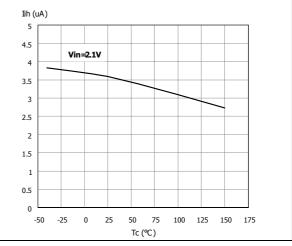
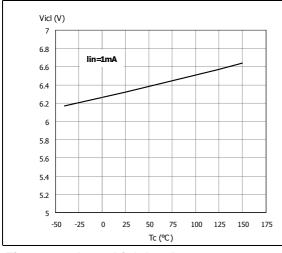


Figure 13. Input clamp voltage

Figure 14. Input low level



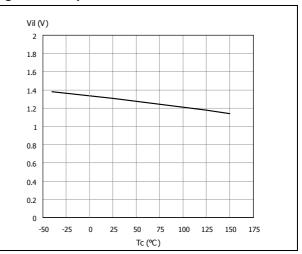
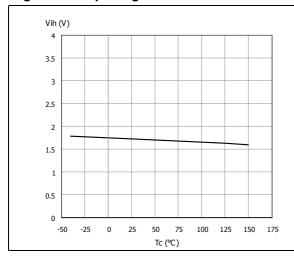
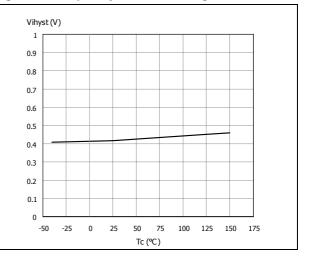


Figure 15. Input high level

Figure 16. Input hysteresis voltage



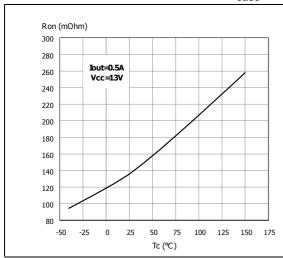


577

18/31

Figure 17. On state resistance vs.  $T_{case}$ 

Figure 18. On state resistance vs. V<sub>CC</sub>



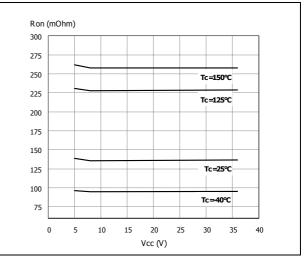
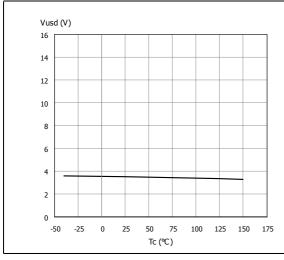


Figure 19. Undervoltage shutdown

Figure 20. Turn-On voltage slope



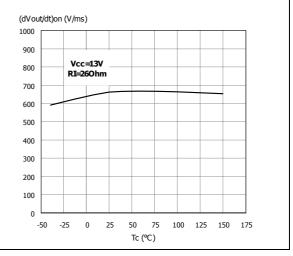
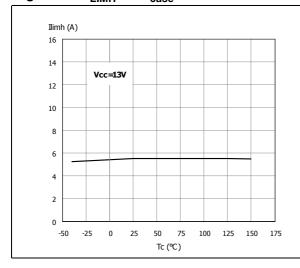


Figure 21. I<sub>LIMH</sub> vs. T<sub>case</sub>

Figure 22. Turn-Off voltage slope



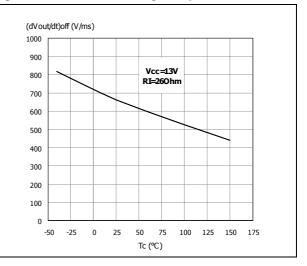
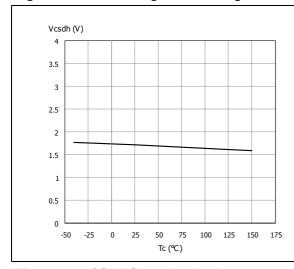


Figure 23. CS\_DIS high level voltage

Figure 24. CS\_DIS clamp voltage



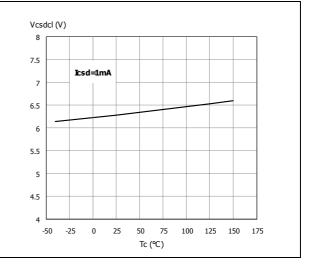
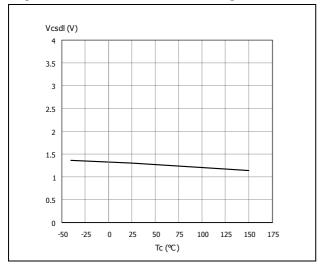


Figure 25. CS\_DIS low level voltage



### 3 Application information

μC R<sub>prot</sub> CS\_DIS

CQURRENT SENSE GND

CEXT RSENSE V<sub>GND</sub> R<sub>GND</sub> D<sub>GND</sub>

Figure 26. Application schematic

Note: Channel 2 has the same internal circuit as channel 1.

#### 3.1 GND protection network against reverse battery

#### 3.1.1 Solution 1 : resistor in the ground line (R<sub>GND</sub> only)

This can be used with any type of load.

The following is an indication on how to dimension the R<sub>GND</sub> resistor.

- 1.  $R_{GND} \leq 600 \text{mV} / (I_{S(on)max})$ .
- 2.  $R_{GND} \ge (-V_{CC}) / (-I_{GND})$

where -I<sub>GND</sub> is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R<sub>GND</sub> (when V<sub>CC</sub><0: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the  $R_{GND}$  will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

#### 3.1.2 Solution 2 : diode (D<sub>GND</sub>) in the ground line

A resistor ( $R_{GND}$ =1k $\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ( $\approx 600 \text{mV}$ ) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

#### 3.2 Load dump protection

 $D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  max DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

#### 3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the MCU I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of MCU and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of MCU I/Os.

 $-V_{CCpeak}/I_{latchup} \le R_{prot} \le (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$ 

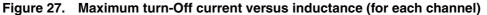
Calculation example:

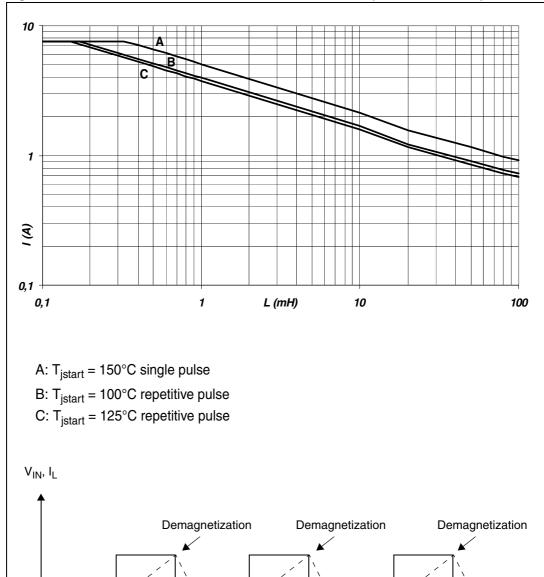
For  $V_{CCpeak}$ = - 100V and  $I_{latchup} \ge 20mA$ ;  $V_{OH\mu C} \ge 4.5V$ 

 $5k\Omega \le R_{prot} \le 180k\Omega$ 

Recommended values:  $R_{prot} = 10k\Omega$ ,  $C_{EXT} = 10nF$ .

## 3.4 Maximum demagnetization energy ( $V_{CC} = 13.5V$ )





Note:

Values are generated with  $R_L = 0 \Omega$ 

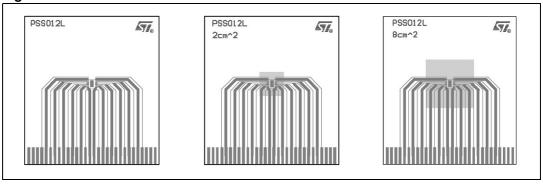
In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

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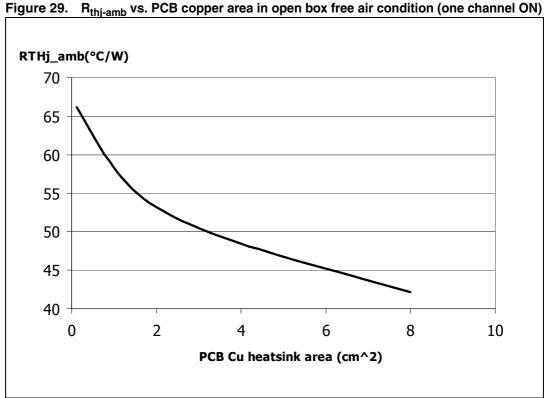
#### Package and PC board thermal data 4

#### 4.1 PowerSSO-12™ thermal data

Figure 28. PowerSSO-12™ PC board



Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double layer, Thermal Vias, FR4 Note: area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70µm (front and back side), Copper areas: from minimum pad lay-out to 8cm<sup>2</sup>).



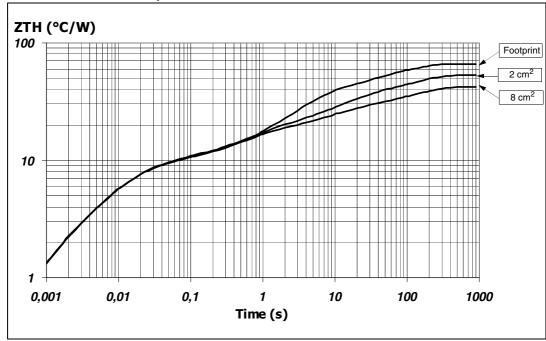
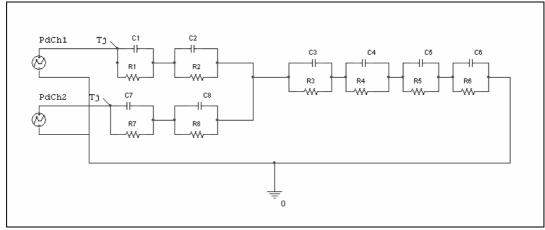


Figure 30. PowerSSO-12™ thermal impedance junction ambient single pulse (one channel ON)

**Equation 1: pulse calculation formula** 

$$\begin{split} Z_{TH\delta} &= R_{TH} \cdot \ \delta + Z_{THtp} (1 - \delta) \\ \text{where } \delta &= t_P / T \end{split}$$

Figure 31. Thermal fitting model of a double channel HSD in PowerSSO-12™ (a)



a. The fitting model is a semplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 13. Thermal parameters

Area/island (cm <sup>2</sup> )	Footprint	2	8
R1= R7 (°C/W)	1.2		
R2= R8 (°C/W)	6		
R3 (°C/W)	3		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1= C7 (W.s/°C)	0.0008		
C2= C8 (W.s/°C)	0.0016		
C3 (W.s/°C)	0.0166		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

### 5 Package and packing information

## 5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

#### 5.2 Package mechanical data

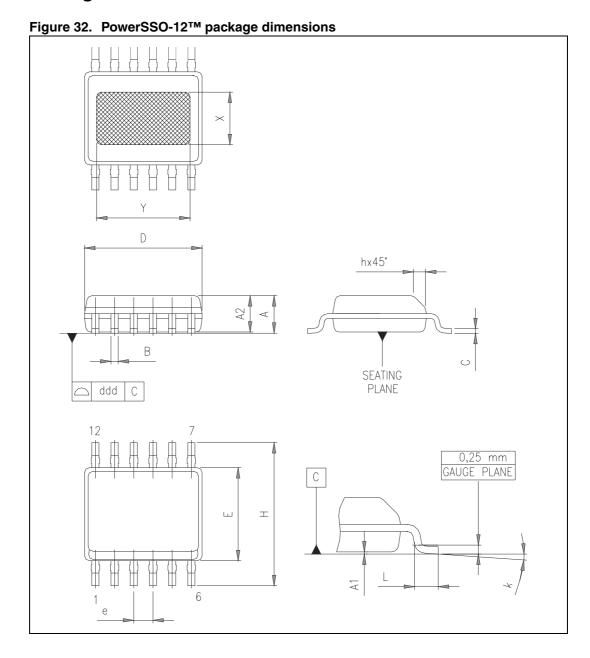


Table 14. PowerSSO-12™ mechanical data

Symbol		Millimeters	
Symbol	Min.	Тур.	Max.
Α	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
В	0.230		0.410
С	0.190		0.250
D	4.800		5.000
E	3.800		4.000
е		0.800	
Н	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
Х	2.200		2.800
Y	2.900		3.500
ddd			0.100

### 5.3 Packing information

Figure 33. PowerSSO-12™ tube shipment (no suffix)

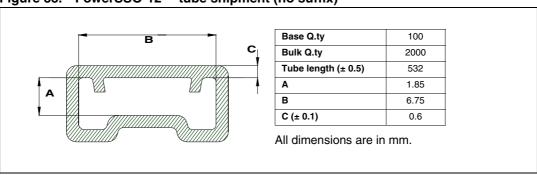
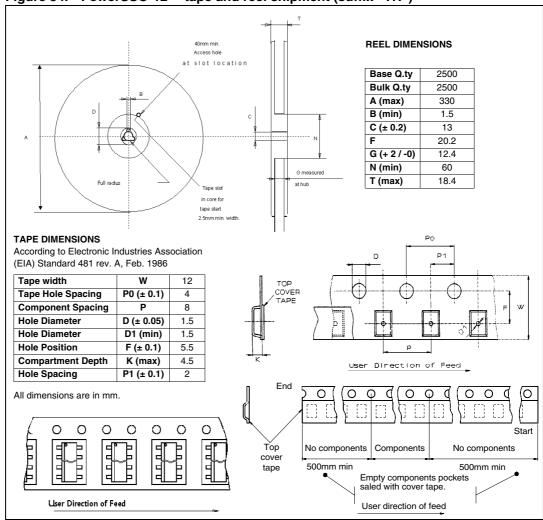


Figure 34. PowerSSO-12™ tape and reel shipment (suffix "TR")



Revision history VND5160AJ-E

# 6 Revision history

Table 15. Document revision history

Date	Revision	Changes
13-Sep-2004	1	Initial release.
10-Apr-2006	2	Layout changed. Major update to Section 2: Electrical specifications.
01-Mar-2007	3	Reformatted. Contents, List of tables and List of figures added. Added Section 3.4: Maximum demagnetization energy (VCC = 13.5V). ECOPACK® package information added.
10-Dec-2007	4	Document reformatted and restructured.  Updated Figure 2: Configuration diagram (top view): pins 7-12 left unconnected (N.C) and added note.  Table 4: Absolute maximum ratings: corrected E <sub>MAX</sub> value from 14 to 34 mJ.  Added Figure 5: Delay response time between rising edge of ouput current and rising edge of current sense (CS enabled).  Updated Figure 6: lout/ Isense vs. lout (see Table 10 for details).  Added Figure 7: Maximum current sense ratio drift vs load current.  Updated Table 10: Current sense (8V <vcc<16v): changed="" t<sub="" —="">DSENSE2H max value from 300 µs to 150 µs.  — added dk1/k1, dk2/k2, dk3/k3, Δt<sub>DSENSE2H</sub>, l<sub>OL</sub> parameters.  Table 12: Electrical transient requirements: updated test level values III and IV for test pulse 5b and notes.  Updated Section 4.1: PowerSSO-12™ thermal data:  — changed Figure 29: Rthj-amb vs. PCB copper area in open box free air condition (one channel ON).  — changed Figure 30: PowerSSO-12™ thermal impedance junction ambient single pulse (one channel ON).  — Figure 31: Thermal fitting model of a double channel HSD in PowerSSO-12™: added note.  — updated Table 13: Thermal parameters:  R3 value changed from 7 to 3 °C/W.  R4 values changed from 10 /10 /9 to 8 /8 /7 °C/W.  C3 value changed from 0.05 to 0.0166 W.s/°C.</vcc<16v):>
12-Feb-2008	5	Corrected typing error in <i>Table 10: Current sense (8V<vcc<16v)< i=""> : changed <math>I_{OL}</math> test condition from <math>V_{IN} = 0V</math> to <math>V_{IN} = 5V</math>.</vcc<16v)<></i>

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