Hardware - Tutorial 3 - Correction
Sequencial Logic

Exercice 1: Adding numbers

Adding numbers in binary is quite similar to adding numbers in decimal. We add digits of the same column and a possible carry from the previous column. We obtain a result and a possible carry for the next column.

We want to design a circuit that is able to add 4 bits binary numbers together. Let us first design a circuit called a “Full adder” that adds 2 bits and a possible carry.

The circuit will have:

- 3 inputs (A, B and Ri) that respectively represents the 2 input bits and the input carry
- 2 outputs (S and R) that respectively represents the result and the output carry.

1) Write down the thruth table of S and R.

Solution:

Ri	A	B	S	R
0	**0**	**0**	0	0
0	**0**	**1**	1	0
0	**1**	**0**	1	0
0	**1**	**1**	0	1
1	**0**	**0**	1	0
1	**0**	**1**	0	1
1	**1**	**0**	0	1
1	**1**	**1**	1	1

2) Fill up two Karnaugh map with theses truth tables and extract the most simplified expression of S and R.

Solution:

S		**AB**			
		00	01	11	10
Ri	0	0	1	0	1
	1	1	0	1	0

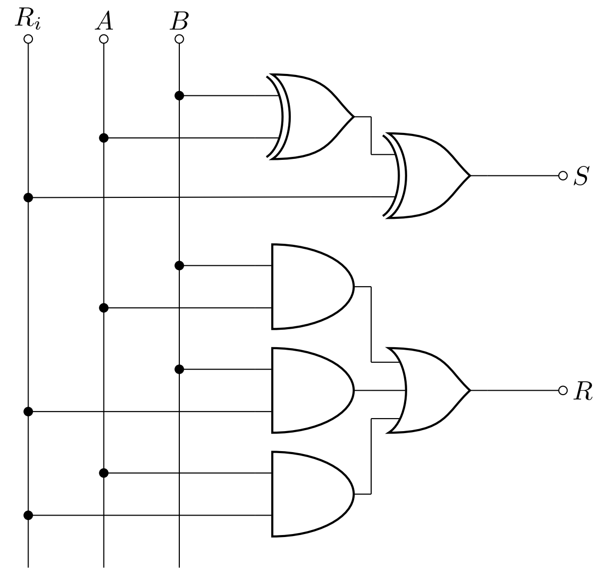
R		**AB**			
		00	01	11	10
Ri	0	0	0	1	0
	1	0	1	1	1

$S = R_i \cdot \bar{A} \cdot \bar{B} + R_i \cdot A \cdot B + \bar{R}_i \cdot \bar{A} \cdot B + \bar{R}_i \cdot A \cdot \bar{B}$
$S = R_i \cdot (\bar{A} \cdot \bar{B} + A \cdot B) + \bar{R}_i \cdot (\bar{A} \cdot B + A \cdot \bar{B})$
$S = R_i \cdot \overline{(A \oplus B)} + \bar{R}_i \cdot (A \oplus B)$
$S = R_i \oplus A \oplus B$

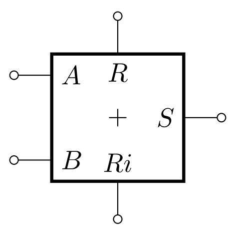
$R = R_i \cdot B + R_i \cdot A + A \cdot B$

3) Draw the circuit diagram of the full adder.

Solution:



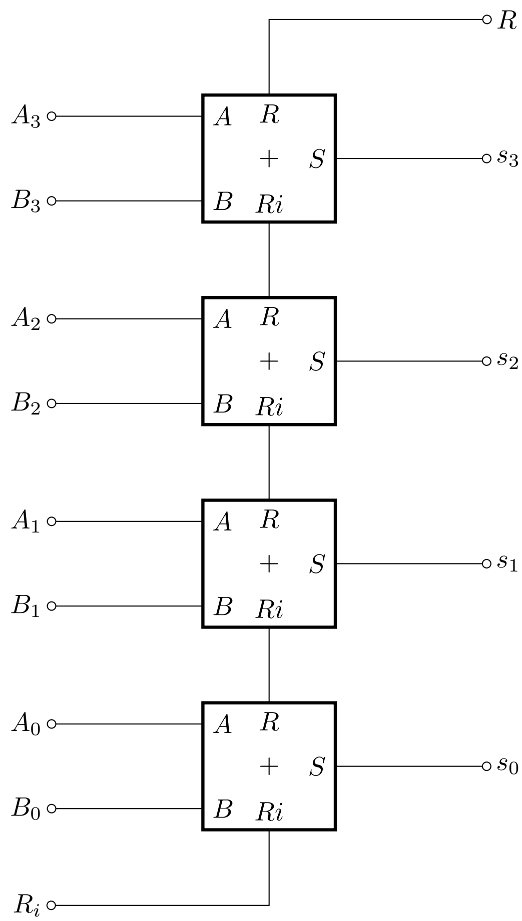
Now we can use the previous circuit as a sub-circuit. Use the following custom component to represent it:



Using 4 full adders, we want to design a 4-bits adder.

4) Draw the circuit diagram of the 4-bits adder. It must have a 1 bit input carry and a 1 bit output carry.

Solution:



Exercice 2: Subtracting numbers

The same way a full adder adds bits, a full subtractor is a circuit that subtracts two bits (A and B) and a possible borrow (Ri). It generates the difference D and a possible output borrow R.

We want to design a full subtractor.

1) Write down the truth tables of D and R.

Solution:

Ri	A	B	S	R
0	**0**	**0**	0	0
0	**0**	**1**	1	1
0	**1**	**0**	1	0
0	**1**	**1**	0	0
1	**0**	**0**	1	1
1	**0**	**1**	0	1
1	**1**	**0**	0	0
1	**1**	**1**	1	1

2) Fill up Karnaugh maps to find the most simplified expressions of these outputs.

Solution:

First, there is no need to fill the Karnaugh map for D: it is the exact same as the S expression we found for the full adder.

Here is the Karnaugh Map for R:

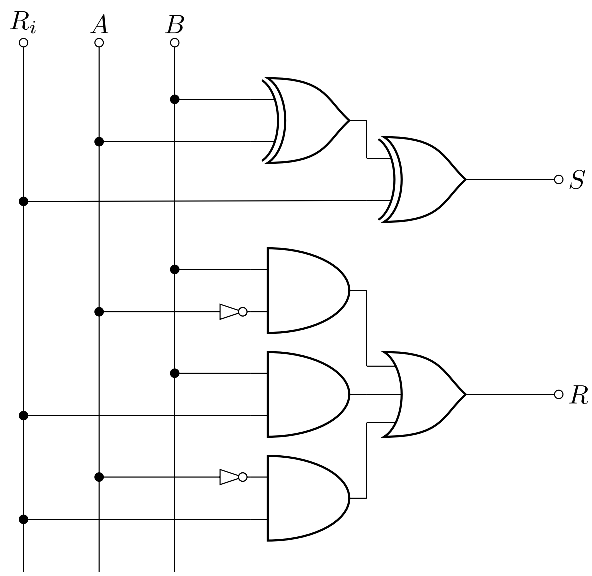
R		**AB**			
		00	01	11	10
Ri	0	0	1	0	0
	1	1	1	1	0

$$D = A \oplus B \oplus R_i$$

$$R = R_i \cdot \bar{A} + R_i \cdot B + \bar{A} \cdot B$$

3) Draw the circuit diagram of the full subtractor.

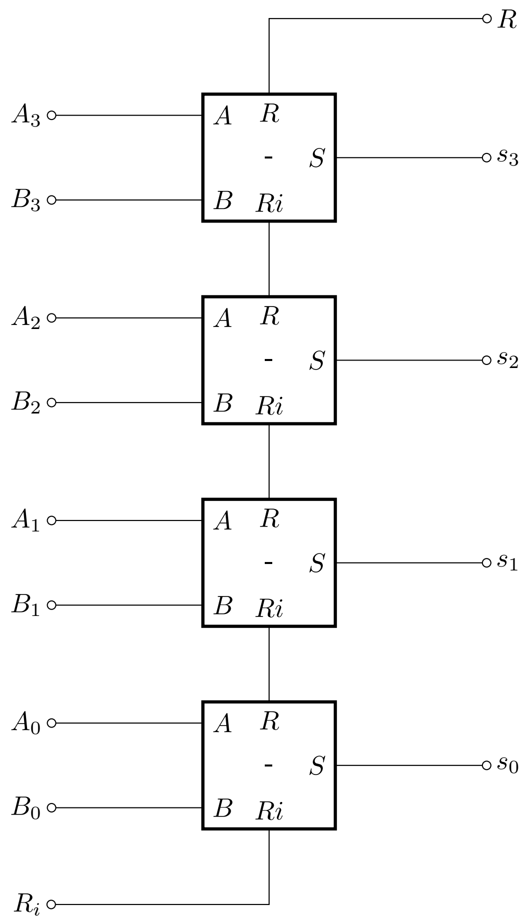
Solution:



Using 4 full subtractors, we want to design a 4-bits subtractor.
4) Draw the circuit diagram of the 4-bits subtractor.

Solution:

The schematic of the 4 bits substractor is the exact same as the 4 bits adder.



Exercice 3: Adder-Subtractor

1) Design a circuit with one output (S) and two inputs (E and C).

- If $C = 0$ then $S = E$
- If $C = 1$ then $S = \bar{E}$

Solution:

Let's fill a truth table for this problem:

C	E	S
0	0	0
0	1	1
1	0	1
1	1	0

This truth table is the truth table of the XOR gate.

2) Using the circuit from the previous question and a 4-bits adder, design a 4-bits adder-subtractor that can either add two 4-bits numbers or subtracts them depending on a C input.

- If $C = 0$ then $S = A + B$

- If $C = 1$ then $S = A - B$

Solution:

The key here is to think about what is a substraction compared to an addition ?

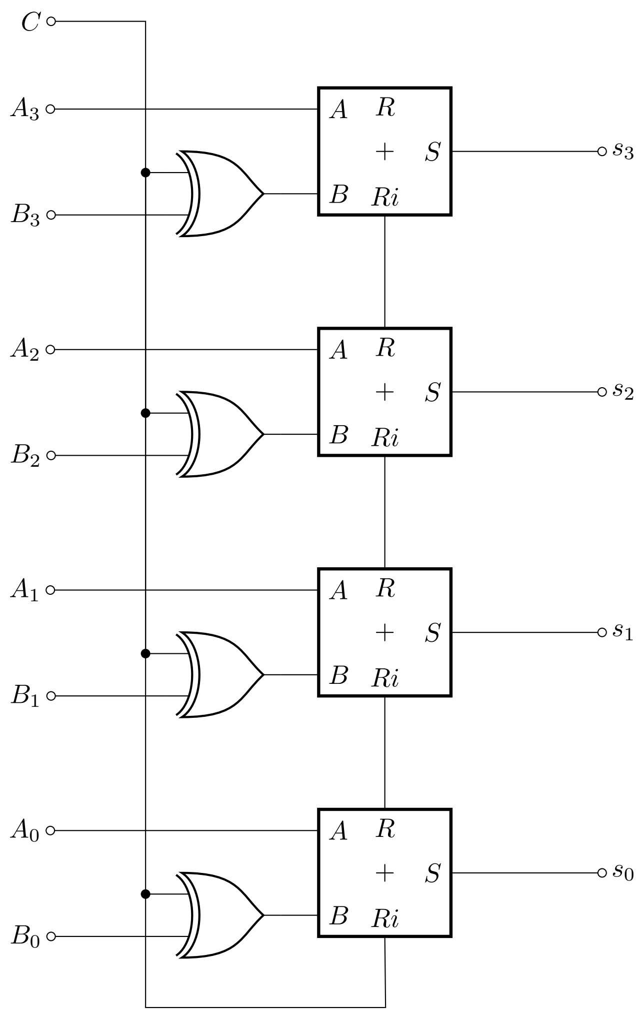
$A - B$ is the same as $A + (-B)$ and you know that $-B$ is the two's complement of B.

To build an adder/substractor you need to build an adder that can change it's B input into its two's complement when the C input is true.

The two's complement of B is just the inversion of all its bits to wich we add 1.

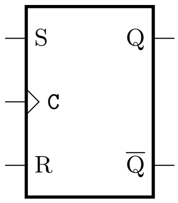
Luckily, the last exercice showed you a component that can invert an input depending on another. That can give you the one's complement of B. Then you just need to add 1 to this to obtain the two's complement and as you are using adders, you have access to the carry input that can add 1 to the result of an addition.

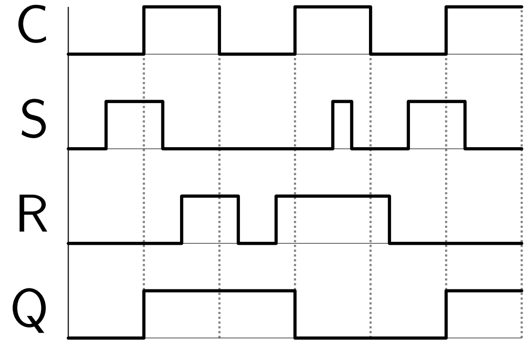
Here is the final schematic of a 4 bits adder/substractor:

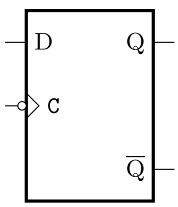


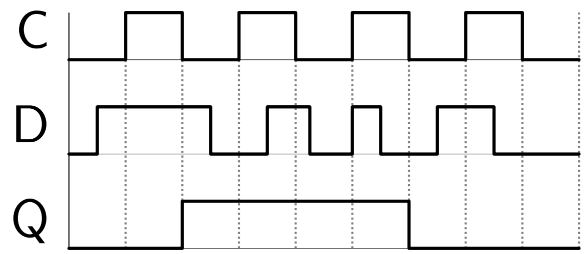
Exercice 4: Flip Flops

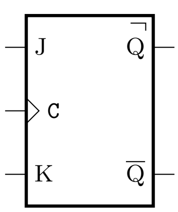
Complete the following timing diagrams for each flip flop. Beware of the synchronisation mode of each flipflop.

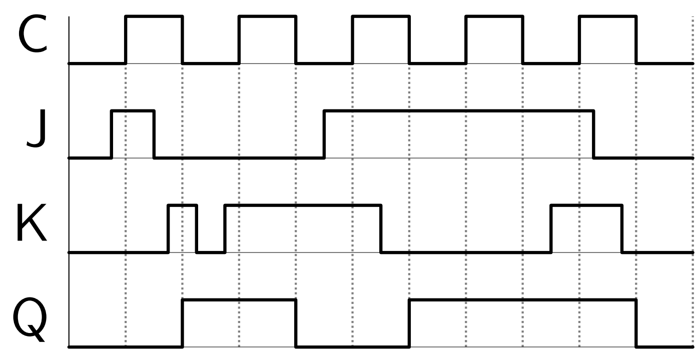

S
Q
C
R
$\overline{Q}$

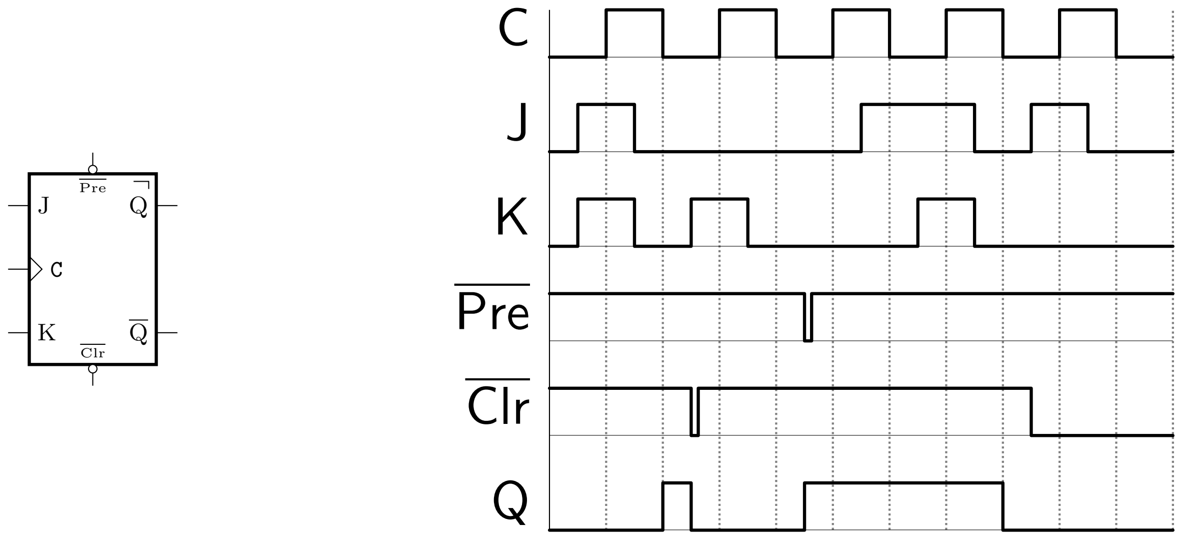

C
S
R
Q


D
Q
C
$\overline{Q}$


C
D
Q


J
Q
C
K
$\overline{Q}$

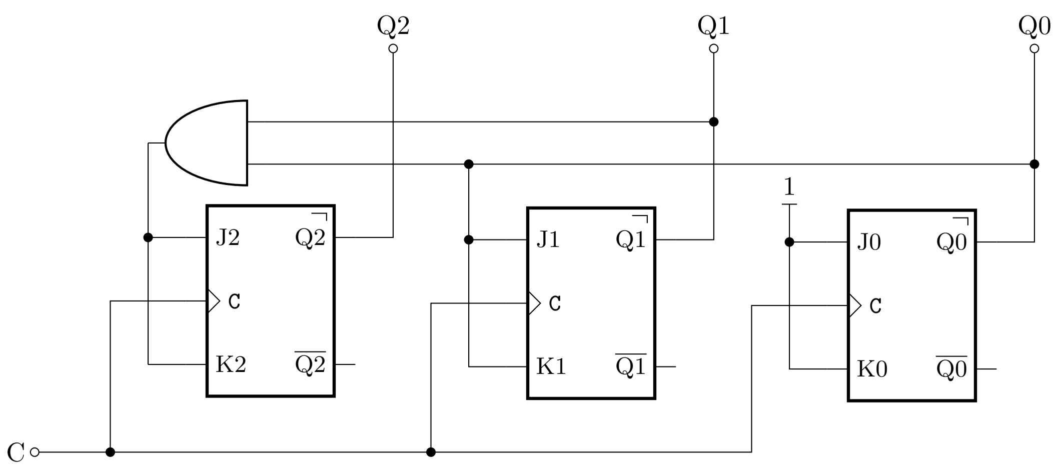

C
J
K
Q

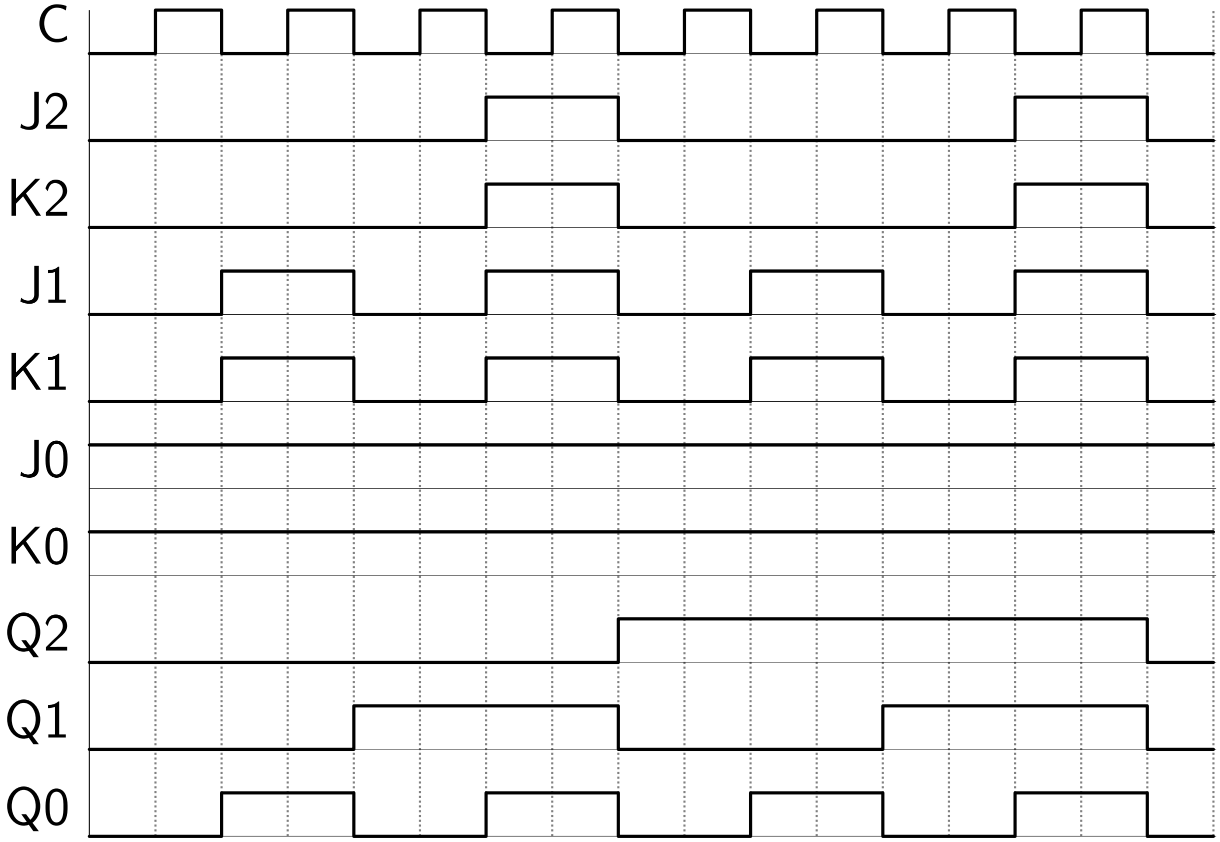


Exercice 5: Circuit Analysis

Given the following sequencial circuit:

- Fill the related timing table
- Find the purpose of such a circuit





This circuit is a synchronous 3 bits counter. If you take all three outputs as a binary number, you will see a cycle from 0 to 7 and back to 0.