Using Vivado, write VHDL code for the implementation of a sequence detector in VHDLusing push buttons. Four push buttons should be used for entering four input buttons(btnu,btnd, btnl, btnr). Further, the push button btnc in the middleshould be used for initialisation. •Up to 10 inputs could be entered after pressing the initialisation push button. When the sequence (btnu,btnd, btnd, btnl, btnr) is entered, then the LEDs should start flashing. Please note that the right sequence of symbols need not necessarily be entered immediately after the initialisation push button is pressed. For example, the sequence "btnu,btnd, btnl, btnr,btnr,btnu,btnd, btnl, btnr" should be able to activate the flashing of the LEDs.•If inputs have been entered but the right sequence of symbols has not appeared yet, then the system should lock and the LEDs should show the following predefined pattern:on, off, on, off, on, off, on, off, on, off, on, off.•If the system is locked, the user will need to press the initialisation button in order to be allowed to start entering new symbols

I want to implement to led flash on condition 111111111 to 00000000when..... - the sequence btnu, btnd, btnd, btnl, btnr, any other 5 buttions - the sequence any other 5 buttions ,btnu, btnd, btnd, btnl, btnr, - the sequence any 1 button input, btnu, btnd, btnl, btnr, any other 4 button inputs. -the sequence any 2 button input, btnu, btnd, btnl, btnr, any 3 button inputs, - the sequence any 3 button input ,btnu, btnd, btnl, btnr, any 2 button input, -the sequence any 4 buttons input, btnu, btnd, btnd, btnl, btnr, any 1 button input, library IEEE; use IEEE.STD LOGIC 1164.ALL; use IEEE.STD LOGIC ARITH.ALL; use IEEE.STD LOGIC UNSIGNED.ALL; entity Counter is Port ( clk: in STD LOGIC; -- High-frequency clock signal (e.g., 100 MHz) -- Button-up signal btnu: in STD LOGIC; -- Button-down signal btnd: in STD LOGIC; btnl: in STD LOGIC; -- Button-left signal -- Button-right signal btnr: in STD LOGIC; btnc: in STD LOGIC; -- Button-center signal led : out STD LOGIC VECTOR(7 downto 0) -- 8-bit LED display ); end Counter; architecture Behavioral of Counter is : STD LOGIC := '0'; -- Slow clock signal for toggling signal clk div signal clk div count : integer := 0; -- Counter for clock division constant DIVISOR : integer := 100000; -- Divide factor for clock (adjust for desired speed) signal pattern : STD LOGIC VECTOR(7 downto 0) := "000000000"; -- LED pattern to display begin

-- Clock Divider Process

process(clk)

begin

```
if rising edge(clk) then
       -- Divide the clock signal by the divisor
       if clk div count = DIVISOR - 1 then
         clk div <= not clk div; -- Toggle the clock signal
         clk div count <= 0; -- Reset the counter
       else
         clk div count <= clk div count + 1; -- Increment the clock divider counter
       end if;
    end if;
  end process;
  -- LED Control Process
  process(btnu, btnd, btnl, btnr, btnc, clk div)
  begin
    if btnu = '1' then
       -- Button Up: Pattern 1 (Alternating LEDs)
       pattern <= "10101010";
    elsif btnd = '1' then
       -- Button Down: Pattern 2 (Inverse Alternating LEDs)
       pattern <= "01010101";
    elsif btnl = '1' then
       -- Button Left: Pattern 3 (Outer LEDs)
       pattern <= "10000001";
    elsif btnr = '1' then
       -- Button Right: Pattern 4 (Inner LEDs)
       pattern <= "01111110";
    elsif btnc = '1' then
       -- Button Center: Pattern 5 (All LEDs ON)
       pattern <= "11111111";
    else
       -- No button pressed: Turn off LEDs
       pattern <= "00000000";
    end if;
  end process;
  -- Assign the current pattern to the LEDs
  led <= pattern;
end Behavioral;
```

write me a code that display four less on four various buttons and central button to use as the reset ....include display 111111111 and 0000000 repetitively only when when the combination of button up, down left right is met

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD LOGIC UNSIGNED.ALL;
entity Counterc is
  Port (
    clk: in STD LOGIC;
                                   -- High-frequency clock signal
                                   -- Button Up
    btnu: in STD LOGIC;
    btnd: in STD LOGIC;
                                   -- Button Down
    btnl: in STD LOGIC;
                                   -- Button Left
    btnr: in STD LOGIC;
                                   -- Button Right
                                   -- Central Button (Reset)
    btnc: in STD LOGIC;
    led : out STD LOGIC VECTOR(7 downto 0) -- 8-bit LED output
  );
end Counterc;
architecture Behavioral of Counterc is
  -- State Machine Definitions
  type State Type is (IDLE, SHOW LESS, CHECK COMBINATION, SUCCESS); --
FSM states
  signal state
                : State Type := IDLE;
                                                   -- Current FSM state
  -- Signals for LED Patterns
  signal display_pattern : STD_LOGIC_VECTOR(7 downto 0) := (others => '0'); -- LED
display pattern
  signal flash clk
                    : STD LOGIC := '0';
                                                          -- Clock for flashing LEDs
  signal flash count : INTEGER := 0;
                                                          -- Counter for flashing clock
  constant FLASH DIVISOR: INTEGER:= 50000000;
                                                                    -- Flashing speed
  -- Combination Check
  signal sequence : STD LOGIC VECTOR(3 downto 0) := "0000";
                                                                        -- Tracks
button combination
begin
  -- Clock Divider for Flashing LEDs
  process(clk)
  begin
    if rising edge(clk) then
      if flash count = FLASH DIVISOR - 1 then
         flash clk <= not flash clk;
                                                     -- Toggle flashing clock
         flash count \leq 0;
                                                  -- Reset flash counter
      else
         flash count <= flash count + 1;
                                                       -- Increment flash counter
```

```
end if;
  end if;
end process;
-- Main FSM Process
process(clk)
begin
  if rising edge(clk) then
    if btnc = '1' then
       -- Reset the system
       state <= IDLE;
       sequence <= "0000";
       display pattern \leq (others \Rightarrow '0');
       case state is
         when IDLE =>
            -- Display four "less" on respective button presses
            if btnu = '1' then
              display pattern <= "10000000"; -- Display less on top LED
              sequence(0) \le '1';
            elsif btnd = '1' then
              display pattern <= "01000000"; -- Display less on bottom LED
              sequence(1) \le '1';
            elsif btnl = '1' then
              display pattern <= "00100000"; -- Display less on left LED
              sequence(2) <= '1';
            elsif btnr = '1' then
              display pattern <= "00010000"; -- Display less on right LED
              sequence(3) \le '1';
            end if;
            -- Move to CHECK COMBINATION when any button is pressed
            if sequence /= "0000" then
              state <= CHECK COMBINATION;
            end if;
         when CHECK COMBINATION =>
            -- Check if the combination "btnu, btnd, btnl, btnr" is met
            if sequence = "1111" then
              state <= SUCCESS; -- Go to SUCCESS state if combination is met
            else
              state <= IDLE; -- Reset to IDLE for invalid combination
            end if;
         when SUCCESS =>
            -- Flash LEDs (11111111 and 00000000 alternately)
            if flash clk = '1' then
              display pattern <= "11111111"; -- All LEDs ON
            else
              display pattern <= "00000000"; -- All LEDs OFF
```

```
end if;
           when others =>
             state <= IDLE; -- Default to IDLE for unexpected states
         end case;
      end if;
    end if:
  end process;
  -- Assign the display pattern to the LEDs
  led <= display_pattern;</pre>
end Behavioral;
counter to count udlr button input attempt and central button to reset
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.STD LOGIC UNSIGNED.ALL;
entity SequenceDetector is
  Port (
    clk: in STD LOGIC;
                                   -- High-frequency clock signal
    btnu: in STD LOGIC;
                                   -- Button Up
    btnl: in STD LOGIC;
                                    -- Button Left
    btnd: in STD LOGIC;
                                   -- Button Down
    btnr: in STD LOGIC;
                                    -- Button Right
                                    -- Central Button (Initialisation)
    btnc: in STD LOGIC;
    led : out STD LOGIC VECTOR(7 downto 0) -- 8-bit LED output
end SequenceDetector;
architecture Behavioral of SequenceDetector is
  -- FSM States
  type State Type is (IDLE, COLLECT, SUCCESS, LOCK);
  signal state : State Type := IDLE;
  -- Signals for sequence detection
  signal sequence buffer: STD LOGIC VECTOR(39 downto 0) := (others => '0'); -- 10
symbols buffer (4 bits per symbol)
  signal current index : INTEGER range 0 to 9 := 0;
                                                                -- Index of entered
symbols
  -- Flashing LEDs
  signal flash clk
                    : STD LOGIC := '0';
                                                           -- Clock for flashing LEDs
  signal flash count : INTEGER := 0;
                                                           -- Counter for flashing clock
  constant FLASH DIVISOR : INTEGER := 50000000;
                                                                      -- Flash speed
constant
```

```
-- Predefined Pattern
  signal display pattern: STD LOGIC VECTOR(7 downto 0) := (others => '0');
begin
  -- Clock Divider for Flashing LEDs
  process(clk)
  begin
    if rising edge(clk) then
       if flash count = FLASH DIVISOR - 1 then
         flash clk <= not flash clk;
                                                         -- Toggle flashing clock
                                                      -- Reset flash counter
         flash count \leq 0;
       else
         flash count <= flash count + 1;
                                                            -- Increment flash counter
       end if;
    end if;
  end process;
  -- Main FSM Logic
  process(clk)
    variable input symbol: STD LOGIC VECTOR(3 downto 0);
    if rising edge(clk) then
       if btnc = '1' then
         -- Reset the system
         state <= IDLE;
         sequence buffer <= (others => '0');
         current index \leq 0;
         display_pattern <= (others => '0');
       else
         case state is
            when IDLE =>
              if btnu = '1' then
                 input symbol := "0001"; -- Up button = '1'
              elsif btnl = '1' then
                 input_symbol := "0010"; -- Left button = '2'
              elsif btnd = '1' then
                 input symbol := "0011"; -- Down button = '3'
              elsif btnr = '1' then
                 input symbol := "0100"; -- Right button = '4'
              else
                 input symbol := (others => '0');
              end if;
              if input symbol /= (others => '0') then
                 state <= COLLECT;</pre>
              end if;
            when COLLECT =>
              -- Collect up to 10 symbols
```

```
sequence buffer <= sequence buffer(35 downto 0) & input symbol;
              if current index < 9 then
                 current index <= current index + 1;
              else
                 -- Check if sequence matches "41123" (Right -> Up -> Down -> Left ->
Up)
                 if sequence buffer = "01000001000100110010" then
                   state <= SUCCESS;</pre>
                 else
                   state <= LOCK;
                 end if;
              end if;
            when SUCCESS =>
              -- Flash LEDs (11111111 and 00000000 alternately)
              if flash clk = '1' then
                 display_pattern <= "11111111"; -- All LEDs ON
              else
                 display pattern <= "00000000"; -- All LEDs OFF
              end if;
            when LOCK =>
              -- Locked state: Show predefined pattern
              if flash clk = '1' then
                 display pattern <= "10101010";
                 display pattern <= "01010101";
              end if;
              -- Return to IDLE if central button is pressed
              if btnc = '1' then
                 state <= IDLE;
              end if;
            when others =>
              state <= IDLE; -- Default state
         end case;
       end if;
     end if;
  end process;
  -- Assign LED display pattern
  led <= display pattern;</pre>
end Behavioral;
sequence detector that detect up down left right !!!
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
```

```
use IEEE.STD LOGIC UNSIGNED.ALL;
entity Counterc is
  Port (
    clk: in STD LOGIC;
                                   -- High-frequency clock signal
                                    -- Button Up
    btnu: in STD LOGIC;
    btnd: in STD LOGIC;
                                    -- Button Down
    btnl: in STD LOGIC;
                                   -- Button Left
    btnr: in STD LOGIC;
                                   -- Button Right
    btnc: in STD LOGIC;
                                   -- Central Button (Reset)
    led : out STD LOGIC VECTOR(7 downto 0) -- 8-bit LED output
  );
end Counterc;
architecture Behavioral of Counterc is
  -- State Machine Definitions
  type State Type is (IDLE, CHECK SEQUENCE, SUCCESS); -- FSM states
  signal state
               : State Type := IDLE;
                                      -- Current FSM state
  -- Signals for LED Patterns
  signal display pattern: STD LOGIC VECTOR(7 downto 0) := (others => '0'); -- LED
display pattern
  signal flash clk
                    : STD LOGIC := '0';
                                                          -- Clock for flashing LEDs
  signal flash count : INTEGER := 0;
                                                          -- Counter for flashing clock
  constant FLASH DIVISOR: INTEGER:= 1000000;
                                                                    -- Flash speed
constant (smaller for testing)
  -- Sequence Detection
  signal sequence index : INTEGER range 0 to 3 := 0;
                                                                -- Tracks current
sequence position
  constant target_sequence : STD_LOGIC_VECTOR(3 downto 0) := "1101";
Encoded target sequence: btnu, btnd, btnl, btnr
  -- Debouncing Signals
  signal btnu stable, btnd stable, btnl stable, btnr stable, btnc stable : STD LOGIC := '0';
  signal btnu count, btnd count, btnl count, btnr count, btnr count : INTEGER := 0;
  constant DEBOUNCE COUNT: INTEGER := 100000;
                                                                       -- Debounce
delay
begin
  -- Button Debouncing Process
  process(clk)
  begin
    if rising edge(clk) then
      -- Debounce btnu
      if btnu = '1' then
         if btnu count < DEBOUNCE COUNT then
           btnu count <= btnu count + 1;
         else
           btnu stable <= '1';
```

```
end if;
else
  btnu count \leq 0;
  btnu stable <= '0';
end if;
-- Debounce btnd
if btnd = '1' then
  if btnd count < DEBOUNCE COUNT then
     btnd count <= btnd count + 1;
  else
     btnd_stable <= '1';
  end if;
else
  btnd count \leq 0;
  btnd stable <= '0';
end if;
-- Debounce btnl
if btnl = '1' then
  if btnl count < DEBOUNCE COUNT then
     btnl count <= btnl count + 1;
  else
     btnl_stable <= '1';
  end if;
else
  btnl count \leq 0;
  btnl stable <= '0';
end if;
-- Debounce btnr
if btnr = '1' then
  if btnr count < DEBOUNCE COUNT then
     btnr_count <= btnr_count + 1;</pre>
  else
     btnr_stable <= '1';
  end if;
else
  btnr_count \le 0;
  btnr stable <= '0';
end if;
-- Debounce btnc
if btnc = '1' then
  if btnc count < DEBOUNCE COUNT then
     btnc_count <= btnc_count + 1;</pre>
  else
     btnc stable <= '1';
  end if;
else
```

```
btnc count \leq 0;
       btnc stable <= '0';
     end if;
  end if:
end process;
-- Clock Divider for Flashing LEDs
process(clk)
begin
  if rising edge(clk) then
     if flash count = FLASH DIVISOR - 1 then
       flash clk <= not flash clk;
                                                        -- Toggle flashing clock
       flash count \leq 0;
                                                     -- Reset flash counter
     else
                                                           -- Increment flash counter
       flash count <= flash count + 1;
     end if;
  end if;
end process;
-- Main FSM Process
process(clk)
begin
  if rising edge(clk) then
     if btnc stable = '1' then
       -- Reset the system
       state <= IDLE;
       sequence index \leq 0;
       display pattern \leq (others \Rightarrow '0');
     else
       case state is
          when IDLE =>
            -- Detect button presses in sequence
            if btnu stable = '1' and sequence index = 0 then
               sequence index \leq 1;
            elsif btnd stable = '1' and sequence index = 1 then
               sequence index \leq 2;
            elsif btnl stable = '1' and sequence index = 2 then
               sequence index \leq 3;
            elsif btnr stable = '1' and sequence index = 3 then
               state <= SUCCESS; -- Sequence matched
            end if:
            -- Show "less" on LEDs based on button presses
            if btnu stable = '1' then
               display pattern <= "10000000";
            elsif btnd stable = '1' then
               display pattern <= "01000000";
            elsif btnl stable = '1' then
               display pattern <= "00100000";
            elsif btnr stable = '1' then
```

```
display_pattern <= "00010000";
             end if;
           when SUCCESS =>
              -- Flash LEDs (11111111 and 00000000 alternately)
             if flash_clk = '1' then
                display pattern <= "111111111"; -- All LEDs ON
                display_pattern <= "00000000"; -- All LEDs OFF
             end if;
           when others =>
             state <= IDLE; -- Default state
         end case;
      end if;
    end if;
  end process;
  -- Assign LED display pattern
  led <= display pattern;</pre>
end Behavioral;
detect up down down left right and flash
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.STD LOGIC UNSIGNED.ALL;
entity Counterc is
  Port (
                                   -- High-frequency clock signal
    clk: in STD LOGIC;
    btnu : in STD_LOGIC;
                                   -- Button Up
    btnd : in STD_LOGIC;
                                    -- Button Down
    btnl: in STD LOGIC;
                                  -- Button Left
    btnr: in STD LOGIC;
                                   -- Button Right
                                    -- Central Button (Reset)
    btnc: in STD LOGIC;
    led : out STD LOGIC VECTOR(7 downto 0) -- 8-bit LED output
  );
end Counterc;
architecture Behavioral of Counterc is
  -- State Machine Definitions
```

```
type State Type is (IDLE, WAIT DOWN1, WAIT DOWN2, WAIT LEFT,
WAIT RIGHT, SUCCESS, LOCK);
  signal state : State Type := IDLE;
                                                    -- Current FSM state
  -- Signals for LED Patterns
  signal display pattern: STD LOGIC VECTOR(7 downto 0) := (others => '0'); -- LED
display pattern
  signal flash clk
                    : STD LOGIC := '0';
                                                           -- Clock for flashing LEDs
  signal flash count : INTEGER := 0;
                                                           -- Counter for flashing clock
  constant FLASH DIVISOR : INTEGER := 5000000;
                                                                      -- Flashing speed
  -- Debounce Counters
  signal btnu count, btnd count, btnl count, btnr count : INTEGER := 0;
  constant DEBOUNCE COUNT: INTEGER := 500000;
                                                                         -- Debounce
threshold
  -- Stable Signals
  signal btnu stable, btnd stable, btnl stable, btnr stable : STD LOGIC := '0';
begin
  -- Clock Divider for Flashing LEDs
  process(clk)
  begin
    if rising edge(clk) then
       if flash count = FLASH DIVISOR - 1 then
         flash clk <= not flash clk;
                                                      -- Toggle flashing clock
         flash count \leq 0;
                                                   -- Reset flash counter
       else
         flash count <= flash count + 1;
                                                         -- Increment flash counter
       end if:
    end if;
  end process;
  -- Debouncing Logic for Each Button
  process(clk)
  begin
    if rising edge(clk) then
       -- Debounce btnu
       if btnu = '1' then
         if btnu count < DEBOUNCE COUNT then
           btnu count <= btnu count + 1;
         else
           btnu stable <= '1';
         end if;
       else
         btnu count \leq 0;
         btnu stable <= '0';
       end if;
       -- Debounce btnd
```

```
if btnd = '1' then
       if btnd count < DEBOUNCE COUNT then
          btnd count <= btnd count + 1;
          btnd stable <= '1';
       end if;
     else
       btnd count \leq 0;
       btnd stable <= '0';
     end if;
     -- Debounce btnl
     if btnl = '1' then
       if btnl count < DEBOUNCE_COUNT then
          btnl count <= btnl count + 1;
       else
          btnl stable <= '1';
       end if;
     else
       btnl count \leq 0;
       btnl stable <= '0';
     end if;
     -- Debounce btnr
     if btnr = '1' then
       if btnr count < DEBOUNCE COUNT then
          btnr count <= btnr count + 1;
       else
          btnr stable <= '1';
       end if;
     else
       btnr count \leq 0;
       btnr stable <= '0';
     end if;
  end if;
end process;
-- Main FSM Process
process(clk)
begin
  if rising edge(clk) then
     if btnc = '1' then
       -- Reset the system
       state <= IDLE;
       display pattern <= (others => '0');
     else
       case state is
          when IDLE =>
            -- Detect first button press (btnu)
            if btnu stable = '1' then
```

```
state <= WAIT_DOWN1;
           end if;
         when WAIT DOWN1 =>
           -- Detect first btnd
           if btnd stable = '1' then
              state <= WAIT DOWN2;
           end if;
         when WAIT DOWN2 =>
           -- Detect second btnd
           if btnd stable = '1' then
              state <= WAIT LEFT;
           end if;
         when WAIT LEFT =>
           -- Detect btnl
           if btnl stable = '1' then
              state <= WAIT RIGHT;
           end if;
         when WAIT RIGHT =>
           -- Detect btnr and move to SUCCESS
           if btnr stable = '1' then
              state <= SUCCESS;
           end if;
         when SUCCESS =>
           -- Flash LEDs (11111111 and 00000000 alternately)
           if flash clk = '1' then
              display_pattern <= "11111111"; -- All LEDs ON
           else
              display pattern <= "00000000"; -- All LEDs OFF
           end if;
         when LOCK =>
           -- Locked state: Reset with central button
           display pattern <= "10000001"; -- Indicate locked state
           if btnc = '1' then
              state <= IDLE;
           end if:
         when others =>
           state <= IDLE; -- Default to IDLE for unexpected states
       end case;
    end if;
  end if;
end process;
-- Assign LED display pattern
```

```
led <= display_pattern;
end Behavioral;</pre>
```

Counter that count how many total number of btn up down left right count

```
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.NUMERIC_STD.ALL;
entity Counterc is
  Port (
     clk: in STD_LOGIC; -- Clock signal
btnu: in STD_LOGIC; -- Button Up
btnd: in STD_LOGIC; -- Button Down
btnl: in STD_LOGIC; -- Button Left
btnr: in STD_LOGIC; -- Button Right
btnc: in STD_LOGIC; -- Reset Button
     btnc: in STD LOGIC;
                                          -- Reset Button
     led : out STD LOGIC VECTOR(7 downto 0) -- 8-bit LED output
   );
end Counterc;
architecture Behavioral of Counterc is
   -- Button Press Counter
  signal total count: INTEGER range 0 to 255 := 0; -- Total count of button presses
  -- Debounce Signals
  signal btnu stable, btnd stable, btnl stable, btnr stable : STD LOGIC := '0';
   signal btnu debounce, btnd debounce, btnl debounce, btnr debounce:
INTEGER range 0 to 500000 := 0;
  constant DEBOUNCE THRESHOLD: INTEGER: = 500000; -- Adjust for
debounce timing
```

```
-- Clock Divider for LED Updates
  signal slow clk: STD LOGIC := '0';
  signal clk_count : INTEGER := 0;
  constant CLK_DIVIDER: INTEGER:= 500000; -- Adjust for slower clock
begin
  -- Clock Divider Process
  process(clk)
  begin
    if rising edge(clk) then
       if clk count = CLK DIVIDER then
         slow_clk <= not slow_clk; -- Toggle slow clock
          clk count <= 0;
       else
          clk_count <= clk_count + 1;
     end if:
  end process;
  -- Debounce Process
  process(clk)
  begin
    if rising edge(clk) then
       -- Debounce btnu
       if btnu = '1' then
          if btnu_debounce < DEBOUNCE_THRESHOLD then
            btnu debounce <= btnu_debounce + 1;</pre>
            btnu stable <= '1';
         end if;
       else
          btnu debounce <= 0;
          btnu stable <= '0';
       end if;
       -- Debounce btnd
       if btnd = '1' then
         if btnd debounce < DEBOUNCE_THRESHOLD then
            btnd_debounce <= btnd_debounce + 1;</pre>
          else
            btnd_stable <= '1';
         end if;
       else
          btnd debounce <= 0;
          btnd stable <= '0';
       end if;
       -- Debounce btnl
       if btnl = '1' then
```

```
if btnl debounce < DEBOUNCE THRESHOLD then
            btnl debounce <= btnl debounce + 1;
            btnl stable <= '1';
          end if;
       else
          btnl debounce <= 0;
          btnl stable <= '0';
       end if:
       -- Debounce btnr
       if btnr = '1' then
          if btnr debounce < DEBOUNCE THRESHOLD then
            btnr debounce <= btnr debounce + 1;
          else
            btnr stable <= '1';
          end if:
       else
          btnr_debounce <= 0;
          btnr stable <= '0';
       end if;
     end if;
  end process;
  -- Counting Button Presses
  process(slow clk)
  begin
     if rising edge(slow clk) then
       if btnc = '1' then
          -- Reset the counter
          total count <= 0;
          -- Increment the counter for each stable button press
          if btnu stable = '1' or btnd stable = '1' or btnl stable = '1' or btnr stable =
'1' then
            total count <= total count + 1;
          end if:
       end if:
     end if:
  end process;
  -- LED Output
  process(slow clk)
  begin
     if rising edge(slow clk) then
       -- Display total count on LEDs
       led <= std_logic_vector(to_unsigned(total_count, 8));</pre>
     end if;
  end process;
```

end Behavioral;

Count the input and display 1010 pattern on 10th attempt

```
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.NUMERIC_STD.ALL;
entity SequenceDetector is
  Port (
    clk : in STD_LOGIC; -- Clock signal btnc : in STD_LOGIC; -- Initialization button (middle)
     btnu : in STD_LOGIC;
btnd : in STD_LOGIC;
                                      -- Button Up
                                       -- Button Down
    btnl : in STD_LOGIC; -- Button Left
btnr : in STD_LOGIC; -- Button Right
     led
           : out STD_LOGIC_VECTOR(6 downto 0) -- LED output for feedback
  );
end SequenceDetector;
architecture Behavioral of SequenceDetector is
  -- Constants
  constant MAX ATTEMPTS: integer := 10;
  constant FLASH PATTERN: STD LOGIC VECTOR(6 downto 0) := "1010100";
  -- Signal declarations
  type SymbolArray is array(0 to MAX_ATTEMPTS - 1) of std_logic_vector(1
downto 0);
```

```
signal entered symbols: SymbolArray:= (others => "00"); -- Stores entered
symbols
  signal current index: integer range 0 to MAX ATTEMPTS:= 0; -- Tracks the
current input index
  signal flash led: STD LOGIC:='0'; -- Indicates flashing state
  -- State management
  type DisplayState is (SHOW COUNT, FLASH PATTERN STATE);
  signal state : DisplayState := SHOW COUNT;
  -- Debounce signals
  signal btnc stable, btnu stable, btnd stable, btnl stable, btnr stable:
STD LOGIC := '0';
  signal btnc debounce, btnu debounce, btnd debounce, btnl debounce,
btnr debounce : integer range 0 to 1000000 := 0;
  constant DEBOUNCE THRESHOLD: integer: = 500000; -- Debounce threshold
for stable signals
  -- Clock divider
  signal slow clk: STD LOGIC := '0';
  signal clk count : integer := 0;
  constant CLK_DIVIDER: integer:= 10000000; -- Slower clock for processing
begin
  -- Clock divider process
  process(clk)
  begin
    if rising edge(clk) then
       if clk count = CLK DIVIDER then
         slow clk <= not slow clk;
         clk count <= 0;
       else
         clk count <= clk count + 1;
       end if:
    end if;
  end process;
  -- Debounce logic for buttons
  process(clk)
  begin
    if rising_edge(clk) then
       -- Debounce btnc
       if btnc = '1' then
         if btnc debounce < DEBOUNCE THRESHOLD then
            btnc debounce <= btnc debounce + 1;
         else
            btnc stable <= '1';
         end if:
       else
         btnc debounce <= 0;
         btnc stable <= '0';
```

```
end if;
  -- Debounce btnu
  if btnu = '1' then
    if btnu_debounce < DEBOUNCE_THRESHOLD then
       btnu debounce <= btnu debounce + 1;
    else
       btnu stable <= '1';
     end if;
  else
    btnu debounce <= 0;
     btnu_stable <= '0';
  end if;
  -- Debounce btnd
  if btnd = '1' then
    if btnd_debounce < DEBOUNCE_THRESHOLD then
       btnd debounce <= btnd debounce + 1;
       btnd_stable <= '1';
    end if;
  else
    btnd debounce <= 0;
    btnd stable <= '0';
  end if;
  -- Debounce btnl
  if btnl = '1' then
    if btnl_debounce < DEBOUNCE_THRESHOLD then
       btnl_debounce <= btnl_debounce + 1;</pre>
    else
       btnl_stable <= '1';
    end if;
  else
    btnl debounce <= 0;
     btnl stable <= '0';
  end if:
  -- Debounce btnr
  if btnr = '1' then
    if btnr_debounce < DEBOUNCE_THRESHOLD then
       btnr_debounce <= btnr_debounce + 1;
    else
       btnr stable <= '1';
    end if;
  else
    btnr_debounce <= 0;
    btnr stable <= '0';
  end if;
end if;
```

```
end process;
  -- Sequence input logic
  process(slow clk)
  begin
    if rising edge(slow clk) then
       case state is
         when SHOW COUNT =>
            if btnc stable = '1' then
              -- Reset the sequence and index
              current index <= 0;
              entered symbols <= (others => "00");
              flash led <= '0';
              state <= SHOW COUNT;
            elsif current index < MAX ATTEMPTS then
              -- Record the symbol based on the button pressed
              if btnu stable = '1' then
                 entered symbols(current index) <= "00"; -- Up
                 current index <= current index + 1;
              elsif btnd stable = '1' then
                 entered symbols(current index) <= "01"; -- Down
                 current index <= current index + 1;
              elsif btnl stable = '1' then
                 entered symbols(current index) <= "10"; -- Left
                 current index <= current index + 1;
              elsif btnr stable = '1' then
                 entered symbols(current index) <= "11"; -- Right
                 current index <= current index + 1;
              end if:
              -- Transition to FLASH PATTERN STATE if max attempts are
reached
              if current index = MAX ATTEMPTS then
                 state <= FLASH PATTERN STATE;
              end if;
            end if;
         when FLASH PATTERN STATE =>
            flash led <= '1'; -- Indicate flashing state
       end case;
    end if:
  end process;
  -- LED output process
  process(slow clk)
  begin
    if rising_edge(slow_clk) then
       if state = FLASH PATTERN STATE then
         -- Flash the LED pattern after 10 inputs
         led <= FLASH PATTERN;</pre>
```

```
else
          -- Display the number of inputs entered
          led <= std logic vector(to unsigned(current index, 7));</pre>
       end if:
    end if;
  end process;
end Behavioral;
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.NUMERIC STD.ALL;
   -- Clock signal
-- Initialization button (middle)
btnu : in STD_LOGIC;
btnd : in STD_LOGIC;
btnl : in STD_LOGIC;
btnr : in STD_LOGIC;
entity SequenceDetector is
  Port (
          : out STD LOGIC VECTOR(7 downto 0) -- LED output
end SequenceDetector;
architecture Behavioral of SequenceDetector is
  -- Constants
  constant MAX ATTEMPTS: integer := 10; -- Max number of button presses stored
  constant SEQUENCE LENGTH: integer := 5;
  constant LOCK_PATTERN: STD_LOGIC_VECTOR(7 downto 0) := "10101010"; --
Predefined locked pattern
  -- Target sequence definition (btnu, btnd, btnd, btnl, btnr)
  constant TARGET SEQUENCE : std logic vector(1 downto 0) := "00";
  constant TARGET SEQUENCE ARRAY: std logic vector(9 downto 0) :=
"0010011011"; -- Encoded
  -- Signal declarations
  type SymbolArray is array(0 to MAX ATTEMPTS - 1) of std logic vector(1 downto 0);
  signal entered symbols : SymbolArray := (others => "00");
  signal current index: integer range 0 to MAX ATTEMPTS:=0; -- Tracks current input
position
  signal sequence detected: STD LOGIC:='0'; -- Indicates sequence is found
  signal locked: STD LOGIC:='0'; -- Indicates system is locked
```

```
signal flash clk: STD LOGIC := '0'; -- Flashing clock for LEDs
  signal flash count : integer := 0;
  -- Button debounce signals
  signal btnu stable, btnd stable, btnl stable, btnr stable, btnc stable : STD LOGIC := '0';
  signal btnu debounce, btnd debounce, btnl debounce, btnr debounce, btnc debounce :
integer range 0 to 1000000 := 0;
  constant DEBOUNCE THRESHOLD: integer := 500000; -- Debounce threshold
  -- Clock divider
  signal slow clk: STD LOGIC := '0';
  signal clk count : integer := 0;
  constant CLK DIVIDER: integer:= 10000000; -- Slower clock for processing
begin
  -- Clock divider process
  process(clk)
  begin
    if rising edge(clk) then
       if clk count = CLK DIVIDER then
         slow clk <= not slow clk;
         clk count \leq 0;
       else
         clk count <= clk count + 1;
       end if;
       -- Flash clock for LEDs
       if flash count = CLK DIVIDER / 2 then
         flash clk <= not flash clk;
         flash count \leq 0;
       else
         flash count <= flash count + 1;
       end if;
    end if;
  end process;
  -- Debounce process for stable button signals
  process(clk)
  begin
    if rising edge(clk) then
       -- Debounce btnu
       if btnu = '1' then
         if btnu debounce < DEBOUNCE THRESHOLD then
            btnu debounce <= btnu debounce + 1;
         else
            btnu stable <= '1';
         end if;
       else
         btnu debounce \leq 0;
         btnu stable <= '0';
       end if;
```

```
-- Debounce btnd
    if btnd = '1' then
       if btnd debounce < DEBOUNCE THRESHOLD then
         btnd debounce <= btnd debounce + 1;
       else
         btnd_stable <= '1';
       end if;
    else
       btnd debounce <= 0;
       btnd stable <= '0';
    end if;
    -- Debounce btnl
    if btnl = '1' then
       if btnl_debounce < DEBOUNCE_THRESHOLD then
         btnl_debounce <= btnl_debounce + 1;</pre>
         btnl stable <= '1';
       end if;
    else
       btnl debounce \leq 0;
       btnl stable <= '0';
    end if;
    -- Debounce btnr
    if btnr = '1' then
       if btnr debounce < DEBOUNCE THRESHOLD then
         btnr_debounce <= btnr_debounce + 1;</pre>
       else
         btnr_stable <= '1';
       end if;
    else
       btnr debounce \leq 0;
       btnr stable <= '0';
    end if;
    -- Debounce btnc
    if btnc = '1' then
       if btnc debounce < DEBOUNCE THRESHOLD then
         btnc debounce <= btnc debounce + 1;
       else
         btnc_stable <= '1';
       end if;
       btnc debounce \leq 0;
       btnc stable <= '0';
    end if;
  end if;
end process;
```

```
-- Sequence input and detection process
process(slow clk)
begin
  if rising edge(slow clk) then
    if btnc stable = '1' then
       -- Reset system
       current index \leq 0;
       entered symbols <= (others => "00");
       sequence detected <= '0';
       locked <= '0';
    elsif current index < MAX ATTEMPTS then
       -- Record button press
       if btnu stable = '1' then
         entered symbols(current index) <= "00";
         current index <= current index + 1;
       elsif btnd stable = '1' then
         entered symbols(current index) <= "01";
         current index <= current index + 1;
       elsif btnl stable = '1' then
         entered symbols(current index) <= "10";
         current index <= current index + 1;
       elsif btnr stable = '1' then
         entered symbols(current index) <= "11";
         current index <= current index + 1;
       end if;
       -- Check for sequence
       for i in 0 to MAX ATTEMPTS - SEQUENCE_LENGTH loop
         if entered symbols(i) = "00" and
           entered symbols(i + 1) = "01" and
           entered symbols(i + 2) = "01" and
           entered symbols(i + 3) = "10" and
           entered symbols(i + 4) = "11" then
            sequence detected <= '1';
            locked <= '0';
            exit;
         end if;
       end loop;
       -- Lock system if full and no sequence found
       if current index = MAX ATTEMPTS and sequence detected = '0' then
         locked <= '1';
       end if;
    end if;
  end if;
end process;
-- LED output control
process(flash clk)
```

```
begin
    if sequence detected = '1' then
      -- Flash LEDs
      led <= (others => flash clk);
    elsif locked = '1' then
      -- Show locked pattern
      led <= LOCK PATTERN;</pre>
    else
      -- Default: show number of inputs
      led <= std_logic_vector(to_unsigned(current index, 8));</pre>
    end if:
  end process;
end Behavioral;
GENERATE 10101010 ON EVERY 11 TH BOTTOM PRESS
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.NUMERIC STD.ALL;
entity Counterc is
  Port (
                                   -- Clock signal
    clk: in STD LOGIC;
    btnu: in STD LOGIC;
                                   -- Button Up
                                   -- Button Down
    btnd: in STD LOGIC;
    btnl: in STD LOGIC;
                                   -- Button Left
    btnr: in STD LOGIC;
                                   -- Button Right
    btnc: in STD LOGIC;
                                   -- Reset Button
    led : out STD LOGIC VECTOR(7 downto 0) -- 8-bit LED output
  );
end Counterc;
architecture Behavioral of Counterc is
  -- Button Press Counter
  signal total count : INTEGER range 0 to 255 := 0; -- Total count of button presses
  -- Debounce Signals
  signal btnu stable, btnd stable, btnl stable, btnr stable : STD LOGIC := '0';
  signal btnu debounce, btnl debounce, btnl debounce : INTEGER range 0
to 500000 := 0;
  constant DEBOUNCE THRESHOLD: INTEGER := 500000; -- Adjust for debounce
timing
  -- Clock Divider for LED Updates
  signal slow clk : STD LOGIC := '0';
  signal clk count : INTEGER := 0;
  constant CLK DIVIDER: INTEGER: = 500000; -- Adjust for slower clock
begin
```

```
-- Clock Divider Process
process(clk)
begin
  if rising edge(clk) then
    if clk count = CLK DIVIDER then
       slow_clk <= not slow_clk; -- Toggle slow clock</pre>
       clk count \le 0;
    else
       clk count <= clk count + 1;
    end if;
  end if;
end process;
-- Debounce Process
process(clk)
begin
  if rising edge(clk) then
    -- Debounce btnu
    if btnu = '1' then
       if btnu debounce < DEBOUNCE THRESHOLD then
         btnu debounce <= btnu debounce + 1;
       else
         btnu_stable <= '1';
       end if;
    else
       btnu_debounce <= 0;
       btnu stable <= '0';
    end if;
    -- Debounce btnd
    if btnd = '1' then
       if btnd debounce < DEBOUNCE THRESHOLD then
         btnd debounce <= btnd debounce + 1;
       else
         btnd_stable <= '1';
       end if;
    else
       btnd debounce \leq 0;
       btnd stable <= '0';
    end if:
    -- Debounce btnl
    if btnl = '1' then
       if btnl debounce < DEBOUNCE THRESHOLD then
         btnl debounce <= btnl debounce + 1;
       else
         btnl stable <= '1';
       end if;
    else
```

```
btnl debounce \leq 0;
       btnl stable <= '0';
     end if;
     -- Debounce btnr
     if btnr = '1' then
       if btnr debounce < DEBOUNCE THRESHOLD then
          btnr debounce <= btnr debounce + 1;
       else
         btnr_stable <= '1';
       end if;
     else
       btnr debounce \leq 0;
       btnr stable <= '0';
     end if;
  end if;
end process;
-- Counting Button Presses
process(slow clk)
begin
  if rising edge(slow clk) then
     if btnc = '1' then
       -- Reset the counter
       total count \leq 0;
     else
       -- Increment the counter for each stable button press
       if btnu stable = '1' or btnd stable = '1' or btnl stable = '1' or btnr stable = '1' then
          total count <= total count + 1;
       end if;
     end if;
  end if;
end process;
-- LED Output
process(slow clk)
begin
  if rising edge(slow clk) then
     if btnc = '1' then
       -- Clear LEDs on reset
       led \le (others => '0');
     elsif total count mod 11 = 0 and total count \neq 0 then
       -- Display 10101010 on every 11th button press
       led <= "10101010";
     else
       -- Display total count on LEDs
       led <= std logic vector(to unsigned(total count, 8));
     end if;
  end if;
end process;
```

```
end Behavioral;
```

```
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.NUMERIC STD.ALL;
entity Counterc is
  Port (
    clk: in STD LOGIC;
                              -- Clock signal
    btnu: in STD LOGIC;
                                 -- Button Up
    btnd: in STD LOGIC;
                                 -- Button Down
                          -- Button Left
-- Button Righ
    btnl: in STD LOGIC;
    btnr: in STD LOGIC;
                                 -- Button Right
    btnc: in STD LOGIC;
                                 -- Reset Button
    led : out STD LOGIC VECTOR(7 downto 0) -- 8-bit LED output
  );
end Counterc;
architecture Behavioral of Counterc is
  -- Button Press Counter
  signal total count : INTEGER range 0 to 255 := 0; -- Total count of button presses
  -- Debounce Signals
  signal btnu stable, btnd stable, btnl stable, btnr stable : STD LOGIC := '0';
  signal btnu debounce, btnd debounce, btnl debounce, btnr debounce : INTEGER range 0
to 500000 := 0;
  constant DEBOUNCE THRESHOLD: INTEGER := 500000; -- Adjust for debounce
timing
  -- Clock Divider for LED Updates
  signal slow clk: STD LOGIC := '0';
  signal clk count : INTEGER := 0;
  constant CLK DIVIDER: INTEGER := 21 000 000; -- Slightly increased for slower
operation
  signal stop flag: STD LOGIC:='0'; -- Flag to stop the system
begin
  -- Clock Divider Process
  process(clk)
  begin
    if rising edge(clk) then
      if clk count = CLK DIVIDER then
        slow clk <= not slow clk; -- Toggle slow clock
        clk count \le 0;
      else
        clk count <= clk count + 1;
      end if:
```

```
end if;
end process;
-- Debounce Process
process(clk)
begin
  if rising edge(clk) then
    -- Debounce btnu
    if btnu = '1' then
       if btnu debounce < DEBOUNCE THRESHOLD then
         btnu debounce <= btnu debounce + 1;
       else
         btnu stable <= '1';
       end if;
    else
       btnu debounce \leq 0;
       btnu stable <= '0';
    end if;
    -- Debounce btnd
    if btnd = '1' then
       if btnd debounce < DEBOUNCE THRESHOLD then
         btnd debounce <= btnd debounce + 1;
       else
         btnd stable <= '1';
       end if;
    else
       btnd debounce \leq 0;
       btnd stable <= '0';
    end if;
    -- Debounce btnl
    if btnl = '1' then
       if btnl debounce < DEBOUNCE THRESHOLD then
         btnl debounce <= btnl debounce + 1;
       else
         btnl_stable <= '1';
       end if;
       btnl debounce \leq 0;
       btnl_stable <= '0';
    end if;
    -- Debounce btnr
    if btnr = '1' then
       if btnr debounce < DEBOUNCE THRESHOLD then
         btnr debounce <= btnr debounce + 1;
         btnr stable <= '1';
       end if;
```

```
else
          btnr debounce \leq 0;
          btnr stable <= '0';
       end if;
     end if;
  end process;
  -- Counting Button Presses
  process(slow clk)
  begin
     if rising edge(slow clk) then
       if btnc = '1' then
          -- Reset the counter and clear the stop flag
          total count \leq 0;
          stop flag \leq 10';
       elsif stop flag = '0' then
          -- Increment the counter for each stable button press if not stopped
          if btnu stable = '1' or btnd stable = '1' or btnl stable = '1' or btnr stable = '1' then
            total count <= total count + 1;
          end if;
          -- Stop when total count reaches 11
          if total count = 11 then
            stop flag <= '1'; -- Activate the stop flag
          end if;
       end if;
     end if;
  end process;
  -- LED Output
  process(slow clk)
  begin
     if rising edge(slow clk) then
       if btnc = '1' then
          -- Clear LEDs on reset
          led \le (others => '0');
       elsif stop flag = '1' then
          -- Freeze LEDs to 10101010 when stopped
          led <= "10101010";
       else
          -- Display total count on LEDs
          led <= std logic vector(to unsigned(total count, 8));
       end if;
     end if;
  end process;
end Behavioral;
```

```
library IEEE;
use IEEE.STD LOGIC_1164.ALL;
use IEEE.NUMERIC STD.ALL;
entity SequenceDetector is
  Port (
    clk
          : in STD LOGIC;
                                   -- Clock signal
    btnc : in STD LOGIC;
                                   -- Initialization button (center)
    btnu : in STD LOGIC;
                                   -- Button Up
    btnd : in STD LOGIC;
                                   -- Button Down
    btnl : in STD LOGIC;
                                   -- Button Left
    btnr : in STD LOGIC;
                                   -- Button Right
          : out STD LOGIC VECTOR(7 downto 0) -- LED output
    led
  );
end SequenceDetector;
architecture Behavioral of SequenceDetector is
  -- Constants
  constant MAX ATTEMPTS: integer := 15; -- Maximum button presses stored
  constant SEQUENCE LENGTH: integer := 5;
  -- Signal declarations
  type SymbolArray is array(0 to MAX ATTEMPTS - 1) of std logic vector(1 downto 0);
  signal entered symbols : SymbolArray := (others => "00");
  signal current index : integer range 0 to MAX ATTEMPTS := 0; -- Tracks current input
position
  signal sequence detected: STD LOGIC:='0'; -- Indicates sequence is found
  signal led output : STD LOGIC VECTOR(7 downto 0) := (others => '0'); -- LED output
  -- Button debounce signals
  signal btnu_stable, btnd_stable, btnl stable, btnr stable, btnc stable : STD LOGIC := '0';
  signal btnu debounce, btnd debounce, btnl debounce, btnr debounce, btnc debounce :
integer range 0 to 1000000 := 0;
  constant DEBOUNCE THRESHOLD: integer := 500000; -- Debounce threshold
  -- Clock divider
  signal slow clk: STD LOGIC := '0';
  signal clk count : integer := 0;
  constant CLK DIVIDER: integer:= 20000000; -- Slower clock for processing
begin
  -- Clock divider process
  process(clk)
  begin
    if rising edge(clk) then
      if clk count = CLK DIVIDER then
        slow clk <= not slow clk;
        clk count \le 0;
```

```
else
       clk count <= clk count + 1;
  end if;
end process;
-- Debounce process for stable button signals
process(clk)
begin
  if rising edge(clk) then
    -- Debounce logic for each button
    if btnu = '1' then
       if btnu debounce < DEBOUNCE THRESHOLD then
         btnu debounce <= btnu debounce + 1;
       else
         btnu_stable <= '1';
       end if;
    else
       btnu_debounce <= 0;
       btnu_stable <= '0';
    end if;
    if btnd = '1' then
       if btnd debounce < DEBOUNCE THRESHOLD then
         btnd debounce <= btnd debounce + 1;
         btnd stable <= '1';
       end if;
    else
       btnd debounce \leq 0;
       btnd stable <= '0';
    end if;
    if btnl = '1' then
       if btnl debounce < DEBOUNCE THRESHOLD then
         btnl_debounce <= btnl_debounce + 1;</pre>
       else
         btnl stable <= '1';
       end if;
    else
       btnl debounce \leq 0;
       btnl stable <= '0';
    end if;
    if btnr = '1' then
       if btnr debounce < DEBOUNCE THRESHOLD then
         btnr debounce <= btnr debounce + 1;
         btnr stable <= '1';
       end if;
```

```
else
       btnr debounce \leq 0;
       btnr stable <= '0';
    end if:
    if btnc = '1' then
       if btnc debounce < DEBOUNCE THRESHOLD then
         btnc debounce <= btnc debounce + 1;
       else
         btnc stable <= '1';
       end if;
    else
       btnc debounce \leq 0;
       btnc stable <= '0';
    end if;
  end if:
end process;
-- Sequence detection and LED output process
process(slow clk)
  variable temp sequence: SymbolArray; -- Temporary sequence holder
begin
  if rising edge(slow clk) then
    if btnc stable = '1' then
       -- Reset system
       current index \leq 0;
       entered symbols <= (others => "00");
       sequence detected <= '0';
       led output \leq (others \Rightarrow '0');
    elsif current index < MAX ATTEMPTS then
       -- Record button press
       if btnu stable = '1' then
         entered symbols(current index) <= "00";
         current index <= current index + 1;
       elsif btnd stable = '1' then
         entered symbols(current index) <= "01";
         current index <= current index + 1;
       elsif btnl stable = '1' then
         entered symbols(current index) <= "10";
         current index <= current index + 1;
       elsif btnr stable = '1' then
         entered symbols(current index) <= "11";
         current index <= current index + 1;
       end if;
       -- Check for the specific sequences
       temp sequence := entered symbols;
       if (temp sequence(0) = "00" and temp sequence(1) = "01" and
         temp sequence(2) = "01" and temp sequence(3) = "10" and
         temp sequence(4) = "11") then
```

```
sequence detected <= '1';
        elsif (temp sequence(1) = "00" and temp sequence(2) = "01" and
            temp sequence(3) = "01" and temp sequence(4) = "10" and
            temp sequence(5) = "11") then
          sequence detected <= '1';
        end if;
      end if;
      -- Set LED output based on sequence detection
      if sequence detected = '1' then
        led output <= (others => '1'); -- Display `11111111`
      else
        led output <= std logic vector(to unsigned(current index, 8)); -- Default to
current index
      end if:
    end if;
  end process;
  -- Assign LED output
  led <= led output;
end Behavioral;
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.NUMERIC STD.ALL;
entity CombinedSystem is
  Port (
                             -- Clock signal
    clk: in STD LOGIC;
    btnc: in STD LOGIC;
                               -- Reset button
    btnu: in STD LOGIC;
                                -- Button Up
    btnd: in STD LOGIC;
                                 -- Button Down
    btnl: in STD LOGIC;
                                -- Button Left
    btnr: in STD LOGIC;
                                 -- Button Right
    led : out STD LOGIC VECTOR(7 downto 0) -- LED output
end CombinedSystem;
architecture Behavioral of CombinedSystem is
  -- Constants
  constant MAX ATTEMPTS: integer := 15; -- Maximum button presses stored
  constant SEQUENCE LENGTH: integer := 5;
  constant DEBOUNCE THRESHOLD: integer := 500000; -- Debounce threshold
  constant CLK_DIVIDER: integer:= 15000000; -- Reduced Clock divider for faster
processing
```

```
-- Button Press Counter
  signal total count: INTEGER range 0 to 255 := 0; -- Total count of button presses
  signal stop flag: STD LOGIC:='0'; -- Stops counting at 11
  -- Sequence Detection
  type SymbolArray is array(0 to MAX ATTEMPTS - 1) of std logic vector(1 downto 0);
  signal entered symbols: SymbolArray := (others => "00");
  signal current index : integer range 0 to MAX ATTEMPTS := 0; -- Tracks current input
position
  signal sequence detected: STD LOGIC:='0'; -- Indicates sequence is found
  -- Clock Divider
  signal slow clk : STD_LOGIC := '0';
  signal clk count : integer := 0;
  -- Debounce Signals
  signal btnu stable, btnd stable, btnl stable, btnr stable, btnc stable : STD LOGIC := '0';
  signal btnu debounce, btnd debounce, btnl debounce, btnr debounce, btnc debounce:
integer range 0 to 1000000 := 0;
  -- LED Output
  signal led output : STD LOGIC VECTOR(7 downto 0) := (others => '0');
begin
  -- Clock Divider Process
  process(clk)
  begin
    if rising edge(clk) then
       if clk count = CLK DIVIDER then
         slow clk <= not slow clk;
         clk count \le 0;
       else
         clk count <= clk count + 1;
       end if;
    end if;
  end process;
  -- Debounce Process
  process(clk)
  begin
    if rising edge(clk) then
       -- Debounce btnu
       if btnu = '1' then
         if btnu debounce < DEBOUNCE THRESHOLD then
           btnu debounce <= btnu debounce + 1;
         else
           btnu stable <= '1';
         end if;
       else
         btnu debounce \leq 0;
         btnu stable <= '0';
```

```
end if;
  -- Debounce btnd
  if btnd = '1' then
    if btnd debounce < DEBOUNCE THRESHOLD then
       btnd debounce <= btnd debounce + 1;
    else
       btnd stable <= '1';
    end if;
  else
    btnd debounce \leq 0;
    btnd stable <= '0';
  end if;
  -- Debounce btnl
  if btnl = '1' then
    if btnl debounce < DEBOUNCE THRESHOLD then
       btnl debounce <= btnl debounce + 1;
    else
       btnl stable <= '1';
    end if;
  else
    btnl debounce \leq 0;
    btnl stable <= '0';
  end if;
  -- Debounce btnr
  if btnr = '1' then
    if btnr debounce < DEBOUNCE THRESHOLD then
       btnr debounce <= btnr_debounce + 1;</pre>
    else
       btnr stable <= '1';
    end if;
  else
    btnr debounce \leq 0;
    btnr stable <= '0';
  end if;
  -- Debounce btnc
  if btnc = '1' then
    if btnc debounce < DEBOUNCE THRESHOLD then
       btnc_debounce <= btnc_debounce + 1;</pre>
    else
       btnc stable <= '1';
    end if;
  else
    btnc debounce \leq 0;
    btnc stable <= '0';
  end if;
end if;
```

```
end process;
```

```
-- Counter and Sequence Detection Process
process(slow clk)
  variable temp sequence: SymbolArray; -- Temporary sequence holder
  variable match count : integer := 0; -- Tracks matching symbols
begin
  if rising edge(slow clk) then
     if btnc stable = '1' then
       -- Reset system
       total count \leq 0;
       stop flag \leq 10';
       current index \leq 0;
       entered symbols <= (others => "00");
       sequence detected <= '0';
       led output \leq (others \Rightarrow '0');
     elsif sequence detected = '0' then
       -- Count button presses
       if stop flag = '0' then
          if btnu stable = '1' or btnd stable = '1' or btnl stable = '1' or btnr stable = '1' then
            total count <= total count + 1;
          end if;
          -- Stop counting at 11
          if total count = 11 then
            stop flag \leq 11';
          end if;
       end if:
       -- Record button press for sequence detection
       if btnu stable = '1' then
          entered symbols(current index) <= "00";
          current index <= current index + 1;
       elsif btnd stable = '1' then
          entered symbols(current index) <= "01";
          current index <= current index + 1;
       elsif btnl stable = '1' then
          entered symbols(current index) <= "10";
          current index <= current index + 1;
       elsif btnr stable = '1' then
          entered symbols(current index) <= "11";
          current index <= current index + 1;
       end if;
       -- Check for target sequence in any position
       for i in 0 to MAX ATTEMPTS - SEQUENCE LENGTH loop
          match count := 0;
          if entered symbols(i) = "00" then
            match count := match count + 1;
          end if;
```

```
if entered symbols(i + 1) = "01" then
              match count := match count + 1;
            end if;
            if entered symbols(i + 2) = "01" then
              match count := match count + 1;
            end if;
            if entered_symbols(i + 3) = "10" then
              match count := match count + 1;
            end if;
            if entered symbols(i + 4) = "11" then
              match count := match count + 1;
            end if;
            if match count = 5 then
              sequence detected <= '1';
              exit;
            end if;
         end loop;
       end if;
       -- Set LED output
       if sequence detected = '1' then
         led output <= (others => '1'); -- Display `111111111`
       elsif stop flag = '1' then
         led output <= "10101010"; -- Display `10101010` when stopped
         led output <= std logic vector(to unsigned(total count, 8)); -- Default to count
       end if;
    end if;
  end process;
  -- Assign LED output
  led <= led output;
end Behavioral;
```

```
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.NUMERIC STD.ALL;
entity CombinedSystem is
  Port (
    clk: in STD LOGIC;
                                -- Clock signal
    btnc: in STD LOGIC;
                                  -- Reset button
                              -- Button Up
-- Button Down
    btnu: in STD LOGIC;
    btnd: in STD LOGIC;
    btnl : in STD_LOGIC;
                                -- Button Left
    btnr: in STD LOGIC;
                                  -- Button Right
    led : out STD LOGIC VECTOR(7 downto 0) -- LED output
end CombinedSystem;
architecture Behavioral of CombinedSystem is
  -- Constants
  constant MAX ATTEMPTS: integer := 15; -- Maximum button presses stored
  constant SEQUENCE LENGTH: integer := 5;
  constant DEBOUNCE THRESHOLD: integer := 500000; -- Debounce threshold
  constant CLK DIVIDER: integer:= 15000000; -- Reduced Clock divider for faster
processing
  constant FLASH DIVIDER: integer:= 10000000; -- Divider for blinking LEDs
  -- Button Press Counter
  signal total count: INTEGER range 0 to 255 := 0; -- Total count of button presses
  signal stop flag: STD LOGIC:='0'; -- Stops counting at 11
  -- Sequence Detection
  type SymbolArray is array(0 to MAX ATTEMPTS - 1) of std logic vector(1 downto 0);
  signal entered symbols : SymbolArray := (others => "00");
  signal current index: integer range 0 to MAX ATTEMPTS:=0; -- Tracks current input
position
  signal sequence detected: STD LOGIC:='0'; -- Indicates sequence is found
  -- Clock Divider
  signal slow clk: STD LOGIC := '0';
  signal flash clk: STD LOGIC := '0'; -- Blinking clock
  signal clk count : integer := 0;
  signal flash count : integer := 0;
  -- Debounce Signals
  signal btnu stable, btnd stable, btnl stable, btnr stable, btnc stable : STD LOGIC := '0';
  signal btnu debounce, btnd debounce, btnl debounce, btnr debounce, btnc debounce :
integer range 0 to 1000000 := \overline{0};
```

-- LED Output

```
signal led_output : STD_LOGIC_VECTOR(7 downto 0) := (others => '0');
  signal flash pattern: STD LOGIC VECTOR(7 downto 0) := (others => '0'); -- Temporary
pattern for blinking
begin
  -- Clock Divider Process
  process(clk)
  begin
    if rising edge(clk) then
       -- Generate slow clock
       if clk count = CLK DIVIDER then
         slow clk <= not slow clk;
         clk count \le 0;
         clk count \le clk count + 1;
       end if:
       -- Generate flash clock for blinking
       if flash count = FLASH DIVIDER then
         flash clk <= not flash clk;
         flash count \leq 0;
       else
         flash count <= flash count + 1;
       end if;
    end if;
  end process;
  -- Debounce Process
  process(clk)
  begin
    if rising edge(clk) then
       -- Debounce btnu
       if btnu = '1' then
         if btnu debounce < DEBOUNCE THRESHOLD then
           btnu debounce <= btnu debounce + 1;
         else
           btnu stable <= '1';
         end if;
       else
         btnu debounce \leq 0;
         btnu stable <= '0';
       end if:
       -- Debounce btnd
       if btnd = '1' then
         if btnd debounce < DEBOUNCE THRESHOLD then
           btnd debounce <= btnd debounce + 1;
         else
           btnd stable <= '1';
         end if;
       else
```

```
btnd debounce \leq 0;
       btnd stable <= '0';
    end if;
    -- Debounce btnl
    if btnl = '1' then
       if btnl debounce < DEBOUNCE THRESHOLD then
         btnl debounce <= btnl debounce + 1;
       else
         btnl stable <= '1';
       end if;
    else
       btnl debounce \leq 0;
       btnl stable <= '0';
    end if;
    -- Debounce btnr
    if btnr = '1' then
       if btnr debounce < DEBOUNCE THRESHOLD then
         btnr debounce <= btnr debounce + 1;
       else
         btnr stable <= '1';
       end if;
    else
       btnr debounce \leq 0;
       btnr_stable <= '0';
    end if;
    -- Debounce btnc
    if btnc = '1' then
       if btnc debounce < DEBOUNCE THRESHOLD then
         btnc debounce <= btnc debounce + 1;
       else
         btnc stable <= '1';
       end if;
    else
       btnc debounce \leq 0;
       btnc_stable <= '0';
    end if;
  end if;
end process;
-- Counter and Sequence Detection Process
process(slow clk)
  variable temp sequence: SymbolArray; -- Temporary sequence holder
  variable match count : integer := 0; -- Tracks matching symbols
begin
  if rising edge(slow clk) then
    if btnc stable = '1' then
       -- Reset system
```

```
total count \leq 0:
  stop flag \leq 10';
  current index <= 0;
  entered symbols <= (others => "00");
  sequence detected <= '0';
  led output \leq= (others \Rightarrow '0');
elsif sequence detected = '0' then
  -- Count button presses
  if stop flag = '0' then
     if btnu stable = '1' or btnd_stable = '1' or btnl_stable = '1' or btnr_stable = '1' then
       total count <= total count + 1;
     end if:
     -- Stop counting at 11
     if total count = 11 then
       stop flag <= '1';
     end if;
  end if;
  -- Record button press for sequence detection
  if btnu stable = '1' then
     entered_symbols(current index) <= "00";
     current index <= current index + 1;
  elsif btnd stable = '1' then
     entered symbols(current index) <= "01";
     current index <= current index + 1;
  elsif btnl stable = '1' then
     entered symbols(current index) <= "10";
     current index <= current index + 1;
  elsif btnr stable = '1' then
     entered symbols(current index) <= "11";
     current index <= current index + 1;
  end if;
  -- Check for target sequence in any position
  for i in 0 to MAX_ATTEMPTS - SEQUENCE_LENGTH loop
     match count := 0;
     if entered symbols(i) = "00" then
       match count := match count + 1;
     end if:
     if entered symbols(i + 1) = "01" then
       match count := match count + 1;
     end if:
     if entered symbols(i + 2) = "01" then
       match count := match count + 1;
     end if;
     if entered symbols(i + 3) = "10" then
       match count := match count + 1;
     end if:
     if entered symbols(i + 4) = "11" then
```

```
match_count := match_count + 1;
            end if;
            if match_count = 5 then
               sequence detected <= '1';
               exit;
            end if;
          end loop;
       end if;
       -- Set LED blinking patterns
       if sequence_detected = '1' then
          flash_pattern <= (others => flash_clk); -- Blink `111111111` and `00000000`
       elsif stop flag = '1' then
          if flash clk = '1' then
            flash_pattern <= "10101010";
            flash pattern <= "01010101";
          end if;
       else
          flash pattern <= std logic vector(to unsigned(total count, 8)); -- Default to count
       led_output <= flash_pattern;</pre>
     end if;
  end process;
  -- Assign LED output
  led <= led_output;</pre>
end Behavioral;
```

```
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.NUMERIC STD.ALL;
entity CombinedSystem is
   btnc: in STD_LOGIC; -- Clock signal
btnc: in STD_LOGIC; -- Reset button
btnu: in STD_LOGIC; -- Button Up
btnd: in STD_LOGIC; -- Button Down
btnl: in STD_LOGIC; -- Button Left
btnr: in STD_LOGIC; -- Button Pictor
led: out STD_LOGIC TO
  Port (
    led : out STD LOGIC VECTOR(7 downto 0) -- LED output
end CombinedSystem;
architecture Behavioral of CombinedSystem is
  -- Constants
  constant MAX ATTEMPTS: integer := 15; -- Maximum button presses stored
  constant SEQUENCE LENGTH: integer := 5;
  constant DEBOUNCE THRESHOLD: integer := 500000; -- Debounce threshold
  constant CLK DIVIDER: integer := 12000000; -- Slightly faster processing
  constant FLASH DIVIDER: integer:= 8000000; -- Slightly faster blinking
  -- Button Press Counter
  signal total count: INTEGER range 0 to 255 := 0; -- Total count of button presses
  signal stop flag: STD LOGIC:='0'; -- Stops counting at 11
  -- Sequence Detection
  type SymbolArray is array(0 to MAX ATTEMPTS - 1) of std logic vector(1 downto 0);
  signal entered symbols: SymbolArray := (others => "00");
  signal current index: integer range 0 to MAX ATTEMPTS:= 0; -- Tracks current input
position
  signal sequence detected: STD LOGIC:='0'; -- Indicates sequence is found
  -- Clock Divider
  signal slow clk: STD LOGIC := '0';
  signal flash clk: STD LOGIC := '0'; -- Blinking clock
  signal clk count : integer := 0;
  signal flash count : integer := 0;
  -- Debounce Signals
  signal btnu stable, btnd stable, btnl stable, btnr stable, btnc stable : STD LOGIC := '0';
  signal btnu debounce, btnd debounce, btnl debounce, btnr debounce, btnc debounce :
integer range 0 to 1000000 := 0;
  -- LED Output
  signal led output : STD LOGIC VECTOR(7 downto 0) := (others => '0');
```

```
signal flash_pattern : STD_LOGIC_VECTOR(7 downto 0) := (others => '0'); -- Temporary
pattern for blinking
begin
  -- Clock Divider Process
  process(clk)
  begin
    if rising edge(clk) then
       -- Generate slow clock
       if clk count = CLK DIVIDER then
         slow clk <= not slow clk;
         clk count \le 0;
       else
         clk count \le clk count + 1;
       end if:
       -- Generate flash clock for blinking
       if flash count = FLASH DIVIDER then
         flash clk <= not flash clk;
         flash count \leq 0;
       else
         flash count <= flash count + 1;
       end if;
    end if;
  end process;
  -- Debounce Process
  process(clk)
  begin
    if rising edge(clk) then
       -- Debounce btnu
       if btnu = '1' then
         if btnu debounce < DEBOUNCE THRESHOLD then
            btnu debounce <= btnu debounce + 1;
         else
            btnu stable <= '1';
         end if;
       else
         btnu debounce \leq 0;
         btnu stable <= '0';
       end if;
       -- Debounce btnd
       if btnd = '1' then
         if btnd debounce < DEBOUNCE THRESHOLD then
            btnd debounce <= btnd debounce + 1;
         else
            btnd stable <= '1';
         end if;
       else
         btnd debounce \leq 0;
```

```
btnd stable <= '0';
    end if;
    -- Debounce btnl
    if btnl = '1' then
       if btnl debounce < DEBOUNCE THRESHOLD then
         btnl debounce <= btnl debounce + 1;
       else
         btnl stable <= '1';
       end if;
    else
       btnl debounce \leq 0;
       btnl stable <= '0';
    end if;
    -- Debounce btnr
    if btnr = '1' then
       if btnr debounce < DEBOUNCE THRESHOLD then
         btnr debounce <= btnr debounce + 1;</pre>
       else
         btnr stable <= '1';
       end if;
    else
       btnr_debounce <= 0;
       btnr stable <= '0';
    end if;
    -- Debounce btnc
    if btnc = '1' then
       if btnc debounce < DEBOUNCE THRESHOLD then
         btnc debounce <= btnc debounce + 1;
       else
         btnc stable <= '1';
       end if;
    else
       btnc debounce \leq 0;
       btnc stable <= '0';
    end if;
  end if;
end process;
-- Counter and Sequence Detection Process
process(slow clk)
  variable temp sequence: SymbolArray; -- Temporary sequence holder
  variable match count : integer := 0; -- Tracks matching symbols
begin
  if rising edge(slow clk) then
    if btnc stable = '1' then
       -- Reset system
       total count \leq 0;
```

```
stop flag \leq 10';
  current index \leq 0;
  entered symbols <= (others => "00");
  sequence detected <= '0';
  led output \leq (others \Rightarrow '0');
elsif sequence detected = '0' then
  -- Count button presses
  if stop flag = '0' then
     if btnu stable = '1' or btnd stable = '1' or btnl stable = '1' or btnr stable = '1' then
       total count <= total count + 1;
     end if;
     -- Stop counting at 11
     if total count = 11 then
       stop flag \leq 11';
     end if;
  end if;
  -- Record button press for sequence detection
  if btnu stable = '1' then
     entered symbols(current index) <= "00";
     current index <= current index + 1;
  elsif btnd stable = '1' then
     entered symbols(current index) <= "01";
     current index <= current index + 1;
  elsif btnl stable = '1' then
     entered symbols(current index) <= "10";
     current index <= current index + 1;
  elsif btnr stable = '1' then
     entered symbols(current index) <= "11";
     current index <= current index + 1;
  end if;
  -- Check for target sequence in any position
  for i in 0 to MAX ATTEMPTS - SEQUENCE LENGTH loop
     match count := 0;
     if entered symbols(i) = "00" then
       match count := match count + 1;
     end if:
     if entered symbols(i + 1) = "01" then
       match count := match count + 1;
     end if;
     if entered symbols(i + 2) = "01" then
       match count := match count + 1;
     end if;
    if entered_symbols(i + 3) = "10" then
       match count := match count + 1;
     end if;
     if entered symbols(i + 4) = "11" then
       match count := match count + 1;
```

```
end if;
             if match count = 5 then
               sequence_detected <= '1';</pre>
               exit;
             end if;
          end loop;
       end if;
       -- Set LED blinking patterns
       if sequence detected = '1' then
          flash_pattern <= (others => flash_clk); -- Blink `111111111` and `00000000`
       elsif stop flag = '1' then
          if flash clk = '1' then
             flash pattern <= "10101010";
          else
             flash_pattern <= "01010101";
          end if;
       else
          flash pattern <= std logic vector(to unsigned(total count, 8)); -- Default to count
       end if;
       led output <= flash pattern;</pre>
     end if;
  end process;
  -- Assign LED output
  led <= led output;</pre>
end Behavioral;
```