CS 061 – Computer Organization — Winter - 2014

Quiz 8 – Friday 2/28 — solution

Construction of an LC-3 instruction (Instruction Register fields):
opcode: [15:12]
Destination register/Source register/condition code test (nzp): [11:9]
Source Register 1/Base Register: [8:6]
Source Register 2: [2:0]
PCoffset9: [8:0] PCoffset11: [10:0] Offset6: [5:0] Imm5: [4:0] trapvec8: [7:0]
Mode flags: [11], [5]

The next two questions refer to the following system:
A certain ISA has a 32-bit word size, uses single word instructions, has 120 opcodes, 32 registers, and 4Gbyte of byte-addressable memory.

One group of instructions in this ISA takes the form:
`OPCODE | DESTINATION REGISTER | SOURCE REGISTER | FLAG | IMMEDIATE VALUE`
Or
`OPCODE | DESTINATION REGISTER | SOURCE REGISTER 1 | FLAG | SOURCE REGISTER 2`
A one-bit flag distinguishes between these two addressing modes.

Another group of instructions takes the form
`OPCODE | SOURCE/DESTINATION REGISTER | PC OFFSET`
Where PC Offset is the 2's complement "distance" from the current PC to the labelled location.

1. What is the range of values that can be stored in the "Immediate" field (as a 2's complement value, to within +/- 1)?
   a. +/- 16 **c.** **+/- 8k** **e.** +/- 32k
   b. +/- 2k **d.** +/-16k **f.** +/- 2M

2. How far (in memory locations) can a labelled location be from an instruction using the PC-relative addressing mode? (to within +/- 1)
   a. +/- 256k **c.** +/- 1M **e.** +/- 4M
   b. **+/- 512k** **d.** +/- 2M **f.** +/- 4G

3. In the ***Direct mode*** of memory addressing in the LC-3 (e.g. the instructions LD and ST), the Effective Address is calculated by:
   a. `(BaseReg) + SEXT(IR[5:0])` **d.** **`(PC) + SEXT(IR[8:0])`**
   b. `(BaseReg) + SEXT(PC[8:0])` **e.** `(IR) + SEXT(PC[5:0])`
   c. `(PC) + SEXT(IR[5:0])` **f.** `(IR) + SEXT(PC[8:0])`

4. Consider the following LC-3 code fragment (the hex values in the first column give the address to which the corresponding instruction is loaded):

```
xB824                   LDI  R3, data_ptr
                          ......
xB875        data_ptr   .FILL   x6000
```

   Given: the LDI opcode is 1010
   What does the instruction at xB824 assemble to (i.e. what is the Machine Language encoding of the instruction)?
   a. xA460 **b.** **xA650** **c.** xA651 **d.** xA350 **e.** xA351
   f. assemble error (no ML translation)

5. How many times is memory accessed in the execution of the LC-3 instruction STI? *(remember to account for the instruction fetch!)*

a. 1 **b.** 2 **c. 3** **d.** 4

6. In the LC-3, the input to the first "arm" of the ALU is always the contents of SR1 (Source Register 1, one of the 8 General Purpose Registers); the second input is ***either*** the contents of SR2 (another GPR) *or*:

a. the contents of a memory location
b. the contents of the "immediate" register
c. the 9-bit offset embedded in the instruction
d. the 5-bit "immediate" value embedded in the instruction
e. the 16-bit word formed from SEXT(IR[4:0])
f. none of the above

7. The SR1 decoder input comes from the SR1MUX. What are two of the inputs to the SR1MUX?

a. `IR[8:6] and IR[11:9]`
b. `[111] and IR[8:6]`
c. `[000] and IR[8:6]`
d. `IR[2:0] and IR[8:6]`
e. `The system bus and IR[8:6]`
f. `(PC) and IR[8:6]`

8. One of the four values of ALUK, the control signal to the LC-3 ALU, instructs the ALU to "pass-through input A" - i.e. input A is connected directly to the output.
Which of the following instruction groups would use this control signal?

a. NOT
b. LD, LDI & LDI
c. ST, STI & STR
d. BR & JMP
e. JSR/JSRR
f. TRAP

9. In the LC-3 data path, the output of the address adder goes to both the MARMUX and the PCMUX, potentially causing two very different register transfers to take place. Why does this not happen?

a. Another multiplexer routes the adder output to the desired target
b. Only one of the two control signals (Marmux.Gate and LD.PC) will be asserted.
c. Only one of the two control signals (MDR.Gate and addressAdder1MUX=select PC) will be asserted
d. Both register transfers actually do take place, but one of them is ignored
e. The MARMUX and the PCMUX can each be caused (via a selector signal) to have no ouput when the other mux is the desired target.

10. How many addressing modes are there in the LC-3 ISA?

a. 2 - immediate and register
b. 3 - direct, indirect, and relative
c. 3 - operations, data movement, and control
d. 3 - immediate, register, and Effective Address
e. 5 - immediate, register, operations, data movement, and control
f. 5 - immediate and register, plus 3 memory addressing modes: direct, indirect, and relative