**CS 061 – Computer Organization** **Winter - 2014**

Quiz 7 – Friday 2/21 solution

1. What data types are implemented natively in the LC-3?
   - **a.** integer, double, character and boolean
   - **b.** **twos complement integer**
   - **c.** twos complement integer and floating point
   - **d.** ASCII and twos complement integer
   - **e.** twos complement integer and Hexadecimal

**For the following four questions:**
An ISA specifies a *word size* of 4 bytes, *byte addressability*, and an *address space* of 16 M; it uses single-word instructions (i.e. each instruction is a single 4 byte word).

2. What is the size of the PC?
   - **a.** 8 bits
   - **b.** 16 bits
   - **c.** **24 bits**
   - **d.** 32 bits
   - **e.** 16 Mbits

3. What is the size of the IR?
   - **a.** 8 bits
   - **b.** 16 bits
   - **c.** 24 bits
   - **d.** **32 bits**
   - **e.** 16 Mbits

4. What is the size of the MAR?
   - **a.** 8 bits
   - **b.** 16 bits
   - **c.** **24 bits**
   - **d.** 32 bits
   - **e.** 16 Mbits

5. What is the size of the MDR?
   - **a.** 8 bits
   - **b.** 16 bits
   - **c.** 24 bits
   - **d.** **32 bits**
   - **e.** 16 Mbits

6. Given that the opcode for the ADD instruction is **0001**, and that the addressing mode flag (bit 5) for the *immediate mode* add instruction is **1**:
   What does the instruction `ADD R6, R5, #-10` assemble to? *(Note the sign!!)*
   - **a.** `x1566`
   - **b.** `x1BBA`
   - **c.** `x1D6A`
   - **d.** **`x1D76`**
   - **e.** `x1BB6`
   - **f.** `x1656`

7. What are the "micro-instructions" that comprise the Fetch phase of the Instruction cycle?
   a. `IR <- (PC); MAR <- (IR); PC <- Mem[(MDR)]; PC <- (PC) + 1;`
   b. `PC <- (MDR) + 1; MAR <- Mem[(PC)]; IR <- (MDR)`
   c. `MAR <- (PC) + 1; MDR <- Mem[(IR)]; IR <- (MAR);`
   d. **`MAR <- (PC); PC <- (PC) + 1; MDR <- Mem[(MAR)]; IR <- (MDR)`**
   e. `MDR <- (PC); PC <- (PC) + 1; MAR <- Mem[(MDR)]; IR <- (PC)`

8. In the ***Relative*** or ***"Base + Offset"*** mode of memory addressing in the LC-3 (e.g. the instructions LDR & STR), the Effective Address is calculated by:
   a. **`(BaseReg) + SEXT(offset6)`**
   b. `Mem[ (BaseReg) + SEXT(offset6) ]`
   c. `(PC) + SEXT(offset6)`
   d. `Mem[ (PC) + SEXT(offset6) ]`
   e. `(IR) + SEXT(offset6)`
   f. `Mem[ (IR) + SEXT(offset6) ]`

9. All control instructions in the LC-3 (e.g. BR, JMP, TRAP, etc.) have one main step in common:
   a. They all write to the IR in the execution phase of the instruction cycle
   b. **They all write to the PC in the execution phase of the instruction cycle**
   c. They all write to the MDR in the execution phase of the instruction cycle
   d. They all write to the GPR bank in the execution phase of the instruction cycle

10. Which of the following is NOT included in a microprocessor's ISA specification?
   a. what are the native data types
   b. which condition codes are set when data is written to register
   c. memory address space
   d. word size
   e. number of instructions in the assembly language
   f. **none of the above *(i.e. all of the above are specified by the ISA)***