

DR <- Mem[BaseReg+SEXT(PCoffset6)]

SR1MUX: IR[8:6]

Select Addr1MUX: SR1 Bus Select Addr2MUX: SEXT(IR[5:0])

MARMUX: Addr. Adder

Gate.MARMUX

LD.MAR

Mem.en /R (wait for ready signal)

LD.MDR Gate.MDR

DRMUX: IR[11:9]

LD.Reg