CS 061 – Computer Organization **Winter - 2014**

Quiz 6 – Friday 2/14 solution

The following questions concern an ISA that has *byte addressable* memory; you also know that the system can perform addition of 16-bit two's complement integers, and it uses 16-bit addressing.

1. What is the address space?
   - **a.** 32
   - **b.** 24k
   - **c. 64k**
   - **d.** 128k
   - **e.** 16M
   - **f.** 256M

2. What is the total memory available?
   - **a. 64 kbytes**
   - **b.** 128 kbytes
   - **c.** 256 kbytes
   - **d.** 16 Mbytes
   - **e.** 64 Mbytes
   - **f.** 256 Mbytes

3. If we were to change the memory design to *word* addressable instead, what would the total memory be?
   - **a.** 64 kbytes
   - **b. 128 kbytes**
   - **c.** 256 kbytes
   - **d.** 16 Mbytes
   - **e.** 64 Mbytes
   - **f.** 256 Mbytes

The next two questions refer to the following scenario:

Consider an elevator that connects the 1st, 2nd, 3rd & 4th floors of a building, able to make "express" rides, e.g. it can.go from the 1st floor to the 3rd or 4th floor without stopping at imtermediate floors (and vice versa).
The controller for this system is an example of a **finite state machine (fsm)**, whose state space consists of the elevator stopped at each of the four floors, with the doors either closed or open (i.e. doors open & doors closed are separate states). The task of the fsm is to control the transitions between all possible states, according to external inputs from button pushes, sensors, etc (which we don't need to worry about here).
To answer the following questions, you will need to sketch the fsm diagram, identifying all possible states and all possible transitions between states. Think carefully about the open- & closed-door states (when can elevator travel?)

4. How many bits would be needed to label all possible states?
   - **a.** 1
   - **b.** 2
   - **c. 3**
   - **d.** 4
   - **e.** 5
   - **f.** 6

5. How many distinct transitions are there between states (*not* including “null transitions”, i.e. transitions back to the current state)?
   - **a.** 4
   - **b.** 6
   - **c.** 8
   - **d.** 12
   - **e. 20**
   - **f.** 24

The following four questions refer to the von Neumann model of computing:

6. The key components of the Processing unit are:
   - **a. the arithmetic & logic unit (ALU) and the register bank**
   - **b.** the ALU and the instruction register
   - **c.** the instruction decoder and the ALU
   - **d.** the memory data register and the program counter
   - **e.** the register bank and the program counter

7. The main purpose of the control unit is:
   a. to store the list of instructions
   b. to fetch the next instruction from memory & decode it
   c. to control the ALU
   d. to control access to memory
   e. to clock the transitions between states of the whole microprocessor

8. The Program Counter is:
   a. a binary counter that keeps track of the number of instructions executed
   b. a register that stores the instruction currently being executed
   c. a control circuit that steps through a sequence of instructions
   d. a register that stores the address of the next memory location to be written to
   e. a register that stores the memory address of the next instruction

9. The Instruction Register is:
   a. a binary counter that keeps track of the number of instructions executed
   b. a register that stores the instruction currently being executed
   c. a control circuit that steps through a sequence of instructions
   d. a register that stores the address of the next memory location to be written to
   e. a register that stores the memory address of the next instruction

10. The purpose of a gate circuit ("tri-state device ") between data "suppliers" and the global bus is:
   a. to prepare the bus to carry the data
   b. to separate the 16 individual bits of data to be carried by the bus
   c. to prevent the contents of the bus being written back to the "supplier" device
   d. to allow a single "supplier" device to control the state of the bus at any one time
   e. to inform the bus regarding the destination of the data