1. Given the instruction (located at address xA400)

   ```
   xA400          LDI  R1,  pointer
   ```
   and given: `pointer` is a label for address `xA460`; memory location `xA460` contains the value `xB000`; memory location `xB000` contains the value `xC000`; and memory location `xC000` contains the value `x00FF`
   What value will `R1` contain after the instruction executes?

   a. `xA400`   **c.** `xB000`   **e.** `x00FF`
   b. `xA460`   **d.** `xC000`

2. Register R3 contains the number xAC4F. Following execution of the instruction
   ```
   NOT R3, R3
   ```
   what does R3 contain?

   a. `x43A0`   **c.** `x53B1`   **e.** `x4DBE`
   b. `x53B0`   **d.** `x5DA1`   **f.** `x53AC`

3. The LC-3 does not have the operation "OR". Which of the following combinations of LC-3 instructions would be the equivalent of
   ```
   OR R3, R1, R2
   ```
   (i.e. bitwise OR the contents of R1 and R2 and store the result into R3)?

   a. `AND R3, R1, R2`
       `NOT R3, R3`
   b. `NOT R1, R1`
       `NOT R2, R2`
       `AND R3, R1, R2`
       `NOT R3, R3`

   c. `NOT R1, R1`
       `ADD R1, R1, #1`
       `ADD R3, R1, R2`
       `NOT R3, R3`
   d. `AND R1, R1, #1`
       `AND R3, R1, R2`
       `NOT R3, R3`

   e. `AND R3, R1, R2`
       `NOT R1, R1`
       `AND R3, R3, R1`
   f. `NOT R1, R1`
       `NOT R2, R2`
       `AND R3, R1, R2`

4. Given that the ASCII codes for 'A' through 'Z' are x41 through x5A; and the codes for 'a' through 'z' are x61 through x7A: which of the following operations would force the character stored in R0 to _lower_ case - i.e. convert a character stored in R0 from _upper_ case into _lower_ case, or _preserve_ the case if it was lower case already.(so 'A' would become 'a', and 'a' would remain unchanged).
   Note: the LC-3 stores ASCII characters in the lower ("right-hand") byte of a 16-bit word, with the upper byte set to zero.

   a. and R0 with x0020   **c.** xor R0 with x0020   **e.** or R0 with x005F
   b. or R0 with x0020   **d.** and R0 with x005F   **f.** and R0 with x004F

5. What is the logic expression corresponding to the following truth table, in the form
Out = f(A, B, C)

A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

a. `Out = A.B + A.C`
b. `Out = A.B' + A.C`
c. `Out = A.B' + B.C`
d. `Out = A.B.C + A'.C`
e. `Out = A.B.C + A'.B'.C'`
f. **`Out = A.B + A.C + B.C`**

6. Simplify the Boolean expression:
    `a.b'.c'.d + a.b'.c.d + a.b.c'.d + a.b.c.d' + a.b.c.d`
   a. `a.b.c + a.b.d + b.c.d`
   b. **`a.d + a.b.c`**
   c. `a.c + a.b.d`
   d. `a.c + b.d + b.c`
   e. can't be simplified

7. How many *select* lines does an 8 data input multiplexer have?
   a. 1   **b. 3**   c. 8   d. 64   e. 256

8. How many *output* lines does an 8 data input multiplexer have?
   a. 1   b. 3   c. 8   d. 64   e. 256

9. How many *inputs* does a full adder have?
   a. 1   b. 2   **c. 3**   d. 4
   e. It depends on the number of bits in the numbers being added

10. What logic circuit would you use for addressing memory?
    a. Full adder   d. Multi-input and gate
    b. Multiplexer   e. Direct Memory Access circuit
    c. Decoder

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