GateMARMUX

MARMUX

GatePC

LD.PC — PC

+1

PCMUX

ZEXT

[7:0]

+

ADDR2MUX

ADDR1MUX

[10:0] SEXT

[8:9] SEXT

[5:0] SEXT

0 SEXT
[4:0]

16

SR2MUX

FINITE STATE MACHINE

R —

CONTROL

ALUK

REG FILE

DR

LD.REG

SR2 OUT   SR1 OUT

SR2   SR1

B   A

ALU

LD.IR — IR

N Z P — LD.CC

LOGIC

GateALU

LD.MDR — MDR   MAR — LD.MAR

MEMORY

INPUT   OUTPUT

MEM.EN, R.W

0010-DR-PCoffset9

DR <— Mem[PC+SEXT(PCoffset9)]

Addr1 Mux:PC
Addr2 Mux: SEXT(IR[8:0])
MARMUX: Addr. Adder
Gate. MARMUX
LD.MAR
Mem.en /R (wait for ready signal)
LD.MDR
Gate.MDR
DRMUX: IR[11:9]
LD.Reg

16