Homework 4

Homework instructions

1. **(1 point)** 3.31

2. **(1 point)** 3.33

3. **(1 point)** 3.35

4. **(7 points)** Construct the Finite State Machine representation for a counter with a cycle length of 4 - i.e a circuit that counts 0 – 1 – 2 – 3 (output as a binary value, obviously) with successive clock pulses, and then starts over.
The ***external output*** is the 2-bit count.
The only ***external input*** is R, a reset pulse: when R = 1 it resets the next count to 0, no matter what the current state (count); when R = 0 it does nothing (i.e. it allows the FSM to transition to the next state in sequence).

   Then construct the complete truth table for the device, showing
   the inputs: "current state" labels, and R
   the outputs: "next state" labels, and the 2-bit count
   (Hint: if you choose the state labels sensibly, they will be the same as the output)

   Finally, derive and simplify the algebraic expression for bit 0 of the output.