1011-SR-PCoffset9

GateMARMUX

GatePC

MARMUX

LD.PC → PC

+1

ZEXT

PCMUX

[7:0]

ADDR2MUX

ADDR1MUX

+

[10:0] SEXT

[8:0] SEXT

[5:0] SEXT

0

SEXT

[4:0]

FINITE STATE MACHINE

R →

CONTROL

SR2MUX

ALUK

ALU

B   A

LD.IR → IR

N Z P ← LD.CC

LOGIC

GateALU

REG FILE

DR

LD.REG

SR2

SR1

SR2 OUT   SR1 OUT   SR1

LD.MDR → MDR

MAR ← LD.MAR

MEMORY

INPUT

OUTPUT

MEM.EN, R.W

Mem[Mem[PC + SEXT(IR[8:0])]] <— SR

ADDR1MUX: PC
ADDR2MUX: SEXT(IR[8:0])
Marmux: Addr. Adder
Gate.Marmux
Ld.Mar
Mem.En /R (wait for ready signal)
LD. MDR
Gate.MDR
LD.MAR
SR1MUX Selects IR[11:9]
ALUK: pass through
Gate.ALU
LD.MDR
Mem.En /W

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