CS 061 – Computer Organization — Winter - 2014

Quiz 9 – Friday 3/7 — solution

Construction of an LC-3 instruction (Instruction Register fields):
opcode: [15:12]
Destination register/Source register/condition code test (nzp): [11:9]
Source Register 1/Base Register: [8:6]
Source Register 2: [2:0]
PCoffset9: [8:0] PCoffset11: [10:0] Offset6: [5:0] Imm5: [4:0] trapvec8: [7:0]
Mode flags: [11], [5]

1. Consider the following LC-3 code fragment (the hex values in the first column give the address to which the corresponding instruction or label is loaded):

```
x3025        loop1     ADD  R4, R5, R6
                       .....
x30EB                  BRn loop1
```

Given that the BR opcode is **b0000**, what does the instruction at x30EB assemble to? *(Note the direction of the branch!)*

a. **x0939** **c.** x093B **e.** x0B3A
b. x093A **d.** x0B39 **f.** x0B3B

2. What is the Register Transfer description of the LC-3 instruction JSR?

a. `R7 <- (PC); PC <- (BaseReg)` *(where BaseReg is IR[8:6])*
b. `R7 <- (PC); PC <- Mem[ (BaseReg) ]`
c. `R7 <- (PC); PC <- (PC) + SEXT(IR[8:0])`
d. `R7 <- (PC); PC <- Mem[ (PC) + SEXT(IR[8:0]) ]`
e. **`R7 <- (PC); PC <- (PC) + SEXT(IR[10:0])`**
f. `R7 <- (PC); PC <- Mem[ (PC) + SEXT(IR[10:0]) ]`

3. What is the Register Transfer description of the LC-3 instruction JSRR?

a. **`R7 <- (PC); PC <- (BaseReg)`** ***(where BaseReg is IR[8:6])***
b. `R7 <- (PC); PC <- Mem[ (BaseReg) ]`
c. `R7 <- (PC); PC <- (PC) + SEXT(IR[8:0])`
d. `R7 <- (PC); PC <- Mem[ (PC) + SEXT(IR[8:0]) ]`
e. `R7 <- (PC); PC <- (PC) + SEXT(IR[10:0])`
f. `R7 <- (PC); PC <- Mem[ (PC) + SEXT(IR[10:0]) ]`

4. The DR decoder input comes from the DRMUX. What are two of the inputs to the DRMUX? *(Hint: think about the JSR/R and TRAP instructions)*

a. `IR[8:6] and IR[11:9]` **d.** `IR[2:0] and IR[11:9]`
b. **`[111] and IR[11:9]`** **e.** `The system bus and IR[11:9]`
c. `[000] and IR[11:9]` **f.** `(PC) and IR[11:9]`

5. In the LC-3 (and most ISAs), the System Control Block, or Trap Vector Table, contains

a. the Trap Service Routines
b. the 9-bit PC offsets of the Trap Service Routine addresses
c. the 8-bit Trap Vector
d. **the starting addresses of the Trap Service Routines**
e. the return addresses to be used after returning from a Trap Service Routine

6. What does the LC-3 pseudo-op `.EXTERNAL` do?
   a. It invokes an external compiler – e.g. for handling embedded code written in a different programming language like C++
   b. It invokes an external subroutine – e.g. a pre-assembled library
   c. It allows external data to be input at run-time
   d. It allows a library to be dynamically linked, rather than statically linked
   e. It will cause the program to be suspended while waiting for an external input.
   f. **It defers resolution of a label to link time**

7. The purpose of the linker program is:
   a. **To produce a single executable file from multiple object files**
   b. To produce a single object file from multiple source files
   c. To implement pseudo-ops in the source file
   d. to build a symbol table relating labels to memory addresses

8. What is the main purpose of the first pass of a two-pass assembler?
   a. to determine if the code will fit into available memory
   b. to produce the machine language equivalent of the assembly language instructions
   c. to link other possible object files in order to create the executable
   d. to remove all pseudo-ops from the code before it is assembled
   e. **to build a symbol table relating labels to memory addresses**

9. What problem could occur if the *keyboard hardware* did not check the KBSR before writing a new ASCII code to the KBDR?
   a. none: the KBSR is read by the cpu only
   b. the cpu might read the same character multiple times
   c. **a character in the KBDR might be overwritten before the cpu has read it**
   d. the keyboard might explode into a million fragments

10. Memory mapping of ports is achieved by:
   a. A BIOS routine (i.e. software) that checks for the mapped address and re-routes the data to the register.
   b. The register is directly connected to the memory circuit decoder output of the mapped address.
   c. **An Address Control Logic circuit decodes the requested address and determines whether the main memory or the register is to be enabled.**
   d. A separate address bus carries the address to the external registers.