CS 061 – Computer Organization **Winter - 2014**

Quiz 5 – Friday 2/7 solution

1. Given that the ASCII codes for 'A' through 'Z' are x41 through x5A; and the codes for 'a' through 'z' are x61 through x7A: which of the following operations would force the character stored in R0 to *upper* case - i.e. convert a character stored in R0 from *lower* case into *upper* case, or *preserve* the case if it was upper case already (so 'a' would become 'A', and 'A' would remain unchanged).
   Note: the LC-3 stores ASCII characters in the lower ("right-hand") byte of a 16-bit word, with the upper byte set to zero.
   a. and R0 with x0020 **c.** xor R0 with x0020 **e.** or R0 with x005F
   b. or R0 with x0020 **d. and R0 with x005F** **f.** and R0 with x004F

2. A "gate delay" can be described as the time needed for the output of a gate to settle to its correct level after one of its inputs has been changed. The full-adder circuit we have designed would therefore result in a gate delay of 2 units.
   How many units of gate delay would a 16-bit ripple-carry adder display?
   a. 2 **b.** 4 **c.** 8 **d.** 16 **e. 32**

3. In order to overcome the gate delay problem of the simple ripple-carry adder circuit, we can design an adder with the following design improvement:
   a. Make each full-adder smaller so as to reduce the gate delay of each.
   b. Pre-calculate the carry bit for each digit.
   c. Add an n-bit register to hold intermediate results, where n is the number of digits being added.
   d. Use a multiplexer to distribute the carry bits to subsequent columns

4. What is the design element that differentiates a circuit like the R-S latch from a combinational circuit such as a multiplexer?
   Specifically, what is it that makes the R-S latch bistable?
   a. the use of NAND gates rather than AND gates
   b. the use of two complementary outputs, Q and Q'
   c. the use of mutual feedback between the gates
   d. the lack of any OR gates.
   e. the use of a clock signal

5. What is the advantage of a gated-d latch over an RS latch?
   a. it enables the use of a single input for the data bit
   b. it allows a control signal to determine the instant at which the data input is sampled
   c. it prevents the R and S lines from transitioning to 0 simultaneously.
   d. all of the above.

6. How do we turn 8 separate gated D-latches into a single 8-bit register?
   a. connect their inputs together
   b. connect their outputs together
   c. connect them to an 8-bit bus
   d. connect their Write-Enable lines together
   e. super-glue them together

7. You are given a box of **4k by 4-bit** memory chips, and asked to construct from them a 128k by 1-byte memory module, utilising the Chip Select (CS) input on each of the chips. This will require "two levels" of addressing -- i.e. a portion of the address will be input to the address pins of the individual chips, and a portion will be input to a module-level decoder driving the chips' CS pins. How many bits will be input to this module-level decoder?

a. 2 **b.** 3 **c.** 4 **d. 5** **e.** 6 **f.** 8

The following questions concern an ISA that has *byte addressable* memory; you also know that the system can perform addition of 32-bit two's complement integers, and it uses 24-bit addressing.

8. What is the address space?

a. 32
b. 24k
c. 64k
d. 16M
e. 256M
f. 4G

9. What is the total memory available?

a. 64 kbytes
b. 256 kbytes
c. 16 Mbytes
d. 64 Mbytes
e. 256 Mbytes
f. 4 Gbytes

10. If we were to change the memory design to *word* addressable instead, what would the total memory be?

a. 64 kbytes
b. 256 kbytes
c. 16 Mbytes
d. 64 Mbytes
e. 256 Mbytes
f. 4 Gbytes