

DR <— SR1 AND SR2 DR <— SR1 AND SEXT(imm5) 0101-DR-SR1-0-00-SR2 0101-DR-SR1-1-imm5

SR1.MUX: IR[8:6] SR2.MUX: IR[2:0]

ALUK: AND Gate.ALU

DR.MUX: IR[11:9]

LD.Reg