CS 061 – Computer Organization **Winter - 2014**

Quiz 10 – Friday 3/14 solution

1. Consider the following LC-3 code fragment (the hex values in the first column give the address to which the corresponding instruction is loaded):

```
x3217        loop1     ADD  R4, R5, R6
                       .....
x32FC                  BRzp loop1
```

Given: the BR opcode is 0000, and the nzp tests are set by bits [11:9]
What does the instruction at x32FC assemble to (i.e. what is the Machine Language encoding of the instruction `BRzp loop1`)?

a. `x06E4`
b. `x06E6`
c. **`x071A`**
d. `x071B`
e. `x071C`
f. assemble error

2. What is the Register Transfer description of the LC-3 instruction JSR?
   a. `R7 <- (PC); PC <- (BaseReg)` *(where BaseReg is IR[8:6])*
   b. `R7 <- (PC); PC <- Mem[ (BaseReg) ]`
   c. `R7 <- (PC); PC <- (PC) + SEXT(IR[8:0])`
   d. `R7 <- (PC); PC <- Mem[ (PC) + SEXT(IR[8:0]) ]`
   e. **`R7 <- (PC); PC <- (PC) + SEXT(IR[10:0])`**
   f. `R7 <- (PC); PC <- Mem[ (PC) + SEXT(IR[10:0]) ]`

3. What component of the cpu gets "interrupted" by an Interrupt signal? (i.e. where does the Interrupt signal go to?)
   a. The PC
   b. The PC-MUX
   c. The MAR-MUX
   d. The global bus
   e. **The FSM**
   f. The Memory Mapping logic

4. What is the purpose of the IACK signal in processing an interrupt?:
   a. It forces the CPU to alter the control sequence to acknowledge the interrupt
   b. **It interrogates the peripheral devices to find out which set the interrupt**
   c. It contains the interrupt vector
   d. It is the response of the peripheral device after the interrupt is acknowledged
   e. None of the above

5. When an Interrupt is accepted, current state information has to be saved by pushing it on a stack. Why is a stack used rather than simply saving it to a fixed location in RAM?
   a. Multiple memory reads are very time-consuming: pushing to a stack is quicker
   b. **To allow for the possibility of nested Interrupts**
   c. To allow the cpu to differentiate between routines with Supervisor privilege and User privilege
   d. Saving the state information to memory would interfere with the process of loading the Interrupt Service Routine from memory
   e. There are no major differences between the two approaches – it is just a minor design decision.

6. What system state information has to be saved before an interrupt-enabled LC-3 can proceed with servicing an interrupt?
   - **a.** the value of every control signal produced by the finite state machine
   - **b.** the value of every control signal produced by the finite state machine, plus the contents of all Registers (GPRs, PC, condition codes, etc.) – except the IR
   - **c.** the PC
   - **d.** the PC and all the General Purpose Registers
   - **e.** **the PC, and the PSR (Processor Status Register, containing the NZP condition codes, the Privilege level, and the current task priority)**
   - **f.** the PC and the MCR (Machine Control Register)

7. In the LC-3, the TRAP instruction and the interrupt handler both manage the invocation of service routines in a similar fashion. Specifically, both use:
   - **a.** polling of status registers to decide when to read from/write to a port
   - **b.** **a trap/interrupt vector as an entry point into a table of service routine addresses**
   - **c.** an IACK signal to determine which service routine is requested
   - **d.** a stack to store information required for the return, allowing nested calls
   - **e.** a system of task priority comparisons to determine whether to invoke the service routine

8. The two main approaches to converting a HLL (Higher Level Language) source code to ML (Machine Language) are:
   - **a.** direct and indirect
   - **b.** memory mapping and polling
   - **c.** assembly and disassembly
   - **d.** **interpreting and compiling**
   - **e.** compiling and linking

9. The structure which allows Higher Level Languages to make nested function calls is:
   - **a.** **Activation records stored on the run-time stack**
   - **b.** The symbol table
   - **c.** The frame pointer
   - **d.** The Processor Status Register
   - **e.** The Machine Control Register

10. One component of a function's activation record is a "frame". What information is stored in the frame?
   - **a.** **a function's local variables**
   - **b.** the function arguments
   - **c.** the dynamic link
   - **d.** the function instructions
   - **e.** the function symbol table
   - **f.** "frame" is just another name for the activation record itself