3.3.1 Cache levels and memory structure

The z14 ZR1 memory subsystem focuses on keeping data “closer” to the PU core. With the current processor configuration, all on chip cache levels increased.

Although L1, L2, and L3 caches are implemented on the PU SCM, the fourth cache level (L4) is implemented within the system controller (SC) SCM. One L4 cache is present in each CPC drawer, which is shared by all PU SCMs. The cache structure of the z14 ZR1 has the following characteristics:

- Larger L1, L2, and L3 caches (more data closer to the core).
- L1 and L2 caches use eDRAM, and are private for each PU core.
- L2-L3 interface has a new *Fetch cancel* protocol, a revised L2 *Least Recent Used* (LRU) demote handling.
- L3 cache also uses eDRAM and is shared by all activated cores within the PU chip. The CPC drawer has up to four L3 caches, depending on CPC drawer feature. Therefore, a Max24 and Max30 CPC drawer feature four L3 caches, which results in 512 MB (4 x 128 MB) of this shared PU chip-level cache. For availability and reliability, L3 cache now implements symbol ECC.
- L4 cache also uses eDRAM, and is shared by all PU chips. L4 cache has 672 MB inclusive of L3’s, 42w Set Associative and 256 bytes cache line size.

  In most real-world situations, several cache lines exist in multiple L3s underneath L4. The L4 does not contain the same line multiple times, but rather once with an indication of all the cores that have a copy of that line. As such, 672 MB of inclusive L4 can easily cover 512 MB of underlying L3 caches.
- Main storage has up to 8 TB addressable memory in the CPC drawer, which uses 20 DIMMs.

Considerations

Cache sizes are limited by ever-diminishing cycle times because they must respond quickly without creating bottlenecks. Access to large caches costs more cycles. Instruction and data cache (L1) sizes must be limited because larger distances must be traveled to reach long cache lines. This L1 access time generally occurs in one cycle, which prevents increased latency.