Weigh the benefits of whether something in this category must use large pages as a result of the system-level costs of tying up real storage. A balance exists between the performance of a process that uses large pages and the performance of the remaining work on the system.

On z14 ZR1 servers, 1 MB large pages become pageable if Virtual Flash Memory[5] is available and enabled. They are available only for 64-bit virtual private storage, such as virtual memory that is greater than 2 GB.

It is easy to assume that increasing the TLB size is a feasible option to deal with TLB-miss situations. However, this process is not as straightforward as it seems. As the size of the TLB increases, so does the processor usage that is involved in managing the TLB's contents. Correct sizing of the TLB is subject to complex statistical modeling to find the optimal tradeoff between size and performance.

3.6.2 Main storage

Main storage is addressable by programs and storage that is not directly addressable by programs. Non-addressable storage includes the hardware system area (HSA).

Main storage provides the following functions:

- Data storage and retrieval for PUs and I/O
- Communication with PUs and I/O
- Communication with and control of optional expanded storage
- Error checking and correction

Main storage can be accessed by all processors, but cannot be shared between LPARs. Any system image (LPAR) must include a defined main storage size. This defined main storage is allocated exclusively to the LPAR during partition activation.

3.6.3 Hardware system area

The HSA is a reserved storage area that contains system LIC and configuration-dependent control blocks. On z14 ZR1 servers, the HSA has a fixed size of 64 GB and is not part of the client purchased memory.

The fixed size of the HSA eliminates planning for future expansion of the HSA because the hardware configuration definition (HCD) and input/output configuration program (IOCP) always reserves space for the following items:

- Three channel subsystems (CSSs)
- A total of 15 LPARs in the first two CSSs and 10 LPARs for the third CSS for a total of 40 LPARs per system
- Subchannel set 0 with 63.75-K devices in each CSS
- Subchannel set 1 with 64-K devices in each CSS
- Subchannel set 2 with 64-K devices in each CSS

The HSA includes sufficient reserved space to allow for dynamic I/O reconfiguration changes to the maximum capability of the processor.

[5] Virtual Flash Memory replaced IBM zFlash Express for z14. No carry forward of zFlash Express exists.