usual memory controller[29]. In contrast, S-class SCM, SSD, and HDD would all be accessed through an I/O controller for asynchronous access. M-class SCM would likely not be as fast as main memory DRAM. But by being non-volatile, lower in power-per-unit-capacity (via high density), and lower in cost-per-capacity, the presence of M-class SCM could potentially allow the total amount of DRAM required to maintain ultra-high bandwidth to be greatly reduced, thus reducing overall system cost and power.

II. PHYSICS OF PCM

A. Phase change materials and scalability

As discussed in Section I, the NVM industry faces the prospect of a costly and risky switch from a known and established technology (Flash) into something much less well known (either PCM or something else). And understandably, the industry wants to make such leaps rare.

The problem here is not that one might fail to create a successful first product. That would be unpleasant but not devastating, because this would happen during the early development stage, where the level of investment is small and multiple alternative approaches are still being pursued. Instead, the nightmare scaling scenario is one in which the new technology works perfectly well for the first generation, yet is doomed to failure immediately afterwards. If only one or two device generations succeed, then the NVM industry, having just invested heavily into this new technology, will be forced to make yet another switch and start the learning process all over again.

Thus scaling studies are designed to look far down the device roadmap, to try to uncover the showstoppers that might bedevil a potential NVM technology at sizes much smaller than what can be built today. In the case of PCM technology, two aspects of scalability need to be considered: the scaling properties of the phase change materials, and the scaling properties of PCM devices. In this Section, we survey recent literature covering both of these considerations. In general, experiments have shown that PCM is a very promising technology with respect to scalability.

It is well known that the properties of nanoscale materials can deviate from those of the bulk material, and can furthermore be a strong function of size. For example, it is typical for nanoparticles to have a lower melting temperature than bulk material of the same chemical composition, because the ratio of surface-atoms to volume-atoms is greatly increased. A recurring theme in such studies is the larger role that surfaces and interfaces play as dimensions are reduced.

Phase change material parameters that are significant for PCM applications—and the device performance properties that are influenced by these parameters—are summarized in Table I. For optical applications the change of optical constants as a function of film thickness is also important, but for this paper we restrict our considerations to material parameters relevant to electronic memory applications. As can be seen from Table I, there is a large set of materials parameters which influence the PCM device, either affecting one of the two writing operations (SET to low resistance; RESET to high resistance) or the read operation.

A particularly important phase change material parameter is the crystallization temperature, T_x. This is not necessarily the temperature at which crystallization is most likely, but instead is the lowest temperature at which the crystallization process becomes "fast." It is typically measured by raising the temperature slowly while monitoring the crystallinity (either looking for X-ray diffraction from the crystalline lattice or the associated large drop in resistivity). Thus the crystallization temperature is a good measure of how hot a PCM cell in the RESET state could be made before the data stored by an amorphous plug would be lost rapidly due to unwanted crystallization. While the crystallization temperature by itself does not reveal how "slowly" such data would be lost for slightly lower or much lower temperatures, it sets a definitive and easily measured upper bound on the retention vs. temperature curve for a new phase change material.

The crystallization temperature of phase change materials tends to vary considerably as a function of material composition[62–64]. For example, some materials, such as pure Sb, crystallize *below* room temperature. Yet adding only a few at. % of Ge to Sb, creating the phase change material Ge_x-Sb_{1-x}, increases the crystallization temperature significantly above room temperature. In fact, T_x can reach almost 500°C for GeSb alloys that are high in Ge content[63, 64]. Studies of the crystallization temperature as a function of film thickness show an exponential increase as film thickness is reduced (for phase change materials sandwiched between insulating materials such as SiO_2 or ZnS-SiO_2)[65, 66]. However, for phase change materials sandwiched between metals, metal-induced crystallization can occur and the crystallization temperature can be reduced for thinner films[67]. It is known that for phase change materials the crystallization is typically heterogeneous, starting at defects which can be located in the bulk, but which tend to be more prevalent at surfaces and interfaces. As film thickness is reduced, the volume-fraction of phase change material that is at or near an interface increases, leading to changes in the externally observable crystallization temperature.

Phase change nanowires are typically fabricated by the vapor-liquid-solid technique, and are crystalline as synthesized[68]. To measure crystallization behavior as a function of wire size, PCM devices were fabricated from single-crystalline, as-grown $Ge_2Sb_2Te_5$ nanowires using Pt contact pads[68]. The central section of the nanowire devices was re-amorphized by electrical current pulses and the activation energy was determined by measuring the recrystallization temperature as a function of heating