Based on IBM benchmarks, the throughput for each On-Chip Compression unit is 12 GBps, which equates to 48 GBps per drawer or 240 GBps for a fully populated five-drawer z15.

On-Chip Compression provides an up to 5% improvement in compression ratios for BSAM/VSAM datasets over zEDC while maintaining full compatibility.

Eliminating adapter sharing by using Nest Compression Accelerator

Sharing of zEDC cards is limited to 15 LPAR guests per adaptor. The Nest Compression Accelerator removes this virtualization constraint because it is shared by all PUs on the processor chip and therefore is available to all LPARs and guests.

Moving the compression function from the (PCIe) I/O drawer to the processor chip means that compression can operate directly in L3 cache and data does not need to be passed by using I/O operations.

Compression modes

Compression is run in one of the following modes:

► Synchronous

Execution occurs in problem state where the user application starts the instruction in its virtual address space.

► Asynchronous

Execution is optimized for Large Operations under z/OS for authorized applications (for example, BSAM) and issues I/O by using EADMF for asynchronous execution.

This type of execution maintains the current user experience and provides a transparent implementation for authorized users of zEDC.

Note: The zEDC Express feature does *not* carry forward to z15.

z15 migration considerations

The IBM Integrated Accelerator for zEDC is fully compatible with zEDC. Data compressed by zEDC can be read by z15 (the on-chip) nest accelerator unit and vice versa.

All z/OS configuration stay the same

No changes are required when moving from earlier systems using zEDC to z15.

The IFAPRDxx feature is still required for authorized services. For problem state services, such as zlib usage of Java, it is not required.

Consider fail-over and DR sizing

The order of magnitude throughput increase on z15 means that the throughput requirements need to be considered whether failing over to earlier systems with zEDC.