Each core on the PU SCM includes an enhanced dedicated coprocessor for data compression and cryptographic functions, which are known as the Central Processor Assist for Cryptographic Functions (CPACF)[11]. Having standard clear key cryptographic coprocessors that are integrated with the processor provides high-speed cryptography for protecting data.

The z15 supports 64-bit addressing mode and uses Complex Instruction Set Computer (CISC), including highly capable and thus complex instructions. Most of the instructions are implemented at the hardware or firmware level for most optimal and effective execution.

Each PU is a superscalar processor, which can decode up to six complex instructions per clock cycle, running instructions out-of-order. The PU uses a high-frequency, low-latency pipeline that provides robust performance across a wide range of workloads.

z/Architecture addressing modes: The z/Architecture simultaneously supports 24-bit, 31-bit, and 64-bit addressing modes. This feature provides compatibility with earlier versions and with that compatibility, investment protection.

Compared to its predecessor, the z15 processor design includes the following improvements and architectural extensions:

- Better performance and throughput:
  - Fast processor units with enhanced microarchitecture
  - Larger L2, L3 caches
  - Up to 12 cores per processor chip
  - More capacity (up to 190 characterizable processor units versus 170 on the z14)
  - Larger cache (and shorter path to cache) means faster uniprocessor performance
  - Innovative core-cache design (L1 and L2 private to the processor core), processor chip-cache design (L3), and processor node design (L4), with focus on keeping more data closer to the processor, increasing the cache sizes, and decreasing the latency to access the next levels of cache.

    This on-chip cache implementation optimizes system performance for high-frequency processors, with cache improvements, new Translation/TLB2 design, pipeline optimizations, better branch prediction, new accelerators, and architecture support.
- Reoptimized design for power and performance:
  - Improved instruction delivery
  - Improved branch prediction
  - Reduced execution latency
  - Optimized third-generation SMT
  - Enhanced out-of-order execution
  - New and enhanced vector instructions
- Dedicated co-processor for each processor unit (PU):
  - The Central Processor Assist for Cryptographic Function (CPACF) is well-suited for encrypting large amounts of data in real time because of its proximity to the processor unit.

[11] Feature code (FC) 3863 must be ordered to enable CPACF. This feature code is available for no extra fee.