USB72x6/USB7252

USB72x6/USB7252 Silicon Errata and Data Sheet Clarification

This document describes known silicon errata for the following USB72x6/USB7252 devices:

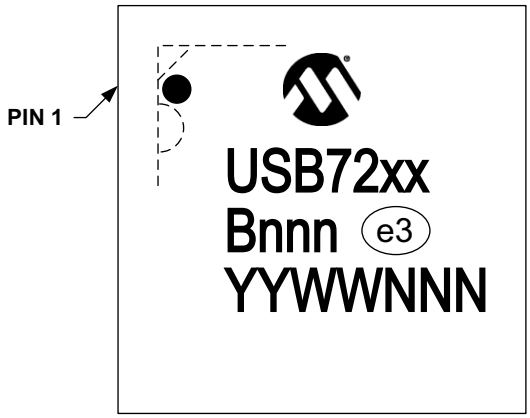
- USB7206
- USB7216
- USB7252

The silicon errata discussed in this document are for silicon with silicon revisions as listed in Table 1. Parts affected by these errata are marked in Figure 1.

TABLE 1: AFFECTED SILICON REVISIONS

Part Numbers	Silicon Revision
USB7206, USB7216, USB7252	B1

FIGURE 1: TOP MARKING SILICON REVISION INDICATION



Note: Figure 1 details the top markings of an example part and highlights the location of the silicon revision. Other top marking values may differ (lot codes, location of manufacture, and so on).

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A summary of USB72x6/USB7252 silicon errata is provided in Table 2.

TABLE 2: SILICON ISSUE SUMMARY

Item Number	Silicon Issue Summary
1.	FlexConnect USB 3.0 operation requires special conditions
2.	Type-C Bridging
3.	Type-C VBUS discharge in Port Power On/Off test
4.	I^2C Bridge sends an extra byte under certain conditions
5.	PF29 cannot be initialized by configuration OTP
6.	Clock Data Recovery Block Power-On Failures for Small Subset of Devices at USB3.x Gen 1 speeds

Silicon Errata Issues

Module 1: FlexConnect USB 3.0 operation requires special conditions

DESCRIPTION

FlexConnect: For USB 3.0 connections only, the following conditions exist:

- The Flexed port may not re-enumerate if disconnected and reconnected.
- After flexing and unflexing, the UFP may not re-enumerate.

These conditions are avoided if both of the following steps are taken:

1. Run the hub using SPI Flash memory.
2. Disable the host (PC) power management.

Note: USB 2.0 connections enumerate normally in all FlexConnect states.

END USER IMPLICATIONS

If FlexConnect operation is required for USB 3.0 connections, both of the following must be met:

- The hub must operate using SPI Flash memory.
- Host power management must be disabled.

Work around

None.

PLAN

This erratum will be corrected in a future revision of this silicon.

Module 2: Type-C Bridging

DESCRIPTION

The internal Type-C Bridge device is not implemented for USB7216 and USB7252 devices with only basic Type-C ports.

END USER IMPLICATIONS

There is no end user impact as long as USB 3 Hub Command Verifier (HUB3CV) Ver. 2.1.12.1 or later is used; with this version, a missing Type-C Bridge device will not result in a compliance test failure.

Work around

None.

PLAN

This erratum will be corrected in a future revision of this silicon.

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Module 3: Type-C VBUS discharge in Port Power On/Off test

DESCRIPTION

One requirement for USB-IF compliance certification of a system with an exposed Type-C port is the *Port Power On/Off* test. This test is part of the HUBCV suite of *Command Verification* tests for USB 2 devices. As part of this test, the hub must discharge VBUS, and then energize VBUS in response to CLEAR_FEATURE and SET_FEATURE commands from the test host.

Frequently, these ports will be implemented with electrolytic VBUS load capacitors, which retain a small residual charge that is released slowly compared to the timing of the discharge. In such cases, as energy is released from the capacitor the voltage can drift upward slightly after the discharge, which can cross the VBUS_DET threshold for detecting VBUS high. In the sequence of the Port Power On/Off test, this can inhibit subsequent turning on of VBUS in response to commands from the test host and the test fails.

This issue does not impact normal operation of the port. Only the Port Power On/Off test is affected.

END USER IMPLICATIONS

Type C ports that have a large electrolytic capacitor may require this workaround to pass the HUBCV Port Power On/Off test.

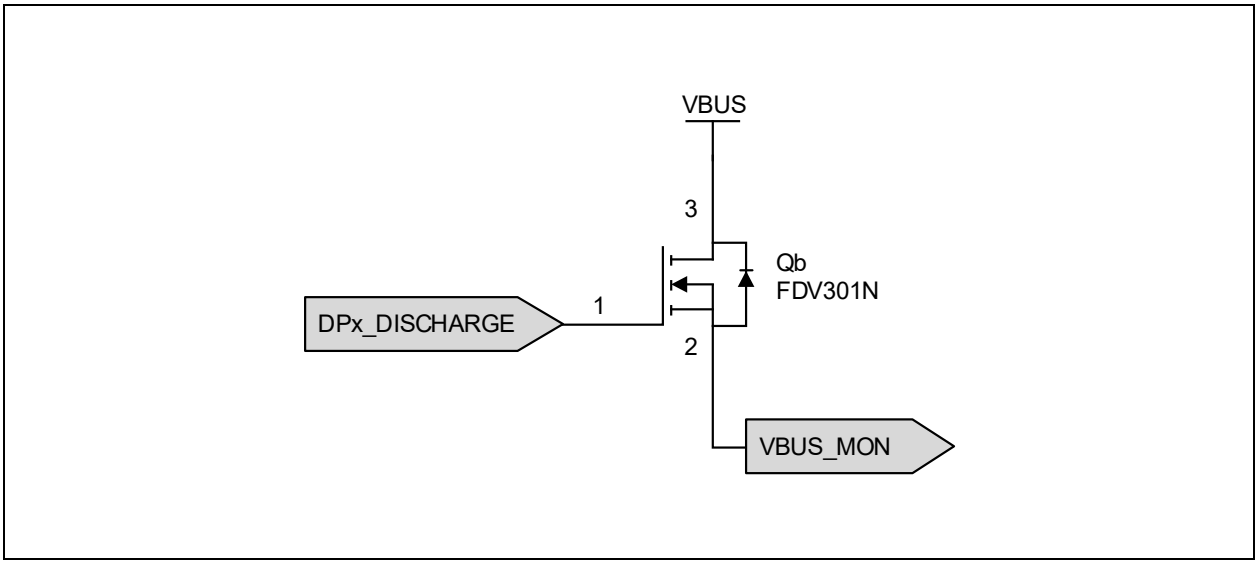
Applications that do not perform HUBCV testing are not affected.

Work around

In reference designs for USB7216 and USB7252 devices, an N-channel MOSFET with a V_{GS} less than 1.0V is connected between VBUS and VBUS_MON, with gate control from the DISCHARGE signal. This additional component creates an additional current path as the discharge is monitored by VBUS_MON, which biases VBUS_MON higher. This results in discharge to a lower voltage than what is otherwise achieved, and compensates for any residual energy that the capacitor releases after the discharge. At times other than the discharge, the MOSFET is turned off and does not influence VBUS.

No components of the reference design need to be removed; only the MOSFET is added.

FIGURE 2: TYPE-C DISCHARGE WORKAROUND FOR MODULE 3



PLAN

There is no plan to correct this erratum.

Module 4: I²C Bridge sends an extra byte under certain conditions

DESCRIPTION

USB7252 is an I²C master that is connected to an I²C slave. In the case where a single byte is to be read, the I²C Bridge responds by reading two bytes. The first of these bytes has an ACK bit, and the second byte has a NACK bit. Only the first byte contains correct data, and the value of the second byte is unpredictable. Only the valid byte is returned to the application or the I²C Read Buffer.

This phenomenon is also seen in cases where the number of bytes to be read is equal to a multiple of 128 plus 1 (for example, 129 bytes, 257 bytes, and so on).

Note: This module applies to all USB7206, USB7216, and USB7252 devices Revision B1.

END USER IMPLICATIONS

I²C slaves may not expect the second byte. The I²C slave software may interpret the incorrect byte as valid, and may malfunction.

Work around

The I²C master software should avoid reading a single byte. When only one byte is desired, the I²C master software should read two bytes and discard the second byte.

PLAN

1. An OTP patch is available that corrects the error in the case of reading one byte. It does not correct the other cases (129 bytes, 257 bytes, and so on).
2. In Revision C0 of the part, the error will be corrected in the hardware.

Module 5: PF29 cannot be initialized by configuration OTP

DESCRIPTION

After reset, PF29 is initialized to these conditions:

- Output is enabled
- Input is enabled
- Output value is High (1)
- Pull-up is enabled
- Open-drain is enabled

These initial conditions cannot be altered by means of writing to the GPIO control registers from configuration OTP.

After initialization is complete (that is, in runtime), the value of the GPIO registers can be altered in the normal manner: through USB host control or through SMBus control.

END USER IMPLICATIONS

If the initial state of PF29 is unacceptable, then a different GPIO pin must be used.

If the initial state of PF29 is not a concern, then PF29 can be used.

Work around

None.

PLAN

The error will be corrected in Revision C0.

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Module 6: Clock Data Recovery Block Power-On Failures for Small Subset of Devices at USB3.x Gen 1 speeds

DESCRIPTION

On a small subset of devices, the clock data recovery block within one or more USB3.2 PHYs may not properly power on when operating at USB3.x Gen 1 (5GHz) speeds.

This failure does not occur when operating at USB3.x Gen 2 (10GHz) or USB2.0-only speeds.

END USER IMPLICATIONS

Devices affected with this errata may fail to connect at USB3.x Gen 1 speeds on the affected port, which may be the upstream port or any of the downstream ports.

Work around

This workaround may be applied universally to all commercial-grade devices to guard against this failure. The following register settings elevate the internal voltage supply to the clock data recovery block. The registers may be modified via 1 of 3 options:

OTP Memory: Programmed permanently at the time of production or in the field through USB or SMBus.

SMBus interface: Set after every power-on/reset.

External SPI Memory: “Pseudo-OTP” memory space when executing firmware and configuration from external SPI memory.

USB3.2 PHY0 (UFP) Register Settings:

0xBF80_6082 = 0x02

0xBF80_6083 = 0x5F

0xBF80_6086 = 0x04

USB3.2 PHY1 Register Settings:

0xBF80_6482 = 0x02

0xBF80_6483 = 0x5F

0xBF80_6486 = 0x04

USB3.2 PHY2 Register Settings:

0xBF80_6882 = 0x02

0xBF80_6883 = 0x5F

0xBF80_6886 = 0x04

USB3.2 PHY3 Register Settings:

0xBF80_6C82 = 0x02

0xBF80_6C83 = 0x5F

0xBF80_6C86 = 0x04

USB3.2 PHY4 Register Settings:

0xBF80_7082 = 0x02

0xBF80_7083 = 0x5F

0xBF80_7086 = 0x04

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USB3.2 PHY5 Register Settings:

0xBF80_7482 = 0x02

0xBF80_7483 = 0x5F

0xBF80_7486 = 0x04

Global Settings (must be applied after the USB Attach Command with SMBus Active [0xAA 0x56] is issued if configuring via SMBus):

0xBF80_6019 = 0x1F

PLAN

Commercial-grade B1 Revision Silicon: The register-based workaround will be included in all B1 silicon devices moving forward. The fix can be verified by checking the bcdDevice descriptor of the hub:

- USB7206 devices with bcdDevice = 0x0612 or higher
- USB7216 devices with bcdDevice = 0x0613 or higher
- USB7252 devices with bcdDevice = 0x0614 or higher

Commercial-grade C0 Revision Silicon: The error will be corrected in all commercial-grade Revision C0 devices.

Industrial-grade B1/C0 Revision Silicon: The is no plan to address this erratum for Industrial-grade B1/C0 devices. Use Revision C1 or newer devices.

All C1 or Newer Revision Silicon: The error will be corrected in all Revision C1 devices (consumer or industrial-grade).

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APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000847D (03-12-21)	Clock Data Recovery Block Power-On Failures for Small Subset of Devices at USB3.x Gen 1 speeds	Added this section.
DS80000847C (08-14-20)	PF29 cannot be initialized by configuration OTP	Added this section.
DS80000847B (05-14-20)	Table 1	Added part number USB7252 in the list of affected silicon revisions.
	Type-C Bridging	Updated to show impact to USB7252.
	Type-C VBUS discharge in Port Power On/Off test	Added this section describing Type-C VBUS discharge in Port Power On/Off test.
	I^2C Bridge sends an extra byte under certain conditions	Added this section describing the scenario where the I^2C Bridge sends two bytes of data
DS80000847A (09-19-19)	Initial release	

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