AN2935

Configuration of USB7202/USB7206/USB7216/USB725x

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INTRODUCTION

The USB7202/USB7206/USB7216/USB7250/USB7251/USB7252/USB7256 can be configured through:

- Hardware configuration straps (See USB7202/USB7206/USB7216/USB7250/USB7251/USB7252/USB7256 Data Sheet for hardware strap descriptions.)
- SMBus during start-up configuration stage (SOC_CFG)
- SMBus during hub operational stages (during runtime)
- One-Time Programmable (OTP) memory
- A USB interface during hub operational stages (during runtime)
- An external Serial Peripheral Interface (SPI) flash

SMBus Configuration: The hub may be configured via the SMBus client interface during the hub's start-up configuration stage (or SOC_CFG). To hold the hub in the SOC_CFG stage, the CONFIG_STRAP pins must be set with the correct configuration mode (CONFIG1 for USB7202/USB7206/USB7216/USB7251/US7252/USB7256, and CONFIG1, 2, 3, or 5 for USB7250). The SMBus client clock and data pins must also be sampled as "high" (10k pull-up resistors to 3.3V recommended) at power-on or when RESET_N is deasserted. Once in the configuration stage, any of the registers may be reconfigured. The hub waits in SOC_CFG indefinitely until it receives the special Attach command.

After the hub has exited the SOC_CFG stage, the Configuration registers may still be manipulated via SMBus. This may be useful for enabling an external SOC to control the hub's GPIOs or to check certain hub status registers.

OTP Memory: The hub's registers may be configured via the hub's internal OTP memory. Any register may be given a new default value. The OTP memory is 8 kB, and each bit within the OTP memory may be set once but never cleared. The OTP commands are loaded sequentially, so it is possible to overwrite a previously programmed register setting by programming that register subsequently with a new value. The OTP memory may be programmed via the USB interface or via SMBus.

USB Interface: All registers are accessible from the USB host using vendor-specific commands issued to the hub's internal Hub Feature Controller device.

External SPI Memory Device: If a custom firmware image is being used and executed from an attached SPI memory device, the Configuration registers may also be configured within the SPI image. This method mimics the OTP configuration method and is referred to as "pseudo-OTP."

SECTIONS

This document includes the following topics:

- Section 1.0, "Hub Operational Mode"
- Section 2.0, "Register Map"
- Section 3.0, "SMBus Configuration"
- Section 4.0, "OTP Configuration"
- Section 5.0, "Hub Product IDs"
- Section 6.0, "Physical and Logical Port Mapping"
- Section 7.0, "Billboard Device"

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REFERENCES

The following documents should be referenced when using this application note. See your Microchip representative for availability.

- *USB7206 6-Port USB 3.1 Gen 2 Controller Hub Data Sheet*
- *MPLAB® Connect Configuration Tool*
- *System Management Bus Specification, Version 1.0*

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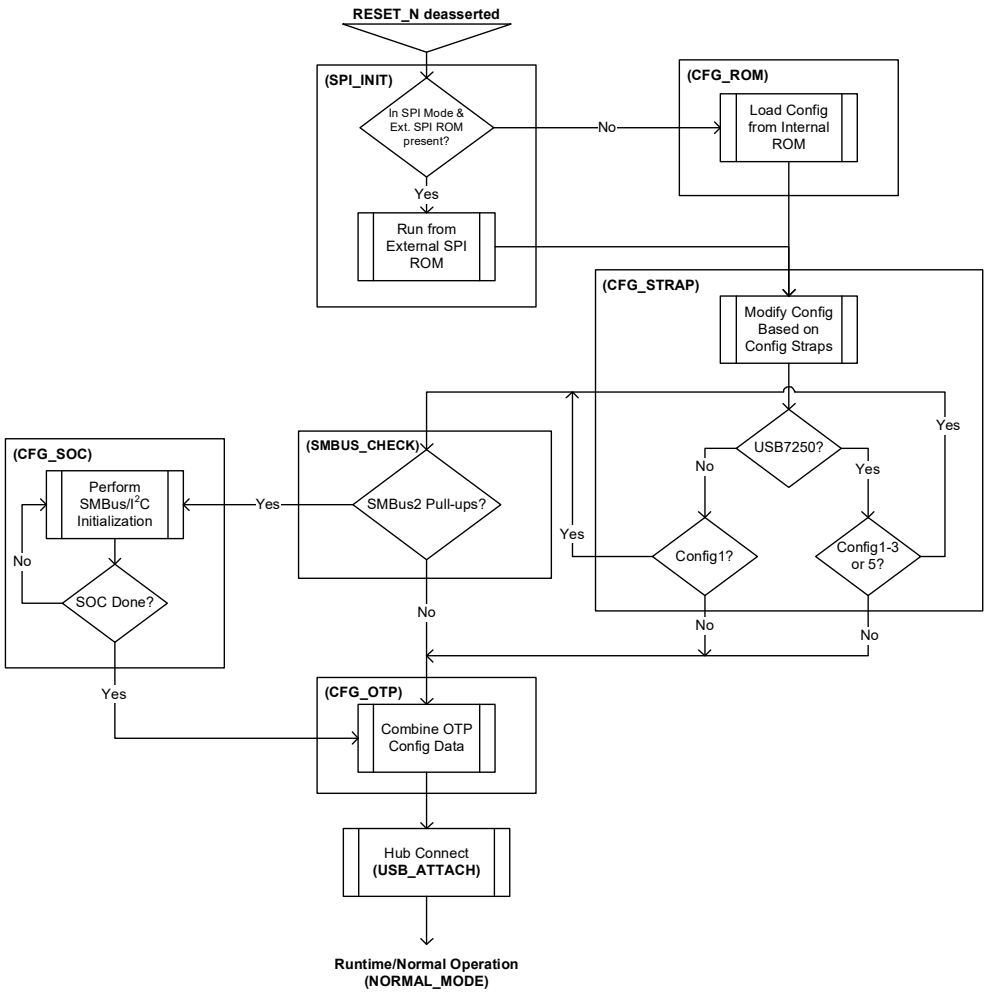
1.0 HUB OPERATIONAL MODE

1.1 Hub Configuration Stages

The hub is configured in three stages. The SOC_CFG stage is only entered if the CONFIG_STRAP pins are set with the correct configuration mode (CONFIG1 for USB7202/USB7206/USB7216/USB7251/US7252/USB7256, and CONFIG1, 2, 3, or 5 for USB7250), and the SMBus client interface pins (data and clock) are both sampled as “high” at start-up. (See **Note 2**.) During this stage, the hub allows an external SOC to configure the registers. The hub waits in SOC_CFG until it receives the special Attach command.

After the SOC_CFG stage is complete (or bypassed), the hub loads its OTP memory contents and manipulates the registers based on the OTP configuration. Figure 1 illustrates the hub start-up flow.

FIGURE 1: HUB CONFIGURATION OPERATIONAL MODE FLOWCHART



Note 1: Because the OTP Configuration registers are loaded after the SOC_CFG stage, it is possible for Configuration registers modified in the SOC_CFG stage to be overwritten in the CFG_OTP stage. If a register is modified in both the SOC_CFG and OTP_CFG stages (an OTP patch was programmed to the hub OTP), then the register value, as written in the OTP_CFG stage, takes effect.

2: The deprecated terms, “master” and “slave,” are replaced with “host” and “client,” respectively, throughout the document.

1.2 SMBus Protocol

The SMBus protocol is a flexible 2-pin serial protocol used for low-speed communication between integrated circuits. The protocol consists of an SMBCLK pin generated by the SMBus host and a bidirectional SMBDATA pin that can be driven by a host or a client. The bus requires a pull-up resistor on both SMBCLK and SMBDATA to function. The hub configures the pins as Open/Drain buffers, where the driver either tristates the pin or drives the pin to GND. The input threshold for the high level ranges from 1.2V to 3.3V, allowing the hub to communicate with a large sample of SOCs on the market. Refer to the *System Management Bus Specification* for more details on the timing specifications of the bus.

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2.0 REGISTER MAP

Note: It is recommended not to modify the current values of reserved bits to avoid operation failure.

2.1 Configuration Registers (Base Address: BF80_0000h)

TABLE 1: CONFIGURATION REGISTERS MEMORY MAP

Configuration Registers			Base Address: BF80_0000h	
Offset	**R/W**	**Name**	**Function**	**Modification Stage**
0000h	R	DEV_REV	Device Revision Register	Configuration
0908h	R/W	PIO96_OEN	PIO[96:64] Output Enable Register	Runtime or Configuration
0918h	R/W	PIO96_IEN	PIO[96:64] Input Enable Register	Runtime or Configuration
0928h	R/W	PIO96_OUT	PIO[96:64] Output Register	Runtime or Configuration
0938h	R/W	PIO96_IN	PIO[96:64] Input Register	Runtime or Configuration
0948h	R/W	PIO96_PU	PIO[96:64] Pull-Up Resistor Register	Runtime or Configuration
0958h	R/W	PIO96_PD	PIO[96:64] Pull-Down Resistor Register	Runtime or Configuration
0968h	R/W	PIO96_OD	PIO[96:64] Open-Drain Mode Register	Runtime or Configuration
09E8h	R/W	PIO96_DEB	PIO[96:64] Debounce Register	Runtime or Configuration
0C04h	R/W	PF1_CTL	Programmable Function 1 Control	Runtime or Configuration
0C05h	R/W	PF2_CTL	Programmable Function 2 Control	Runtime or Configuration
0C06h	R/W	PF3_CTL	Programmable Function 3 Control	Runtime or Configuration
0C07h	R/W	PF4_CTL	Programmable Function 4 Control	Runtime or Configuration
0C08h	R/W	PF5_CTL	Programmable Function 5 Control	Runtime or Configuration
0C09h	R/W	PF6_CTL	Programmable Function 6 Control	Runtime or Configuration
0C0Ah	R/W	PF7_CTL	Programmable Function 7 Control	Runtime or Configuration
0C0Bh	R/W	PF8_CTL	Programmable Function 8 Control	Runtime or Configuration
0C0Ch	R/W	PF9_CTL	Programmable Function 9 Control	Runtime or Configuration
0C0Dh	R/W	PF10_CTL	Programmable Function 10 Control	Runtime or Configuration
0C0Eh	R/W	PF11_CTL	Programmable Function 11 Control	Runtime or Configuration
0C0Fh	R/W	PF12_CTL	Programmable Function 12 Control	Runtime or Configuration
0C10h	R/W	PF13_CTL	Programmable Function 13 Control	Runtime or Configuration
0C11h	R/W	PF14_CTL	Programmable Function 14 Control	Runtime or Configuration

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TABLE 1: CONFIGURATION REGISTERS MEMORY MAP (CONTINUED)

Configuration Registers			Base Address: BF80_0000h	
Offset	**R/W**	**Name**	**Function**	**Modification Stage**
0C12h	R/W	PF15_CTL	Programmable Function 15 Control	Runtime or Configuration
0C13h	R/W	PF16_CTL	Programmable Function 16 Control	Runtime or Configuration
0C14h	R/W	PF17_CTL	Programmable Function 17 Control	Runtime or Configuration
0C15h	R/W	PF18_CTL	Programmable Function 18 Control	Runtime or Configuration
0C16h	R/W	PF19_CTL	Programmable Function 19 Control	Runtime or Configuration
0C17h	R/W	PF20_CTL	Programmable Function 20 Control	Runtime or Configuration
0C18h	R/W	PF21_CTL	Programmable Function 21 Control	Runtime or Configuration
0C19h	R/W	PF22_CTL	Programmable Function 22 Control	Runtime or Configuration
0C1Ah	R/W	PF23_CTL	Programmable Function 23 Control	Runtime or Configuration
0C1Bh	R/W	PF24_CTL	Programmable Function 24 Control	Runtime or Configuration
0C1Ch	R/W	PF25_CTL	Programmable Function 25 Control	Runtime or Configuration
0C1Dh	R/W	PF26_CTL	Programmable Function 26 Control	Runtime or Configuration
0C1Eh	R/W	PF27_CTL	Programmable Function 27 Control	Runtime or Configuration
0C1Fh	R/W	PF28_CTL	Programmable Function 28 Control	Runtime or Configuration
0C20h	R/W	PF29_CTL	Programmable Function 29 Control	Runtime or Configuration
0C21h	R/W	PF30_CTL	Programmable Function 30 Control	Runtime or Configuration
0C22h	R/W	PF31_CTL	Programmable Function 31 Control	Runtime or Configuration
3000h	R/W	VID_LSB	Vendor ID LSB	Configuration
3001h	R/W	VID_MSB	Vendor ID MSB	Configuration
3002h	R/W	PID_LSB	Product ID LSB	Configuration
3003h	R/W	PID_MSB	Product ID MSB	Configuration
3004h	R/W	DID_LSB	Device ID LSB	Configuration
3005h	R/W	DID_MSB	Device ID MSB	Configuration
3006h	R/W	HUB_CFG1	Hub Configuration Data Byte 1	Configuration
3007h	R/W	HUB_CFG2	Hub Configuration Data Byte 2	Configuration
3008h	R/W	HUB_CFG3	Hub Configuration Data Byte 3	Configuration
3009h	R/W	HUB_NRD	USB2 Hub Non-Removable Device	Configuration
300Ah	R/W	PORT_DIS_S	Port Disable – Self-Powered	Configuration
300Bh	R/W	PORT_DIS_B	Port Disable – Bus-Powered	Configuration
300Ch	R/W	H_MAXP_S	Hub Max Power – Self-Powered	Configuration
300Dh	R/W	H_MAXP_B	Hub Max Power – Bus-Powered	Configuration

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TABLE 1: CONFIGURATION REGISTERS MEMORY MAP (CONTINUED)

Configuration Registers			Base Address: BF80_0000h	
Offset	**R/W**	**Name**	**Function**	**Modification Stage**
300Eh	R/W	HC_MAXP_S	Hub Feature Controller Max Current – Self-Powered	Configuration
300Fh	R/W	HC_MAXP_B	Hub Feature Controller Max Current – Bus-Powered	Configuration
3010h	R/W	PWR_ON_TIME	Power-On Time Register	Configuration
3013h	R/W	MFR_STR_INDEX	USB2.0 Hub Manufacturer String Index Register	Configuration
3014h	R/W	PRD_STR_INDEX	USB2.0 Hub Product String Index Register	Configuration
3015h	R/W	SER_STR_INDEX	USB2.0 Hub Serial String Index Register	Configuration
30D0h	R	BC_EN	Battery Charging Enable Status Register	Runtime
30E1h	R/W	OCS_LOCKOUT	Start OCS Lockout Timer Register	Configuration
30E5h	R	PORT_PWR_STAT	Port Power Status	Runtime
30E6h	R	USB2_TEST_MODE	USB2 Test Mode Register	Runtime or Configuration
30E7h	R/W	HS_TRESP_TIMEOUT	LPM Turnaround Timeout	Configuration
30E9h	R/W	ENABLE_OCS_LEGACY	Enable OCS Legacy Register	Configuration
30EAh	R/W	OCS_MIN_WIDTH	OCS Minimum Width Register	Configuration
30EBh	R/W	OCS_INACTIVE_TIMER	OCS Inactive Timer	Configuration
30FAh	R/W	HUB_PRT_SWAP	Hub Port Swap Register	Configuration
30FBh	R/W	HUB_PRT_REMAP_12	USB2 Hub Port Remap 1-2 Register	Configuration
30FCh	R/W	HUB_PRT_REMAP_34	USB2 Hub Port Remap 3-4 Register	Configuration
30FDh	R/W	HUB_PRT_REMAP_56	USB2 Hub Port Remap 5-6 Register	Configuration
30FEh	R/W	HUB_PRT_REMAP_7	USB2 Hub Port Remap 7 Register	Configuration
3100h	R	USB2_LINK_STATE1	USB2 Link State Port 0-3	Runtime
3101h	R	USB2_LINK_STATE2	USB2 Link State Port 4-7	Runtime
3104h	R/W	USB2_HUB_CTL	USB2 Hub Control	Runtime
3108h	R/W	USB2_BCDUSB	USB2 Version BCD[15:0]	Configuration
318Ch	R/W	CNTLP	Hub Control Portable Test	Runtime
318Dh	R/W	EMBED_TEST_PORT_SEL	Embedded Hub Test Port Select	Runtime
3194h	R	USB2_HUB_STAT	USB2 Hub Status Register	Runtime
3195h	R	USB2_DN_SPEED41	USB2 Downstream Device Speed[4-1]	Runtime
3196h	R	USB2_DN_SPEED75	USB2 Downstream Device Speed[7-5]	Runtime
3197h	R	USB2_SUSP_IND	USB2 Suspend Indicator	Runtime
3840h	R/W	USB3_HUB_CTL	USB3 Hub Control	Configuration
3841h	R/W	USB3_HUB_CTL2	USB3 Hub Control 2	Configuration
3842h	R/W	USB3_HUB_CTL3	USB3 Hub Control 3	Configuration
3843h	R/W	USB3_VBUS_DEB_PERIOD	USB3 VBUS Debounce Register	Configuration
3844h	R/W	USB3_HUB_CTL4	USB3 Hub Control 4	Configuration
3849h	R/W	USB3_HUB_CTL5	USB3 Hub Control 5	Configuration
3851h	R	USB30_HUB_STAT	USB3 Hub Status Register	Runtime
3852h	R	USB30_HUB_DN_SPEED_IND1	USB3 Downstream Speed Indicator Register	Runtime
3853h	R	USB30_HUB_DN_SPEED_IND2	USB3 Downstream Speed Indicator Register 2	Runtime

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TABLE 1: CONFIGURATION REGISTERS MEMORY MAP (CONTINUED)

Configuration Registers			Base Address: BF80_0000h	
Offset	**R/W**	**Name**	**Function**	**Modification Stage**
3857h	R	USB30_SUSP_IND	USB3 Suspend Indicator	Runtime
3858h	R/W	USB3_PRT_REMAP	USB3 Port Remap Enable Register	Configuration
3860h	R/W	USB3_PRT_REMAP_2AND1	USB3 Port Remap Ports 1 and 2	Configuration
3861h	R/W	USB3_PRT_REMAP_4AND3	USB3 Port Remap Ports 3 and 4	Configuration
3862h	R/W	USB3_PRT_REMAP_6AND5	USB3 Port Remap Ports 5 and 6	Configuration
3870h	R	PHY_STATE1	USB3 PHY States Register 1	Runtime
3874h	R	PHY_STATE2	USB3 PHY States Register 2	Runtime
392Ch	R/W	USB_GEN2_HUB_CTRL_REG	USB GEN2 Hub Control Register	Configuration
3C00h	R/W	PORT_CFG_SEL_0	PORT 0 (Upstream) Port Power Select	Configuration
3C04h	R/W	PORT_CFG_SEL_1	PORT 1 Port Power Select	Configuration
3C08h	R/W	PORT_CFG_SEL_2	PORT 2 Port Power Select	Configuration
3C0Ch	R/W	PORT_CFG_SEL_3	PORT 3 Port Power Select	Configuration
3C10h	R/W	PORT_CFG_SEL_4	PORT 4 Port Power Select	Configuration
3C14h	R/W	PORT_CFG_SEL_5	PORT 5 Port Power Select	Configuration
3C18h	R/W	PORT_CFG_SEL_6	PORT 6 Port Power Select	Configuration
3C20h	R/W	USB_OCS_SEL_1	USB Port 1 OCS Source Select	Configuration
3C24h	R/W	USB_OCS_SEL_2	USB Port 2 OCS Source Select	Configuration
3C28h	R/W	USB_OCS_SEL_3	USB Port 3 OCS Source Select	Configuration
3C2Ch	R/W	USB_OCS_SEL_4	USB Port 4 OCS Source Select	Configuration
3C30h	R/W	USB_OCS_SEL_5	USB Port 5 OCS Source Select	Configuration
3034h	R/W	USB_OCS_SEL_6	USB Port 6 OCS Source Select	Configuration
3038h	R/W	USB_OCS_SEL_7	USB Port 7 OCS Source Select	Configuration
3C40h	R/W	VBUS_PASS_THRU	VBUS_DET Pass-Through Register	Configuration
3C50h	R	PORT_STAT_REG_0	Port 0 (Upstream) Status Register	Runtime
3C54h	R	PORT_STAT_REG_1	Port 1 Status Register	Runtime
3C58h	R	PORT_STAT_REG_2	Port 2 Status Register	Runtime
3C5Ch	R	PORT_STAT_REG_3	Port 3 Status Register	Runtime
3C60h	R	PORT_STAT_REG_4	Port 4 Status Register	Runtime
3C64h	R	PORT_STAT_REG_5	Port 5 Status Register	Runtime
3C68h	R	PORT_STAT_REG_6	Port 6 Status Register	Runtime
3C6Ch	R	PORT_STAT_REG_7	Port 7 Status Register	Runtime
6086h	R/W	SS_P0_AFE_TEST_IN4	USB3 Upstream TX Pre-Driver	Configuration
60C8h	R/W	UP_RISE_FALL_ADJ	USB 2.0 Upstream Rise and Fall Adjustment Register	Configuration
60CAh	R/W	HS_P0_BOOST	USB Port 0 Boost Register	Configuration
60CCh	R/W	HS_P0_VSENSE	USB Port 0 VariSense™ Register	Configuration
61C0h	R	SS_P0_LTSSM_STATE	USB3 Upstream LTSSM State	Runtime
61C1h	R/W	SS_P0_TEST_PIPE_DC	USB3 Upstream DC Test Register	Configuration
61C3h	R/W	SS_P0_TEST_PIPE_TX_PAT	USB3 Upstream TX Test Pattern Register	Configuration
61D0h	R/W	SS_P0_TEST_PIPE_PIPE_CTL_0	USB3 Upstream TX_MARGIN	Configuration
62A0h	R/W	SS_P0_PIPE_TX_DEEMPH_CTL	USB3 Upstream Gen1 Deemphasis	Configuration

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TABLE 1: CONFIGURATION REGISTERS MEMORY MAP (CONTINUED)

Configuration Registers			Base Address: BF80_0000h	
Offset	**R/W**	**Name**	**Function**	**Modification Stage**
62B8h	R/W	SS_P0_PIPE_TX_DEEMPH_GEN2_CTL	USB3 Upstream Gen2 Deemphasis	Configuration
6486h	R/W	SS_P1_AFE_TEST_IN4	USB3 Port 1 TX Pre-Driver	Configuration
64C8h	R/W	P1_RISE_FALL_ADJ	USB 2.0 Port 1 Rise and Fall Adjustment Register	Configuration
64CAh	R/W	HS_P1_BOOST	USB Port 1 Boost Register	Configuration
64CCh	R/W	HS_P1_VSENSE	USB Port 1 VariSense™ Register	Configuration
65C0h	R	SS_P1_LTSSM_STATE	USB3 Port 1 LTSSM State	Runtime
65C1h	R/W	SS_P1_TEST_PIPE_DC	USB3 Port 1 DC Test Register	Configuration
65C3h	R/W	SS_P1_TEST_PIPE_TX_PAT	USB3 Port 1 TX Test Pattern Register	Configuration
65D0h	R/W	SS_P1_TEST_PIPE_PIPE_CTL_0	USB3 Port 1 TX_MARGIN	Configuration
66A0h	R/W	SS_P1_PIPE_TX_DEEMPH_CTL	USB3 Port 1 Gen1 Deemphasis	Configuration
66B8h	R/W	SS_P1_PIPE_TX_DEEMPH_GEN2_CTL	USB3 Port 1 Gen2 Deemphasis	Configuration
6886h	R/W	SS_P2_AFE_TEST_IN4	USB3 Port 2 TX Pre-Driver	Configuration
68C8h	R/W	P2_RISE_FALL_ADJ	USB 2.0 Port 6 Rise and Fall Adjustment Register	Configuration
68CAh	R/W	HS_P2_BOOST	USB Port 2 Boost Register	Configuration
68CCh	R/W	HS_P2_VSENSE	USB Port 2 VariSense™ Register	Configuration
69C0h	R	SS_P2_LTSSM_STATE	USB3 Port 2 LTSSM State	Runtime
69C1h	R/W	SS_P2_TEST_PIPE_DC	USB3 Port 2 DC Test Register	Configuration
69C3h	R/W	SS_P2_TEST_PIPE_TX_PAT	USB3 Port 2 TX Test Pattern Register	Configuration
69D0h	R/W	SS_P2_TEST_PIPE_PIPE_CTL_0	USB3 Port 2 TX_MARGIN	Configuration
6AA0h	R/W	SS_P2_PIPE_TX_DEEMPH_CTL	USB3 Port 2 Gen1 Deemphasis	Configuration
6AB8h	R/W	SS_P2_PIPE_TX_DEEMPH_GEN2_CTL	USB3 Port 2 Gen2 Deemphasis	Configuration
6CCAh	R/W	HS_P3_BOOST	USB Port 3 Boost Register	Configuration
6CCCh	R/W	HS_P3_VSENSE	USB Port 3 VariSense™ Register	Configuration
6CC8h	R/W	P3_RISE_FALL_ADJ	USB 2.0 Port 3 Rise and Fall Adjustment Register	Configuration
6C86h	R/W	SS_P3_AFE_TEST_IN4	USB3 Port 3 TX Pre-Driver	Configuration
6DC0h	R	SS_P3_LTSSM_STATE	USB3 Port 3 LTSSM State	Runtime
6DC1h	R/W	SS_P3_TEST_PIPE_DC	USB3 Port 3 DC Test Register	Configuration
6DC3h	R/W	SS_P3_TEST_PIPE_TX_PAT	USB3 Port 3 TX Test Pattern Register	Configuration
6DD0h	R/W	SS_P3_TEST_PIPE_PIPE_CTL_0	USB3 Port 3 TX_MARGIN	Configuration
6EA0h	R/W	SS_P3_PIPE_TX_DEEMPH_CTL	USB3 Port 3 Gen1 Deemphasis	Configuration
6EB8h	R/W	SS_P3_PIPE_TX_DEEMPH_GEN2_CTL	USB3 Port 3 Gen2 Deemphasis	Configuration
70CAh	R/W	HS_P4_BOOST	USB Port 4 Boost Register	Configuration

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TABLE 1: CONFIGURATION REGISTERS MEMORY MAP (CONTINUED)

Configuration Registers			Base Address: BF80_0000h	
Offset	**R/W**	**Name**	**Function**	**Modification Stage**
70CCh	R/W	HS_P4_VSENSE	USB Port 4 VariSense™ Register	Configuration
70C8h	R/W	P4_RISE_FALL_ADJ	USB 2.0 Port 4 Rise and Fall Adjustment Register	Configuration
7086h	R/W	SS_P4_AFE_TEST_IN4	USB3 Port 4 TX Pre-Driver	Configuration
71C0h	R	SS_P4_LTSSM_STATE	USB3 Port 4 LTSSM State	Runtime
71C1h	R/W	SS_P4_TEST_PIPE_DC	USB3 Port 4 DC Test Register	Configuration
71C3h	R/W	SS_P4_TEST_PIPE_TX_PAT	USB3 Port 4 TX Test Pattern Register	Configuration
71D0h	R/W	SS_P4_TEST_PIPE_PIPE_CT-L_0	USB3 Port 4 TX_MARGIN	Configuration
72A0h	R/W	SS_P4_PIPE_TX_DEEMPH_CTL	USB3 Port 4 Gen1 Deemphasis	Configuration
72B8h	R/W	SS_P4_PIPE_TX_DEEMPH_GEN2_CTL	USB3 Port 4 Gen2 Deemphasis	Configuration
74CAh	R/W	HS_P5_BOOST	USB Port 5 Boost Register	Configuration
74CCh	R/W	HS_P5_VSENSE	USB Port 5 VariSense™ Register	Configuration
74C8h	R/W	P5_RISE_FALL_ADJ	USB 2.0 Port 5 Rise and Fall Adjustment Register	Configuration
7486h	R/W	SS_P5_AFE_TEST_IN4	USB3 Port 5 TX Pre-Driver	Configuration
75C0h	R	SS_P5_LTSSM_STATE	USB3 Port 5 LTSSM State	Runtime
75C1h	R/W	SS_P5_TEST_PIPE_DC	USB3 Port 5 DC Test Register	Configuration
75C3h	R/W	SS_P5_TEST_PIPE_TX_PAT	USB3 Port 5 TX Test Pattern Register	Configuration
75D0h	R/W	SS_P5_TEST_PIPE_PIPE_CT-L_0	USB3 Port 5 TX_MARGIN	Configuration
76A0h	R/W	SS_P5_PIPE_TX_DEEMPH_CTL	USB3 Port 5 Gen1 Deemphasis	Configuration
76B8h	R/W	SS_P5_PIPE_TX_DEEMPH_GEN2_CTL	USB3 Port 5 Gen2 Deemphasis	Configuration
78CAh	R/W	HS_P6_BOOST	USB 2.0 Downstream Port 6 PHYBoost Register	Configuration
78CCh	R/W	HS_P6_SENSE	USB 2.0 Downstream Port 6 Varisense™ Register	Configuration
7886h	R/W	SS_P6_AFE_TEST_IN4	USB3 Port 6 TX Pre-Driver	Configuration
79C0h	R	SS_P6_LTSSM_STATE	USB3 Port 6 LTSSM State	Runtime
79C1h	R/W	SS_P6_TEST_PIPE_DC	USB3 Port 6 DC Test Register	Configuration
79C3h	R/W	SS_P6_TEST_PIPE_TX_PAT	USB3 Port 6 TX Test Pattern Register	Configuration
79D0h	R/W	SS_P6_TEST_PIPE_PIPE_CT-L_0	USB3 Port 6 TX_MARGIN	Configuration
7AA0h	R/W	SS_P6_PIPE_TX_DEEMPH_CTL	USB3 Port 6 Gen1 Deemphasis	Configuration
7AB8h	R/W	SS_P6_PIPE_TX_DEEMPH_GEN2_CTL	USB3 Port 6 Gen2 Deemphasis	Configuration

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2.2 Configuration Registers (Base Address: BFD2_0000h)

TABLE 2: CONFIGURATION REGISTERS MEMORY MAP

Configuration Registers			Base Address: BFD2_0000h	
Offset	**R/W**	**Name**	**Function**	**Recommended Modification Stage**
2866h	R/W	HFC_PID_LSB	HFC Product ID LSB	Configuration
2867h	R/W	HFC_PID_MSB	HFC Product ID MSB	Configuration
2864h	R/W	HFC_VID_LSB	HFC Vendor ID LSB	Configuration
2865h	R/W	HFC_VID_MSB	HFC Vendor ID MSB	Configuration
2868h	R/W	HFC_DID_LSB	HFC Device ID (bcdDevice) LSB	Configuration
2869h	R/W	HFC_DID_MSB	HFC Device ID (bcdDevice) MSB	Configuration
286Ah	R/W	HFC_MFR_STR_INDEX	USB2.0 HFC Manufacturer String Index Register	Configuration
286Bh	R/W	HFC_PRD_STR_INDEX	USB2.0 HFC Product String Index Register	Configuration
286Ch	R/W	HFC_SER_STR_INDEX	USB2.0 HFC Serial String Index Register	Configuration
28FAh	R/W	HFC_LANG_ID	HFC LANG_ID[15:0] Language Identifier	Configuration
28FCh	R/W	HFC_STR_CONTAINTER	HFC Product String Descriptor Container	Configuration
3202h	R/W	USB2_HUB_LANG_ID	USB2.0 Hub LANG_ID[15:0] Language Identifier	Configuration
3204h	R/W	USB2_HUB_STR_CONTAINTER	USB2.0 Hub String Descriptor Container	Configuration
3400h	R/W	RUNTIME_FLAGS	Runtime Flags Memory	Runtime or Configuration
3408h	R/W	RUNTIME_FLAGS2	Runtime Flags 2 Memory	Runtime or Configuration
3412h	R/W	I2S_FEAT_SEL	I2S Feature Select Register	Configuration
3413h	R/W	I2S_HFEAT_SEL	I2S HID Feature Select Register	Configuration
3419h	R/W	SMBUS_OTP_RES	SMBUS OTP Result	Configuration
341Bh	R/W	OTP_UDC_ENABLE	OTP UDC Enumeration	Configuration
341Eh	R/W	HUB_DEF_PIDM	Hub PID MSB	Configuration
341Fh	R/W	HUB_DEF_PIDL	Hub PID LSB	Configuration
3433h	R/W	BC_CONFIG_P1	Port 1 Battery Charging Configuration	Configuration
3434h	R/W	BC_CONFIG_P2	Port 2 Battery Charging Configuration	Configuration
3435h	R/W	BC_CONFIG_P3	Port 3 Battery Charging Configuration	Configuration
3436h	R/W	BC_CONFIG_P4	Port 4 Battery Charging Configuration	Configuration
3437h	R/W	BC_CONFIG_P5	Port 5 Battery Charging Configuration	Configuration
3438h	R/W	BC_CONFIG_P6	Port 6 Battery Charging Configuration	Configuration
3442h	R/W	FLEX_IN_PORT1	FLEX_IN_Port1	Configuration
3443h	R/W	FLEX_IN_PORT2	FLEX_IN_Port2	Configuration
3444h	R/W	FLEX_IN_PORT3	FLEX_IN_Port3	Configuration
3445h	R/W	FLEX_IN_PORT4	FLEX_IN_Port4	Configuration
3446h	R/W	FLEX_IN_PORT5	FLEX_IN_Port5	Configuration
3447h	R/W	FLEX_IN_PORT6	FLEX_IN_Port6	Configuration
3448h	R/W	FLEX_OUT_PORT1	FLEX_OUT_Port1	Configuration
3449h	R/W	FLEX_OUT_PORT2	FLEX_OUT_Port2	Configuration
344Ah	R/W	FLEX_OUT_PORT3	FLEX_OUT_Port3	Configuration

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TABLE 2: CONFIGURATION REGISTERS MEMORY MAP (CONTINUED)

Configuration Registers			Base Address: BFD2_0000h	
Offset	**R/W**	**Name**	**Function**	**Recommended Modification Stage**
344Bh	R/W	FLEX_OUT_PORT4	FLEX_OUT_Port4	Configuration
344Ch	R/W	FLEX_OUT_PORT5	FLEX_OUT_Port5	Configuration
344Dh	R/W	FLEX_OUT_PORT6	FLEX_OUT_Port6	Configuration
344Eh	R/W	FLEX_PRTCTL_PORT1	FLEX_PRTCTL_Port1	Configuration
344Fh	R/W	FLEX_PRTCTL_PORT2	FLEX_PRTCTL_Port2	Configuration
3450h	R/W	FLEX_PRTCTL_PORT3	FLEX_PRTCTL_Port3	Configuration
3451h	R/W	FLEX_PRTCTL_PORT4	FLEX_PRTCTL_Port4	Configuration
3452h	R/W	FLEX_PRTCTL_PORT5	FLEX_PRTCTL_Port5	Configuration
3453h	R/W	FLEX_PRTCTL_PORT6	FLEX_PRTCTL_Port6	Configuration
3454h	R/W	FLEX_VBUSDET	FLEX_VBUSDET	Configuration
3455h	R/W	FLEX_ATTACH_DELAY	FlexConnect Hub Attach Delay	Configuration
3456h	R/W	ROLE_SWITCH_DELAY	Role Switch Delay	Configuration
346Ah	R/W	MFG_STR_LEN	Manufacturer String Length	Configuration
3472h	R/W	PROD_STR_LEN	Product String Length	Configuration
E542h	R/W	USB3_HUB_BCDUSB_LSB	USB3 Hub BcdUSB LSB	Configuration
E542h	R/W	USB3_HUB_BCDUSB_MSB	USB3 Hub BcdUSB MSB	Configuration
E548h	R/W	USB3_HUB_VID_LSB	USB3 Hub Vendor ID LSB	Configuration
E549h	R/W	USB3_HUB_VID_MSB	USB3 Hub Vendor ID MSB	Configuration
E54Ah	R/W	USB3_HUB_PID_MSB	USB3 Hub Product ID MSB	Configuration
E54Bh	R/W	USB3_HUB_PID_LSB	USB3 Hub Product ID LSB	Configuration
E54Ch	R/W	USB3_HUB_DID_LSB	USB3 Hub Device ID (bcdDevice) LSB	Configuration
E54Dh	R/W	USB3_HUB_DID_MSB	USB3 Hub Device ID (bcdDevice) MSB	Configuration
E54Eh	R/W	USB3_HUB_MFR_STR_INDEX	USB3 Hub Manufacturer String Index Register	Configuration
E54Fh	R/W	USB3_HUB_PRD_STR_INDEX	USB3 Hub Product String Index Register	Configuration
E550h	R/W	USB3_HUB_SER_STR_INDEX	USB3 Hub Serial String Index Register	Configuration
E5DAh	R/W	USB3_HUB_LANG_ID	USB3 Hub LANG_ID[15:0] Language Identifier	Configuration
E5E0h	R/W	USB3_HUB_STR_CONTAINTER	USB3 Hub String Descriptor Container	Configuration
E55Fh	R/W	USB3_HUB_ATTRIBUTES	USB3 Hub Attributes Descriptor	Configuration
E560h	R/W	USB3_HUB_MAX_POWER	USB3 Hub Max Power Descriptor	Configuration
E5CAh	R/W	USB3_HUB_NBR_PORTS	USB3 Hub Number of Ports Descriptor	Configuration
E5CBh	R/W	USB3_HUB_CHARACTERISTICS	USB3 Hub Characteristics Descriptor	Configuration
E5CDh	R/W	UBS3_HUB_PWR2PWRGOOD	USB3 Hub Power-to-Power Good Descriptor	Configuration
E5D2h	R/W	USB3_HUB_NON_REM	USB3 Hub Non-Removable Parts Descriptor	Configuration

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2.3 PFx Function/Pin Number/PIO Register Mapping

TABLE 3: PFX TO PIN NUMBER AND PIO REGISTER MAPPING

PFx	USB7202	USB7206	USB7250	USB7251	USB7252	USB7216/ USB7256	PIO	Register
	Pin #	Pin #	Pin #	Pin #	Pin #	Pin #		
PF2			43				GPIO66	PIO96[2]
PF3			44				GPIO67	PIO96[3]
PF4			45	45			GPIO68	PIO96[4]
PF5			56				GPIO69	PIO96[5]
PF6	47		47	47	47	47	GPIO70	PIO96[6]
PF7	48		48	48	48	48	GPIO71	PIO96[7]
PF10						51	GPIO74	PIO96[10]
PF11						51	GPIO75	PIO96[11]
PF12	54						GPIO76	PIO96[12]
PF14	57		57	57	57		GPIO78	PIO96[14]
PF18	61						GPIO82	PIO96[18]
PF19	66		66	66	66		GPIO83	PIO96[19]
PF26	75		75	75	75		GPIO90	PIO96[26]
PF27	76		76	76	76		GPIO91	PIO96[27]
PF28	77		77	77	77		GPIO92	PIO96[28]
PF29	74		74	74	74		GPIO93	PIO96[29]
PF30	2		2	2			GPIO94	PIO96[30]
PF31	3		3	3			GPIO95	PIO96[31]

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2.3.1 REGISTER DEFINITIONS

TABLE 4: DEVICE REVISION REGISTER

DEV_REV OFFSET: 0000h RESET = Depends on device			**Device Revision Register Base Address: BF80_0000h**
Bit	**Name**	**R/W**	**Description**
31:16	DEVID	R	Device ID: 0589h
15:8	Reserved	R	Always ‘0’
7:0	REVID	R	Silicon Revision ID A0h = A0 silicon B0h = B0 silicon C0h = C0 silicon

TABLE 5: PIO[96:64] OUTPUT ENABLE REGISTER

PIO96_OEN OFFSET: 0908h RESET = Depends on device and CFG_STRAP settings			**PIO96 Output Enable Register Base Address: BF80_0000h**
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_OEN[96:64]	R/W	PIO96_OEN[x] ‘0’ = Disabled ‘1’ = Enabled

Note 1: 0908h-[7:0], 0909h-[15:8], 090Ah-[23:16], 090Bh-[31:24]

TABLE 6: PIO[96:64] INPUT ENABLE REGISTER

PIO96_IEN OFFSET: 0918h RESET = Depends on device and CFG_STRAP settings			**PIO96 Input Enable Register Base Address: BF80_0000h**
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_IEN[96:64]	R/W	PIO96_IEN[x] ‘0’ = Disabled ‘1’ = Enabled

Note 1: 0918h-[7:0], 0919h-[15:8], 091Ah-[23:16], 091Bh-[31:24]

TABLE 7: PIO[96:64] OUTPUT REGISTER

PIO96_OUT OFFSET: 0928h RESET = Depends on device and CFG_STRAP settings			**PIO96 Output Register Base Address: BF80_0000h**
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_OUT[96:64]	R/W	PIO96_OUT[x] ‘0’ = Output is 0 ‘1’ = Output is 1

Note 1: 0928h-[7:0], 0929h-[15:8], 092Ah-[23:16], 092Bh-[31:24]

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TABLE 8: PIO[96:64] INPUT REGISTER

PIO96_IN OFFSET: 0938h RESET = Depends on device and CFG_STRAP settings			PIO96 Input Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_IN[96:64]	R/W	PIO96_IN[x] '0' = Input is 0 '1' = Input is 1

Note 1: 0938h-[7:0], 0939h-[15:8], 093Ah-[23:16], 093Bh-[31:24]

TABLE 9: PIO[96:64] PULL-UP RESISTOR REGISTER

PIO96_PU OFFSET: 0948h RESET = Depends on device and CFG_STRAP settings			PIO96 Pull-Up Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_PU[96:64]	R/W	PIO96_PU[x] '0' = Pull-Up Disabled '1' = Pull-Up Enabled

Note 1: 0948h-[7:0], 0949h-[15:8], 094Ah-[23:16], 094Bh-[31:24]

TABLE 10: PIO[96:64] PULL-DOWN RESISTOR REGISTER

PIO96_PD OFFSET: 0958h RESET = Depends on device and CFG_STRAP settings			PIO96 Pull-Down Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_PD[96:64]	R/W	PIO96_PD[x] '0' = Pull-Down Disabled '1' = Pull-Down Enabled

Note 1: 0958h-[7:0], 0959h-[15:8], 095Ah-[23:16], 095Bh-[31:24]

TABLE 11: PIO[96:64] OPEN-DRAIN MODE REGISTER

PIO96_OD OFFSET: 0968h RESET = Depends on device and CFG_STRAP settings			PIO96 Open-Drain Mode Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_OD[96:64]	R/W	PIO96_OD[x] '0' = Open Drain Disabled '1' = Open Drain Enabled If bit is 1 and the corresponding output is enabled {If output register is 1, output is Hi-Z unless pull-up is enabled. If output register is 0, output is 0.}

Note 1: 0968h-[7:0], 0969h-[15:8], 096Ah-[23:16], 096Bh-[31:24]

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TABLE 12: PIO[96:64] DEBOUNCE REGISTER

PIO96_DEB OFFSET: 09E8h RESET = 0000_0000h			PIO96 Debounce Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_DEB[96:64]	R/W	PIO96_DEB[x] '0' = No debounce '1' = Input debounced as specified in GPIO_DEBOUNCE

Note 1: 09E8h-[7:0], 09E9h-[15:8], 09EAh-[23:16], 09EBh-[31:24]

TABLE 13: PROGRAMMABLE FUNCTION 1 CONTROL

PF1_CTL OFFSET: 0C04h RESET = Depends on device and CFG_STRAP settings			PF1 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always '0'
3:0	Select	R/W	000 = GPIO65

TABLE 14: PROGRAMMABLE FUNCTION 2 CONTROL

PF2_CTL OFFSET: 0C05h RESET = Depends on device and CFG_STRAP settings			PF2 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always '0'
3:0	Select	R/W	000 = GPIO66 001 = Reserved 010 = UART_nCTS 011 = DP1_VCONN1 100 = UART_nDSR 101 = PD_SPI_CE_N4 110 = I2S_SDO

TABLE 15: PROGRAMMABLE FUNCTION 3 CONTROL

PF3_CTL OFFSET: 0C06h RESET = Depends on device and CFG_STRAP settings			PF3 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always '0'
3:0	Select	R/W	000 = GPIO67 001 = I2S_SDI 010 = UART_nRTS 011 = DP1_VCONN2 100 = PD_SPI_CE_N3

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TABLE 16: PROGRAMMABLE FUNCTION 4 CONTROL

PF4_CTL OFFSET: 0C07h RESET = Depends on device and CFG_STRAP settings			PF4 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO68 001 = I2S_SDO 010 = UART_nDSR 011 = DP3_DISCHARGE 100 = PD_SPI_CE_N2 101 = DP1_VCONN1

TABLE 17: PROGRAMMABLE FUNCTION 5 CONTROL

PF5_CTL OFFSET: 0C08h RESET = Depends on device and CFG_STRAP settings			PF5 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO69 001 = I2S_SCK 010 = UART_nDTR 011 = DP1_DISCHARGE 100 = PD_SPI_CE_N1

TABLE 18: PROGRAMMABLE FUNCTION 6 CONTROL

PF6_CTL OFFSET: 0C09h RESET = Depends on device and CFG_STRAP settings			PF6 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO70 001 = I2S_LRCK 010 = UART_RX 011 = DP1_DISCHARGE 100 = PD_SPI_CE_N0 101 = PRT_CTL1_U3

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TABLE 19: PROGRAMMABLE FUNCTION 7 CONTROL

PF7_CTL OFFSET: 0C0Ah RESET = Depends on device and CFG_STRAP settings			PF7 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO71 001 = I2S_MCLK 010 = UART_TX 011 = DP1_DISCHARGE 100 = PD_SPI_CLK 101 = PRT_CTL2_U3

TABLE 20: PROGRAMMABLE FUNCTION 8 CONTROL

PF8_CTL OFFSET: 0C0Bh RESET = Depends on device and CFG_STRAP settings			PF8 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO72 001 = PD_I2C_DATA 010 = Reserved 011 = DP1_VCONN1 100 = PD_SPI_DO

TABLE 21: PROGRAMMABLE FUNCTION 9 CONTROL

PF9_CTL OFFSET: 0C0Ch RESET = Depends on device and CFG_STRAP settings			PF9 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO73 001 = PD_I2C_CLK 010 = Reserved 011 = DP1_VCONN2 100 = PD_SPI_DI

TABLE 22: PROGRAMMABLE FUNCTION 10 CONTROL

PF10_CTL OFFSET: 0C0Dh RESET = Depends on device and CFG_STRAP settings			PF10 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’

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TABLE 22: PROGRAMMABLE FUNCTION 10 CONTROL (CONTINUED)

PF10_CTL OFFSET: 0C0Dh RESET = Depends on device and CFG_STRAP settings			PF10 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	Select	R/W	000 = GPIO74 001 = MSTR_I2C_DATA 010 = PRT_CTL3_U3 011 = DP3_VCONN1 100 = PD_SPI_CE_N5 101 = I2S_SDI

TABLE 23: PROGRAMMABLE FUNCTION 11 CONTROL

PF11_CTL OFFSET: 0C0Eh RESET = Depends on CFG_STRAP settings			PF11 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO75 001 = MSTR_I2C_CLK 010 = PRT_CTL4_U3 011 = DP3_VCONN2 100 = PD_SPI_CE_N6 101 = I2S_MCLK

TABLE 24: PROGRAMMABLE FUNCTION 12 CONTROL

PF12_CTL OFFSET: 0C0Fh RESET = Depends on device and CFG_STRAP settings			PF12 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO76 001 = PRT_CTL5_U3

TABLE 25: PROGRAMMABLE FUNCTION 13 CONTROL

PF13_CTL OFFSET: 0C10h RESET = Depends on device and CFG_STRAP settings			PF13 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO77 001 = PRT_CTL5/OCS 010 = PRT_CTL4/OCS

TABLE 26: PROGRAMMABLE FUNCTION 14 CONTROL

PF14_CTL OFFSET: 0C11h RESET = Depends on device and CFG_STRAP settings			PF14 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO78 001 = I2S_SDI 010 = UART_nCTS 011 = PRT_CTL4/OCS 100 = MSTR_I2C_CLK 101 = UART_nRTS 110 = UART_nDTR

TABLE 27: PROGRAMMABLE FUNCTION 15 CONTROL

PF15_CTL OFFSET: 0C12h RESET = Depends on device and CFG_STRAP settings			PF15 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO79 001 = PRT_CTL3/OCS

TABLE 28: PROGRAMMABLE FUNCTION 16 CONTROL

PF16_CTL OFFSET: 0C13h RESET = Depends on device and CFG_STRAP settings			PF16 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO80 001 = PRT_CTL2/OCS

TABLE 29: PROGRAMMABLE FUNCTION 17 CONTROL

PF17_CTL OFFSET: 0C14h RESET = Depends on device and CFG_STRAP settings			PF17 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO81 001 = PRT_CTL1/OCS

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TABLE 30: PROGRAMMABLE FUNCTION 18 CONTROL

PF18_CTL OFFSET: 0C15h RESET = Depends on device and CFG_STRAP settings			PF18 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO82 001 = I2S_LRCK 010 = UART_nDCD 011 = Reserved 100 = MSTR_I2C_CLK

TABLE 31: PROGRAMMABLE FUNCTION 19 CONTROL

PF19_CTL OFFSET: 0C16h RESET = Depends on device and CFG_STRAP settings			PF19 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO83 001 = I2S_SDO 010 = UART_nRTS 011 = SLV_I2C_DATA 100 = MSTR_I2C_DATA

TABLE 32: PROGRAMMABLE FUNCTION 20 CONTROL

PF20_CTL OFFSET: 0C17h RESET = Depends on device and CFG_STRAP settings			PF20 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO84 001 = SPI_CE_N

TABLE 33: PROGRAMMABLE FUNCTION 21 CONTROL

PF21_CTL OFFSET: 0C18h RESET = Depends on device and CFG_STRAP settings			PF21 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO85 001 = SPI_CLK

TABLE 34: PROGRAMMABLE FUNCTION 22 CONTROL

PF22_CTL OFFSET: 0C19h RESET = Depends on device and CFG_STRAP settings			PF22 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO86 001 = SPI_D0

TABLE 35: PROGRAMMABLE FUNCTION 23 CONTROL

PF23_CTL OFFSET: 0C1Ah RESET = Depends on device and CFG_STRAP settings			PF23 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO87 001 = SPI_D1

TABLE 36: PROGRAMMABLE FUNCTION 24 CONTROL

PF24_CTL OFFSET: 0C1Bh RESET = Depends on device and CFG_STRAP settings			PF24 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO88 001 = SPI_D2

TABLE 37: PROGRAMMABLE FUNCTION 25 CONTROL

PF25_CTL OFFSET: 0C1Ch RESET = Depends on device and CFG_STRAP settings			PF25 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO89 001 = SPI_D3

TABLE 38: PROGRAMMABLE FUNCTION 26 CONTROL

PF26_CTL OFFSET: 0C1Dh RESET = Depends on device and CFG_STRAP settings			PF26 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’

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TABLE 38: PROGRAMMABLE FUNCTION 26 CONTROL (CONTINUED)

PF26_CTL OFFSET: 0C1Dh RESET = Depends on device and CFG_STRAP settings			PF26 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	Select	R/W	000 = GPIO90 001 = I2S_SCK 010 = UART_nDSR 011 = Reserved 100 = SLV_I2C_CLK

TABLE 39: PROGRAMMABLE FUNCTION 27 CONTROL

PF27_CTL OFFSET: 0C1Eh RESET = Depends on device and CFG_STRAP settings			PF27 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always 0’
3:0	Select	R/W	000 = GPIO91 001 = I2S_MCLK 010 = UART_nDTR 011 = Reserved 100 = SLV_I2C_DATA 101 = PRT_CTL6/OCS 110 = UART_RX

TABLE 40: PROGRAMMABLE FUNCTION 28 CONTROL

PF28_CTL OFFSET: 0C1Fh RESET = Depends on device and CFG_STRAP settings			PF28 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	Select	R/W	000 = GPIO92 001 = I2S_LRCK 010 = UART_nDSD 011 = PRT_CTL6/OCS 100 = UART_TX

TABLE 41: PROGRAMMABLE FUNCTION 29 CONTROL

PF29_CTL OFFSET: 0C20h RESET = Depends on device and CFG_STRAP settings			PF29 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’

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TABLE 41: PROGRAMMABLE FUNCTION 29 CONTROL (CONTINUED)

PF29_CTL OFFSET: 0C20h RESET = Depends on device and CFG_STRAP settings			PF29 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	Select	R/W	000 = GPIO93 001 = CLOCK_OUT 010 = USB3_SUSP_IND 011 = USB2_SUSP_IND 100 = USB2_SUSP_IND or USB3_SUSP_IND (logical OR'ing of both USB2 and USB suspend indicators)

TABLE 42: PROGRAMMABLE FUNCTION 30 CONTROL

PF30_CTL OFFSET: 0C21h RESET = Depends on device and CFG_STRAP settings			PF30 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always '0'
3:0	Select	R/W	000 = GPIO94 001 = VBUS Routed to GPIO16 010 = MSTR_I2C_CLK

TABLE 43: PROGRAMMABLE FUNCTION 31 CONTROL

PF31_CTL OFFSET: 0C22h RESET = Depends on device and CFG_STRAP settings			PF31 Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always '0'
3:0	Select	R/W	000 = GPIO95 001 = MSTR_I2C_DATA 010 = I2S_CLK

TABLE 44: VENDOR ID LSB

VID_LSB OFFSET: 3000h RESET = 24h			USB2.0 Vendor ID LSB Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	VID_LSB	R/W	Least Significant Byte of the Hub Vendor ID. This is a 16-bit value that uniquely identifies the vendor of the user device (assigned by USB-Implementers Forum). The Microchip Vendor ID is 0424h.

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TABLE 45: VENDOR ID MSB

VID_MSB OFFSET: 3001h RESET = 04h			USB2.0 Vendor ID MSB Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	VID_MSB	R/W	Most Significant Byte of the Hub Vendor ID. This is a 16-bit value that uniquely identifies the vendor of the user device (assigned by USB-Implementors Forum). The Microchip Vendor ID is 0424h.

TABLE 46: PRODUCT ID LSB

PID_LSB OFFSET: 3002h RESET = XXh			USB2.0 Product ID LSB Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PID_LSB	R/W	Least Significant Byte of the Hub Product ID. This is a 16-bit value that the vendor can assign and uniquely identifies this product. The default value is dependent on the part as shown below: USB7202 = 02h USB7206 = 06h USB7250 = 50h USB7251 = 51h USB7252 = 52h USB7216/USB7256 = 56h

Note 1: If port disable straps are implemented, these values will automatically decrement by the number of ports disabled by strapping. For example, if a design that implements USB7216/USB7256 with two ports disabled by strapping, the Product ID (PID) will automatically change to 0x7254.

TABLE 47: PRODUCT ID MSB

PID_MSB OFFSET: 3003h RESET = 42h			USB2.0 Product ID MSB Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PID_MSB	R/W	Most Significant Byte of the Hub Product ID. This is a 16-bit value that the vendor can assign and uniquely identifies this product. The default value is shown below: All part numbers = 42h

Note 1: The USB2.0 hub Product ID MSB is assigned “42.” The USB3.2 equivalent Product ID descriptor MSB is assigned “72.” This allows simpler distinction between the USB2.0 portion of the hub and the USB3.2 portion of the hub.

TABLE 48: DEVICE ID LSB

DID_LSB OFFSET: 3004h RESET = Depends on device			Device ID LSB Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	DID_LSB	R/W	Least Significant Byte of the Hub Device ID. This is a 16-bit device release number in BCD format assigned by OEM. This value will vary by part number and firmware/configuration revision.

TABLE 49: DEVICE ID MSB

DID_MSB OFFSET: 3005h RESET = Depends on device			Device ID MSB Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	DID_MSB	R/W	Most Significant Byte of the Hub Device ID. This is a 16-bit device release number in BCD format assigned by OEM. This value will vary by part number and firmware/configuration revision.

TABLE 50: HUB CONFIGURATION DATA BYTE 1

HUB_CFG1 OFFSET: 3006h RESET = 9Bh			Hub Configuration Data Byte 1 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	SELF_BUS_PWR	R/W	Self or Bus Power. Selects between self-powered and bus-powered operation. The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to 100 mA maximum of upstream power prior to being configured by the host controller). When configured as a bus-powered device, the Microchip hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered Microchip hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system-dependent, and the OEM must ensure that the USB2.0 specifications are not violated. When configured as a self-powered device, less than 1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current. ‘0’ = Bus-powered operation ‘1’ = Self-powered operation
6	VSM_DISABLE	R/W	‘0’ = VSM messaging is supported. ‘1’ = VSM messaging is disabled. When VSM is disabled, all vendor-specific messaging to the hub endpoint will be ignored with no ill effect.
5	HS_DISABLE	R/W	High-Speed Disable. Disables the capability to attach as either a High-Speed or Full-Speed device, and forces attachment as Full-Speed only (i.e. no High-Speed support) ‘0’ = High-Speed/Full-Speed ‘1’ = Full-Speed-Only (High-Speed disabled!)
4	MTT_ENABLE	R/W	Multi-TT Enable. Enables one transaction translator per port operation. Selects between a mode where only one transaction translator is available for all ports (Single-TT) and a mode where each port gets a dedicated transaction translator (Multi-TT). The host may force Single-TT mode only. ‘0’ = Single TT for all ports ‘1’ = One TT per port (multiple TT’s supported)

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TABLE 50: HUB CONFIGURATION DATA BYTE 1 (CONTINUED)

HUB_CFG1 OFFSET: 3006h RESET = 9Bh			Hub Configuration Data Byte 1 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3	EOP_DISABLE	R/W	EOP Disable. Disables EOP generation of EOF1 when in Full-Speed mode. During FS operation only, this permits the hub to send EOP if no downstream traffic is detected at EOF1. See *Section 11.3.1* of the *USB 2.0 Specification* for additional details. Note that generation of an EOP at the EOF1 point may prevent a host controller (operating in FS mode) from placing the USB bus in suspend. '0' = An EOP is generated at the EOF1 point if no traffic is detected. '1' = EOP generation at EOF1 is disabled. This is a normal USB operation.
2:1	CURRENT_SNS	R/W	Overcurrent Sense. Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs). The ability to support current sensing on a port or ganged basis is hardware implementation dependent. 00 = Ganged sensing (all ports together). The OCS source select registers need to be updated to select the OCS ganged input. 01 = Individual port-by-port 1x = Overcurrent sensing not supported (must only be used with Bus- Powered configurations)
0	PORT_PWR	R/W	Port Power Switching. Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port-by-port basis (individual). The ability to support power enabling on a port or ganged basis is hardware implementation dependent. '0' = Ganged switching (all ports together) '1' = Individual port-by-port switching

TABLE 51: HUB CONFIGURATION DATA BYTE 2

HUB_CFG2 OFFSET: 3007h RESET = 28h			Hub Configuration Data Byte 2 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	Reserved	R/W	Reserved
5:4	OC_TIMER	R/W	Overcurrent Timer. Overcurrent Timer delay. This measures the minimum pulse width for which a pulse is considered valid. 00 = 50 ns 01 = 100 ns 10 = 200 ns 11 = 400 ns
3	COMPOUND	R/W	Compound Device. This allows the OEM to indicate that the hub is part of a compound device (See the USB specification for definition.). The applicable ports must also be defined as having a “Non-Removable Device.” When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. ‘0’ = No ‘1’ = Yes, the hub is part of a compound device.
2:0	Reserved	R/W	Always ‘0’

TABLE 52: HUB CONFIGURATION DATA BYTE 3

HUB_CFG3 OFFSET: 3008h RESET = 09h			Hub Configuration Data Byte 3 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	Reserved
3	PRTMAP_EN	R/W	Port Remapping Enable. This selects the method used by the hub to assign port numbers and disable ports. ‘0’ = Standard mode. Strap options or the following registers are used to define which ports are enabled, and the port mapped as Port ‘n’ on the hub is reported as Port ‘n’ to the host. Unless one of the ports is disabled, the higher numbered ports are remapped to report contiguous port numbers to the host. ‘1’ = Port Remap mode. The mode enables remapping via the registers defined below. Disable the LPM to use this feature in USB2 Hub Control.
2:1	Reserved	R/W	Always ‘0’
0	STRING_EN	R/W	Enables String Descriptor Support ‘0’ = String support disabled ‘1’ = String support enabled

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TABLE 53: USB2 HUB NON-REMOVABLE DEVICE

USB2_HUB_NRD OFFSET: 3009h RESET = Depends on device and CFG_NON_REM settings			USB2 Hub Non-Removable Device Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	HUB_NON_REM	R/W	Non-Removable Device. This indicates which physical ports include non-removable devices. ‘0’ = Port is removable. ‘1’ = Port is non-removable. Informs the host if one of the active ports has a permanent device that is non-detachable from the Hub. The device must provide its own descriptor data. Bit 7 = 1; PHYSICAL Port 7 is non-removable. Bit 6 = 1; PHYSICAL Port 6 is non-removable. Bit 5 = 1; PHYSICAL Port 5 is non-removable. Bit 4 = 1; PHYSICAL Port 4 is non-removable. Bit 3 = 1; PHYSICAL Port 3 is non-removable. Bit 2 = 1; PHYSICAL Port 2 is non-removable. Bit 1 = 1; PHYSICAL Port 1 is non removable. Bit 0 = Reserved, always = ‘0’ When using the CFG_NON_REM strap, the port configuration is selected by the resistor used as follows: 200K PD = All removable 200K PU = Port 1 non-removable 10K PD = Ports 1, 2 non-removable 10K PU = Ports 1, 2, 3 non-removable 10R PD = Ports 1, 2, 3, 4 non-removable 10R PU = Ports 1, 2, 3, 4, 5, 6 non-removable No resistor = Not allowed The default value of this register depends on the product number and GFG_NON_REM strap setting.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

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TABLE 54: PORT DISABLE – SELF-POWERED

PORT_DIS_S OFFSET: 300Ah RESET = Depends on device and port disable strap settings			Port Disable for Self-Powered Operation Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PORT_DIS_SELF	R/W	Port Disable Self-Powered. Disables 1 or more ports. ‘0’ = Port is available. ‘1’ = Port is disabled. During self-powered operation when PRTMAP_EN = 0, this selects the physical ports that are permanently disabled and are not available to be enabled or enumerated by a host controller. The ports can be disabled in any order. The internal logic automatically reports the correct number of enabled ports to the USB host and reorders the active ports to ensure proper function. When using the internal default option, the PRT_DIS[1:0] pins disable the appropriate ports. Bit 7 = 1; PHYSICAL Port 7 is disabled. Bit 6 = 1; PHYSICAL Port 6 is disabled. Bit 5 = 1; PHYSICAL Port 5 is disabled. Bit 4 = 1; PHYSICAL Port 4 is disabled. Bit 3 = 1; PHYSICAL Port 3 is disabled. Bit 2 = 1; PHYSICAL Port 2 is disabled. Bit 1 = 1; PHYSICAL Port 1 is disabled. Bit 0 = Reserved, always = ‘0’

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

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TABLE 55: PORT DISABLE – BUS-POWERED

PORT_DIS_B OFFSET: 300Bh RESET = Depends on device and port disable strap settings			Port Disable for Bus-Powered Operation Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PORT_DIS_BUS	R/W	Port Disable Bus-Powered. Disables 1 or more ports. ‘0’ = Port is available. ‘1’ = Port is disabled. During Bus-Powered operation, when PRTMAP_EN = 0, this selects the PHYSICAL ports that are permanently disabled and are not available to be enabled or enumerated by a host controller. The ports can be disabled in any order. The internal logic automatically reports the correct number of enabled ports to the USB host and reorders the active ports to ensure proper function. When using the internal default option, the PRT_DIS[1:0] pins disable the appropriate ports. Bit 7 = 1; PHYSICAL Port 7 is disabled. Bit 6 = 1; PHYSICAL Port 6 is disabled. Bit 5 = 1; PHYSICAL Port 5 is disabled. Bit 4 = 1; PHYSICAL Port 4 is disabled. Bit 3 = 1; PHYSICAL Port 3 is disabled. Bit 2 = 1; PHYSICAL Port 2 is disabled. Bit 1 = 1; PHYSICAL Port 1 is disabled. Bit 0 = Reserved, always = ‘0’

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 56: HUB MAX POWER – SELF-POWERED

H_MAXP_S OFFSET: 300Ch RESET = 00h			Max Current for Self-Powered Operation Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	MAX_PWR_SP	R/W	Max Power Self-Powered. Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors. The USB2.0 specification does not permit this value to exceed 100 mA.

TABLE 57: HUB MAX POWER – BUS-POWERED

H_MAXP_B OFFSET: 300Dh RESET = 50h			Max Current for Bus-Powered Operation Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	MAX_PWR_BP	R/W	Max Power Bus-Powered. Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors.

TABLE 58: HUB FEATURE CONTROLLER MAX CURRENT – SELF-POWERED

HC_MAXP_S OFFSET: 300Eh RESET = 00h			Hub Feature Controller Max Current for Self-Powered Operation Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	HC_MAX_C_SP	R/W	Hub Feature Controller Max Current Self-Powered. Value in 1 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. The USB2.0 specification does not permit this value to exceed 100 mA.

TABLE 59: HUB FEATURE CONTROLLER MAX CURRENT – BUS-POWERED

HC_MAXP_B OFFSET: 300Fh RESET = 50h			Hub Feature Controller Max Current for Bus-Powered Operation Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	HC_MAX_C_BP	R/W	Hub Feature Controller Max Current Bus-Powered. Value in 1 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.

TABLE 60: POWER-ON TIME REGISTER

PWR_ON_TIME OFFSET: 3010h RESET = 32h			Power-On Time Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	POWER_ON_TIME	R/W	Power-On Time. This is the length of time (in 2 ms intervals) between the point where the host begins to initiate a power-on sequence on a port and the point where power is good on that port. The system software uses this value to determine the waiting time for accessing a powered-on port.

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TABLE 61: USB2.0 HUB MANUFACTURER STRING INDEX REGISTER

MFR_STR_INDEX OFFSET: 3013h RESET = 01h			USB2.0 Hub Manufacturer String Index Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	MFR_STR_INDEX	R/W	Manufacturer String Index

TABLE 62: USB2.0 HUB PRODUCT STRING INDEX REGISTER

PRD_STR_INDEX OFFSET: 3014h RESET = 02h			USB2.0 Hub Product String Index Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PRD_STR_INDEX	R/W	Product String Index

TABLE 63: USB2.0 HUB SERIAL STRING INDEX REGISTER

SER_STR_INDEX OFFSET: 3015h RESET = 00h			USB2.0 Hub Serial String Index Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	SER_STR_INDEX	R/W	Serial String Index

TABLE 64: BATTERY CHARGING ENABLE STATUS REGISTER

BC_EN Offset: 30D0h RESET = XXh			Battery Charging Enable Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always '0'
6:1	BC_EN_STAT	R	'0' = Battery Charging is OFF '1' = Battery Charging is ON Bit 6 = Physical Port 6 Bit 5 = Physical Port 5 Bit 4 = Physical Port 4 Bit 3 = Physical Port 3 Bit 2 = Physical Port 2 Bit 1 = Physical Port 1 The default state of the register depends on the CFG_BC_EN strap setting. When using the CFG_BC_EN strap, the port configuration is selected by the resistor used as follows: 200K PD = Battery charging is disabled on all ports. 200K PU = Port 1 BC is enabled. 10K PD = Ports 1, and 2 BC are enabled. 10K PU = Ports 1, 2, and 3 BC are enabled. 10R PD = Ports 1, 2, 3, and 4 BC are enabled. 10R PU = Ports 1, 2, 3, 4, 5, and 6 BC are enabled. No resistor = Not allowed See **Note 1**.
0	Reserved	R	Always '0'

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 65: START OCS LOCKOUT TIMER REGISTER

OCS_LOCKOUT OFFSET: 30E1h RESET = 0Ah			Start OCS Lockout Timer Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	START_OCS_LOCK	R/W	This timer blocks OCS events after the port power is enabled and is specified in 1 ms increments.

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TABLE 66: PORT POWER STATUS

PORT_PWR_STAT OFFSET: 30E5h RESET = 00h			Port Power Status Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
7:1	BPRTPWR[4:1]	R	‘0’ = State of Port Power Enable is OFF ‘1’ = State of Port Power Enable is ON Bit 7 = Physical Port 7 Bit 6 = Physical Port 6 Bit 5 = Physical Port 5 Bit 4 = Physical Port 4 Bit 3 = Physical Port 3 Bit 2 = Physical Port 2 Bit 1 = Physical Port 1 See **Note 1**.
0	Reserved	R	Always ‘0’

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 67: USB2 TEST MODE REGISTER

USB2_TEST_MODE OFFSET: 30E6h RESET = 00h			USB2 Test Mode Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’
6:1	H_DN_STATE_PORT_TES	R	‘0’ = Port is not in a USB2.0 Test mode. Bit 6 = 1; Physical Port 6 is in a USB2.0 Test mode. Bit 5 = 1; Physical Port 5 is in a USB2.0 Test mode. Bit 4 = 1; Physical Port 4 is in a USB2.0 Test mode. Bit 3 = 1; Physical Port 3 is in a USB2.0 Test mode. Bit 2 = 1; Physical Port 2 is in a USB2.0 Test mode. Bit 1 = 1; Physical Port 1 is in a USB2.0 Test mode. See **Note 1**.
0	UP_STAT_TEST_MODE	R	‘0’ = Upstream port is not in a USB2.0 Test mode. ‘1’ = Upstream port is in a USB2.0 Test mode.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 68: LPM TURNAROUND TIMEOUT

HS_TRESP_TIMEOUT OFFSET: 30E7h RESET = 00h			LPM Turnaround Timeout Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
6:0	LPM_TIMEOUT	R/W	This register sets the number of clocks the LPM logic will wait before timing out an LPM transaction on a downstream port. When this register is left at '0', a default value of 0x25 is used. When this register holds a non-zero value, the register value is used.

TABLE 69: ENABLE OCS LEGACY REGISTER

ENABLE_OCS_LEGACY OFFSET: 30E9h RESET = 05h			Enable OCS Legacy Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do not modify.
2	ENABLE_OCS_LEGACY	R/W	—
1:0	Reserved	R	'0' = Allows the timer values to be programmable. Single-pulse OCS or double-pulse OCS detection is based on timer values as configured in OC_TIMER and OCS_MIN_WIDTH, respectively. '1' = Enables the Legacy mode of OCS detection. Timer registers are not programmable, and all timer values are set to the default value.

TABLE 70: OCS MINIMUM WIDTH REGISTER

OCS_MIN_WIDTH OFFSET: 30EAh RESET = 05h			OCS Minimum Width Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	OCS _MIN_WIDTH	R/W	Contains the minimum OCS pulse width required to detect an OCS event. This field provides a range from 0 to 5 milliseconds in 1 ms increments.

TABLE 71: OCS INACTIVE TIMER

OCS_INACTIVE_TIMER OFFSET: 30EBh RESET = 14h			OCS Inactive Timer After First OCS Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	OCS _INACTIVE	R/W	Contains the maximum delay between two consecutive OCS pulses to occur to register as an OCS event. This field provides a range from 0 to 255 milliseconds in 1 ms increments.

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TABLE 72: HUB PORT SWAP REGISTER

HUB_PRT_SWAP OFFSET: 30FAh RESET = 00h			Hub Port Swap Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
5:0	PRT_SWAP	R/W	Port Swap. Swaps the upstream and downstream USB DP and DM pins for ease of board routing to devices and connectors. '0' = USB D+ functionality is associated with the DP pin, and D– functionality is associated with the DM pin. '1' = USB D+ functionality is associated with the DM pin, and D– functionality is associated with the DP pin. Bit 5 = '1': Physical Port 5 DP/DM is swapped. Bit 4 = '1': Physical Port 4 DP/DM is swapped. Bit 3 = '1': Physical Port 3 DP/DM is swapped. Bit 2 = '1': Physical Port 2 DP/DM is swapped. Bit 1 = '1': Physical Port 1 DP/DM is swapped. Bit 0 = '1': Physical Port 0 (Upstream) Port DP/DM is swapped.
7:6	Reserved	R	Always '0'

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 73: USB2 HUB PORT REMAP 1-2 REGISTER

HUB_PRT_REMAP_12 OFFSET: 30FBh RESET = Depends on device and port disable strap options			USB2 Hub Port 1-2 Remap Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	PRT_2_MAP	R/W	0000b = Physical Port 2 is disabled. 0001b = Physical Port 2 is mapped to Logical Port 1. 0010b = Physical Port 2 is mapped to Logical Port 2. 0011b = Physical Port 2 is mapped to Logical Port 3. 0100b = Physical Port 2 is mapped to Logical Port 4. 0101b = Physical Port 2 is mapped to Logical Port 5. 0110b = Physical Port 2 is mapped to Logical Port 6. 0111b = Physical Port 2 is mapped to Logical Port 7. All other values default to 0000b value.
3:0	PRT_1_MAP	R/W	0000b = Physical Port 1 is disabled. 0001b = Physical Port 1 is mapped to Logical Port 1. 0010b = Physical Port 1 is mapped to Logical Port 2. 0011b = Physical Port 1 is mapped to Logical Port 3. 0100b = Physical Port 1 is mapped to Logical Port 4. 0101b = Physical Port 1 is mapped to Logical Port 5. 0110b = Physical Port 1 is mapped to Logical Port 6. 0111b = Physical Port 1 is mapped to Logical Port 7. All other values default to 0000b value.

Note 1: Writes to this register are disabled unless PRTMAP_EN bit in HUB_CFG_3 is set.

TABLE 74: USB2 HUB PORT REMAP 3-4 REGISTER

HUB_PRT_REMAP_34 OFFSET: 30FCh RESET = Depends on device and port disable strap options			USB2 Hub Port 3-4 Remap Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	PRT-4_MAP	R/W	0000b = Physical Port 4 is disabled. 0001b = Physical Port 4 is mapped to Logical Port 1. 0010b = Physical Port 4 is mapped to Logical Port 2. 0011b = Physical Port 4 is mapped to Logical Port 3. 0100b = Physical Port 4 is mapped to Logical Port 4. 0101b = Physical Port 4 is mapped to Logical Port 5. 0110b = Physical Port 4 is mapped to Logical Port 6. 0111b = Physical Port 4 is mapped to Logical Port 7. All other values default to 0000b value.
3:0	PRT-3_MAP	R/W	0000b = Physical Port 3 is disabled. 0001b = Physical Port 3 is mapped to Logical Port 1. 0010b = Physical Port 3 is mapped to Logical Port 2. 0011b = Physical Port 3 is mapped to Logical Port 3. 0100b = Physical Port 3 is mapped to Logical Port 4. 0101b = Physical Port 3 is mapped to Logical Port 5. 0110b = Physical Port 3 is mapped to Logical Port 6. 0111b = Physical Port 3 is mapped to Logical Port 7. All other values default to 0000b value.

Note 1: Writes to this register are disabled unless PRTMAP_EN bit in HUB_CFG_3 is set.

TABLE 75: USB2 HUB PORT REMAP 5-6 REGISTER

HUB_PRT_REMAP_56 OFFSET: 30FDh RESET = Depends on device and port disable strap options			USB2 Hub Port 5-6 Remap Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	PRT-6_MAP	R/W	0000b = Physical Port 6 is disabled. 0001b = Physical Port 6 is mapped to Logical Port 1. 0010b = Physical Port 6 is mapped to Logical Port 2. 0011b = Physical Port 6 is mapped to Logical Port 3. 0100b = Physical Port 6 is mapped to Logical Port 4. 0101b = Physical Port 6 is mapped to Logical Port 5. 0110b = Physical Port 6 is mapped to Logical Port 6. 0111b = Physical Port 6 is mapped to Logical Port 7. All other values default to 0000b value.

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TABLE 75: USB2 HUB PORT REMAP 5-6 REGISTER (CONTINUED)

HUB_PRT_REMAP_56 OFFSET: 30FDh RESET = Depends on device and port disable strap options			USB2 Hub Port 5-6 Remap Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	PRT-5_MAP	R/W	0000b = Physical Port 5 is disabled. 0001b = Physical Port 5 is mapped to Logical Port 1. 0010b = Physical Port 5 is mapped to Logical Port 2. 0011b = Physical Port 5 is mapped to Logical Port 3. 0100b = Physical Port 5 is mapped to Logical Port 4. 0101b = Physical Port 5 is mapped to Logical Port 5. 0110b = Physical Port 5 is mapped to Logical Port 6. 0111b = Physical Port 5 is mapped to Logical Port 7. All other values default to 0000b value.

Note 1: Writes to this register are disabled unless PRTMAP_EN bit in HUB_CFG_3 is set.

TABLE 76: USB2 HUB PORT REMAP 7 REGISTER

HUB_PRT_REMAP_7 OFFSET: 30FEh RESET = Depends on device and port disable strap options			USB2 Hub Port 7 Remap Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
3:0	PRT-7_MAP	R/W	0000b = Physical Port 7 is disabled. 0001b = Physical Port 7 is mapped to Logical Port 1. 0010b = Physical Port 7 is mapped to Logical Port 2. 0011b = Physical Port 7 is mapped to Logical Port 3. 0100b = Physical Port 7 is mapped to Logical Port 4. 0101b = Physical Port 7 is mapped to Logical Port 5. 0110b = Physical Port 7 is mapped to Logical Port 6. 0111b = Physical Port 7 is mapped to Logical Port 7. All other values default to 0000b value.

Note 1: Writes to this register are disabled unless PRTMAP_EN bit in HUB_CFG_3 is set.

TABLE 77: USB2 LINK STATE PORT 0-3

USB2_LINK_STATE1 OFFSET: 3100h RESET = FFh			USB2 Link State 1 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	L_STATE3	R	Indicates the state of Physical Downstream Port 3 00b = L0 Normal Operation 01b = L1 Sleep 10b = L2 Suspend 11b = L3 Off

TABLE 77: USB2 LINK STATE PORT 0-3 (CONTINUED)

USB2_LINK_STATE1 OFFSET: 3100h RESET = FFh			USB2 Link State 1 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
5:4	L_STATE2	R	Indicates the state of Physical Downstream Port 2 00b = L0 Normal Operation 01b = L1 Sleep 10b = L2 Suspend 11b = L3 Off
3:2	L_STATE1	R	Indicates the state of Physical Downstream Port 1 00b = L0 Normal Operation 01b = L1 Sleep 10b = L2 Suspend 11b = L3 Off
1:0	L_STATE0	R	Indicates the state of Physical Upstream Port 0 00b = L0 Normal Operation 01b = L1 Sleep 10b = L2 Suspend 11b = L3 Off

TABLE 78: USB2 LINK STATE PORT 4-7

USB2_LINK_STATE2 OFFSET: 3101h RESET = FFh			USB2 Link State 2 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	L_STATE7	R	Indicates the state of Physical Downstream Port 7 00b = L0 Normal Operation 01b = L1 Sleep 10b = L2 Suspend 11b = L3 Off
5:4	L_STATE6	R	Indicates the state of Physical Downstream Port 6 00b = L0 Normal Operation 01b = L1 Sleep 10b = L2 Suspend 11b = L3 Off
3:2	L_STATE5	R	Indicates the state of Physical Downstream Port 5 00b = L0 Normal Operation 01b = L1 Sleep 10b = L2 Suspend 11b = L3 Off
1:0	L_STATE4	R	Indicates the state of Physical Downstream Port 4 00b = L0 Normal Operation 01b = L1 Sleep 10b = L2 Suspend 11b = L3 Off

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TABLE 79: USB2 HUB CONTROL

USB2_HUB_CTL OFFSET: 3104h RESET = 00h			USB2 Hub Control Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:2	RESERVED	R	Reserved
1	LPM_DISABLE	R/W	Disables Link Power Management
0	RESET	R/W	Hub Reset downstream '0' = Hub is in Normal mode. '1' = Hub is kept in Reset.

TABLE 80: USB2 VERSION BCD[15:0]

USB2_BCDUSB OFFSET: 3108h RESET = 1002h			USB2 Version BCD Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
15:0	USBVCD[15:0]	R/W	USB Specification Release Number in BCD format

Note 1: 3108h-[15:8], 3109h-[7:0]

TABLE 81: HUB CONTROL PORTABLE TEST

CNTLP OFFSET: 318Ch RESET = 00h			Hub Control Portable Test Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	RESERVED	R	Reserved
3:1	EMBEDTEST	R/W	Embedded Host USB2 Compliance Testing modes. Enables USB2 test modes on USB ports. To facilitate embedded host compliance testing, the SOC may select any of the following test modes using the serial port interface instead of modifying the embedded host stack to accomplish the same modes using USB communication to the hub controller with standard SETUP packet commands. Both methods can be used for embedded host compliance testing with equivalent results. The test modes described below are related to *Section 7.1.20 of the USB 2.0 Specification* and associated errata. Encoded values match the low nibble of the PID asserted by the HS-OPT when it requests the host to enter the associated test mode. When the test mode is entered, the port will remain in the test mode until the SOC reverts the value of the register back to '000', or the hub is reset. 0 (000) = Default Operation – No Test mode asserted 1 (001) = TEST_SE0_NAK – The hub enters High-Speed receive and drives SE0 on the hub's downstream port, 2 (010) = TEST_J – The hub's downstream port enters High-Speed J state. 3 (011) = TEST_K – The hub's downstream port enters High-Speed K state. 4 (100) = TEST_PACKET – Sends test packets on downstream port. All others are reserved. The port in use is selected using the EMBED_TEST_PORT_SEL register.
0	Reserved	R	Reserved

TABLE 82: EMBEDDED HUB TEST PORT SELECT

EMBED_TEST_PORT_SEL OFFSET: 318Dh RESET = 00h			Hub Test Port Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	Reserved	R	Reserved
5:0	PORT_SEL[4:0]	R/W	Enables a port at the particular bit position. Any combination is permissible. Some examples are shown below: 00_0000 = Normal operation 00_0001 = Physical Downstream Port 1 00_0010 = Physical Downstream Port 2 00_0100 = Physical Downstream Port 3 00_1000 = Physical Downstream Port 4 01_0000 = Physical Downstream Port 5 00_0011 = Physical Downstream Port 1 and Port 2 00_0111 = Physical Downstream Port 1-3 00_1111 = Physical Downstream Port 1-4 11_1111 = Physical Downstream Port 1-6 To enable testing of the upstream port, use FlexConnect to swap Port 1 with the upstream port, and then run the EMBEDTEST on Port 1. See **Note 1**.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

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TABLE 83: USB2 HUB STATUS REGISTER

USB2_HUB_STAT OFFSET: 3194h RESET = 00h			USB2 Hub Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:1	USB2_DN_CONNECTED	R	USB Device connected on downstream port ’1’ = Device connected ‘0’ = No device connected Bit 7 = Physical Port 7 Bit 6 = Physical Port 6 Bit 5 = Physical Port 5 Bit 4 = Physical Port 4 Bit 3 = Physical Port 3 Bit 2 = Physical Port 2 Bit 1 = Physical Port 1 See **Note 1**.
0	USB2_HOST_DETECT	R	‘1’ = USB2 host connected ‘0’ = No USB2 host connected

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 84: USB2 DOWNSTREAM DEVICE SPEED[4-1]

USB2_DN_SPEED41 OFFSET: 3195h RESET = 00h			USB2 Downstream Device Speed1 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB2_DN4_DEV_SPEED	R	Indicates the USB2.0 state of Physical Downstream Port 4 00b = No connect 01b = LS 10b = FS 11b = HS
5:4	USB2_DN3_DEV_SPEED	R	Indicates the USB2.0 state of Physical Downstream Port 3 00b = No connect 01b = LS 10b = FS 11b = HS
3:2	USB2_DN2_DEV_SPEED	R	Indicates the USB2.0 state of Physical Downstream Port 2 00b = No connect 01b = LS 10b = FS 11b = HS
1:0	USB2_DN1_DEV_SPEED	R	Indicates the USB2.0 state of Physical Downstream Port 1 00b = No connect 01b = LS 10b = FS 11b = HS

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 85: USB2 DOWNSTREAM DEVICE SPEED[7-5]

USB2_DN_SPEED75 OFFSET: 3196h RESET = 00h			USB2 Downstream Device Speed2 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	Reserved	R	Always ‘0’

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

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TABLE 85: USB2 DOWNSTREAM DEVICE SPEED[7-5] (CONTINUED)

USB2_DN_SPEED75 OFFSET: 3196h RESET = 00h			USB2 Downstream Device Speed2 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
5:4	USB2_DN7_DEV_SPEED	R	Indicates the USB2.0 state of Physical Downstream Port 7 00b = No connect 01b = LS 10b = FS 11b = HS
3:2	USB2_DN6_DEV_SPEED	R	Indicates the USB2.0 state of Physical Downstream Port 6 00b = No connect 01b = LS 10b = FS 11b = HS
1:0	USB2_DN5_DEV_SPEED	R	Indicates the USB2.0 state of Physical Downstream Port 5 00b = No connect 01b = LS 10b = FS 11b = HS

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 86: USB2 SUSPEND INDICATOR

USB2_SUSP_IND OFFSET: 3197h RESET = 00h			USB2 Suspend Indicator Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:1	Reserved	R	Always ‘0.’ Do not modify.
0	USB_SUSPEND	R	Suspend indicator ‘0’ = Active. The hub is configured and operational. ‘1’ = Inactive. The hub is not configured, or configured and is suspended in Sleep state.

TABLE 87: USB3 HUB CONTROL

USB3_HUB_CTL OFFSET: 3840h RESET = 20h			USB3 Hub Control Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	Reserved	R	Always ‘0’
5	SCRAMBLE_EN	R/W	0b = Scrambling disabled 1b = Scrambling enabled
4	GANGE_OVER_CURRENT	R/W	0b = Individual Overcurrent 1b = Gang Overcurrent

TABLE 87: USB3 HUB CONTROL (CONTINUED)

USB3_HUB_CTL OFFSET: 3840h RESET = 20h			USB3 Hub Control Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3	BUS_POWERED	R/W	0b = Self-powered hub 1b = Bus-powered hub
2:0	Reserved	R	Always ‘0’

TABLE 88: USB3 HUB CONTROL 2

USB3_HUB_CTL2 OFFSET: 3841h RESET = 01h			USB3 Hub Control 2 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	HUB_DS_PROP_RST_CTRL	R/W	Reset propagation behavior 0b = If a propagated Reset ends up as warm Reset on DFP, CCS is made low. 1b = If a propagated Reset ends up as warm Reset on DFP, CCS remains high. This behavior matches with the Spec where CCS should be 1 in DSPOrt resetting state.
6	HUB_U3_RMT_WKUP_EN	R/W	Remote wakeup behavior 0b = Propagating DS wakeup does not depend on hub remote wakeup enable. 1b = Hub has to be enabled for remote wakeup for propagating DS wakeup.
5	HUB_U1_U2_EXIT_FAILED	R/W	U1, U2 exit failure control. 0b = On a U1/U2, exit fail link transitions to SS_INACTIVE. 1b = On a U1/U2, exit fail link transitions to Recovery.
4	Reserved	R	Always ‘0’
3	HUB_STALL_EP0_HALT	R/W	USB3 Hub Configuration bit. Stall behavior. 0b = Respond with Stall to SetfeatureHalt(EP0) 1b = Do not respond with Stall to SetfeatureHalt(EP0).
2	Reserved	R	Always ‘0’
1	USB3_HUB_VSM_PD_DIS-ABLE	R/W	0b = USB3 VSM messaging is enabled. For any unsupported commands, firmware will respond with Stall. 1b = USB3 VSM messaging is disabled (default). The hardware will respond with Stall to VSM commands.
0	USB3_HUB_ENABLE	R/W	This bit enables the USB3 hub. 0b = Hub held in Reset. 1b = Hub operational

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TABLE 89: USB3 HUB CONTROL 3

USB3_HUB_CTL3 OFFSET: 3842h RESET = 01h			USB3 Hub Control 3 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’
6	FORCE_U1_U2_FF	R/W	U1, U2 Timer Force bit. 0b = Downstream port U1/U2 timers follow normal operation. 1b = Downstream port U1/U2 timers will be forced to 0xFF.
5:4	HUB_SCALEDOWN	R/W	00b = Disables all scale-downs. Actual timing values are used. 01b = Enables scaled down SS timing and repeat values including: - Number of TxEq training sequences reduced to 8 - LFPS polling burst time reduced to 100 ns - LFPS warm Reset receive reduced to 30 us. 10b = No TxEq training sequences are sent; overrides bit 4. 11b = Enables bit 0 and bit 1 scale-down timing values.
3	DISABLE_U1_U2	R/W	0b = U1/U2 entry is enabled as per USB specification. 1b = The hub upstream and downstream ports do not request a low-power entry (U1/U2) and also reject any low-power entry request from their link partners.
2	DISABLE_P3	R/W	Not used in the latest RTL; done through override parameters
1	USB3_BIAS_ON	R/W	This bit forces the USB3 bias request on. Bias will not be shut down in global P3.
0	USB3_XTAL_ON	R/W	1b = The USB3 will not request crystal shutdown. Firmware should keep this bit set to ‘1’ at all times during normal operation.

TABLE 90: USB3 VBUS DEBOUNCE REGISTER

USB3_HUB_CTL3 OFFSET: 3843h RESET = 64h			USB3 VBUS Debounce Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	DEBOUNCE	R/W	Debounce period to be used for VBUS debounce for the USB3 Hub in VBUS Bypass mode. This register only takes effect if USB3_PASS_THRU is set in VBUS_PASS_THRU register. This value is in units of 1 ms. The default value is 100 ms.

TABLE 91: USB3 HUB CONTROL 4

USB3_HUB_CTL4 OFFSET: 3844h RESET = 01h			USB3 Hub Control 4 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’

TABLE 91: USB3 HUB CONTROL 4 (CONTINUED)

USB3_HUB_CTL4 OFFSET: 3844h RESET = 01h			USB3 Hub Control 4 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
6	WKUP_200US_N100US	R/W	This bit selects the wakeup timer for the clock: 1b = 200 µsec 0b = 100 µsec This register bit only has meaning when USB3 PLL is shut down.
5:4	Reserved	R	Always ‘0’
3	USB3_GANG_PWR_EN	R/W	0b = Individual power switching is enabled. 1b = Power to all USB3 downstream ports will be enabled if the host enables power to any one of the USB3 downstream ports. If a port is to be disabled in Gang mode, the PRT_SEL for that port must be set to 0x00 to disable port power.
2:1	Reserved	R	Always ‘0’
0	HUB_DS_POWR_SW_EN	R/W	0b = The USB 3.0 Downstream Facing Hub Port State Machine assumes DS power switches are not supported. 1b = The USB 3.0 Downstream Facing Hub Port State Machine assumes DS power switches are supported. This bit does not have any effect if HUB_DIS_DSPORT_ECR (bit 2) and HUB_DIS_VBUS_OFF_ECR (bit 1) are set.

TABLE 92: USB3 HUB CONTROL 5

USB3_HUB_CTL5 OFFSET: 3849h RESET = 00h			USB3 Hub Control 5 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’
6	DISABLE_HP_PENDING_FIX	R/W	0b = Pending HP count is reset when the link receives the LGOOD advertisement when it enters U0. Therefore, when the link comes back from Recovery due to Pending HP timeout to U0 and the LGOOD advertisement is successfully received from the link partner, the next Recovery due to Pending HP timeout will not be considered consecutive. 1b = The LInk goes to Inactive state when there are four consecutive recoveries due to the pending HP timeout even though the link might be stable in U0 and transfers data between these recoveries.

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TABLE 92: USB3 HUB CONTROL 5 (CONTINUED)

USB3_HUB_CTL5 OFFSET: 3849h RESET = 00h			USB3 Hub Control 5 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
5:4	US_SET_FTR_FC_EN	R/W	Places EP0 in flow control during the status stage of any of these commands: - set_feature[PORT_LINK_STATE] - set_feature[PORT_U2_TIMEOUT] - set_feature[FORCE_LINKPM_ACCEPT] Adding a timed hardware flow control during the status stage of such commands will keep the host from proceeding further. It will also avoid potential Race condition between the host setting the feature and the host getting a port status. The hub will send NRDY during the status stage and will start the timer. When the timer expires, the hub sends ERDY and then ACKs the STATUS TP. ‘00’ = Do not enter flow control ‘01’ = 1 msec ‘10’ = 4 msec ‘11’ = 16 msec
3	Reserved	R	Always ‘0’
2	LINK_ULORU2_UL_TIME-OUT_WKP_EN	R/W	0b = The DFP will not leave U1 or U2 if u1_timeout is updated through SetPortFeature(PORT_U1_TIMEOUT). 1b = The DFP will wake up from U1 or U2 when the host issues SetPortFeature (PORT_U1_TIMEOUT).
1	DS_LINK_CONFIG_FAIL_C-TRL	R/W	0b = If the downstream port did not finish link configuration, no packets will be sent to that port 1b = Packets are sent to the DFP even if the port didn't finish the link configuration.
0	US_LINKCONFIG_FAIL_C-TRL	R/W	0b = If upstream port did not finish link configuration, the packets to the DS ports will be discarded. 1b = UFP forwards the packets to the DFPs before it completes the link configuration.

TABLE 93: USB3 HUB STATUS REGISTER

USB30_HUB_STAT OFFSET: 3851h RESET = 00h			USB3 Hub Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0’
6	USB3_DN_CONNECT_DE-TECT_P6	R	USB3 device connected on Downstream Port 6 0b = Connected 1b = Not connected
5	USB3_DN_CONNECT_DE-TECT_P5	R	USB3 device connected on Downstream Port 5 0b = Connected 1b = Not connected

TABLE 93: USB3 HUB STATUS REGISTER (CONTINUED)

USB30_HUB_STAT OFFSET: 3851h RESET = 00h			USB3 Hub Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
4	USB3_DN_CONNECT_DETECT_P4	R	USB3 device connected on Downstream Port 4 0b = Connected 1b = Not connected
3	USB3_DN_CONNECT_DETECT_P3	R	USB3 device connected on Downstream Port 3 0b = Connected 1b = Not connected
2	USB3_DN_CONNECT_DETECT_P2	R	USB3 device connected on Downstream Port 2 0b = Connected 1b = Not connected
1	USB3_DN_CONNECT_DETECT_P1	R	USB3 device connected on Downstream Port 1 0b = Connected 1b = Not connected
0	USB3_HOST_DETECT	R	Hub upstream port connected to USB3 host 0b = No host connected 1b = USB3 host connected

TABLE 94: USB3 DOWNSTREAM SPEED INDICATOR REGISTER

USB30_HUB_DN_SPEED_IND1 OFFSET: 3852h RESET = 00h			USB3 Downstream Speed Indicator Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB3_DN4_DEV_SPEED	R	USB3 device speed on Downstream Port 1 01b = 5G 10b = 10G 11b = 20G All other values = No connection present
5:4	USB3_DN3_DEV_SPEED	R	USB3 device speed on Downstream Port 1 01b = 5G 10b = 10G 11b = 20G All other values = No connection present
3:2	USB3_DN2_DEV_SPEED	R	USB3 device speed on Downstream Port 1 01b = 5G 10b = 10G 11b = 20G All other values = No connection present

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TABLE 94: USB3 DOWNSTREAM SPEED INDICATOR REGISTER (CONTINUED)

USB30_HUB_DN_SPEED_IND1 OFFSET: 3852h RESET = 00h			USB3 Downstream Speed Indicator Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
1:0	USB3_DN1_DEV_SPEED	R	USB3 device speed on Downstream Port 1 01b = 5G 10b = 10G 11b = 20G All other values = No connection present

TABLE 95: USB3 DOWNSTREAM SPEED INDICATOR REGISTER 2

USB30_HUB_DN_SPEED_IND2 OFFSET: 3853h RESET = 00h			USB3 Downstream Speed Indicator Register 2 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:2	Reserved	R	Always ‘0’
1:0	USB3_DN5_DEV_SPEED	R	USB3 device speed on Downstream Port 5 01b = 5G 10b = 10G 11b = 20G All other values = No connection present

TABLE 96: USB3 SUSPEND INDICATOR

USB30_SUSP_IND OFFSET: 3857h RESET = 00h			USB3 Downstream Speed Indicator Register 2 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:1	Reserved	R	Always ‘0’
0	USB3_SUSP_IND	R	Suspend/resume indicator for USB3 hub controller 0b = USB3 is in functional state. 1b = USB3 is in suspend state.

TABLE 97: USB3 PORT REMAP ENABLE REGISTER

USB3_PRT_REMAP OFFSET: 3858h RESET = Depends on device			USB3 Port Remap Enable Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:1	Reserved	R	Always ‘0’
0	USB3_PRT_REMAP_EN	R/W	0b = Port remap is disabled. Port is mapped in ascending order. 1b = Port remap is enabled. DS ports are remapped in the order of Port Remap register values.

Note 1: If USB3_PRT_REMAP_EN =’1’, then the physical port can only be disabled through the USB3_PRT_REMAP registers. If USB3_PRT_REMAP_EN = ‘0’, then physical ports can only be disabled through PORT_CONFIGURATION_SEL_[7:1] registers.

TABLE 98: USB3 PORT REMAP PORTS 1 AND 2

USB3_PRT_REMAP_2AND1 OFFSET: 3860h RESET = Depends on device			USB3 Port Remap Ports 1 and 2 Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	PRT_2_MAP	R/W	0000b = Physical Port 2 is disabled. 0001b = Physical Port 2 is mapped to Logical Port 1. 0010b = Physical Port 2 is mapped to Logical Port 2. 0011b = Physical Port 2 is mapped to Logical Port 3. 0100b = Physical Port 2 is mapped to Logical Port 4. 0101b = Physical Port 2 is mapped to Logical Port 5. 0110b = Physical Port 2 is mapped to Logical Port 6. 0111b = Physical Port 2 is mapped to Logical Port 7.
3:0	PRT_1_MAP	R/W	0000b = Physical Port 1 is disabled. 0001b = Physical Port 1 is mapped to Logical Port 1. 0010b = Physical Port 1 is mapped to Logical Port 2. 0011b = Physical Port 1 is mapped to Logical Port 3. 0100b = Physical Port 1 is mapped to Logical Port 4. 0101b = Physical Port 1 is mapped to Logical Port 5. 0110b = Physical Port 1 is mapped to Logical Port 6. 0111b = Physical Port 1 is mapped to Logical Port 7.

TABLE 99: USB3 PORT REMAP PORTS 3 AND 4

USB3_PRT_REMAP_4AND3 OFFSET: 3861h RESET = Depends on device			USB3 Port Remap Ports 3 and 4 Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	PRT_4_MAP	R/W	0000b = Physical Port 4 is disabled. 0001b = Physical Port 4 is mapped to Logical Port 1. 0010b = Physical Port 4 is mapped to Logical Port 2. 0011b = Physical Port 4 is mapped to Logical Port 3. 0100b = Physical Port 4 is mapped to Logical Port 4. 0101b = Physical Port 4 is mapped to Logical Port 5. 0110b = Physical Port 4 is mapped to Logical Port 6. 0111b = Physical Port 4 is mapped to Logical Port 7.
3:0	PRT_3_MAP	R/W	0000b = Physical Port 3 is disabled. 0001b = Physical Port 3 is mapped to Logical Port 1. 0010b = Physical Port 3 is mapped to Logical Port 2. 0011b = Physical Port 3 is mapped to Logical Port 3. 0100b = Physical Port 3 is mapped to Logical Port 4. 0101b = Physical Port 3 is mapped to Logical Port 5. 0110b = Physical Port 3 is mapped to Logical Port 6. 0111b = Physical Port 3 is mapped to Logical Port 7.

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TABLE 100: USB3 PORT REMAP PORTS 5 AND 6

USB3_PRT_REMAP_6AND5 OFFSET: 3862h RESET = Depends on device			USB3 Port Remap Ports 5 and 6 Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	PRT_6_MAP	R/W	0000b = Physical Port 6 is disabled. 0001b = Physical Port 6 is mapped to Logical Port 1. 0010b = Physical Port 6 is mapped to Logical Port 2. 0011b = Physical Port 6 is mapped to Logical Port 3. 0100b = Physical Port 6 is mapped to Logical Port 4. 0101b = Physical Port 6 is mapped to Logical Port 5. 0110b = Physical Port 6 is mapped to Logical Port 6. 0111b = Physical Port 6 is mapped to Logical Port 7.
3:0	PRT_5_MAP	R/W	0000b = Physical Port 5 is disabled. 0001b = Physical Port 5 is mapped to Logical Port 1. 0010b = Physical Port 5 is mapped to Logical Port 2. 0011b = Physical Port 5 is mapped to Logical Port 3. 0100b = Physical Port 5 is mapped to Logical Port 4. 0101b = Physical Port 5 is mapped to Logical Port 5. 0110b = Physical Port 5 is mapped to Logical Port 6. 0111b = Physical Port 5 is mapped to Logical Port 7.

TABLE 101: USB3 PHY STATES REGISTER 1

USB3_PHY_STATE1 OFFSET: 3870h RESET = 00000000h			USB 3 PHY State Register 1 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	P_STATE3	R	Indicates the state of downstream PHY3 00b = P0 normal operation 01b = P1 low recovery time latency 10b = P2 longer recovery time latency 11b = P3 lowest Power state
5:4	P_STATE2	R	Indicates the state of downstream PHY2 00b = P0 normal operation 01b = P1 low recovery time latency 10b = P2 longer recovery time latency 11b = P3 lowest Power state
3:2	P_STATE1	R	Indicates the state of downstream PHY1 00b = P0 normal operation 01b = P1 low recovery time latency 10b = P2 longer recovery time latency 11b = P3 lowest Power state
1:0	P_STATE0	R	Indicates the state of upstream PHY0 00b = P0 normal operation 01b = P1 low recovery time latency 10b = P2 longer recovery time latency 11b = P3 lowest Power state

TABLE 102: USB3 PHY STATES REGISTER 2

USB3_PHY_STATE2 OFFSET: 3874h RESET = 00h			USB 3 PHY State Register 2 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always ‘0’
5:4	P_STATE6	R	Indicates state of downstream PHY6 00b = P0 normal operation 01b = P1 low recovery time latency 10b = P2 longer recovery time latency 11b = P3 lowest Power state
3:2	P_STATE5	R	Indicates state of downstream PHY5 00b = P0 normal operation 01b = P1 low recovery time latency 10b = P2 longer recovery time latency 11b = P3 lowest Power state
1:0	P_STATE4	R	Indicates state of upstream PHY4 00b = P0 normal operation 01b = P1 low recovery time latency 10b = P2 longer recovery time latency 11b = P3 lowest Power state

TABLE 103: USB GEN2 HUB CONTROL REGISTER

USB3_GEN2_HUB_CTRL_REG OFFSET: 392Ch Reset = 0x00000000			GEN2 Hub Control Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:14	Reserved	R	Always ‘0’
13	HOST_FORCE_GEN1_-SPEED_P5	R	Port 5 USB Super Speed link Gen1 Link Speed Control ‘0’ = Max Link Speed is Gen2. ‘1’ = Max Link Speed is Gen1.
12	HOST_FORCE_GEN1_-SPEED_P4	R	Port 4 USB Super Speed link Gen1 Link Speed Control ‘0’ = Max Link Speed is Gen2. ‘1’ = Max Link Speed is Gen1.
11	HOST_FORCE_GEN1_-SPEED_P3	R	Port 3 USB Super Speed link Gen1 Link Speed Control ‘0’ = Max Link Speed is Gen2. ‘1’ = Max Link Speed is Gen1.
10	HOST_FORCE_GEN1_-SPEED_P2	R	Port 2 USB Super Speed link Gen1 Link Speed Control ‘0’ = Max Link Speed is Gen2. ‘1’ = Max Link Speed is Gen1.
9	HOST_FORCE_GEN1_-SPEED_P1	R	Port 1 USB Super Speed link Gen1 Link Speed Control ‘0’ = Max Link Speed is Gen2. ‘1’ = Max Link Speed is Gen1.

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TABLE 103: USB GEN2 HUB CONTROL REGISTER (CONTINUED)

USB3_GEN2_HUB_CTRL_REG OFFSET: 392Ch Reset = 0x00000000			GEN2 Hub Control Register Base Address: BF80_0000h
8	HOST_FORCE_GEN1_-SPEED_P0	R	It is not recommended to modify this bit. Port 0 (upstream port) USB Super Speed link Gen1 Link Speed Control. 0 = Max Link Speed is Gen2. 1= Max Link Speed is Gen1.
7:0	Reserved	R	Always '0'

TABLE 104: PORT 0 (UPSTREAM) PORT POWER SELECT

PORT_CFG_SEL_0 OFFSET: 3C00h RESET = Depends on device			Physical Port 0 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:23	Reserved	R	Always ‘0.’ Do not modify.
22	ORIENTATION_POLARITY	R/W	This bit indicates/controls the Type-C orientation of the port. This register bit is controlled by the firmware and should not be modified externally under normal-use cases.
21	CC_ENABLE	R/W	This bit controls the Enable to CC Pin Detection logic. This should always be enabled for Type-C ports. This register bit is controlled by the firmware and should not be modified externally under normal-use cases.
20:16	Reserved	R	Always ‘0.’ Do not modify.
15	MUX_EN	R/W	Enables the internal MUX for Type-C routing of the USB3.1 signals. This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 0 = Port MUX disabled. 1 = Port MUX enabled.
14	Reserved	R	Always ‘0.’ Do not modify.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 104: PORT 0 (UPSTREAM) PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_0 OFFSET: 3C00h RESET = Depends on device			Physical Port 0 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
13:12	C_MUX_SEL[1:0]	R/W	Control mode for the MUX for Type-C routing of the USB3.1 signals. This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 00 = Firmware controls attach and orientation. (This mode is used for Power Delivery enabled ports.) 01 = Firmware controls C_ATTACH. Hardware logic controls ORIENTATION. (Used in custom application only) 10 = Firmware controls ORIENTATION, hardware logic controls C_ATTACH. (Used in custom application only) 11 = Hardware logic controls C_ATTACH and ORIENTATION. (This mode is used for standard Type-C ports with no PD enabled.)
11	C_SEL_BNA	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls which USB3.1 PHY is selected for the Type-C attach orientation. This bit is valid only if MUX_EN = 1 and PORT_TYPE = Type-C. 0 = PHY side ‘A’ is selected. 1 = PHY side ‘B’ is selected.
10	C_ATTACH	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls if a Type-C attach is detected. 0 = No Type-C attach 1 = Type-C attach detected.
9:8	PORT_TYPE	R/W	Indicates the type of USB receptacle used on the port 00 = Type-A with USB2 and USB3 01 = Type-C with USB2 and USB3 10 = Split. Type-A USB2 only, internal (embedded device) USB3 11 = Split. Type-C USB2 only, internal (embedded device) USB3
7	COMBINED _MODE	R/W	This should always be set to 1 for the standard-use case as both pins are always physically bonded out the same pin in the package. 0 = The Port Power and Overcurrent Sense functions use separate physical pins. 1 = The Port Power and Overcurrent Sense functions use the same physical pin.
6	GANG_PIN	R/W	When set, the port power will be connected to the GANG_PWR pin.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

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TABLE 104: PORT 0 (UPSTREAM) PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_0 OFFSET: 3C00h RESET = Depends on device			Physical Port 0 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
5	DISABLED	R/W	When set, it disables the port. Used to inform the USB hub that a port is permanently disabled.
4	PERMANENT	R/W	When set, it indicates that the port has a permanently attached device.
3:0	PRT_SEL	R/W	This selects the source for PRT_CTL1. 0000b = The port power is disabled. 0001b = The port is on if the USB2 port power is on (enable port power command received from USB2 host). 0010b = The port is on if the USB3 port power is on (enable port power command received from USB3 host). 0011b = The port is on if the USB2 or USB3 port power is on (enable port power command received from USB2 or USB3 host). 0100b = The port is on if the designated GPIO is on (change PRT_CTL pin to GPIO mode for external control via USB register write or SMBus/I^2C register write). All other values are reserved.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 105: PORT 1 PORT POWER SELECT

PORT_CFG_SEL_1 OFFSET: 3C04h RESET = Depends on device			Physical Port 1 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:23	Reserved	R	Always ‘0.’ Do not modify.
22	ORIENTATION_POLARITY	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls the Type-C orientation of the port.
21	CC_ENABLE	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit controls the Enable to CC Pin Detection logic. This should always be enabled for Type-C ports.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 105: PORT 1 PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_1 OFFSET: 3C04h RESET = Depends on device			Physical Port 1 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
20	AUTO_DETACH	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. When this bit is set, the MINIHOST_CONNECT bits will be set to 000b automatically when a device detach is detected.
19:17	MINIHOST_CONNECT[2:0]	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 000 = Neutral condition (Disconnected state) 001 = Port is connected to Mini-host. 010 = Port is connected to the USB2 hub in USB1.1 mode. 011 = Port is connected in USB2 mode. 100 = Port is connected in USB3.1 Gen 1 mode. Others are reserved.
16	MINI_HOST_ENABLE	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. ‘0’ = The port is a standard USB port connected to the USB hub. ‘1’ = The port is under control by the Mini-host.
15	MUX_EN	R/W	Enables the internal MUX for Type-C routing of the USB3.1 signals. This register bit is controlled by the firmware and should not be modified externally under normal-use cases. ‘0’ = Port MUX disabled ‘1’ = Port MUX enabled
14	Reserved	R	Always ‘0.’ Do not modify.
13:12	C_MUX_SEL[1:0]	R/W	Control mode for the MUX for Type-C routing of the USB3.1 signals. This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 00 = Firmware controls attach and orientation. (This mode is used for Power Delivery enabled ports.) 01 = Firmware controls C_ATTACH, hardware logic controls ORIENTATION. (Used in custom application only) 10 = Firmware controls ORIENTATION, hardware logic controls C_ATTACH. (Used in custom application only) 11 = Hardware logic controls C_ATTACH and ORIENTATION. (This mode is used for standard Type-C ports with no PD enabled.)

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

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TABLE 105: PORT 1 PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_1 OFFSET: 3C04h RESET = Depends on device			Physical Port 1 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
11	C_SEL_BNA	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls which USB3.1 PHY is selected for the Type-C attach orientation. This bit is valid only if MUX_EN = 1 and PORT_TYPE = Type-C. '0' = PHY side 'A' is selected. '1' = PHY side 'B' is selected.
10	C_ATTACH	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls if a Type-C attach is detected. '0' = No Type-C attach '1' = Type-C attach detected
9:8	PORT_TYPE	R/W	Indicates the type of USB receptacle used on the port. 00 = Type-A with USB2 and USB3 01 = Type-C with USB2 and USB3 10 = Split. Type-A USB2 only, internal (embedded device) USB3 11 = Split. Type-C USB2 only, internal (embedded device) USB3
7	COMBINED _MODE	R/W	This should always be set to '1' for the standard-use case as both pins are always physically bonded out the same pin in the package. '0' = The Port Power and Overcurrent Sense functions use separate physical pins. '1' = The Port Power and Overcurrent Sense functions use the same physical pin.
6	GANG_PIN	R/W	When set, the port power will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, it disables the port. Used to inform the USB hub that a port is permanently disabled.
4	PERMANENT	R/W	When set, it indicates that the port has a permanently attached device.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 105: PORT 1 PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_1 OFFSET: 3C04h RESET = Depends on device			Physical Port 1 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	PRT_SEL	R/W	This selects the source for PRT_CTL1. 0000b = The port power is disabled. 0001b = The port is on if the USB2 port power is on (enable port power command received from USB2 host). 0010b = The port is on if the USB3 port power is on (enable port power command received from USB3 host). 0011b = The port is on if the USB2 or USB3 port power is on (enable port power command received from USB2 or USB3 host). 0100b = The port is on if the designated GPIO is on (change PRT_CTL pin to GPIO mode for external control via USB register write or SMBus/I^2C register write). All other values are reserved.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 106: PORT 2 PORT POWER SELECT

PORT_CFG_SEL_2 OFFSET: 3C08h RESET = Depends on device			Physical Port 2 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:23	Reserved	R	Always ‘0.’ Do not modify.
22	ORIENTATION_POLARITY	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls the Type-C orientation of the port.
21	CC_ENABLE	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit controls the Enable to CC Pin Detection logic. This should always be enabled for Type-C ports.
20	AUTO_DETACH	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. When this bit is set, the MINIHOST_CONNECT bits will be set to 000b automatically when a device detach is detected.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

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TABLE 106: PORT 2 PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_2 OFFSET: 3C08h RESET = Depends on device			Physical Port 2 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
19:17	MINIHOST_CONNECT[2:0]	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 000 = Neutral condition (Disconnected state) 001 = The port is connected to Mini-host. 010 = The port is connected to the USB2 hub in USB1.1 mode. 011 = The port is connected in USB2 mode. 100 = The port is connected in USB3.1 Gen 1 mode. Others are reserved.
16	MINI_HOST_ENABLE	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. ‘0’ = The port is a standard USB port connected to the USB hub. ‘1’ = The port is under control by the Mini-host.
15	MUX_EN	R/W	Enables the internal MUX for Type-C routing of the USB3.1 signals. This register bit is controlled by the firmware and should not be modified externally under normal-use cases. ‘0’ = Port MUX disabled ‘1’ = Port MUX enabled
14	Reserved	R	Always ‘0.’ Do not modify.
13:12	C_MUX_SEL[1:0]	R/W	Control mode for the MUX for Type-C routing of the USB3.1 signals. This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 00 = Firmware controls attach and orientation. (This mode is used for Power Delivery enabled ports.) 01 = Firmware controls C_ATTACH, and hardware logic controls ORIENTATION. (Used in custom application only.) 10 = Firmware controls ORIENTATION, and hardware logic controls C_ATTACH. (Used in custom application only.) 11 = Hardware logic controls C_ATTACH and ORIENTATION. (This mode used for standard Type-C ports with no PD enabled.)
11	C_SEL_BNA	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls wherein USB3.1 PHY is selected for the Type-C attach orientation. This bit is valid only if MUX_EN = 1 and PORT_TYPE = Type-C. 0 = PHY side ‘A’ is selected. 1 = PHY side ‘B’ is selected.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 106: PORT 2 PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_2 OFFSET: 3C08h RESET = Depends on device			Physical Port 2 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
10	C_ATTACH	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls if a Type-C attach is detected. 0 = No Type-C attach 1 = Type-C attach detected
9:8	PORT_TYPE	R/W	Indicates the type of USB receptacle used on the port. 00 = Type-A with USB2 and USB3 01 = Type-C with USB2 and USB3 10 = Split. Type-A USB2 only, internal (embedded device) USB3 11 = Split. Type-C USB2 only, internal (embedded device) USB3
7	COMBINED _MODE	R/W	This should always be set to 1 for the standard-use case as both pins are always physically bonded out the same pin in the package. 0 = The Port Power and Overcurrent Sense functions use separate physical pins. 1 = The Port Power and Overcurrent Sense functions use the same physical pin.
6	GANG_PIN	R/W	When set, the port power will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, it disables the port. Used to inform the USB hub that a port is permanently disabled.
4	PERMANENT	R/W	When set, it indicates that the port has a permanently attached a device.
3:0	PRT_SEL	R/W	This selects the source for PRT_CTL2. 0000b = The port power is disabled. 0001b = The port is on if the USB2 port power is on. (Enables port power command received from USB2 host) 0010b = The port is on if the USB3 port power is on. (Enables port power command received from USB3 host). 0011b = The port is on if the USB2 or USB3 port power is on. (Enables port power command received from USB2 or USB3 host). 0100b = The port is on if the designated GPIO is on. (Changes PRT_CTL pin to GPIO mode for external control via USB register write or SMBus/I^2C register write) All other values are reserved.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

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TABLE 107: PORT 3 PORT POWER SELECT

PORT_CFG_SEL_3 OFFSET: 3C0Ch RESET = Depends on device			Physical Port 3 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:23	Reserved	R	Always '0.' Do not modify.
22	ORIENTATION_POLARITY	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates or controls the Type-C orientation of the port.
21	CC_ENABLE	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit controls the Enable to CC Pin Detection logic. This should always be enabled for Type-C ports.
20	AUTO_DETACH	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. When this bit is set, the MINIHOST_CONNECT bits will be set to 000b automatically when a device detach is detected.
19:17	MINIHOST_CONNECT[2:0]	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 000 = Neutral condition (Disconnected state) 001 = The port is connected to Mini-host. 010 = The port is connected to the USB2 hub in USB1.1 mode. 011 = The port is connected in USB2 mode. 100 = The port is connected in USB3.1 Gen 1 mode. Others are reserved.
16	MINI_HOST_ENABLE	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. '0' = The port is a standard USB port connected to the USB hub. '1' = The port is under control by the Mini-host.
15	MUX_EN	R/W	This enables the internal MUX for Type-C routing of the USB3.1 signals. This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 0 = Port MUX disabled 1 = Port MUX enabled
14	Reserved	R	Always '0.' Do not modify.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 107: PORT 3 PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_3 OFFSET: 3C0Ch RESET = Depends on device			Physical Port 3 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
13:12	C_MUX_SEL[1:0]	R/W	Control mode for the MUX for Type-C routing of the USB3.1 signals. This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 00 = Firmware controls attach and orientation. (This mode is used for Power Delivery enabled ports.) 01 = Firmware controls C_ATTACH, and hardware logic controls ORIENTATION. (Used in custom application only) 10 = Firmware controls ORIENTATION, and hardware logic controls C_ATTACH. (Used in custom application only) 11 = Hardware logic controls C_ATTACH and ORIENTATION. (This mode used for standard Type-C ports with no PD enabled.)
11	C_SEL_BNA	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls which USB3.1 PHY is selected for the Type-C attach orientation. This bit is valid only if MUX_EN = 1 and PORT_TYPE = Type-C. ‘0’ = PHY side ‘A’ is selected. ‘1’ = PHY side ‘B’ is selected.
10	C_ATTACH	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls if a Type-C attach is detected. ‘0’ = No Type-C attach ‘1’ = Type-C attach detected
9:8	PORT_TYPE	R/W	Indicates the type of USB receptacle used on the port 00 = Type-A with USB2 and USB3 01 = Type-C with USB2 and USB3 10 = Split. Type-A USB2 only, internal (embedded device) USB3 11 = Split. Type-C USB2 only, internal (embedded device) USB3
7	COMBINED _MODE	R/W	This should always be set to ‘1’ for the standard-use case as both pins are always physically bonded out the same pin in the package. ‘0’ = The Port Power and Overcurrent Sense functions use separate physical pins. ‘1’ = The Port Power and Overcurrent Sense functions use the same physical pin.
6	GANG_PIN	R/W	When set, the port power will be connected to the GANG_PWR pin.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

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TABLE 107: PORT 3 PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_3 OFFSET: 3C0Ch RESET = Depends on device			Physical Port 3 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
5	DISABLED	R/W	When set, it disables the port. Used to inform the USB hub that a port is permanently disabled.
4	PERMANENT	R/W	When set, it indicates that the port has a permanently attached device.
3:0	PRT_SEL	R/W	This selects the source for PRT_CTL3. 0000b = The port power is disabled. 0001b = The port is on if the USB2 port power is on. (enable port power command received from USB2 host). 0010b = The port is on if the USB3 port power is on. (enable port power command received from USB3 host). 0011b = The port is on if the USB2 or USB3 port power is on. (enable port power command received from USB2 or USB3 host). 0100b = The port is on if the designated GPIO is on. (change PRT_CTL pin to GPIO mode for external control via USB register write or SMBus/I^2C register write). All other values are reserved.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 108: PORT 4 PORT POWER SELECT

PORT_CFG_SEL_4 OFFSET: 3C10h RESET = Depends on device			Physical Port 4 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:23	Reserved	R	Always ‘0.’ Do not modify.
22	ORIENTATION_POLARITY	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls the Type-C orientation of the port.
21	CC_ENABLE	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit controls the Enable to CC Pin Detection logic. This should always be enabled for Type-C ports.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 108: PORT 4 PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_4 OFFSET: 3C10h RESET = Depends on device			Physical Port 4 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
20	AUTO_DETACH	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. When this bit is set, the MINIHOST_CONNECT bits will be set to 000b automatically when a device detach is detected.
19:17	MINIHOST_CONNECT[2:0]	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 000 = Neutral condition (Disconnected state) 001 = The port is connected to Mini-host. 010 = The port is connected to the USB2 hub in USB1.1 mode. 011 = The port is connected in USB2 mode. 100 = The port is connected in USB3.1 Gen 1 mode. Others are reserved.
16	MINI_HOST_ENABLE	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. ‘0’ = The port is a standard USB port connected to the USB hub. ‘1’ = The port is under control by the Mini-host.
15	MUX_EN	R/W	Enables the internal MUX for Type-C routing of the USB3.1 signals. This register bit is controlled by the firmware and should not be modified externally under normal-use cases. ‘0’ = Port MUX disabled ‘1’ = Port MUX enabled
14	Reserved	R	Always ‘0.’ Do not modify.
13:12	C_MUX_SEL[1:0]	R/W	Control mode for the MUX for Type-C routing of the USB3.1 signals. This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 00 = Firmware controls attach and orientation. (This mode used for Power Delivery enabled ports.) 01 = Firmware controls C_ATTACH, and hardware logic controls ORIENTATION. (Used in custom application only.) 10 = Firmware controls ORIENTATION, hardware logic controls C_ATTACH. (Used in custom application only.) 11 = Hardware logic controls C_ATTACH and ORIENTATION. (This mode used for standard Type-C ports with no PD enabled.)

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

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TABLE 108: PORT 4 PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_4 OFFSET: 3C10h RESET = Depends on device			Physical Port 4 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
11	C_SEL_BNA	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls which USB3.1 PHY is selected for the Type-C attach orientation. This bit is valid only if MUX_EN = 1 and PORT_TYPE = Type-C. ‘0’ = PHY side ‘A’ is selected. ‘1’ = PHY side ‘B’ is selected.
10	C_ATTACH	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls if a Type-C attach is detected. ‘0’ = No Type-C attach ‘1’ = Type-C attach detected
9:8	PORT_TYPE	R/W	Indicates the type of USB receptacle used on the port. 00 = Type-A with USB2 and USB3 01 = Type-C with USB2 and USB3 10 = Split. Type-A USB2 only, internal (embedded device) USB3 11 = Split. Type-C USB2 only, internal (embedded device) USB3
7	COMBINED _MODE	R/W	This should always be set to 1 for the standard-use case as both pins are always physically bonded out the same pin in the package. ‘0’ = The Port Power and Overcurrent Sense functions use separate physical pins. ‘1’ = The Port Power and Overcurrent Sense functions use the same physical pin.
6	GANG_PIN	R/W	When set, the port power will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, it disables the port. Used to inform the USB hub that a port is permanently disabled.
4	PERMANENT	R/W	When set, it indicates that the port has a permanently attached a device.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 108: PORT 4 PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_4 OFFSET: 3C10h RESET = Depends on device			Physical Port 4 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	PRT_SEL	R/W	This selects the source for PRT_CTL4. 0000b = The port power is disabled. 0001b = The port is on if the USB2 port power is on. (Enables port power command received from USB2 host) 0010b = The port is on if the USB3 port power is on. (Enables port power command received from USB3 host) 0011b = The port is on if the USB2 or USB3 port power is on. (Enables port power command received from USB2 or USB3 host) 0100b = The port is on if the designated GPIO is on. (Changes PRT_CTL pin to GPIO mode for external control via USB register write or SMBus/I^2C register write) All other values are reserved.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 109: PORT 5 PORT POWER SELECT

PORT_CFG_SEL_5 OFFSET: 3C14h RESET = Depends on device			Port 5 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:23	Reserved	R	Always ‘0.’ Do not modify.
22	ORIENTATION_POLARITY	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls the Type-C orientation of the port.
21	CC_ENABLE	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit controls the Enable to CC Pin Detection logic. This should always be enabled for Type-C ports.
20	AUTO_DETACH	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. When this bit is set, the MINIHOST_CONNECT bits will be set to 000b automatically when a device detach is detected.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

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TABLE 109: PORT 5 PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_5 OFFSET: 3C14h RESET = Depends on device			Port 5 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
19:17	MINIHOST_CONNECT[2:0]	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 000 = Neutral condition (Disconnected state) 001 = The port is connected to Mini-host. 010 = The port is connected to the USB2 hub in USB1.1 mode. 011 = The port is connected in USB2 mode. 100 = The port is connected in USB3.1 Gen 1 mode. Others are reserved.
16	MINI_HOST_ENABLE	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. ‘0’ = The port is a standard USB port connected to the USB hub. ‘1’ = The port is under control by the Mini-host.
15	MUX_EN	R/W	Enables the internal MUX for Type-C routing of the USB3.1 signals. This register bit is controlled by the firmware and should not be modified externally under normal-use cases. ‘0’ = Port MUX disabled ‘1’ = Port MUX enabled
14	Reserved	R	Always ‘0.’ Do not modify.
13:12	C_MUX_SEL[1:0]	R/W	Control mode for the MUX for Type-C routing of the USB3.1 signals. This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 00 = Firmware controls attach and orientation. (This mode used for Power Delivery enabled ports.) 01 = Firmware controls C_ATTACH, and hardware logic controls ORIENTATION. (Used in custom application only) 10 = Firmware controls ORIENTATION, and hardware logic controls C_ATTACH. (Used in custom application only) 11 = Hardware logic controls C_ATTACH and ORIENTATION. (This mode used for standard Type-C ports with no PD enabled.)
11	C_SEL_BNA	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls which USB3.1 PHY is selected for the Type-C attach orientation. This bit is valid only if MUX_EN = 1 and PORT_TYPE = Type-C. ‘0’ = PHY side ‘A’ is selected. ‘1’ = PHY side ‘B’ is selected.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

TABLE 109: PORT 5 PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_5 OFFSET: 3C14h RESET = Depends on device			Port 5 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
10	C_ATTACH	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls if a Type-C attach is detected. ‘0’ = No Type-C attach ‘1’ = Type-C attach detected
9:8	PORT_TYPE	R/W	Indicates the type of USB receptacle used on the port 00 = Type-A with USB2 and USB3 01 = Type-C with USB2 and USB3 10 = Split. Type-A USB2 only, internal (embedded device) USB3 11 = Split. Type-C USB2 only, internal (embedded device) USB3
7	COMBINED _MODE	R/W	This should always be set to ‘1’ for the standard-use case as both pins are always physically bonded out of the same pin in the package. ‘0’ = The Port Power and Overcurrent Sense functions use separate physical pins. ‘1’ = The Port Power and Overcurrent Sense functions use the same physical pin.
6	GANG_PIN	R/W	When set, the port power will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, it disables the port. Used to inform the USB hub that a port is permanently disabled.
4	PERMANENT	R/W	When set, it indicates that the port has a permanently attached device.
3:0	PRT_SEL	R/W	This selects the source for PRT_CTL5. 0000b = The port power is disabled. 0001b = The port is on if the USB2 port power is on. (enable port power command received from USB2 host) 0010b = The port is on if the USB3 port power is on. (enable port power command received from USB3 host). 0011b = The port is on if the USB2 or USB3 port power is on. (enable port power command received from USB2 or USB3 host). 0100b = The port is on if the designated GPIO is on. (Change PRT_CTL pin to GPIO mode for external control via USB register write or SMBus/I^2C register write). All other values are reserved.

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed and the settings are not impacted by logical port renumbering/remapping. See Section 6.0, "Physical and Logical Port Mapping" for details on the logical versus physical mapping for each device in this family.

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TABLE 110: PORT 6 PORT POWER SELECT

PORT_CFG_SEL_6 OFFSET: 3C04h RESET = Depends on device			Physical Port 6 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:23	Reserved	R	Always '0.' Do not modify.
22	ORIENTATION_POLARITY	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates or controls the Type-C orientation of the port.
21	CC_ENABLE	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit controls the Enable to CC Pin Detection logic. This should always be enabled for Type-C ports.
20	AUTO_DETACH	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. When this bit is set, the MINIHOST_CONNECT bits will be set to 000b automatically when a device detach is detected.
19:17	MINIHOST_CONNECT[2:0]	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 000 = Neutral condition (Disconnected state) 001 = The port is connected to Mini-host. 010 = The port is connected to the USB2 hub in USB1.1 mode. 011 = The port is connected in USB2 mode. 100 = The port is connected in USB3.1 Gen 1 mode. Others are reserved.
16	MINI_HOST_ENABLE	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 0 = The port is a standard USB port connected to the USB hub. 1 = The port is under control by the Mini-host.
15	MUX_EN	R/W	Enables the internal MUX for Type-C routing of the USB3.1 signals. This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 0 = Port MUX disabled 1 = Port MUX enabled
14	Reserved	R	Always '0.' Do not modify.
13:12	C_MUX_SEL[1:0]	R/W	Control mode for the MUX for Type-C routing of the USB3.1 signals. This register bit is controlled by the firmware and should not be modified externally under normal-use cases. 00 = Firmware controls attach and orientation. (This mode is used for Power Delivery enabled ports.) 01 = Firmware controls C_ATTACH, and hardware logic controls ORIENTATION. (Used in custom application only) 10 = Firmware controls ORIENTATION, and hardware logic controls C_ATTACH. (Used in custom application only) 11 = Hardware logic controls C_ATTACH and ORIENTATION. (This mode used for standard Type-C ports with no PD enabled.)

TABLE 110: PORT 6 PORT POWER SELECT (CONTINUED)

PORT_CFG_SEL_6 OFFSET: 3C04h RESET = Depends on device			Physical Port 6 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
11	C_SEL_BNA	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls which USB3.1 PHY is selected for the Type-C attach orientation. This bit is valid only if MUX_EN = 1 and PORT_TYPE = Type-C. 0 = PHY side 'A' is selected. 1 = PHY side 'B' is selected.
10	C_ATTACH	R/W	This register bit is controlled by the firmware and should not be modified externally under normal-use cases. This bit indicates/controls if a Type-C attach is detected. 0 = No Type-C attach 1 = Type-C attach detected
9:8	PORT_TYPE	R/W	Indicates the type of USB receptacle used on the port. 00 = Type-A with USB2 and USB3 01 = Type-C with USB2 and USB3 10 = Split. Type-A USB2 only, internal (embedded device) USB3 11 = Split. Type-C USB2 only, internal (embedded device) USB3
7	COMBINED _MODE	R/W	This should always be set to '1' for the standard-use case as both pins are always physically bonded out the same pin in the package. 0 = The Port Power and Overcurrent Sense functions use separate physical pins. 1 = The Port Power and Overcurrent Sense functions use the same physical pin.
6	GANG_PIN	R/W	When set, the port power will be connected to the GANG_PWR pin.
5	DISABLED	R/W	When set, it disables the port. Used to inform the USB hub that a port is permanently disabled
4	PERMANENT	R/W	When set, it indicates that the port has a permanently attached device.
3:0	PRT_SEL	R/W	This selects the source for PRT_CTL6. 0000b = The port power is disabled. 0001b = The port is on if the USB2 port power is on. (Enables port power command received from USB2 host.) 0010b = The port is on if the USB3 port power is on. (Enables port power command received from USB3 host.) 0011b = The port is on if the USB2 or USB3 port power is on. (Enables port power command received from USB2 or USB3 host). 0100b = The port is on if the designated GPIO is on. (Changes PRT_CTL pin to GPIO mode for external control via USB register write or SMBus/I^2C register write.) All other values are reserved.

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TABLE 111: USB PORT 1 OCS SOURCE SELECT

USB_OCS_SEL_1 OFFSET: 3C20h RESET = Depends on device			Port 1 OCS Source Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	OCS_SEL_USB3	R/W	This selects the source for the OCS signal for Port 1. 0000b = OCS is disabled. 0001b = OCS comes from USB3 Hub OCS pin. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.
3:0	OCS_SEL_USB2	R/W	This selects the source for the OCS signal for Port 1. 0000b = OCS is disabled. 0001b = OCS comes from USB2 Hub OCS logic. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.

TABLE 112: USB PORT 2 OCS SOURCE SELECT

USB_OCS_SEL_2 OFFSET: 3C24h RESET = Depends on device			Port 2 OCS Source Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	OCS_SEL_USB3	R/W	This selects the source for the OCS signal for Port 2. 0000b = OCS is disabled. 0001b = OCS comes from USB3 Hub OCS pin. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.
3:0	OCS_SEL_USB2	R/W	This selects the source for the OCS signal for Port 2. 0000b = OCS is disabled. 0001b = OCS comes from USB2 Hub OCS logic. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.

TABLE 113: USB PORT 3 OCS SOURCE SELECT

USB_OCS_SEL_3 OFFSET: 3C28h RESET = Depends on device			Port 3 OCS Source Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	This selects the source for the OCS signal for Port 3. 0000b = OCS is disabled. 0001b = OCS comes from USB3 Hub OCS pin. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.
3:0	OCS_SEL	R/W	This selects the source for the OCS signal for Port 3. 0000b = OCS is disabled. 0001b = OCS comes from USB2 Hub OCS logic. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.

TABLE 114: USB PORT 4 OCS SOURCE SELECT

USB_OCS_SEL_4 OFFSET: 3C2Ch RESET = Depends on device			Port 4 OCS Source Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	This selects the source for the OCS signal for Port 4. 0000b = OCS is disabled. 0001b = OCS comes from USB3 Hub OCS pin. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.
3:0	OCS_SEL	R/W	This selects the source for the OCS signal for Port 4. 0000b = OCS is disabled. 0001b = OCS comes from USB2 Hub OCS logic. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.

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TABLE 115: USB PORT 5 OCS SOURCE SELECT

USB_OCS_SEL_5 OFFSET: 3C30h RESET = Depends on device			Port 5 OCS Source Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	This selects the source for the OCS signal for Port 5. 0000b = OCS is disabled. 0001b = OCS comes from USB3 Hub OCS pin. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.
3:0	OCS_SEL	R/W	This selects the source for the OCS signal for Port 5. 0000b = OCS is disabled. 0001b = OCS comes from USB2 Hub OCS logic. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.

TABLE 116: USB PORT 6 OCS SOURCE SELECT

USB_OCS_SEL_6 OFFSET: 3034h RESET = Depends on device			Port 6 OCS Source Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	This selects the source for the OCS signal for Port 6. 0000b = OCS is disabled. 0001b = OCS comes from USB3 Hub OCS pin. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.
3:0	OCS_SEL	R/W	This selects the source for the OCS signal for Port 6. 0000b = OCS is disabled. 0001b = OCS comes from USB2 Hub OCS logic. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.

TABLE 117: USB PORT 7 OCS SOURCE SELECT

USB_OCS_SEL_7 OFFSET: 3038h RESET = 00h			Port 7 OCS Source Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	This selects the source for the OCS signal for Port 7. 0000b = OCS is disabled. 0001b = OCS comes from USB3 Hub OCS pin. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.
3:0	OCS_SEL	R/W	This selects the source for the OCS signal for Port 7. 0000b = OCS is disabled. 0001b = OCS comes from USB2 Hub OCS logic. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.

TABLE 118: VBUS_DET PASS-THROUGH REGISTER

VBUS_DET_PASS_THRU OFFSET: 3C40h RESET = 0Ah			VBUS_DET Pass-Through Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	Always ‘0’
3:2	USB3_PASS_THRU	R/W	00 = The VBUS detection to the USB3 Hub comes from internal PIO24. 01 = The VBUS detection to the USB3 Hub comes from the VBUS_DET pin. 10 = The VBUS detection to the USB3 Hub comes from VBUS_MON pin. 11 = Reserved
1:0	USB2_PASS_THRU	R/W	00 = The VBUS detection to the USB2 Hub comes from internal PIO32. 01 = The VBUS detection to the USB2 Hub comes from the VBUS_DET pin. 10 = The VBUS detection to the USB2 Hub comes from VBUS_MON pin. 11 = Reserved

TABLE 119: PORT 0 (UPSTREAM) STATUS REGISTER

PORT_STAT_REG_0 OFFSET: 3C50h RESET = 00h			Port 0 Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R/W	Always ‘0’
4	C_ATTACH_STATUS	R	The current state of the Type-C port attach status. ‘1’ = Type-C port currently has an attached device. ‘0’ = Type-C port does not have an attached device.

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TABLE 119: PORT 0 (UPSTREAM) STATUS REGISTER (CONTINUED)

PORT_STAT_REG_0 OFFSET: 3C50h RESET = 00h			Port 0 Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3	Reserved	R/W	Always ‘0’
2	USB_C_ATTACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.
1	Reserved	R/W	Always ‘0’
0	USB_C_DETACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.

TABLE 120: PORT 1 STATUS REGISTER

PORT_STAT_REG_1 OFFSET: 3C54h RESET = 00h			Port 1 Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R/W	Always’ 0’
4	C_ATTACH_STATUS	R	The current state of the Type-C port attach status ‘1’ = Type-C port currently has an attached device. ‘0’ = Type-C port does not have an attached device.
3	Reserved	R/W	Always ‘0’
2	USB_C_ATTACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.
1	Reserved	R/W	Always ‘0’
0	USB_C_DETACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.

TABLE 121: PORT 2 STATUS REGISTER

PORT_STAT_REG_2 OFFSET: 3C58h RESET = 00h			Port 2 Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R/W	Always ‘0’
4	C_ATTACH_STATUS	R	The current state of the Type-C port attach status 1 = Type-C port currently has an attached device. 0 = Type-C port does not have an attached device.
3	Reserved	R/W	Always ‘0’
2	USB_C_ATTACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.
1	Reserved	R/W	Always ‘0’
0	USB_C_DETACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.

TABLE 122: PORT 3 STATUS REGISTER

PORT_STAT_REG_3 OFFSET: 3C5Ch RESET = 00h			Port 3 Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R/W	Always ‘0’
4	C_ATTACH_STATUS	R	The current state of the Type-C port attach status 1 = Type-C port currently has an attached device. 0 = Type-C port does not have an attached device.
3	Reserved	R/W	Always ‘0’
2	USB_C_ATTACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.
1	Reserved	R/W	Always ‘0’
‘0	USB_C_DETACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.

TABLE 123: PORT 4 STATUS REGISTER

PORT_STAT_REG_4 OFFSET: 3C60h RESET = 00h			Port 4 Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R/W	Always ‘0’
4	C_ATTACH_STATUS	R	The current state of the Type-C port attach status ‘1’ = Type-C port currently has an attached device. ‘0’ = Type-C port does not have an attached device.
3	Reserved	R/W	Always ‘0’
2	USB_C_ATTACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.
1	Reserved	R/W	Always ‘0’
0	USB_C_DETACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.

TABLE 124: PORT 5 STATUS REGISTER

PORT_STAT_REG_5 OFFSET: 3C64h RESET = 00h			Port 5 Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R/W	Always ‘0’
4	C_ATTACH_STATUS	R	The current state of the Type-C port attach status. ‘1’ = Type-C port currently has an attached device. ‘0’ = Type-C port does not have an attached device.
3	Reserved	R/W	Always ‘0’
2	USB_C_ATTACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.
1	Reserved	R/W	Always ‘0’

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TABLE 124: PORT 5 STATUS REGISTER (CONTINUED)

PORT_STAT_REG_5 OFFSET: 3C64h RESET = 00h			Port 5 Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
0	USB_C_DETACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.

TABLE 125: PORT 6 STATUS REGISTER

PORT_STAT_REG_6 OFFSET: 3C68h RESET = 00h			Port 6 Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R/W	Always ‘0’
4	C_ATTACH_STATUS	R	The current state of the Type-C port attach status ‘1’ = Type-C port currently has an attached device. ‘0’ = Type-C port does not have an attached device.
3	Reserved	R/W	Always ‘0’
‘2	USB_C_ATTACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.
1	Reserved	R/W	Always ‘0’
0	USB_C_DETACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.

TABLE 126: PORT 7 STATUS REGISTER

PORT_STAT_REG OFFSET: 3C6Ch RESET = 00h			Port 7 Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R/W	Always ‘0’
4	C_ATTACH_STATUS	R	The current state of the Type-C port attach status ‘1’ = Type-C port currently has an attached device. ‘0’ = Type-C port does not have an attached device.
3	Reserved	R/W	Always ‘0’
2	USB_C_ATTACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.
1	Reserved	R/W	Always ‘0’
‘0	USB_C_DETACH	R	Set = 1 by hardware when USB Type-C attach detected. Cleared by the hardware if the port power is not enabled for this port.

TABLE 127: USB3 UPSTREAM TX PRE-DRIVER

SS_P0_AFE_TEST_IN4 OFFSET: 6086h RESET = 00h			USB3 Physical Port 0 TX Pre-Driver Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do no modify.

TABLE 127: USB3 UPSTREAM TX PRE-DRIVER (CONTINUED)

SS_P0_AFE_TEST_IN4 OFFSET: 6086h RESET = 00h			USB3 Physical Port 0 TX Pre-Driver Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
2:1	PRE_DRIVER	R/W	Physical Port 0 Transmitter Pre-Driver current adjust 00 = 100 µA (default biasing) 01 = 125 µA 10 = 87.5 µA 11 = 112.5 µA
0	Reserved	R	Reserved. Do no modify.

TABLE 128: USB 2.0 UPSTREAM RISE AND FALL ADJUSTMENT REGISTER

UP_RISEFALL_ADJ OFFSET: 60C8h RESET = 00h			USB 2.0 Upstream Rise/Fall Adjust Register Base Address: BF80_0000h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:2	HS_TX_RISEFALL_ADJUST	R/W	High-Speed TX rise/fall adjust 00 = Default 01 = +18% 10 = –18% 11 = –12%
1:0	LS_TX_RISEFALL_ADJUST	R/W	Low-Speed/Full-Speed TX rise/fall adjust 00 = Default 01 = +100% 10 = –30% 11 = –50%

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TABLE 129: USB PORT 0 BOOST REGISTER

HS_P0_BOOST OFFSET: 60CAh RESET = 00h			USB Port 0 Boost Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved. Do not modify.
2:0	HS_BOOST	R/W	HS Output Current 000b = Nominal 17.78 mA 001b = Decrease by 5% 010b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25% See **Note 1**.

Note 1: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] register if High-Speed disconnect issues are encountered.

TABLE 130: USB PORT 0 VARISENSE™ REGISTER

HS_P0_VSENSE OFFSET: 60CCh RESET = 00h			USB Port 0 VariSense™ Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b = Nominal (575 mV) threshold 01b = 625 mV threshold (+8.6%) 10b = 675 mV threshold (+17%) 11b = 700 mV threshold (+22%)
5:3	Reserved	R	Reserved. Do not modify.
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b = Nominal 100 mV Trip Point 001b = Decrease by 12.5 mV 010b = Decrease by 25 mV 011b = Decrease by 37.5 mV 100b = Decrease by 50 mV 101b = Decrease by 62.5 mV 110b = Increase by 25 mV 111b = Increase by 12.5 mV

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TABLE 131: USB3 UPSTREAM LTSSM STATE

SS_P0_LTSSM_State OFFSET: 61C0h RESET = 00h			USB3 Upstream Physical Port 0 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	Physical Port 0 LTSSM state 0000b = U0 (no substates) 0001b = U1 (no substates) 0010b = U2 (no substates) 0011b = U3 (no substates) 0100b = SS.Disabled (see substate below) 0101b = Rx.Detect (see substate below) 0110b = SS.Inactive (see substate below) 0111b = Polling (see substate below) 1000b = Recovery (see substate below) 1001b = HotReset (see substate below) 1010b = Compliance (no substates) 1011b = Loopback (no substates)

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TABLE 131: USB3 UPSTREAM LTSSM STATE (CONTINUED)

SS_P0_LTSSM_State OFFSET: 61C0h RESET = 00h			USB3 Upstream Physical Port 0 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	Physical Port 0 LTSSM substate. Undefined values are invalid. U0 substates: none U1 substates: 0x0 U1 POWER = PHY Power state P0 -> P1 request 0x1 U1_POWER_A = Wait for PHY power change done 0x2 U1_ACTIVE = Wait for remote/local U1 exit 0x3 U1_EXIT_LOC_RESP = Start U1 exit and wait for min response from remote partner 0x4 U1_EXIT_LOC_FIN = Locally initiated U1 exit; send min required U1 exit 0x5 U1_EXIT_REM = Remote initiated U1 exit; send min required U1 exit 0x6 U1_EXIT_P0 = PHY Power state P1 -> P0 request 0x7 U1_EXIT_P0_A = Wait for PHY power change P1 -> P0 done 0x8 U1_EXIT_DONE = U1 exit successful; U1 -> Recovery U2 substates: 0x0 U2_POWER = PHY Power state P0 -> P2 request 0x1 U2_POWER2 = Wait for PHY power change done 0x2 U2_ACTIVE = Wait for remote/local U2 exit 0x3 U2_ACTIVE_0 = Request to start receiver detection 0x4 U2_ACTIVE_1 = Wait for Receiver detection response 0x5 U2_EXIT_LOC_RESP = Start U2 exit and wait for min response from remote partner 0x6 U2_EXIT_LOC_FIN = Locally initiated U2 exit; send min required U2 exit 0x7 U2_EXIT_REM = Remote initiated U2 exit; send min required U2 exit 0x8 U2_EXIT_P0 = PHY Power state P2 -> P0 request 0x9 U2_EXIT_P0_A = Wait for PHY power change P1 -> P0 done 0xA U2_EXIT_DONE = U2 exit successful; U2 -> Recovery U3 substates: 0x0 U3_POWER = PHY Power state P0 -> P2/P3 request 0x1 U3_POWER3 = Wait for PHY power change done 0x2 U3_ACTIVE = Wait for remote/local U3 exit 0x3 U3_ACTIVE_0 = Request to start receiver detection 0x4 U3_ACTIVE_1 = Wait for receiver detection response 0x5 U3_EXIT_LOC_POW = PHY Power state P3 -> P0 -> P2 request 0x6 U3_EXIT_LOC_POW_A = Wait for PHY power change done 0x7 U3_EXIT_LOC_RESP = Start U3 exit and wait for min response from remote partner 0x8 U3_EXIT_LOC_FIN = Locally initiated U3 exit; send min required U3 exit 0x9 U3_EXIT_REM_POW = PHY Power state P3 -> P0 -> P2 request 0xA U3_EXIT_REM_POW_A = Wait for PHY power change done 0xB U3_EXIT_REM = Remote initiated U3 exit; send min required U3 exit 0xC U3_EXIT_P0 = PHY Power state P2/P3 -> P0 request 0xD U3_EXIT_P0_A = Wait for PHY power change P2/P3 -> P0 done 0xE U3_EXIT = Received remote/local U3 exit 0xF U3_EXIT_DONE U3 = Exit successful; U3 -> Recovery

TABLE 131: USB3 UPSTREAM LTSSM STATE (CONTINUED)

SS_P0_LTSSM_State OFFSET: 61C0h RESET = 00h			USB3 Upstream Physical Port 0 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	SS.Disabled substates: 0x0 ESSD_POWER3 = PHY Power state P2/P3 request 0x1 ESSD_POWER3A = Wait for PHY power change done 0x2 ESSD_MAIN = Wait for RUN/STOP bit 0x3 ESSD_RATE = Wait for rate change 0x4 ESSD_POWER2 = Wait for PHY Power state P2/P3 request Rx.Detect substates: 0x0 RXD_INIT = PHY Power state P2 request 0x1 RXD_POWER2 = Wait for PHY power change done 0x2 RXD_RESET = Warm Reset 0x3 RXD_ACTIVE0 = Request to start receiver detection 0x4 RXD_ACTIVE1 = Wait for receiver detection response 0x5 RXD_QUIET = Wait for 12 ms-timer timeout 0x6 RXD_RATE = Wait for rate change SS.Inactive substates: 0x0 ESSI_RESET = PHY Power state P0 -> P2 request 0x1 ESSI_POWER2 = Wait for PHY power change done 0x2 ESSI_QUIET0 = Start 12 ms timer 0x3 ESSI_QUIET1 = Wait for 12 ms-timer timeout 0x4 ESSI_DIS_DET0 = Request to start receiver detection 0x5 ESSI_DIS_DET1 = Wait for receiver detection response Polling substates: 0x0 POLL_RESET = PHY Power state P0 request 0x1 POLL_POWER0 = Wait for PHY power change done 0x2 POLL_LFPS = Send/Receive Poll; LFPS 0x3 POLL_LFPSPLUS = Send/Receive SCD2 0x4 POLL_PMATCH = Send/Receive LBPM PHY capability 0x5 POLL_PCONFIG = Change rate and Send/Receive LBPM PHY ready 0x6 POLL_UPDATE_RATE = Wait for rate changed 0x7 POLL_RXEQ = Send/Receive TSEQ Training set 0x8 POLL_ACTIVE = Send/Receive TS1 Training set 0x9 POLL_CONFIG = Send/Receive TS2 Training set 0xA POLL_IDLE = Send/Receive Logical IDLE symbols Recovery substates: 0x0 RECOV_RESET = PHY Power state P0 request 0x1 RECOV_POWER0 = Wait for PHY power change done 0x2 RECOV_ACTIVE = Send/Receive TS1 Training set 0x3 RECOV_CONFIG = Send/Receive TS2 Training set 0x4 RECOV_IDLE = Send/Receive Logical IDLE symbols HotReset substates: 0x0 HRESET_RST = Request TCRRL to send TS2 0x1 HRESET_GO = Start 12 ms Timer 0x2 HRESET_ACT1 = Send/Receive TS1 Training set with Reset bit 0x3 HRESET_ACT2 = Send/Receive TS1 Training set without Reset bit 0x4 HRESET_EXIT = Send/Receive Logical IDLE symbols

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TABLE 131: USB3 UPSTREAM LTSSM STATE (CONTINUED)

SS_P0_LTSSM_State OFFSET: 61C0h RESET = 00h			USB3 Upstream Physical Port 0 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	Compliance substates - none Loopback substates: 0x0 LPBK_IDLE = Wait for Loop back start request 0x1 LPBK_MASTER = Host mode; wait for Loopback Exit request 0x2 LPBK_SLAVE = Client mode; wait for Loopback Exit request 0x3 LPBK_EXIT_LOC_RESP = Start Loopback exit and wait for minimum response from remote partner

TABLE 132: USB3 UPSTREAM DC TEST REGISTER

SS_UP_TEST_PIPE_DC OFFSET: 61C1h RESET = 00h			USB3 Upstream Physical Port 0 DC Test Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DE-TR_LPBK	R/W	Transmit Detect Receiver and Loopback mode. This signal is synchronous to PCLK in P0, P1, and P2 modes and asynchronous in P3 mode. This is used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINA-TION	R/W	Receiver Termination Control. This signal is asynchronous. It controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	Reserved	R	Always ‘0’
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. ‘0’ = Full Swing ‘1’ = Low Swing
2	PIPE_TX-C_DRIVE_HI GH	R/W	Sets the DC state of the TX output 0: TXP = 0, TXN = 1 1: TXP = 1, TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enables Transmitter DC Drive mode
0	PIPE_TX_ELEC_I-DLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with pow-er_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either Normal Transmit mode, Electrical Idle, LFPS Transmission, or Receiver Detection).

TABLE 133: USB3 UPSTREAM TX TEST PATTERN REGISTER

SS_UP_TEST_PIPE_TX_PAT OFFSET: 61C3h RESET = 00h			USB3 Upstream Physical Port 0 TX Pattern Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’

TABLE 133: USB3 UPSTREAM TX TEST PATTERN REGISTER (CONTINUED)

SS_UP_TEST_PIPE_TX_PAT OFFSET: 61C3h RESET = 00h			USB3 Upstream Physical Port 0 TX Pattern Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. 0 = Disable pattern generator (Normal mode. Transmit data driven over the tx_data interface) 1 = Enable pattern generator
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. Gen1 mode: 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 = CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = Custom CP9 (TS1 + Random data + 1 SKP every 354 symbols) 10 = Custom CP10 (TS1 + 1 SKP every 354 symbols) 11 = Custom CP11 (TSEQ repeated) 12 to 15 = Reserved Gen2 mode: 0 = Spec CP9 (Pseudo random data) 1 = Spec CP10 (AAh, Nyquist, not 128b132b encoded) 2 = Spec CP11 (CCh, Nyquist/2, not 128b132b encoded) 3 = Spec CP12 (LFSR15, not 128b132b encoded) 4 = Spec CP13 (64 1s / 64 0s, w/ pre, no de) 5 = Spec CP14 (64 1s / 64 0s, no pre, w/ de) 6 =Spec CP15 (64 1s / 64 0s, w/ pre, w/ de) 7 = Spec CP16 (64 1s / 64 0s, no pre, no de) 8 = Custom CP17 (Random data + SYNC OS every 16 data blocks for the first 800 blocks and then once every 14K data blocks + 3 SKP blocks every 115 blocks) 9 = Custom CP18 (Random data + SYNC OS every 32 data blocks + 2 SKP blocks every 80 blocks) 10 to 15 = Reserved

TABLE 134: USB3 UPSTREAM TX_MARGIN

SS_UP_TEST_PIPE_CTL_0 OFFSET: 61D0h RESET = 00h			USB3 Upstream Physical Port 0 TX Margin Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0.’ Do not modify.

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TABLE 134: USB3 UPSTREAM TX_MARGIN (CONTINUED)

SS_UP_TEST_PIPE_CTL_0 OFFSET: 61D0h RESET = 00h			USB3 Upstream Physical Port 0 TX Margin Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
6:4	PIPE_TX_MARGIN[2:0]	R/W	Physical Port 1 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 = +33% 100 = –67% 101 = –64% 110 = –61% 111 = –57%
3:0	Reserved	R	Always ‘0.’ Do not modify.

TABLE 135: USB3 UPSTREAM GEN1 DEEMPHASIS

SS_P0_PIPE_TX_DEEMPH_CTL OFFSET: 62A0h RESET = 40030C1h			USB3 Upstream Physical Port 0 Gen1 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:27	Reserved	R	Always ‘0’
26	USB3_PIPE_DEEM-PH_POST_EN	R/W	TX Post-Emphasis enable for Gen1
25	USB3_PIPE_DEEM-PH_PRE_EN	R/W	TX Pre-Emphasis enable for Gen1
24:14	Reserved	R	Always ‘0’
13:12	POST_FFE_CONTROL	R/W	00 = +2.7 dB from default 01 = +1.8 dB from default 10 = +0.9 dB from default 11 = Default (–3.8 dB)
11:8	Reserved	R	Always ‘0’
7:6	TX_SWING	R/W	0 = 526 mV 1 = 687 mV 2 = 857 mV 3 = 970 mV(default)
5:2	Reserved	R	Always ‘0’
1:0	PRE_FFE_CONTROL	R/W	00 = –1.5 dB from default 01 = –1 dB from default 10 = –0.5 dB from default 11 = Default (2 dB)

TABLE 136: USB3 UPSTREAM GEN2 DEEMPHASIS

SS_P0_PIPE_TX_DEEMP_GEN2_CTL OFFSET: 62B8h RESET = 60030C1h			USB3 Upstream Physical Port 0 Gen2 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:27	Reserved	R	Always ‘0’
26	USB3_PIPE_DEEMPH_-GEN2_POST_EN	R/W	TX Post-Emphasis enable for Gen2

TABLE 136: USB3 UPSTREAM GEN2 DEEMPHASIS (CONTINUED)

SS_P0_PIPE_TX_DEEMP_GEN2_CTL OFFSET: 62B8h RESET = 60030C1h			USB3 Upstream Physical Port 0 Gen2 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
25	USB3_PIPE_DEEMPH_-GEN2_PRE_EN	R/W	TX Pre-Emphasis enable for Gen2
24:14	Reserved	R	Always ‘0’
13:12	POST_FFE_CONTROL	R/W	00 = +2.7 dB from default 01 = +1.8 dB from default 10 = +0.9 dB from default 11 = Default (–3.1 dB)
11:8	Reserved	R	Always ‘0’.
7:6	TX_SWING	R/W	0 = 526 mV 1 = 687 mV 2 = 857 mV 3 = 970 mV (Default)
5:2	Reserved	R	Always ‘0’
1:0	PRE_FFE_CONTROL	R/W	00 = –1.5 dB from default 01 = –1 dB from default 10 = –0.5 dB from default 11 = Default (2 dB)

TABLE 137: USB3 PORT 1 TX PRE-DRIVER

SS_P1_AFE_TEST_IN4 OFFSET: 6486h RESET = 00h			USB3 Physical Port 1 TX Pre-Driver Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do no modify.
2:1	PRE_DRIVER	R/W	Physical Port 1 Transmitter Pre-Driver current adjust 00 = 100A (default biasing) 01 = 125 µA 10 = 87.5 µA 11 = 112.5 µA
0	Reserved	R	Reserved. Do no modify.

TABLE 138: USB 2.0 PORT 1 RISE AND FALL ADJUSTMENT REGISTER

P1_RISEFALL_ADJ OFFSET: 64C8h RESET = 00h			USB 2.0 Port 1 Rise/Fall Adjust Register Base Address: BF80_0000h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:2	HS_TX_RISEFALL_ADJUST	R/W	High-Speed TX rise/fall adjust 00 = Default 01 = +18% 10 = –18% 11 = –12%

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TABLE 138: USB 2.0 PORT 1 RISE AND FALL ADJUSTMENT REGISTER (CONTINUED)

P1_RISEFALL_ADJ OFFSET: 64C8h RESET = 00h			USB 2.0 Port 1 Rise/Fall Adjust Register Base Address: BF80_0000h
BIT	**Name**	**R/W**	**Description**
1:0	LS_TX_RISEFALL_ADJUST	R/W	Low-Speed/Full-Speed TX rise/fall adjust 00 = Default 01 = +100% 10 = –30% 11 = –50%

TABLE 139: USB PORT 1 BOOST REGISTER

HS_P1_BOOST OFFSET: 64CAh RESET = 00h			USB Port 1 Boost Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved. Do not modify.
2:0	HS_BOOST	R/W	HS Output Current 000b = Nominal 17.78 mA 001b = Decrease by 5% 010b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25% See **Note 1**.

Note 1: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] register if High-Speed disconnect issues are encountered.

TABLE 140: USB PORT 1 VARISENSE™ REGISTER

HS_P1_VSENSE OFFSET: 64CCh RESET = 00h			USB Port 1 VariSense™ Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b = Nominal (575 mV) threshold 01b = 625 mV threshold (+8.6%) 10b = 675 mV threshold (+17%) 11b = 700 mV threshold (+22%)
5:3	Reserved	R	Reserved. Do not modify.

TABLE 140: USB PORT 1 VARISENSE™ REGISTER (CONTINUED)

HS_P1_VSENSE OFFSET: 64CCh RESET = 00h			USB Port 1 VariSense™ Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b = Nominal 100 mV Trip Point 001b = Decrease by 12.5 mV 010b = Decrease by 25 mV 011b = Decrease by 37.5 mV 100b = Decrease by 50 mV 101b = Decrease by 62.5 mV 110b = Increase by 25 mV 111b = Increase by 12.5 mV

TABLE 141: USB3 PORT 1 LTSSM STATE

SS_P1_LTSSM_State OFFSET: 65C0h RESET = 00h			USB3 Physical Port 1 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	Physical Port 1 LTSSM state. 0000b = U0 (no substates) 0001b = U1 (no substates) 0010b = U2 (no substates) 0011b = U3 (no substates) 0100b = SS.Disabled (see substate below) 0101b = Rx.Detect (see substate below) 0110b = SS.Inactive (see substate below) 0111b = Polling (see substate below) 1000b = Recovery (see substate below) 1001b = HotReset (see substate below) 1010b = Compliance (no substates) 1011b = Loopback (no substates)

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TABLE 141: USB3 PORT 1 LTSSM STATE (CONTINUED)

SS_P1_LTSSM_State OFFSET: 65C0h RESET = 00h			USB3 Physical Port 1 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	Physical Port 1 LTSSM substate. Undefined values are invalid. U0 substates: none U1 substates: 0x0 U1 POWER = PHY Power state P0 -> P1 request 0x1 U1_POWER_A = Wait for PHY power change done 0x2 U1_ACTIVE = Wait for remote/local U1 exit 0x3 U1_EXIT_LOC_RESP = Start U1 exit and wait for min response from remote partner 0x4 U1_EXIT_LOC_FIN = Locally initiated U1 exit; send min required U1 exit 0x5 U1_EXIT_REM = Remote initiated U1 exit; send min required U1 exit 0x6 U1_EXIT_P0 = PHY Power state P1 -> P0 request 0x7 U1_EXIT_P0_A = Wait for PHY power change P1 -> P0 done 0x8 U1_EXIT_DONE = U1 exit successful; U1 -> Recovery U2 substates: 0x0 U2_POWER = PHY Power state P0 -> P2 request 0x1 U2_POWER2 = Wait for PHY power change done 0x2 U2_ACTIVE = Wait for remote/local U2 exit 0x3 U2_ACTIVE_0 = Request to start receiver detection 0x4 U2_ACTIVE_1 = Wait for receiver detection response 0x5 U2_EXIT_LOC_RESP = Start U2 exit and wait for min response from remote partner 0x6 U2_EXIT_LOC_FIN = Locally initiated U2 exit; send min required U2 exit 0x7 U2_EXIT_REM = Remote initiated U2 exit; send min required U2 exit 0x8 U2_EXIT_P0 PHY = Power state P2 -> P0 request 0x9 U2_EXIT_P0_A = Wait for PHY power change P1 -> P0 done 0xA U2_EXIT_DONE U2 = Exit successful; U2 -> Recovery U3 substates: 0x0 U3_POWER = PHY Power state P0 -> P2/P3 request 0x1 U3_POWER3 = Wait for PHY power change done 0x2 U3_ACTIVE = Wait for remote/local U3 exit 0x3 U3_ACTIVE_0 = Request to start receiver detection 0x4 U3_ACTIVE_1 = Wait for receiver detection response 0x5 U3_EXIT_LOC_POW = PHY Power state P3 -> P0 -> P2 request 0x6 U3_EXIT_LOC_POW_A = Wait for PHY power change done 0x7 U3_EXIT_LOC_RESP = Start U3 exit and wait for min response from remote partner 0x8 U3_EXIT_LOC_FIN = Locally initiated U3 exit; send min required U3 exit 0x9 U3_EXIT_REM_POW = PHY Power state P3 -> P0 -> P2 request 0xA U3_EXIT_REM_POW_A = Wait for PHY power change done 0xB U3_EXIT_REM = Remote initiated U3 exit; send min required U3 exit 0xC U3_EXIT_P0 = PHY Power state P2/P3 -> P0 request 0xD U3_EXIT_P0_A = Wait for PHY power change P2/P3 -> P0 done 0xE U3_EXIT = Received remote/local U3 exit 0xF U3_EXIT_DONE U3 = Exit successful; U3 -> Recovery

TABLE 141: USB3 PORT 1 LTSSM STATE (CONTINUED)

SS_P1_LTSSM_State OFFSET: 65C0h RESET = 00h			USB3 Physical Port 1 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	SS.Disabled substates: 0x0 ESSD_POWER3 = PHY Power state P2/P3 request 0x1 ESSD_POWER3A = Wait for PHY power change done 0x2 ESSD_MAIN = Wait for RUN/STOP bit 0x3 ESSD_RATE = Wait for rate change 0x4 ESSD_POWER2 = Wait for PHY Power state P2/P3 request Rx.Detect substates: 0x0 RXD_INIT = PHY Power state P2 request 0x1 RXD_POWER2 = Wait for PHY power change done 0x2 RXD_RESET = Warm Reset 0x3 RXD_ACTIVE0 = Request to start receiver detection 0x4 RXD_ACTIVE1 = Wait for receiver detection response 0x5 RXD_QUIET = Wait for 12 ms-timer timeout 0x6 RXD_RATE = Wait for rate change SS.Inactive substates: 0x0 ESSI_RESET = PHY Power state P0 -> P2 request 0x1 ESSI_POWER2 = Wait for PHY power change done 0x2 ESSI_QUIET0 = Start 12 ms timer 0x3 ESSI_QUIET1 = Wait for 12 ms-timer timeout 0x4 ESSI_DIS_DET0 = Request to start receiver detection 0x5 ESSI_DIS_DET1 = Wait for Receiver detection response Polling substates: 0x0 POLL_RESET PHY = Power state P0 request 0x1 POLL_POWER0 = Wait for PHY power change done 0x2 POLL_LFPS = Send/Receive Poll LFPS 0x3 POLL_LFPSPLUS = Send/Receive SCD2 0x4 POLL_PMATCH = Send/Receive LBPM PHY capability 0x5 POLL_PCONFIG = Change rate and Send/Receive LBPM PHY ready 0x6 POLL_UPDATE_RATE = Wait for rate changed 0x7 POLL_RXEQ = Send/Receive TSEQ Training set 0x8 POLL_ACTIVE = Send/Receive TS1 Training set 0x9 POLL_CONFIG = Send/Receive TS2 Training set 0xA POLL_IDLE = Send/Receive Logical IDLE symbols Recovery substates: 0x0 RECOV_RESET = PHY Power state P0 request 0x1 RECOV_POWER0 = Wait for PHY power change done 0x2 RECOV_ACTIVE = Send/Receive TS1 Training set 0x3 RECOV_CONFIG = Send/Receive TS2 Training set 0x4 RECOV_IDLE = Send/Receive Logical IDLE symbols HotReset substates: 0x0 HRESET_RST = Request TCRRL to send TS2 0x1 HRESET_GO = Start 12 ms Timer 0x2 HRESET_ACT1 = Send/Receive TS1 Training set with Reset bit 0x3 HRESET_ACT2 = Send/Receive TS1 Training set without Reset bit 0x4 HRESET_EXIT = Send/Receive Logical IDLE symbols

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TABLE 141: USB3 PORT 1 LTSSM STATE (CONTINUED)

SS_P1_LTSSM_State OFFSET: 65C0h RESET = 00h			USB3 Physical Port 1 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	Compliance substates - none Loopback substates: 0x0 LPBK_IDLE = Wait for Loop back start request 0x1 LPBK_MASTER = Host mode: wait for Loopback Exit request 0x2 LPBK_SLAVE = Client mode: wait for Loopback Exit request 0x3 LPBK_EXIT_LOC_RESP = Start Loopback exit and wait for min response from remote partner

TABLE 142: USB3 PORT 1 DC TEST REGISTER

SS_P1_TEST_PIPE_DC OFFSET: 65C1h RESET = 00h			USB3 Physical Port 1 DC Test Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DETR_LPBK	R/W	Transmit Detect Receiver and Loopback mode. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. Used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINATION	R/W	Receiver Termination Control. This signal is asynchronous. Controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	Reserved	R	Reserved
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. ‘0’ = Full swing ‘1’ = Low swing
2	PIPE_TXC_DRIVE_HI GH	R/W	Sets the DC state of the TX output 0: TXP = 0; TXN = 1 1: TXP = 1; TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enables the Transmitter DC Drive mode
0	PIPE_TX_ELEC_IDLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with pow-er_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either Normal Transmit mode, Electrical Idle, LFPS transmission, or Receiver Detection).

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TABLE 143: USB3 PORT 1 TX TEST PATTERN REGISTER

SS_P1_TEST_PIPE_TX_PAT OFFSET: 65C3h RESET = 00h			USB3 Physical Port 1 TX Pattern Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always'0'
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. '0' = Disable pattern generator (Normal mode. Transmit data driven over the tx_data interface) '1' = Enable pattern generator
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. Gen1 Mode: 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 = CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = Custom CP9 (TS1 + Random data + 1 SKP every 354 symbols) 10 = Custom CP10 (TS1 + 1 SKP every 354 symbols) 11 = Custom CP11 (TSEQ repeated) 12 to 15 = Reserved Gen2 Mode: 0 = Spec CP9 (Pseudo random Data) 1 = Spec CP10 (AAh, Nyquist, not 128b132b encoded) 2 = Spec CP11 (CCh, Nyquist/2, not 128b132b encoded) 3 = Spec CP12 (LFSR15, not 128b132b encoded) 4 = Spec CP13 (64 1s / 64 0s, w/ pre, no de) 5 = Spec CP14 (64 1s / 64 0s, no pre, w/ de) 6 = Spec CP15 (64 1s / 64 0s, w/ pre, w/ de) 7 = Spec CP16 (64 1s / 64 0s, no pre, no de) 8 = Custom CP17 (Random data + SYNC OS every 16 data blocks for the first 800 blocks and then once every 14K data blocks + 3 SKP blocks every 115 blocks) 9: Custom CP18 (Random data + SYNC OS every 32 data blocks + 2 SKP blocks every 80 blocks 10 to 15 = Reserved

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TABLE 144: USB3 PORT 1 TX_MARGIN

SS_P1_TEST_PIPE_CTL_0 OFFSET: 65D0h RESET = 00h			USB3 Physical Port 1 TX Margin Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0.’ Do not modify.
6:4	PIPE_TX_MARGIN[2:0]	R/W	Physical Port 1 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 = +33% 100 = –67% 101 = –64% 110 = –61% 111 = –57%
3:0	Reserved	R	Always ‘0.’ Do not modify.

TABLE 145: USB3 PORT 1 GEN1 DEEMPHASIS

USB3_PIPE_TX_DEEMPH_CONTROL OFFSET: 66A0h RESET = 40030C1h			USB3 Physical Port 1 Gen1 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:27	Reserved	R	Always ‘0’
26	USB3_PIPE_DEEMPH_POST_EN	R/W	TX Post-Emphasis enable for Gen1
25	USB3_PIPE_DEEMPH_PRE_EN	R/W	TX Pre-Emphasis enable for Gen1
24:14	Reserved	R	Always ‘0’
13:12	POST_FFE_CONTROL	R/W	00 = +2.7 dB from default 01 = +1.8 dB from default 10 = +0.9 dB from default 11 = Default (–3.8 dB)
11:8	Reserved	R	Always ‘0’
7:6	TX_SWING	R/W	0 = 526 mV 1 = 687 mV 2 = 857 mV 3 = 970 mV (Default)
5:2	Reserved	R	Always ‘0’
1:0	PRE_FFE_CONTROL	R/W	00 = –1.5 dB from default 01 = –1 dB from default 10 = –0.5 dB from default 11 = Default (2 dB)

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TABLE 146: USB3 PORT 1 GEN2 DEEMPHASIS

USB3_PIPE_TX_DEEMP_GEN2_CONTROL OFFSET: 66B8h RESET = 60030C1h			USB3 Physical Port 1 Gen2 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:27	Reserved	R	Always ‘0’
26	USB3_PIPE_DEEM-PH_-GEN2_POST_EN	R/W	TX Post-Emphasis enable for Gen2
25	USB3_PIPE_DEEM-PH_GEN2_PRE_EN	R/W	TX Pre-Emphasis enable for Gen2
24:14	Reserved	R	Always ‘0’
13:12	POST_FFE_CON-TROL	R/W	00 = +2.7 dB from default 01 = +1.8 dB from default 10 = +0.9 dB from default 11 = Default (–3.1 dB)
11:8	Reserved	R	Always ‘0’
7:6	TX_SWING	R/W	0 = 526 mV 1 = 687 mV 2 = 857 mV 3 = 970 mV (Default)
5:2	Reserved	R	Always ‘0’
1:0	PRE_FFE_CON-TROL	R/W	00 = –1.5 dB from default 01 = –1 dB from default 10 = –0.5 dB from default 11 = Default (2 dB)

TABLE 147: USB3 PORT 2 TX PRE-DRIVER

SS_P2_AFE_TEST_IN4 OFFSET: 6886h RESET = 00h			USB3 Physical Port 2 TX Pre-Driver Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do no modify.
2:1	PRE_DRIVER	R/W	Physical Port 2 Transmitter Pre-Driver current adjust 00 = 100 µA (default biasing) 01 = 125 µA 10 = 87.5 µA 11 = 112.5 µA
0	Reserved	R	Reserved. Do no modify.

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TABLE 148: USB 2.0 PORT 6 RISE AND FALL ADJUSTMENT REGISTER

P6_RISEFALL_ADJ OFFSET: 68C8h RESET = 00h			USB 2.0 Port 6 Rise/Fall Adjust Register Base Address: BF80_0000h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:2	HS_TX_RISEFALL_ADJUST	R/W	High-Speed TX rise/fall adjust 00 = Default 01 = +18% 10 = –18% 11 = –12%
1:0	LS_TX_RISEFALL_ADJUST	R/W	Low-Speed/Full-Speed TX rise/fall adjust 00 = Default 01 = +100% 10 = –30% 11 = –50%

TABLE 149: USB PORT 2 BOOST REGISTER

HS_P2_BOOST OFFSET: 68CAh RESET = 00h			USB Port 2 Boost Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved. Do not modify.
2:0	HS_BOOST	R/W	HS Output Current 000b = Nominal 17.78 mA 001b = Decrease by 5% 010b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25% See **Note 1**.

Note 1: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] register if High-Speed disconnect issues are encountered.

TABLE 150: USB PORT 2 VARISENSE™ REGISTER

HS_P2_VSENSE OFFSET: 68CCh RESET = 00h			USB Port 2 VariSense™ Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b = Nominal (575 mV) threshold 01b = 625 mV threshold (+8.6%) 10b = 675 mV threshold (+17%) 11b = 700 mV threshold (+22%)
5:3	Reserved	R	Reserved. Do not modify.
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b = Nominal 100 mV Trip Point 001b = Decrease by 12.5 mV 010b = Decrease by 25 mV 011b = Decrease by 37.5 mV 100b = Decrease by 50 mV 101b = Decrease by 62.5 mV 110b = Increase by 25 mV 111b = Increase by 12.5 mV

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TABLE 151: USB3 PORT 2 LTSSM STATE

SS_P2_LTSSM_State OFFSET: 69C0h RESET = 00h			USB3 Physical Port 2 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	Physical Port 2 LTSSM state 0000b = U0 (no substates) 0001b = U1 (no substates) 0010b = U2 (no substates) 0011b = U3 (no substates) 0100b = SS.Disabled (see substate below) 0101b = Rx.Detect (see substate below) 0110b = SS.Inactive (see substate below) 0111b = Polling (see substate below) 1000b = Recovery (see substate below) 1001b = HotReset (see substate below) 1010b = Compliance (no substates) 1011b = Loopback (no substates)

TABLE 151: USB3 PORT 2 LTSSM STATE (CONTINUED)

SS_P2_LTSSM_State OFFSET: 69C0h RESET = 00h			USB3 Physical Port 2 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	Physical Port 2 LTSSM substate. Undefined values are invalid. U0 substates: none U1 substates: 0x0 U1 POWER = PHY Power state P0 -> P1 request 0x1 U1_POWER_A = Wait for PHY power change done 0x2 U1_ACTIVE = Wait for remote/local U1 exit 0x3 U1_EXIT_LOC_RESP = Start U1 exit and wait for min response from remote partner 0x4 U1_EXIT_LOC_FIN = Locally initiated U1 exit; send min required U1 exit 0x5 U1_EXIT_REM = Remote initiated U1 exit; send min required U1 exit 0x6 U1_EXIT_P0 = PHY Power state P1 -> P0 request 0x7 U1_EXIT_P0_A = Wait for PHY power change P1 -> P0 done 0x8 U1_EXIT_DONE = U1 exit successful. U1 -> Recovery U2 substates: 0x0 U2_POWER = PHY Power state P0 -> P2 request 0x1 U2_POWER2 = Wait for PHY power change done 0x2 U2_ACTIVE = Wait for remote/local U2 exit 0x3 U2_ACTIVE_0 = Request to start receiver detection 0x4 U2_ACTIVE_1 = Wait for Receiver detection response 0x5 U2_EXIT_LOC_RESP = Start U2 exit and wait for min response from remote partner 0x6 U2_EXIT_LOC_FIN = Locally initiated U2 exit; send min required U2 exit 0x7 U2_EXIT_REM = Remote initiated U2 exit; send min required U2 exit 0x8 U2_EXIT_P0 = PHY Power state P2 -> P0 request 0x9 U2_EXIT_P0_A = Wait for PHY power change P1 -> P0 done 0xA U2_EXIT_DONE = U2 exit successful. U2 -> Recovery U3 substates: 0x0 U3_POWER = PHY Power state P0 -> P2/P3 request 0x1 U3_POWER3 = Wait for PHY power change done 0x2 U3_ACTIVE = Wait for remote/local U3 exit 0x3 U3_ACTIVE_0 = Request to start receiver detection 0x4 U3_ACTIVE_1 = Wait for Receiver detection response 0x5 U3_EXIT_LOC_POW = PHY Power state P3 -> P0 -> P2 request 0x6 U3_EXIT_LOC_POW_A = Wait for PHY power change done 0x7 U3_EXIT_LOC_RESP = Start U3 exit and wait for min response from remote partner 0x8 U3_EXIT_LOC_FIN = Locally initiated U3 exit; send min required U3 exit 0x9 U3_EXIT_REM_POW = PHY Power state P3 -> P0 -> P2 request 0xA U3_EXIT_REM_POW_A = Wait for PHY power change done 0xB U3_EXIT_REM = Remote initiated U3 exit; send min required U3 exit 0xC U3_EXIT_P0 = PHY Power state P2/P3 -> P0 request 0xD U3_EXIT_P0_A = Wait for PHY power change P2/P3 -> P0 done 0xE U3_EXIT = Received remote/local U3 exit 0xF U3_EXIT_DONE = U3 exit successful. U3 -> Recovery

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TABLE 151: USB3 PORT 2 LTSSM STATE (CONTINUED)

SS_P2_LTSSM_State OFFSET: 69C0h RESET = 00h			USB3 Physical Port 2 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	SS.Disabled substates: 0x0 ESSD_POWER3 = PHY Power state P2/P3 request 0x1 ESSD_POWER3A = Wait for PHY power change done 0x2 ESSD_MAIN = Wait for RUN/STOP bit 0x3 ESSD_RATE = Wait for rate change 0x4 ESSD_POWER2 = Wait for PHY Power state P2/P3 request Rx.Detect substates: 0x0 RXD_INIT = PHY Power state P2 request 0x1 RXD_POWER2 = Wait for PHY power change done 0x2 RXD_RESET = Warm Reset 0x3 RXD_ACTIVE0 = Request to start receiver detection 0x4 RXD_ACTIVE1 = Wait for Receiver detection response 0x5 RXD_QUIET = Wait for 12 ms-timer timeout 0x6 RXD_RATE = Wait for rate change SS.Inactive substates: 0x0 ESSI_RESET = PHY Power state P0 -> P2 request 0x1 ESSI_POWER2 = Wait for PHY power change done 0x2 ESSI_QUIET0 = Start 12 ms timer 0x3 ESSI_QUIET1 = Wait for 12 ms-timer timeout 0x4 ESSI_DIS_DET0 = Request to start receiver detection 0x5 ESSI_DIS_DET1 = Wait for receiver detection response Polling substates: 0x0 POLL_RESET PHY = Power state P0 request 0x1 POLL_POWER0 = Wait for PHY power change done 0x2 POLL_LFPS = Send/Receive Poll.LFPS 0x3 POLL_LFPSPLUS = Send/Receive SCD2 0x4 POLL_PMATCH = Send/Receive LBPM PHY capability 0x5 POLL_PCONFIG = Change rate and Send/Receive LBPM PHY ready 0x6 POLL_UPDATE_RATE = Wait for rate changed 0x7 POLL_RXEQ = Send/Receive TSEQ Training set 0x8 POLL_ACTIVE = Send/Receive TS1 Training set 0x9 POLL_CONFIG = Send/Receive TS2 Training set 0xA POLL_IDLE = Send/Receive Logical IDLE symbols Recovery substates: 0x0 RECOV_RESET = PHY Power state P0 request 0x1 RECOV_POWER0 = Wait for PHY power change done 0x2 RECOV_ACTIVE = Send/Receive TS1 Training set 0x3 RECOV_CONFIG = Send/Receive TS2 Training set 0x4 RECOV_IDLE = Send/Receive Logical IDLE symbols HotReset substates: 0x0 HRESET_RST = Request TCRRL to send TS2 0x1 HRESET_GO = Start 12 ms Timer 0x2 HRESET_ACT1 = Send/Receive TS1 Training set with Reset bit 0x3 HRESET_ACT2 = Send/Receive TS1 Training set without Reset bit 0x4 HRESET_EXIT = Send/Receive Logical IDLE symbols

TABLE 152: USB3 PORT 2 DC TEST REGISTER

SS_P2_TEST_PIPE_DC OFFSET: 69C1h RESET = 00h			USB3 Physical Port 2 DC Test Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DE-TR_LPBK	R/W	Transmit Detect Receiver and Loopback mode. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. Used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINA-TION	R/W	Receiver Termination Control. This signal is asynchronous. Controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	Reserved	R	Always ‘0’
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. ‘0’ = Full Swing ‘1’ = Low Swing
2	PIPE_TX-C_DRIVE_HI GH	R/W	Sets the DC state of the TX output 0: TXP = 0, TXN = 1 1: TXP = 1, TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enables Transmitter DC Drive mode
0	PIPE_TX_ELEC_I-DLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with pow-er_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either normal transmit mode, electrical idle, LFPS transmission, or receiver detection).

TABLE 153: USB3 PORT 2 TX TEST PATTERN REGISTER

SS_P2_TEST_PIPE_TX_PAT OFFSET: 69C3h RESET = 00h			USB3 Physical Port 2 TX Pattern Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. ‘0’ = Disable pattern generator (Normal mode. Transmit data driven over the tx_data interface) ‘1’ = Enable pattern generator

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TABLE 153: USB3 PORT 2 TX TEST PATTERN REGISTER (CONTINUED)

SS_P2_TEST_PIPE_TX_PAT OFFSET: 69C3h RESET = 00h			USB3 Physical Port 2 TX Pattern Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. Gen1 Mode: 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 = CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = Custom CP9 (TS1 + Random data + 1 SKP every 354 symbols) 10 = Custom CP10 (TS1 + 1 SKP every 354 symbols) 11 = Custom CP11 (TSEQ repeated) 12 to 15 = Reserved Gen2 Mode: 0 = Spec CP9 (Pseudo random Data) 1 = Spec CP10 (AAh, Nyquist, not 128b132b encoded) 2 = Spec CP11 (CCh, Nyquist/2, not 128b132b encoded) 3 = Spec CP12 (LFSR15, not 128b132b encoded) 4 = Spec CP13 (64 1s / 64 0s, w/ pre, no de) 5 = Spec CP14 (64 1s / 64 0s, no pre, w/ de) 6 = Spec CP15 (64 1s / 64 0s, w/ pre, w/ de) 7 = Spec CP16 (64 1s / 64 0s, no pre, no de) 8 = Custom CP17 (Random data + SYNC OS every 16 data blocks for the first 800 blocks and then once every 14K data blocks + 3 SKP blocks every 115 blocks) 9 = Custom CP18 (Random data + SYNC OS every 32 data blocks + 2 SKP blocks every 80 blocks) 10 to 15 = Reserved

TABLE 154: USB3 PORT 2 TX_MARGIN

SS_P2_TEST_PIPE_CTL_0 OFFSET: 69D0h RESET = 00h			USB3 Physical Port 2 TX Margin Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always ‘0.’ Do not modify.
6:4	PIPE_TX_MAR-GIN[2:0]	R/W	Physical Port 2 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 = +33% 100 = –67% 101 = –64% 110 = –61% 111 = –57%
3:0	Reserved	R	Always ‘0.’ Do not modify.

TABLE 155: USB3 PORT 2 GEN1 DEEMPHASIS

USB3_PIPE_TX_DEEMPH_CONTROL OFFSET: 6AA0h RESET = 40030C1h			USB3 PHYSICAL Port 2 Gen1 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:27	Reserved	R	Always ‘0’
26	USB3_PIPE_DEEM-PH_POST_EN	R/W	TX Post-Emphasis enable for Gen1
25	USB3_PIPE_DEEM-PH_PRE_EN	R/W	TX Pre-Emphasis enable for Gen1
24:14	Reserved	R	Always ‘0’.
13:12	POST_FFE_CONTROL	R/W	00 = +2.7 dB from default 01 = +1.8 dB from default 10 = +0.9 dB from default 11 = Default (–3.8 dB)
11:8	Reserved	R	Always ‘0’
7:6	TX_SWING	R/W	0 = 526 mV 1 = 687 mV 2 = 857 mV 3 = 970 mV (Default)
5:2	Reserved	R	Always ‘0’.
1:0	PRE_FFE_CONTROL	R/W	00 = –1.5 dB from default 01 = –1 dB from default 10 = –0.5 dB from default 11 = Default (2 dB)

TABLE 156: USB3 PORT 2 GEN2 DEEMPHASIS

USB3_PIPE_TX_DEEMP_GEN2_CONTROL OFFSET: 6AB8h RESET = 60030C1h			USB3 Physical Port 2 Gen2 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:27	Reserved	R	Always ‘0’
26	USB3_PIPE_DEEMPH_-GEN2_POST_EN	R/W	TX Post-Emphasis enable for Gen2
25	USB3_PIPE_DEEMPH_-GEN2_PRE_EN	R/W	TX Pre-Emphasis enable for Gen2
24:14	Reserved	R	Always ‘0’.
13:12	POST_FFE_CONTROL	R/W	00 = +2.7 dB from default 01 = +1.8 dB from default 10 = +0.9 dB from default 11 = Default (–3.1 dB)
11:8	Reserved	R	Always ‘0’.
7:6	TX_SWING	R/W	0 = 526 mV 1 = 687 mV 2 = 857 mV 3 = 970 mV (Default)
5:2	Reserved	R	Always ‘0’

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TABLE 156: USB3 PORT 2 GEN2 DEEMPHASIS (CONTINUED)

USB3_PIPE_TX_DEEMP_GEN2_CONTROL OFFSET: 6AB8h RESET = 60030C1h			USB3 Physical Port 2 Gen2 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
1:0	PRE_FFE_CONTROL	R/W	00 = –1.5 dB from default 01 = –1 dB from default 10 = –0.5 dB from default 11 = Default (2 dB)

TABLE 157: USB PORT 3 BOOST REGISTER

HS_P3_BOOST OFFSET: 6CCAh RESET = 00h			USB Port 3 Boost Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved. Do not modify.
2:0	HS_BOOST	R/W	HS Output Current. 000b = Nominal 17.78 mA 001b = Decrease by 5% 010b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25% See **Note 1**.

Note 1: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] register if High-Speed disconnect issues are encountered.

TABLE 158: USB PORT 3 VARISENSE™ REGISTER

HS_P3_VSENSE OFFSET: 6CCCh RESET = 00h			USB Port 3 VariSense™ Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b = Nominal (575 mV) threshold 01b = 625 mV threshold (+8.6%) 10b = 675 mV threshold (+17%) 11b = 700 mV threshold (+22%)
5:3	Reserved	R	Reserved. Do not modify.
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b = Nominal 100 mV Trip Point 001b = Decrease by 12.5 mV 010b = Decrease by 25 mV 011b = Decrease by 37.5 mV 100b = Decrease by 50 mV 101b = Decrease by 62.5 mV 110b =Increase by 25 mV 111b = Increase by 12.5 mV

TABLE 159: USB 2.0 PORT 3 RISE AND FALL ADJUSTMENT REGISTER

P3_RISEFALL_ADJ OFFSET: 6CC8h RESET =00h			USB 2.0 Port 3 Rise/Fall Adjust Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved.
3:2	HS_TX_RISE-FALL_AD JUST	R/W	High-Speed TX rise/fall adjust. 00 = Default 01 = +18% 10 = –18% 11 = –12%
1:0	LS_TX_RISEFALL_A D JUST	R/W	Low-Speed/Full-Speed TX rise/fall adjust. 00 = Default 01 = +100% 10 = –30% 11 = –50%

TABLE 160: USB3 PORT 3 TX PRE-DRIVER

SS_P3_AFE_TEST_IN4 OFFSET: 6C86h RESET = 00h			USB3 Physical Port 3 TX Pre-Driver Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do no modify.
2:1	PRE_DRIVER	R/W	Physical Port 3 Transmitter Pre-Driver current adjust 00 = 100 µA (default biasing) 01 = 125 µA 10 = 87.5 µA 11 = 112.5 µA
0	Reserved	R	Reserved. Do no modify.

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TABLE 161: USB3 PORT 3 LTSSM STATE

SS_P3_LTSSM_State OFFSET: 6DC0h RESET = 00h			USB3 Physical Port 3 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	Physical Port 3 LTSSM state. 0000b = U0 (no substates) 0001b = U1 (no substates) 0010b = U2 (no substates) 0011b = U3 (no substates) 0100b = SS.Disabled (see substate below) 0101b = Rx.Detect (see substate below) 0110b = SS.Inactive (see substate below) 0111b = Polling (see substate below) 1000b = Recovery (see substate below) 1001b = HotReset (see substate below) 1010b = Compliance (no substates) 1011b = Loopback (no substates)

TABLE 161: USB3 PORT 3 LTSSM STATE (CONTINUED)

SS_P3_LTSSM_State OFFSET: 6DC0h RESET = 00h			USB3 Physical Port 3 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	Physical Port 3 LTSSM substate. Undefined values are invalid. U0 substates: none U1 substates: 0x0 U1 POWER = PHY Power state P0 -> P1 request 0x1 U1_POWER_A = Wait for PHY power change done 0x2 U1_ACTIVE = Wait for remote/local U1 exit 0x3 U1_EXIT_LOC_RESP = Start U1 exit and wait for min response from remote partner 0x4 U1_EXIT_LOC_FIN = Locally initiated U1 exit; send min required U1 exit 0x5 U1_EXIT_REM = Remote initiated U1 exit; send min required U1 exit 0x6 U1_EXIT_P0 = PHY Power state P1 -> P0 request 0x7 U1_EXIT_P0_A = Wait for PHY power change P1 -> P0 done 0x8 U1_EXIT_DONE = U1 exit successful. U1 -> Recovery U2 substates: 0x0 U2_POWER = PHY Power state P0 -> P2 request 0x1 U2_POWER2 = Wait for PHY power change done 0x2 U2_ACTIVE = Wait for remote/local U2 exit 0x3 U2_ACTIVE_0 = Request to start receiver detection 0x4 U2_ACTIVE_1 = Wait for receiver detection response 0x5 U2_EXIT_LOC_RESP = Start U2 exit and wait for min response from remote partner 0x6 U2_EXIT_LOC_FIN = Locally initiated U2 exit; send min required U2 exit 0x7 U2_EXIT_REM = Remote initiated U2 exit; send min required U2 exit 0x8 U2_EXIT_P0 = PHY Power state P2 -> P0 request 0x9 U2_EXIT_P0_A = Wait for PHY power change P1 -> P0 done 0xA U2_EXIT_DONE = U2 exit successful. U2 -> Recovery U3 substates: 0x0 U3_POWER = PHY Power state P0 -> P2/P3 request 0x1 U3_POWER3 = Wait for PHY power change done 0x2 U3_ACTIVE = Wait for remote/local U3 exit 0x3 U3_ACTIVE_0 = Request to start receiver detection 0x4 U3_ACTIVE_1 = Wait for Receiver detection response 0x5 U3_EXIT_LOC_POW = PHY Power state P3 -> P0 -> P2 request 0x6 U3_EXIT_LOC_POW_A = Wait for PHY power change done 0x7 U3_EXIT_LOC_RESP = Start U3 exit and wait for min response from remote partner 0x8 U3_EXIT_LOC_FIN = Locally initiated U3 exit, Send min required U3 exit 0x9 U3_EXIT_REM_POW = PHY Power state P3 -> P0 -> P2 request 0xA U3_EXIT_REM_POW_A = Wait for PHY power change done 0xB U3_EXIT_REM = Remote initiated U3 exit; send min required U3 exit 0xC U3_EXIT_P0 = PHY Power state P2/P3 -> P0 request 0xD U3_EXIT_P0_A = Wait for PHY power change P2/P3 -> P0 done 0xE U3_EXIT = Received remote/local U3 exit 0xF U3_EXIT_DONE = U3 exit successful. U3 -> Recovery

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TABLE 161: USB3 PORT 3 LTSSM STATE (CONTINUED)

SS_P3_LTSSM_State OFFSET: 6DC0h RESET = 00h			USB3 Physical Port 3 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	SS.Disabled substates: 0x0 ESSD_POWER3 = PHY Power state P2/P3 request 0x1 ESSD_POWER3A = Wait for PHY power change done 0x2 ESSD_MAIN = Wait for RUN/STOP bit 0x3 ESSD_RATE = Wait for rate change 0x4 ESSD_POWER2 = Wait for PHY Power state P2/P3 request Rx.Detect substates: 0x0 RXD_INIT = PHY Power state P2 request 0x1 RXD_POWER2 = Wait for PHY power change done 0x2 RXD_RESET = Warm Reset 0x3 RXD_ACTIVE0 = Request to start receiver detection 0x4 RXD_ACTIVE1 = Wait for Receiver detection response 0x5 RXD_QUIET = Wait for 12 ms-timer timeout 0x6 RXD_RATE = Wait for rate change SS.Inactive substates: 0x0 ESSI_RESET = PHY Power state P0 -> P2 request 0x1 ESSI_POWER2 = Wait for PHY power change done 0x2 ESSI_QUIET0 = Start 12 ms timer 0x3 ESSI_QUIET1 = Wait for 12-ms timer timeout 0x4 ESSI_DIS_DET0 = Request to start receiver detection 0x5 ESSI_DIS_DET1 = Wait for Receiver detection response Polling substates: 0x0 POLL_RESET = PHY Power state P0 request 0x1 POLL_POWER0 = Wait for PHY power change done 0x2 POLL_LFPS = Send/Receive Poll.LFPS 0x3 POLL_LFPSPLUS = Send/Receive SCD2 0x4 POLL_PMATCH = Send/Receive LBPM PHY capability 0x5 POLL_PCONFIG = Change rate and Send/Receive LBPM PHY ready 0x6 POLL_UPDATE_RATE = Wait for rate changed 0x7 POLL_RXEQ = Send/Receive TSEQ Training set 0x8 POLL_ACTIVE = Send/Receive TS1 Training set 0x9 POLL_CONFIG = Send/Receive TS2 Training set 0xA POLL_IDLE = Send/Receive Logical IDLE symbols Recovery substates: 0x0 RECOV_RESET = PHY Power state P0 request 0x1 RECOV_POWER0 = Wait for PHY power change done 0x2 RECOV_ACTIVE = Send/Receive TS1 Training set 0x3 RECOV_CONFIG = Send/Receive TS2 Training set 0x4 RECOV_IDLE = Send/Receive Logical IDLE symbols HotReset substates: 0x0 HRESET_RST = Request TCRRL to send TS2 0x1 HRESET_GO = Start 12 ms timer 0x2 HRESET_ACT1 = Send/Receive TS1 Training set with Reset bit 0x3 HRESET_ACT2 = Send/Receive TS1 Training set without Reset bit 0x4 HRESET_EXIT = Send/Receive Logical IDLE symbols

TABLE 161: USB3 PORT 3 LTSSM STATE (CONTINUED)

SS_P3_LTSSM_State OFFSET: 6DC0h RESET = 00h			USB3 Physical Port 3 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	Compliance substates - none Loopback substates: 0x0 LPBK_IDLE = Wait for Loop back start request 0x1 LPBK_MASTER = Host mode; wait for Loopback Exit request 0x2 LPBK_SLAVE = Client mode; wait for Loopback Exit request 0x3 LPBK_EXIT_LOC_RESP = Start Loopback exit and wait for min response from remote partner

TABLE 162: USB3 PORT 3 DC TEST REGISTER

SS_P3_TEST_PIPE_DC OFFSET: 6DC1h RESET = 00h			USB3 Physical Port 3 DC Test Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DE-TR_LPBK	R/W	Transmit Detect Receiver and Loopback Mode. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. Used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINA-TION	R/W	Receiver Termination Control. This signal is asynchronous. Controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	Reserved	R	Always ‘0’.
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. ‘0’ = Full Swing ‘1’ = Low Swing
2	PIPE_TX-C_DRIVE_HI GH	R/W	Sets the DC state of the TX output 0: TXP = 0, TXN = 1 1: TXP = 1, TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enables Transmitter DC Drive mode
0	PIPE_TX_ELEC_I-DLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with power_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either Normal Transmit mode, Electrical Idle, LFPS transmission, or Receiver Detection).

TABLE 163: USB3 PORT 3 TX TEST PATTERN REGISTER

SS_P3_TEST_PIPE_TX_PAT OFFSET: 6DC3h RESET = 00h			USB3 Physical Port 3 TX Pattern Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always ‘0’

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TABLE 163: USB3 PORT 3 TX TEST PATTERN REGISTER (CONTINUED)

SS_P3_TEST_PIPE_TX_PAT OFFSET: 6DC3h RESET = 00h			USB3 Physical Port 3 TX Pattern Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. '0' = Disable pattern generator (Normal mode. Transmit data driven over the tx_data interface.) '1' = Enable pattern generator
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. Gen1 Mode: 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 = CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = Custom CP9 (TS1 + Random data + 1 SKP every 354 symbols) 10 = Custom CP10 (TS1 + 1 SKP every 354 symbols) 11 = Custom CP11 (TSEQ repeated) 12 to 15 = Reserved Gen2 Mode: 0 = Spec CP9 (Pseudo random Data) 1 = Spec CP10 (AAh, Nyquist, not 128b132b encoded) 2 = Spec CP11 (CCh, Nyquist/2, not 128b132b encoded) 3 = Spec CP12 (LFSR15, not 128b132b encoded) 4 = Spec CP13 (64 1s / 64 0s, w/ pre, no de) 5 = Spec CP14 (64 1s / 64 0s, no pre, w/ de) 6 = Spec CP15 (64 1s / 64 0s, w/ pre, w/ de) 7 = Spec CP16 (64 1s / 64 0s, no pre, no de) 8 = Custom CP17 (Random data + SYNC OS every 16 data blocks for the first 800 blocks and then once every 14K data blocks + 3 SKP blocks every 115 blocks) 9 = Custom CP18 (Random data + SYNC OS every 32 data blocks + 2 SKP blocks every 80 blocks) 10 to 15 = Reserved

TABLE 164: USB3 PORT 3 TX_MARGIN

SS_P3_TEST_PIPE_CTL_0 OFFSET: 6DD0h RESET = 00h			USB3 Physical Port 3 TX Margin Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always '0.' Do not modify.
6:4	PIPE_TX_MARGIN[2:0]	R/W	Physical Port 3 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 = +33% 100 = –67% 101 = –64% 110 = –61% 111 = –57%
3:0	Reserved	R	Always '0.' Do not modify.

TABLE 165: USB3 PORT 3 GEN1 DEEMPHASIS

SS_P3_PIPE_TX_DEEMPH_CTL OFFSET: 6EA0h RESET = 40030C1h			USB3 Physical Port 3 Gen1 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:27	Reserved	R	Always '0'
26	USB3_PIPE_DEEMPH_POST_EN	R/W	TX Post-Emphasis enable for Gen1
25	USB3_PIPE_DEEMPH_PRE_EN	R/W	TX Pre-Emphasis enable for Gen1
24:14	Reserved	R	Always '0'
13:12	POST_FFE_CONTROL	R/W	00 = +2.7 dB from default 01 = +1.8 dB from default 10 = +0.9 dB from default 11 = Default (–3.8 dB)
11:8	Reserved	R	Always '0'
7:6	TX_SWING	R/W	0 = 526 mV 1 = 687 mV 2 = 857 mV 3 = 970 mV (Default)
5:2	Reserved	R	Always '0'
1:0	PRE_FFE_CONTROL	R/W	00 = –1.5 dB from default 01 = –1 dB from default 10 = –0.5 dB from default 11 = Default (2 dB)

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TABLE 166: USB3 PORT 3 GEN2 DEEMPHASIS

SS_P3_PIPE_TX_DEEMP_GEN2_CTL OFFSET: 6EB8h RESET = 60030C1h			USB3 Physical Port 3 Gen2 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:27	Reserved	R	Always ‘0’
26	USB3_PIPE_DEEM-PH_-GEN2_POST_EN	R/W	TX Post-Emphasis enable for Gen2
25	USB3_PIPE_DEEM-PH_GEN2_PRE_EN	R/W	TX Pre-Emphasis enable for Gen2
24:14	Reserved	R	Always ‘0’.
13:12	POST_FFE_CON-TROL	R/W	00 = +2.7 dB from default 01 = +1.8 dB from default 10 = +0.9 dB from default 11 = Default (–3.1 dB)
11:8	Reserved	R	Always ‘0’
7:6	TX_SWING	R/W	0 = 526 mV 1 = 687 mV 2 = 857 mV 3 = 970 mV (Default)
5:2	Reserved	R	Always ‘0’
1:0	PRE_FFE_CON-TROL	R/W	00 = –1.5 dB from default 01 = –1 dB from default 10 = –0.5 dB from default 11 = Default (2 dB)

TABLE 167: USB PORT 4 BOOST REGISTER

HS_P4_BOOST OFFSET: 70CAh RESET = 00h			USB Port 4 Boost Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved. Do not modify.
2:0	HS_BOOST	R/W	HS Output Current 000b = Nominal 17.78 mA 001b = Decrease by 5% 010b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25% See **Note 1**.

Note 1: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] register if High-Speed disconnect issues are encountered.

TABLE 168: USB PORT 4 VARISENSE™ REGISTER

HS_P4_VSENSE OFFSET: 70CCh RESET = 00h			USB Port 4 VariSense™ Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b = Nominal (575 mV) threshold 01b = 625 mV threshold (+8.6%) 10b = 675 mV threshold (+17%) 11b = 700 mV threshold (+22%)
5:3	Reserved	R	Reserved. Do not modify.
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000 = Nominal 100-mV Trip Point 001 = Decrease by 12.5 mV 010 = Decrease by 25 mV 011 = Decrease by 37.5 mV 100 = Decrease by 50 mV 101 = Decrease by 62.5 mV 110 = Increase by 25 mV 111 = Increase by 12.5 mV

TABLE 169: USB 2.0 PORT 4 RISE AND FALL ADJUSTMENT REGISTER

P4_RISEFALL_ADJ OFFSET: 70C8h RESET = 00h			USB 2.0 Port 4 Rise/Fall Adjust Register Base Address: BF80_0000h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:2	HS_TX_RISEFALL_ADJUST	R/W	High-Speed TX rise/fall adjust 00 = Default 01 = +18% 10 = –18% 11 = –12%
1:0	LS_TX_RISEFALL_ADJUST	R/W	Low-Speed/Full-Speed TX rise/fall adjust 00 = Default 01 = +100% 10 = –30% 11 = –50%

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TABLE 170: USB3 PORT 4 TX PRE-DRIVER

SS_P4_AFE_TEST_IN4 OFFSET: 7086h RESET = 00h			USB3 Physical Port 4 TX Pre-Driver Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do no modify.
2:1	Length	R/W	Physical Port 4 Transmitter Pre-Driver current adjust 00 = 100 µA (default biasing) 01 = 125 µA 10 = 87.5 µA 11 = 112.5 µA
0	Reserved	R	Reserved. Do no modify.

TABLE 171: USB3 PORT 4 LTSSM STATE

SS_P4_LTSSM_State OFFSET: 71C0h RESET = 00h			USB3 PHYSICAL Port 4 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	PHYSICAL Port 4 LTSSM state. 0000b = U0 (no sub-states) 0001b = U1 (no sub-states) 0010b = U2 (no sub-states) 0011b = U3 (no sub-states) 0100b = SS.Disabled (see sub-state below) 0101b = Rx.Detect (see sub-state below) 0110b = SS.Inactive (see sub-state below) 0111b = Polling (see sub-state below) 1000b = Recovery (see sub-state below) 1001b = HotReset (see sub-state below) 1010b = Compliance (no sub-states) 1011b = Loopback (no sub-states)

TABLE 171: USB3 PORT 4 LTSSM STATE (CONTINUED)

SS_P4_LTSSM_State OFFSET: 71C0h RESET = 00h			USB3 PHYSICAL Port 4 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	PHYSICAL Port 4 LTSSM substate. Undefined values are invalid. U0 sub-states: none U1 sub-states: 0x0 U1 POWER = PHY Power state P0 -> P1 request 0x1 U1_POWER_A = Wait for PHY power change done 0x2 U1_ACTIVE = Wait for remote/local U1 exit 0x3 U1_EXIT_LOC_RESP = Start U1 exit and wait for min response from remote partner 0x4 U1_EXIT_LOC_FIN = Locally initiated U1 exit, Send min required U1 exit 0x5 U1_EXIT_REM = Remote initiated U1 exit, Send min required U1 exit 0x6 U1_EXIT_P0 PHY = Power state P1 -> P0 request 0x7 U1_EXIT_P0_A = Wait for PHY power change P1 -> P0 done 0x8 U1_EXIT_DONE = U1 exit successful. U1 -> Recovery U2 sub-states: 0x0 U2_POWER = PHY Power state P0 -> P2 request 0x1 U2_POWER2 = Wait for PHY power change done 0x2 U2_ACTIVE = Wait for remote/local U2 exit 0x3 U2_ACTIVE_0 = Request to start receiver detection 0x4 U2_ACTIVE_1 = Wait for Receiver detection response 0x5 U2_EXIT_LOC_RESP = Start U2 exit and wait for min response from remote partner 0x6 U2_EXIT_LOC_FIN = Locally initiated U2 exit, Send min required U2 exit 0x7 U2_EXIT_REM = Remote initiated U2 exit, Send min required U2 exit 0x8 U2_EXIT_P0 = PHY Power state P2 -> P0 request 0x9 U2_EXIT_P0_A = Wait for PHY power change P1 -> P0 done 0xA U2_EXIT_DONE = U2 exit successful. U2 -> Recovery U3 sub-states: 0x0 U3_POWER = PHY Power state P0 -> P2/P3 request 0x1 U3_POWER3 = Wait for PHY power change done 0x2 U3_ACTIVE = Wait for remote/local U3 exit 0x3 U3_ACTIVE_0 = Request to start receiver detection 0x4 U3_ACTIVE_1 = Wait for Receiver detection response 0x5 U3_EXIT_LOC_POW = PHY Power state P3 -> P0 -> P2 request 0x6 U3_EXIT_LOC_POW_A = Wait for PHY power change done 0x7 U3_EXIT_LOC_RESP = Start U3 exit and wait for min response from remote partner 0x8 U3_EXIT_LOC_FIN = Locally initiated U3 exit, Send min required U3 exit 0x9 U3_EXIT_REM_POW = PHY Power state P3 -> P0 -> P2 request 0xA U3_EXIT_REM_POW_A = Wait for PHY power change done 0xB U3_EXIT_REM = Remote initiated U3 exit, Send min required U3 exit 0xC U3_EXIT_P0 PHY = Power state P2/P3 -> P0 request 0xD U3_EXIT_P0_A = Wait for PHY power change P2/P3 -> P0 done 0xE U3_EXIT = Received remote/local U3 exit 0xF U3_EXIT_DONE = U3 exit successful. U3 -> Recovery

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TABLE 171: USB3 PORT 4 LTSSM STATE (CONTINUED)

SS_P4_LTSSM_State OFFSET: 71C0h RESET = 00h			USB3 PHYSICAL Port 4 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	SS.Disabled substates: 0x0 ESSD_POWER3 = PHY Power state P2/P3 request 0x1 ESSD_POWER3A = Wait for PHY power change done 0x2 ESSD_MAIN = Wait for RUN/STOP bit 0x3 ESSD_RATE = Wait for rate change 0x4 ESSD_POWER2 = Wait for PHY Power state P2/P3 request Rx.Detect substates: 0x0 RXD_INIT = PHY Power state P2 request 0x1 RXD_POWER2 = Wait for PHY power change done 0x2 RXD_RESET = Warm Reset 0x3 RXD_ACTIVE0 = Request to start receiver detection 0x4 RXD_ACTIVE1 = Wait for Receiver detection response 0x5 RXD_QUIET = Wait for 12 ms timer timeout 0x6 RXD_RATE = Wait for rate change SS.Inactive substates: 0x0 ESSI_RESET = PHY Power state P0 -> P2 request 0x1 ESSI_POWER2 = Wait for PHY power change done 0x2 ESSI_QUIET0 = Start 12 ms timer 0x3 ESSI_QUIET1 = Wait for 12-ms timer timeout 0x4 ESSI_DIS_DET0 = Request to start receiver detection 0x5 ESSI_DIS_DET1 = Wait for Receiver detection response Polling substates: 0x0 POLL_RESET = PHY Power state P0 request 0x1 POLL_POWER0 = Wait for PHY power change done 0x2 POLL_LFPS = Send/Receive Poll.LFPS 0x3 POLL_LFPSPLUS = Send/Receive SCD2 0x4 POLL_PMATCH = Send/Receive LBPM PHY capability 0x5 POLL_PCONFIG = Change rate and Send/Receive LBPM PHY ready 0x6 POLL_UPDATE_RATE = Wait for rate change 0x7 POLL_RXEQ = Send/Receive TSEQ Training set 0x8 POLL_ACTIVE = Send/Receive TS1 Training set 0x9 POLL_CONFIG = Send/Receive TS2 Training set 0xA POLL_IDLE = Send/Receive Logical IDLE symbols Recovery substates: 0x0 RECOV_RESET = PHY Power state P0 request 0x1 RECOV_POWER0 =Wait for PHY power change done 0x2 RECOV_ACTIVE = Send/Receive TS1 Training set 0x3 RECOV_CONFIG = Send/Receive TS2 Training set 0x4 RECOV_IDLE = Send/Receive Logical IDLE symbols HotReset substates: 0x0 HRESET_RST = Request TCRRL to send TS2 0x1 HRESET_GO = Start 12 ms Timer 0x2 HRESET_ACT1 = Send/Receive TS1 Training set with Reset bit 0x3 HRESET_ACT2 = Send/Receive TS1 Training set without Reset bit 0x4 HRESET_EXIT = Send/Receive Logical IDLE symbols

TABLE 171: USB3 PORT 4 LTSSM STATE (CONTINUED)

SS_P4_LTSSM_State OFFSET: 71C0h RESET = 00h			USB3 PHYSICAL Port 4 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	Compliance substates - none Loopback substates: 0x0 LPBK_IDLE = Wait for Loop back start request 0x1 LPBK_MASTER = Host mode; wait for Loopback Exit request 0x2 LPBK_SLAVE = Client mode; wait for Loopback Exit request 0x3 LPBK_EXIT_LOC_RESP = Start Loopback exit and wait for min response from remote partner

TABLE 172: USB3 PORT 4 DC TEST REGISTER

SS_P4_TEST_PIPE_DC OFFSET: 71C1h RESET = 00h			USB3 Physical Port 4 DC Test Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DE-TR_LPBK	R/W	Transmit Detect Receiver and Loopback mode. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. Used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINA-TION	R/W	Receiver Termination Control. This signal is asynchronous. Controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	Reserved	R	Always ‘0’.
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. ‘0’ = Full Swing ‘1’ = Low Swing
2	PIPE_TX-C_DRIVE_HI GH	R/W	Sets the DC state of the TX output 0: TXP = 0, TXN = 1 1: TXP = 1, TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enables Transmitter DC Drive mode
0	PIPE_TX_ELEC_I-DLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with pow-er_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either Normal Transmit mode, Electrical Idle, LFPS Transmission, or Receiver Detection).

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TABLE 173: USB3 PORT 4 TX TEST PATTERN REGISTER

SS_P4_TEST_PIPE_TX_PAT OFFSET: 71C3h RESET = 00h			USB3 Physical Port 4 TX Pattern Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always'0'
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. '0' = Disable pattern generator (Normal mode. Transmit data driven over the tx_data interface) '1' = Enable pattern generator
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. Gen1 mode: 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 = CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = Custom CP9 (TS1 + Random data + 1 SKP every 354 symbols) 10 = Custom CP10 (TS1 + 1 SKP every 354 symbols) 11 = Custom CP11 (TSEQ repeated) 12 to 15 = Reserved Gen2 mode: 0 = Spec CP9 (Pseudo random Data) 1 = Spec CP10 (AAh, Nyquist, not 128b132b encoded) 2 = Spec CP11 (CCh, Nyquist/2, not 128b132b encoded) 3 = Spec CP12 (LFSR15, not 128b132b encoded) 4 = Spec CP13 (64 1s / 64 0s, w/ pre, no de) 5 = Spec CP14 (64 1s / 64 0s, no pre, w/ de) 6 = Spec CP15 (64 1s / 64 0s, w/ pre, w/ de) 7 = Spec CP16 (64 1s / 64 0s, no pre, no de) 8 = Custom CP17 (Random data + SYNC OS every 16 data blocks for the first 800 blocks and then once every 14K data blocks + 3 SKP blocks every 115 blocks) 9 = Custom CP18 (Random data + SYNC OS every 32 data blocks + 2 SKP blocks every 80 blocks) 10 to 15 = Reserved

TABLE 174: USB3 PORT 4 TX_MARGIN

SS_P4_TEST_PIPE_CTL_0 OFFSET: 71D0h RESET = 00h			USB3 Physical Port 4 TX Margin Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always '0.' Do not modify.

TABLE 174: USB3 PORT 4 TX_MARGIN (CONTINUED)

SS_P4_TEST_PIPE_CTL_0 OFFSET: 71D0h RESET = 00h			USB3 Physical Port 4 TX Margin Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
6:4	PIPE_TX_MARGIN[2:0]	R/W	Physical Port 4 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 = +33% 100 = –67% 101 = –64% 110 = –61% 111 = –57%
3:0	Reserved	R	Always ‘0.’ Do not modify.

TABLE 175: USB3 PORT 4 GEN1 DEEMPHASIS

SS_P4_PIPE_TX_DEEMPH_CTL OFFSET: 72A0h RESET = 40030C1h			USB3 PHYSICAL Port 4 Gen1 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:27	Reserved	R	Always ‘0’.
26	USB3_PIPE_DEEMPH_POST_EN	R/W	TX Post-Emphasis enable for Gen1
25	USB3_PIPE_DEEMPH_PRE_EN	R/W	TX Pre-Emphasis enable for Gen1
24:14	Reserved	R	Always ‘0’.
13:12	POST_FFE_CONTROL	R/W	00 = +2.7 dB from default 01 = +1.8 dB from default 10 = +0.9 dB from default 11 = Default (–3.8 dB)
11:8	Reserved	R	Always ‘0’.
7:6	TX_SWING	R/W	0 = 526 mV 1 = 687 mV 2 = 857 mV 3 = 970 mV (Default)
5:2	Reserved	R	Always ‘0’.
1:0	PRE_FFE_CONTROL	R/W	00 = –1.5dB from default 01 =–1dB from default 10 = –0.5dB from default 11 =Default (2 dB)

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TABLE 176: USB3 PORT 4 GEN2 DEEMPHASIS

SS_P4_PIPE_TX_DEEMP_GEN2_CTL OFFSET: 72B8h RESET = 60030C1h			USB3 Physical Port 4 Gen2 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:27	Reserved	R	Always ‘0’
26	USB3_PIPE_DEEMPH_-GEN2_POST_EN	R/W	TX Post-Emphasis enable for Gen2
25	USB3_PIPE_DEEMPH_-GEN2_PRE_EN	R/W	TX Pre-Emphasis enable for Gen2
24:14	Reserved	R	Always ‘0’.
13:12	POST_FFE_CONTROL	R/W	00 = +2.7 dB from default 01 = +1.8 dB from default 10 = +0.9 dB from default 11 = Default (–3.1 dB)
11:8	Reserved	R	Always ‘0’
7:6	TX_SWING	R/W	0 = 526 mV 1 = 687 mV 2 = 857 mV 3 = 970 mV (Default)
5:2	Reserved	R	Always ‘0’
1:0	PRE_FFE_CONTROL	R/W	00 = –1.5 dB from default 01 = –1 dB from default 10 = –0.5 dB from default 11 = Default (2 dB)

TABLE 177: USB PORT 5 BOOST REGISTER

HS_P5_BOOST OFFSET: 74CAh RESET = 00h			USB Port 5 Boost Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R/W	Reserved. Do not modify.
2:0	HS_BOOST	R/W	HS Output Current 000b = Nominal 17.78 mA 001b = Decrease by 5% 010b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25% See **Note 1**.

Note 1: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] register if High-Speed disconnect issues are encountered.

TABLE 178: USB PORT 5 VARISENSE™ REGISTER

HS_P5_VSENSE OFFSET: 74CCh RESET = 10h			USB Port 5 VariSense™ Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b = Nominal (575 mV) threshold 01b = 625 mV threshold (+8.6%) 10b = 675 mV threshold (+17%) 11b = 700 mV threshold (+22%)
5:3	Reserved	R	Reserved. Do not modify.
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b = Nominal 100 mV Trip Point 001b = Decrease by 12.5 mV 010b = Decrease by 25 mV 011b = Decrease by 37.5 mV 100b = Decrease by 50 mV 101b = Decrease by 62.5 mV 110b = Increase by 25 mV 111b = Increase by 12.5 mV

TABLE 179: USB 2.0 PORT 5 RISE AND FALL ADJUSTMENT REGISTER

P5_RISEFALL_ADJ OFFSET: 74C8h RESET = 00h			USB 2.0 Port 5 Rise/Fall Adjust Register Base Address: BF80_0000h
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:2	HS_TX_RISEFALL_ADJUST	R/W	High-Speed TX rise/fall adjust 00 = Default 01 = +18% 10 = –18% 11 = –12%
1:0	LS_TX_RISEFALL_ADJUST	R/W	Low-Speed/Full-Speed TX rise/fall adjust 00 = Default 01 = +100% 10 = –30% 11 = –50%

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TABLE 180: USB3 PORT 5 TX PRE-DRIVER

SS_P5_AFE_TEST_IN4 OFFSET: 7486h RESET = 00h			USB3 Physical Port 5 TX Pre-Driver Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do no modify.
2:1	PRE_DRIVER	R/W	Physical Port 5 Transmitter Pre-Driver current adjust 00 = 100 µA (default biasing) 01 = 125 µA 10 = 87.5 µA 11 = 112.5 µA
0	Reserved	R	Reserved. Do no modify.

TABLE 181: USB3 PORT 5 LTSSM STATE

SS_P5_LTSSM_State OFFSET: 75C0h RESET = 00h			USB3 Physical Port 5 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	Physical Port 5 LTSSM state 0000b = U0 (no substates) 0001b = U1 (no substates) 0010b = U2 (no substates) 0011b = U3 (no substates) 0100b = SS.Disabled (see substate below) 0101b = Rx.Detect (see substate below) 0110b = SS.Inactive (see substate below) 0111b = Polling (see substate below) 1000b = Recovery (see substate below) 1001b = HotReset (see substate below) 1010b = Compliance (no substates) 1011b = Loopback (no substates)

TABLE 181: USB3 PORT 5 LTSSM STATE (CONTINUED)

SS_P5_LTSSM_State OFFSET: 75C0h RESET = 00h			USB3 Physical Port 5 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	Physical Port 5 LTSSM substate. Undefined values are invalid. U0 substates: none U1 substates: 0x0 U1 POWER = PHY Power state P0 -> P1 request 0x1 U1_POWER_A = Wait for PHY power change done 0x2 U1_ACTIVE = Wait for remote/local U1 exit 0x3 U1_EXIT_LOC_RESP = Start U1 exit and wait for min response from remote partner 0x4 U1_EXIT_LOC_FIN = Locally initiated U1 exit; send min required U1 exit 0x5 U1_EXIT_REM = Remote initiated U1 exit; send min required U1 exit 0x6 U1_EXIT_P0 = PHY Power state P1 -> P0 request 0x7 U1_EXIT_P0_A = Wait for PHY power change P1 -> P0 done 0x8 U1_EXIT_DONE = U1 exit successful. U1 -> Recovery U2 substates: 0x0 U2_POWER = PHY Power state P0 -> P2 request 0x1 U2_POWER2 = Wait for PHY power change done 0x2 U2_ACTIVE = Wait for remote/local U2 exit 0x3 U2_ACTIVE_0 = Request to start receiver detection 0x4 U2_ACTIVE_1 = Wait for Receiver detection response 0x5 U2_EXIT_LOC_RESP = Start U2 exit and wait for min response from remote partner 0x6 U2_EXIT_LOC_FIN = Locally initiated U2 exit; send min required U2 exit 0x7 U2_EXIT_REM = Remote initiated U2 exit; send min required U2 exit 0x8 U2_EXIT_P0 = PHY Power state P2 -> P0 request 0x9 U2_EXIT_P0_A = Wait for PHY power change P1 -> P0 done 0xA U2_EXIT_DONE = U2 exit successful. U2 -> Recovery U3 substates: 0x0 U3_POWER = PHY Power state P0 -> P2/P3 request 0x1 U3_POWER3 = Wait for PHY power change done 0x2 U3_ACTIVE = Wait for remote/local U3 exit 0x3 U3_ACTIVE_0 = Request to start receiver detection 0x4 U3_ACTIVE_1 = Wait for Receiver detection response 0x5 U3_EXIT_LOC_POW = PHY Power state P3 -> P0 -> P2 request 0x6 U3_EXIT_LOC_POW_A = Wait for PHY power change done 0x7 U3_EXIT_LOC_RESP = Start U3 exit and wait for min response from remote partner 0x8 U3_EXIT_LOC_FIN = Locally initiated U3 exit; send min required U3 exit 0x9 U3_EXIT_REM_POW = PHY Power state P3 -> P0 -> P2 request 0xA U3_EXIT_REM_POW_A = Wait for PHY power change done 0xB U3_EXIT_REM = Remote initiated U3 exit; send min required U3 exit 0xC U3_EXIT_P0 = PHY Power state P2/P3 -> P0 request 0xD U3_EXIT_P0_A = Wait for PHY power change P2/P3 -> P0 done 0xE U3_EXIT = Received remote/local U3 exit 0xF U3_EXIT_DONE = U3 exit successful. U3 -> Recovery

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TABLE 181: USB3 PORT 5 LTSSM STATE (CONTINUED)

SS_P5_LTSSM_State OFFSET: 75C0h RESET = 00h			USB3 Physical Port 5 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	SS.Disabled substates: 0x0 ESSD_POWER3 = PHY Power state P2/P3 request 0x1 ESSD_POWER3A = Wait for PHY power change done 0x2 ESSD_MAIN = Wait for RUN/STOP bit 0x3 ESSD_RATE = Wait for rate change 0x4 ESSD_POWER2 = Wait for PHY Power state P2/P3 request Rx.Detect substates: 0x0 RXD_INIT = PHY Power state P2 request 0x1 RXD_POWER2 = Wait for PHY power change done 0x2 RXD_RESET = Warm Reset 0x3 RXD_ACTIVE0 = Request to start receiver detection 0x4 RXD_ACTIVE1 = Wait for Receiver detection response 0x5 RXD_QUIET = Wait for 12 ms-timer timeout 0x6 RXD_RATE = Wait for rate change SS.Inactive substates: 0x0 ESSI_RESET = PHY Power state P0 -> P2 request 0x1 ESSI_POWER2 = Wait for PHY power change done 0x2 ESSI_QUIET0 = Start 12 ms timer 0x3 ESSI_QUIET1 = Wait for 12 ms-timer timeout 0x4 ESSI_DIS_DET0 = Request to start receiver detection 0x5 ESSI_DIS_DET1 = Wait for Receiver detection response Polling substates: 0x0 POLL_RESET = PHY Power state P0 request 0x1 POLL_POWER0 = Wait for PHY power change done 0x2 POLL_LFPS = Send/Receive Poll.LFPS 0x3 POLL_LFPSPLUS = Send/Receive SCD2 0x4 POLL_PMATCH = Send/Receive LBPM PHY capability 0x5 POLL_PCONFIG = Change rate and Send/Receive LBPM PHY ready 0x6 POLL_UPDATE_RATE = Wait for rate changed 0x7 POLL_RXEQ = Send/Receive TSEQ Training set 0x8 POLL_ACTIVE = Send/Receive TS1 Training set 0x9 POLL_CONFIG = Send/Receive TS2 Training set 0xA POLL_IDLE = Send/Receive Logical IDLE symbols Recovery substates: 0x0 RECOV_RESET = PHY Power state P0 request 0x1 RECOV_POWER0 = Wait for PHY power change done 0x2 RECOV_ACTIVE = Send/Receive TS1 Training set 0x3 RECOV_CONFIG = Send/Receive TS2 Training set 0x4 RECOV_IDLE = Send/Receive Logical IDLE symbols HotReset substates: 0x0 HRESET_RST = Request TCRRL to send TS2 0x1 HRESET_GO = Start 12 ms timer 0x2 HRESET_ACT1 = Send/Receive TS1 Training set with Reset bit 0x3 HRESET_ACT2 = Send/Receive TS1 Training set without Reset bit 0x4 HRESET_EXIT = Send/Receive Logical IDLE symbols

TABLE 181: USB3 PORT 5 LTSSM STATE (CONTINUED)

SS_P5_LTSSM_State OFFSET: 75C0h RESET = 00h			USB3 Physical Port 5 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	Compliance substates - none Loopback substates: 0x0 LPBK_IDLE = Wait for Loop back start request 0x1 LPBK_MASTER = Host mode; wait for Loopback Exit request 0x2 LPBK_SLAVE = Client mode; wait for Loopback Exit request 0x3 LPBK_EXIT_LOC_RESP = Start Loopback exit and wait for min response from remote partner

TABLE 182: USB3 PORT 5 DC TEST REGISTER

SS_P5_TEST_PIPE_DC OFFSET: 75C1h RESET = 00h			USB3 Physical Port 5 DC Test Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DE-TR_LPBK	R/W	Transmit Detect Receiver and Loopback mode. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. Used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINA-TION	R/W	Receiver Termination Control. This signal is asynchronous. Controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	Reserved	R	Always ‘0’
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. ‘0’ = Full Swing ‘1’ = Low Swing
2	PIPE_TX-C_DRIVE_HI GH	R/W	Sets the DC state of the TX output 0: TXP = 0, TXN = 1 1: TXP = 1, TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enables Transmitter DC Drive mode
0	PIPE_TX_ELEC_I-DLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with pow-er_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either Normal Transmit mode, Electrical Idle, LFPS Transmission, or Receiver Detection).

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TABLE 183: USB3 PORT 5 TX TEST PATTERN REGISTER

SS_P5_TEST_PIPE_TX_PAT OFFSET: 75C3h RESET = 00h			USB3 Physical Port 5 TX Pattern Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always'0'
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. '0' = Disable pattern generator (normal mode. Transmit data driven over the tx_data interface) '1' = Enable pattern generator
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. Gen1 mode: 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 = CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = Custom CP9 (TS1 + Random data + 1 SKP every 354 symbols) 10 = Custom CP10 (TS1 + 1 SKP every 354 symbols) 11 = Custom CP11 (TSEQ repeated) 12 to 15 = Reserved Gen2 mode: 0 = Spec CP9 (Pseudo random data) 1 = Spec CP10 (AAh, Nyquist, not 128b132b encoded) 2 = Spec CP11 (CCh, Nyquist/2, not 128b132b encoded) 3 = Spec CP12 (LFSR15, not 128b132b encoded) 4 = Spec CP13 (64 1s / 64 0s, w/ pre, no de) 5 = Spec CP14 (64 1s / 64 0s, no pre, w/ de) 6 = Spec CP15 (64 1s / 64 0s, w/ pre, w/ de) 7 = Spec CP16 (64 1s / 64 0s, no pre, no de) 8 = Custom CP17 (Random data + SYNC OS every 16 data blocks for the first 800 blocks and then once every 14K data blocks + 3 SKP blocks every 115 blocks) 9 = Custom CP18 (Random data + SYNC OS every 32 data blocks + 2 SKP blocks every 80 blocks) 10 to 15 = Reserved

TABLE 184: USB3 PORT 5 TX_MARGIN

SS_P5_TEST_PIPE_CTL_0 OFFSET: 75D0h RESET = 00h			USB3 Physical Port 5 TX Margin Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always '0'. Do not modify.

TABLE 184: USB3 PORT 5 TX_MARGIN (CONTINUED)

SS_P5_TEST_PIPE_CTL_0 OFFSET: 75D0h RESET = 00h			USB3 Physical Port 5 TX Margin Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
6:4	PIPE_TX_MARGIN[2:0]	R/W	Physical Port 5 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 = +33% 100 = –67% 101 = –64% 110 = –61% 111 = –57%
3:0	Reserved	R	Always ‘0’. Do not modify.

TABLE 185: USB3 PORT 5 GEN1 DEEMPHASIS

SS_P5_PIPE_TX_DEEMPH_CTL OFFSET: 76A0h RESET = 40030C1h			USB3 Physical Port 5 Gen1 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:27	Reserved	R	Always ‘0’
26	USB3_PIPE_DEEMPH_POST_EN	R/W	TX Post-Emphasis enable for Gen1
25	USB3_PIPE_DEEMPH_PRE_EN	R/W	TX Pre-Emphasis enable for Gen1
24:14	Reserved	R	Always ‘0’
13:12	POST_FFE_CONTROL	R/W	00 = +2.7 dB from default 01 = +1.8 dB from default 10 = +0.9 dB from default 11 = Default (–3.8 dB)
11:8	Reserved	R	Always ‘0’.
7:6	TX_SWING	R	0 = 526 mV 1 = 687 mV 2 = 857 mV 3 = 970 mV (Default)
5:2	Reserved	R	Always ‘0’.
1:0	PRE_FFE_CONTROL	R/W	00 = –1.5 dB from default 01 = –1 dB from default 10 = –0.5 dB from default 11 = Default (2 dB)

TABLE 186: USB3 PORT 5 GEN2 DEEMPHASIS

SS_P5_PIPE_TX_DEEMP_GEN2_CTL OFFSET: 76B8h RESET = 60030C1h			USB3 Physical Port 5 Gen2 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:27	Reserved	R	Always ‘0’

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TABLE 186: USB3 PORT 5 GEN2 DEEMPHASIS (CONTINUED)

SS_P5_PIPE_TX_DEEMP_GEN2_CTL OFFSET: 76B8h RESET = 60030C1h			USB3 Physical Port 5 Gen2 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
26	USB3_PIPE_DEEM-PH_-GEN2_POST_EN	R/W	TX Post-Emphasis enable for Gen2
25	USB3_PIPE_DEEM-PH_GEN2_PRE_EN	R/W	TX Pre-Emphasis enable for Gen2
24:14	Reserved	R	Always ‘0’
13:12	POST_FFE_CON-TROL	R/W	00 = +2.7 dB from default 01 = +1.8 dB from default 10 = +0.9 dB from default 11 = Default (–3.1 dB)
11:8	Reserved	R	Always ‘0’.
7:6	TX_SWING	R/W	0 = 526 mV 1 = 687 mV 2 = 857 mV 3 = 970 mV (Default)
5:2	Reserved	R	Always ‘0’
1:0	PRE_FFE_CON-TROL	R/W	00 = –1.5 dB from default 01 = –1 dB from default 10 = –0.5 dB from default 11 = Default (2 dB)

TABLE 187: USB 2.0 DOWNSTREAM PORT 6 PHYBOOST REGISTER

HS_P6_BOOST OFFSET: 78CAh RESET = 00h			USB 2.0 Downstream Physical Port 6 PHYBoost Register Base Address: BF80_0000h
BIT	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS Output Current Adjustment 000b = Nominal 001b = Decrease by 5% 00b = Increase by 10% 011b = Increase by 5% 100b = Increase by 20% 101b = Increase by 15% 110b = Increase by 30% 111b = Increase by 25%

TABLE 188: USB 2.0 DOWNSTREAM PORT 6 VARISENSE™ REGISTER

HS_P6_SENSE OFFSET: 78CCh RESET = 00h			USB 2.0 Downstream Physical Port 6 VariSense Register Base Address: BF80_0000h
BIT	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE	R/W	USB 2.0 AFE HS Disconnect Tune - revision C silicon only Allows the HS disconnect threshold to be increased. Recommended to be used only when PHYBoost is also set. 0 = Nominal 575 mV Trip Point 1 = Increase by 50 mV 2 = Increase by 100 mV 3 = Increase by 125 mV
5:3	Reserved	R	Reserved
2:0	HS_SENSE	R/W	HS VariSense Tune (Squelch Tune) 000b = Nominal 100 mV Trip Point 001b = Decrease by 12.5 mV 00b = Decrease by 25 mV 011b = Decrease by 37.5 mV 100b = Decrease by 50 mV 101b = Decrease by 62.5 mV 110b = Increase by 25 mV 111b = Increase by 12.5 mV

TABLE 189: USB3 PORT 6 TX PRE-DRIVER

SS_P6_AFE_TEST_IN4 OFFSET: 7886h RESET = 00h			USB3 Physical Port 6 TX Pre-Driver Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved. Do no modify.
2:1	PRE_DRIVER	R/W	Physical Port 6 Transmitter Pre-Driver current adjust 00 = 100 µA (default biasing) 01 = 125 µA 10 = 87.5 µA 11 = 112.5 µA
0	Reserved	R	Reserved. Do no modify.

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TABLE 190: USB3 PORT 6 LTSSM STATE

SS_P6_LTSSM_State OFFSET: 79C0h RESET = 00h			USB3 Physical Port 6 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	LTSSM_STATE	R	Physical Port 6 LTSSM state. 0000b = U0 (no substates) 0001b = U1 (no substates) 0010b = U2 (no substates) 0011b = U3 (no substates) 0100b = SS.Disabled (see substate below) 0101b = Rx.Detect (see substate below) 0110b = SS.Inactive (see substate below) 0111b = Polling (see substate below) 1000b = Recovery (see substate below) 1001b = HotReset (see substate below) 1010b = Compliance (no substates) 1011b = Loopback (no substates)

TABLE 190: USB3 PORT 6 LTSSM STATE (CONTINUED)

SS_P6_LTSSM_State OFFSET: 79C0h RESET = 00h			USB3 Physical Port 6 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	Physical Port 6 LTSSM substate. Undefined values are invalid. U0 substates: none U1 substates: 0x0 U1 POWER = PHY Power state P0 -> P1 request 0x1 U1_POWER_A = Wait for PHY power change done 0x2 U1_ACTIVE = Wait for remote/local U1 exit 0x3 U1_EXIT_LOC_RESP = Start U1 exit and wait for min response from remote partner 0x4 U1_EXIT_LOC_FIN = Locally initiated U1 exit; send min required U1 exit 0x5 U1_EXIT_REM = Remote initiated U1 exit; send min required U1 exit 0x6 U1_EXIT_P0 = PHY Power state P1 -> P0 request 0x7 U1_EXIT_P0_A = Wait for PHY power change P1 -> P0 done 0x8 U1_EXIT_DONE = U1 exit successful. U1 -> Recovery U2 substates: 0x0 U2_POWER = PHY Power state P0 -> P2 request 0x1 U2_POWER2 = Wait for PHY power change done 0x2 U2_ACTIVE = Wait for remote/local U2 exit 0x3 U2_ACTIVE_0 = Request to start receiver detection 0x4 U2_ACTIVE_1 = Wait for Receiver detection response 0x5 U2_EXIT_LOC_RESP = Start U2 exit and wait for min response from remote partner 0x6 U2_EXIT_LOC_FIN = Locally initiated U2 exit; send min required U2 exit 0x7 U2_EXIT_REM = Remote initiated U2 exit; send min required U2 exit 0x8 U2_EXIT_P0 = PHY Power state P2 -> P0 request 0x9 U2_EXIT_P0_A = Wait for PHY power change P1 -> P0 done 0xA U2_EXIT_DONE = U2 exit successful. U2 -> Recovery U3 substates: 0x0 U3_POWER = PHY Power state P0 -> P2/P3 request 0x1 U3_POWER3 = Wait for PHY power change done 0x2 U3_ACTIVE = Wait for remote/local U3 exit 0x3 U3_ACTIVE_0 = Request to start receiver detection 0x4 U3_ACTIVE_1 = Wait for Receiver detection response 0x5 U3_EXIT_LOC_POW = PHY Power state P3 -> P0 -> P2 request 0x6 U3_EXIT_LOC_POW_A = Wait for PHY power change done 0x7 U3_EXIT_LOC_RESP = Start U3 exit and wait for min response from remote partner 0x8 U3_EXIT_LOC_FIN = Locally initiated U3 exit; send min required U3 exit 0x9 U3_EXIT_REM_POW = PHY Power state P3 -> P0 -> P2 request 0xA U3_EXIT_REM_POW_A = Wait for PHY power change done 0xB U3_EXIT_REM = Remote initiated U3 exit; send min required U3 exit 0xC U3_EXIT_P0 PHY = Power state P2/P3 -> P0 request 0xD U3_EXIT_P0_A = Wait for PHY power change P2/P3 -> P0 done 0xE U3_EXIT = Received remote/local U3 exit 0xF U3_EXIT_DONE = U3 exit successful. U3 -> Recovery

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TABLE 190: USB3 PORT 6 LTSSM STATE (CONTINUED)

SS_P6_LTSSM_State OFFSET: 79C0h RESET = 00h			USB3 Physical Port 6 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	SS.Disabled substates: 0x0 ESSD_POWER3 = PHY Power state P2/P3 request 0x1 ESSD_POWER3A = Wait for PHY power change done 0x2 ESSD_MAIN = Wait for RUN/STOP bit 0x3 ESSD_RATE = Wait for rate change 0x4 ESSD_POWER2 = Wait for PHY Power state P2/P3 request Rx.Detect substates: 0x0 RXD_INIT PHY = Power state P2 request 0x1 RXD_POWER2 = Wait for PHY power change done 0x2 RXD_RESET = Warm Reset 0x3 RXD_ACTIVE0 = Request to start receiver detection 0x4 RXD_ACTIVE1 = Wait for Receiver detection response 0x5 RXD_QUIET = Wait for 12 ms-timer timeout 0x6 RXD_RATE = Wait for rate change SS.Inactive substates: 0x0 ESSI_RESET = PHY Power state P0 -> P2 request 0x1 ESSI_POWER2 = Wait for PHY power change done 0x2 ESSI_QUIET0 = Start 12 ms timer 0x3 ESSI_QUIET1 = Wait for 12 ms-timer timeout 0x4 ESSI_DIS_DET0 = Request to start receiver detection 0x5 ESSI_DIS_DET1 = Wait for Receiver detection response Polling substates: 0x0 POLL_RESET = PHY Power state P0 request 0x1 POLL_POWER0 = Wait for PHY power change done 0x2 POLL_LFPS = Send/Receive Poll.LFPS 0x3 POLL_LFPSPLUS = Send/Receive SCD2 0x4 POLL_PMATCH = Send/Receive LBPM PHY capability 0x5 POLL_PCONFIG = Change rate and Send/Receive LBPM PHY ready 0x6 POLL_UPDATE_RATE = Wait for rate changed 0x7 POLL_RXEQ = Send/Receive TSEQ Training set 0x8 POLL_ACTIVE = Send/Receive TS1 Training set 0x9 POLL_CONFIG = Send/Receive TS2 Training set 0xA POLL_IDLE = Send/Receive Logical IDLE symbols Recovery substates: 0x0 RECOV_RESET = PHY Power state P0 request 0x1 RECOV_POWER0 = Wait for PHY power change done 0x2 RECOV_ACTIVE = Send/Receive TS1 Training set 0x3 RECOV_CONFIG = Send/Receive TS2 Training set 0x4 RECOV_IDLE = Send/Receive Logical IDLE symbols HotReset substates: 0x0 HRESET_RST = Request TCRRL to send TS2 0x1 HRESET_GO = Start 12 ms timer 0x2 HRESET_ACT1 = Send/Receive TS1 Training set with Reset bit 0x3 HRESET_ACT2 = Send/Receive TS1 Training set without Reset bit 0x4 HRESET_EXIT = Send/Receive Logical IDLE symbols

TABLE 190: USB3 PORT 6 LTSSM STATE (CONTINUED)

SS_P6_LTSSM_State OFFSET: 79C0h RESET = 00h			USB3 Physical Port 6 LTSSM State Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
3:0	LTSSM_SUB_STATE	R	Compliance substates - none Loopback substates: 0x0 LPBK_IDLE = Wait for Loop back start request 0x1 LPBK_MASTER = Host mode; wait for Loopback Exit request 0x2 LPBK_SLAVE = Client mode; wait for Loopback Exit request 0x3 LPBK_EXIT_LOC_RESP = Start Loopback exit and wait for min response from remote partner

TABLE 191: USB3 PORT 6 DC TEST REGISTER

SS_P6_TEST_PIPE_DC OFFSET: 79C1h RESET = 00h			USB3 Physical Port 6 DC Test Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	PIPE_TX_DE-TR_LPBK	R/W	Transmit Detect Receiver and Loopback mode. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. Used to tell the PHY to begin receiver loopback or to signal LFPS during polling.
6	PIPE_RX_TERMINA-TION	R/W	Receiver Termination Control. This signal is asynchronous. Controls presence of receiver terminations. ‘0’ = Terminations removed ‘1’ = Terminations present
5:4	Reserved	R	Always ‘0’
3	PIPE_TX_SWING	R/W	Transmit Swing Control. This signal is asynchronous. ‘0’ = Full Swing ‘1’ = Low Swing
2	PIPE_TX-C_DRIVE_HI GH	R/W	Sets the DC state of the TX output 0: TXP = 0, TXN = 1 1: TXP = 1, TXN = 0
1	PIPE_TXDC_EN ABLE	R/W	Enables the Transmitter DC Drive mode
0	PIPE_TX_ELEC_I-DLE	R/W	Transmit Electrical Idle. This signal is synchronous to pclk in P0, P1, and P2 modes and asynchronous in P3 mode. This signal is used in conjunction with pow-er_down[1:0] and tx_detrx_lpbk to set the state of the transmitter (either Normal Transmit mode, Electrical Idle, LFPS Transmission, or Receiver Detection).

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TABLE 192: USB3 PORT 6 TX TEST PATTERN REGISTER

SS_P6_TEST_PIPE_TX_PAT OFFSET: 79C3h RESET = 00h			USB3 Physical Port 6 TX Pattern Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always'0'
4	PIPE_TX_CGEN_EN	R/W	Internal Transmit Pattern Generator Enable. This signal is asynchronous. '0' = Disable pattern generator (normal mode. Transmit data driven over the tx_data interface) '1' = Enable pattern generator
3:0	PIPE_TX_CPGEN_-SEL	R/W	Internal Transmit Pattern Generator Select. This signal is asynchronous. Gen1 mode: 0 = CP0 (D0.0, scrambled, no SKP) 1 = CP1 (D10.2, Nyquist frequency) 2 = CP2 (D24.3, Nyquist/2 frequency) 3 = CP3 (K28.5, COM pattern) 4 = CP4 (LFPS) 5 = CP5 (K28.7, with de-emphasis) 6 = CP5 (K28.7, without de-emphasis) 7 = CP7 (50-250 1's and 0's, with de-emphasis) 8 = CP8 (50-250 1's and 0's, no de-emphasis) 9 = Custom CP9 (TS1 + Random data + 1 SKP every 354 symbols) 10 = Custom CP10 (TS1 + 1 SKP every 354 symbols) 11 = Custom CP11 (TSEQ repeated) 12 to 15 = Reserved Gen2 mode: 0 = Spec CP9 (Pseudo random Data) 1 = Spec CP10 (AAh, Nyquist, not 128b132b encoded) 2 = Spec CP11 (CCh, Nyquist/2, not 128b132b encoded) 3 = Spec CP12 (LFSR15, not 128b132b encoded) 4 = Spec CP13 (64 1s / 64 0s, w/ pre, no de) 5 = Spec CP14 (64 1s / 64 0s, no pre, w/ de) 6 = Spec CP15 (64 1s / 64 0s, w/ pre, w/ de) 7 = Spec CP16 (64 1s / 64 0s, no pre, no de) 8 = Custom CP17 (Random data + SYNC OS every 16 data blocks for the first 800 blocks and then once every 14K data blocks + 3 SKP blocks every 115 blocks) 9 = Custom CP18 (Random data + SYNC OS every 32 data blocks + 2 SKP blocks every 80 blocks) 10 to 15 = Reserved

TABLE 193: USB3 PORT 6 TX_MARGIN

SS_P6_TEST_PIPE_CTL_0 OFFSET: 79D0h RESET = 00h			USB3 Physical Port 6 TX Margin Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Always '0'. Do not modify.

TABLE 193: USB3 PORT 6 TX_MARGIN (CONTINUED)

SS_P6_TEST_PIPE_CTL_0 OFFSET: 79D0h RESET = 00h			USB3 Physical Port 6 TX Margin Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
6:4	PIPE_TX_MARGIN[2:0]	R/W	Physical Port 6 transmitter biasing and amplitude adjust 000 = 0% change (default) 001 = +11% 010 = +21% 011 = +33% 100 = –67% 101 = –64% 110 = –61% 111 = –57%
3:0	Reserved	R	Always ‘0.’ Do not modify.

TABLE 194: USB3 PORT 6 GEN1 DEEMPHASIS

SS_P6_PIPE_TX_DEEMPH_CTL OFFSET: 7AA0h RESET = 40030C1h			USB3 Physical Port 6 Gen1 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:27	Reserved	R	Always ‘0’
26	USB3_PIPE_DEEMPH_POST_EN	R/W	TX Post-Emphasis enable for Gen1
25	USB3_PIPE_DEEMPH_PRE_EN	R/W	TX Pre-Emphasis enable for Gen1
24:14	Reserved	R	Always ‘0’
13:12	POST_FFE_CONTROL	R/W	00 = +2.7 dB from default 01 = +1.8 dB from default 10 = +0.9 dB from default 11 = Default (–3.8 dB)
11:8	Reserved	R	Always ‘0’
7:6	TX_SWING	R/W	0 = 526 mV 1 = 687 mV 2 = 857 mV 3 = 970 mV (Default)
5:2	Reserved	R	Always ‘0’
1:0	PRE_FFE_CONTROL	R/W	00 = –1.5 dB from default 01 = –1 dB from default 10 = –0.5 dB from default 11 = Default (2 dB)

TABLE 195: USB3 PORT 6 GEN2 DEEMPHASIS

SS_P6_PIPE_TX_DEEMP_GEN2_CTL OFFSET: 7AB8h RESET = 60030C1h			USB3 Physical Port 6 Gen2 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:27	Reserved	R	Always ‘0’

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TABLE 195: USB3 PORT 6 GEN2 DEEMPHASIS (CONTINUED)

SS_P6_PIPE_TX_DEEMP_GEN2_CTL OFFSET: 7AB8h RESET = 60030C1h			USB3 Physical Port 6 Gen2 Deemphasis Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
26	USB3_PIPE_DEEMPH_-GEN2_POST_EN	R/W	TX Post-Emphasis enable for Gen2
25	USB3_PIPE_DEEMPH_GEN2_PRE_EN	R/W	TX Pre-Emphasis enable for Gen2
24:14	Reserved	R	Always ‘0’
13:12	POST_FFE_CONTROL	R/W	00 = +2.7 dB from default 01 = +1.8 dB from default 10 = +0.9 dB from default 11 = Default (–3.1 dB)
11:8	Reserved	R	Always ‘0’.
7:6	TX_SWING	R/W	0 = 526 mV 1 = 687 mV 2 = 857 mV 3 = 970 mV (Default)
5:2	Reserved	R	Always ‘0’
1:0	PRE_FFE_CONTROL	R/W	00 = –1.5 dB from default 01 = –1 dB from default 10 = –0.5 dB from default 11 = Default (2 dB)

TABLE 196: HFC PRODUCT ID LSB

HFC_PID_LSB OFFSET: 2866h RESET = Varies			HFC Product ID LSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	HFC_PID_LSB	R/W	Least Significant Byte of the HFC Product ID. This is a 16-bit value that uniquely identifies this HFC device. The default value depends on the features enabled on the device as shown below: I^2S™ Audio only = 42h I^2S Audio/HID = 43h CDC = 44h I^2S, CDC = 46h I^2S Audio/HID, CDC = 47h WinUSB only = 40h I^2S Audio, WinUSB = 4Ah I^2S Audio/HID, WinUSB = 4Bh WinUSB, CDC = 4Ch I^2S Audio, WinUSB, CDC = 4Eh I^2S Audio/HID, WinUSB, CDC = 4Fh

TABLE 197: HFC PRODUCT ID MSB

HFC_PID_MSB OFFSET: 2867h RESET = 3C			HFC Product ID MSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	HFC_PID_MSB	R/W	Most Significant Byte of the HFC Product ID. This is a 16-bit value that uniquely identifies this HFC device.

TABLE 198: HFC VENDOR ID LSB

HFC_VID_LSB OFFSET: 2864h RESET = 24h			HFC Vendor ID LSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	HFC_DID_LSB	R/W	Least Significant Byte of the HFC Product ID. This is a 16-bit value that identifies the vendor of the product (as registers with USB-IF).

TABLE 199: HFC VENDOR ID MSB

HFC_VID_MSB OFFSET: 2865h RESET = 04h			HFC Vendor ID MSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	HFC_DID_MSB	R/W	Most Significant Byte of the HFC Product ID. This is a 16-bit value that identifies the vendor of the product (as registers with USB-IF).

TABLE 200: HFC DEVICE ID (BCDDEVICE) LSB

HFC_PID_MSB OFFSET: 2868h RESET = Varies by device			Hub Feature Controller Device ID LSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	HFC_DID_LSB	R/W	Least Significant Byte of the HFC Device ID. This is a 16-bit value that is used for firmware or device revision tracking purposes.

Note 1: The default Device ID may change with silicon or firmware revisions.

TABLE 201: HFC DEVICE ID (BCDDEVICE) MSB

HFC_PID_MSB OFFSET: 2869h RESET = Varies by device			Hub Feature Controller Device ID MSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	HFC_DID_MSB	R/W	Most Significant Byte of the HFC Product ID. This is a 16-bit value that is used for firmware or device revision tracking purposes.

Note 1: The default Device ID may change with silicon or firmware revisions.

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TABLE 202: USB2.0 HFC MANUFACTURER STRING INDEX REGISTER

HFC_MFR_STR_INDEX OFFSET: 286Ah RESET = 10h			Hub Feature Controller Manufacturer String Index Register Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	MFR_STR_INDEX	R/W	Manufacturer String Index Set = '00b' if unused

TABLE 203: USB2.0 HFC PRODUCT STRING INDEX REGISTER

HFC_PRD_STR_INDEX OFFSET: 286Bh RESET = 02h			Hub Feature Controller Product String Index Register Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PRD_STR_INDEX	R/W	Product String Index Set = '00b' if unused

TABLE 204: USB2.0 HFC SERIAL STRING INDEX REGISTER

HFC_SER_STR_INDEX OFFSET: 286Ch RESET = 00h			Hub Feature Controller Serial String Index Register Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	SER_STR_INDEX	R/W	Serial String Index Set = '00b' if unused

TABLE 205: HFC LANG_ID[15:0] LANGUAGE IDENTIFIER

HFC_LANG_ID OFFSET: 28FAh RESET = 0409h			HFC USB-IF Language Identifier Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
15:0	LANG_ID	R/W	USB-IF Language Identifier. Default is English (United States).

Note 1: 28FAh-[7:0], 28FBh-[15:8]

TABLE 206: HFC PRODUCT STRING DESCRIPTOR CONTAINER

HFC_STR_CONTAINER OFFSET: 28FCh			USB2.0 HFC String Container Base Address: BFD2_0000h
Byte	**Name**	**R/W**	**Description**
95:0	Length	R/W	Container for All HFC Strings. This must follow the formatting as described in the *USB2.0 Specification* for string descriptors. All Hub Feature Controller product, manufacturer, and serial string are contained within this register array.

Note 1: 28FCh-[7:0], 28FDh-[15:8], 28FEh-[23:16], 28FFh-[31:24], 2900h-[39:32],... 295Bh-[95:88]

TABLE 207: USB2.0 HUB LANG_ID[15:0] LANGUAGE IDENTIFIER

USB2_HUB_LANG_ID OFFSET: 3202h RESET = 0409h			USB2.0 Hub USB-IF Language Identifier Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
15:0	LANG_ID	R/W	USB-IF Language Identifier. Default is English (United States).

Note 1: 3202h-[7:0], 3203h-[15:8]

TABLE 208: USB2.0 HUB STRING DESCRIPTOR CONTAINER

USB2_HUB_STR_CONTAINER OFFSET: 3204h			USB2.0 Hub String Container Base Address: BFD2_0000h
Byte	**Name**	**R/W**	**Description**
95:0	Length	R/W	Container for All USB2.0 Hub Strings. This must follow the formatting as described in the *USB2.0 Specification* for string descriptors. All Hub Feature Controller Product, Manufacturer, and Serial string are contained within this register array.

Note 1: 3204h-[7:0], 3205h-[15:8], 3206h-[23:16], 3207h-[31:24], 3208h-[39:32],... 3263h-[95:88]

TABLE 209: RUNTIME FLAGS MEMORY

RUNTIME_FLAGS OFFSET: 3400h RESET = 08426228h			Runtime Flags Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
31:28	RESERVED	R	Reserved. Do not modify.
27	GEN_EXCEPTION_RESET	R/W	'1' = If an exception occurs, reset the hub. '0' = If an exception occurs, code execution gets stuck in an infinite loop.
26	RESERVED	R	Reserved. Do not modify.
25	SS_MUX_FLIPPED	R/W	'1' = Enable SS MUX flipped '0' = Disable SS MUX flipped ROM default value is 0.
24	RESERVED	R	Reserved. Do not modify.
23	DISABLE_CDP_MULTIPLE_HANDSHAKE	R/W	'1' = Except the primary handshake in CDP mode, subsequent handshake by the downstream device while in CDP mode will be ignored by the firmware. '0' = Multiple handshakes by the downstream device while in CDP mode will be acknowledged by the firmware until a time period of BC_CDP_MULTIPLE_HANDSHAKE_TIMEOUT expires after the first handshake in CDP mode.
22	ENABLE_QUADSPI	R/W	'0' = Quad SPI support is disabled in the firmware. '1' = Quad SPI support is enabled in the firmware.
21	DISABLE_I2CM_PULLUP_CHECK	R/W	'0' = Presence of I^2C pull-up resistors will be checked prior to I^2C bridging and in any other operation involving the hub as I^2C host. '1' = Presence of I^2C pull-up resistors will not be checked prior to I^2C bridging and in any other operation involving the hub as I^2C host.

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TABLE 209: RUNTIME FLAGS MEMORY (CONTINUED)

RUNTIME_FLAGS OFFSET: 3400h RESET = 08426228h			Runtime Flags Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
20	DISABLE_USB3HUB	R/W	Flag to disable USB3 hub ‘0’ = USB3 hub is enabled. ‘1’ = USB3 hub is disabled. Default ROM value is 0.
19	ENABLE_POWERSAVE	R/W	‘1’ = The clock control bits mentioned below will be turned off by the firmware, when not required. ‘0’ = The clock control bits mentioned below will not be turned off by the firmware, once turned on. UDC1_CLK_EN_DUR_SUSPEND UDC2_CLK_EN_DUR_SUSPEND
18:14	RESERVED	R	Reserved
13	ENABLE_CDP_TO_SDP_RECOV-ERY	R/W	‘1’ = Toggle downstream VBUS when a downstream device does not enumerate in CDP mode. ‘0’ = Do not toggle downstream VBUS when a downstream device does not enumerate in CDP mode. Note that by default in ROM, the flag is 1 to ensure that downstream device enumeration is prioritized. This bit needs to be cleared to zero to run battery charging compliance tests using PET tester.
12	OTP_LOCK	R/W	When set, this is a soft lock of the OTP.
11	DISABLE_CDC_REMOTEWAKE-UP_FEATURE	R/W	‘0’ = CDC interface if enabled, reports as remote wakeup-capable. ‘1’ = CDC interface is enabled, does not report as remote wakeup-capable.
10	DISABLE_125K_PU	R/W	‘0’ = 125K pull-up resistors are enabled in China-mode battery charging. ‘1’ = 125K pull-up resistors are disabled in China-mode battery charging.
9	ENABLE_BC_UNIVERSAL	R/W	‘0’ = Disable BC 1.2-compliant changes to Universal BC algorithm ‘1’ = Enable BC 1.2-compliant changes to Universal BC algorithm regardless of BC12_DCP bit in Runtime BC Flags (0x413X) If this is set to 1, then the HEARTBEAT_UNIT will be 5 ms. If this is set to 0, then the HEARTBEAT_UNIT will be 10 ms.
8	RESERVED	R	Reserved. Do not modify
7	ENABLE_SPI_BYTE_FLASH	R/W	‘0’ = Generic SPI Flash commands issued for SPI Flash programming ‘1’ = Microchip Byte Flash commands issued for SPI Flash programming
6	BYPASS_MCU_SUSPEND	R/W	‘0’ = Default UDC suspend handling ‘1’ = MCU will not handle UDC suspend and will ignore the same. Note that if there is a suspend hook function present, that will still be invoked.

TABLE 209: RUNTIME FLAGS MEMORY (CONTINUED)

RUNTIME_FLAGS OFFSET: 3400h RESET = 08426228h			Runtime Flags Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
5	TARGET_OTP	R/W	Set target OTP ‘0’ = Any command targeted to OTP (OTP read, OTP programming, and so on) is redirected to the pseudo OTP in SPI Flash physical address 0x40000 to 0x41FFF. ‘1’ = Any command targeted to OTP (OTP read, OTP programming, and so on) is directed to the OTP.
4	CFG_FROM_SPI	R/W	Load config from SPI ‘1’ = Configuration is loaded from pseudo OTP in SPI. ‘0’ = Configuration will not be loaded from pseudo OTP in SPI.
3	CFG_FROM_OTP	R/W	Load config from OTP ‘1’ = The firmware will load configuration from OTP. ‘0’ = Configuration will not be loaded from OTP.
2	HUB_CFG_CLK	R/W	Enable Hubcfg interface power-down ‘1’ = Clock-to-hub Configuration registers are turned off after hub-attach to USB. ‘0’ = Clock-to-hub Configuration registers are left on.
1	UPDRESET_THROUGH_GPIO	R/W	Reserved, do not modify
0	DISABLE_BC	R/W	Disable battery charging ‘1’ = Battery charging logic is completely disabled. ‘0’ = Battery charging logic is left enabled based on other flags. ROM default is 0.

TABLE 210: RUNTIME FLAGS 2 MEMORY

RUNTIME_FLAGS2 OFFSET: 3408h RESET = 01C81000h			Runtime Flags 2 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
31:14	RESERVED	R	Reserved. Do not modify.
13	SPIPASSTHRU_RUN_FROM_ROM	R/W	Flag to enable SPI pass-through function running from SPI or ROM ‘0’ = Running from SPI ‘1’ = Running from ROM
12	PORTSPLIT_ENABLE_LTSSM_-CHECK	R/W	Flag to disable LTSSM state machine ‘1’ = LTSSM state check enabled ‘0’ = LTSSM state check disabled ROM default value is 1.

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TABLE 210: RUNTIME FLAGS 2 MEMORY (CONTINUED)

RUNTIME_FLAGS2 OFFSET: 3408h RESET = 01C81000h			Runtime Flags 2 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
11	I2CM_READ_MODE_INT	R/W	Flag to use Polling or Interrupt mode ‘1’ = Interrupt mode ‘0’ = Polling mode ROM default value is 1.
10	I2CM_WRITE_MODE_INT	R/W	Flag to use Polling or Interrupt mode ‘1’ = Interrupt mode ‘0’ = Polling mode ROM default value is 1.
9	BILLBOARD_ENABLE	R/W	Billboard Device functionality enable ‘0’ = Billboard Device functionality disabled ‘1’ = Billboard Device functionality enabled ROM default value is 0. See Section 6.0, "Physical and Logical Port Mapping" for more details.
8	DISABLE_UDC0_PORT	R/W	Flag to disable UDC0 port ‘0’ = UDC0 port is enabled. ‘1’ = UDC0 port is disabled. ROM default value is 0.
7	ENABLE_HIDBRIDGE	R/W	Flag to enable HID interface ‘0’ = HID interface is disabled. ‘1’ = HID interface is enabled. ROM default value is 0.
6:5	RESERVED	R	Reserved, do not modify
4	CDC_DISABLE	R/W	Flag to disable CDC interface when CDC configuration is selected through CFG_STRAP ‘0’ = Not valid ‘1’ = CDC interface is disabled in CDC mode ROM default value is 0.
3	I2S_DISABLE	R/W	Flag to disable I^2S™ interface when I^2S configuration is selected through CFG_STRAP ‘0’ = Not valid ‘1’ = I^2S interface is disabled in I^2S mode ROM default value is 0.
2	CONFIG_PORT_SPLIT	R/W	Flag to enable Port Split ‘0’ = Port Split interface is disabled. ‘1’ = Port Split interface is enabled. ROM default value is 0.
1	OTP_BASED_UDC_CONFIG	R/W	Flag to disable UDC configuration by ROM ‘0’ = UDC port is configured by ROM. ‘1’ = UDC port is configured by OTP/SMBus. ROM default value is 0.

TABLE 210: RUNTIME FLAGS 2 MEMORY (CONTINUED)

RUNTIME_FLAGS2 OFFSET: 3408h RESET = 01C81000h			Runtime Flags 2 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
0	HFC_DISABLE	R/W	Flag to disable the Hub Feature Controller (HFC) ‘0’ = HFC is enabled. ‘1’ = HFC is disabled. Default ROM value is 0.

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TABLE 211: I2S FEATURE SELECT REGISTER

I2S_FEAT_SEL OFFSET: 3412h RESET = 03h			I^2S Feature Unit Select Register Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	I2S_UNIT_SEL	R/W	Control features of the I^2S interface if an I^2S configuration is selected 00h = I^2S is disabled. 01h = Audio IN through microphone is enabled. 02h = Audio OUT is enabled. 03h = Both Audio IN are enabled. All other values are reserved.

TABLE 212: I2S HID FEATURE SELECT REGISTER

I2S_HFEAT_SEL OFFSET: 3413h RESET = 00h			I^2S HID Feature Select Register Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	I2S_HID_SEL	R/W	Control features of the HID Control of the I^2S interface if an I^2S configuration is selected 00h = No I^2S HID control 01h = Reserved 02h = HID interface controls speaker mute 03h = HID interface controls speaker mute and microphone mute All other values are reserved.

TABLE 213: SMBUS OTP RESULT

SMBUS_OTP_RES OFFSET: 3419h RESET = 00h			SMBUS OTP Result Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:1	RESERVED	R	Always ‘0’
0	RESULT	R	Result of the last OTP command received through SMBus ‘0’ = Command completed successfully ‘1’ = Command failed

TABLE 214: OTP UDC ENUMERATION

OTP_UDC_ENABLE OFFSET: 341Bh RESET = 00h			OTP UDC Enumeration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	MODE	R/W	Controls UDC Enumeration. 00h = No change from default ROM behavior 01h = Enable UDC enumeration 02h = Disable UDC enumeration All other values are reserved.

TABLE 215: HUB PID MSB

HUB_DEF_PIDM OFFSET: 341Eh RESET = 01h			Primary Hub Default PID MSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PRIH_PIDM	R/W	USB Primary Hub Default PID MSB. Reflects the SKU based on the bond and strap options, and could be different from the product PID.

TABLE 216: HUB PID LSB

HUB_DEF_PIDL OFFSET: 341Fh RESET = 00h			Primary Hub Default PID LSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PRIH_PIDL	R/W	USB Primary Hub Default PID LSB. Reflects the SKU based on the bond and strap options, and could be different from the product PID.

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TABLE 217: PORT 1 BATTERY CHARGING CONFIGURATION

BC_CONFIG_P1 OFFSET: 3433h RESET = Depends on CFG_BC_EN strap settings			Port 1 Battery Charging Configuration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:6	UCS_LIM	R/W	When controlling UCS through I^2C, this sets the current limit. 00b = 500 mA 01b = 1000 mA 10b = 1500 mA 11b = 2000 mA
5	DCP	R/W	USB-IF Dedicated Charging Mode Enable. If bit 4 is set, this bit is ignored. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. ‘0 ‘= DCP disabled ‘1’ = DCP enabled
4	CHINA_MODE	R/W	China mode. Enables a 125k pull-up to D+/D– while shorting D+/D– together to allow certain Chinese market phones to charge. ‘0’ = China mode disabled ‘1’ = China mode enabled
3	Reserved	R/W	Reserved
2:1	SE1_EN[1:0]	R/W	Enables SE1 charging mode for certain devices. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. 00b = SE1 mode disabled 01b = SE1 1A mode enabled (D–: 2.7V, D+: 2.0V) 10b = SE1 2A mode enabled (D–: 2.0V, D+: 2.7V) 11b = SE1 2.5A mode enabled (D–: 2.7V, D+: 2.7V)
0	BC_EN	R/W	Battery Charging Support Enable. This bit enables CDP and must be set for any battery charging functions to be enabled. Other functions in addition to CDP are enabled by setting their respective bits in addition to this bit. ‘0‘= Battery charging support disabled ‘1’ = Battery charging support enabled

TABLE 218: PORT 2 BATTERY CHARGING CONFIGURATION

BC_CONFIG_P2 OFFSET: 3434h RESET = Depends on CFG_BC_EN strap settings			Port 2 Battery Charging Configuration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:6	UCS_LIM	R/W	When controlling UCS through I^2C, this sets the current limit. 00b = 500 mA 01b = 1000 mA 10b = 1500 mA 11b = 2000 mA
5	DCP	R/W	USB-IF Dedicated Charging Mode Enable. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. ‘0’ = DCP disabled ‘1’ = DCP enabled
4:3	CHINA_MODE	R/W	China mode. Enables a 125k pull-up to D+/D– while shorting D+/D– together to allow certain Chinese market phones to charge. ‘0’ = China mode disabled ‘1’ = China mode enabled
2:1	SE1_EN[1:0]	R/W	Enables SE1 charging mode for certain devices. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. 00b = SE1 mode disabled 01b = SE1 1A mode enabled (D–: 2.7V, D+: 2.0V) 10b = SE1 2A mode enabled (D–: 2.0V, D+: 2.7V) 11b = SE1 2.5A mode enabled (D–: 2.7V, D+: 2.7V)
0	BC_EN	R/W	Battery Charging Support Enable. This bit enables CDP and must be set for any battery charging functions to be enabled. Other functions in addition to CDP are enabled by setting their respective bits in addition to this bit. 0 = Battery charging support disabled 1 = Battery charging support enabled

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TABLE 219: PORT 3 BATTERY CHARGING CONFIGURATION

BC_CONFIG_P3 OFFSET: 3435h RESET = Depends on CFG_BC_EN strap settings			Port 3 Battery Charging Configuration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:6	UCS_LIM	R/W	When controlling UCS through I^2C, this sets the current limit. 00b = 500 mA 01b = 1000 mA 10b = 1500 mA 11b = 2000 mA
5	DCP	R/W	USB-IF Dedicated Charging Mode Enable. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. ‘0’ = DCP disabled ‘1’ = DCP enabled
4:3	CHINA_MODE	R/W	China mode. Enables a 125k pull-up to D+/D– while shorting D+/D– together to allow certain Chinese market phones to charge. ‘0’ = China mode disabled ‘1’ = China mode enabled
2:1	SE1_EN[1:0]	R/W	Enables SE1 charging mode for certain devices. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. 00b = SE1 mode disabled 01b = SE1 1A mode enabled (D–: 2.7V, D+: 2.0V) 10b = SE1 2A mode enabled (D–: 2.0V, D+: 2.7V) 11b = SE1 2.5A mode enabled (D–: 2.7V, D+: 2.7V)
0	BC_EN	R/W	Battery Charging Support Enable. This bit enables CDP and must be set for any battery charging functions to be enabled. Other functions in addition to CDP are enabled by setting their respective bits in addition to this bit. ‘0’ = Battery charging support disabled ‘1’ = Battery charging support enabled

TABLE 220: PORT 4 BATTERY CHARGING CONFIGURATION

BC_CONFIG_P4 OFFSET: 3436h RESET = Depends on CFG_BC_EN strap settings			Port 4 Battery Charging Configuration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:6	UCS_LIM	R/W	When controlling UCS through I^2C, this sets the current limit. 00b = 500 mA 01b = 1000 mA 10b = 1500 mA 11b = 2000 mA
5	DCP	R/W	USB-IF Dedicated Charging Mode Enable. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. ‘0’ = DCP disabled ‘1’ = DCP enabled
4:3	CHINA_MODE	R/W	China mode. Enables a 125k pull-up to D+/D– while shorting D+/D– together to allow certain Chinese market phones to charge. ‘0’ = China mode disabled ‘1’ = China mode enabled
2:1	SE1_EN[1:0]	R/W	Enables SE1 charging mode for certain devices. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. 00b = SE1 mode disabled 01b = SE1 1A mode enabled (D–: 2.7V, D+: 2.0V) 10b = SE1 2A mode enabled (D–: 2.0V, D+: 2.7V) 11b =SE1 2.5A mode enabled (D–: 2.7V, D+: 2.7V)
0	BC_EN	R/W	Battery Charging Support Enable. This bit enables CDP and must be set for any battery charging functions to be enabled. Other functions in addition to CDP are enabled by setting their respective bits in addition to this bit. ‘0’ = Battery charging support disabled ‘1’ = Battery charging support enabled

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TABLE 221: PORT 5 BATTERY CHARGING CONFIGURATION

BC_CONFIG_P5 OFFSET: 3437h RESET = Depends on CFG_BC_EN strap settings			Port 5 Battery Charging Configuration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:6	UCS_LIM	R/W	When controlling UCS through I^2C, this sets the current limit. 00b = 500 mA 01b = 1000 mA 10b = 1500 mA 11b = 2000 mA
5	DCP	R/W	USB-IF Dedicated Charging Mode Enable. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. ‘0’ = DCP disabled ‘1’ = DCP enabled
4:3	CHINA_MODE	R/W	China mode. Enables a 125k pull-up to D+/D– while shorting D+/D– together to allow certain Chinese market phones to charge. ‘0’ = China mode disabled ‘1’ = China mode enabled
2:1	SE1_EN[1:0]	R/W	Enables SE1 charging mode for certain devices. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. 00b = SE1 mode disabled 01b = SE1 1A mode enabled (D–: 2.7V, D+: 2.0V) 10b = SE1 2A mode enabled (D–: 2.0V, D+: 2.7V) 11b = SE1 2.5A mode enabled (D–: 2.7V, D+: 2.7V)
0	BC_EN	R/W	Battery Charging Support Enable. This bit enables CDP and must be set for any battery charging functions to be enabled. Other functions in addition to CDP are enabled by setting their respective bits in addition to this bit. ‘0’ = Battery charging support disabled ‘1’ = Battery charging support enabled

TABLE 222: PORT 6 BATTERY CHARGING CONFIGURATION

BC_CONFIG_P6 OFFSET: 3438h RESET = Depends on CFG_BC_EN strap settings			Port 6 Battery Charging Configuration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:6	UCS_LIM	R/W	When controlling UCS through I^2C, this sets the current limit. 00b = 500 mA 01b = 1000 mA 10b = 1500 mA 11b = 2000 mA
5	DCP	R/W	USB-IF Dedicated Charging Mode Enable. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. ‘0’ = DCP disabled ‘1’ = DCP enabled
4:3	CHINA_MODE	R/W	China mode. Enables a 125k pull-up to D+/D– while shorting D+/D– together to allow certain Chinese market phones to charge. ‘0’ = China mode disabled ‘1’ = China mode enabled
2:1	SE1_EN[1:0]	R/W	Enables SE1 charging mode for certain devices. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. 00b = SE1 mode disabled 01b = SE1 1A mode enabled (D–: 2.7V, D+: 2.0V) 10b = SE1 2A mode enabled (D–: 2.0V, D+: 2.7V) 11b = SE1 2.5A mode enabled (D–: 2.7V, D+: 2.7V)
0	BC_EN	R/W	Battery Charging Support Enable. This bit enables CDP and must be set for any battery charging functions to be enabled. Other functions in addition to CDP are enabled by setting their respective bits in addition to this bit. ‘0’ = Battery charging support disabled ‘1’ = Battery charging support enabled

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TABLE 223: FLEX_IN_PORT1

FLEX_IN_PORT1 OFFSET: 3442h RESET = 00h			FlexConnect Trigger Input Configuration Port 1 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_IN_EN	R/W	This bit is used to enable FlexConnect trigger for Port 1 through the PIO input. The PIO is specified in the FLEX_IN_IO field. 0b = FlexConnect trigger is disabled. 1b = FlexConnect trigger is enabled.
6:3	RESERVED	R/W	Reserved
2:0	FLEX_IN_IO	R/W	Selects the PIO used for FlexConnect trigger 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 224: FLEX_IN_PORT2

FLEX_IN_PORT2 OFFSET: 3443h RESET = 00h			FlexConnect Trigger Input Configuration Port 2 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_IN_EN	R/W	This bit is used to enable FlexConnect trigger for Port 2 through the PIO input. The PIO is specified in the FLEX_IN_IO field. 0b = FlexConnect trigger is disabled. 1b = FlexConnect trigger is enabled.
6:3	RESERVED	R/W	Reserved
2:0	FLEX_IN_IO	R/W	Selects the PIO used for FlexConnect trigger 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 225: FLEX_IN_PORT3

FLEX_IN_PORT3 OFFSET: 3444h RESET = 00h			FlexConnect Trigger Input Configuration Port 3 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_IN_EN	R/W	This bit is used to enable FlexConnect trigger for Port 3 through the PIO input. The PIO is specified in the FLEX_IN_IO field. 0b = FlexConnect trigger is disabled. 1b = FlexConnect trigger is enabled.
6:3	RESERVED	R/W	Reserved
2:0	FLEX_IN_IO	R/W	Selects the PIO used for FlexConnect trigger 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 226: FLEX_IN_PORT4

FLEX_IN_PORT4 OFFSET: 3445h RESET = 00h			FlexConnect Trigger Input Configuration Port 4 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_IN_EN	R/W	This bit is used to enable FlexConnect trigger for Port 4 through the PIO input. The PIO is specified in the FLEX_IN_IO field. 0b = FlexConnect trigger is disabled. 1b = FlexConnect trigger is enabled.
6:3	RESERVED	R/W	Reserved
2:0	FLEX_IN_IO	R/W	Selects the PIO used for FlexConnect trigger 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

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TABLE 227: FLEX_IN_PORT5

FLEX_IN_PORT5 OFFSET: 3446h RESET = 00h			FlexConnect Trigger Input Configuration Port 5 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_IN_EN	R/W	This bit is used to enable FlexConnect trigger for Port 5 through the PIO input. The PIO is specified in the FLEX_IN_IO field. 0b = FlexConnect trigger is disabled. 1b = FlexConnect trigger is enabled.
6:3	RESERVED	R/W	Reserved
2:0	FLEX_IN_IO	R/W	Selects the PIO used for FlexConnect trigger 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 228: FLEX_IN_PORT6

FLEX_IN_PORT6 OFFSET: 3447h RESET = 00h			FlexConnect Trigger Input Configuration Port 6 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_IN_EN	R/W	This bit is used to enable FlexConnect trigger for Port 6 through the PIO input. The PIO is specified in the FLEX_IN_IO field. 0b = FlexConnect trigger is disabled. 1b = FlexConnect trigger is enabled.
6:3	RESERVED	R/W	Reserved
2:0	FLEX_IN_IO	R/W	Selects the PIO used for FlexConnect trigger 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 229: FLEX_OUT_PORT1

FLEX_OUT_PORT1 OFFSET: 3448h RESET = 00h			FlexConnect State Indicator Configuration Port 1 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	This bit is used to enable the FlexConnect state indicator for Port 1 through the PIO input. The PIO is specified in the FLEX_OUT_IO field. 0b = FlexConnect state indicator is disabled. 1b = FlexConnect state indicator is enabled.
6	FLEX_OUT ACTIVE_HIGH	R/W	Selects PIO Active state polarity 0b = PIO is driven active-low in Flexstate. 1b = PIO is driven active-high in Flexstate.
5	FLEX_OUT_OD	R/W	This bit is used to enable open-drain output. 0b = PIO output is set as standard push-pull. 1b = PIO output is set as open drain.
4:3	RESERVED	R/W	Reserved
2:0	FLEX_OUT_IO	R/W	Selects the PIO used as the FlexConnect state indicator 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 230: FLEX_OUT_PORT2

FLEX_OUT_PORT2 OFFSET: 3449h RESET = 00h			FlexConnect State Indicator Configuration Port 2 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	This bit is used to enable the FlexConnect state indicator for Port 2 through the PIO input. The PIO is specified in the FLEX_OUT_IO field. 0b = FlexConnect state indicator is disabled. 1b = FlexConnect state indicator is enabled.
6	FLEX_OUT ACTIVE_HIGH	R/W	Selects PIO Active state polarity 0b = PIO is driven active-low in Flexstate. 1b = PIO is driven active-high in Flexstate.
5	FLEX_OUT_OD	R/W	This bit is used to enable open-drain output. 0b = PIO output is set as standard push-pull. 1b = PIO output is set as open drain.
4:3	RESERVED	R/W	Reserved

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TABLE 230: FLEX_OUT_PORT2 (CONTINUED)

FLEX_OUT_PORT2 OFFSET: 3449h RESET = 00h			FlexConnect State Indicator Configuration Port 2 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
2:0	FLEX_OUT_IO	R/W	Selects the PIO used as the FlexConnect state indicator 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 231: FLEX_OUT_PORT3

FLEX_OUT_PORT3 OFFSET: 344Ah RESET = 00h			FlexConnect State Indicator Configuration Port 3 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	This bit is used to enable the FlexConnect state indicator for Port 3 through the PIO input. The PIO is specified in the FLEX_OUT_IO field. 0b = FlexConnect state indicator is disabled. 1b = FlexConnect state indicator is enabled.
6	FLEX_OUT ACTIVE_HIGH	R/W	Selects PIO Active state polarity 0b = PIO is driven active-low in Flexstate. 1b = PIO is driven active-high in Flexstate.
5	FLEX_OUT_OD	R/W	This bit is used to enable open-drain output. 0b = PIO output is set as standard push-pull. 1b = PIO output is set as open drain.
4:3	RESERVED	R/W	Reserved
2:0	FLEX_OUT_IO	R/W	Selects the PIO used as the FlexConnect state indicator 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 232: FLEX_OUT_PORT4

FLEX_OUT_PORT4 OFFSET: 344Bh RESET = 00h			FlexConnect State Indicator Configuration Port 4 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	This bit is used to enable the FlexConnect state indicator for Port 4 through the PIO input. The PIO is specified in the FLEX_OUT_IO field. 0b = FlexConnect state indicator is disabled. 1b = FlexConnect state indicator is enabled.
6	FLEX_OUT ACTIVE_HIGH	R/W	Selects PIO Active state polarity 0b = PIO is driven active-low in Flexstate. 1b = PIO is driven active-high in Flexstate.
5	FLEX_OUT_OD	R/W	This bit is used to enable open drain output. 0b = PIO output is set as standard push-pull. 1b = PIO output is set as open-drain.
4:3	RESERVED	R/W	Reserved
2:0	FLEX_OUT_IO	R/W	Selects the PIO used as the FlexConnect state indicator 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 233: FLEX_OUT_PORT5

FLEX_OUT_PORT5 OFFSET: 344Ch RESET = 00h			FlexConnect State Indicator Configuration Port 5 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	This bit is used to enable the FlexConnect state indicator for Port 5 through the PIO input. The PIO is specified in the FLEX_OUT_IO field. 0b = FlexConnect state indicator is disabled. 1b = FlexConnect state indicator is enabled.
6	FLEX_OUT ACTIVE_HIGH	R/W	Selects PIO Active state polarity 0b = PIO is driven active-low in Flexstate. 1b = PIO is driven active-high in Flexstate.
5	FLEX_OUT_OD	R/W	This bit is used to enable open-drain output. 0b = PIO output is set as standard push-pull. 1b = PIO output is set as open drain.
4:3	RESERVED	R/W	Reserved

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TABLE 233: FLEX_OUT_PORT5 (CONTINUED)

FLEX_OUT_PORT5 OFFSET: 344Ch RESET = 00h			FlexConnect State Indicator Configuration Port 5 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
2:0	FLEX_OUT_IO	R/W	Selects the PIO used as the FlexConnect state indicator 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 234: FLEX_OUT_PORT6

FLEX_OUT_PORT6 OFFSET: 344Dh RESET = 00h			FlexConnect State Indicator Configuration Port 6 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	This bit is used to enable the FlexConnect state indicator for Port 6 through the PIO input. The PIO is specified in the FLEX_OUT_IO field. 0b = FlexConnect state indicator is disabled. 1b = FlexConnect state indicator is enabled.
6	FLEX_OUT ACTIVE_HIGH	R/W	Selects PIO Active state polarity 0b = PIO is driven active-low in Flexstate. 1b = PIO is driven active-high in Flexstate.
5	FLEX_OUT_OD	R/W	This bit is used to enable open drain output. 0b = PIO output is set as standard push-pull. 1b = PIO output is set as open drain.
4:3	RESERVED	R/W	Reserved
2:0	FLEX_OUT_IO	R/W	Selects the PIO used as the FlexConnect state indicator 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 235: FLEX_PRTCTL_PORT1

FLEX_PRTCTL_PORT1 OFFSET: 344Eh RESET = 00h			FlexConnect PRTCTL Configuration Port 1 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	This bit is used to enable Flex PRTCTL for PORT 1. The PIO is specified in the FLEX_PRTCTL_IO field. 0b = Disables Flex PRTCTL1 output 1b = Enables Flex PRTCTL1 output
6:5	PRTCTL_OUT[1:0]	R/W	Selects the Flex PRTCTL1 Output mode 00b = PRTCTL1 is tristated. 01b = PRTCTL1 is driven high. 10b = PRTCTL1 is driven low. 11b = PRTCTL1 is pulled up with internal pull-up.
4	RESERVED	R/W	Reserved
3	FLEX_PRTCTL_OEN	R/W	This bit is used to enable the Flex PRTCTL1 to output. 0b = Flex PRTCTL1 output is disabled. 1b = Flex PRTCTL1 output is enabled.
2:0	FLEX_PRTCTL_IO	R/W	Selects the PIO used as Flex PRTCTL1 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

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TABLE 236: FLEX_PRTCTL_PORT2

FLEX_PRTCTL_PORT2 OFFSET: 344Fh RESET = 00h			FlexConnect PRTCTL Configuration Port 2 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	This bit is used to enable Flex PRTCTL for PORT 2. The PIO is specified in the FLEX_PRTCTL_IO field. 0b = Disables Flex PRTCTL2 output 1b = Enables Flex PRTCTL2 output
6:5	PRTCTL_OUT[1:0]	R/W	Selects the Flex PRTCTL2 Output mode 00b = PRTCTL2 is tristated. 01b = PRTCTL2 is driven high. 10b = PRTCTL2 is driven low. 11b = PRTCTL2 is pulled up with internal pull-up.
4	RESERVED	R/W	Reserved
3	FLEX_PRTCTL_OEN	R/W	This bit is used to enable the Flex PRTCTL2 to output. 0b = Flex PRTCTL2 output is disabled. 1b = Flex PRTCTL2 output is enabled.
2:0	FLEX_PRTCTL_IO	R/W	Selects the PIO used as Flex PRTCTL2 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 237: FLEX_PRTCTL_PORT3

FLEX_PRTCTL_PORT3 OFFSET: 3450h RESET = 00h			FlexConnect PRTCTL Configuration Port 3 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	This bit is used to enable Flex PRTCTL for PORT 3. The PIO is specified in the FLEX_PRTCTL_IO field. 0b = Disables Flex PRTCTL3 output 1b = Enables Flex PRTCTL3 output
6:5	PRTCTL_OUT[1:0]	R/W	Selects the Flex PRTCTL3 Output mode 00b = PRTCTL3 is tristated. 01b = PRTCTL3 is driven high. 10b = PRTCTL3 is driven low. 11b = PRTCTL3 is pulled up with internal pull-up.
4	RESERVED	R/W	Reserved
3	FLEX_PRTCTL_OEN	R/W	This bit is used to enable the Flex PRTCTL3 to output. 0b = Flex PRTCTL3 output is disabled. 1b = Flex PRTCTL3 output is enabled.
2:0	FLEX_PRTCTL_IO	R/W	Selects the PIO used as Flex PRTCTL3 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

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TABLE 238: FLEX_PRTCTL_PORT4

FLEX_PRTCTL_PORT4 OFFSET: 3451h RESET = 00h			FlexConnect PRTCTL Configuration Port 4 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	This bit is used to enable Flex PRTCTL for Port 4. The PIO is specified in the FLEX_PRTCTL_IO field. 0b = Disables Flex PRTCTL4 output 1b = Enables Flex PRTCTL4 output
6:5	PRTCTL_OUT[1:0]	R/W	Selects the Flex PRTCTL4 Output mode 00b = PRTCTL4 is tristated. 01b = PRTCTL4 is driven high. 10b = PRTCTL4 is driven low. 11b = PRTCTL4 is pulled up with internal pull-up.
4	RESERVED	R/W	Reserved
3	FLEX_PRTCTL_OEN	R/W	This bit is used to enable the Flex PRTCTL4 to output. 0b = Flex PRTCTL4 output is disabled. 1b = Flex PRTCTL4 output is enabled.
2:0	FLEX_PRTCTL_IO	R/W	Selects the PIO used as Flex PRTCTL4 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 239: FLEX_PRTCTL_PORT5

FLEX_PRTCTL_PORT5 OFFSET: 3452h RESET = 00h			FlexConnect PRTCTL Configuration Port 5 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	This bit is used to enable Flex PRTCTL for Port 5. The PIO is specified in the FLEX_PRTCTL_IO field. 0b = Disables Flex PRTCTL5 output 1b = Enables Flex PRTCTL5 output
6:5	PRTCTL_OUT[1:0]	R/W	Selects the Flex PRTCTL5 output mode 00b = PRTCTL5 is tristated. 01b = PRTCTL5 is driven high. 10b = PRTCTL5 is driven low. 11b = PRTCTL5 is pulled up with internal pull-up.
4	RESERVED	R/W	Reserved
3	FLEX_PRTCTL_OEN	R/W	This bit is used to enable the Flex PRTCTL5 to output. 0b = Flex PRTCTL5 output is disabled. 1b = Flex PRTCTL5 output is enabled.
2:0	FLEX_PRTCTL_IO	R/W	Selects the PIO used as Flex PRTCTL5 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

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TABLE 240: FLEX_PRTCTL_PORT6

FLEX_PRTCTL_PORT6 OFFSET: 3453h RESET = 00h			FlexConnect PRTCTL Configuration Port 6 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	This bit is used to enable Flex PRTCTL for PORT 6. The PIO is specified in the FLEX_PRTCTL_IO field. 0b = Disables Flex PRTCTL6 output 1b = Enables Flex PRTCTL6 output
6:5	PRTCTL_OUT[1:0]	R/W	Selects the Flex PRTCTL6 Output mode 00b = PRTCTL6 is tristated. 01b = PRTCTL6 is driven high. 10b = PRTCTL6 is driven low. 11b = PRTCTL6 is pulled up with internal pull-up.
4	RESERVED	R/W	Reserved
3	FLEX_PRTCTL_OEN	R/W	This bit is used to enable the Flex PRTCTL6 to output. 0b = Flex PRTCTL6 output is disabled. 1b = Flex PRTCTL6 output is enabled.
2:0	FLEX_PRTCTL_IO	R/W	Selects the PIO used as Flex PRTCTL6 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 241: FLEX_VBUSDET

FLEX_VBUSDET OFFSET: 3454h RESET = 00h			FlexConnect VBUSDET Configuration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_VBUSDET_EN	R/W	This bit is used to select the source for VBUS_DET while in Flex state. 0b = VBUS_DET Hub pin is the VBUS_DET in Flex state. 1b = PFx pin selected in FLEX_VBUSDET_IO is the VBUS_DET in Flex state.
6	FLEX_VBUSDET_HIGH	R/W	0b = VBUS_DET is driven as selected by FLEX_VBUSDET_EN. 1b = VBUS_DET is driven high internally.
5:3	RESERVED	R/W	Reserved

TABLE 241: FLEX_VBUSDET (CONTINUED)

FLEX_VBUSDET OFFSET: 3454h RESET = 00h			FlexConnect VBUSDET Configuration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
2:0	FLEX_VBUSDET_IO	R/W	Selects the PFx used as Flex VBUSDET 000b = PF6 001b = PF7 010b = PF14 011b = PF19 100b = PF26 101b = PF27 110b = PF28 111b = PF29

TABLE 242: FLEXCONNECT HUB ATTACH DELAY

FLEX_ATTACH_DELAY OFFSET: 3455h RESET = 00h			FlexConnect Hub Attach Delay Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	FLEX_ATTACH_DELAY	R/W	This field specifies the delay in 10-millisecond increments after Flex-Connect is initiated before the hub is attached. This might be required to provide a debounce time between a USB device detach and a sub-sequent attach.

TABLE 243: ROLE SWITCH DELAY

ROLE_SWITCH_DELAY OFFSET: 3450h RESET = 00h			Role Switch Delay Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	ROLE_SWITCH_DELAY	R/W	This field specifies the delay in 10-millisecond increments after the SET_ROLE_SWITCH command is initiated before the role switch is done. This might be required to provide a debounce time between a USB device detach and a subsequent attach.

TABLE 244: MANUFACTURER STRING LENGTH

MFG_STR_LEN OFFSET: 346Ah RESET = 14h			Manufacturer String Length Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	Length	R/W	Manufacturer String Descriptor size. This must be the same as the value in the Length field of the Manufacturer String Descriptor.

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TABLE 245: PRODUCT STRING LENGTH

PROD_STR_LEN OFFSET: 3472h RESET = 24h			Product String Length Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	Length	R/W	Product String Descriptor size. This must be same as the value in the Length field of the Product String Descriptor.

TABLE 246: USB3 HUB BCDUSB LSB

USB3_HUB_BCDUSB_LSB OFFSET: E542h RESET = 02h			USB3 Hub bcdUSB LSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_BCDUS-B_LSB	R/W	Least Significant Byte of the HFC Product ID. This is a 16-bit value that identifies the USB-IF specification revision that the product adheres to.

TABLE 247: USB3 HUB BCDUSB MSB

USB3_HUB_BCDUSB_MSB OFFSET: E543h RESET = 03h			USB3 Hub bcdUSB MSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_BCDUS-B_MSB	R/W	Most Significant Byte of the USB3Hub BcdUSB descriptor. This is a 16-bit value that identifies the USB-IF specification revision that the product adheres to.

TABLE 248: USB3 HUB VENDOR ID LSB

USB3_HUB_VID_LSB OFFSET: E548h RESET = 24h			USB3 Hub Vendor ID LSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_-DID_MSB	R/W	Least Significant Byte of the HFC Product ID. This is a 16-bit value that identifies the vendor of the product (as registers with USB-IF). The Microchip Vendor ID is 0424h.

TABLE 249: USB3 HUB VENDOR ID MSB

USB3_HUB_VID_MSB OFFSET: E549h RESET = 04h			USB3 Hub Vendor ID MSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_-DID_MSB	R/W	Least Significant Byte of the HFC Product ID. This is a 16-bit value that identifies the vendor of the product (as registers with USB-IF). The Microchip Vendor ID is 0424h.

TABLE 250: USB3 HUB PRODUCT ID MSB

USB3_HUB_PID_MSB OFFSET: E54Ah RESET = XXh			USB3 Hub Product ID MSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_PID_MSB	R/W	Most Significant Byte of the USB3 Hub Product ID. This is a 16-bit value that uniquely identifies this USB3 Hub device. The default value is dependent on the part as shown below: USB7202 = 02h USB7206 = 06h USB7250 = 50h USB7251 = 51h USB7216 = 16h USB7252 = 52h USB7216/USB7256 = 56h

Note 1: If port disable straps are implemented, these values will automatically decrement by the number of ports disabled by strapping. For example, if a design that implements USB7216/USB7256 with two ports disabled by strapping, the Product ID (PID) will automatically change to 0x7254.

TABLE 251: USB3 HUB PRODUCT ID LSB

USB3_HUB_PID_LSB OFFSET: E54Bh RESET = 72h			USB3 Hub Product ID LSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_PID_LSB	R/W	Least Significant Byte of the USB3 Hub Product ID. This is a 16-bit value that uniquely identifies this USB3 Hub device. All devices: 72h

TABLE 252: USB3 HUB DEVICE ID (BCDDEVICE) LSB

USB3_HUB_PID_MSB OFFSET: E54Ch RESET = XXh			USB3 Hub Device ID LSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_-DID_LSB	R/W	Least Significant Byte of the USB3 Hub Device ID. This is a 16-bit value used for firmware or device revision tracking purposes.

Note 1: The default Device ID may change with silicon or firmware revisions.

TABLE 253: USB3 HUB DEVICE ID (BCDDEVICE) MSB

USB3_HUB_PID_MSB OFFSET: E54Dh RESET = XXh			USB3 Hub Device ID MSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_-DID_MSB	R/W	Most Significant Byte of the USB3 Hub Device ID. This is a 16-bit value used for firmware or device revision tracking purposes.

Note 1: The default Device ID may change with silicon or firmware revisions.

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TABLE 254: USB3 HUB MANUFACTURER STRING INDEX REGISTER

USB3_HUB_MFR_STR_INDEX OFFSET: E54Eh RESET = 01h			USB3 Hub Manufacturer String Index Register Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_MFR_STR_INDEX	R/W	Manufacturer String Index Set = '00b' if unused

TABLE 255: USB3 HUB PRODUCT STRING INDEX REGISTER

USB3_HUB_PRD_STR_INDEX OFFSET: E54Fh RESET = 02h			USB3 Hub Product String Index Register Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_PRD_STR_INDEX	R/W	Product String Index Set = '00b' if unused

TABLE 256: USB3 HUB SERIAL STRING INDEX REGISTER

USB3_HUB_SER_STR_INDEX OFFSET: E550h RESET = 00h			USB3 Hub Serial String Index Register Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_SER_STR_INDEX	R/W	Serial String Index Set = '00b' if unused

TABLE 257: USB3 HUB LANG_ID[15:0] LANGUAGE IDENTIFIER

USB3_HUB_LANG_ID OFFSET: E5DAh RESET = 0409h			USB3 Hub USB-IF Language Identifier Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
15:0	USB3_HUB_LANG_ID	R/W	USB-IF Language Identifier. Default is English (United States).

Note 1: 28FAh-[7:0], 28FBh-[15:8]

TABLE 258: USB3 HUB STRING DESCRIPTOR CONTAINER

USB3_HUB_STR_CONTAINER OFFSET: E5E0h			USB3 Hub String Container Base Address: BFD2_0000h
Byte	**Name**	**R/W**	**Description**
95:0	USB3_HUB_STRINGS	R/W	Container for All HFC Strings. This must follow the formatting as described in the *USB2.0 Specification* for string descriptors. All Hub Feature Controller product, manufacturer, and serial string are contained within this register array.

Note 1: 80E0h-[7:0], 80E1h-[15:8], 80E2h-[23:16], 80E3h-[31:24], 80E4h-[39:32],... 819Fh-[95:88]

TABLE 259: USB3 HUB ATTRIBUTES DESCRIPTOR

USB3_HUB_ATTRIBUTES OFFSET: E55Fh RESET = E0h			USB3 Hub Attributes Descriptor Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	Reserved	R	Reserved, always set to '1b'
6	SELF_POWERED	R/W	0b = Hub is not self-powered. (Hub is powered from upstream port VBUS.) 1b = Hub is self-powered. (Hub has its own power source.)
5	REMOTE_WAKEUP	R/W	0b = Hub is not remote wakeup capable. 1b = Hub is remote wakeup capable.
4:0	Reserved	R	Reserved, always set to '0b'.

TABLE 260: USB3 HUB MAX POWER DESCRIPTOR

USB3_HUB_MAX_POWER OFFSET: E560h RESET = 00h			USB3 Hub Max Power Descriptor Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_MAX-_POWER	R/W	Maximum power consumption of the hub from VBUS when fully operational 2 mA intervals. The default setting for this value is 2 mA (indicating almost no power consumption from VBUS) as most USB3 hub applications are not bus-powered applications.

TABLE 261: USB3 HUB NUMBER OF PORTS DESCRIPTOR

USB3_HUB_NBR_PORTS OFFSET: E5CAh RESET = Depends on device and port disable strap settings			USB3 Hub Number of Ports Descriptor Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_N-BR_PORTS	R/W	The number of downstream ports on the USB3 side of the hub (does not include any USB2-only ports). The default value depends on the hub device. 00h = Invalid 01h = 1 USB3 downstream port 02h = 2 USB3 downstream ports 03h = 3 USB3 downstream ports 04h = 4 USB3 downstream ports 05h = 5 USB3 downstream ports 06h = FFh = Invalid

TABLE 262: USB3 HUB CHARACTERISTICS DESCRIPTOR

USB3_HUB_CHARACTERISTICS OFFSET: E5CBh RESET = 09h			USB3 Hub Characteristics Descriptor Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved

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TABLE 262: USB3 HUB CHARACTERISTICS DESCRIPTOR (CONTINUED)

USB3_HUB_CHARACTERISTICS OFFSET: E5CBh RESET = 09h			USB3 Hub Characteristics Descriptor Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
4:3	OVER_CURRENT_-MODE	R/W	00 = Global overcurrent protection. The hub reports overcurrent as a summation of all ports' current draw, without a breakdown of individual port over-current status. 01b = Individual port overcurrent protection. The hub reports overcurrent on a per-port basis. Each port has an overcurrent status. 1Xb = No overcurrent protection. This option is allowed only for bus-powered hubs that do not implement overcurrent protection.
2	COMPOUND_DE-VICE	R/W	0b = Hub is not part of a compound device. 1b = Hub is part of a compound device. A USB3 device is permanently attached to one or more of the USB3 ports.
1:0	LOGICAL_POWER_-MODE	R/W	00 = Ganged power switching. All ports power at once from a single control signal. 01b = Individual port power switching. Each port has an individual power switch with individual control signal. 1Xb = Reserved

TABLE 263: USB3 HUB POWER-TO-POWER GOOD DESCRIPTOR

USB3_HUB_PWR2PWRGOOD OFFSET: E5CDh RESET = 30h			USB3 Hub Power to Power Good Descriptor Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_P-WR2PWRGOOD	R/W	Time in 2 ms intervals from the time the power-on sequence begins on a port until power is good on that port. The USB system software uses this value to determine how long to wait before accessing a powered-on port. This value should be set to zero if power-switching is not supported in the system design.

Note 1: A 'zero' setting should never be used on a design which includes Type-C ports.

TABLE 264: USB3 HUB NON-REMOVABLE PARTS DESCRIPTOR

USB3_HUB_NON_REM OFFSET: E5D2h RESET = Depends on CFG_NON_REM hardware strap settings			**USB3 Hub Non Removable Ports Descriptor Base Address: BFD2_0000h**
Bit	**Name**	**R/W**	**Description**
7:0	USB3_HUB_NON_REM	R/W	A descriptor which communicates the non-removable settings for the logical port numbering. 0b = Device is removable 1b = Device is non-removable Bit 0 = Reserved Bit 1 = Port 1 Bit 2 = Port 2 Bit 3 = Port 3 Bit 4 = Port 4 Bit 5 = Port 5 Bit 6 = Reserved Bit 7 = Reserved

Note 1: Certain port settings are made with respect to logical port numbering, and other port settings are made with respect to physical port numbering. Logical port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. Physical port number is the port number with respect to the physical PHY on the chip. Physical port numbering is fixed, and the settings are not impacted by logical port renumbering or remapping.

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3.0 SMBUS CONFIGURATION

The SMBus configuration begins in the SOC Configuration Stage. In this stage, the SOC may modify any of the configuration settings to customize the hub to their purposes. The SOC can configure the hub as Full-Speed only or can have the hub report a port as non-removable. The SOC can also disable a port entirely to conserve power. The hub can be addressed at the address ***2Dh*** and interprets the data bytes as shown in the following subsections.

3.1 SMBus Block Write

The SMBus block write consists of an Address+Direction(0) byte followed by the 16-bit memory address, split into two bytes. The address is used for special commands and as a pointer to the hub's internal memory. Following the address, the next byte of data corresponds to the count of data bytes that follows, which is up to 128 bytes in a block. Finally, a 00h write is used to terminate the write operation, followed by the SMBus stop signal. See Table 265.

TABLE 265: SMBUS BLOCK WRITE

Field	Description
Start bit (S)	Start condition
I^2C Address	7-bit SMBus Address (2Dh)
Direction	1-bit, 0 = Write
ACK	Acknowledge from SMBus client
Offset MSB	Most significant byte of address to internal buffer (00h)
ACK	Acknowledge from SMBus client
Offset LSB	Least significant byte of address to internal buffer (00h)
ACK	Acknowledge from SMBus client
Count	Start Condition
ACK	Acknowledge from SMBus client
Data 0	First byte of data
ACK	Acknowledge from SMBus client
Data 1	Second byte of data
ACK	Acknowledge from SMBus client
Data n	Last byte of data
ACK	Acknowledge from SMBus client
Stop (P)	Stop condition

Note: The 7-bit address of the hub is ***2Dh***, or the first byte is ***5Ah*** for an SMBus Write.

3.2 SMBus Block Read

The SMBus block read consists of an Address+Direction(0) byte with the 16-bit memory address, followed by a repeat Start signal and an Address+Direction(1) byte. The hub then starts to output the count (128 bytes) and the contents of the internal registers starting at the 16-bit address specified. See Table 266.

TABLE 266: SMBUS BLOCK READ

Field	Description
Start bit (S)	Start condition
I^2C Address	7-bit SMBus Address (2Dh)
Direction	1-bit, 0 = Write
ACK	Acknowledge from SMBus client
Offset MSB	Most Significant Byte of address to internal buffer (00h)
ACK	Acknowledge from SMBus client
Offset LSB	Least Significant Byte of address to internal buffer (00h)
ACK	Acknowledge from SMBus client
Start bit (Sr)	Repeated Start condition
I^2C Address	7-bit SMBus Address (2Dh)
Direction	1-bit, 1 = Read
ACK	Acknowledge from SMBus client
Count	Number of bytes to read from client
ACK	Acknowledge from SMBus host
Data 0	First byte of data from SMBus client
ACK	Acknowledge from SMBus host
Data 1	Second byte of data from SMBus client
ACK	Acknowledge from SMBus host
Data n	Last data byte from SMBus client
ACK	Acknowledge from SMBus host
Stop (P)	Stop condition

Note: The 7-bit address of the hub is ***2Dh***, or the first byte is ***5Ah*** for a write and ***5Bh*** for a read.

3.3 Special Commands

Special commands can be sent in the place of the 16-bit address bytes. These commands are used to enumerate the hub, access the Configuration registers, or reset the device. The commands consist of the 16-bit command followed by a 00h byte to terminate the command. See Table 267.

TABLE 267: SPECIAL SMBUS COMMANDS

Operation	OPCODE	Description
Configuration Register Access	9937h	Read and Write Configuration registers
USB Attach	AA55h	Exit SOC_CONFIG and Enter HUB_CONFIG stage
USB Attach with SMBus Runtime Access	AA56h	Exit SOC_CONFIG and Enter HUB_CONFIG stage with SMBus client enabled
OTP Program	9933h	Permanently program configuration commands to the OTP
OTP Read	9934h	Read the values of the OTP register

Note: OTP Program and OTP Read commands reference data starting at Configuration Register 4800h.

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3.4 Accessing Configuration Registers

The Configuration Register Access command allows the SMBus host to read or write to the internal registers of the hub. When the Configuration Register Access command is sent, the hub interprets the memory starting at offset 0000h as in Table 268.

TABLE 268: MEMORY FORMAT FOR CONFIGURATION REGISTER ACCESS

Buffer Address	Description	Notes
0000h	Direction	0 = Register Write, 1 = Register Read
0001h	Data Length	Number of bytes to read/write, maximum of 128 bytes
0002h-0005h	Memory Address	32-bit memory address to read or write in big-endian format
0006h~ 0084h	Data	Data to write or read from the Memory Address, number of bytes specified in the Data Length field

3.4.1 CONFIGURATION REGISTER WRITE EXAMPLE

To write to a Configuration register:

1. Write the command block to the buffer area.
2. Execute the special Configuration Register Access command.

EXAMPLE 3-1: FORMATTING SMBUS MESSAGES TO SET HUB VID TO CUSTOM VALUE

The following example shows how the SMBus messages are formatted to set the VID of the hub to a custom value, 1234h:

1. Write the command block to the buffer area (See Table 269.):

TABLE 269: SMBUS WRITE COMMAND BLOCK FOR REGISTER WRITE

Byte	Value	Comment
0	5Ah	Client address plus write bit (2Dh left shifted by 1)
1	00h	Buffer address MSB **00**00h
2	00h	Buffer address LSB 00**00**h
3	08h	Number of bytes to write to command block buffer area
4	00h	Write VID Register
5	02h	Writing two bytes to VID register
6	BFh	VID is in register **BF**80_3000h.
7	80h	VID is in register BF**80**_3000h.
8	30h	VID is in register BF80_**30**00h.
8	00h	VID is in register BF80_30**00**h.
A	34h	LSB of Vendor ID 12**34**h
B	12h	MSB of Vendor ID **12**34h

2. Execute the Configuration Register Access command (See Table 270.):

TABLE 270: CONFIGURATION REGISTER ACCESS COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit
1	99h	Command **99**37h
2	37h	Command 99**37**h
3	00h	Command completion

3.4.2 CONFIGURATION REGISTER READ EXAMPLE

To read Configuration registers:

1. Write the command block to the buffer area.
2. Execute the Configuration Register Access command.
3. Read the data from the memory.

EXAMPLE 3-2: READING THE PID

The example below shows how to read the PID.

1. Write the data to the memory of the hub (See Table 271.):

TABLE 271: SMBUS WRITE COMMAND BLOCK FOR REGISTER READ

Byte	Value	Comment
0	5Ah	Client address plus write bit (2Dh left shifted by 1)
1	00h	Memory address **00**00h
2	00h	Memory address 00**00**h
3	06h	Number of bytes to write to memory
4	01h	Read Configuration register
5	02h	Reading two bytes from PID register
6	BFh	VID is in register **BF**80_3002h.
7	80h	VID is in register BF**80**_3002h.
8	30h	VID is in register BF80_**30**02h.
9	02h	VID is in register BF80_30**02**h.

2. Execute the Configuration Register Access command (See Table 272.):

TABLE 272: CONFIGURATION REGISTER ACCESS COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit (2Dh left shifted by 1)
1	99h	Command **99**37h
2	37h	Command 99**37**h
3	00h	Command completion

3. Read back data starting at memory offset 04h, which is where the Data byte starts (See Table 273.):

TABLE 273: EXAMPLE SMBUS READ COMMAND

Byte	Value	Comments
0	5Ah	Client address plus write bit (2Dh left shifted by 1)
1	00h	Memory Address **00**06h
2	06h	Memory Address 00**06**h
3	5Bh	Client address plus read bit (2Dh left shifted by 1 + 1)
4	08h	Device sends a count of 8 bytes
5	16h	PID LSB
6	49h	PID MSB

Note 1: Although the device can send out 8 bytes, it is not necessary to read the 8 bytes. The SMBus host can send a stop at any time.

3.5 SMBus Runtime

After the hub is enumerated (after USB Attach with SMBus Runtime Access), the same registers can be accessed during runtime.

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4.0 OTP CONFIGURATION

The USB7202/USB7206/USB7216/USB725x hubs have 8k bytes of One-Time Programmable (OTP) memory to enable customization and limited firmware updates in the field. The OTP memory organization and OTP configuration are described in the next sections.

4.1 OTP Memory Organization

The OTP memory is divided into four regions as follows:

- OTP Flags
- Configuration Commands
- Blank Memory
- Configuration Index Records

Figure 2 shows the OTP memory organization example. Each product have unique default contents.

FIGURE 2: OTP MEMORY ORGANIZATION

	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
0000h	**OTP Flags**															
0010h						**Configuration Commands**										
0020h																
0030h								00h	00h	00h	00h	00h	00h	00h	00h	00h
0040h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
0050h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
	00h	00h	00h	00h	00h	**Blank Memory**							00h	00h	00h	00h
...	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FC0h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FD0h	00h	00h	00h	00h	00h	00h	00h									
1FE0h						**Configuration Index Records**										
1FF0h																

4.1.1 OTP FLAGS

The first 2 to 4 bytes of the OTP memory are the OTP Flags, indicating how many times the OTP has been programmed by the MPLAB® Connect Configurator tool. (When programming via SMBus, these bits are not updated.) For an unprogrammed part, these two bytes are 0000h. Every time the OTP is programmed using MPLAB Connect Configurator, a bit is set. When the first OTP is programmed, this becomes 0001h, then 0003h, 0007h, and continues until all bits are set. After all OTP Flag bits are set, OTP programming is still possible as long as the OTP space is available.

4.1.2 CONFIGURATION COMMANDS

The configuration commands section grows from the start of the OTP data. These are the commands that are appended every time a Program OTP command is sent through SMBus and can vary in length depending on how many Configuration registers have been manipulated.

4.1.3 BLANK MEMORY

This memory region is initially 00h on an unprogrammed part and decreases in size as configuration commands and configuration index records are programmed.

4.1.4 CONFIGURATION INDEX RECORDS

The Configuration Index Records area contains Configuration Index Records that are automatically generated when the OTP data is programmed. A Configuration Index Record is always 8 bytes per OTP program and is appended to the back of the OTP memory space every time the Program OTP command is sent. It contains a checksum to confirm that the configuration command was written correctly and the information on the location of the configuration commands is within the OTP memory space and total length. The Configuration Index Record format is shown in Figure 3.

The CheckSum algorithm for the CheckSum byte is Checksum8-Xor.

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FIGURE 3: CONFIGURATION INDEX RECORD FORMAT

BYTE	1	2	3	4	5	6	7	8
Description	Signature			Checksum	CFG ADDRESS		CFG LENGTH	
Contents	I (49h)	D (44h)	X (58h)	Checksum	MSB	LSB	MSB	LSB

4.2 OTP Configuration Using MPLAB® Connect Configurator

The easiest method to program the USB7202/USB7206/USB7216/USB725x Hub OTP is with the MPLAB Connect Configurator tool, available at http://www.microchip.com/design-centers/usb/mplab-connect-configurator.

MPLAB Connect Configurator programs the configuration in the next available slot in the configuration commands area, programs the Index Record in the Configuration Index Records area, and updates the OTP Flags count field.

This tool can be used to generate a configuration file (.cfg) and to program the generated configuration file permanently to the hub's OTP memory space using USB commands.

Alternatively, the `.cfg` file can be constructed manually using a binary/hex editor. Follow the formatting instructions shown in Table 274, and refer to the example in Section 4.3.1, "OTP Configuration File Examples".

4.3 OTP Configuration Using SMBus

The OTP memory can be programmed through the SMBus interface in the SOC_CONFIG stage (during start-up). The OTP memory is configured as a series of commands that manipulates the Configuration registers. The USB7202/USB7206/USB7216/USB725x hubs have a total of 8 kB of OTP memory space, and each byte of OTP memory may be written only once. The OTP memory space can be successively written to (each programming instance appends the new command to the bottom of the OTP memory space) until the space is completely filled.

During the HUB_CONFIG stage, temporary OTP Configuration registers are written to. The contents in the OTP Configuration registers are then permanently loaded to the OTP memory space after sending a special OTP program command. These registers permanently change the default behavior of the hub during normal operation. These commands are stored into the OTP memory as shown in Figure 2.

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TABLE 274: OTP STORAGE COMMANDS

Command	OPCODE	Length	Description
NULL	00h	N/A	No action; advance memory counter by 1 and move to the next instruction.
MODIFY_BYTES	01h-7Fh	OPCODE	Modifies the following bytes starting at the current memory address for length = OPCODE. The previously used SET_MODE command is used for selecting the bit operation. The default mode is WRITE_BYTES if there is no preceding SET_MODE command.
SET_MEMORY ADDRESS	80h XXh XXh XXh XXh	N/A	Load the MEMORY_ADDRESS register with the four XXh XXh XXh XXh bytes. Example: 80h BFh 80h 30h 00h sets the memory address to BF80_3000h.
SKIP_MEMORY_WRITE	81h-FDh	OPCODE [6:0]	Skip the length number of bytes starting at the location of the MEMORY_ADDRESS register. At the end of the operation, the MEMORY_ADDRESS register is incremented by length = OPCODE[6:0].
SET_MODE_WRITE_BYTE	FEh 00h	N/A	If the byte following SET_MODE = 00h, all writes replace the memory value at that location.
SET_MODE_SET_BITS	FEh 01h	N/A	If the byte following SET_MODE = 01h, all writes are OR'ed in. This is a mechanism used to set the selected bits in a register without changing the others. Set the bits to be set.
SET_MODE_CLEAR_BITS	FEh 02h	N/A	If the byte following SET_MODE = 02h, all writes are NAND'ed in. This is a mechanism used to clear the selected bits in a register without changing the others. Set the bits to be cleared.
STOP	FFh	N/A	The completion of the storage commands indicates the termination of the command sequence.

4.3.1 OTP CONFIGURATION FILE EXAMPLES

Example 4-1 and Example 4-2 show the hex data in a configuration file.

EXAMPLE 4-1: CONFIGURING PF28 AS AN OUTPUT GPIO

To configure PF28 as an output assuming that PF28 is already configured as a GPIO (as it is in USB7202, all CFG_STRAP options), the corresponding bit in the output enable register that must be set is GPIO92. Refer to Table 3.

TABLE 275: SET BIT COMMAND SEQUENCE EXAMPLE

Byte	Value	Comment
1	80h	SET_ADDRESS command
2	BFh	Address **BF**80_090Bh
3	80h	Address BF**80**_090Bh
4	09h	Address BF80**_09**0Bh
5	0B	Address BF80_09**0B**h
6	FEh	SET_MODE command
7	01h	SET_BITS mode
8	01h	Data length of 1 byte
9	04h	Set PIO96_OEN[Bit 28]
10	FFh	Stop command

EXAMPLE 4-2: CHANGING THE USB DOWNSTREAM PORT 1 BOOST REGISTER TO INCREASE THE HS OUTPUT CURRENT BY 5%

TABLE 276: WRITE BYTE COMMAND SEQUENCE EXAMPLE

Byte	Value	Comment
1	80h	SET_ADDRESS command
2	BFh	Address **BF**80_64CAh
3	80h	Address BF**80**_64CAh
4	64h	Address BF80**_64**CAh
5	CAh	Address BF80_64**CA**h
6	FEh	SET_MODE command
7	01h	WRITE_BYTE mode
8	01h	Data length of 1 byte
9	03h	Increase HS output current by 5%
10	FFh	Stop command

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4.3.2 OTP CONFIGURATION VIA SMBUS

The commands in Table 277 can be used to access and program the OTP memory. These can be used by an automated test equipment (ATE) equipment.

TABLE 277: SPECIAL OTP SMBUS COMMANDS

Operation	OPCODE	Description
SMB_CMD_OTP	9933h	Execute OTP Command based on CMD_TYPE
SMB_CMD_READ_OTP	9934h	Read OTP register
SMB_CMD_OTP_ATE	9939h	Execute OTP Command based on CMD_TYPE. This command is for use with ATE. Command success or failure is reported via signal pins. The device does not respond afterwards until Reset. • Command status pin: PRT_PWR1 (0 = Passed, 1 = OTP Failed) • Command completion pin: PRT_PWR2 (0 = In progress, 1 = done)

Note 1: Before any OTP commands can be executed, a data structure must be created in the memory using SMBus block writes.

4.3.3 SMBUS OTP COMMAND STRUCTURE

The OTP command structure in Table 278 is used for accessing the OTP memory.

TABLE 278: SMBUS OTP COMMAND STRUCTURE

Buffer Address	Description	Notes
BFD2_2100h	CMD_TYPE	Command Type is one of the commands in the **OTP Command Type** table.
BFD2_2101h	ADDR[15:0]	OTP Address to read from or write to; set to 0000h.
BFD2_2103h	LENGTH[15:0]	Number of bytes to transfer
BF90_7000h	Data	Data for OTP transaction. **MULTI_HOST_CLK_EN** and **MHB_MEM_CLK_EN** bits must be set before accessing the DATA_BUFFER.
BFD2_3419h	SMBusOTPResult	Result of OTP operation as specified in the **OTP Return Status**

TABLE 279: OTP COMMAND TYPE

Code	CMD_TYPE	Description
00h	SMB_OTP_RAW_PGM	Raw OTP Programming mode *ADVANCED* OTP will be programmed starting at the OTP memory offset of ADDR for size LENGTH. The OTP memory at any location with the OTP can be programmed. No signature is generated. It is possible to corrupt existing configuration using this mode. A new OTP configuration block programmed using this mode will also need a valid signature to be manually added to the correct signature memory location. Status on completion: • 00h = OTP was programmed and verified successfully. • 01h = OTP programming failed.

TABLE 279: OTP COMMAND TYPE (CONTINUED)

Code	CMD_TYPE	Description
03h	SMB_OTP_PGM	"Smart" OTP Programming mode This programs the OTP configuration block automatically after the last programmed OTP record. The hub will automatically generate and program the signature at the end of the OTP memory space in the next available memory space including the IDX signature, record checksum, start offset, and length. The LENGTH and DATA buffer must be initialized before issuing this command. Status on completion: • 00h = OTP was programmed and verified successfully. • 01h = OTP programming failed.
05h	SMB_OTP_BLANKCHECK	This verifies that the OTP is blank and has not been programmed. Status on completion: • 00h = PASS; OTP is blank and has not been programmed. • 01h = FAIL; OTP blank check failed.
06h	SMB_OTP_RESET	This resets the OTP core. Status on completion: • 00h = OTP_NO_ERROR
07h	SMB_OTP_READ	This command reads the number of bytes specified in the LENGTH field and stores them in data buffer. Status on completion: • 00h = OTP data was read successfully. • 01h = OTP read failed.

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4.3.4 STEPS FOR PROGRAMMING OTP USING SMBUS

1. Write the OTP memory structure.
2. Send the Execute OTP command.
3. Read SMBus OTP Result.

EXAMPLE 4-3: SMBUS OTP "SMART" PROGRAMMING

The "Smart" OTP programming method allows users to program an OTP configuration block without the calculation of OTP memory offset and manual generation or programming of configuration index signature. In "Smart" OTP Programming mode, the hub automatically places the Configuration data into the next available memory space and generates/programs the correct Configuration Index signature.

This example changes the PID LSB at BF803002h to 34h and the PID MSB at BF803003h to 12h.

The OTP configuration data for this is `80 BF 80 30 02 02 34 12 FF`. Refer to Table 280.

TABLE 280: STEPS FOR SMBUS OTP "SMART" PROGRAMMING

Writing the OTP Memory Structure
1. Write 86, C7, 01, E0 to BF80_0B00h: `00 00 0A 00 04 BF 80 0B 00 86 C8 00 E0` 2. Write SMBus Configuration Register Access command: `5A 99 37 00`
3. Resume HFC Operation: `00 00 07 00 01 BF 80 2C 02 C2` 4. Write SMBus Configuration Register Access command: `5A 99 37 00` 5. Write OTP Patch to Data Area at BF90_7000h: `5A 00 00 0F 00 09 BF 90 70 00 80 BF 80 30 02 02 34 12 FF` 6. Write SMBus Configuration Register Access command: `5A 99 37 00` 7. Write OTP "03" to BFD2_2100 to indicate "Smart OTP" programming to program to next available OTP space: `00 00 07 00 01 BF D2 21 00 03` 8. Write SMBus Configuration Register Access command: `5A 99 37 00` 9. Write OTP patch length (09h) to BFD2_2103h: `00 00 08 00 02 BF D2 21 03 00 09` 10. Write SMBus Configuration Register Access command: `5A 99 37 00`
Sending the Execute OTP Command
11. Write to SMBus: `5A 99 33 00`
Reading the SMBus OTP Result Register
12. Set the command block for status read at BFD2_3419h: `5A 00 00 06 01 01 BF D2 34 19` 13. Write SMBus Configuration Register Access command: `5A 99 37 00` 14. Read Data (**Note 1**): `5A 00 06 5B 08 XX`

Note 1: `XX` is the status returned: 00 = Pass.

EXAMPLE 4-4: SMBUS OTP "RAW" PROGRAMMING (ADVANCED)

The Raw OTP Programming method allows any byte or block of bytes to be programmed within the hub OTP memory. Generally, when programming typical configuration memory blocks, the standard OTP programming method should be used.

The Raw OTP Programing feature can be used to intentionally corrupt a previously programmed configuration block's CheckSum byte in the Configuration Index signature. Doing this prevents the configuration block from being loaded. This technique can be used to recover a hub that was rendered non-functional by an incorrectly formatted configuration data block.

For example, if the CheckSum byte of the configuration block that needs to be prevented from being loaded is located at memory offset 1FEBh (meaning, it was the third configuration block to be programmed into the hub's OTP memory), then the commands in Table 281 can be followed to overwrite that byte with an FFh to intentionally corrupt that byte.

TABLE 281: STEPS FOR SMBUS OTP "RAW" PROGRAMMING

Writing the OTP Memory Structure
1. Write 86, C7, 01, E0 to BF80_0B00h: `00 00 0A 00 04 BF 80 0B 00 86 C8 00 E0`
2. Write SMBus Configuration Register Access command: `5A 99 37 00`
3. Resume HFC Operation: `00 00 07 00 01 BF 80 2C 02 C2`
4. Write SMBus Configuration Register Access command: `5A 99 37 00`
5. Write OTP Patch to Data Area at BF90_7000h: `5A 00 00 07 00 01 BF 90 70 00 FF`
6. Write SMBus Configuration Register Access command: `5A 99 37 00`
7. Write OTP "00" to BFD2_2100 to indicate "Smart OTP" programming to program to next available OTP space: `00 00 07 00 01 BF D2 21 00 00`
8. Write SMBus Configuration Register Access command: `5A 99 37 00`
9. Write OTP patch memory offset (1FEBh) to BFD2_2101h to overwrite the data payload (FFh) to the third Configuration Index signature location: `00 00 08 00 02 BF D2 21 01 1F FE`
10. Write SMBus Configuration Register Access command: `5A 99 37 00`
11. Write OTP patch length (01h) to BFD2_2103h: `00 00 08 00 02 BF D2 21 03 00 01`
12. Write SMBus Configuration Register Access command: `5A 99 37 00`
Sending the Execute OTP Command
13. Write to SMBus: `5A 99 33 00`
Reading the SMBus OTP Result Register
14. Set the command block for status read at BFD2_3419h: `5A 00 00 06 01 01 BF D2 34 19`
15. Write SMBus Configuration Register Access command: `5A 99 37 00`
16. Read data: `5A 00 06 5B 08 XX`

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EXAMPLE 4-5: SMBUS OTP READ

The OTP memory of the hub can be read via SMBus in its entirety or in selected chunks.

The example in Table 282 shows how to read back the entire OTP memory.

.

TABLE 282: STEPS FOR SMBUS OTP READ

General Setup
1. Set up CLK_CTL_REG BF80_0B00h: `5A 00 00 0A 00 04 BF 80 0B 00 86 C8 00 E0` 2. Write SMBus Configuration Register Access command: `5A 99 37 00`
3. Start-up HFC Execution, Length at BF80_2CC2h: `5A 00 00 07 00 01 BF 80 2C 02 C2` 4. Write SMBus Configuration Register Access command: `5A 99 37 00`
Configuring for Read-back of first 4 kB of OTP Memory Space
5. Configure to take the first 4 kB of OTP memory and dump to BF90_7000h space: `5A 00 00 0B 00 05 BF D2 21 00 07 00 00 10 00` 6. Write SMBus Configuration Register Access command: `5A 99 37 00`
Sending the Execute OTP Command
7. Write to SMBus: `5A 99 33 00`
Reading the SMBus OTP Result Register
8. Set the command block for status read at BFD2_3419h: `5A 00 00 06 01 08 BF D2 34 19` 9. Write SMBus Configuration Register Access command: `5A 99 37 00` 10. Read data: `5A 00 06 5B 06 XX` **Note:** `XX` is the status returned: 00 = Pass.
Reading back the first 4 kB of OTP Memory
11. Set the command block for read-back of first 128 kB chunk of OTP starting from BF90_7000h: `5A 00 00 06 01 80 BF 90 70 00` 12. Write SMBus Configuration Register Access command: `5A 99 37 00` 13. Read data: `5A 00 06 5B 06` XX_0 – XX_{127} **Note:** XX_0 – XX_{127} is returned 128 kB of OTP memory 14. Set the command block for read-back next 128 kB chunk of OTP starting from BF90_7080h: `5A 00 00 06 01 80 BF 90 70 80` 15. Write SMBus Configuration Register Access command: `5A 99 37 00` 16. Read data: `5A 00 06 5B 06` XX_{128} – XX_{255} XX_{128} – XX_{255} is returned 128 kB of OTP memory 17. Set the command block for read-back next 128 kB chunk of OTP starting from BF90_7100h: `5A 00 00 06 01 80 BF 90 71 00` 18. Write SMBus Configuration Register Access command: `5A 99 37 00` 19. Read data: `5A 00 06 5B 06` XX_{256} – XX_{383} XX_{256} – XX_{383} is returned 128 kB of OTP memory 20. Continue until the first 4 kB of OTP memory is retrieved.
Configuring for Read-back of the second 4 kB of OTP Memory Space
21. Configure to take the second 4 kB of OTP memory and dump to BF90_7000h space: `5A 00 00 0B 00 05 BF D2 21 00 07 10 00 10 00` 22. Write SMBus Configuration Register Access command: `5A 99 37 00`
Sending the Execute OTP Command
23. Write to SMBus: `5A 99 33 00`

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TABLE 282: STEPS FOR SMBUS OTP READ (CONTINUED)

Reading back the second 4 kB of OTP Memory Space
24. Set the command block for read-back next 128 kB chunk of OTP starting from BF90_7100h: `5A 00 00 06 01 80 BF 90 70 00` 25. Write SMBus Configuration Register Access command: `5A 99 37 00` 26. Read data: `5A 00 06 5B 06` $XX_{4,096}$ – $XX_{4,223}$ $XX_{4,096}$ – $XX_{4,223}$ is returned 128 kB of OTP memory 27. Continue until the second 4 kB of OTP memory is retrieved.

4.4 OTP Configuration via USB

The following are the steps to configure OTP via USB:

1. Read OTP Setup Transaction
2. Set OTP Program Code
3. Program OTP Transaction to Program OTP Configuration Data to OTP
4. Get Status OTP Transaction

4.4.1 READ OTP SETUP TRANSACTION

To program OTP via USB, the entire OTP memory contents must be read to obtain the correct memory offset location for the OTP configuration block and the signature. Refer to the Section 4.1, "OTP Memory Organization" for the OTP memory organization.

The new configuration block should be programmed to the next byte following the end of the most recently programmed configuration block (configuration command blocks work forward from the beginning of the OTP memory space). The new Configuration Index signature should begin 8 bytes before the start of the most recently programmed Configuration Index signature. (Signatures are added backwards from the end of the memory space.)

Note: Two to four bytes at the very beginning of the OTP memory are left intentionally blank at the time of production. The MPLAB Connect Configurator tool uses these bytes to keep track of the number of times the tool has been used to update the OTP memory. When programming OTP via USB manually, these bits may be optionally used to keep track of the number of additional times the hub OTP memory has been programmed. The hub FW does not actually use these bytes for any purpose.

Issue the command in Table 283 to read the OTP memory.

TABLE 283: OTP READ SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0xC1	Device-to-host to data transfer, using vendor-specific command, targeting interface
bRequest	0x01	CMD_OTP_READ
wValue	OTP_ADRESS	Address of the OTP ROM to be read
wIndex	0x00	Reserved
wLength	Data Length	Length of data to be read

Note 1: **Command phase:** Receives the SETUP packet with the parameters specified above
Data phase: Sends the data bytes of length wLength from address wValue
Status phase:
•STALL – on read error
•ACK – on successful completion of command

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4.4.2 SET OTP PROGRAM CODE

The OTP memory can be programmed by either the PROGRAM command or the PROGRAMVERIFY command. CMD_OTP_SET_PROGRAM_MODE selects the internal command that the ROM will issue to the OTP during subsequent CMD_OTP_PROGRAM commands. (See Table 284 and Table 285.)

The default mode in the ROM is PROGRAMVERIFY (without requiring the Set OTP Program Mode command to be issued always).

TABLE 284: SET OTP PROGRAM MODE SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device to data transfer, using vendor-specific command, targeting interface
bRequest	0xF1	CMD_OTP_SET_PROGRAM_MODE
wValue	Programming Option	Indicates if the future CMD_OTP_PROGRAM commands will issue the PROGRAMVERIFY or PROGRAM command • 0x01 – PGMVFY • 0x02 – PROGRAM
wIndex	0x0000	Reserved
wLength	Data Length	No Data Command

Note 1: **Command phase:** Receives the SETUP packet as specified in the table
Status phase:
•ACK – On successful completion of the command

4.4.3 PROGRAM OTP TRANSACTION TO PROGRAM OTP CONFIGURATION DATA TO OTP

Method 1: Program the entire 8 kB in a single step.

This method allows the OTP to be updated with a signal program command, but requires transferring 8 kB to the hub before sending the program command.

To simplify the update process, it is recommended to first read back the entire 8 kB OTP memory space, insert the new Configuration data block and index signature to the read back file, and transfer the entire amended 8 kB back to the hub. Overwriting previously written to bytes with the same redundant data is supported and will have no negative effect.

With this method, OTP_ADDRESS is always 0x000, and wLength is always 0x1FFF.

Method 2: Program only the new configuration data block and signature index in two separate programming steps.

This method allows the hub OTP to be updated with the minimum amount of data transfer possible, but requires two separate program commands to achieve.

An alternate method is to perform an OTP memory dump, locate the offset of the configuration data block, and program only the new configuration block to the proper memory offset. Then, in a separate programming step, add the new configuration index signature to the correct memory offset.

An optional read-back step can be performed to ensure the data is correctly stored.

TABLE 285: OTP PROGRAM SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device data transfer, using vendor-specific command, targeting interface
bRequest	0x00	CMD_OTP_PROGRAM
wValue	OTP_ADDRESS	Address of the OTP memory for the Configuration Data block to be written
wIndex	0x00	Reserved
wLength	Data Length	Length of data to be written

Note 1: **Command phase:** Receives the SETUP packet with the parameters specified above
Data phase: Receives the data bytes of length wLength and programs the OTP accordingly
Status phase:
•STALL – on programming error
•ACK – on successful completion of programming

Use CMD_OTP_GET_STATUS to get the status for more information on the failure.

Note: Programming OTP via USB requires that a valid signature at the end of OTP is also manually generated and programmed to the correct memory location. There is no automated signature generation option when programming OTP via USB. For a configuration block to be loaded by the hub FW, steps 3 and 4 must also be followed correctly.

4.4.4 GET STATUS OTP TRANSACTION

To ensure the previous Configuration block was programmed to OTP successfully, issue the command in Table 286 to get the OTP status.

TABLE 286: OTP GET STATUS SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0xC1	Device-to-host to data transfer, using vendor-specific command, targeting interface
bRequest	0x02	CMD_OTP_GET_STATUS
wValue	0x0000	Address of the OTP ROM to be read
wIndex	0x0000	Reserved
wLength	0x01	One byte status to be returned

Note 1: **Command phase:** Receives the SETUP packet with the parameters specified above
Data phase: Sends the status byte
Status phase:
•STALL – on read error
•ACK – on successful completion of command

The status code returned is shown in Table 287.

TABLE 287: OTP STATUS CODES

Status Code	Description
0x00	Command successful completion
0x01	Generic error

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EXAMPLE 4-6: OTP PROGRAMMING EXAMPLE

An OTP patch is generated to change the value of register 0xBF80_3000 = 0x34 and 0xBF80_3001 = 0x12, such that the VID is changed to 0x1234.

The OTP contents for this patch would be:

```
80 BF 80 30 00 FE 00 02 34 12 FF
```

Step 1: An OTP memory read-back is performed, and the following data is returned (See Figure 4.):

FIGURE 4: EXAMPLE RETURNED OTP READ

	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
0000h	OTP Flags															
0010h	OTP Flags		80	BF	CF	80	8E	10	00	00	00	00	00	00	00	0B
0020h	12	1A	04	03	01	02	80	BF	D2	2E	1A	10	00	00	00	00
0030h	00	00	00	0B	24	0B	12	1A	04	03	01	02	FFh	00h	00h	00h
0040h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
0050h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
	00h	00h	00h	00h	00h	Blank Memory							00h	00h	00h	00h
…	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FC0h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FD0h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FE0h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FF0h	00h	00h	00h	00h	00h	00h	00h	00h	49h	44h	58h	D8h	00h	12h	00h	2Dh

Step 2: The Configuration data should be placed as shown in yellow in Figure 5 at memory offset 003Dh – 0047h.

The Configuration Index signature should be placed in the next available signature location as shown in yellow in Figure 5 at memory offset 1FF0h – 1FF7h.

FIGURE 5: OTP MEMORY WITH NEW CONFIGURATION DATA INSERTED

	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
0000h	OTP Flags															
0010h	OTP Flags		80	BF	CF	80	8E	10	00	00	00	00	00	00	00	0B
0020h	12	1A	04	03	01	02	80	BF	D2	2E	1A	10	00	00	00	00
0030h	00	00	00	0B	24	0B	12	1A	04	03	01	02	FFh	80h	BFh	80h
0040h	30h	00h	Feh	00h	02h	34h	12h	FFh	00h	00h	00h	00h	00h	00h	00h	00h
0050h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
	00h	00h	00h	00h	00h	Blank Memory							00h	00h	00h	00h
…	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FC0h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FD0h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FE0h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FF0h	49h	44h	58h	AAh	00h	3Dh	00h	0Bh	49h	44h	58h	D8h	00h	12h	00h	2Dh

The signature data is generated based upon the data contents, a checksum, the location that it is placed within the OTP memory, and the length. Hence, the signature for this example is shown in Figure 6.

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FIGURE 6: EXAMPLE CONFIGURATION INDEX

BYTE	1	2	3	4	5	6	7	8
Description	Signature			Checksum	CFG ADDRESS		CFG LENGTH	
Contents	I (49h)	D (44h)	X (58h)	AAh	00h	3Dh	00h	0Bh

Step 3: Send the CMD_OTP_PROGRAM command with the 8 kB of amended OTP data as the data payload for the USB transaction.

Step 4: Verify that programming was successful by sending CMD_OTP_GET_STATUS and verifying that the returned payload is 0x00.

Step 5: Perform another OTP memory read to confirm programming was successful.

4.5 Memory Access during Runtime via USB

The hub memory mapped registers can be accessed during runtime via USB. See Table 288 and Table 289.

Note: Not all registers should be modified during runtime as this could affect normal operation.

TABLE 288: MEMORY WRITE SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0x40	Host-to-device data transfer, vendor class, targeted to interface
bRequest	0x03	CMD_MEMORY_WRITE
wValue	ADDR_LO	Lower 16 bits of the Target Memory Address in little-endian format
wIndex	ADDR_HI	Upper 16 bits of the Target Memory Address in little-endian format
wLength	Data Length	Length of data to be written

Note 1: **Command phase:** Receives the SETUP packet with the parameters specified above
Data phase: Receives the data bytes of length wLength and writes data starting at the target memory address
Status phase:
•ACK – on successful completion of memory write

TABLE 289: MEMORY READ SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0xC0	Device-to-host data transfer, vendor class, targeted to interface
bRequest	0x04	CMD_MEMORY_READ
wValue	ADDR_LO	Lower 16 bits of the Target Memory Address in little-endian format
wIndex	ADDR_HI	Upper 16 bits of the Target Memory Address in little-endian format
wLength	Data Length	Length of data to read

Note 1: **Command phase:** Receives the SETUP packet with the parameters specified above
Data phase: Sends the data bytes of length wLength starting from the target memory address
Status phase:
•ACK – on successful completion of programming

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EXAMPLE 4-7: USB MEMORY WRITE

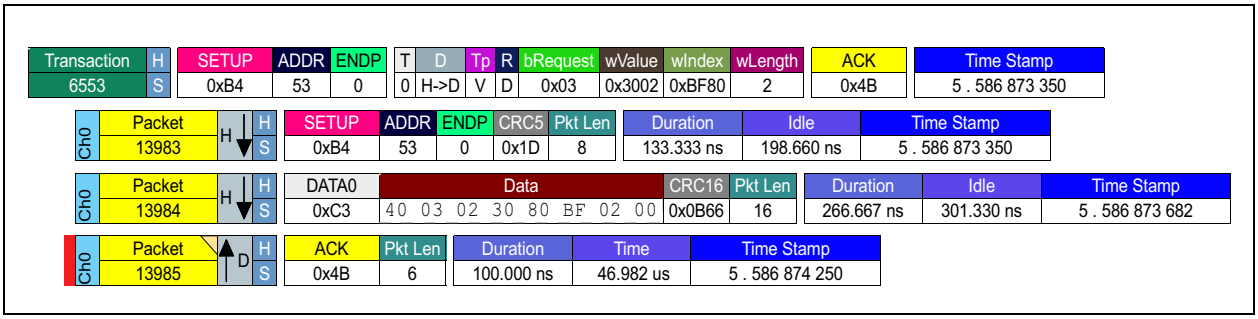
This example changes the PID at location BF80_3002h.

1. **Memory Write SETUP Phase Transaction:** The USB host sends the SETUP packet to the Hub Feature Controller at Endpoint 0. See Table 290 and Figure 7.

TABLE 290: MEMORY WRITE SETUP PACKET

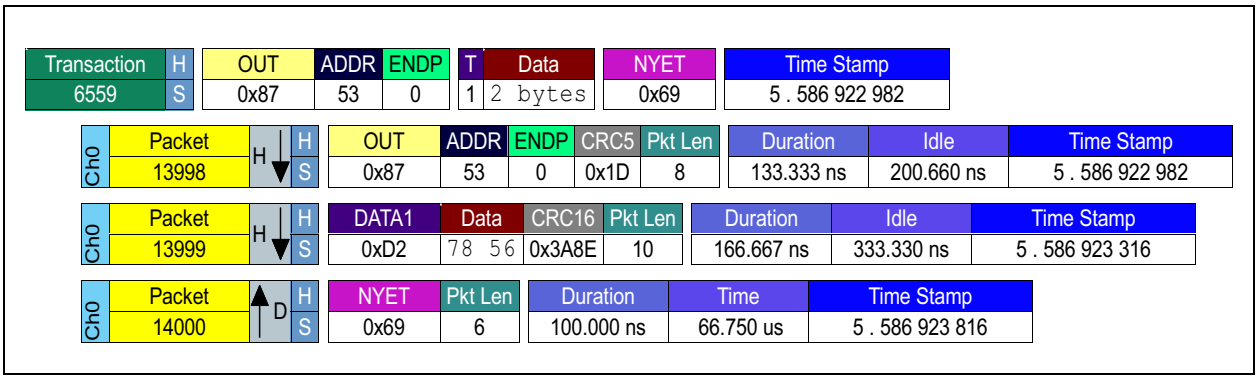
SETUP Packet	Value	Description
bmRequestType	0x40	Host-to-device data transfer, vendor class
bRequest	0x03	CMD_MEMORY_WRITE
wValue	0x3002	Lower 16 bits of the Target Memory Address in little-endian format
wIndex	0xBF80	Upper 16 bits of the Target Memory Address in little -endian format
wLength	0x0002	Length of data to be written

FIGURE 7: MEMORY WRITE SETUP TRANSACTION



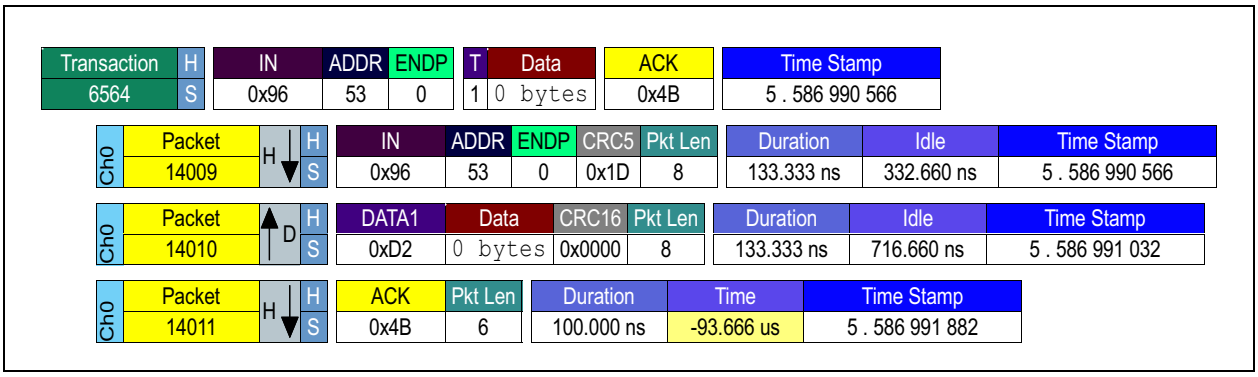
2. **Memory Write Data Phase OUT Transaction:** The USB host sends two data bytes to set BF803002 = 5678h. See Figure 8.

FIGURE 8: MEMORY WRITE OUT TRANSACTION



3. **Memory Write Status Phase IN Transaction:** The USB host sends an IN packet to complete the transfer. The Hub Feature Controller responds with a zero length data packet. See Table 290 and Figure 9.

FIGURE 9: MEMORY WRITE IN TRANSACTION



EXAMPLE 4-8: USB MEMORY READ

This example reads the PID at location BF80_3002h.

1. **Memory Read SETUP Phase Transaction:** The USB host sends the SETUP packet below to the Hub Feature Controller at Endpoint 0. See Table 291 and Figure 10.

TABLE 291: READ SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0xC0	Device-to-host data transfer, vendor class
bRequest	0x04	CMD_MEMORY_READ
wValue	0x3002	Lower 16 bits of the Target Memory Address in little-endian format
wIndex	0xBF80	Upper 16 bits of the Target Memory Address in little-endian format
wLength	0x0002	Length of data to read

FIGURE 10: MEMORY READ SETUP TRANSACTION

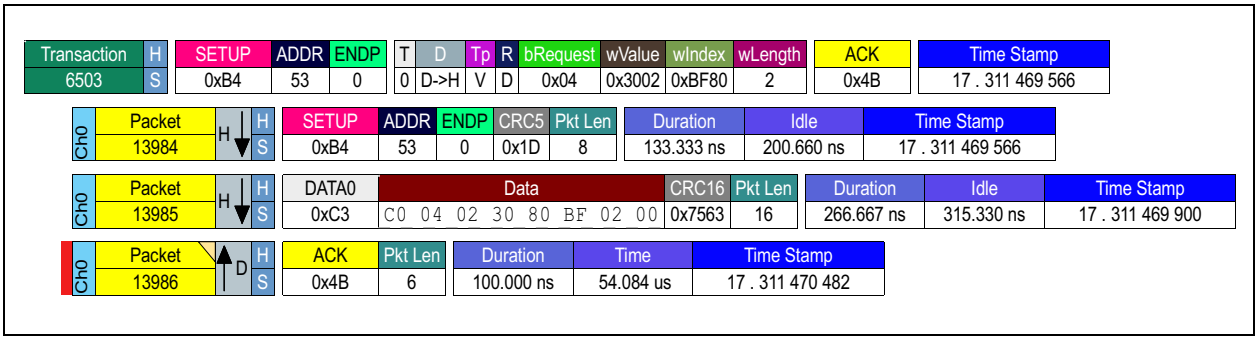


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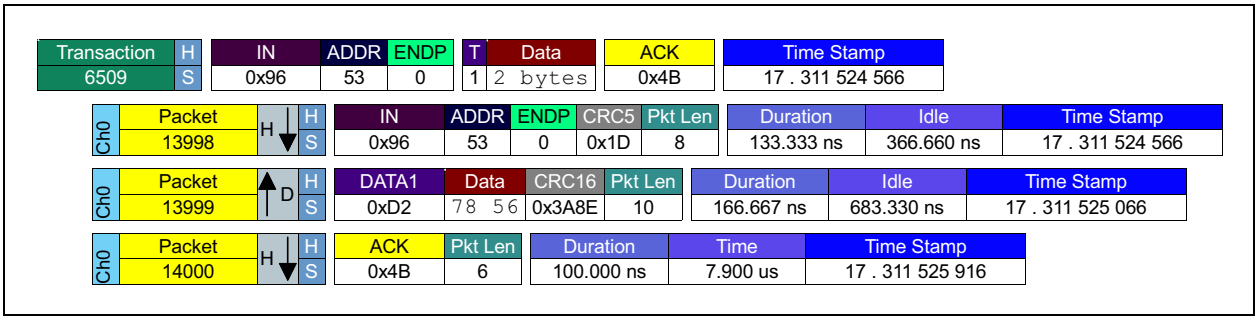
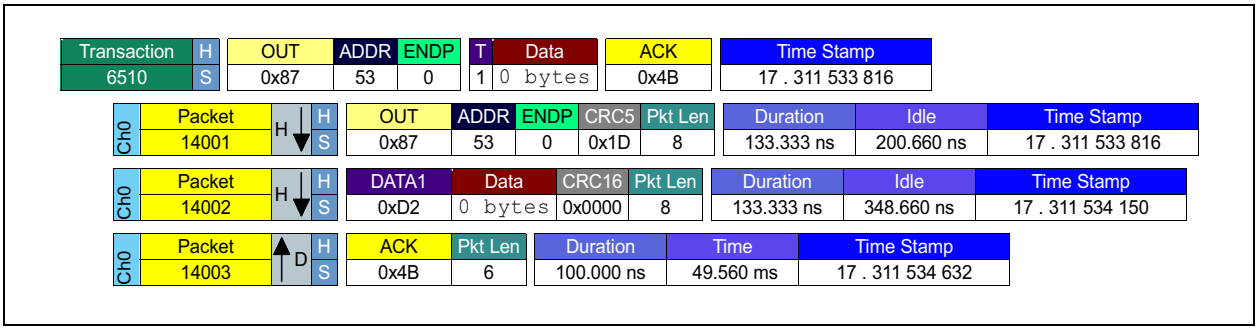
FIGURE 11: MEMORY READ IN TRANSACTION



2. **Memory Read Data Phase IN Transaction:** The USB host sends an IN packet to read the data. The Hub Feature Controller returns two bytes of data to complete the transfer. Data 5678h is read from location BF803002h. See Figure 11.
3. **Memory Read Status Phase OUT Transaction:** The USB host sends an OUT packet to complete the transfer. The Hub Feature Controller responds with a zero length data packet. See Figure 12.

FIGURE 12: MEMORY READ OUT TRANSACTION



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5.0 HUB PRODUCT IDS

5.1 Hub Feature Controller (UDC0)

The Hub Feature Controller (UDC0) is enabled by default, and thus reported as a non-removable device.

The Hub Feature Controller exposes different USB interfaces depending on the state of the configuration straps (CONFIG_STRAPx pins), enabling the features relevant to the selected PFx pins. Exposing a different PID for different configurations is required so that the correct USB client drivers are loaded.

The base PID is maintained as 0x7240. However, the last nibble is maintained to reflect the enabled features as shown in Table 292, with bit 0 indicating the presence of I²S™ HID, bit 1 indicating the presence of I²S Audio, bit 2 indicating the presence of CDC, and bit 3 indicating the presence of Generic USB Device (WinUSB on Windows).

TABLE 292: HUB FUNCTION CONTROLLER (UDC0) PIDS

WinUSB	CDC	I²S™ Audio	I²S HID	UDC0 Device Configuration	PID
No	No	No	No	No interface present; will not enumerate	NA
No	No	No	Yes	Invalid	NA
No	No	Yes	No	I²S™ Audio	7242h
No	No	Yes	Yes	I²S Audio, I²S HID	7243h
No	Yes	No	No	CDC Data, CDC Control	7244h
No	Yes	No	Yes	Invalid	NA
No	Yes	Yes	No	CDC Data, CDC Control, I²S Audio	7246h
No	Yes	Yes	Yes	CDC Data, CDC Control, I²S Audio, I²S HID	7247h
Yes	No	No	No	Generic USB Device (WinUSB on Windows)	7240h
Yes	No	No	Yes	Invalid	NA
Yes	No	Yes	No	Generic USB Device (WinUSB on Windows)	724Ah
Yes	No	Yes	Yes	Generic USB Device (WinUSB on Windows), I²S Audio, I²S HID	724Bh
Yes	Yes	No	No	Generic USB Device (WinUSB on Windows), CDC Data, CDC Control	724Ch
Yes	Yes	No	Yes	Invalid	NA
Yes	Yes	Yes	No	Generic USB Device (WinUSB on Windows), CDC Data, CDC Control, I²S Audio	724Eh
Yes	Yes	Yes	Yes	Generic USB Device (WinUSB on Windows), CDC Data, CDC Control, I²S Audio, I²S HID	724Fh

5.2 Hub PID Selection

Table 293 shows the Primary Hub, Secondary Hub, UDC1, and UDC2 PIDs based on the part number.

TABLE 293: PID SELECTION OPTIONS

Device	Package	USB2 HUB PID	USB3 HUB PID	Multi-Host Endpoint Reflector UDC1 PID (Upstream Port Side)	Multi-Host Endpoint Reflector UDC2 PID (Downstream Port Side)
USB7202	QFN100	4202h[1]	7202h[1]	7210h	7220h
USB7206	QFN100	4206h[1]	7206h[1]	7210h	7220h
USB7250	QFN100	4250h[1]	7250h[1]	7210h	7220h
USB7251	QFN100	4251h[1]	7251h[1]	7210h	7220h
USB7252	QFN100	4252h[1]	7252h[1]	7210h	7220h
USB7216/ USB7256	QFN100	4256h[1]	7256h[1]	7210h	7220h

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6.0 PHYSICAL AND LOGICAL PORT MAPPING

The USB7202/USB7206/USB7216/USB7250/USB7251/USB7252/USB7256 family of devices are based upon a common architecture, but all have different modifications and/or pin bond outs to achieve the various device configurations.

The base chip is composed of a total of 6 USB3 PHYs and 7 USB2 PHYs. These PHYs are physically arranged on the chip in a certain way referred to as the physical port mapping.

The actual port numbering may be remapped by default in different ways on each product. This changes the way that the ports are numbered from the USB host's perspective. This is referred to as logical mapping.

The various configuration options available for these devices may, at times, be with respect to physical mapping or logical mapping. Each individual configuration option which has a physical or logical dependency is declared as such within the register description.

The physical vs. logical mapping is described within each device's respective data sheet, and is also abbreviated from Table 294 to Table 297.

Note: The device data sheets also include visual aids for describing the logical vs. physical mapping.

A system design in schematics and layout is generally performed using the pinout from the device data sheet, which is assigned by the default logical mapping. Hence, it is necessary to cross reference the physical vs. logical lookup tables when determining the hub configuration.

Note: The MPLAB Connect tool makes configuration simple. The settings can be selected by the user with respect to the logical port numbering. The tool handles the necessary linking to the physical port settings.

TABLE 294: USB7202 PYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER						PHYSICAL PORT NUMBER						
		0	1	2	3	4	5	0	1	2	3	4	5	6
5	USB2DN_DP1		X						X					
6	USB2DN_DM1		X						X					
7	USB3DN_TXDP1A		X						X					
8	USB3DN_TXDM1A		X						X					
10	USB3DN_RXDP1A		X						X					
11	USB3DN_RXDM1A		X						X					
14	USB2DN_DP3				X					X				
15	USB2DN_DM3				X					X				
16	USB3DN_TXDP1B		X							X				
17	USB3DN_TXDM1B		X							X				
19	USB3DN_RXDP1B		X							X				
20	USB3DN_RXDM1B		X							X				
29	USB2DN_DP2			X							X			
30	USB2DN_DM2			X							X			
31	USB3DN_TXDP2A			X							X			
32	USB3DN_TXDM2A			X							X			
34	USB3DN_RXDP2A			X							X			
35	USB3DN_RXDM2A			X							X			
37	USB2DN_DP4					X						X		
38	USB2DN_DM4					X						X		
39	USB3DN_TXDP2B			X								X		
40	USB3DN_TXDM2B			X								X		
42	USB3DN_RXDP2B			X								X		
43	USB3DN_RXDM2B			X								X		

TABLE 294: USB7202 PYSICAL VS. LOGICAL PORT MAPPING (CONTINUED)

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER						PHYSICAL PORT NUMBER						
		0	1	2	3	4	5	0	1	2	3	4	5	6
81	USB3UP_TXDMB	X											X	
82	USB3UP_TXDPB	X											X	
84	USB3UP_RXDMB	X											X	
85	USB3UP_RXDPB	X											X	
89	USB2UP_DM	X						X						
90	USB2UP_DP	X						X						
91	USB3UP_TXDMA	X						X						
92	USB3UP_TXDPA	X						X						
94	USB3UP_RXDMA	X						X						
95	USB3UP_RXDPA	X						X						

TABLE 295: USB7206 PYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER							PHYSICAL PORT NUMBER						
		0	1	2	3	4	5	6	0	1	2	3	4	5	6
5	USB2DN_DP1		X							X					
6	USB2DN_DM1		X							X					
7	USB3DN_TXDP1		X							X					
8	USB3DN_TXDM1		X							X					
10	USB3DN_RXDP1		X							X					
11	USB3DN_RXDM1		X							X					
14	USB2DN_DP2			X							X				
15	USB2DN_DM2			X							X				
16	USB3DN_TXDP2			X							X				
17	USB3DN_TXDM2			X							X				
19	USB3DN_RXDP2			X							X				
20	USB3DN_RXDM2			X							X				
27	USB2DN_DP3				X							X			
28	USB2DN_DM3				X							X			
29	USB3DN_TXDP3				X							X			
30	USB3DN_TXDM3				X							X			
32	USB3DN_RXDP3				X							X			
33	USB3DN_RXDM3				X							X			
34	USB2DN_DP4					X							X		
35	USB2DN_DM4					X							X		
36	USB3DN_TXDP4					X							X		
37	USB3DN_TXDM4					X							X		
39	USB3DN_RXDP4					X							X		
40	USB3DN_RXDM4					X							X		
41	USB2DN_DP6							X							X
42	USB2DN_DM6							X							X
81	USB2DN_DP5						X							X	
82	USB2DN_DM5						X							X	

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TABLE 295: USB7206 PYSICAL VS. LOGICAL PORT MAPPING (CONTINUED)

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER							PHYSICAL PORT NUMBER						
		0	1	2	3	4	5	6	0	1	2	3	4	5	6
83	USB3DN_TXDM5						X							X	
84	USB3DN_TXDP5						X							X	
86	USB3DN_RXDM5						X							X	
87	USB3DN_RXDP5						X							X	
89	USB2UP_DM	X							X						
90	USB2UP_DP	X							X						
91	USB3UP_TXDMA	X							X						
92	USB3UP_TXDPA	X							X						
94	USB3UP_RXDMA	X							X						
95	USB3UP_RXDPA	X							X						

TABLE 296: USB7250, USB7251, USB7252 PYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER					PHYSICAL PORT NUMBER						
		0	1	2	3	4	0	1	2	3	4	5	6
5	USB2DN_DP1		X					X					
6	USB2DN_DM1		X					X					
7	USB3DN_TXDP1A		X					X					
8	USB3DN_TXDM1A		X					X					
10	USB3DN_RXDP1A		X					X					
11	USB3DN_RXDM1A		X					X					
14	USB2DN_DP4					X			X				
15	USB2DN_DM4					X			X				
16	USB3DN_TXDP1B		X						X				
17	USB3DN_TXDM1B		X						X				
19	USB3DN_RXDP1B		X						X				
20	USB3DN_RXDM1B		X						X				
29	USB2DN_DP2			X						X			
30	USB2DN_DM2			X						X			
31	USB3DN_TXDP2A			X						X			
32	USB3DN_TXDM2A			X						X			
34	USB3DN_RXDP2A			X						X			
35	USB3DN_RXDM2A			X						X			
37	USB3DN_TXDP2B			X							X		
38	USB3DN_TXDM2B			X							X		
40	USB3DN_RXDP2B			X							X		
41	USB3DN_RXDM2B			X							X		
81	USB2DN_DP3				X							X	
82	USB2DN_DM3				X							X	
83	USB3DN_TXDM3				X							X	
84	USB3DN_TXDP3				X							X	
86	USB3DN_RXDM3				X							X	

TABLE 296: USB7250, USB7251, USB7252 PYSICAL VS. LOGICAL PORT MAPPING (CONTINUED)

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER					PHYSICAL PORT NUMBER						
		0	1	2	3	4	0	1	2	3	4	5	6
87	USB3DN_RXDP3				X							X	
89	USB2UP_DM	X					X						
90	USB2UP_DP	X					X						
91	USB3UP_TXDM	X					X						
92	USB3UP_TXDP	X					X						
94	USB3UP_RXDM	X					X						
95	USB3UP_RXDP	X					X						

TABLE 297: USB7216/USB7256 PYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER							PHYSICAL PORT NUMBER						
		0	1	2	3	4	5	6	0	1	2	3	4	5	6
5	USB2DN_DP1		X							X					
6	USB2DN_DM1		X							X					
7	USB3DN_TXDP1A		X							X					
8	USB3DN_TXDM1A		X							X					
10	USB3DN_RXDP1A		X							X					
11	USB3DN_RXDM1A		X							X					
14	USB2DN_DP5						X				X				
15	USB2DN_DM5						X				X				
16	USB3DN_TXDP1B		X								X				
17	USB3DN_TXDM1B		X								X				
19	USB3DN_RXDP1B		X								X				
20	USB3DN_RXDM1B		X								X				
27	USB2DN_DP2			X								X			
28	USB2DN_DM2			X								X			
29	USB3DN_TXDP2			X								X			
30	USB3DN_TXDM2			X								X			
32	USB3DN_RXDP2			X								X			
33	USB3DN_RXDM2			X								X			
34	USB2DN_DP3				X								X		
35	USB2DN_DM3				X								X		
36	USB3DN_TXDP3				X								X		
37	USB3DN_TXDM3				X								X		
39	USB3DN_RXDP3				X								X		
40	USB3DN_RXDM3				X								X		
41	USB2DN_DP6							X							X
42	USB2DN_DM6							X							X
81	USB2DN_DP4					X								X	
82	USB2DN_DM4					X								X	
83	USB3DN_TXDM4					X								X	
84	USB3DN_TXDP4					X								X	

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TABLE 297: USB7216/USB7256 PYSICAL VS. LOGICAL PORT MAPPING (CONTINUED)

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER							PHYSICAL PORT NUMBER						
		0	1	2	3	4	5	6	0	1	2	3	4	5	6
86	USB3DN_RXDM4					X								X	
87	USB3DN_RXDP4					X								X	
89	USB2UP_DM	X							X						
90	USB2UP_DP	X							X						
91	USB3UP_TXDMA	X							X						
92	USB3UP_TXDPA	X							X						
94	USB3UP_RXDMA	X							X						
95	USB3UP_RXDPA	X							X						

7.0 BILLBOARD DEVICE

An internal Billboard device is used to communicate certain conditions within a Power Delivery system, such as failure to establish a DisplayPort Alternate mode. For device with native Power Delivery support (USB7250, USB7251, USB7252, USB7216, and USB7256), the hub firmware automatically determines the appropriate timing for attaching and detaching the Billboard device.

Devices without native Power Delivery support may still be used within a Power Delivery system, and the internal Billboard device may still be used. These hubs require control from an external Power Delivery controller. The external Power Delivery controller can force the Billboard device to attach or detach through:

- Hub SMBus client interface
- Hub GPIO pin

The Billboard device attaches as an added interface to the existing Hub Feature Controller interface, UART COM interface, and I^{2}S™ Audio interface that are enabled.

7.1 Enabling Billboard Device Functionality

The BILLBOARD_ENABLE (bit 9) in Table 210 must be set to '1' in order for the billboard device to be enabled with the options below.

7.1.1 BILLBOARD DEVICE CONTROL THROUGH SMBUS

Issue the special command via SMBus during hub runtime stage to control the attach or detach of the Billboard device. See Table 298.

TABLE 298: SPECIAL SMBUS COMMANDS

Operation	OPCODE	Description
Billboard Device Attach	AA 5C 00h	Attach the Billboard Interface.
Billboard Device Detach	AA 5D 00h	Detach the Billboard Interface.

7.1.2 BILLBOARD DEVICE CONTROL THROUGH GPIO

A pin which is not allocated for any other purpose in the hub configuration may be assigned the role of Billboard enable GPIO.

The pin is selected through the register below, which can be configured through OTP or through SMBus configuration.

When the pin is sensed as low, this will trigger the Billboard device to attach. The Billboard device is automatically detached after it has been enumerated by the host and the detach timer expires. See Table 299.

TABLE 299: BILLBOARD DEVICE

GBYBBGPIO ADDRESS: BFD2_458Eh RESET = 14h			**Billboard Device Control Input GPIO Assignment**
Bit	**Name**	**R/W**	**Description**
7:0	GPIO_SELECT	R/W	Value selects the GPIO to be used for Billboard Device control input: Selects the PIO used for Billboard Device Trigger. Example: Map PF29 as Billboard Device Control PF29 is associated with GPIO93. To select PF29, set GPIO_SELECT = 5Dh (93d)

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7.2 Billboard Device Detach Timer

The Billboard device can be configured to automatically detach after a timer expires. This timer can be configured using the register in Table 300.

TABLE 300: BILLBOARD DETACH TIMER

GBYBBDETACHHBUNIT ADDRESS: BFD2_458Ch RESET = 00h			**Billboard Device Auto Detach Timer**
Bit	**Name**	**R/W**	**Description**
7:0	Reserved	R/W	Timer for automatic detach of the Billboard device. This is configured in 5 ms intervals. 0000_0000: Timer disabled 0000_0001: Detach after 5 ms ... 1111_1111: Detach after 1,275 ms

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002935B (12-23-20)	Table 1 - Table 2	Reworked tables to add registers and re-arrange ordering of other registers. Consolidated three tables into two.
	Table 4	Deleted Note 1 (note not applicable to register)
	Table 6 - Table 11	Fixed bit offset typo in Note 1 for bits 23:16 and bits 31:24 for all registers
	Table 73 - Table 76	Added “USB2” to register titles to improve clarity.
	Table 93 - Table 102	Added new registers.
	Table 119 - Table 126	Changed all Type-A status bits to Reserved.
	Table 263	Corrected default value.
	Table 264	Corrected port numbering typos for Configuration bits 3-5
	Table 246 - Table 264	Corrected base address and offset.
	Table 299	Correction to Configuration bit options for selecting Billboard enable GPIO.
	Section 7.1.2, Billboard Device Control through GPIO	Revised wording on GPIO behavior to improve clarity.
	All	Added USB71216 to the list of devices. Replaced deprecated terms, “master” and “slave” with “host” and “client,” respectively. Made minor text and formatting changes.
DS00002935A (3-27-19)	Initial release	

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