AN2936

USB-to-UART Bridging with Microchip USB7202, USB7250, USB7251, and USB7252 Hubs

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INTRODUCTION

The USB-to-UART bridging feature of Microchip hubs provides system designers with expanded system control and potential BOM reductions. When using Microchip's USB hubs, a separate USB-to-Universal-Asynchronous-Receiver-Transmitter (UART) device is no longer required and a downstream USB port is not lost as occurs when a standalone USB-to-UART device is implemented. This feature is available on the Microchip USB7202, USB7250, USB7251, and USB7252 hubs.

Commands may be sent from the USB Host to the internal Hub Feature Controller (HFC) device in the Microchip hub to perform the following functions:

- Enable/Disable UART Interface
- Set UART Interface Baud Rate
- UART Write
- UART Read

SECTIONS

REFERENCES

Consult the following documents for details on the specific parts referred to in this document:

- *Microchip USB7202 Data Sheet*
- *Microchip USB7250 Data Sheet*
- *Microchip USB7251 Data Sheet*
- *Microchip USB7252 Data Sheet*
- *Microchip AN2935 Configuration of USB7202/USB7206/USB725x*

GENERAL INFORMATION

Microchip hub USB Bridging features work via host commands sent to an embedded Hub Feature Controller within the device located on an additional internal USB port. In order for the bridging features to work correctly, this internal Hub Feature Controller must be enabled by default. Table 1 provides details on default Hub Feature Controller settings per device.

TABLE 1: DEFAULT SETTINGS FOR HUB FEATURE CONTROLLER ENABLE

Part Number	Part Summary	Hub Feature Controller Default Setting
USB7202	4-Port USB3.1G1 hub – 2xUSB-C with cc pin i/f, 2 x Type A DFP (2.0), No PD	Enabled by default
USB7250	4-Port USB3.1G1 hub – 2xUSB-C with UPD350, 2 x Type A DFP (2.0/3.1), PD FW	Enabled by default
USB7251	4-Port USB3.1G1 hub – 2xUSB-C with cc pin/350, 2 x Type A DFP (2.0/3.1), PD FW	Enabled by default
USB7252	4-Port USB3.1G1 hub – 2xUSB-C with cc pin i/f, 2 x Type A DFP (2.0/3.1), PD FW	Enabled by default

The Hub Feature Controller is connected to an extra internal port in the hub. It is mapped to the highest numbered port on the hub by default.

The internal block diagrams of the USB7202, USB7250, USB7251, and USB7252 in an upstream Type-C application are shown in Figure 1, Figure 2, Figure 3, and Figure 4, respectively.

FIGURE 1: USB7202 INTERNAL BLOCK DIAGRAM – UPSTREAM TYPE-C APPLICATION

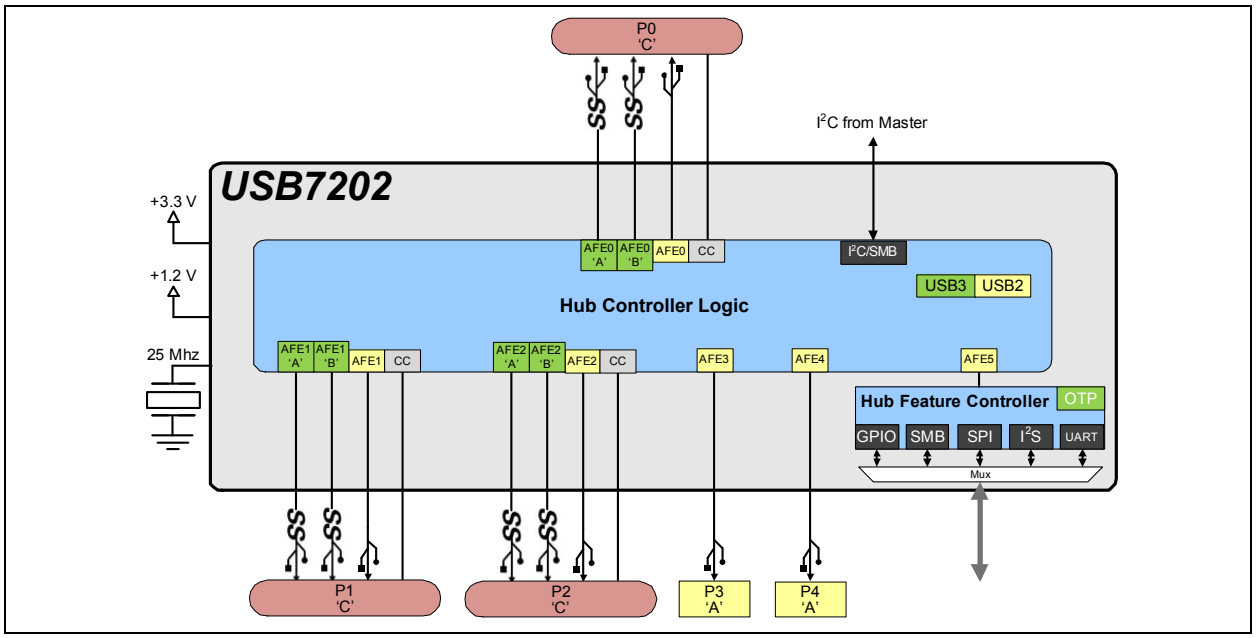


FIGURE 2: USB7250 INTERNAL BLOCK DIAGRAM – UPSTREAM TYPE-C APPLICATION

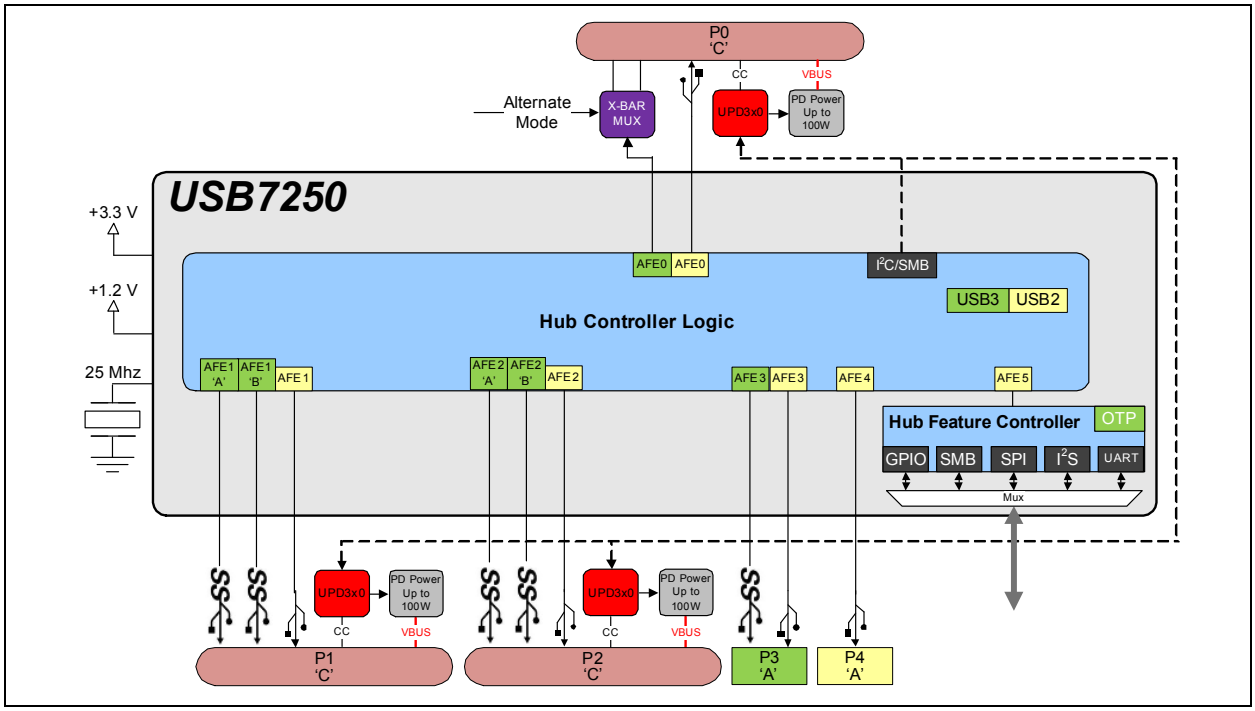


FIGURE 3: USB7251 INTERNAL BLOCK DIAGRAM – UPSTREAM TYPE-C APPLICATION

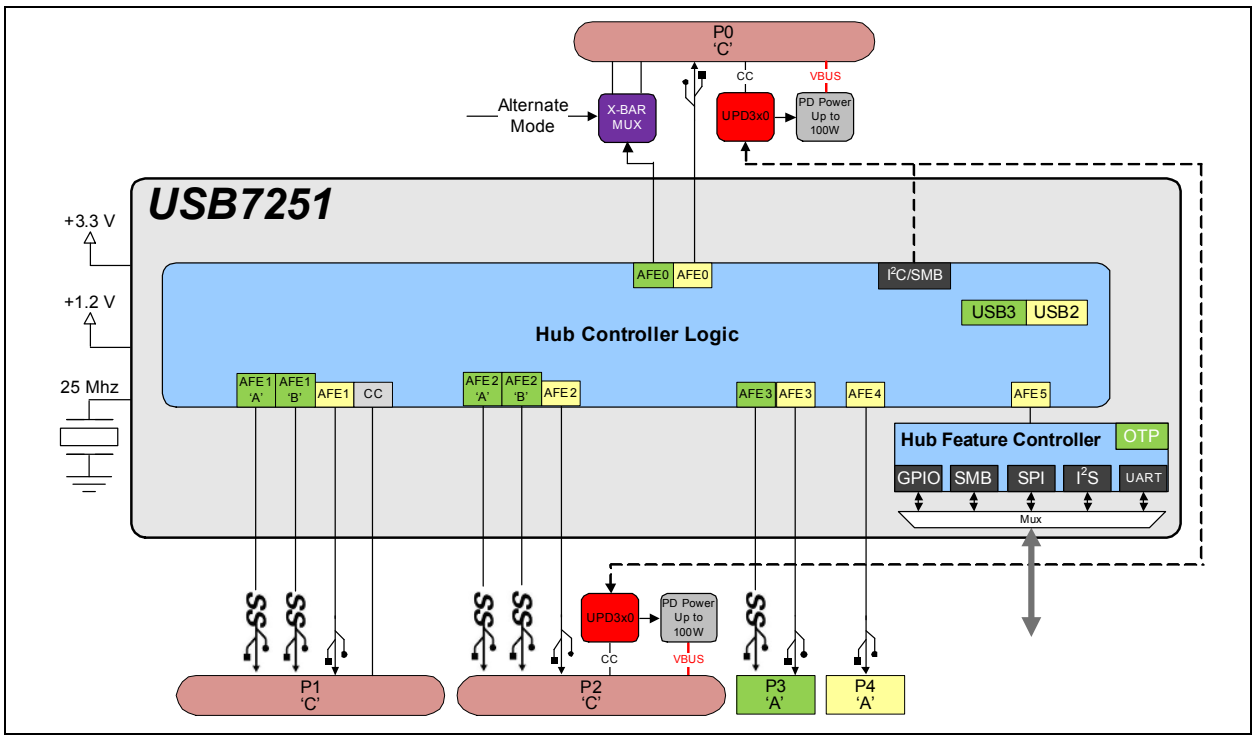
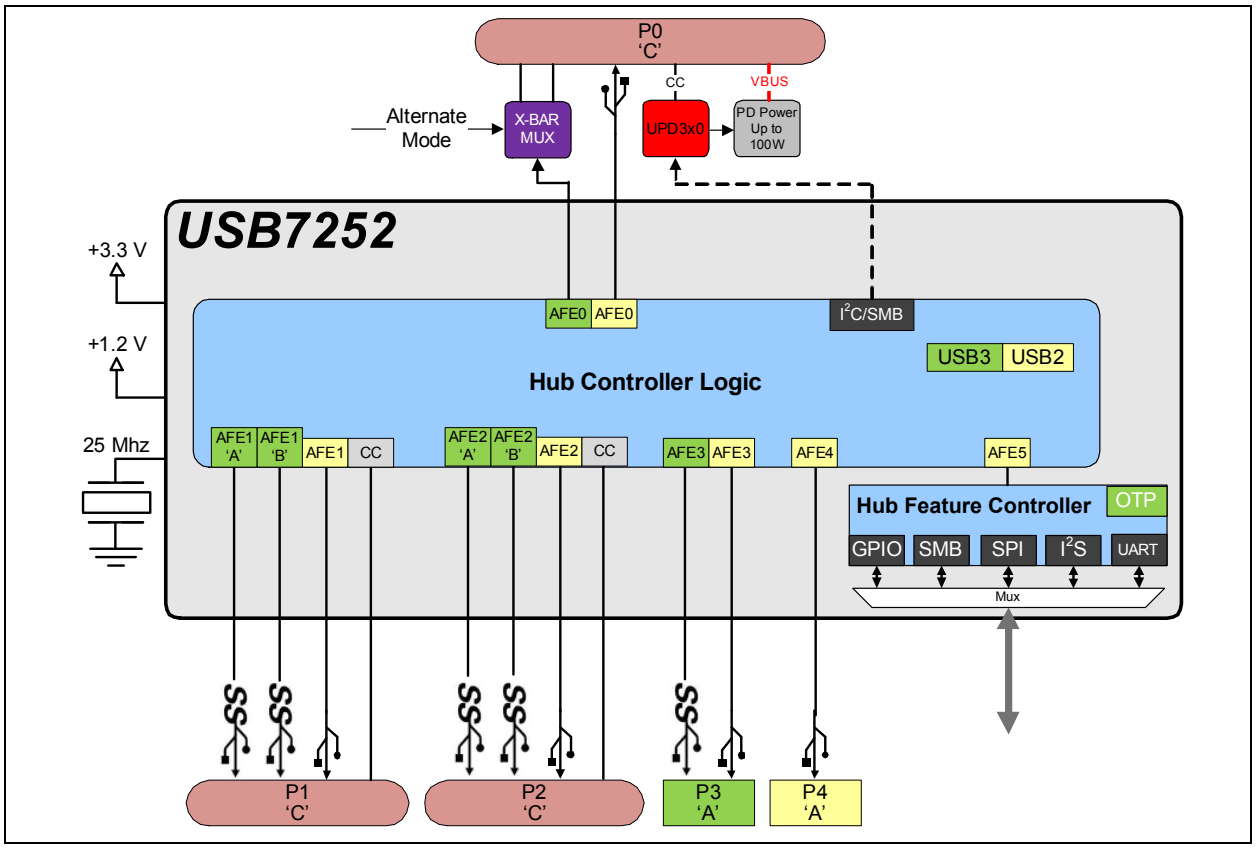


FIGURE 4: USB7252 INTERNAL BLOCK DIAGRAM – UPSTREAM TYPE-C APPLICATION



UART Bridging Commands

The following UART functions are supported:

- Enable/Disable UART Pass-Through Interface
- Set UART Baud Rate
- UART Write
- UART Read

ENABLE/DISABLE THE UART INTERFACE

A single command to enable the UART interface is required before performing any UART Write or Read commands. The UART interface has a variable baud rate which can be adjusted via a bridging command. The UART interface may be disabled after writing/reading to the device is complete.

Note:	The maximum possible UART baud rate in both HS and FS without flow control is 115.2 kHz.

SET UART BAUD RATE

The UART baud rate may be adjusted via a bridging command. The suggested standard baud rate values are 600 Hz, 1.2 kHz, 2.4 kHz, 4.8 kHz, 9.6 kHz, 19.2 kHz, 38.4 kHz, 57.6 kHz, and 115.2 kHz.

UART WRITE

Transfer data through the UART serial port to a connected serial peripheral.

UART READ

Synchronously receive data through a serial port from a connected serial peripheral.

UART Interface Details

UART INTERFACE

The device incorporates a fully programmable UART that is functionally compatible with the NS 16550AF, 16450, 16450 ACE registers, and the 16C550A. The UART performs serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. Two sets of baud rates are provided: 24 MHz and 16 MHz. When the 24 MHz source clock is selected, standard baud rates from 50K to 115.2K are available. When the source clock is 16 MHz, baud rates from 125K to 1,000K are available. The character options are programmable for the transmission of data for the following:

- Word lengths ranging from five to eight
- One Start bit
- One, 1.5, or 2 Stop bits
- Even, odd, sticky or no parity
- Prioritized interrupts

The UART contains a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from one to 65535. The UART is also capable of supporting the MIDI data rate.

TRANSMIT OPERATION

Transmission is initiated by writing the data to be sent to the TX Holding register or TX FIFO (if enabled). The data is then transferred to the TX Shift register together with a Start bit and parity and Stop bits as determined by settings in the Line Control register. The bits to be transmitted are then shifted out of the TX Shift register in the following order: Start bit, Data bits (LSB first), Parity bit, and Stop bit. This can be done using the output from the Baud Rate Generator (divided by 16) as the clock.

If enabled, a TX Holding register Empty interrupt is generated when the TX Holding register or the TX FIFO (if enabled) becomes empty.

When FIFOs are enabled (i.e. bit 0 of the FIFO Control register is set), the UART can store up to 16 bytes of data for transmission at a time. Transmission continues until the TX FIFO is empty. The FIFO's readiness to accept more data is indicated by interrupt.

RECEIVE OPERATION

Data is sampled into the RX Shift register using the Receive clock, divided by 16. The Receive clock is provided by the Baud Rate Generator. A filter is used to remove spurious inputs that last for less than two periods of the Receive clock. When the complete word has been clocked into the receiver, the data bits are transferred to the RX Buffer register or to the RX FIFO (if enabled) to be read by the CPU. (The first bit of the data to be received is placed in bit 0 of this register.) The receiver also checks that the Parity bit and Stop bits are as specified by the Line Control register.

If enabled, an RX Data Received interrupt is generated when the data has been transferred to the RX Buffer register or when the RX Trigger Level has been reached provided that FIFOs are enabled. Interrupts can also be generated to signal RX FIFO Character Timeout, incorrect parity, a missing Stop bit (frame error), or other line status errors.

When FIFOs are enabled (i.e. bit 0 of the FIFO Control register is set), the UART can store up to 16 bytes of received data at a time. Depending on the selected RX Trigger Level, interrupt goes active to indicate that data is available when the RX FIFO contains 1, 4, 8, or 14 bytes of data.

PART NUMBER-SPECIFIC INFORMATION

Part Summary

Table 2 to Table 5 show the UART interface pins by part number and notes on those pins:

TABLE 2: USB7202 UART PINS

	CONFIG1	CONFIG2	CONFIG3	CONFIG4
PF6	*UART NOT AVAILABLE*	*UART NOT AVAILABLE*	*UART_RX*	*UART NOT AVAILABLE*
PF7			*UART_TX*	
PF14			*UART_nCTS*	
PF18			*UART_nDCD*	
PF19			*UART_nRTS*	
PF26			*UART_nDSR*	
PF27			*UART_nDTR*	

TABLE 3: USB7250 UART PINS

	CONFIG1	CONFIG2	CONFIG3	CONFIG4
PF2	*UART NOT AVAILABLE*	*UART NOT AVAILABLE*	*UART_nCTS*	*UART NOT AVAILABLE*
PF3			*UART_nRTS*	
PF4			*UART_nDSR*	
PF5			*UART_nDTR*	
PF6			*UART_RX*	
PF7			*UART_TX*	
PF28			*UART_nDCD*	

TABLE 4: USB7251 UART PINS

	CONFIG1	CONFIG2	CONFIG3	CONFIG4
PF6	*UART NOT AVAILABLE*	*UART NOT AVAILABLE*	*UART_RX*	*UART NOT AVAILABLE*
PF7			*UART_TX*	
PF14			*UART_nCTS*	
PF19			*UART_nRTS*	
PF26			*UART_nDSR*	
PF27			*UART_nDRT*	
PF28			*UART_nDCD*	

Note 1: Typo DOS Page 506 Table 25.7 PF28 = UART_nDSD (should be DCD)

TABLE 5: USB7252 UART PINS

	CONFIG1	CONFIG2	CONFIG3	CONFIG4
PF6	***UART NOT AVAILABLE***	***UART NOT AVAILABLE***	*UART_RX*	***UART NOT AVAILABLE***
PF7			*UART_TX*	
PF14			*UART_nCTS*	
PF19			*UART_nRTS*	
PF26			*UART_nDSR*	
PF27			*UART_nDRT*	
PF28			*UART_nDCD*	

Note 1: Typo DOS Page 506 Table 25.8 PF28 = UART_nDSD (should be DCD)

SOFTWARE IMPLEMENTATION

The UART Bridge interface automatically appears as a standard serial COM port when the UART interface is enabled via correct CFG_SEL pin strapping. The USB-to-UART bridge may be sent commands using the standard COM port drivers that are native to most operating systems. No special drivers or USB commands are required. Thus, the USB-to-UART interface does not require any special software development or the use of the MPLAB Connect DLL library.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002936A (2-27-19)	All	Initial release

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