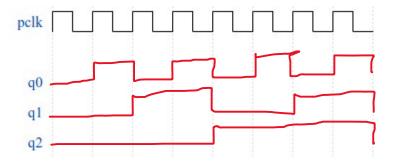
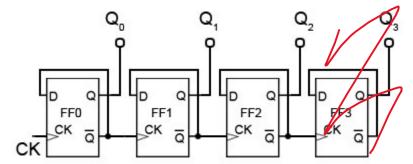


a. The starting state is Q0=Q1=Q2=0. This is a rising-edge device. Fill out the timing diagram below.

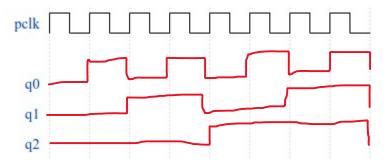


- b. What kind of counter is this? 3Bit Binary Up Ripple Counter (Asynchronous)
- c. Fill out the table below.

State number	Q2	Q1	Q0
0 (no rising edges yet)	0	0	0
1 (after first edge)	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0
9	0	0	1

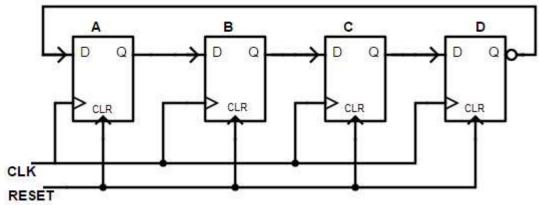


a. The starting state is Q0=Q1=Q2=0. This is a rising-edge device. Fill out the timing diagram below. Ignore Q3.

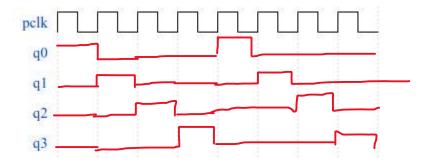


- b. What kind of counter is this? 3 Bit Binary Up Ripple Counter (Async)
- c. How is this different to the counter in #1? It uses D type instead of JK
- d. Fill out the table below.

State number	Q2	Q1	Q0
0 (no rising edges yet)	0	0	0
1 (after first edge)	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0
9	0	0	1



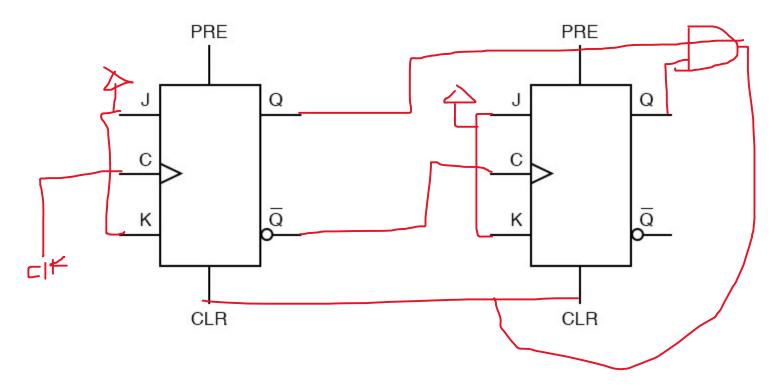
b. The starting state is Q0=1, Q1=Q2=Q3=0. This is a rising-edge device. Fill out the timing diagram below. Ignore the RESET line. (A=Q0, B=Q1, C=Q2, D=Q3)



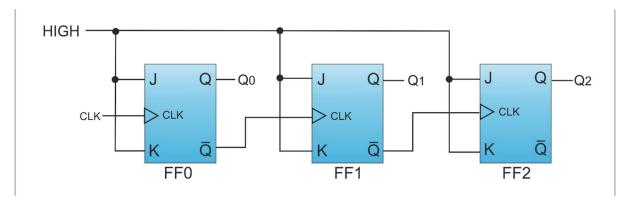
- b. What kind of counter is this? 4 bit ring counter (synchronous)
- c. How is this different to the counters in #1 and #2? Moves data through rather than "counting"
- d. Fill out the table below.

State number	Q3	Q2	Q1	Q0
0 (no rising edges yet)	0	0	0	1
1 (after first edge)	0	0	1	0
2	0	1	0	0
3	1	0	0	0
4	0	0	0	1
5	0	0	1	0
6	0	1	0	0
7	1	0	0	0
8	0	0	0	1
9	0	0	1	0

4. Design a mod-3 asynchronous counter using JK flip-flops. Use the RESET line (also called CLR)!



5. We talked about the "glitch" or unwanted states that arise when using asynchronous counters. Fill out the table below detailing those glitch states. This is a rising-edge device. Use the counter from #1 as reference:



GLITCH STATES FOR A 3-BIT ASYNCHRONOUS COUNTER (000->111)

CURRENT STATE	NEXT STATE	GLITCH STATES IN BETWEEN
000	001	N/A
001	010	000
010	011	N/A
011	100	010, 000
100	101	N/A
101	110	100
110	111	N/A
111	000	110, 100