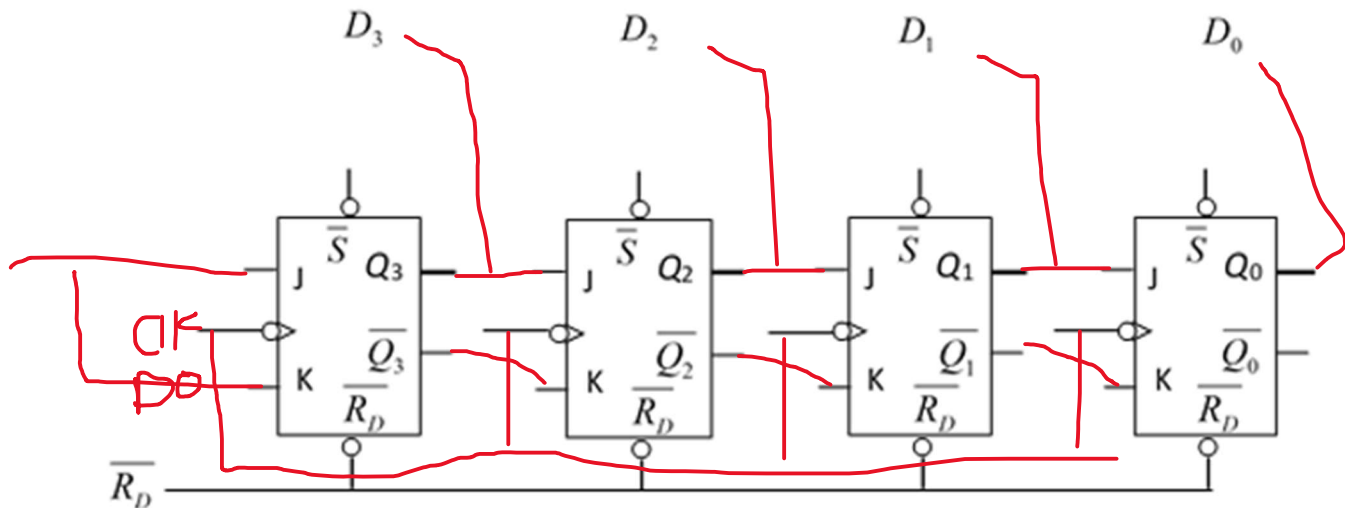**DLD STEM ICE – Week 2 Monday AM Part 2**

1. Construct a 4-bit shift register with JK flip-flops. Load the shift register serially, take output in parallel. Let D3 be the MSB and D0 be the LSB.

a. Complete the function table for a JK flip flop.

J	K	Q
0	0	Hold
0	1	0 (reset)
1	0	1 (set)
1	1	toggle

b. Make the clock connections on the diagram above so that all the JK flip flops are clocked at the same time (synchronously).

c. Make J and K connections for data to shift right (Hint: output of one becomes input of the other). For the input into J3 and K3, what must the relationship be between J3 and K3? How can you use logic to ensure that is always true? **J3≠K3**

d. What are the logic values at Q3, Q2, Q1, and Q0 initially? Initially we don't know, unless we assert the reset pin (R_D)

e. Serially load binary number "0000" onto the shift register. Complete the table for loading "0000"
f. Now we will serially load decimal number 11 onto the shift register. Add loading 11 to the table below. Binary: 1011

Clock Pulse	Q3	Q2	Q1	Q0
0	?	?	?	?
1	0	?	?	?
2	0	0	?	?
3	0	0	0	?
4	0	0	0	0
5	1	0	0	0
6	1	1	0	0
7	0	1	1	0
8	1	0	1	1
9				
10				
11				
12				

g. How many clock pulses will it take to "clear" ("0000") serially? How many clock pulses did it take to load 11 serially? How many clock pulses total? **4, 4, 8 total**

h. Draw the timing diagram from D3, D2, D1, and D0 from the table with the flip flops falling-edge triggered. (Sketch the clock pulse at the top then logic values for Q3, Q2, Q1, and Q0).