Clock Detector

1. Detect Available Clocks:
   - Checks the availability of each clock input by creating a "slow" clock for each clock domain and verifying if it toggles within a timeout.

2. Select Clocks: Selects a clock based on two conditions:
   - The clock is available.
   - Clock priority.

PPS (Pulse per second) Slave

1. PPS Timestamping:

   - Uses a high-resolution clock to timestamp PPS input.
   - The timestamp is taken when a PPS edge is detected, and the event is marked in the shift register.
   - Compensates for delays in high-resolution clock, input, and cable delays.

2. PPS Input Validation:

   - Validates the PPS input by checking the pulse period (expected ~1 second) and pulse width (expected 900ms low, and 100ms high if configured to check on the rising edge).
   - When the pulse period or width is out of bounds, an error is reported, and the timestamp is ignored.
   - Initialization requires two active edges of the PPS input for proper synchronization.

3. Offset and Drift Correction Calculation:

   - Calculates offset by comparing the timestamp with the nearest second change (positive if after, negative if before).
   - Calculates drift as the delta between two consecutive timestamps, normalized over the interval.
   - Sends calculated corrections to the Adjustable Clock, which applies smooth offset and drift adjustments to the local clock.

Adjustable Clock

1. Offset and Drift Adjustments: Processes the offset and drift adjustments.
   - Receives the offset (phase) and drift adjustment values (frequency) from PPS Slave.
   - Converts the adjustments into incremental corrections.
   - Generates correction signals for the timer clock.

2. Corrections to the timer clock: Applies the corrections to the timer clock.
   - Keeps the timer clock running continuously whilst applying precise corrections.
   - Time sets the timer clock if the changes are too large to apply smoothly.

3. Adjustable clock flags: Updates the InSync and InHoldover flags
   - InSync flag
     - Activated if 4 consecutive offset adjustments are below a predefined threshold.
     - Deactivated if a time set is applied, the offset adjustment is too large, or the clock is disabled.
   - InHoldover flag
     - Activated if the timer clock was InSync and no offset adjustment is received for a predefined timeout period.
     - Deactivated if the clock goes out of sync, a time set or offset adjustment is received, or the clock is disabled.

Time of Day (Tod) Slave: Need to configure for CAN.

1. UART Reception:

   - UART Reception: Converts UART signals to byte streams, handles RS232 protocol, and supports multiple baud rates for communication with GNSS receivers.
   - Message Detection: Detects and extracts information from UBX and TSIPv1 messages, including time and status data. Invalid or unsupported messages are ignored.
   - Time Conversion: Converts GNSS time to TAI (International Atomic Time) in seconds format, enabling synchronization with the Adjustable Clock.
   - Time Adjustment: Compares calculated TAI with the current time, and if they differ, adjusts the time at the beginning of the next second for smooth synchronization.

2. Supported GNSS Message Types:

   - UBX Protocol: Supports several UBX message types (e.g., MOMN HW, NAV SAT, NAV TIMELS, NAV TIMEUTC, NAV STATUS) for reporting antenna status, satellites, UTC offset, time, and GPS fix.

- TSIP Protocol: Supports TSIP messages like Timing Info, Alarms, Receiver Info, Position Info, and Satellite Info for reporting similar data as UBX but in different formats.

3. Time Adjustment Details:
    - When TAI seconds differ from the clock time, a time adjustment is applied at the next second's start, with the nanoseconds field set to zero.
    - The adjustment is applied 2 clock cycles before the new second begins to ensure smooth synchronization.

PPS Generator

1. Main Operations:
    - Periodically Generate the Pulse: The PPS pulse is generated at the start of each new second of the synchronized local time, adjusting for accumulated output delays. The pulse generation is aligned with the local time and has a fixed duty cycle of 500ms.
    - Fine-Tune Pulse Generation: The pulse is generated with high precision by a high-resolution clock, compensating for output delays, and ensuring exact timing.
2. Periodically generate the PPS
    - The pulse generation starts when the local time reaches a new second, and the system compares the current local time with the max nanosecond value (1 second) minus the output delays.
    - The duty cycle is fixed, and pulse deactivation may not align with local time. Errors are reported if the local time is disabled or a time jump occurs, but the pulse continues until the issue is resolved.
3. Computing the exact time of the generation
    - A high-resolution clock, whose frequency is a multiple of the system clock, is used to fine-tune the PPS pulse generation.
    - A shift register is used to track the number of high-resolution clock periods required to match the time difference between the local time and the pulse generation time.

Communication Selector

- Determines which communication interface (UART, I2C, CAN) will be used between the FPGA and the oscillators (CSAC, TCXO).