Each team member will identify at least one topic/skill that is new to them that they will learn independently, and which will help the team. This may be something technical (e.g., learn a new CAD package, fabrication skill, or discipline-specific analysis tool or technique, etc.), it could be process-related (e.g. new project management tool, or a design process tool), or it could be a personal skill (e.g., communication, personal task management, or interacting with your team).

Luke Schrom :

- I want to try and design the systems on the FPGA in Vivado and try and hone my skill with PCB design in Altium.
- This will benefit the team because we will be able to have two different eyes on the FPGA design and the hardware design
- I will complete the on boarding from RIT EVT for Altium designer https://docs.google.com/document/d/1PLjWkKGezvbbdJ3cc1dlqvaQjWPtTVO7K9AMgZSgf5M/edit#heading=h.dpvxiju8vobr
- I will complete the tutorial by the end of the system level design phase. And I will be contributing to the teams PCB design

Eva Czukkermann

1. I plan to expand my Ansys analysis skills
2. This will be beneficial when we need to analyze the mechanical (structural, thermal) aspects of the project. Additionally, having these skills will benefit me once I graduate.
3. I will watch some videos and/or read some articles about the different things to consider when running structural and thermal analysis in ANSYS. Websites include:
   Structural:https://www.linkedin.com/pulse/understanding-structural-analysis-ansys-eleation
   Thermal:https://thermalds.com/thermal-analysis-thermal-modeling/
4. I will complete this and return to my team with the results once we have an initial model of the board that I can use in the analysis. This should be before the end of the fall semester ideally.

Nsadhu Muyinda:

- The team will be using Verilog to design the logic on the FPGA, however I only have experience with VHDL. I plan to learn Verilog.
- This will give the team another person to help with problem solving for the FPGA design.
- I am going to complete the Verilog HDL basics course by intel. https://learning.intel.com/developer/learn/courses/235/verilog-hdl-basics
- I'll complete the tutorial by the end of the System Level Design Phase and I will be contributing to the team's FPGA design.