Detailed Design Review Notes: P22257

Date 12/5/2024

Attendees

- Team - Ian, Tanner, Luke, Drew, Eva, Nsadhu
- Guide - Dr. McCauley
- Client - Philip Linden, Ashley Kosak
- Guests - Carlos Barrios, Rachel Williams, Mark Indovina, Stephen

Goals

- Present current progress of project

Agenda and discussion notes

Time	Item	Who	Notes
60 min	Design Review Presentation	Team	See below
15 min	Questions/Comments	All	See below

Issues Raised

- See Action Items section

Decisions Made

- Requirements are during steady state operations. Ok if takes a day to stabilize
- Power budget is 5 watts

Action items/Meeting Notes

- Join OCP TA Discord to ask everyone directly about calculations for feasibility analysis done by Ian
    - Join time card server
- Want to see more detail on what is plugging into Fref, are clock and GNSS going to same rail?
    - Make a diagram to understand mapping of everything
- Get external TCXO controlled by DAQ, need reference to compare to Atomic Clock
    - Adjust TCXO with DAQ to get much more stable block
    - If keep digital it will drift over long periods of time, analog will keep it stable
    - reference block is driving TCXO
    - use DPLL to drive a DAQ
    - reference side where you're adjusting is slightly different
    - Meet with Mark, he will help
- Create design limit for % utilization for SOC - 80% is a good limit

- Email support about getting footprint and pin out for CSAC
- Need to complete feasibility for power budget - why is it 5 watts
- Ask Carlos about connectors, solder mask, need to make sure board house can put solder mask between pads
    - Consider doing signal planes in the middle
    - Carlos worried about noise in both directions - can talk about it later
    - Might be worthwhile to consider 6 layer board - Mark
- Do we want to make enclosure? ESD is concern, especially for transport
- Specify what you are measuring for test - histogram and graph
    - Measure temperature during test
- What is our plan for getting temperature and what other metrics are we getting during test?
    - Adding temperature
    - Current
    - voltage
    - humidity
    - pressure
    - Can get a single chip to measure environment - temperature, pressure, humidity
    - How different is our test environment from its operating environment - in atmosphere versus space
    - Is there a way the measure voltage and current for select components? - I^2C part where you can measure voltage form current
    - Understanding what were doing will allow us to understand why we got the outputs we did
- Want to hook it to a frequency counter and capture data for a high period of time
    - might need to rent one
    - want a high precision one
- Banana plugs versus screwing wires in - want to eliminiate any drop since it'll be sitting there for a long time
- Show startup process - compare steady state to what it was looking like when it started
- Deliver allen deviation plot as well for time card
- RJ minimum (statistical), timeframe (window) for measuring RJ
    - there will be requirement for jitter and scew that they will see on their end
- When building loop filter how will test what it is actually doing? How do we prove that it is doing what it is intended to do?
    - should be built into the design to some capacity
    - need to be able to hijack oscillator
        - what if oscipator in oepration condition far form normal, what do you do from that?
    - usually intermediate processing withinoclock itself on board
    - can change the way the reference clock appear by hijacking it
    - inject noise on output of the DAQ
    - want ocntorl system to be able to compensate for those

        - if dont test can;t tell if loop filter has bandwidth for that
    - if can do fft on board
    - should be able to collect measurements nad send back for analysis
    - all operating conditions need to be monitored