Identify at least three feasibility questions for your team to answer. One each that can be answered by:

- Analysis
- Benchmarking
- Prototyping

Submissions should be in pdf format

***Luke:***

**Analysis:**

Q. How can we make sure everything is connected to where it needs to be?

A .Using a multimeter and checking the continuity of each connection to where it should land.

Q. How can we test signals on the PCB?

A. When designing the PCB placing test points all over the board on different connections to ensure that the signals being produced are correct.

**Benchmarking**:

Q. How can we measure the clock signal being generated?

A. Connecting an Oscilloscope to the clock output signal.

**Prototyping:**

Q. How can we connect the FPGA or SOC to the PCIe lane?

A. By either getting or making a PCIe breakout board, or by taking a connector and inverting the connections to make direct connections.

***Eva Czukkermann***

**Analysis**

Question: How do we know the structure will be able to withstand conditions in space and adhere to the given specifications?
Answer: Once a 3D model is procured, use Ansys to run an environmental simulation (vibe and shock) to ensure the structure can withstand the stresses caused by the environment.

**Benchmarking**

Question: What is the maximum power the system should be consuming?
Answer: Competitors' products typically consume approximately 10W maximum. As a result, the maximum power consumption for the system should be set at 10W.

**Prototyping**

Question: How can we determine that the components will not overheat when operating within the system?
Answer: Run each component at a higher power consumption/production rate than what it will experience in the system. Measure the temperature output as well as test its performance capabilities at the advanced level to ensure it can operate properly. If it can operate properly and not overheat in that environment, it can operate within the system.

***Nsadhu Muyinda***

**Analysis**

Question: How will errors be detected and corrected?
Answer: Errors can be detected using mechanisms like parity bits or error-correcting code(ECC) which detects and corrects errors.

**Benchmarking**

Question: How can the latency between FPGA and microcontroller be determined over SPI, $I^2C$, or UART?
Answer: Use a logic analyzer to measure the timing signals and calculate the latency.

**Prototyping**

Question: How can we verify that the FPGA is functioning properly with the microcontroller?

Answer: By using an oscilloscope or logic analyzer to check signals and data communication.

***Drew Schacke***

**Analysis**

Question: On the system level of this card we will have forms of programmable logic, a processing system, oscillator, voltage/power regulation, and communication driver and auxiliary circuitry, how will we segregate and ensure cross-talk is valid yet never intruding?

Answer: Through the power of system design, we can delegate individuals to design and test portions and come together with a system integration engineer to first understand aspects of all systems and then creatively source a solution to layout on PCB all described aspects.

**Benchmarking**

Question: After the completion of the prototype design we have reached the point of benchmarking, what aspects and tests will be run to validate this design?

Answer: Per client specification, we are to produce a working system that *can* be placed under rigorous testing due to space travel. To prepare for this we have contacts in the SPEX who have access to vibe-tables and other simulation devices. Additionally, we can compile and track precision as a function of time to display and characterize the final time-keeping system.

**Prototyping**

Question: The most important aspect of this project is to keep time, how will we calibrate and verify the precision desired is reached?

Answer: Through complex verification analysis a testbench can be created to *smartly* test our precision for a simulated duration of time.

***Tanner Smith***

**Analysis**

Question: How will we implement security systems in order to prevent threats such as spoofing, jamming, and DDoS.

Answer: Hopefully perform ‘long run holdover to protect against jamming. DDoS will require more attention external to the timecard. As for spoofing, a higher quality GNSS receiver may be required to verify packet signature.

**Benchmarking**

Question: How do we verify board functionality and connectivity, as well as power requirements?

Answer: Upon receiving an initial PCB, each feature of the board should be tested. As far as power requirements go, average usage should be calculated through the use of stress tests.

**Prototyping**

Question: How do we verify functionality and features when compared to ‘competitors’ / similar products (Safran and Meta cards)?

Answer: Try to include most of the pre-existing features such as the multiple interfaces (GNSS SMA, IRIG-B, DCF77).