

System Level Design: Phase-End Summary

Team Vision for System Level Design Phase:

As a team, our main goals for the system level design phase was to identify the key functions of the time card. Through the use of functional decomposition we were able to parse through functionalities that are required and generate initial concepts in order to achieve mentioned functions.

Overall, the functional decomposition allowed us to identify required functions and risks. As well as shorten the list for required standards, documentation. This allowed for a greater understanding as a team how we are going to solve the outstanding issues, and whether our goals are feasible.

Problem Statement Redefined:

The current ready-to-use space-qualified precision timekeeping devices available cost hundreds to millions of dollars.

The goal of this project is to design and build a derivative FPGA(Field Programmable Gate Array) Time Card. The timekeeping drift must be less than 30 nanoseconds per Earth day. It must be compatible with CubeSats and its standards, compatible with existing spacecraft, and able to communicate with existing time networks.

This low-cost alternative must have comparable performance under \$10k. Operational characteristics will be compliant with NASA LunaNet Standard, and its size, weight, and power characteristics will be compatible with a 12U CubeSat or smaller. There shall be minimal error when synchronizing on-board time and when synchronizing with other systems' times. The precision clock must survive deep space conditions for at least 10 years.

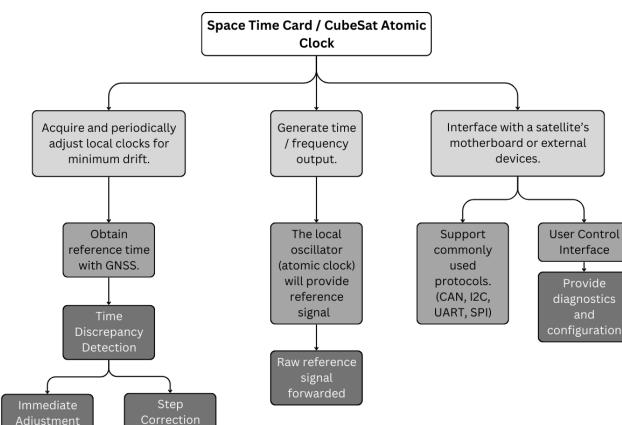
Functional Decomposition:

The main function of this timecard, simply put, is to keep the time. The additional functions all revolve around communication with external elements or input.

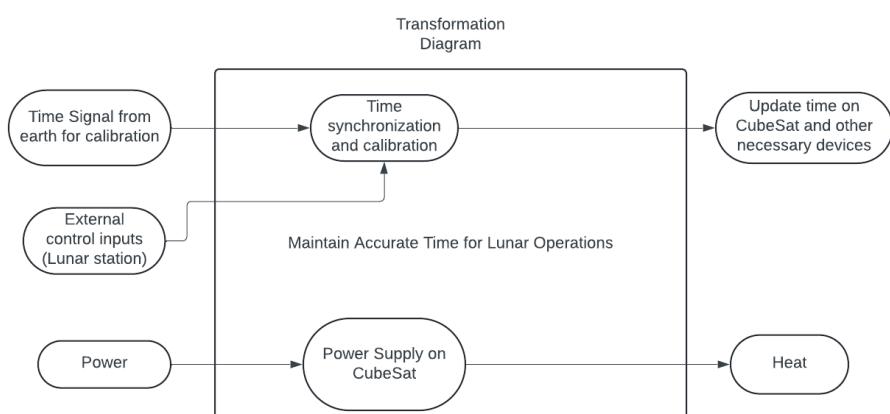
The various functions of the card are listed below:

- Acquire and periodically adjust local clocks to minimize drift.
- Including ‘hold-over’ functionality, local systems should be able to rely on the frequency signals provided for a long (weeks) period of time.
- Various protocol support to interface with a satellite’s motherboard or external devices.
- Initially, GNSS support was included, after some conversation, we decided that if possible and time allows, GNSS support will be continued.
- Time discrepancy detection including immediate adjustments and step corrections.

Function Tree:

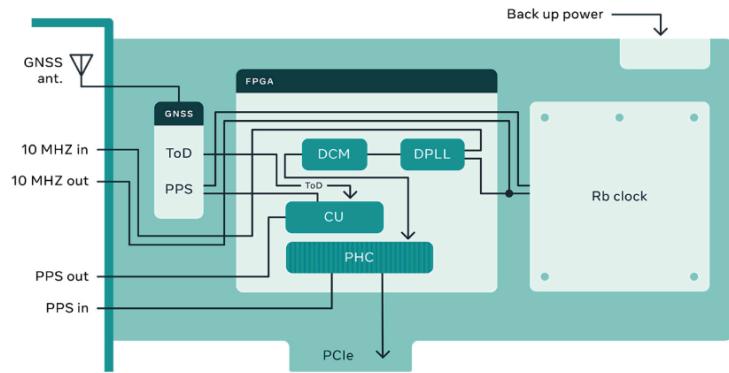


Transformation Diagram:



Functional Benchmarking:

Open Timeserver Timecard



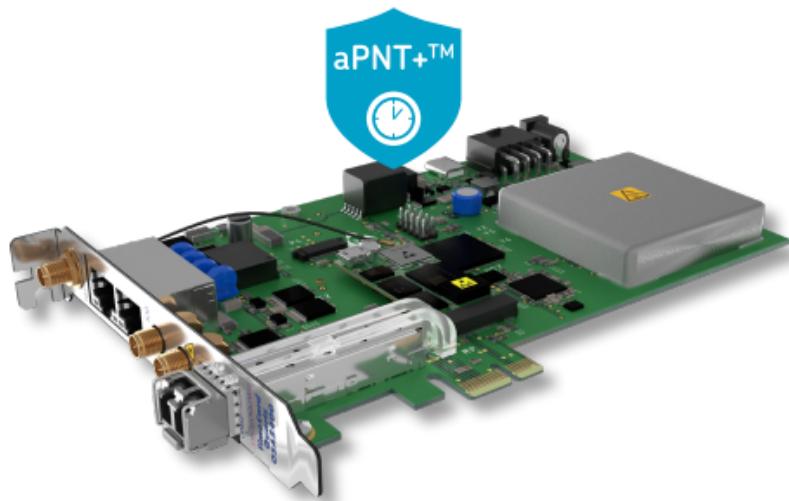
This is an open source timecard developed by a team at Meta, and it is our main reference as a competitor product.

Features:

- On-board Global Navigation Satellite System (GNSS) communications
- Miniature Rubidium Atomic Clock
- PCIe Interface
 - < 200 ns drift per earth day (likely improved by Phase Locked Loop (PLL) circuit)
- Synchronizes clock using Pulse Per Second (PPS) or 10MHz

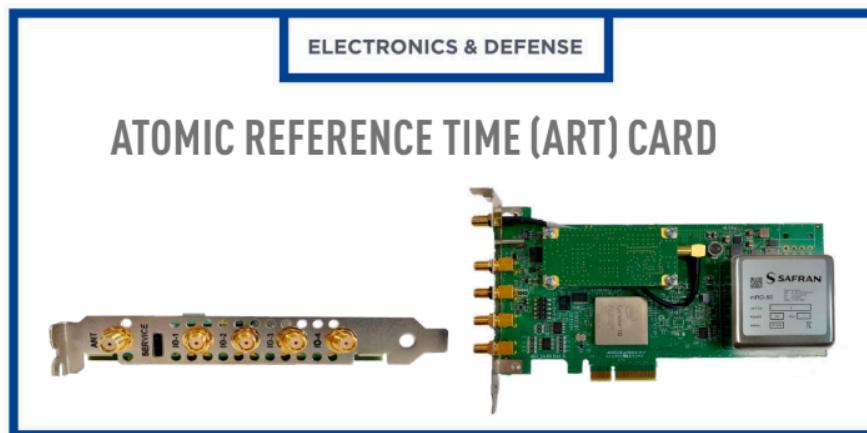
OSA 5400 Timecard

22257: Space Time Card



- On-board GNSS communications
- Rubidium or Oven-Controlled Crystal Oscillator (OCXO)
- PCIe Interface
 - Can show up as Physical Hardware Clock (PHC) or PPS device
- Remote management with SSH/Telnet/SNMP
- Can use PPS or Precision Timing Protocol (PTP) for synchronizing
- ITU-T G.8272 Class A Primary Reference Timing Clock (PRTC)
 - ±100ns from UTC

Safran mR0-50



- PCIe Interface
- Onboard GNSS
- PPS and 10MHz, future support for PTP
- 2us drift per Earth day

22257: Space Time Card

Product Name	Holdover Drift	Sync Protocol	Interface	Size	GNSS compatibility	Temp Range	Max power consumption	Oscillator Type	Communication Protocol
Ours	<30 nsec / earth day	PPS / 10MHz	Single Lane or double*	12U	GNSS Not Onboard	0-70 C	5W	OCXO	CAN (subject to change)
Safran ART time card	< 2us / earth day	PPS / 10MHz, PTP in future	PCIe 2.0 x 4	169.7mm x 86.4mm	GNSS L1/L2 or L1/L5 reception	-10°C to +60°C	Not Advertised	Rubidium (mR0-50)	USB-UART
OSA 5400 Timecard	±100ns from UTC	PTP or PPS	PCIe	111.15 mm x 14.47mm	GNSS L1/L2/L5	0°C to 70°C	Quartz HQ++: 10.5W (typical), 18.5W (max.)	OCXO or Rubidium	Proprietary
Open Timecard	Not advertised, just clock < 200ns drift	PPS	PCIe	Not Specified	GNSS L1/L2/L5	Not specified	Not specified	Rubidium	Not Specified

Concept Development:

Timekeeping:

Primary goal of the project is to develop a precise time keeping card for use in space applications. To do this we need a high precision clocking device.

Options:

- 1 - mRO-50
- 2 - SiT5801
- 3 - SiT5802
- 4 - SiT5356

Mechanical Communication Fixture:

Our time card will communicate via a server onboard the CubeSat which further provides communication between earth and other satellites. Our card needs a mechanical connection to the server to provide necessary data packets.

Options:

- 1 - PCIe
- 2 - USB
- 3 - RS232

Communication Protocol:

To provide the data communication a protocol is necessary to communicate to the server and receive information back.

Options:

- 1 - I²C
- 2 - SPI
- 3 - UART
- 4 - CAN
- 5 - USB

Programmable Logic:

Digital logic is necessary to create the Time Engine which will analyze and process a high precision clocking device to create a functionally sound timekeeping card down to a 30ns drift per earth day.

Options:

- 1 - MicroZed 7Z010 (PLA-FPGA)
- 2 - AC7Z035B (Zynq SoC)
- 3 - AC7100B (Pure FPGA)

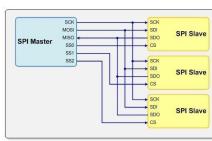
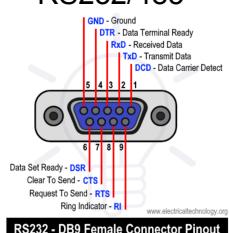
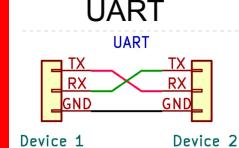
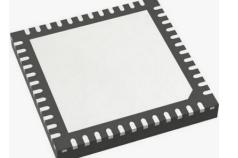
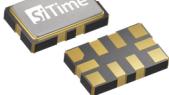
Processing:

A simple processing system will provide ease to provide simple algorithms for port buffering, time analysis, and data communication.

Options:

- 1 - MicroZed 7Z010 (Dual Core ARM)
- 2 - AC7Z035B (Zynq SoC)
- 3 - MSP430FR5969-SP (microcontroller)
- 4 - STM32WBA52CG (microcontroller)

Morphological Chart and System Concept Generation:

Method of Timekeeping	Method of Communication	Communication Protocol	Programmable Logic	Processing System
mRO-50 	PCIe 	I ² C 	MicroZed 7Z010 	MicroZed 7Z010 
SiT5801 	USB 	SPI 	AC7100B (Just FPGA) 	MSP430FR5969-SP 
SiT5802 	RS232/485 	UART 	AC7Z035B (SoC ARM-PS/PLA-F PGA) 	STM32WBA52CG 
SiT5356 		CAN 		AC7Z035B (SoC ARM-PS/PLA-F PGA) 
SiT5346 		Ethernet 		

SiT5356AI-FQ033IT-10.000000

Revised August 2024

SiT5356AI-FQ133IT-10.000000**SiT5356AI-FQ233IT-10.000000**

The SiT5356 is a 60 MHz oscillator designed with a 0 PPM pull range, reducing frequency drift. It costs approximately \$60 when purchased individually. For higher precision needs, the military-grade variant, SiT5346, provides superior accuracy but comes at a much higher cost of around \$400.

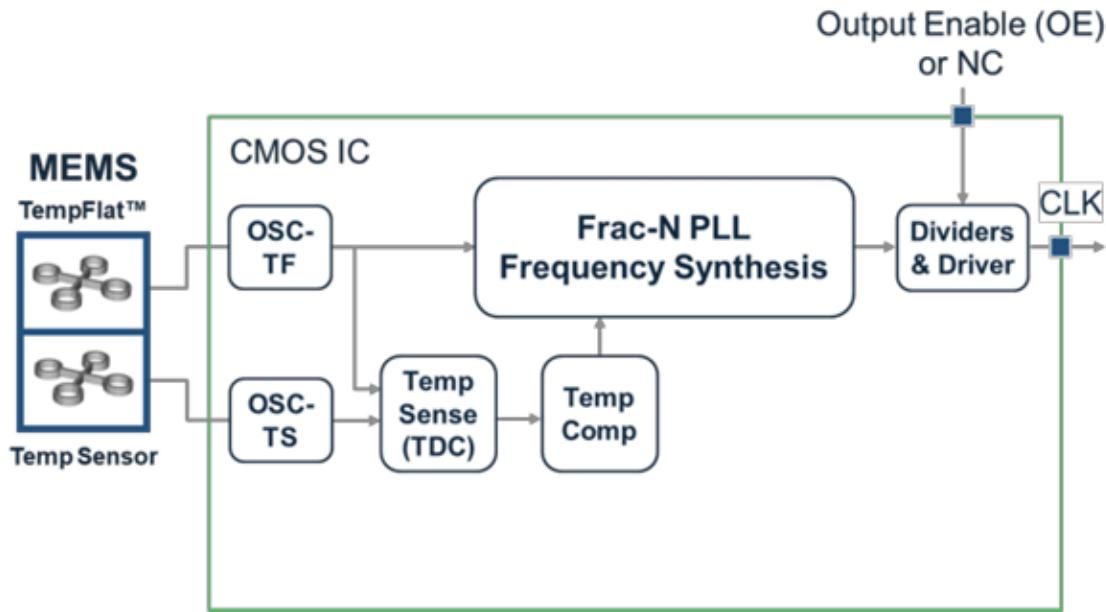


Figure 46. Block Diagram – TCXO

TCXO Configuration

The TCXO generates a fixed frequency output, as shown in [Figure 46](#). The frequency is specified by the user in the frequency field of the device ordering code and then factory programmed. Other factory programmable options include supply voltage, output types (LVCMOS or clipped sinewave), and pin 1 functionality (OE or NC).

While PCIe is not commonly available on most motherboards, RS232 remains widely used. Communication between systems can be facilitated using a CAN

The **MicroZed** platform was selected due to its cost-effective SoC from the Zynq family, which includes a Dual-Core ARM processing system (PS) and a programmable logic array (FPGA fabric). Familiarity with the platform and the availability of US-based suppliers were additional factors in the decision.

Updated Project Overview:

Work Breakdown Structure Link: [Work Breakdown Structure](#)

Objectives

1. Long Term:
 - a. Create a fully functional precision clock time card.
 - i. Has a timekeeping drift of less than 30 nanoseconds.
 - ii. Compatible with existing space craft motherboards and external devices.
 - b. Develop GNSS communication.
 - c. Develop a testbench to test clock and communication functionality.
2. Short Term:
 - a. Continue to select materials/development kits to assist with the preliminary prototype development.
 - b. Develop an initial BOM (Bill of materials).
 - c. Begin development of a prototype with pre-identified materials, and review availability and costs.
 - d. Review previously identified risks and concepts.

The tasks and objectives described above can also be found within the linked Gantt chart below, some notes on the Gantt chart are also included:

Gantt Chart Link: [!\[\]\(9c4f697052545ae4fab36076e03db94f_img.jpg\) Gantt chart](#)

Gantt Chart Notes:

- PCIe offers a secure connection but we could not find 12U boards that supported it.
- USB is simpler to implement but it does not offer a secure connection.
- RS232 offers a secure connection and is simple to implement.

We communicate with our customers and guide via email and Slack. We communicate with each other via text messages.

Phase-appropriate feasibility: analysis, prototyping, and/or benchmarking of critical technology:

Form of communication between the timecard and the 12U cubesat.

- PCIe is an industry standard but many of the 12U boards we researched did not have PCIe. However if chosen, the team would need to purchase or make a PCIe breakout board. PCIe also offers a secure connection to the server which other communication methods do not.
- USB is an alternative but unlike PCIe does not offer a secure connection to the server. On the other hand it is simpler to implement communication protocols for.
- RS232 is a mechanical connection fixture that offers a secure connection and can be integrated with multiple different communication protocols. On the other hand, RS232 is outdated and poses challenges implementing some communication protocols like ethernet.

Determine whether to use an FPGA and microcontroller or a SOC(System on Chip)

- Using an FPGA with a microcontroller would be more cost effective however, creating a PCB to integrate them together would pose its own set of challenges.
- A SOC would be simpler to work with eliminating the problems that come with working with an FPGA and microcontroller. However, a SOC is much more expensive.

Determine whether the timecard will have GNSS.

- GNSS would be used to communicate with a server. However, that would add to functionality that would need to be designed.
- Excluding GNSS would allow the team to focus on designing a properly functioning timecard leaving GNSS and other functionality to other components on the 12U cubesat.

Concept Evaluation & Selection:

Method of Timekeeping	Weight	Default Choice	SiT5356	SiT5801	SiT5802	mRO-50	SiT5346
Frequency	1	0	0	0	1	0	0
Operating Temperature Range	1	0	0	0	0	0	0
Frequency Stability	1	0	0	1	1	1	0
Cost	3	0	0	-3	-3	-1	-1
Pull Range (ppm)	1	0	0	0	0	0	1
Phase Jitter (rms)	1	0	0	0	0	0	0
Totals		0	0	-8	-7	-2	-2

Method of Communication	Weight	Default Choice	RS232	USB	PCIe
Cost	1	0	0	0	0
Complexity	1	0	0	-1	-1
Strength of connection	1	0	0	-1	1
Testability	1	0	0	-1	-1
Integration	1	0	0	1	-1
Totals		0	0	-2	-2

Communication Protocol	Weight	Default Choice	UART	I2C	SPI	CAN	Automotive Ethernet
Ease of Implementation	1	0	0	0	0	-1	-1
Real-Time Capability	1	0	0	0	0	1	1
Reliability	1	0	0	0	0	1	1
Efficiency	1	0	0	1	1	1	1
Error Detection	3	0	0	0	0	1	1
Modularity & Flexibility	1	0	0	1	1	1	0
Cost	1	0	0	0	0	-1	-1
Sensitivity	3	0	0	0	0	1	1
Totals		0	0	2	2	8	7

22257: Space Time Card

Programmable Logic	Weight	Default Choice	MicroZed 7Z010	AC7100B (Just FPGA)	AC7Z035B (SoC ARM-PS/PLA-FPGA)
Cost	1	0	0	1	-1
Works in space	3	0	0	-1	-1
I/O	1	0	0	0	0
Logic Cells	1	0	0	0	0
Memory	1	0	0	0	1
Totals		0	0	-2	-3

Processing	Weight	Default Choice	MicroZed 7Z010	MSP430FR5969-SP	STM32WBA52CG	AC7Z035B (SoC ARM-PS/PLA-FPGA)
Cost	3	0	0	-1	0	-1
I/O	1	0	0	-1	-1	0
Long life	1	0	0	1	0	0
FRAM	1	0	0	1	0	0
Complexity	1	0	0	0	0	0
Totals		0	0	-2	-1	-3

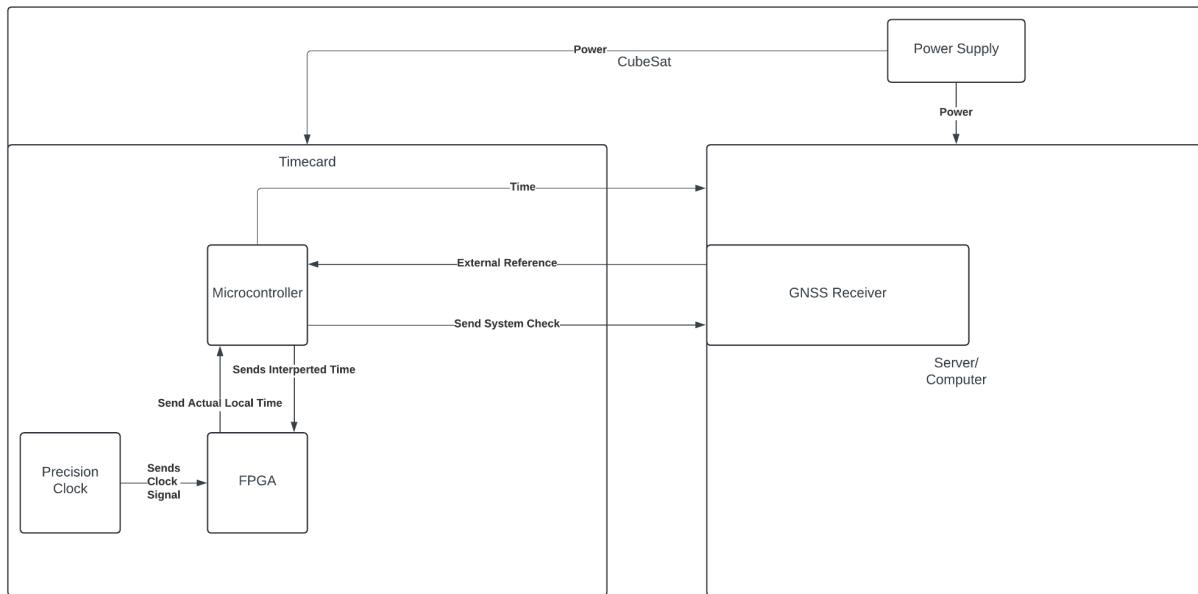
Using Pugh charts, we were able to make a more informed decision for our design by evaluating it against customer requirements, engineering requirements, and constraints. The initial choice was selected as a baseline based on preliminary research, and we compared competing products against it using specific criteria. From the charts, we concluded that the SiT5356 would be the best choice for our clock. Although the SiT5346, commonly used in modern space applications, offers higher precision, the SiT5356 provides a more cost-effective alternative while maintaining sufficient accuracy. Additionally, both chips use the same footprint, allowing for the SiT5346 to be easily swapped in if needed.

For communication methods, we chose RS232 because it is widely compatible with most hardware and offers robust communication protocols capable of handling the interference present in space environments. We will be using the CAN protocol, which pairs well with RS232, providing error checking and high noise resistance.

Regarding programmable logic, we selected the MicroZed 7Z010. It offers multiple output options and includes a microcontroller, simplifying the design and implementation of an FPGA-based system. While we considered radiation-hardened microcontrollers for extended multi-year missions, they were significantly more expensive and lacked the performance of consumer-grade electronics.

System Architecture:

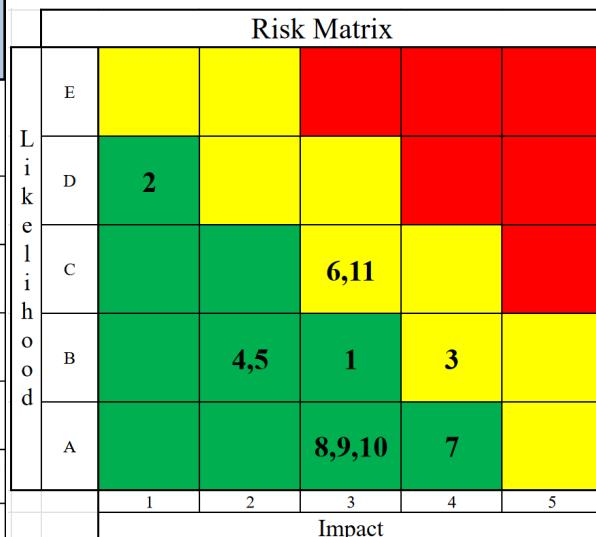
This diagram represents the general system architecture of the time card. The primary objective is for the FPGA to receive a clock signal from a precision clock. The microcontroller interfaces with the GNSS receiver, located on the main computer, to obtain a reference time. The FPGA and microcontroller communicate to maintain a synchronized current time, which is then reported back to the main server or computer.



Risk Assessment:

ID	IF Statement	THEN Statement	Cause	Likelihood	Cost Impact	Schedule Impact	Importance	Action to Minimize Risk
1	IF timecard is exposed to higher EMI than expected	THEN received data will become corrupted/incorrect	Strong electromagnetic fields and RF from other satellites	B	2	3	B3	Provide error flag and power cycle device
2	IF communication protocol experiences bit flip and interference	THEN stored data will become corrupted/incorrect	Cosmic Rays	D	1	1	D1	Force development to parity and error detection schemes in firmware for all communications
3	IF open source programs do not work as described	THEN design is set behind due to designing additional programs/functions/blocks	Unpredicted Factors	B	3	4	B4	Our team will produce our own open source programs for any of those which do not work as described
4	IF vacuum causes solderpoints to flake and cause shorts	THEN a high current flow (short) can occur, causing component damage	Material Science Factors	B	2	2	B2	Utilize Sn62Pb37 solder rather than lead-free (tin) solder
5	IF vacuum causes PCB to outgas	THEN surrounding components and systems experience unexpected debris which may lead to opens/shorts	Material Science Factors	B	2	2	B2	Place PCBs through vaccum cycles prior to using
6	IF cubesat vibrates more than design specifications	THEN connection would be lost between the timecard and motherboard	Rough Launch, Space Debris Collision	B	2	3	B3	Develop option to mechanically strengthen the electrical connectors
7	IF the timecard loses power	THEN the oscillator and all other components will not function	CubeSat loses power	A	3	4	A4	No resolution, other than power cycle once CubeSat regains power
8	IF Displacement Damage Dose occurs	THEN non-ionizing energy loss occurs causing device and/or component degradation	Energy deposition by impinging radiation	A	3	3	A3	If CubeSat is not protected, develop protection barrier
9	IF Single Event Effects (Single Event Latch Up) occur	THEN communication packets will contain incorrect data	Singular, stray, energetic particles	A	3	3	A3	If CubeSat is not protected, develop protection barrier. Can additional implement stronger parity detection and schemes
10	IF Atomic Oxidation occurs	THEN electrical connection including solder points may lose conductivity	Presence of strong oxidizing agents	A	3	3	A3	If CubeSat is not protected, develop protection barrier
11	IF parts have lead times over a month	THEN parts may not be in hand when required to prototype	Supply/Demand	C	2	3	C3	Order significantly early than expected, if not possible, look for other vendors or options.

ID	IF Statement	THEN Statement
1	IF timecard is exposed to higher EMI than expected	THEN received data will become corrupted/incorrect
2	IF communication protocol experiences bit flip and interference	THEN stored data will become corrupted/incorrect
3	IF open source programs do not work as described	THEN design is set behind due to designing additional programs/functions/blocks
4	IF vacuum causes solderpoints to flake and cause shorts	THEN a high current flow (short) can occur, causing component damage
5	IF vacuum causes PCB to outgas	THEN surrounding components and systems experience unexpected debris which may lead to opens/shorts
6	IF cubesat vibrates more than design specifications	THEN connection would be lost between the timecard and motherboard
7	IF the timecard loses power	THEN the oscillator and all other components will not function
8	IF Displacement Damage Dose occurs	THEN non-ionizing energy loss occurs causing device and/or component degradation
9	IF Single Event Effects (Single Event Latch Up) occur	THEN communication packets will contain incorrect data
10	IF Atomic Oxidation occurs	THEN electrical connection including solder points may lose conductivity
11	IF parts have lead times over a month	THEN parts may not be in hand when required to prototype



Solution Statement - Expected Project Outcomes:

The end result of this project is a functioning prototype of a derivative Time Card, containing an FPGA. This Time Card will independently maintain accuracy over time with the timekeeping drift not exceeding 30 nanoseconds. The product will be compatible with existing spacecraft systems, including CubeSats and its standards and able to communicate with existing time networks.

Open Items:

- Obtain details about development equipment from Spex
- Contact Safran and Meta about power requirements

Design Review Materials:

Pre-Read: [Presentation](#) and [Summary Report](#)

Presenters: Eva Czukkermann, Ian Dolfi, Nsadhu Muyinda, Drew Schacke, Luke Schrom, Tanner Smith

Notes from Review: [Document](#) (see snippet below)

Agenda and discussion notes

Time	Item	Who	Notes
65 min	Design Review Presentation	All team members	<ul style="list-style-type: none">- Need to form BOM with lead times and get approval to purchase components with long lead times ASAP (SA45 has lead time of 4/15 at the earliest)- Use PTP and CAN- Add lead times in risk assessment<ul style="list-style-type: none">- Ashley said design risk, not project risk so don't need to include in chart (asked Dr. McCauley 10/17/24)- Leo orbit is goal, tech demo is in geo orbit
5 min	Questions/Discussion	All	<ul style="list-style-type: none">- Don't let price limit what we consider - see if it would be worth spending the money- Focus on timekeeping for prototype- Identify environmental risks and modify them as best as we can- Good job incorporating feedback- Allan deviation is good way to represent clock drift over different timescales

Issues Raised

Revised August 2024

22257: Space Time Card

- PTP and CAN
- Lead times
- Is it worth spending more money to get better quality?

Decisions Made

- None

Action items

- Decide what we need to buy, form BOM, and get approval to purchase components from client ASAP - some components have long lead times and November is coming fast [Drew, 10/24/2024]
- Displacement Damage Dose - need to contact SPEX and see what info they have, if they have nothing contact Philip [2:00PM 10/19/24, Tanner (Possibly) and Luke].
- SA45 - research - <https://www.microchip.com/en-us/product/csac-sa45s> [Tanner, 10/22/24]
- CSAC 0090-03240-003 ships by 10/21 - research - <https://www.microchip.com/en-us/product/CSAC-SA45S> [All, 10/17/24]
- Add the higher priced oscillators to chart to see if spending the money would be worth it - could find more funding [Luke, 10/22/24]
- Luke will make MATLAB model for CubeSat if he has time between classes [Luke, 11/1/2024]
- Add lead time to risk assessment [Drew, 10/17/24]
 - In talking with Dr. McCauley, Ashley is correct that normally it wouldn't be included as a risk but due to the tight timeframe of our project with no option for an extension it is a risk.

Supporting Documentation:

[Gantt Chart](#)

[Initial Concept Generation](#)

[Morphological Chart](#)

[Pugh Chart](#)

[Risk Management](#)

[Standards](#)

[Work Breakdown Structure](#)

Goals for next phase:

Within the next phase we plan to start preliminary prototyping to prove the functionality of our solutions presented within the concept generation and functionality sections. This includes revised component selections, the development of a BOM, development kits, and testbenches. As well as furnishing risks and feedback from this phase review.

Link to Gantt chart: [!\[\]\(3cf084882489248c66b41ee5d191c91e_img.jpg\) Gantt chart](#)

Personal goals are described below:

Eva Czukkermann:

- Complete all the non-technical aspects of the assignments to make it easier for the team to add the technical aspects that I do not understand.
- Ensure the team is keeping track of feedback received from our client and guide. This includes taking detailed notes during every meeting.

Drew Schacke:

- Apply knowledge from graduate research in areas including high-level computational digital systems and their implementations. (Digital Design complete by Christmas Break)
- Purchase evaluation boards to begin design development (by week 9)
- Bibliographic research for further applications of a space-rated precision TimeCard allows for further understanding of the importance of this design for all team members. (May 2025)

Ian Dolfi:

- Prototype synchronization with GNSS development board
- Characterize time synch path delays and errors

Luke Schrom:

- Testbench
- Assist with design.

Nsadhu Muyinda:

- Assist with the digital design of the FPGA/SOC.

Tanner Smith:

- Assist with the development of the preliminary BOM.
- Assist with PCB and electrical design characteristics.