Preliminary Detailed Design: Phase-End Summary

This document should continue to document your journey through MSD, so include work-in-progress as well as latest results – this document can be edited live online. Any time you post a snapshot of a document for a phase review, be sure you have a live document to back it up. **Your file repository should still contain original editable files, not just .pdf files**.

Use the Phase 3 folder to store information supporting this document. Some templates are available in this folder for your use.

Remove all template text from this page prior to your Week 10/11 Preliminary Detailed Level Design Review.

Individual and Team Vision for Preliminary Detailed Design Phase [Tanner]

- What did your team plan to do during this phase?
- What did your team actually accomplish during this phase?
- Since this phase will require students to do more independent work, your team should also capture a summary of key tasks completed, and who was responsible.

****Team plan for this phase:**

We planned to start preliminary prototyping in order to prove functionality of our proposed solution that we presented previously. This includes revising component selections, development of a BOM, proposing development kits, testbenches, and ordering long lead time items.

**** Accomplished during this phase:**

We started producing the preliminary BOM, researching the functionality of the timecard through MATLAB, researching hold over drift characteristics of proposed CSAC and inserting other clocks, as well as inserting ordered items here.

Feasibility: Analysis, Simulations [Team]

Goals

- Justify that the design decisions you are making will result in an acceptable solution.

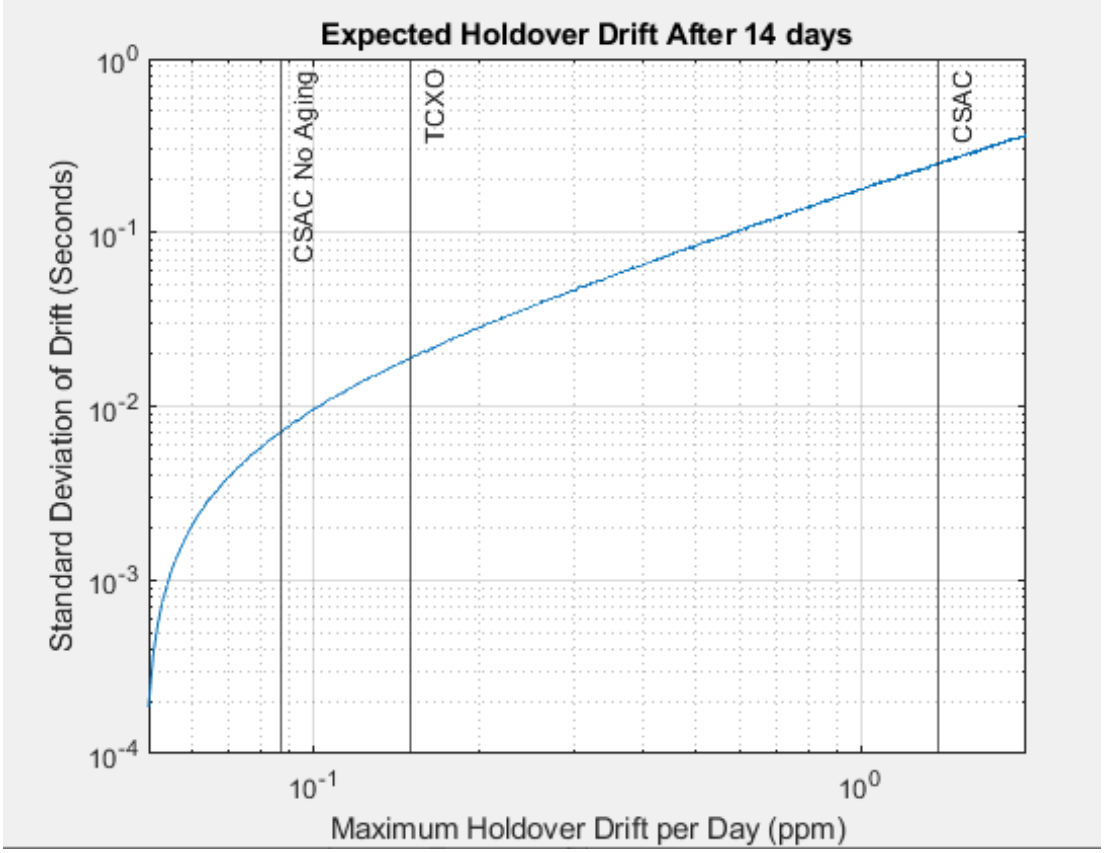
Instructions

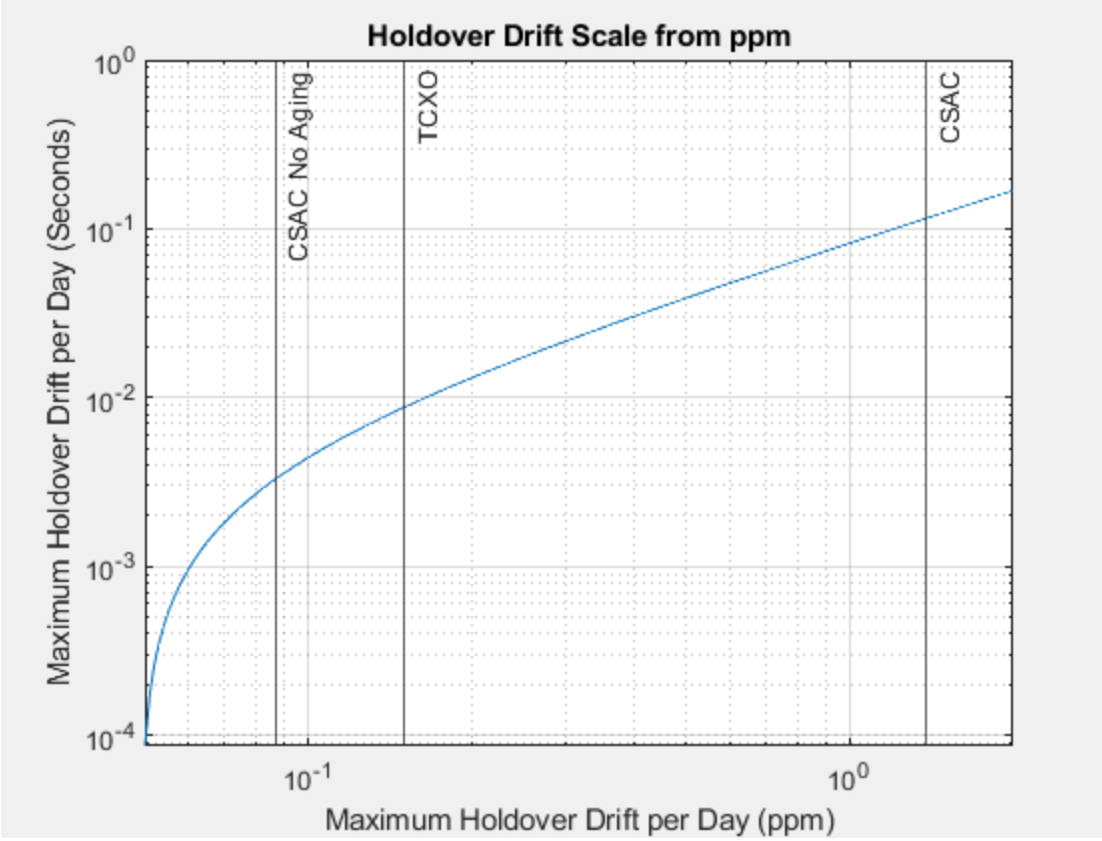
1. Complete various analysis and simulation exercises, especially of critical subsystems. This could include ballpark estimates, and first order analysis.
2. Identify system "transfer function" based inputs, outputs, and key design parameters. This can be done via theoretical analysis or empirical prototyping. It's often helpful to work with multiple members to make sure each subsystem is accurate.
3. Using all of your analyses and models, determine values of all quantitative design parameters. These could be specific values and/or acceptable ranges.

4. Confirm that the selected concepts and design plans will be able to achieve the desired performance of your system. Also anticipate any potential failure modes associated with your chosen concepts.

Required Artifacts

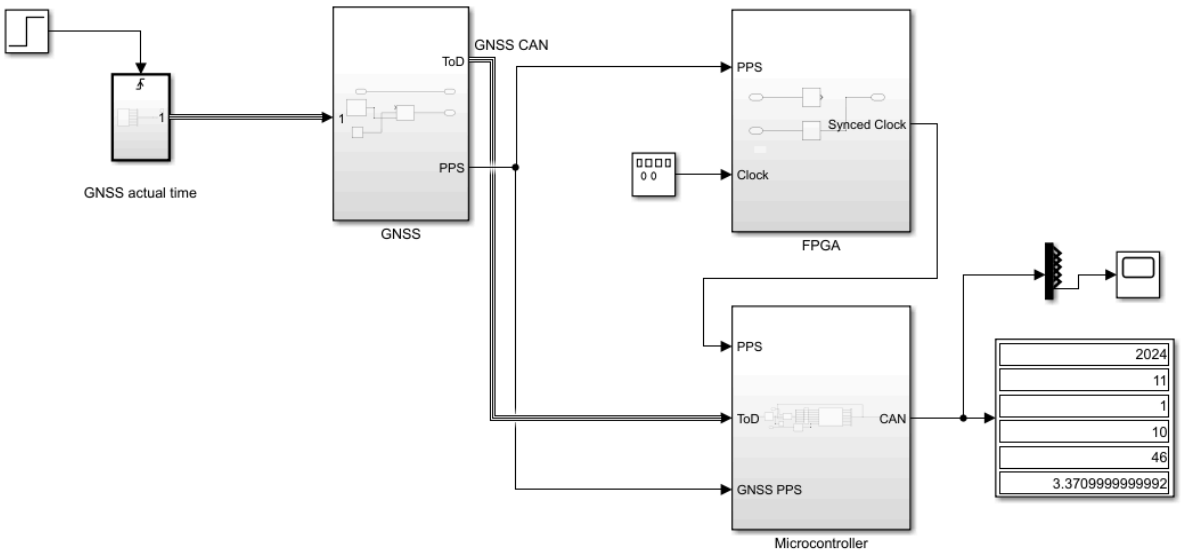
- Document listing your quantitative Design Parameters, including quantitative targets and acceptable tolerances.
- Evidence of your feasibility work, including write ups of any theoretical analysis, and/or photos and videos of your simulations
- Summarize what you learned for each feasibility activity, and what decisions were made as a result.



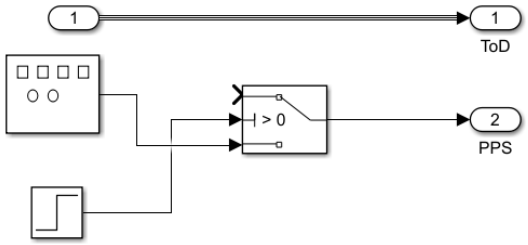


Feasibility: Prototyping [Luke]

The goal is to create a model that emulates the Cubesat Timecard. The model has 3 major parts to it, the FPGA, Microcontroller, and GNSS. Each other these parts are not fully flushed out models instead they are quick approximations of what is happening in each system.

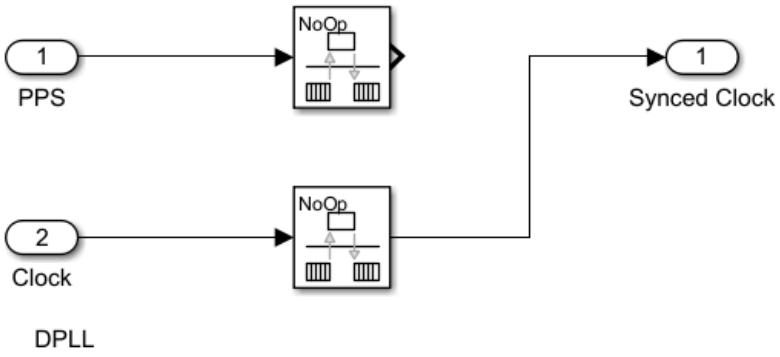


The model takes a GNSS input signal, this signal has two pieces of information that is necessary for what the time card is trying to do. The Pulse per second (PPS), and Time of Day (ToD). The function on the right grabs the time of day that is currently happening. On the left is the PPS signal that is being received.

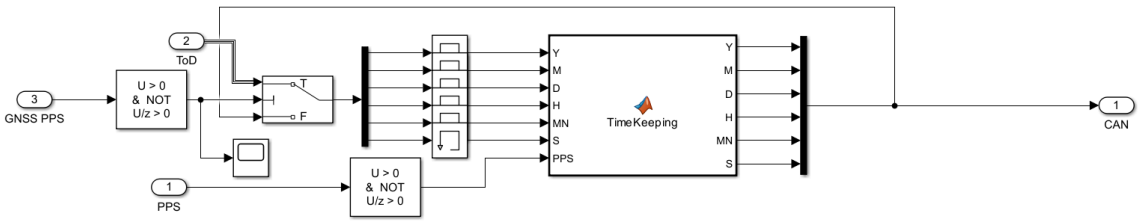



```
function [Y, M, D, H, MN, S] = fcn()
    eml.extrinsic('now');
    eml.extrinsic('datevec');
    Y = 0;
    M = 0;
    D = 0;
    H = 0;
    MN = 0;
    S = 0;
    [Y, M, D, H, MN, S] = datevec(now);
end
```

Once the signal is received then the PPS and ToD is used until disconnected. The FPGA then takes the PPS from the GNSS and then syncs the clock that is onboard with that PPS in a Digital Phase Lock Loop (DPLL). This is done with the following system on the FPGA.



This synchronization clock is then used by the microcontroller to manage the time that is being kept. The signal can also be sent back out as an output for any other devices that want a PPS. The Microcontroller takes the ToD from the GNSS and saves it into memory, it will also take in a PPS to then manage the time, incrementing the seconds based on the rising edge of the PPS.

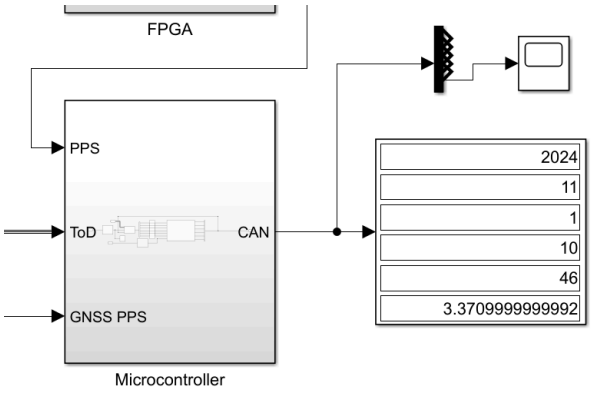


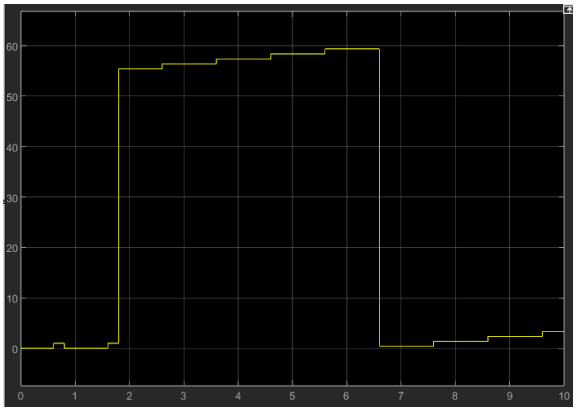
Here is the function that is managing the time keeping.

```
function [Y, M, D, H, MN, S] = TimeKeeping(Y, M, D, H, MN, S, PPS)

    if (PPS == 1)
        S = S + 1;
    end
    if (S > 60)
        S = S- 60;
        MN = MN+1;
    end
    if (MN > 60)
        MN = MN - 60;
        H = H + 1;
    end
    if (H > 24)
        H = H - 24;
        D = D + 1;
    end
    if (D > 30)
        D = D - 30;
        M = M + 1;
    end
    if (M > 12)
        M = M - 12;
        Y = Y+1;
    end
end
```

For simplicity the assumption is made that a month is 30 days, when implemented in the future there will be a lookup table to determine the number of days in each month. The following is a demonstration of the time being managed handling seconds and minutes.





Over the course of 10 seconds the system gets a GNSS signal in the first 2 seconds, then the ToD is stored into the main memory (MM). The system continues the time by incrementing the time

on each rising edge. When the minute threshold is reached it returns seconds to 0 and increments the minute.

Goals

- Quickly test the feasibility of competing options that would be time consuming to simulate
- Quickly evaluate a key but uncertain component or subsystem of your design before making design decisions dependent on that component or subsystem
- Begin fabricating or implementing critical elements of your final product or process

Instructions

1. Identify the functions that are uncertain, which can best be addressed by prototyping
2. Make use of MSD surplus, rapid prototyping, foam core, breadboard, cardboard, wireframe, etc.
3. Consider investing more time and budget into higher-fidelity prototypes
4. Consider purchasing high-risk components

Required Artifacts

- In this document, include
    - what you wanted to learn
    - the limitations of the prototype
    - summarize what you learned
    - explain the decision made as a result
- Photos can be embedded in this document. Videos can be posted in EduSourced.

Drawing, Schematics, Diagrams [Tanner & Nsadhu]

Goals

- Complete a significant portion of the detailed design of your system.

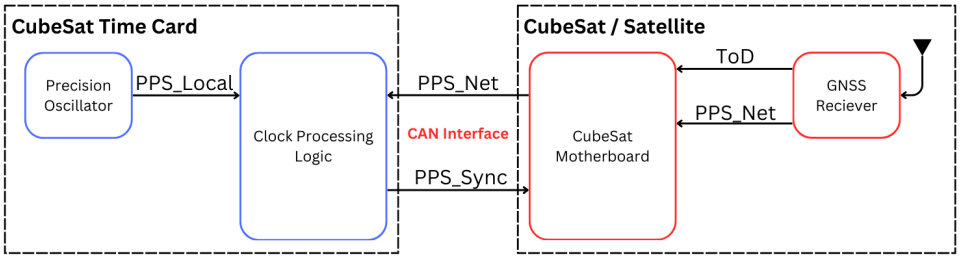
Instructions

1. Define all mechanics of subsystems, including geometries, software design, interfaces, and fabrication instructions for unique parts.
2. Call out all purchased parts
3. Adhere to all required design standards.
4. As with your feasibility analysis, anticipate potential failure modes with your chosen designs.

Required Artifacts

- Complete hierarchy of design files, from system level down to components. This may include (but is not limited to):
    - CAD models/sketches
    - Software design, including specific coding requirements
    - Electrical diagrams
    - Note that your file archive needs to include actual design files, in addition to manufacturing files (e.g., CAD solid model files, plus manufacturing files like drawing files and/or STL files)
    - List of relevant standards, and how your team is satisfying them

High Level System diagram:



Link to Edit:
https://www.canva.com/design/DAGU9_wbepU/g5HjgDUYyRt2cYX66BF65w/edit?utm_content=DAGU9_wbepU&utm_campaign=designshare&utm_medium=link2&utm_source=sharebutton
Public View Link:
https://www.canva.com/design/DAGU9_wbepU/3GgiWLj0Og3cwYhZnoNWGQ/view?utm_content=DAGU9_wbepU&utm_campaign=designshare&utm_medium=link&utm_source=editor

Phase Detector:
Takes two PPS inputs, produces output that is proportional to the phase difference between the two input signals. Traditionally output a pulse width proportional to the phase difference.

Loop Filter:
Reduces noise, improves stability, shapes the transient response, and controls the phase margin. Outputs a VCO control signal, used to tune / adjust the characteristics of the local TCXO / Atomic clock.

SteeringProcess:
Run through this on 11/5/2024 with group… (Im a little confused on how this is implemented).

Divider:
Receives the LVCMOS signal produced from the TCXO / Atomic Clock. Reduces the frequency of the input by a specific ratio. This must be an accurate and precise process.

Phase Lock Loop [PLL]:
Often used for frequency synthesis, clock recovery, and motor controllers. The PLL receives two input signals, identified as the reference and feedback signals. In this case the feedback signal is represented by the locally produced PPS. Similarly, the reference signal is represented by the PPS produced from the GNSS. The difference in phase between the two input signals is extracted through the use of a phase detector. This difference is then fed into a loop filter that produces a correlated value to the phase difference. This in turn gives a variable that can be used to “tune” the local TCXO / Atomic clock, to be in phase with the external network GNSS produced PPS.

Bill of Material (BOM) [Drew (The purchaser)]

Team #:	P22257	Team Name:	Atomic Clock	Budget:	$4,000				
Date:	10/17/2024	Document Owner:	Team Member	Total:	6704.16				
Revision #:	1			Remaining:	-$2,704				

Subsystem	Team Part #	Item	Qty	Unit Cost	Total Cost	Vendor	Website	Ordered	Received
Electrical	00001	AES-Z7MB-7Z010-SOM-I-G/REV-H	2	259.00	518.00	Avnet	https://www.avnet.com/shop/us/products/avnet-engineering-services/aes-z7mb-7z010-som-i-g-rev-h-3074457345644698176/#		
Electrical	00002	Ceramic Capacitor Kit 10pF ~ 10µF	1	48.24	48.24	DigiKey	https://www.digikey.com/en/products/detail/kemet/CER-ENG-KIT-29/5039067		
Electrical	00003	Resistor Kit 1k ~ 9.76k Ohm ±1% 1/10W	1	38.30	38.30	DigiKey	https://www.digikey.com/en/products/detail/stackpole-electronics-inc/KIT-RMCF0603FT-04/2773766		
Electrical	00004	Resistor Kit 10k ~ 97.6k Ohm ±1% 1/10W	1	38.30	38.30	DigiKey	https://www.digikey.com/en/products/detail/stackpole-electronics-inc/KIT-RMCF0603FT-05/2773767		
Electrical	00005	SiT5356AI-FQ233IT-10.000000F	3	68.812	206.44	SiTime	https://www.sitime.com/products/super-tcxo/sit5356#buy-now%20		
Electrical	00006	SiT5356AI-FQ133IT-10.000000F	3	68.812	206.44	SiTime	https://www.sitime.com/products/super-tcxo/sit5356#buy-now%20		
Electrical	00007	SiT5356AI-FQ033IT-10.000000F	3	68.812	206.44	SiTime	https://www.sitime.com/products/super-tcxo/sit5356#buy-now%20		
Electrical	00008	090-03240-003	1	5,377.76	5377.76	MicroChip	https://www.microchip.com/en-us/product/csac-sa45s#document-table		
Electrical	00009	MCP251863T-H/SS	10	2.34	23.40	DigiKey	https://www.digikey.com/en/products/detail/microchip-technology/MCP251863T-H-SS/15985649		
Electrical	00010	SMT Breakout PCB for SOIC-28 or TSSOP-28 - 3 Pack!	1	4.95	4.95	Adafruit	https://www.adafruit.com/product/1208		
Electrical	00011	Large Premium Solderless Breadboard	1	19.95	19.95	Adafruit	https://www.adafruit.com/product/443		
Electrical	00012	Hook-up Wire Spool Set - 22AWG Solid Core - 6 x 25 ft	1	15.95	15.95	Adafruit	https://www.adafruit.com/product/1311		

Required Artifacts

- Draft BOM available in EduSourced, with a snapshot/summary in this document.
- Brief summary of the team's budget status: what assumptions have you made, are you projected to be within budget or not, are there any cost risks, etc?
- If the team is requesting additional budget, include rationale here

Test Plans [Ian & Eva]

Goals

- To create a set of test plans that will demonstrate objectively the degree to which the Engineering Requirements will be satisfied by the either component, subsystem, or system tests.
- To create a set of test plans that will enable you to objectively determine that your components or subsystems are functional and ready for system integration

Instructions

1. Complete test plans specifying the data to be collected, instrumentation to be used, testing procedures and personnel who will conduct the tests.
2. Tests to assess accuracy of feasibility models: Make plans and execute these tests throughout the second half of MSD I
3. Tests to verify that your final subsystems work: Make plans and execute these tests once you start your final prototyping, prior to system integration
4. Tests to verify that your final system satisfies the ERs your team and client agreed to: Generally, you will execute these tests once you start your final system integration
5. Note that tests to verify that you've met a system constraint or delivered a required feature may be fairly trivial. You don't need a detailed test plan to demonstrate that your

prototype budget was <$500 or that your full system weighs less than 20 lb, for example. Discuss with your guide if you're not sure how much detail to include.

6. If your team's testing will involve human subjects, you must review the RIT Human Subjects Research Office "Protecting Human Subjects" page found here: https://www.rit.edu/research/hsro/ for details on securing approval for work with human subjects
7. Look at industry test standards (e.g., ASTM). The RIT library maintains an infoguide with links to standards databases found here: https://infoguides.rit.edu/standards , many of which provide industry-standard test procedures for a variety of components and systems. Cite these if used.

Required Artifacts

- Test Plans (use the “Requirements and Testing.xlsx” template), available in EduSourced. Include an updated version of the document in this phase folder, labeled by phase to distinguish it.
- In this document, include a table that summarizes the degree to which ERs are addressed by your test plans.
- If applicable, an Institute Review Board or Institute Biosafety Committee submission (allow **at least** 30 days for this to be reviewed - more time is ideal, since the IRB or IBC outcome may be a request for you to modify your proposed test protocol)

System Design and Flowcharts/System Block Diagram [Tanner/Drew]

Goals

- Provide a high-level view of elements involved in building and operating your system.

Instructions

1. Continuously update the diagrams from your systems level design documentation.

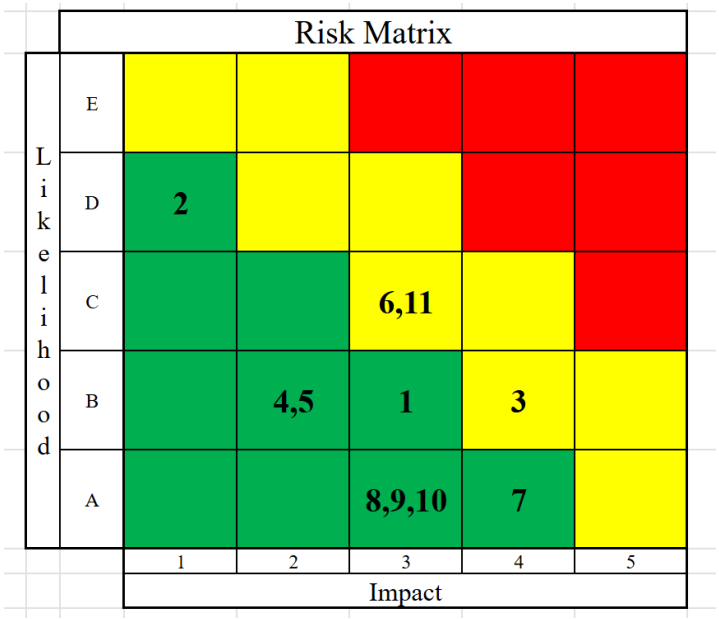
Required Artifacts

- A snapshot of your current system design diagrams
- A link to the live version of your system diagrams, if applicable.
- A brief summary of the current status of the design, based on work done during this phase. Which blocks/functions are complete, which are nearly complete, which still need work?

This is the same as the block diagrams above. I believe the diagrams belong here not above. As above should be more technical such as pinouts and

Risk Assessment [Drew]

ID	IF Statement	THEN Statement	Cause	Likelihood	Cost Impact	Schedule Impact	Importance	Action to Minimize Risk
1	IF timecard is exposed to higher EMI than expected	THEN received data will become corrupted/incorrrect	Strong electromagnetic fields and RF from other satillites	B	2	3	B3	Provide error flag and power cycle device
2	IF communication protocol experiences bit flip and interference	THEN stored data will become corrupted/incorrect	Cosmic Rays	D	1	1	D1	Force developmet to parity and error detection schemes in firmaware for all communications
3	IF open source programs do not work as described	THEN design is set behind due to designing additional programs/functions/blocks	Unpredicted Factors	B	3	4	B4	Our team will produce our own open source programs for any of those which do not work as described
4	IF vaccum causes solderpoints to flake and cause shorts	THEN a high current flow (short) can occur, causing component damage	Material Science Factors	B	2	2	B2	Utilize Sn62Pb37 solder rather than lead-free (tin) solder
5	IF vaccum causes PCB to outgas	THEN surrounding components and systems experience unexpected debris which may lead to opens/shorts	Material Science Factors	B	2	2	B2	Place PCBs through vaccum cycles prior to using
6	IF cubesat vibrates more than design specifications	THEN connection would be lost between the timecard and motherboard	Rough Launch, Space Debris Collision	B	2	3	B3	Develop option to mechanically strengthen the electrical connectors
7	IF the timecard loses power	THEN the oscillator and all other components will not function	CubeSat loses power	A	3	4	A4	No resolution, other than power cycle once CubeSat regains power
8	IF Displacement Damage Dose occurs	THEN non-ionizing energy loss occurs causing device and/or component degradation	Energy deposition by impinging radiation	A	3	3	A3	If CubeSat is not protected, develop protection barrier
9	IF Single Event Effects (Single Event Latch Up) occur	THEN communication packets will contain incorrect data	Singular, stray, energetic particles	A	3	3	A3	If CubeSat is not protected, develop protection barrier. Can additional implement strongery parity detection and schemes
10	IF Atomic Oxidation occurs	THEN electrical connection including solder points may lose conductivity	Presence of strong oxidizing agents	A	3	3	A3	If CubeSat is not protected, develop protection barrier
11	IF parts have lead times over a month	THEN parts may not be in hand when required to prototype	Supply/Demand	C	2	3	C3	Order significantly early than expected, if not possible, look for other vendors or options.



Required Artifacts

- Risk register that is updated regularly, posted in EduSourced with associated Risk Burndown Chart by phase
- Summarize highest priority risks in this document: *what* are they, and *who* is doing *what* to mitigate them?

Open Items [Ian & Nsadhu]

Use this space to call out unresolved items and provide your plans for resolution.

22257: Space Time Card

Project Management [Tanner & Eva]

Developed a Task-based Project Management list using Trello. Each card should include:

- Description of Task to be completed by next group meeting by individual team members
- Task Owner identified
- Date Task issued
- At minimum there should be 3 column from L to R:
    - Planned Tasks
    - Tasks in Process
    - Completed Tasks

The Trello board should be linked to this document along with a snapshot

Mid-Phase Sprint/Scrum Review with Guide based on Trello board

Sprint-end Retrospective - Answer the following questions:

- What went well?
- What could be improved?
- What do we commit to improving in the next Sprint?

Link to Trello:
https://trello.com/invite/b/671a78edf4f62e22545281ae/ATTI2b4091480a6eaea83d203fbbd5bb69d9F87302C9/atomic-clock

Design Review Materials [Eva]

Be sure to update the following in your Phase 3 folder:

- Pre-read with agenda and presenters listed
- Presentation and/or handouts
- Notes from review, including action Items
- Supporting documentation for your client.

Share this page and relevant supporting documents with your client in preparation for the review. This will ensure that they know what you will be presenting and how to view all of your work. Draft work you've been keeping in a Google drive should be copied to this phase folder in EduSourced as a snapshot in time of your progress.

Pre-read: Summary Report and Presentation

- Agenda
    - Discuss progress made in the Preliminary Detailed Design Phase
- Presenters
    - Eva Czukkermann, Ian Dolfi, Nsadhu Muyinda, Drew Schacke, Luke Schrom, Tanner Smith

Notes from Review: Design Review Notes

Documentation:

Presentation

Block Diagrams

Trello Board

Risk Assessment

Gantt Chart

22257: Space Time Card

Requirements and Testing
Bill of Materials

Goals for next phase [Tanner]

As a team, where do you want to be at your next review? Visualize for the customer what the end state for the next phase will be. What are your goals for the next phase?

Individual phase plans (what did I plan to do, what did I actually do, what did I learn, what do I plan to do next, and what blockers might I have) are due to myCourses.

Required Artifacts

- Include a list of planned tasks, by team member, for the upcoming phase. *A snapshot of your overall project plan (Gantt chart) should be linked in this document, and must be included in your EduSourced Phase folder*
- Phase-end Retrospective - Answer the following questions:
    - What went well?
    - What could be improved?
    - What do we commit to improving in the next Phase?