Technology for integrated systems

# Before packaging

## Wafer thinning

* Back grinding thinning the substrate.
* After back grinding, Si-back is damaged because the stress. Relief by dry polishing, CMP, wet etching and dry etching.

## Wafer dicing

* Dicing wheel cause damage like clam shell and crack. (想象切玻璃)
* Step-up dicing: 宽刀接着窄刀Traditional dicing 切low-k BEOL（金属连接层）很容易damage, set-up dicing 解决了这个问题。
* Laser dicing: 有heated affected Zone, 影响精度。
* Stealth Dicing: 在不破坏表面的情况下，通过内部的精确切合来分离出die。Two stages: laser beam creating a modified layer or stealth-dicing layer, then external force is applied to simulate the dies along the modified layer. (掰玻璃) 比起两种方法: No damage, no need for cleaning, no cutting loss.
* Plasma dicing: 用Plasma 照patterned区域完成分割。

# Die attach

## Wire bonding

* Pros: no special additional chip process, software tooling, design flexibility（允许芯片上任何位置的pin连接到pad）, die availability（不需要特殊的die来执行packaging）.
* Cons: Large total footprint（线连出来占地方）, One bond a time, lead inductance(parasitic), limited Pre-testability（连好才知道好坏），repair difficulties.
* Loop shape: 引脚和其他连接点的弯曲属性
* Ball bonding and wedge bonding: <https://youtu.be/fazeH4PHvpk>
* Wedge boding: substrate heating not required (less heat，ball bonding有一个融化的过程), unidirectional bonding (less optimistic angle to reach), low profile and fine pitch (loop非常好控制，不需要formation bond，所以能实现fine pitch), Less susceptible to cleanliness/Yield issue (在较低的温度下进行), High susceptibility to Fatigue (At bond heel) , Greater Part Clearance required (有杂质粘不住), Slower bonding process

## Tape Automated Bonding 用于解决Wire bonding 太慢的问题

* 已经做好的线框直接连到chip上，裁剪以后直接压到carrier 上

## Flip-chip technology

* Mounting the chip upside-down on a substrate with direct electrical connections through a conductive “bump”, but matching I/O on the receiving substrate (alignment).
* 类似于BGA：[https://youtu.be/Aw6Pq7TkDyo](https://youtu.be/Aw6Pq7TkDyo?si=yzdfKJNwr89KJEzd)
* Underfill: 让bump更稳，two options: 1. Underfill在锡球完成以后从侧面进去 2. 先搞胶，因为是流动的所以可以连接bump，然后curing.

### Soldering reflow

1. Electrolytic plating of solder bumps: 目的是为了拉一个pad到bump的金属层出来。在含有金属离子的溶液中，将基底作为阴极放入，通过施加电流，金属离子被还原并在基底表面形成均匀的金属层。
2. Electroless plating: 将基底浸入含有金属离子和还原剂的溶液中。金属离子在没有电流的情况下被还原，并在基底表面自发形成金属层。
3. Solder paste: [https://youtu.be/p6h6DMhBBpM](https://youtu.be/p6h6DMhBBpM?si=u-XzsVM2F3v6rHGi)
4. “stud bump”: 类似于wire bonding 形成一个pad上的bump然后压。

### Adhesive joining

ICA: 只跟pad连接

ACA: glue 里面有有些conductive的球，能导电，bond pad把这些给压实了。

Non-conductive adhesive: bond pad直接连接，adhesive 只做连接。

### Conclusion

* Pros: area array connections are possible, high I/O counts and /or relaxed I/O pitch; 尽可能少的空间; all connections in one step, high yield; high alignment precision; low electrical inductance.
* Cons: requires additional processing of the wafers (form the contact pads); not readily available, many technologies; visual inspection bumps difficult; no repair after underfill process; requires matching I/O pattern; 热疲劳; require high temperature process.

Encapsulation by liquid dispense: <https://youtu.be/c68SR9XLsbg>

# Established Packaging

## Single chip packaging

Leaded package: SIP 封装

Leadless (no legs)

## BGA packaging

## Chip-Scale Package

* Future reduces the size and thickness of the BGA packages, evolution to smaller ball pitches. Since the packages are about not more than 1.2 times the area of the chip.
* Some examples like thin-film ball grid array, thermal-enhanced

## High density “interposer” substrate BGA (redistribution layer, interposer)

* To solve the problem of the gap between PCB scaling and IC.

# Wafer-level packaging

承接上部分的interposer technique

* Dielectric 之间的金属连接层，用导线进行连接
* Main technology for metal is semi-additive Cu electroplating.
* Using different layouts to achieve L, C, R.
* Thin-film process: lift-off metal patterning gap略大于pattern, subtractive etching 导致 resist strip: gap >> pattern, semi-additive electroplating.

## Wafer level chip-scale packaging

### Flip-chip redistribution (Die 的bonds重新distribute 下去)

* Fan-in 封装技术通常用于那些I/O端口数量较少的芯片。在这种封装中，所有的I/O连接都被设计为向芯片中心汇集，这意味着封装的尺寸通常不大于芯片本身的尺寸。因此，芯片的外围边缘被用来放置连接点，而且通常封装面积不会超过芯片的面积。
* Fan-out 封装技术是针对高I/O密度的芯片设计的。在fan-out封装中，芯片的I/O端口会扩展到芯片尺寸之外的区域。这种设计允许芯片外围的封装面积大于芯片本身，从而提供更多的空间布置额外的I/O端口。

### Wafer-level chip Scale packaging

* Fabricated in wafer-level process
* Directly mounting to the PCB and therefore with a large area array contact pitch.

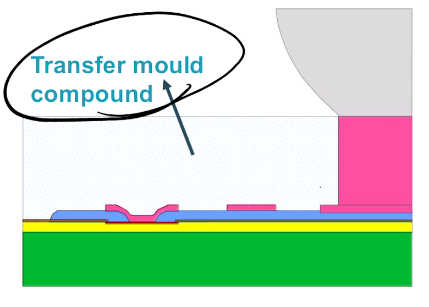
## WLCSP technologies with improved thermos-mechanical reliability

### Epoxy-Collar CSP

* Reinforcing polymer “collar” around the base of the sold ball.
* A drawing of a pair of binoculars

  Description automatically generated

### Bump on pillar

* Placing the solder ball on a metallic pillar.
* 

### Compliant layer

* 焊点下加柔性层，以显著减少热应力

## “Reconstructed” WLCSP technology

Thinning 和 dicing 过后attach the “know-good-die” on a new wafer with larger inter-chip spacing. Perform WLP-CSP technology on the reconstructed wafer.

## Conclusion

* Reduce the packing cost by collective processing.
* 弥补”interconnect GAP” 的差距
* By the “multilayer thin film technology”, Enable “above-IC” processing of interconnect lines and high-quality passive components. Building high density interposer substrates.

# 3D packaging

* Stack-die packages by wiring bonds. 比较古早的技术。
* Cost effective processes: maximize the use of collective process: at wafer and panel level and avoid individual die handling.
* High density 3D-technology opportunity: 3D is not limited to connecting the I/O bond-pads of different die. Possible to interconnect tiles on a die to other.

## Technology for 3D interconnect

### 3D SOC

* Semi-global: hybrid bonding contact at contact interface.
* Intermediate: dielectric bonding contact, TSV contact after stacking.
* Local: post BEOL tier, to second device.

这三者之间的区别可以理解为最后一个是直接在CMOS工艺上面直接继续动刀。Semi-global就是直接process上面流出pad后直接跟第二个Device连接，而intermediate 选择使用一层dielectric, 在silicon 上做via连接。

### Via middle Through-Si-Via process

简单来说，这个方式做到了在原有wafer 上面直接搞出从背面过信号线的pad.

1. High aspect ratio Cu Damascene technique.
2. Contact the Si carrier with temporary glue.
3. Thinner the water until there is residual Si thickness.
4. Then process dry etch make the “soft” TSV reveal, expose TSV with liner oxide.
5. Backside passivation and RDL, micro-bump processing.

The connection (bump) is continuing to scale.

### 2.5D technology

High density lateral die-die interconnect on Si interposer substrate

### Important graph that almost explains everything

A screenshot of a diagram

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# MEMS packaging

## Bulk micromachining

Selectively removal of substrate material by chemical and physical way.

Must be simple complexity and can’t be integrated with microelectronics.

## Surface micromachining

* Use single-sided wafer processing, make use of sacrificial and structural layers, give more precise dimensional control.
* Deposition: sputtering, evaporation, CVD, Thermal oxidation.
* Etching: isotropic and anisotropic, plasma etching.

### MEMS Capping

0-level vs. 1-level packaging:

0-level packaging，通常指的是在微电子和微机电系统中最基础的封装形式。这个阶段涉及到芯片本身的直接封装，包括晶圆的划分、裸芯片的测试、和芯片的初步封装处理。0-level packaging 旨在保护芯片免受物理和环境伤害，同时为电气连接提供必要的界面。

在MEMS中，0-level packaging 特别重要，因为它不仅要提供物理保护，还可能涉及到在封装内部创建特定的环境（例如真空或特定气体环境），这对MEMS设备的功能至关重要。

1-level packaging，这一级别通常涉及将一个或多个芯片（已经经过0-level封装的）与其他电子元件集成在一个单一的封装单元中。这一点是跟之前的微电子的封装是一样的概念。

Hermetic: need the electrical connection feedthrough - Feedthrough connection 通常涉及一个特制的组件，这个组件能够穿过一个隔离层或壳体，同时保持该层的密封性和保护功能。

## Thin-film MEMS packaging

* Lateral holes and channel created.
* Vertical holes with sealing layer.
* Pores layer with sealing layer.

## Vertical etching channels

Using a sacrificial layer to encapsulate the cantilever and etch away after the packaging is established. Then with a sealing layer on the top.

## Different electrical feedthrough technique

A diagram of a diagram

Description automatically generated with medium confidence

* Gettering material absorb the residual gas.
* Hermeticity is not 100%, degradation based on time. The leakage rate is based on the width of BCB seal.
* Gross leak test and fine leak test.

A table with text on it

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我不知道为什么要考这个 结论是gyro 用getter Acc不用 to keep the atmosphere stable. 如果问到optical MEMS, DLP，就是要保持干燥密封 那也可以用getter absorb water.

# Image sensor

Mono sensor and color sensor: 区不区分每一个pixel上的颜色

# Etching – guest lecture

## Basics

* Selectivity: the rate of etching A and etching B
* Plasma: ions + electrons
* Etching = ions + neutrals

## Anisotropic

* The wafer under plasma becomes negatively charged. So, there is electron repulsive potential.
* The combination of ions and reactive chemical species. Surface with ions and surface without ions. Ions 破坏了原有的化学键的结构，使得chemical spices更容易对surface进行反应。只要ions存在方向性，就能让Vertical etch rate >> horizontal etch rate.
* Make horizontal etch rate to zero, we can make use of protection of sidewall.
* At the same time of the etch process, deposition of polymer layer.
* Gas mixture, create C-N sidewall passivation.

## Selectivity

* Etching Si selective to SiO2: Addition of Oxygen: increase selectivity. Since the presence of Carbon reduces selectivity, extracts Oxygen from plasma and stop layer C-O bound.
* Etching SiO2 selective to Si: The O in SiO2, stimulates the desorption of the C-F by formation of CO, CO2. On Si, no Oxygen is release resulting a thick polymer layer, low etch rate.
* Additional Hydrogen make the plasma more F deficient (HF), etch rate of SiO2 and Si decreases.

## Strip refers to the removal of resist and residuals after etching

* In-situ: make use of excited state reactive gas like (O) to make the organic resists become CO, CO2 fragments.
* Low efficiency, that’s why introduce implanted resist.

## Tool

* Density regulation and ion energy regulation by induction induced plasma and capacitive coupling respectively.

# Process

Basic NMOS process (skip, most general MOSFET process)

与基本CMOS制造流程内容一样

Notice: 对poly 也会施加doping，原因是希望他locally conducting

## 3um CMOS process (only new process will be added)

* Easy CMOS there is single well p-well, NMOS required high doping for Vt control.
* Well formation: guild ring was implemented. There is n+ and p+ region below the local oxidation part to prevent the parasitic bipolar transistors to switch on.
* Punch through was introduced, AntiPT is going to avoid it. Grow implantation oxide on channel and doping P. And Higher channel doping also raises the potential barrier between the source and drain. Why only pMOS? p-well is in a n-type substrate so that have a lower doping level.
* S-D formation, p+ implantation for the source and drain areas (unmasked), for the cost, just get rid of unnecessary masks. Could be done by counter doping.
* An implantation oxide? 1. Never put PR directly on Si. 2. Generation of particles during implantation. 3. Channeling, 过度穿透。

## 1.25 um CMOS process (first scaling step)

* Drain engineering: keep constant field scaling.
* LDD = lowly doped drain. Decrease the strength of electrical field.
* Peak electrical field can cause degradation, worst case = nMOS (electron mobility is higher than holes)
* Make a spacer to separate the low dopants and high dopants region, high dopants area has a better connection. Spacer normally SiN or SiO, fabricated by CVD.
* Metal hillock to avoid some issues.
* Planarization: to accommodate the litho/step coverage.

## More scaling and the potential challenges

* Vertical scaling: scale the Cox. Vertical scaling forces us to scale the current proportional as well as the depletion region. 这里他没讲清楚，其实就是要让output 一样，而output 是由gm所决定的，而进行vertical scaling 主要原因就是为了scaling gm, 使得long channel = short channel transistor. 也可以通过别的手段来叙述：比如说induce higher electrical field to control the carriers in the channel.
* Subthreshold swing > 60mV/dec
* Constant field scaling idea however Vdd can’t be scale sometimes due to the reliability issue.
* Short channel lowering the barrier induce by the drain bias.
* Less electrons to get the current and cause the scattering. Then reach the velocity saturation. If the channel gets shorter, the output characterization becomes linear rather than quadratic dependence. Saturation point becomes lower, and need to have more Vgs to make large Id.
* Effective mobility: intrinsic silicon electron is not collided with lattice. Add dopants, not fit, so that symmetry is broken. The surface is a kind of defect. E is pulling the electron to the surface. (look at the graph)
* Snapback: the holes has strongly push to the substrate. Like npn bipolar transistor, gives a base current to the substrate while the structure source-drain-substrate is exactly a bipolar transistor.
* Hot carrier: change the interface, make the threshold voltage shifts.
* HC lifetime: to decide the Vdd.
* Oxide Breakdown: charge injection in the oxide under influence of large electrical field. Drop in lifetime at fixed gate voltage due to temperature, area and percentile. Thinner, worse.
* CMOS latchup: several bipolar transistors occur. Retrograde well to make the doping deeper.
* Atom is not scalable, Roughness of the line, doping distribution, tunnelling effect…

## Scaling to

* Quasi-constant voltage scaling: till 0.25um
* Twin well: better diffusion, n-well and p-well
* Amorphous-buffered LOCOs: create a buffer to inhibit the growth of the oxidation laterally.
* Dual poly problem (inverter): contact.
* Salicide: sputtering a metal on the top, and do Rapid thermal processing, there is a layer of metallization form only on the drain and gate. Need to control the depth quite accurate to avoid direct connection to the substrate.
* Rapid thermal annealing: dopants are introduced by Ion implantation and then needs activation to promote substitutional lattices sites. 不同node下的thermal 需求量是不一样的。
* New contact: TiN to Alu.

## Aggressive scaling to 0.18 - 0.13um

* Shallow Trench Isolation: field oxide. **Not growth oxide** on the wafer, active area patterning, then etch the wafer and create the silicon oxide by HDP oxide **deposition**. Finally, planarization it by the CMP.
* High density plasma CVD: deposition – sputtering (deposition)
* Gate module: remove implant oxide –> gate oxidation –> LPCVD poly layer -> photo poly -> dry etch poly -> strip resist -> re-oxidation.

A graph of a line graph

Description automatically generated with medium confidence

* Saturation is even worse because the effective channel length becomes shorter.
* Halo implant: opposite polarity on the drain and source sides.

A diagram of a graph

Description automatically generated

* **Spacer module**: etching can’t remove the Silicide at two sides of the gate. 1. Electrical isolation between gate and S/D. 2. Offset S/D regions and extension.
* Changing from Al to Cu: lower resistivity, more resistant to electromigration. Make use of Damascence to do patterning => fills into the pattern without etching, then CMP.

## Scaling below .13

* Gate insulator scaling: too thin => yield and reliability, penetrating.
* High-k material introduced to compensate the scaling of the tox.
* Gate-poly depletion effect: capacitor connect in series, when the apply voltage on the gate, the carrier’s redistribution will make the carrier depleted. Make variation between Cgate(total cap)/Cox => HKMG
* Gate replacement: low thermal budget for Metal gate available. Dummy poly gate first, then etch dummy gate away then form metal layers.
* Improve mobility: tensile improves nMOS and compressive layer improves pMOS. Also orientation dependence.
* 3rd way to increase mobility: Ge substrate.
* RC reduction: lowing C low-k material. Deposition of sealing layer to do to change the surface state. Mechanical properties…
* Power: Vdd decreases, if put Idsat as constant, Vt decreases, Ioff increases. Leakage power becomes dominant in power.
* News structures: PD-SOI, FD-SOI. Mutli-gate devices. => FinFET Wfin is most crucial parameter not Lg. Vt can’t be tuned by doping but geometry becomes width.

# Lithography

与基本CMOS制造流程的课上相同的内容不列出

* General lithography…(skip)
* Fourier transforms of the image
* 我只要0-order and 1st-order to goes into the lens after the mask. (这章最难理解的是这个部分) : 可以将打出mask的光看作是一个Fourier series, more order captured more resolution. Also, by superposition of all light sources, there is a distribution from the specific lighting points. 增加了NA. By off-axis, the on-axis which is low resolution part has been abandoned and left the high-resolution image. 又增加了NA
* Standing wave reflection: top ARC, bottom ARC.
* OPC, phase shifter…

# Micro implants

与BioMEMS 相同的内容不列出了

* Biostable and biocompatible: the ability of a material/device to perform with an appropriate host response in a specific application. != biocompatible material, might have a foreign body reaction exists.
* FB: results in mechanical anchoring of implant, isolates implant from the host. Chronic inflammation(慢性发炎)。
* Biocompatibility is contextual: external environment determines the clinical outcome of the medical device. We can consider accelerating the process of the test.
* Biostability: ability of material to keep all its properties despite **all stresses** to which it **is exposed during the ‘exposed’ period** -> contextual material property! Four aspects in affecting the biostability: 1. Physico-chemical stress 2. Biochemical stress 3. Electro-chemical stress 4. Mechanical stress.
* Trends: smaller device and packaging, power of implants…

# Memory

Extension from the lecture of **computer architecture** （省略部分内容例如存储hierarchy）

## Current memory technology

* Volatile (易失性的): the data will be destroyed if external voltage supply is not exists. SRAM, DRAM
* Scaling of DRAM (requirement same capacitor): scaling the EOT, keep the effective A constant.
* Barrier of semiconductor to reduce the leakage from the transistor side.
* Threshold voltage shifted by the electrons in the gate, read-out by selecting element and current sensing.
* Fowler-Northeim mechanism: quantomechanical tunneling through an energy barrier. An appearance of stress-induced leakage currents. In NAND. 把电子吸上来
* Channel hot electron injection: injected over the gate oxide into the floating gate. NOR
* EPROM: a small cell, UV light for erasing. EEPROM is a larger cell. NOR: ½ drain contact is fast access. NAND all but slow access.
* Retention (老化测试):

## Charge trapping memory

* Electron or holes are transported through the oxide and stored in traps inside the nitride. SONOs, Poly-si – SiO2 – SiN – SiO2, advanced to the TANOs then.
* Deep hole and electron traps in trapping layer (retention)… 看slides 吧

## 3D integration

看tutorial讲得很好很细节。

## New type memories

* FeRAM
* FEFET: dielectric in a ferroelectric FET, polarization charge compensated by charge in channel.
* Phase charge memory: based on the melting and crystallization of material.
* Magnetic memory: based on magnetic tunnel junction.
* STT: two distinct resistance states.
* RRAM: in metal oxides, a conductive filament (could be oxygen vacancies) is formed by “breakdown”. Local oxidation reset and local reduction form.