**12/06/2024**

**Van Hoofs part**

**1)Question about the pin count. 800 pin counts on a chip with peripheral pitch of 40 μm. The graph for the area array pad pitch of a chip with 40 μm peripheral pitch was given.**

**a: Calculate the area array pad pitch with seven rows and peripheral pitch of 40 μm.**

**b: Calculate the area array pad pitch with 2 rows and 30 μm of peripheral pitch.**

**2) What is the main function of the underfill?**

**Mechanical Support CTE**

**3) Two chips of same size, but with different numbers of I/Os.**

**a: Can you do flip chip between them? No, different I/Os.**

**b: If you had an interposer would it be useful or not? (something like that I don't remember) yes, I/O Redistribution**

**4) Write two limitations of MEMS thin film packages.**

**Hermeticity, Mechanical Durability**

**5) What does it mean that cell cultures have a low translational value?**

后面有。

**Part Van Hoof**

**2019**

* Give the formula for the relationship between chip size and pitch, pin count in peripheral bonding and area array. (graph provided)
* We have a wafer containing dies of 1mm\*1mm. Each die has 120 pin on peripheral. We want to transform it into an area array package (10\*12).

(1) what technology (wafer level) will you choose if the pitch of the area array is 300 um. WLCSP

(2) what technology (wafer level) will you choose if the pitch of the area array is 80 um. Fan-Out Wafer Level Packaging

Fan-out 不是用来适应更大的pitch嘛？

(3) what are the key steps in both technologies

* Can I use ICA for the two given chips (drawing of two chips, one with very small pitch size and one with large pitch size) what technique would you use?

ICA for large pitch; ACA for small pitch 对的！！

* Scientists use cell culture as a first step although it has low translational “output” What is translational “output”? Some other techniques have a high translation “output” what are they and why they are not being used as a first step?

Skip

* What is the risk to use Glob top as the final sealing layer on thin film capping MEMS?

What is global top sealing?

My answer: limit choice for the sealing ambient (gas pressure problems) also the sealing layer could be possible to be deposited into the cavity, cause the change of the performance of the device.

* Choose a technique based on the number of Pin and Area (calculate density and decide)
* RIGHT/WRONG on medical implantation
* Laser Dicing ..is it suitable for Cu and Low-k materials./ Would you use laser dicing for Cu-low K? https://www.disco.co.jp/eg/solution/library/laser/low\_k.html

Cu has high thermal conductivity; low-k is temperature sensitive—crack

* Does silicone solve all the stress?
* Given a finished 300 mm wafer with 1000 dies in 28 nm technology, each die having about 800 IOs. You want to attach an unfinished memory die to it and have to decide on the technology. These memory chips will be made on a 200 mm wafer and have about 200 IOs. Do you choose a hybrid or 3D integration: 2D, 3D-SiP, 3D-WLP, 3D-SiC and do you go for D2W or W2W?
* For a small chip with 48 IOs that are closely spaced together, which adhesion technique do you choose: ICA, ACA, NCA?
* RIGHT/WRONG: The foreign body reaction does not depend on shape, material or texture of an implant. wrong
* why Al wire bonding is less strictly required with cleanness than Au wire bonding (ultrasonic vs thermosonic)

Al has better oxidation resistance, ultrasonic can handle surface contaminants; gold not, ductility（延展性）

* mathematical formula for chip i/o graph chip size vs periphery bond pitch and area array pitch
* what is the process for "Cu nail" expose after BEOL/FEOL (ans:Bonding wafer to temporary carrier
* Wafer thinning back-side to expose Cu-nail; back grinding can not touch Cu)
* Benefits of 3D-SIP compared to 3D-WLP.

3D SIP is stacking in chip level. Wafer-level packaging is making use of TSV to connect.

* Power amplifier, 40 I/O’s spaced apart. Which adhesive technology can be used (NCA, ACA, ICA)?
* Explain graph “CHIP I/O DENSITY”, Chip size vs Pin count for periphery bond pitch and area array pitch.
* Give the formula for the relationship between chip size and pitch, pin count in peripheral bonding and area array. (graph provided)
* Explain the risks of using ICA, NCA for two given chips.

NCA has some problems against uniformity of the pad.

ICA has misalignment of the pads cause shift of the adhesive glue?

ICA: maybe it can cause shortcut when the pitch is small.

NCA: two bumps may not contact, no electrical connection. (个人理解

* Micra is the most advanced pacemaker on the market. Why are some patients stilling using the traditional pacemaker? Is there any situation only Micra can be used? Is there any situation Micra can’t be used?
* What are the mathematical relations/formula for chip size vs. pin count for peripheral bonds and area array bonds? [Displays I/O graph]
* For medical implants, is the FBR affected by the surgeon? And by the engineer who designs it? And by the patient? Explain.

Yes (需要完善答案) the position of the implant is critical.

**2023**

1. You want to redistribute a chip with 1600 I/O's and a peripheral pitch of 20 μm. Calculate the area array pitch in 4 situations, ignore corners. The graph was given, but only went to 400 I/O's and was for a peripheral pitch of 40 µm. In case you have:

Isn’t there a formula for this?

a) 2 rows

Area array pad pitch (AAPP) of 56 µm (assuming cte total pad area)

AAPP ⇒ 80 µm at pin count = 800 @ 40µm PP ~ 1600 @ 20µm PP

Pad area = (800(80µm)²)/4 = 1280000 µm² (Assuming cst total pad area )

1280000 µm² = (1600(x)²)/4 ⇒ x = sqr((1280000\*4)/1600) ~ 56  µm

I’m not sure if you are required to keep the pad area constant. What do you guys think?

I get ~40 µm

b) 4 rows

~77.6 µm

c) 7 rows

~126.6 µm

d) full area array

Area array pitch of 200 µm (assuming cte pad area)

400 pin count ⇒ 200 µm (from graph)

⇩ x 2 ⇩ x √(2)

800 pin count ⇒ 280 µm

Pad area = (800(280µm)²)/4 =15680000 µm² (peripheral pitch = 40 µm)

Now for peripheral pitch of 20µm

Assuming cte total pad area, AAPP =  √((4\*15680000 µm²)/1600) = 197.9 ~ 200 µm

Upper limit pad area = chip size = ((20µm \* 1600))/4)² = 64000000 µm²

Total pad area ~ ¼ of total chip area when using full area array!

2. A picture of two wafers and then the question was if you could bond them using flip chip, and whether you could do so if you used solder reflow first. One of the wafers had bumps of about 50 μm wide (not sure about this number) and they were either 45 or 55 μm high (so nonuniform, that's why he's asking about the reflow in the second question), with 6 μm in between every bump.

If we would do flip chip immediately, some bonds will not be connected because of the non-uniformities (up to 10 µm of space).

Reflow is used to lower the non-uniformity of the solder bumps since height uniformities are larger than volume non-uniformities for the same amount of material. One must be careful about the low spacing between the bumps (6 µm) to avoid the bumps touching (-> shorting) when reflowing.

3. a) Does it make sense to use a metal seal for a polymer substrate MEMS bolometer?

No, it does not make sense to use metal seals for a MEMS bolometer, since IR radiation is reflected by the metal, and thus the bolometer is not exposed to IR radiation. A ceramic packaging technique which is transparent towards the IR radiation is a more suitable

b) Can we use getters?

Yes, getters can be used in a MEMS bolometer. [Thin-film getter integration is one of the key technologies enabling the development of a wide class of MEMS devices, such as IR microbolometers and inertial sensors, where stringent vacuum requirements are needed](https://www.researchgate.net/publication/347653332_Vacuum_Packaging_Requirements_for_MEMS_and_Characterization_Techniques). The getter material should however not interfere with the transparency window (for IR) that is required for the bolometer to be sensitive to IR.

4. Can a 1 mm diameter solder bump be considered a micro bump? What are the requirements?

No, micro bumps are a lot smaller in size (µm size) and are typically purely i ntermetallic (e.g. CuSn) as opposed to solder bumps which are composed of a high melting point solder (core) and a low melting point solder “jacket”.

5. 300 mm wafer with 5x5 mm Image sensor chips with 400 I/O's and 300 mm wafer with 5x10mm image processing chip with 700 I/O's. All I/O's of the sensor chip go to the processing chip.

a) What are the requirements to use flip-chip?

We can’t use wafer-to-wafer bonding as the processing chips are larger than the sensor chips -> we can use die (sensors) to wafer (processing). The 400 IOs of the sensor chip need to match the corresponding IOs on the signal processing chip. The remaining connections to the packaging can be done using wire bonding

Backside illumination

Remember to thin the wafer. Use an interposer (?) only way without dicing and redistributing

b) What are the requirements for using 3D-SIC?

We need to be able to make through-Si vias, the contact pitch is somewhere between ***40 and 5 µm*** (process between FEOL and BEOL -> we can’t do this on finished chips)

He mentioned that both were possible, you had to say in what situation they are possible

**2022**

**4. A 200mm wafer with 7000 sensor chips with 16 IOs: 14 IOs to connect to the signal processing chip and 2 IOs for power supply (VDD and GND). A sufficient number of 200mm wafers with 800 signal processing chips with 64 IOs: 2 IOs for power supply, 14 IOs to the sensor and the rest are digital and analog IOs. There are sufficient numbers of 128-pin package of 15x15mm.**

**a. Can the sensor chip be integrated to the processing chip using flipchip technology? Why/why not? How can you solve it?**

Yes, the sensor chip can be integrated with the processing chip using flip chip technology. The primary challenge is ensuring precise alignment and reliable connections. This can be addressed by using high-precision bonding equipment, and if necessary, employing an interposer or RDL to handle any discrepancies in pad layout or routing requirements. Careful design, verification, and testing are crucial to the success of this integration.

**b. Can the sensor chip be integrated to the processing chip using TSV technology? Why/why not? How can you solve it?**

We can.

**c. Suggest the simplest method to interconnect and package both chips with the above package.**

**d. If you can change the package, which one would you choose? (From the given image, the current package has leads).**

**5. Given the area-array pitch vs chip count graph (from 2 rows to full arrays) with peripheral pitch of 40um.**

**a. If there are 40000 IOs, what will be the area-array pitch of 5 rows?**

2110 µm? If we take 0.05 as the slope and assuming linear growth

I get 199.6 µm

**b. If there are 40000 IOs, what will be the area-array pitch of full-array?**

8060 µm? Taking 0.2 for the slope I’m getting 2000 µm = 2 mm. Question seems unrealistic though. 40000 I/Os \* 40 µm is a circumference of 1.6 m! Then assuming it’s square, sides of 400 mm, which is huge! That’s what she said.  
That gives an area of (400 mm)^2, so sqrt((400mm)^2 / 40000) = 400 mm / sqrt(40000) = 2 mm (dividing the area by the amount of I/O’s, gives the area per I/O in the area array. Taking the square root of that, should give the pitch).

I get 2000 µm

**6. Given a polymer MEMS on silicone polymer substrate.**

**a. Is it reasonable to use metal seal for this MEMS?**

No need for a metal seal as the silicone substrate is already leaky

**b. Is it reasonable to use getter for this MEMS**

**?**

Silicones are one of the most permeable materials, so if it’s used as a substrate, adding a getter will not make a lot of sense, it will quickly saturate

**2016**

* Choose a technique based on the number of Pin and Area (calculate density and decide)
* RIGHT/WRONG on medical implantation
* Does silicone solve all the stress?
* Given a finished 300 mm waver with 1000 dies in 28 nm technology, each die having about 800 IOs. You want to attach an unfinished memory die to it and have to decide on the technology. These memory chips will be made on a 200 mm wafer and have about 200 IOs. Do you choose a hybrid or 3D integration: 2D, 3D-SiP, 3D-WLP, 3D-SiC and do you go for D2W or W2W?
* RIGHT/WRONG: The foreign body reaction does not depend on shape, material or texture of an implant.
* mathematical formula for chip i/o graph chip size vs periphery bond pitch and area array pitch
* what is the process for "Cu nail" expose after BEOL/FEOL (ans:Bonding wafer to temporary carrier

Wafer thinning back-side to expose Cu-nail; back grinding can not touch Cu)

**2015**

* 150 Camera chips in a 300mm wafer (400 I/O’s), already manufactured. Integrate them with processors that are on another 300mm wafer, also already finished. Which type of 3D integration can you use? What are the requirements for the chips and their I/O’s?
* Explain graph “CHIP I/O DENSITY”, Chip size vs Pin count for periphery bond pitch and area array pitch.

**2024**

* **1) What are salicides? Why do we always need spacers with this technology?**
* **Salicide self-aligning-silicide the fact that it is used for better contacts. He told me spacers are needed to avoid bridging which is a contact between S/D and the polysilicon gate.**

两个作用 1. Avoid bridging 2. Assistance for the S/D I/I. (halo implant and LDD)

* **2) Talk about SRAM and DRAM and their major scaling issues.**

SRAM scaling issue: 1.2.3.

DRAM scaling issue: 1. Leakage 2. Physical boundary hits for the d of the cap.

**23 June 2023**

**Part Van Houdt**

1. Discuss the steps in the production of state-of-the-art nMOS (planar). And explain the function of all implants. (With state-of-the-art nMOS, he meant the nMOS in CMOS)

Can describe the C013 imec process flow for an Nmos transistor with Cu/low k interconnects (damascene)

For real “state-of-the-art”, look at last chapter (still considering a planar structure): replacement of SiO2 with high-k oxides on the gate (EOT scaling), metal gate, gate-last, strain engineering to increase µ through the use of a strain-inducing capping layer (end of FEOL)& SOI(silicon on insulator)

2. Which techniques/tools do you know to make finer patterns?

Laterally: lithography scaling (wavelength) + tricks (Optical proximity correction, off-axis illumination, micro mirror array, phase shifting mask, immersion lithography, double patterning), etch (ion beam, plasma, …)

Vertically: thin film deposition such as ALD, controlled etching

**24 June 2022**

**Part Van Houdt**

**1. What is salicide and why do we need it? Why do we always need spacer technology?**

***Salicide = Self-aligned silicide (Si-metal compound) Ti, Co, Ni***Metal deposited over S/D and gate, rapid thermal anneal induces silicidation at metal-polySi contacts. No reaction at metal-(dielectric) spacer contact, metal over spacer is removed.

Salicide reduces Polysilicon Gate Resistance and source/drain *contact resistance* as the dimensions of the device get smaller. Hence they help scaling down.

Used to introduce p type polysilicon to the CMOS architecture, enabling us to make pmos transistors

Also used to interconnect p+ and n+ polysilicon (else it would form a pn junction = diode) in inverters?

***Spacer*** technology is used in salicide processes to prevent the metal from diffusing into the silicon substrate and forming a high-resistance contact. The spacer is a thin layer of dielectric material that is deposited between the metal and the silicon. This prevents the metal from diffusing into the silicon and ensures that the contact resistance remains low + used for HDD/LDD before silicide ???

I think there is LDD before the silicide and HDD after.

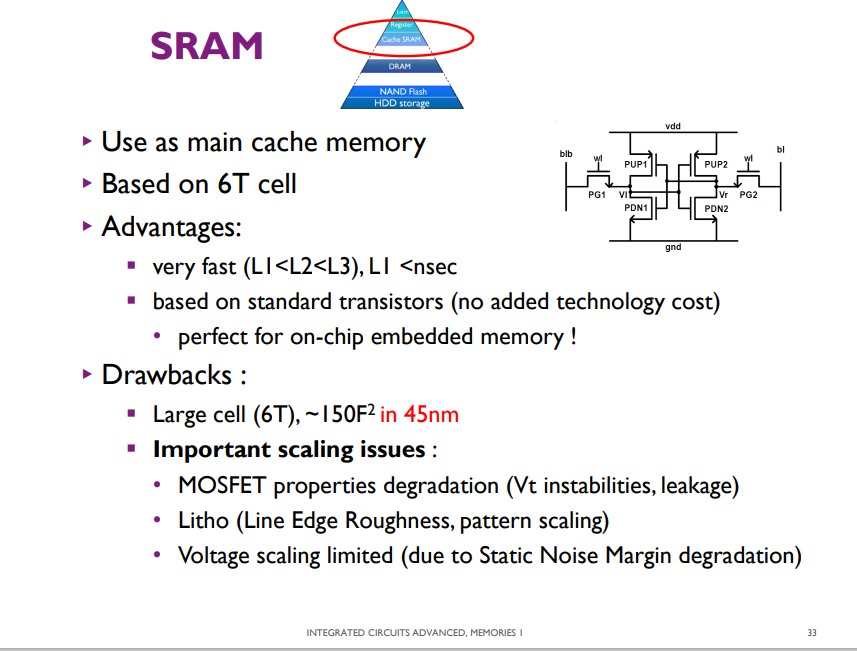
& **Separate drain from the gate; channel control**-- *Lateral Diffusion Control: Spacers help control the lateral diffusion of dopants during the source/drain implantation process. This ensures that the source and drain regions do not extend too close to the gate, which could otherwise lead to short-channel effects.*

*Defining Source/Drain Extensions: Spacers define the lightly doped drain (LDD) regions, which help reduce electric field peaks at the drain end of the channel, thereby reducing hot carrier injection and improving device reliability*; **selective etching; isolation and prevention of short circuit.**

**2. Discuss the main characteristics of SRAM (Random access memory) and DRAM and their scaling issues.**

SRAM (static: memory content stable in presence of power supply, 6T) is volatile memory, which means that it loses its data when the power is turned off. However, SRAM is very fast and has a low access latency. This makes it suitable for applications where speed is critical, such as cache memory.

DRAM (dynamic: information leaks away fast -> needs regular refresh, 1T1C) is also volatile memory, which means that it loses its data when the power is turned off. However, DRAM is much denser than SRAM, which means that it can store more data in a smaller space. This makes it suitable for applications where memory density is critical, such as main memory. (Less 8 slide 33) Scaling DRAM issues: **capacitor** we want high capacitance, but low leakage



**3. Implantable devices need a lot of tests.**

**a. What is low translational value test?**

Translational value tests are evaluations conducted to determine the real-world value, benefits, and impact of medical interventions or technologies. These tests help bridge the gap between research and practical application by providing data on the intervention's effectiveness, safety, and feasibility in real clinical settings, ultimately guiding their integration into routine patient care. These tests are designed to bridge the gap between scientific research and practical application, with the goal of translating scientific discoveries or innovations into tangible benefits for patients and healthcare. In the case of implantable devices, it's crucial to ensure that the testing procedures and methodologies closely mimic the physiological conditions, environmental factors, and patient population that the device will be exposed to after implantation. This helps improve the translational value of the tests, meaning the degree to which the test results can be reliably extrapolated or applied to real-world situations.

A low translational value indicates that the ability to accurately represent the device's performance or predict its clinical outcomes may be limited. In such cases, additional or alternative testing methods may be required to enhance the understanding of the device's behavior and optimize its design, safety, and effectiveness.

**b. Why don't we start the first tests with the highest translational value?**

As stated in the previous question, ideally tests with high transitional values are suggested to be tested in order to mimic the real-world conditions where the implant is going to be placed.

**c. Which tests have higher translational values?**

**26 June 2019**

**Part Van Houdt - Oral**

* Explain schematically the process of NMOS and show all the implants and mention their functions?
* What is the difference between SRAM & DRAM what is all the limitations when scaling them down?
* For his follow up questions he went very deep with the process of SRAM & DRAM and also names of some techniques and parts of the NMOS and what would be the different steps if you have the NMOS as part of the CMOS. Really know everything by heart.
* When Tech can be defined scalable? (Good scaling : Area of cell = Cte.F2, With F the feature size (min print dimension)
* How Floating Gate Tansistor work?
* What type of non volatile CHARGED based memories do you know?
* Difference between NOR and NAND flash. Which emerging memory could replace them?

MRAM, or charge trap memory

* Explain Moore’s law and the benefits, why wafer size increases with time?

chip area per function: 2 every 2-3 years, the number of transistors on a microchip doubles approximately every two years, while the cost per transistor decreases.; cost, performance, power. Cost per die decreases, more yielding dies per wafer.

* Explain the use of implantation oxide. What is a FMEMrificial layer? Give 2 examples.
* Scaling is driven by reducing cost per bit. How is scaling being done by moving to 3D (in general and for flash specifically?)

**June 2016**

**Part Van Houdt**

* When Tech can be defined scalable? (Cf^2 Should decrease when F increases)
* What type of non volatile CHARGED based meemories do you know?
* Difference between NOR and NAND flash. Which emerging memory could replace them?

**June 2015**

**Part Van Houdt**

* Difference between NOR and NAND flash. Which emerging memory could replace them?

**June 2014**

**Prof Wouters: (2 questions)**

* **Describe the evolution of the gate stack: gate insulator and gate electrode in CMOS when scaling further and further. What is next?**
* **Scaling of memories is driven by cost per bit, what strategies can we use to increase the amount of bits/Si area**

**Prof Van Hoof: (5 questions)**

* **Why is dual cut dicing used, and how does it compare with laser?**
* **Explain the I/O graph**
* **Is the implementation of silicone under solderbump enough to relieve all stress from thermechanical processes**
* **What issues do you encounter with non-conductive adhesion (flip chip)**
* **Give some example of materials that are biocompatible AND biostable, biocompatible but not biostable (and vice versa)**

**June 2013**

**Prof Wouters: 2 questions:**

* **in MOSFET technology, where is ion implantation used, which type (consider pMOS) and why?**
* **which parameters of the light source can be optimised to get the highest possible resolution in patterning**

**Prof Van Hoof: 5 questions**

* **can a material by biocompatible but not biostable? Give examples.**

A material that is biocompatible but not biostable may initially be safe for use in the body, but it may eventually break down or degrade over time. This can lead to the release of harmful substances into the body, which can cause adverse reactions.

For example, a metal implants that is biocompatible may initially be safe for use in the body. However, the metal may eventually corrode or wear away over time. This can lead to the release of metal ions into the body, which can cause inflammation

* **what are microbumps**