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PowerMX: A versatile signal processing platform for the SKA and other applications

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Malta HPSP Conference, October 28-31, 2014

NRC-Herzberg Astronomy Technology Program

Outline

- Overview of the SKA.
- Motivation for PowerMX.
- PowerMX PMX.1 Base Specification.
- Packaging/use examples.
- Application of PowerMX to the SKA.
- Developments and performance.
- Evolving specifications.

Overview of the SKA

- International effort to build the world's largest m/cm-wave radio telescope; 100X more powerful than anything (i.e. the Jansky Very Large Array) that exists today.
  - SKA1 -- ~10% of SKA, currently approaching PDR/costing review.
  - SKA2 – 100% SKA, next decade.
  - www.skatelescope.org

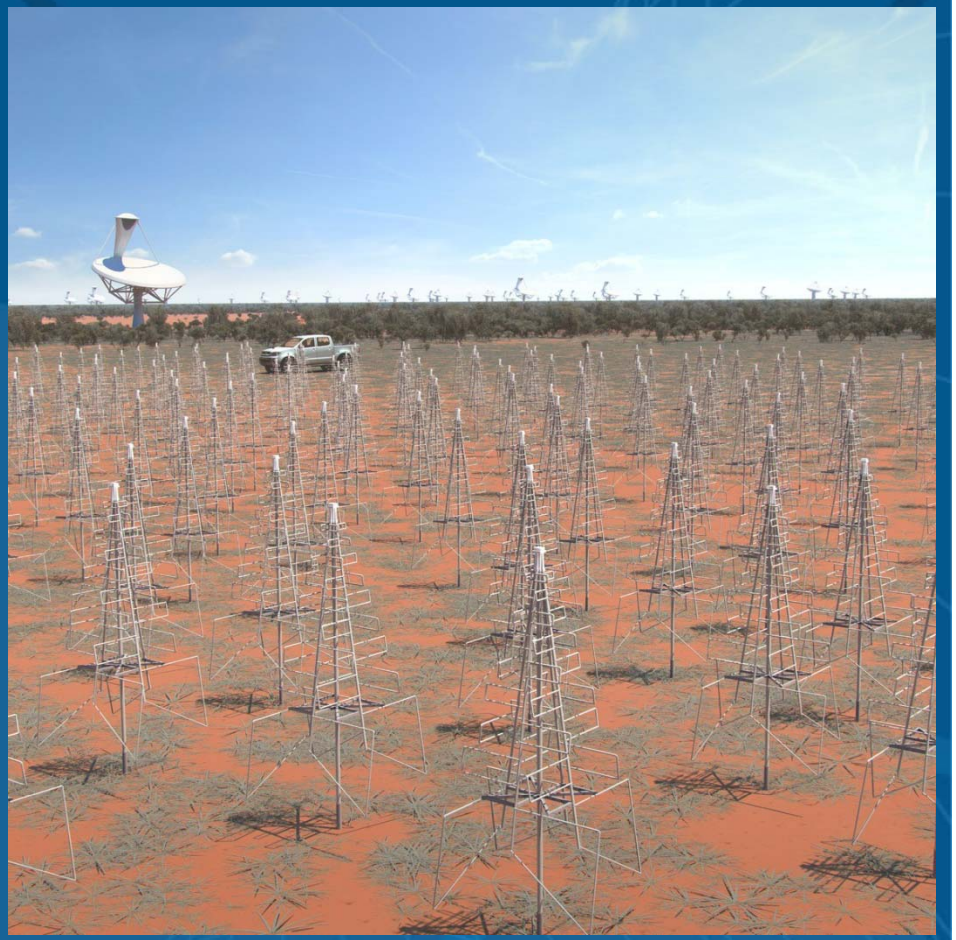
- 3 telescopes currently being considered:
  - Low-frequency aperture array ("SKA1-Low"). Western Australia.
  - Mid-frequency dish array ("SKA1-Mid"). Karoo, South Africa
  - Survey dish array ("SKA1-Survey"). Western Australia.

Jansky Very Large Array; credit: NSF/AUI/NRAO

Overview of the SKA

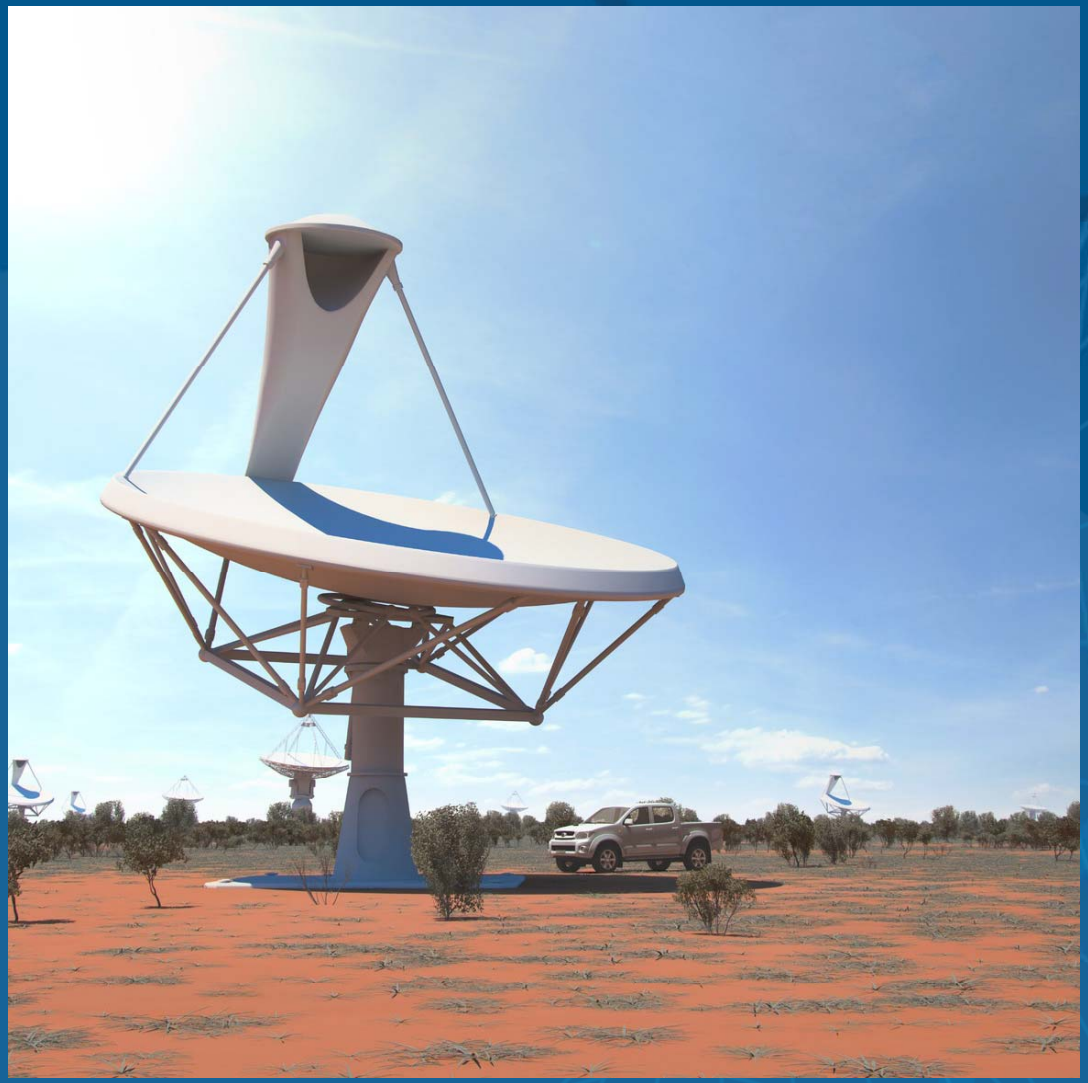
- SKA1-Low:
  - ~256k cross-dipole elements, 300 MHz BW/pol, arranged as 1024 stations of 256 elements each.
  - Each station requires beamforming.
- SKA1-Mid:
  - 254, 15 m dishes (190 SKA1, 64 “MeerKAT”).
  - 5 bands, up to 5 GHz/pol.
  - Central beamforming for pulsar searching. Pulsar searching/timing.
- SKA1-Survey
  - 96, 15 m dishes (60 SKA1, 36 “ASKAP”).
  - Phased-Array feeds with 36 dual-pol beams for fast imaging.
  - PAF: ~192 receivers form 36 dual-pol beams, 500 MHz/pol’n.

SKA1-Low: MRO site, Western Australia



SKA1-Mid: Karoo desert, South Africa

SKA1-Survey: MRO site, Western Australia



DVA1—full SKA1 Dish prototype, Penticton, BC, Canada

Motivation for PowerMX

- The SKA1 project is divided into several major components referred to as “Elements”.
- The Central Signal Processing (CSP) Element is where signals from all receptors are “combined” (correlation, beamforming, pulsar search+timing) to produce data ready for image processing and further scientific analysis.
- This is a major real-time DSP computational task, but upcoming 14 nm tri-gate and HMC is making it a much easier task than before.
  - Note that SKA2—full SKA—will be a 100X to 3000X larger task!

Motivation for PowerMX

- Total data rate into the SKA1-Mid CSP-correlator is ~25 Tbps.
  - Total processing is ~3-5k TMAC/s.

- We (engineers in the CSP consortium) are tasked with developing and costing designs now, for production and deployment in the 2018-2022 timeframe.
  - Anything we do now may be obsolete requiring expensive re-design…but limited funds and resources.
  - Is there a way to minimize the cost of the next design cycle?

Motivation for PowerMX

- Rather than develop a board, or develop to an existing industry standard that is looking old or doesn't have the performance/ scalability/capability we need…

- Develop a *specification* which has features that meet our needs, with lots of I/O and performance.
  - Factor out, as much as possible, those bits that can survive technology generations…leaving the minimum to develop on the next generation.
  - Enough specification for compatibility, enough room for innovation.
  - Of course, it has a form factor and connectors...and every such technology specification eventually maxes out and needs updating…maybe a fool's game?
  - *Provide a platform to facilitate access/connectivity of FPGAs.*
  - Needs significant performance to have any decent lifetime.

PowerMX PMX.1 Base Specification

- See www.powermx.org for the full PMX.1 Base Spec, open, public, freely available for use.
- '**POWERMX**' is a registered prohibited TM in Canada.

- Basic concept:
  - Motherboard contains M&C and power infrastructure…1-4 sites.
  - Processing (PMXM) and I/O (PMX_IOC) mezzanine boards.
  - All SERDES connectivity…
  - Use 4 mm stack FCI Meg-Array (400, 100 pin) connector for reliability and 28G/pair performance.
  - Full 4-site motherboard: 384 serial I/Os (@28G ea ~= 10.75 Tbps)

- Precipitated from Aug 28-30, 2013 mtg—16 participants, 9 organizations.
  - Not everyone is convinced this is the way to go…
  - Currently "Preliminary"…undergoing H/W design/test.

PowerMX PMX.1 Base Specification

- List of contributing authors (attendees at Aug/2103 mtg):

  Andre Gunst – Astron, Netherlands
  Gjis Schoonderbeek – Astron, Netherlands
  Francois Kapp – SKA-SA, South Africa
  Jason Manley – SKA-SA, South Africa
  Henno Kriel – SKA-SA, South Africa
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  Bruce Mellado Garcia – CERN
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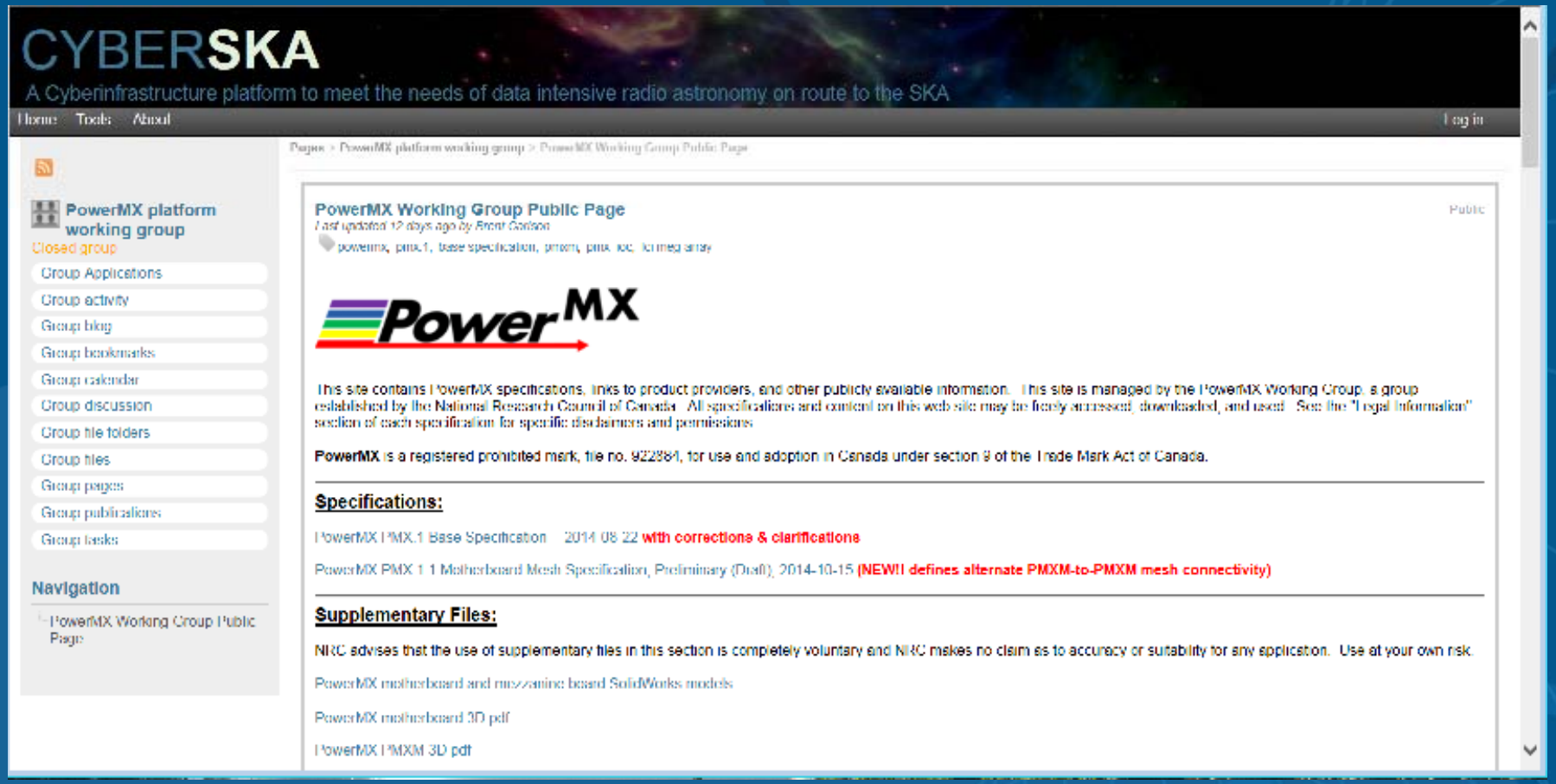
  Andrew Ensor – AUT Auckland, NZ
  Richard Oberland – Uman, SADT, UK
  Chris Shenton – AASL, UK
  Kristian Zarb-Adami – Oxford U, UK
  Rob Halsall – STFC-RAL, UK
  Brent Carlson – NRC-Herzberg, Canada


CYBERSKA
A Cyberinfrastructure platform to meet the needs of data intensive radio astronomy on route to the SKA
Home Tools About
Log in
PowerMX platform working group
Closed group
Group Applications
Group activity
Group blog
Group bookmarks
Group calendar
Group discussion
Group file folders
Group files
Group pages
Group publications
Group tasks
Navigation
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PowerMX
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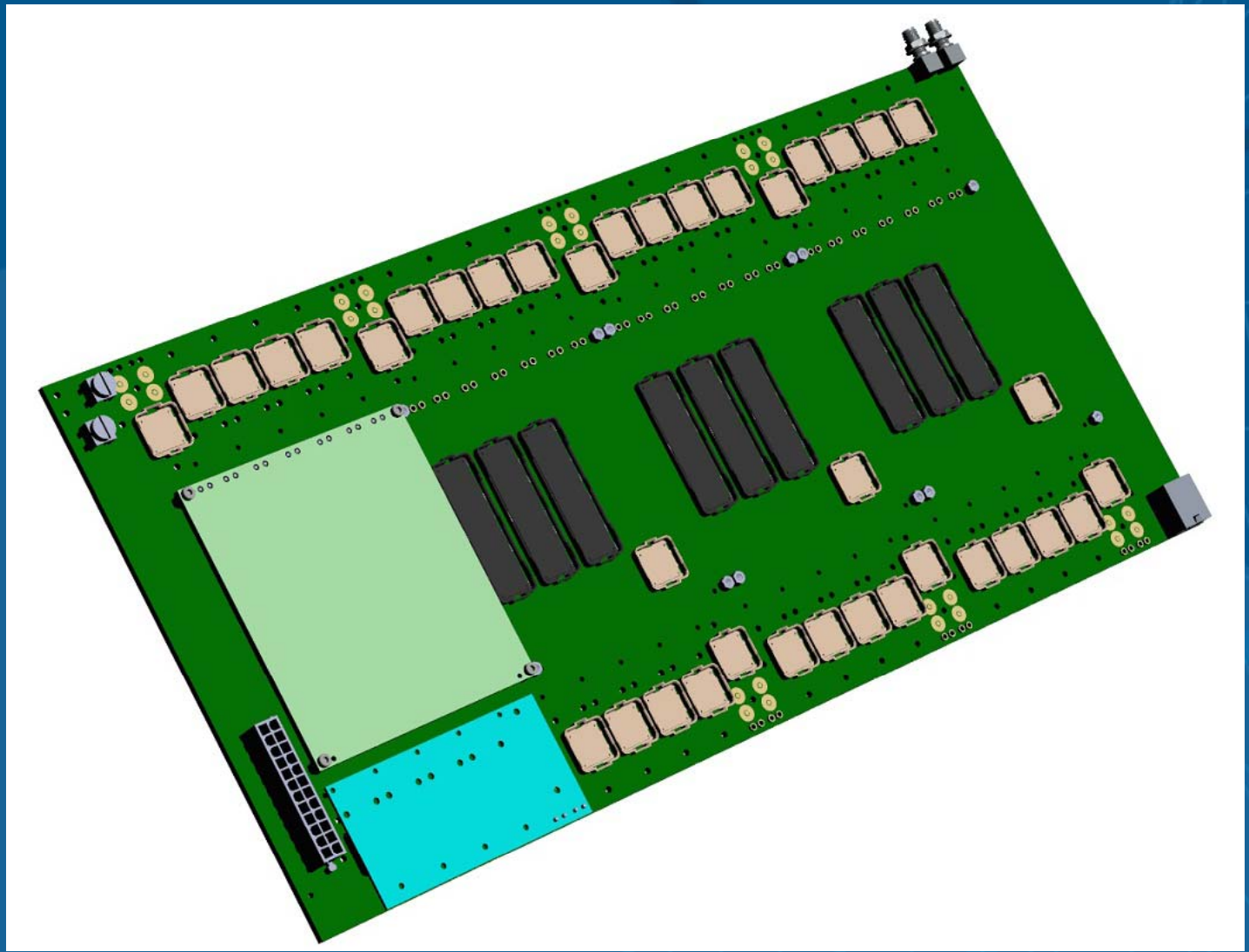
PowerMX is a registered prohibited mark, file no. 922881, for use and adoption in Canada under section 9 of the Trade Mark Act of Canada.
Specifications:
PowerMX PMX-1 Base Specification 2014 08 22 with corrections & clarifications
PowerMX PMX 1.1 Motherboard Mesh Specification, Preliminary (Draft), 2014-10-15 (NEW!! defines alternate PMXM-to-PMXM mesh connectivity)
Supplementary Files:
NRC advises that the use of supplementary files in this section is completely voluntary and NRC makes no claim as to accuracy or suitability for any application. Use at your own risk.
PowerMX motherboard and mezzanine board SolidWorks models
PowerMX motherboard 3D pdf
PowerMX PMXM 3D pdf

PowerMX PMX.1 Base Specification



PowerMX PMX.1 Base Specification

PowerMX
PMX.1
Base Specification

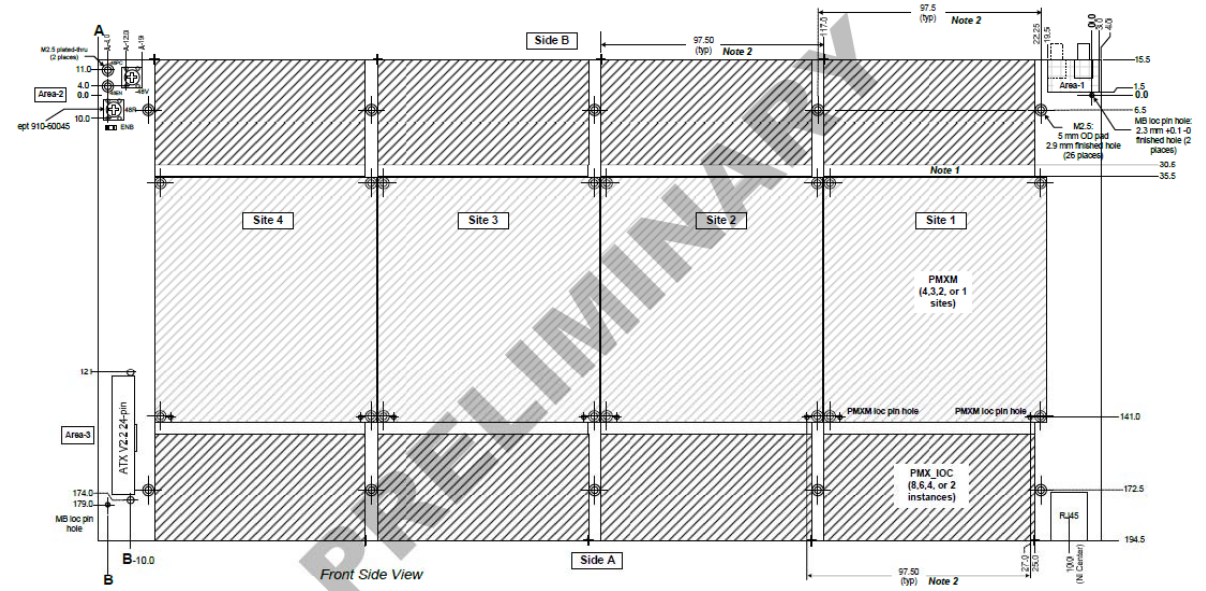


Figure 5-1 PowerMX motherboard dimensions. Coordinates A and B depend on the number of sites provided and are defined in Table 5-1.

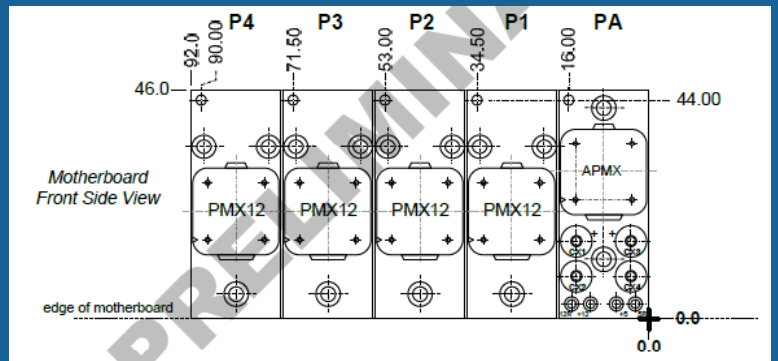


Figure 5-3 PMX_IOC footprint on motherboard showing key coordinates and nomenclature. Note that APMX and PMX12 footprint dimensions are 18.0 mm x 46.0 mm with an 18.50 mm intra PMX_IOC module-to-module pitch.

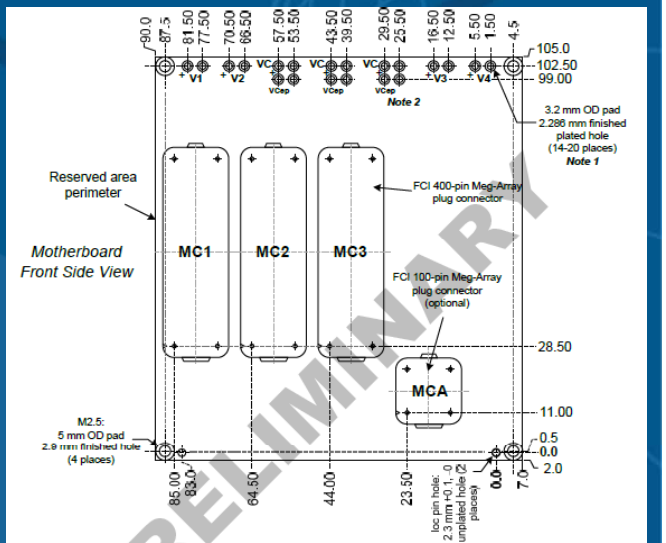


Figure 5-6 PMXM footprint on the motherboard. The "reserved area perimeter" indicates the perimeter within which only those components shown in this drawing may be located on the Front Side of the motherboard.

PRELIMINARY

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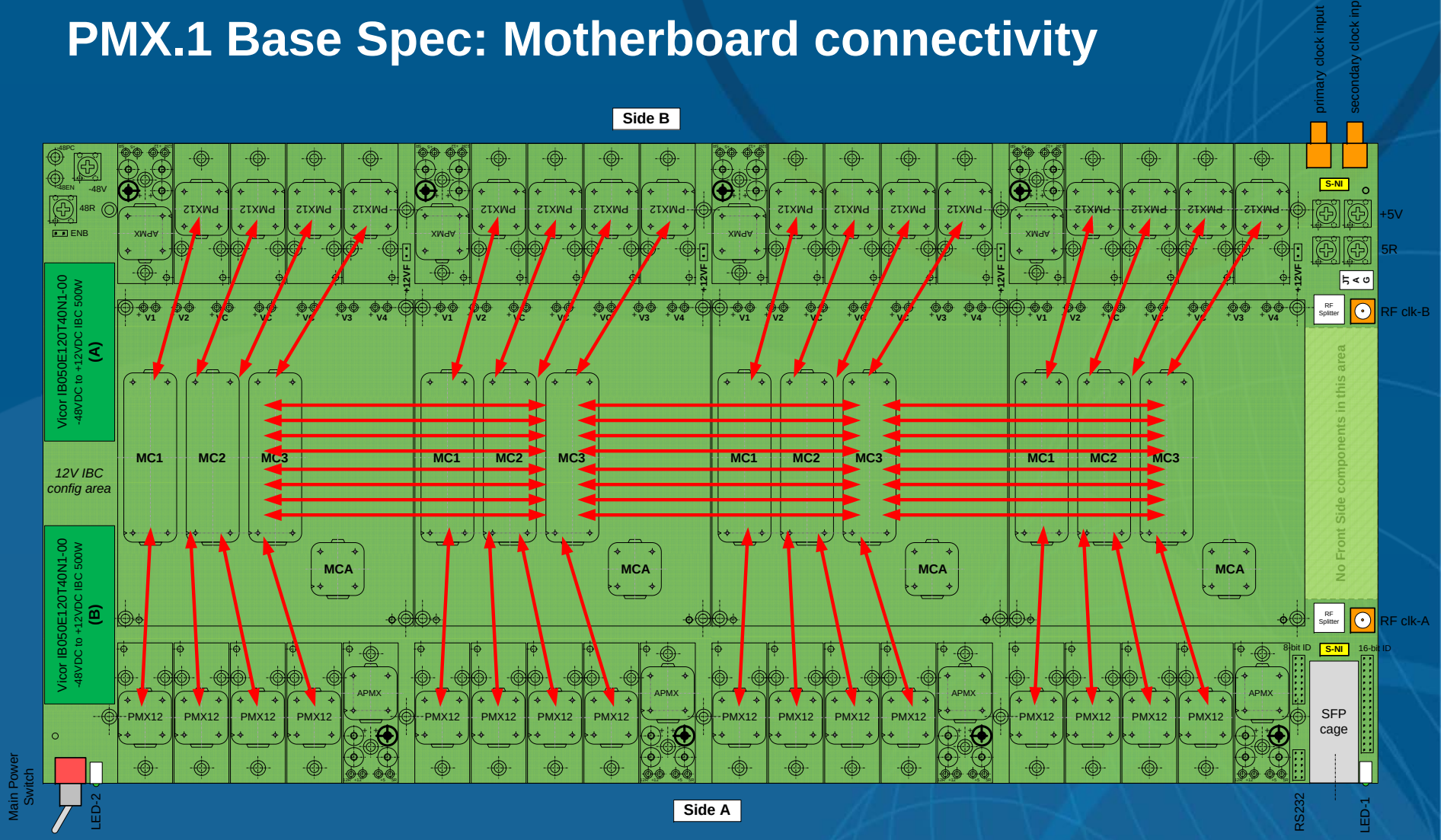
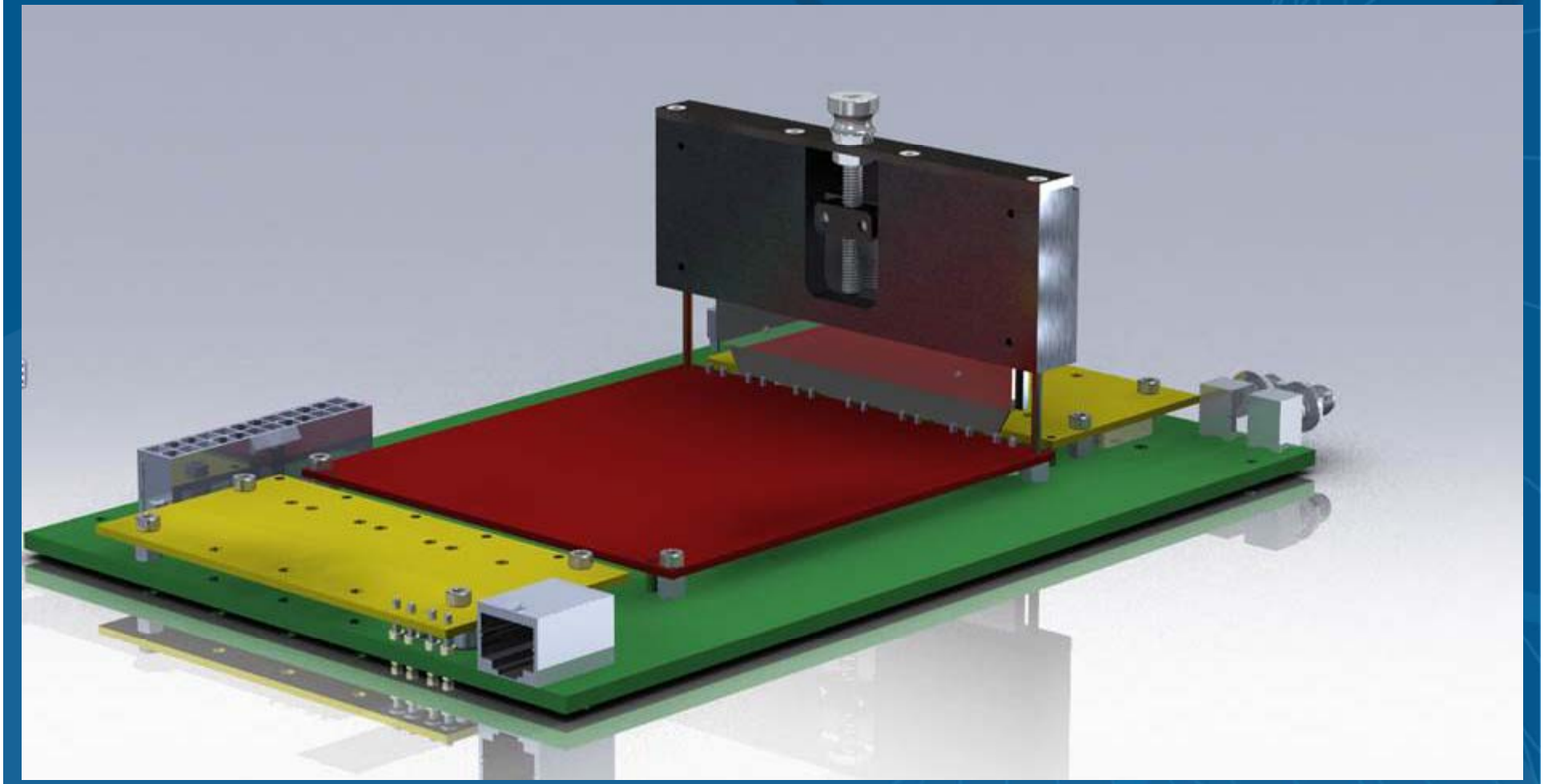
PMX.1 Base Spec: Motherboard connectivity



PMXM module extractor tool

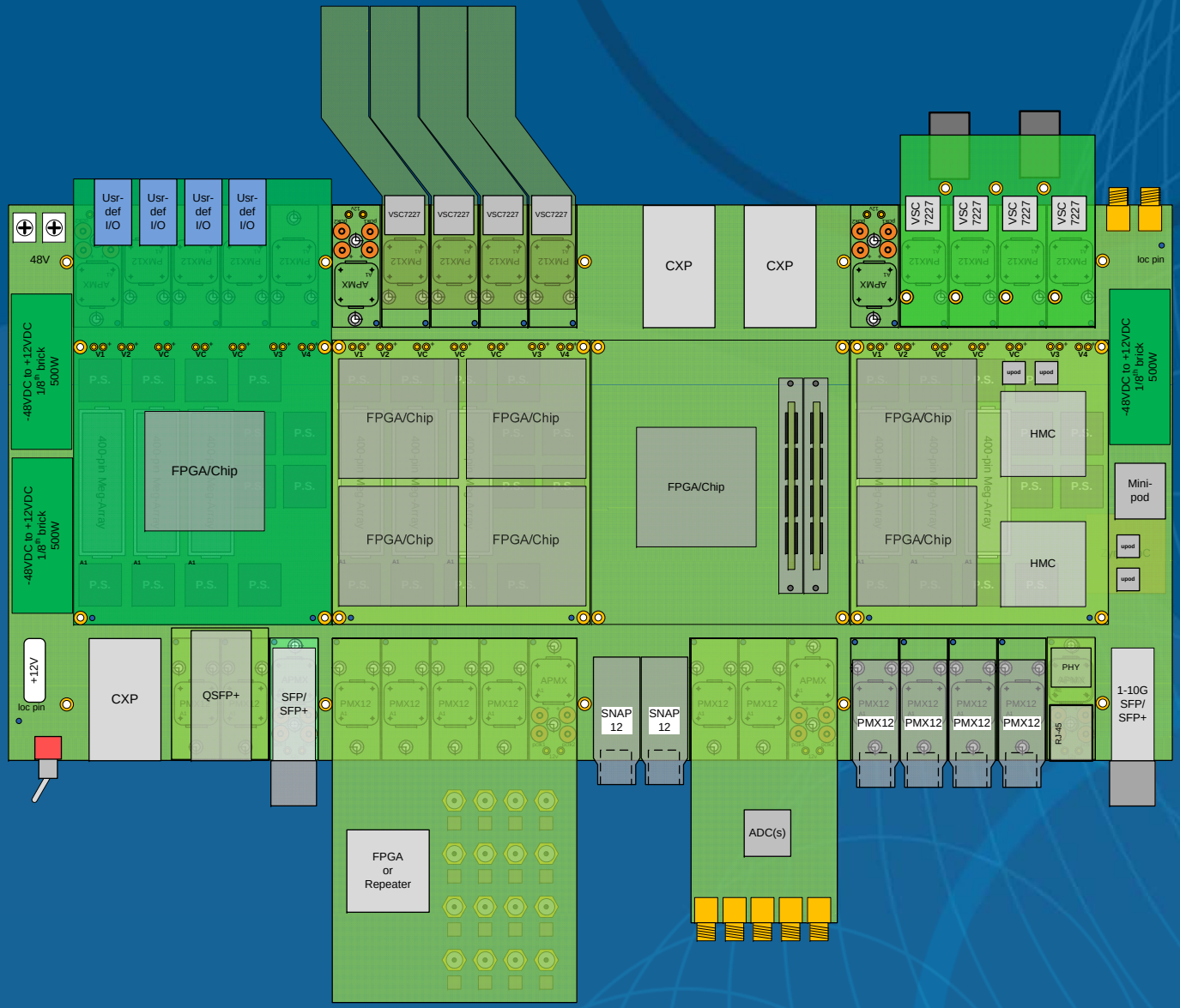


PowerMX PMX.1 Base Specification

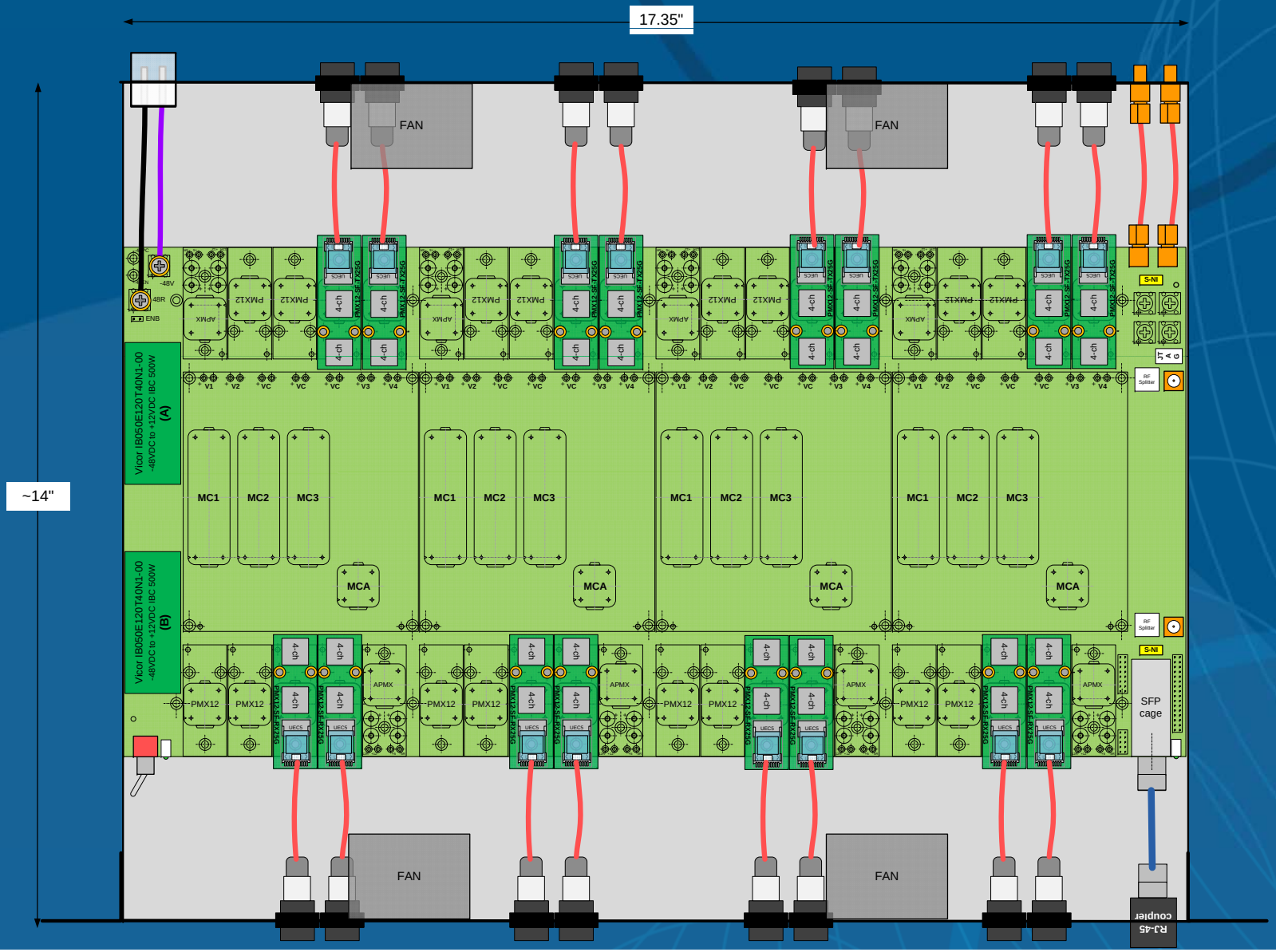
- Includes PA/QA requirements, reliability reporting…and auditing.
  - Establishes base level of quality and reliability reporting.

- Also includes description of plan/vision for more layers, defined in other specification documents:
  - Other H/W layers (PMX.1.x)
    - E.g.: “full duplex spec”, “standard I/O form factor spec”…
  - SMC: Supervisory M&C (PMX.2.x)
  - AMC : Application M&C (PMX.3.x)
  - PMX.4.x: Application F/W
  - PMX.5.x: Applications…

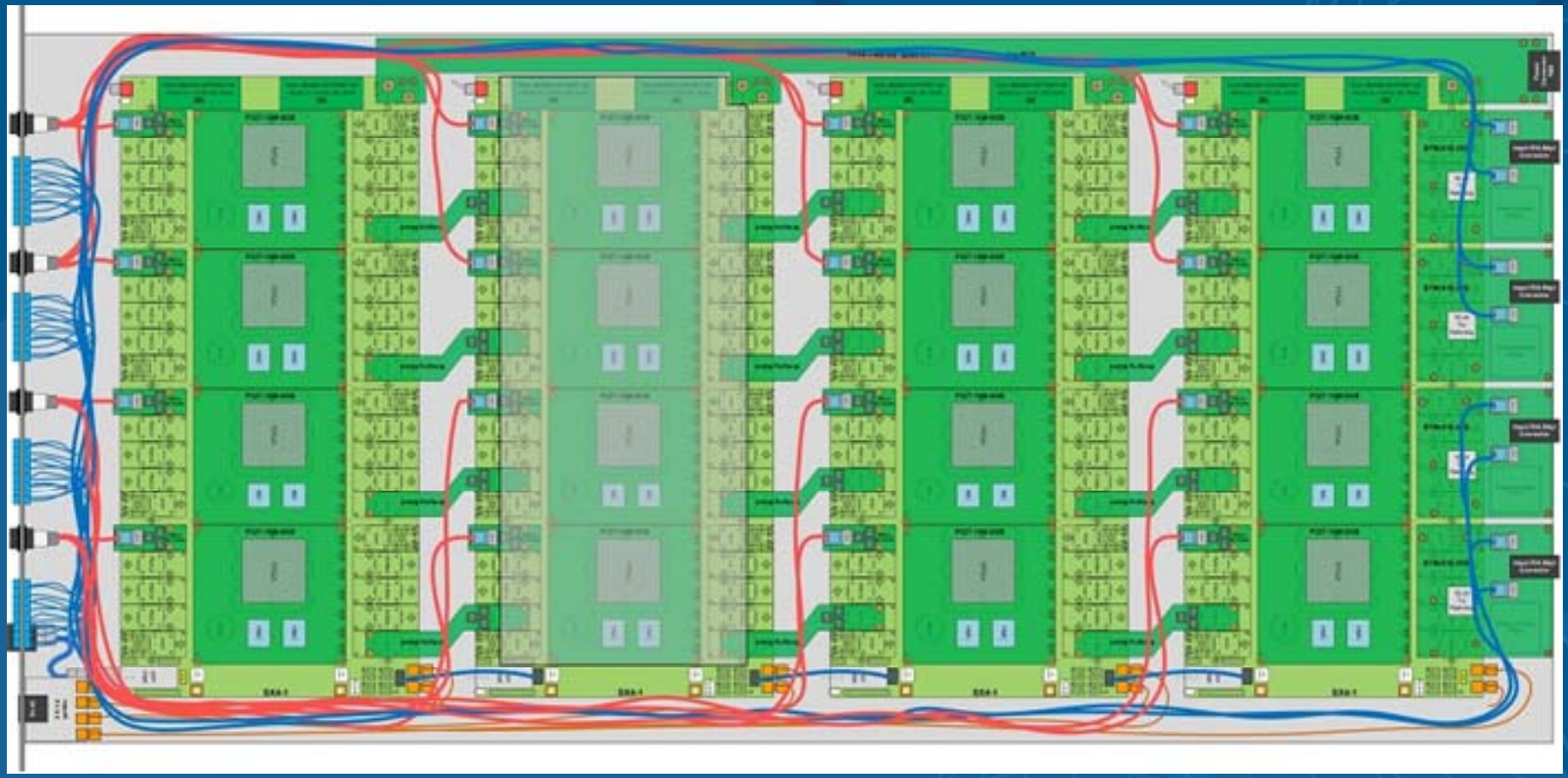
Packaging/Use Examples: Collage of possibilities



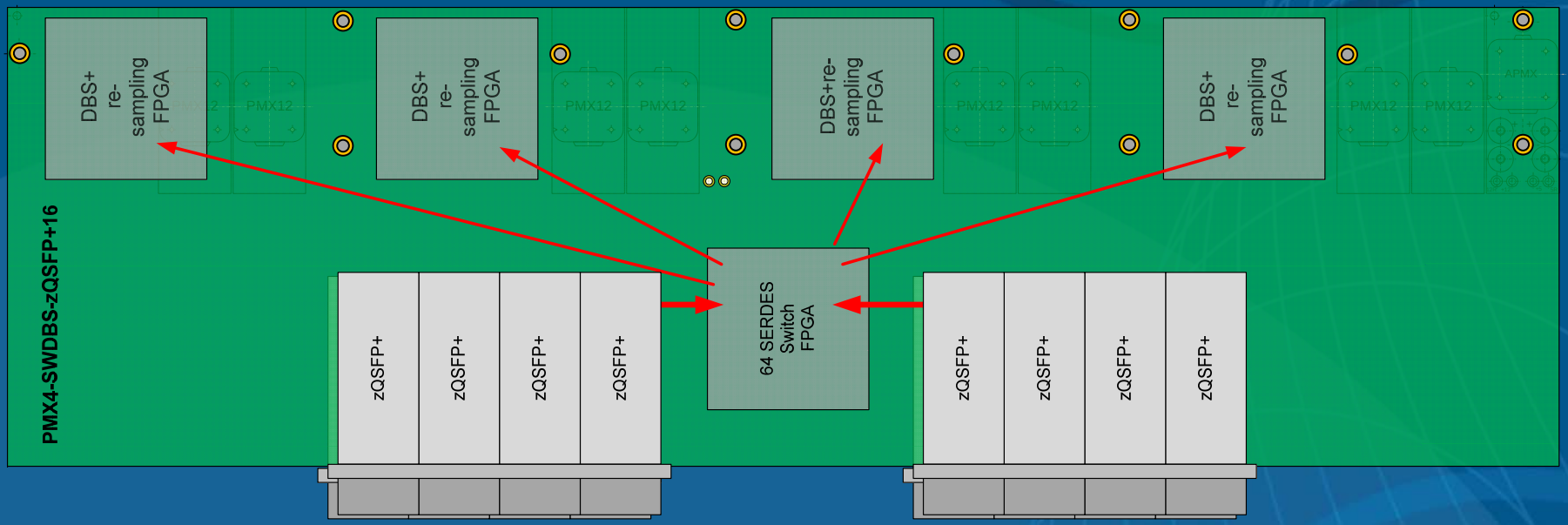
Packaging/Use Examples: Pizza box

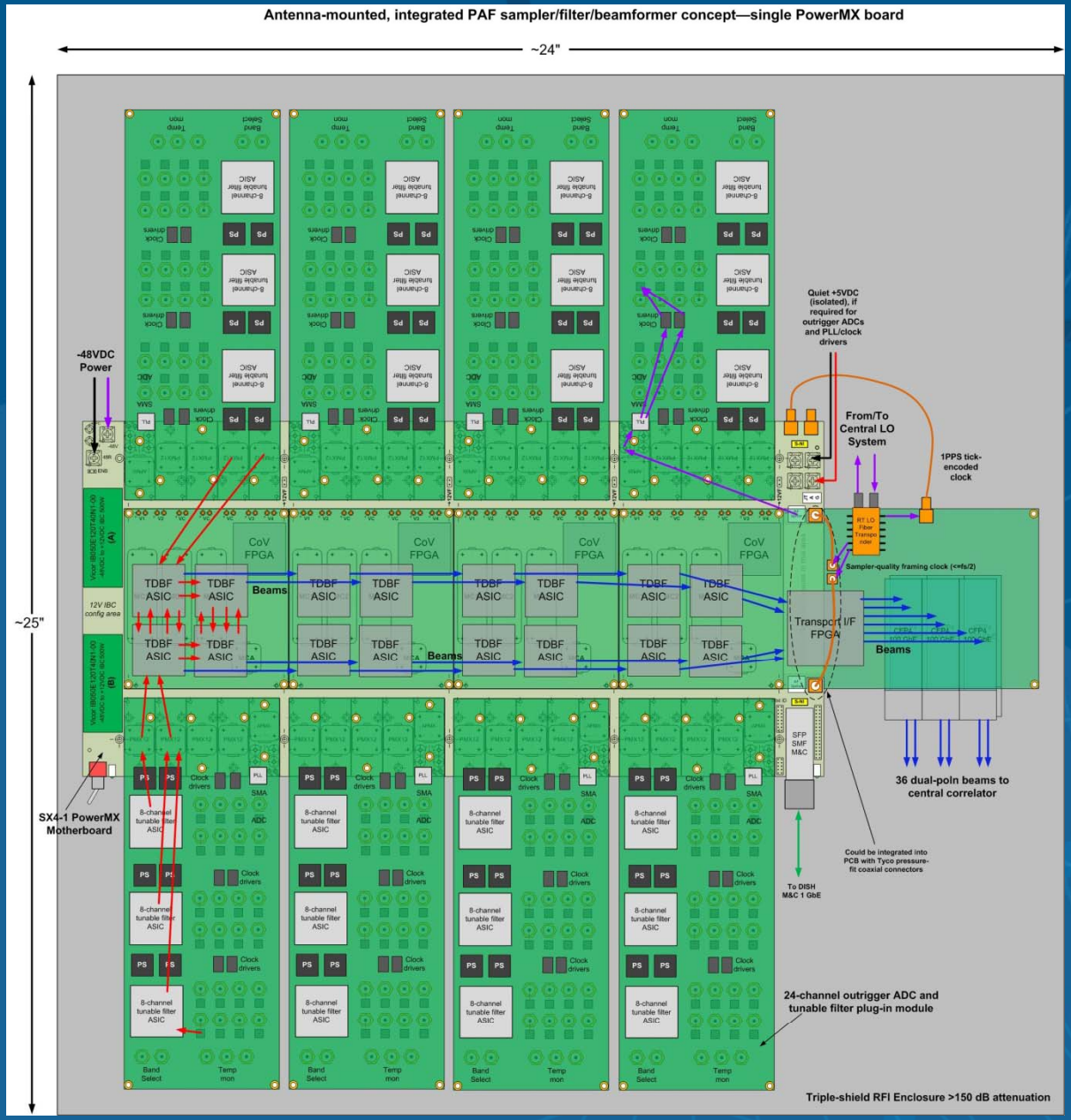


Packaging/Use Examples: Multi-board blade



Packaging/Use Examples: complex multi-site PMX_IOC module

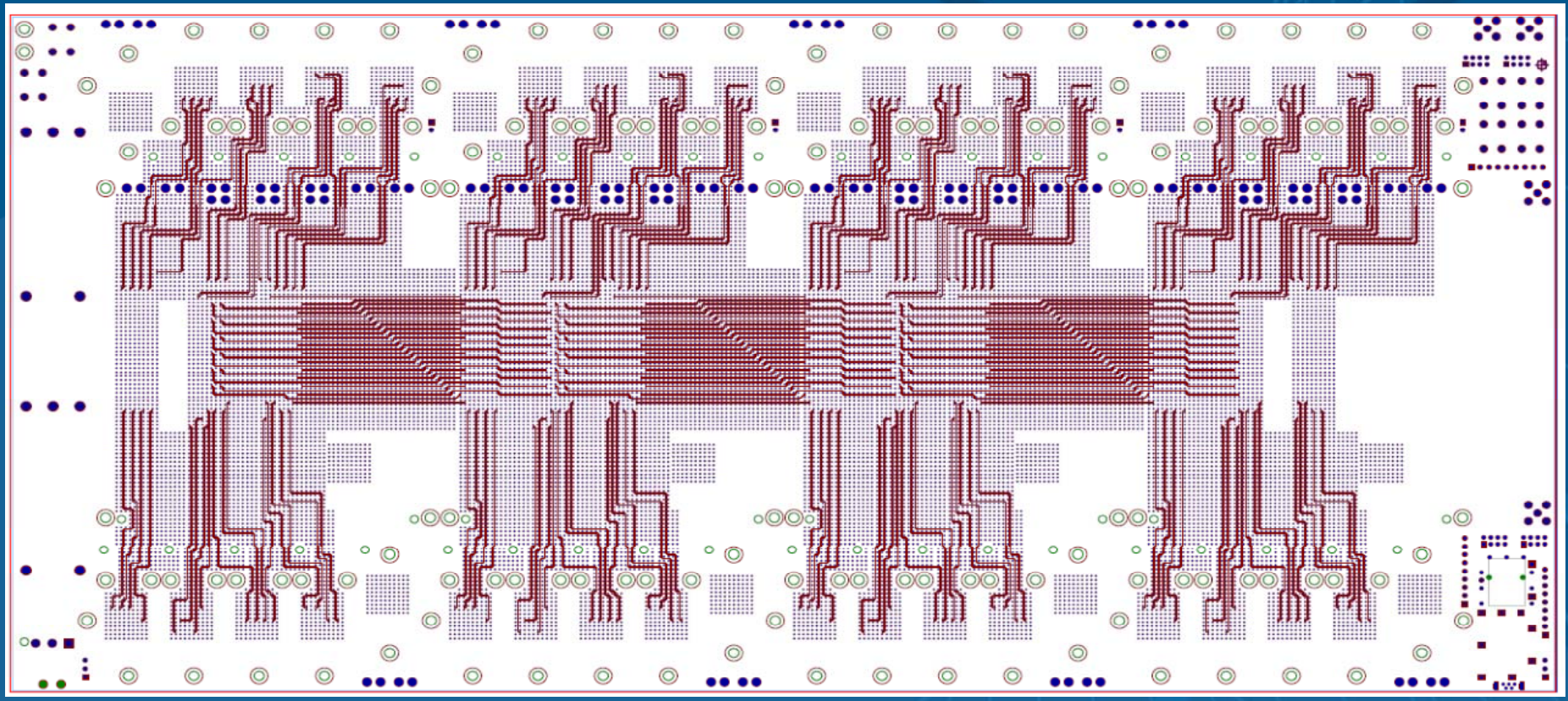



Antenna-mounted, integrated PAF sampler/filter/beamformer concept—single PowerMX board
~24"
~25"
-48VDC Power
Quiet +5VDC (isolated), if required for outrigger ADCs and PLL/clock drivers
From/To Central LO System
1PPS tick-encoded clock
Sampler-quality framing clock (<=fs/2)
CoV FPGA
TDBF ASIC
Beams
Transport I/F FPGA
SFP SMF M&C
36 dual-poln beams to central correlator
Could be integrated into PCB with Tyco pressure-fit coaxial connectors
To DISH M&C 1 GbE
SX4-1 PowerMX Motherboard
12V IBC config area
8-channel tunable filter ASIC
Clock drivers
PS
PLL
SMA
ADC
Band Select
Temp mon
24-channel outrigger ADC and tunable filter plug-in module
Triple-shield RFI Enclosure >150 dB attenuation

Application of PowerMX to the SKA

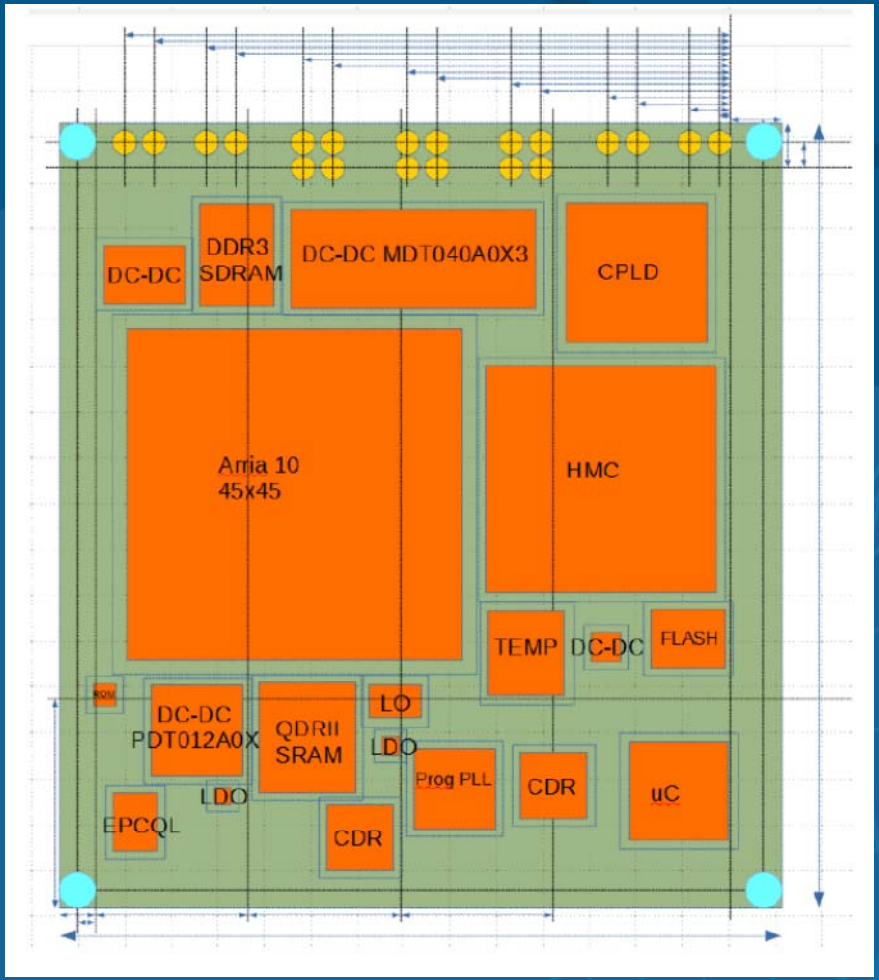
- Many areas where it *could* potentially be used:
  - Pizza box with fiber and/or complex I/O module I/O…ready to plug in PMXM and PMX_IOC modules.
  - **Multi-board blades in blade/shelf (SKA1-MID correlator concept has 16 F-blades, 16 X-blades…for total of 512 FPGAs connected by mesh backplane).**
  - Single 4-site motherboard SKA1-Low station beamformer with 8 x 32-channel A/D sampling I/O boards, PMXM beamforming boards.
  - Single 4-site motherboard SKA1-Survey PAF beamformer.
  - Pizza box with heterogeneous FPGA/multi-core PMXM as Science Data Processor (SDP) accelerator or main processing node. THIS IS BY FAR THE BIGGEST PROCESSING PROBLEM IN THE SKA.
    - Green upgrade path…remove PMXM, install new one.

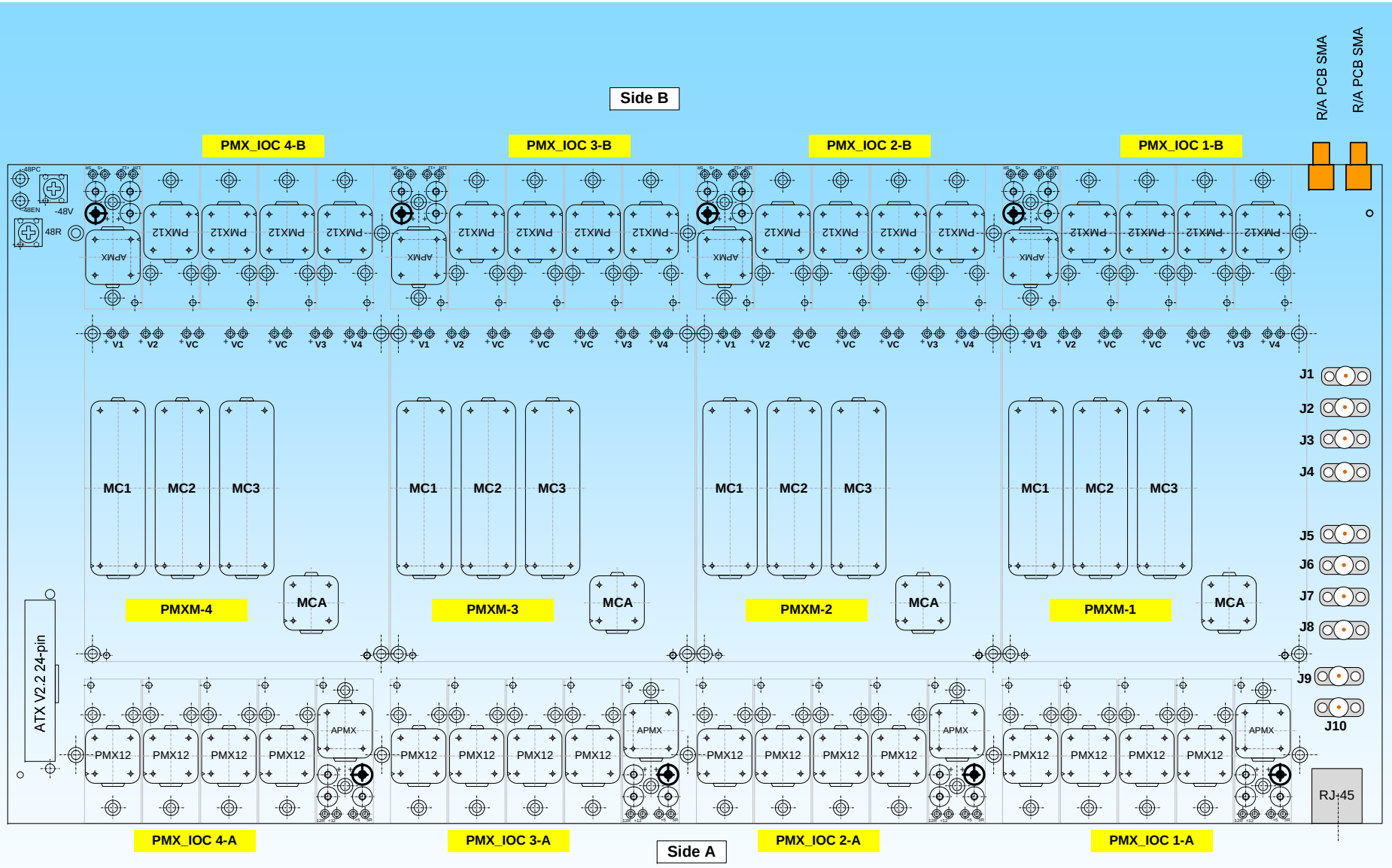
“SX4-1” 4-site 48VDC motherboard under development



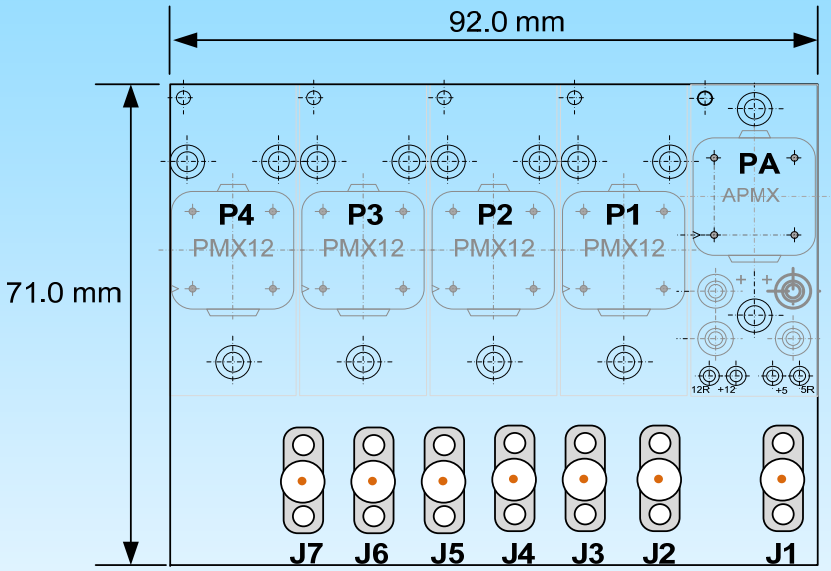
Credit: Heng Zhang, NRC, using Mentor Graphics Expedition PCB

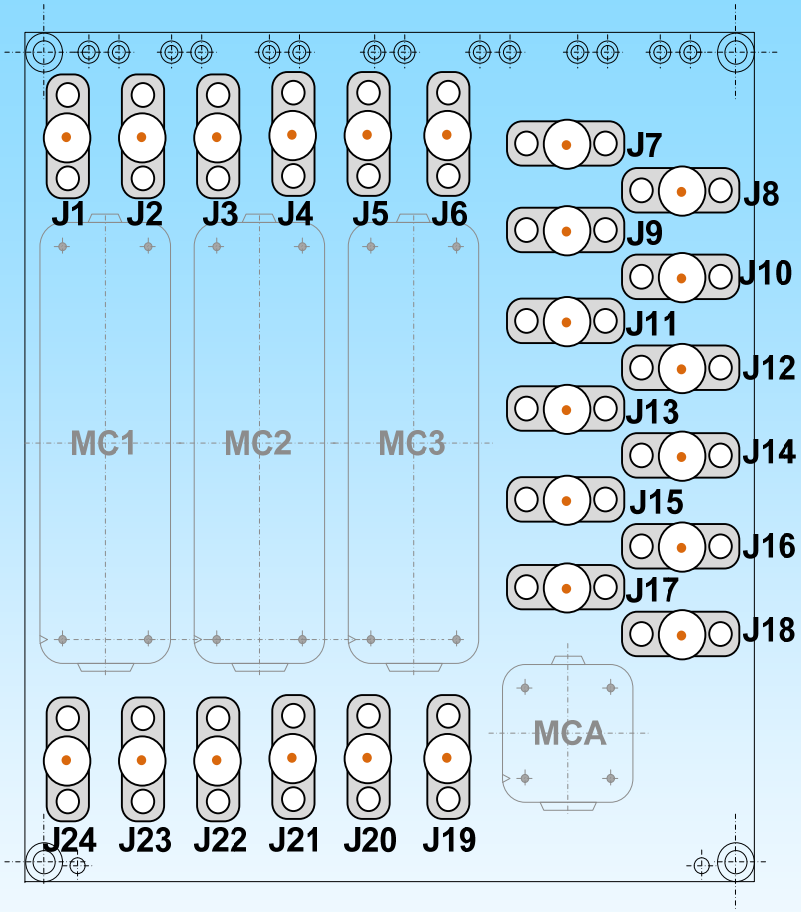
“P32S” module under development (CEI)





“MEX4” Mechanical/Electrical Model: motherboard





Purpose: to check mechanics of mating connectors and verify signalling performance.

“MEX4” Mechanical/Electrical Model: mez cards

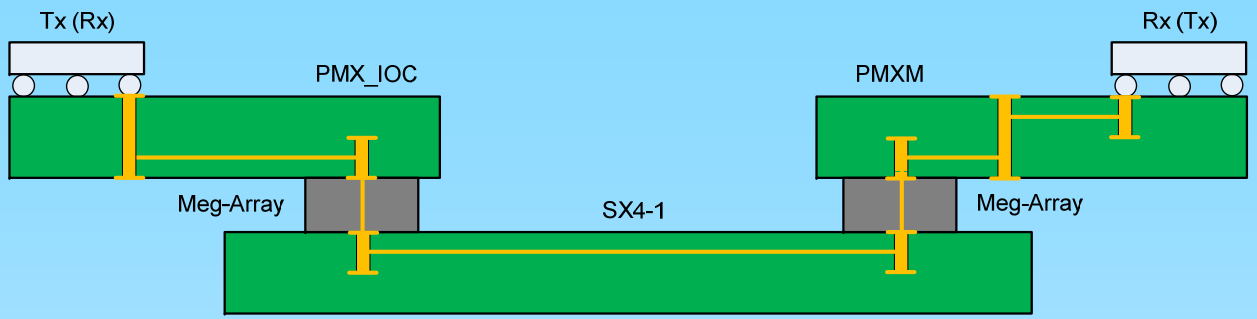
Other developments…way forwad

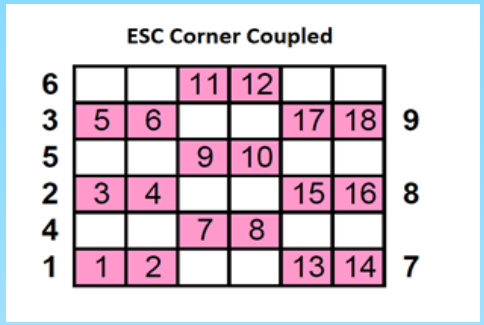
- PMXM active-fan “skiveed” copper heatsink.
- PMXM liquid cooling plate.
- Pizza box packaging/cooling of SX4-1 (TBDev).

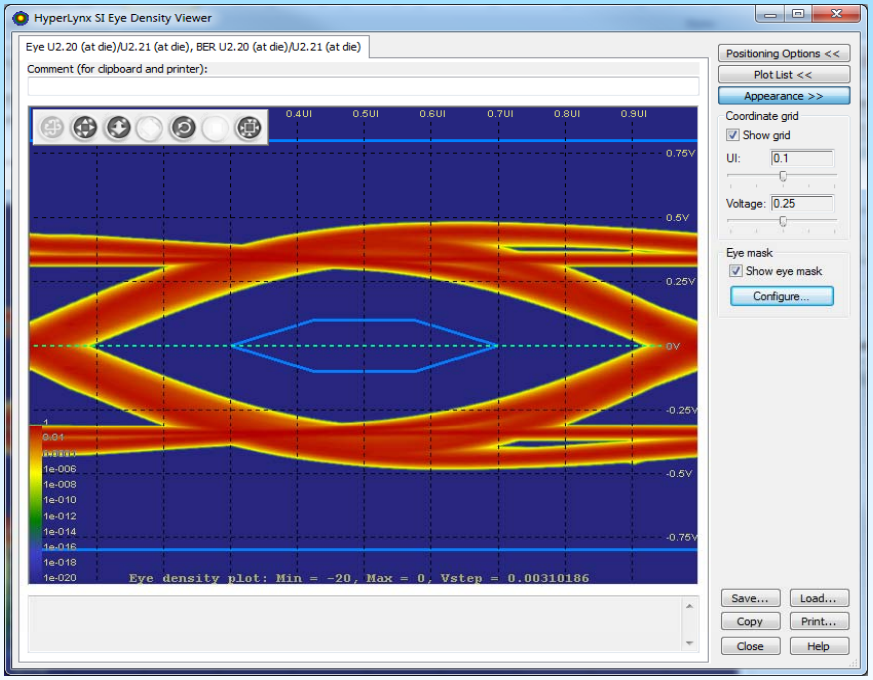
- Plan is that all products/associated products once tested/qualified for production will be listed on the www.powermx.org website with:
  - Product Description/Data Sheet.
  - Ordering information (P/N, options, supplier, MOQs, price).

- Not just NRC-designed products…any “qualified” mfg.
  - Qualification process/providers.

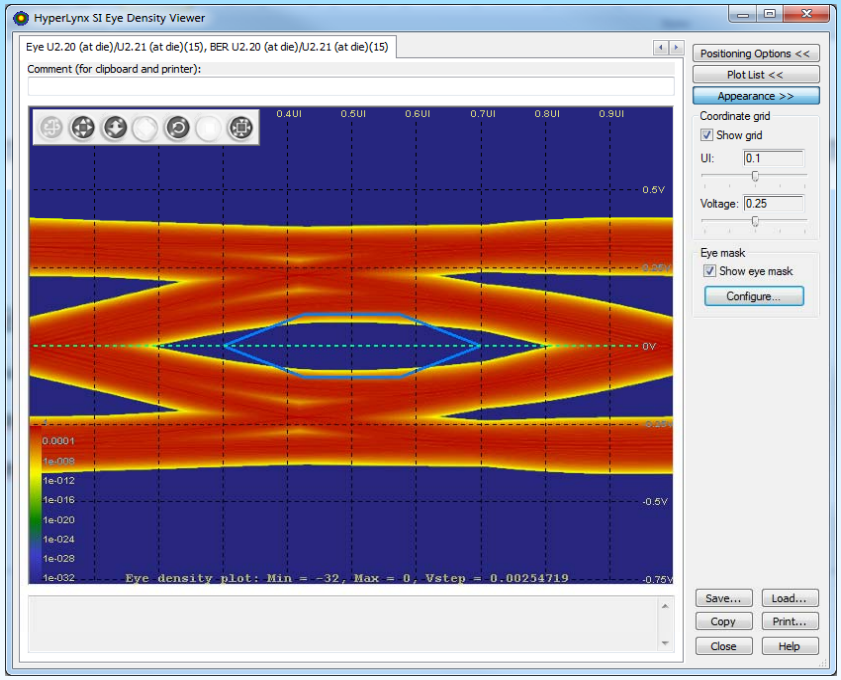
- Plan is to extend to include applications S/W, F/W…





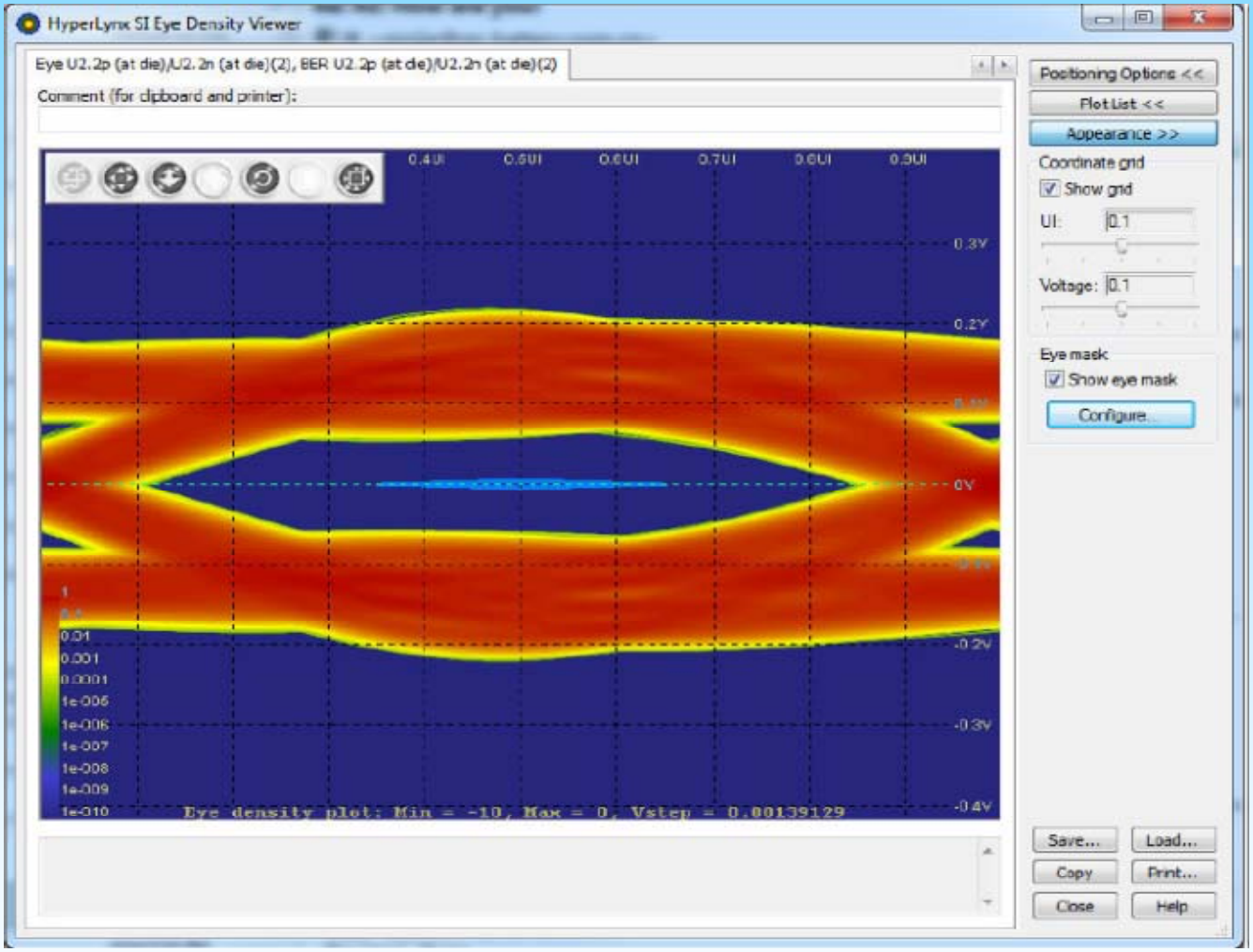


10G eye, Stratix-V GX transceiver, FEXT, Meg-6



28G eye, Stratix-GT transceiver, no Xtalk, Meg-6; 28 nm transcvrs not good enough.

Credit: Heng Zhang, NRC, Mentor Hyperlinks 3D EM modeller and Sim

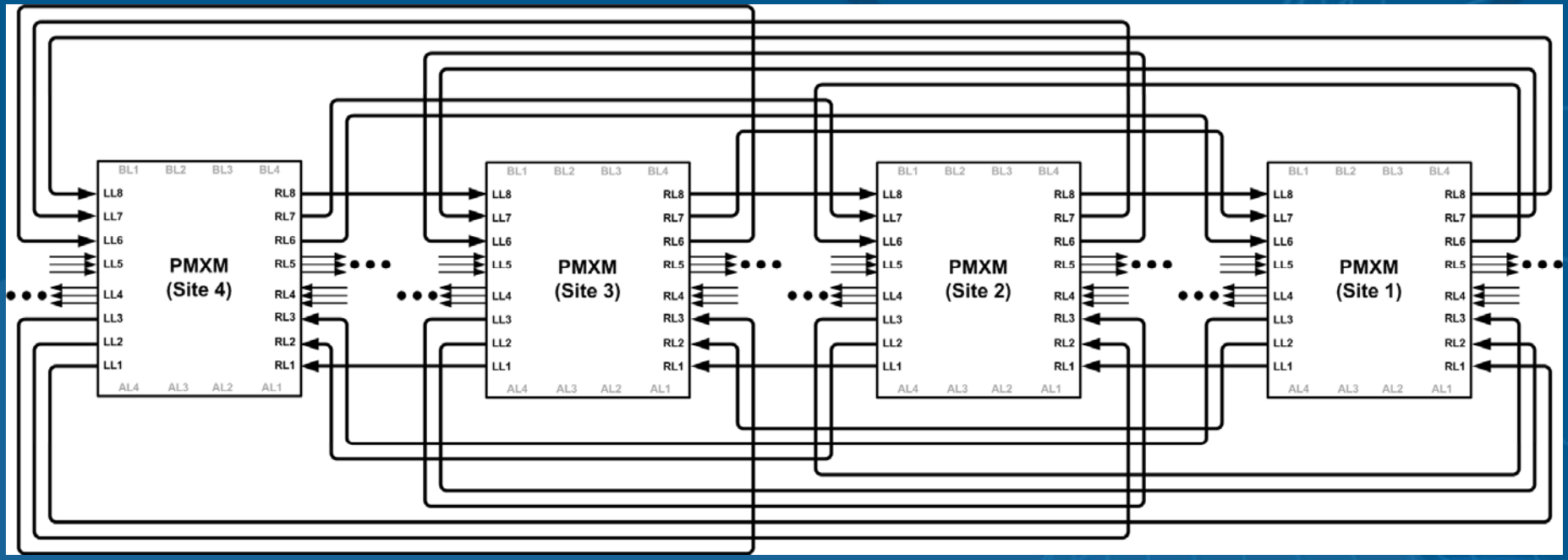


28G eye, Semtech GN2504 retimer, 40” Meg-6 backplane stripline, Molex Impel connectors, FEXT

Evolving Specifications

- The idea is that specifications evolve with time…modelled after IEEE 802.3.
  - Don’t change existing specs…add new ones.
  - Providers can design to any spec, state what specs a product is compliant to.
  - Goal: agile to changing technology, while providing a foundation for compatibility.

PMX.1.1: Motherboard mesh specification



Alternate PMXM-PMXM connectivity.
Allows for scaled capability; hybrid with nearest neighbour connections.
If there can be different flavours of mezzanines, then why not motherboards/connectivity?
Now on powermx.org (Prelim/Draft)

Alternate PMX12: “PMX16” connector definition?

VCC	GND	GND	GND	VCC	VCC	VCC	GND	GND	VCC	1
GND	P0+	P0-	GND	GND	P8+	P8-	GND	GND	GND	2
Tm	GND	GND	P4+	P4-	GND	GND	P12+	P12-	GND	3
GND	P1+	P1-	GND	GND	P9+	P9-	GND	GND	GND	4
VCCm	GND	GND	P5+	P5-	GND	GND	P13+	P13-	+12V	5
GND	P2+	P2-	GND	GND	P10+	P10-	GND	GND	GND	6
SD	GND	GND	P6+	P6-	GND	GND	P14+	P14-	+12V	7
GND	P3+	P3-	GND	GND	P11+	P11-	GND	GND	GND	8
Hn	GND	GND	P7+	P7-	GND	GND	P15+	P15-	Vsen-	9
Fn_E	1W	VCC	VCC	GND	GND	VCC	VCC	VCC	Vsen+	10
A	B	C	D	E	F	G	H	J	K	

Also, requires new PMXM-PMXM connectivity definition. For more I/O intensive applications…but the numerology still works out nicely (i.e. 64 PMXM-to-PMXM connections per PMXM site)

A next generation/alternate connector?

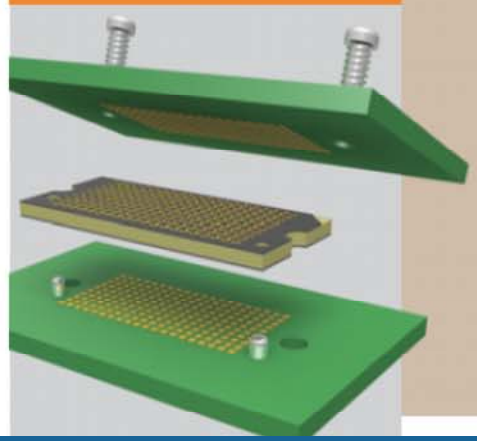
ULTRA LOW PROFILE MICRO ARRAYS

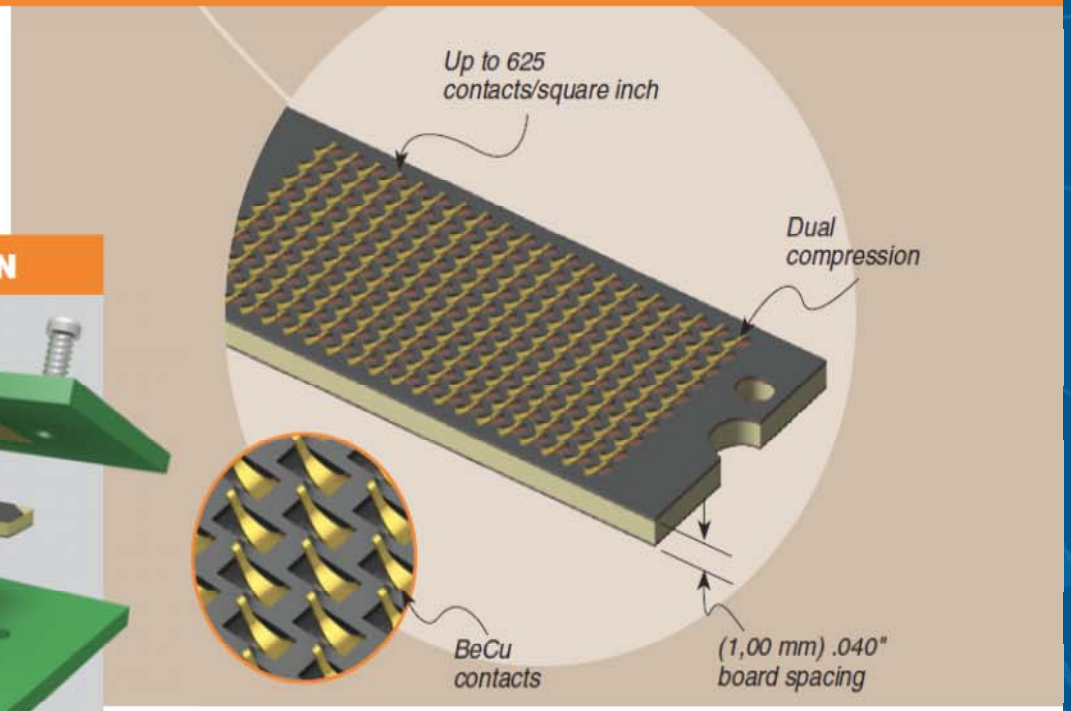
SPECIFICATIONS

For complete specifications and recommended PCB layouts see www.samtec.com?ZA1

Insulator Material:
FR4
Contact Material:
BeCu
Plating:
Au over 50µ" (1,27 µm) Ni
Operating Temp Range:
-55°C to +125°C
Current Rating:
Testing Now!
RoHS Compliant:
Yes

APPLICATION





Samtec micro-interposer, 4 mm, 1.27 mm, balls one side, “drop-in” replacement for FCI Meg-Array?…solder to mez, motherboard just has pads. Currently investigating feasibility + cost.

Other PMX.1.x Specification ideas

- Full duplex specification.
  - PMX.1 Base Spec. motherboard is agnostic to signal direction.
  - Define signal directions for module compatibility.

- PMX_IOC form factor.
  - PMX.1 Base Spec. places no limits on one dimension of the PMX_IOC module.
  - Define 1, maybe 2 standard form factors with mounting holes for module and enclosure compatibility.
  - Include definition of user faceplate (like FMC).

Review

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- Motivation for PowerMX.
- PowerMX Base Specification.
- Packaging/use examples.
- Application of PowerMX to the SKA.
- Developments and performance.
- Evolving specifications.

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Thank you

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