Data Acquisition on FPGA and direct memory access over PCI Express on MTCA 4 platform used at FLASH

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HELMHOLTZ ASSOCIATION

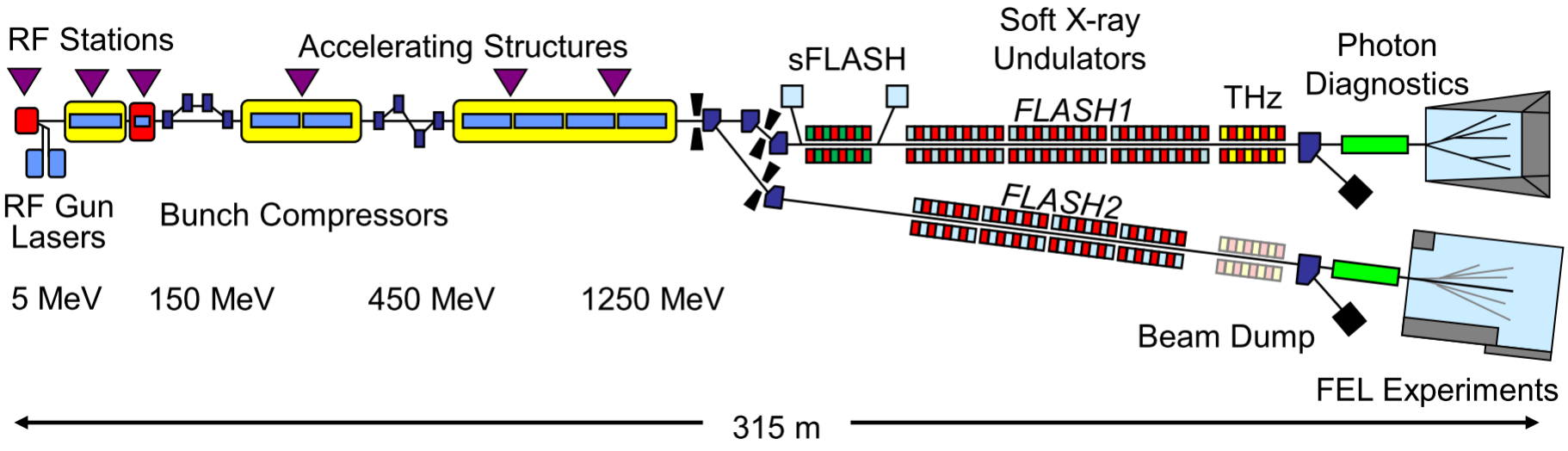
DESY

Outline

- System overview
  - FLASH accelerator
  - MTCA.4 architecture
- LLRF system
  - Implemetation on MTCA.4
  - Controller structure
- LLRF controller firmware on MTCA.4
- DAQ modules
- DMA controller

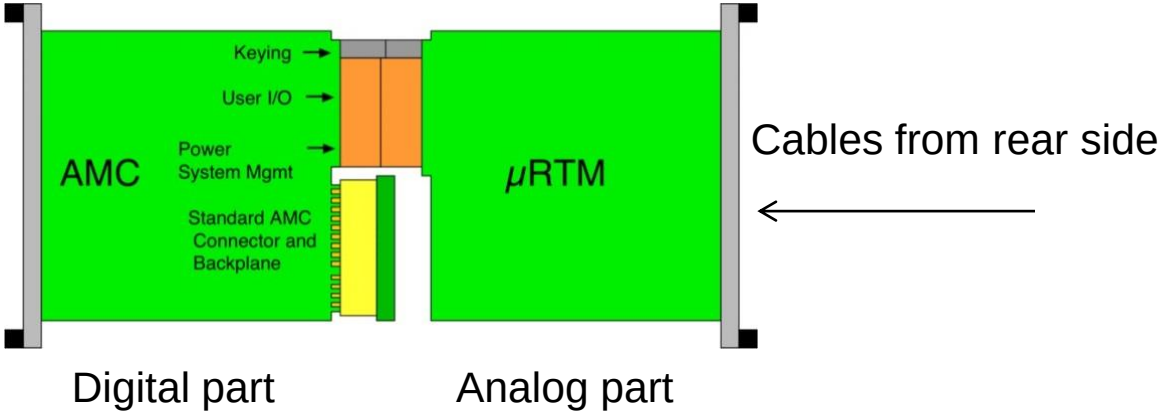
FLASH

- Free-Electron Laser in Hamburg (FLASH)
  - 315 meters long, 6 RF station, 1 normal conducting electron gun, 8 superconducting accelerating modules, 2 undulator sections
- Electron energies between 0.37 and 1.25 GeV
- Producing soft X-ray pulses as short as 50 fsec, for users since 2005
- Test Facility for European XFEL



MTCA.4

- **M**icro **T**elecommunications **C**omputing **A**rchitecture .4 (MTCA.4)
- MTCA.4 specifies extensions to the MicroTCA standard to provide support for I/O bound applications in industry and science.

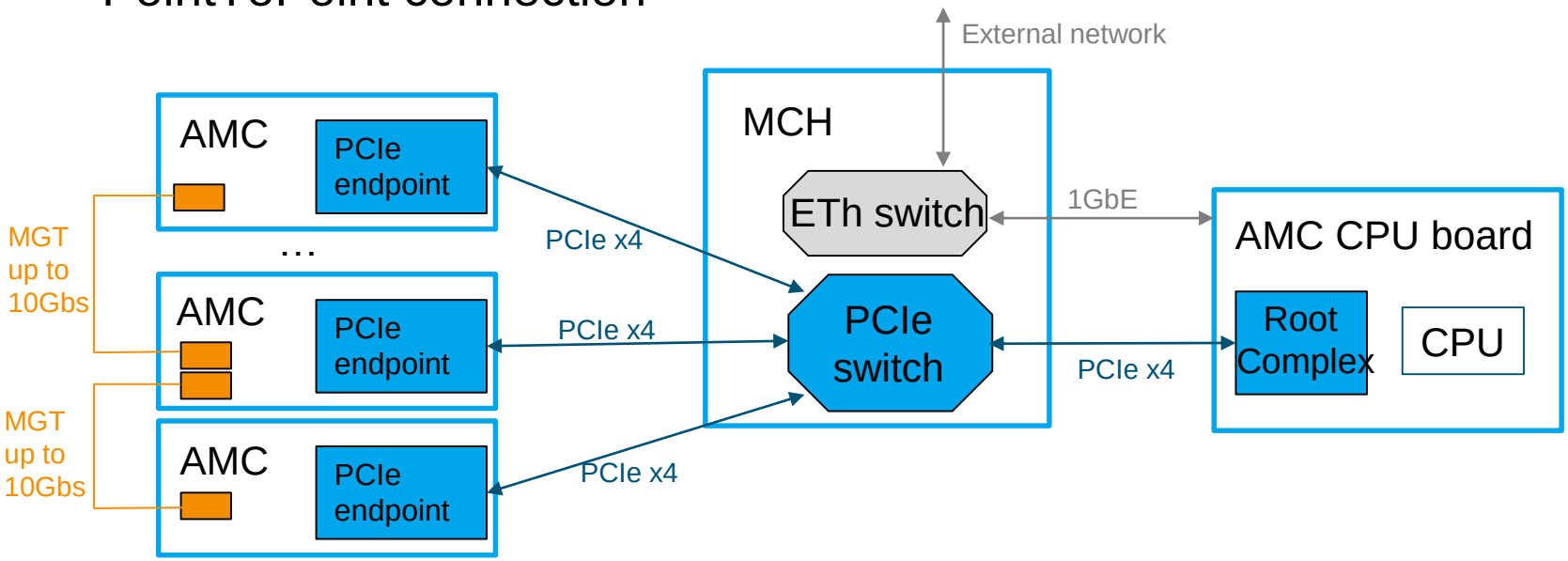


- Redundant power
- Well defined remote management
- High digital performance
  Very low analog distortions
- Modular + Reusability

- Since end of 2013 used for LLRF control system at FLASH accelerator
- Architecture will be used at XFEL

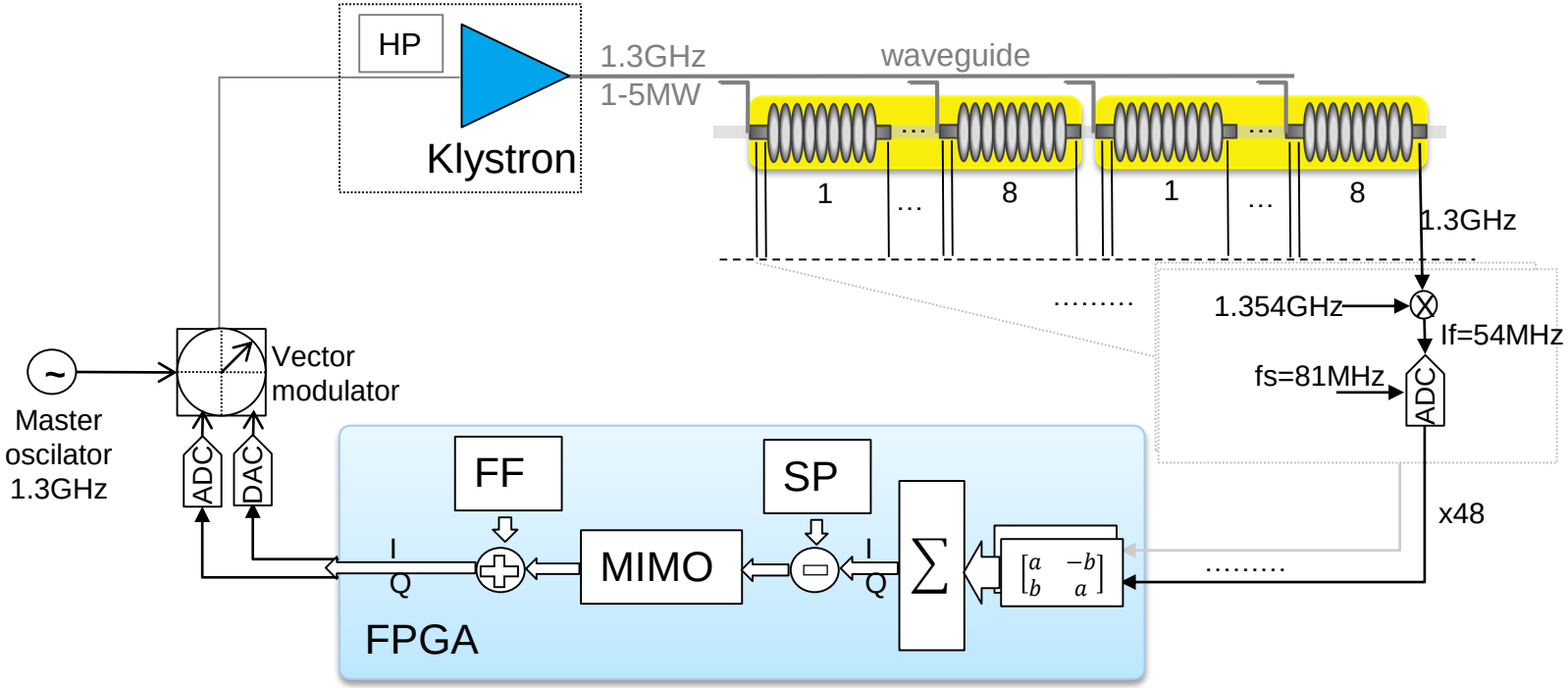
Boards communication

- Management board in crate (MCH) has a Ethernet and PCIe switch, available connection to every slot
- Each board can communicate with CPU using PCIe protocol
- Boards directly can communicate using MGT trnascievers over PointToPoint connection



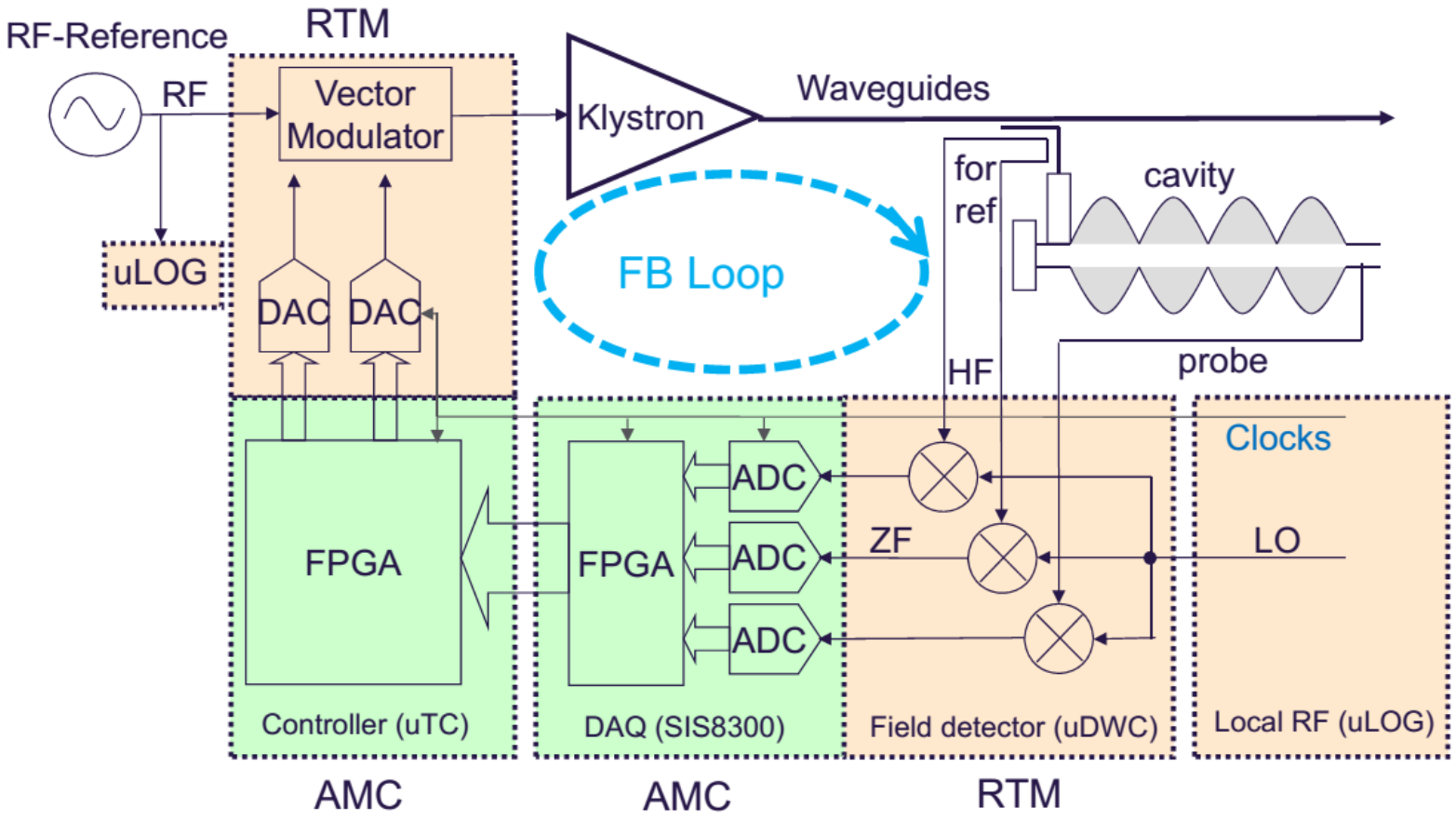
Low-Level Radio Frequency (LLRF) system

- The goal of the LLRF system is to control the accelerating gradient in amplitude and phase for each high power RF station
- Its task is to measure electromagnetic field inside accelerating structures, compare it with a required value, and adjust an output of an RF field source accordingly to ensure required field stability



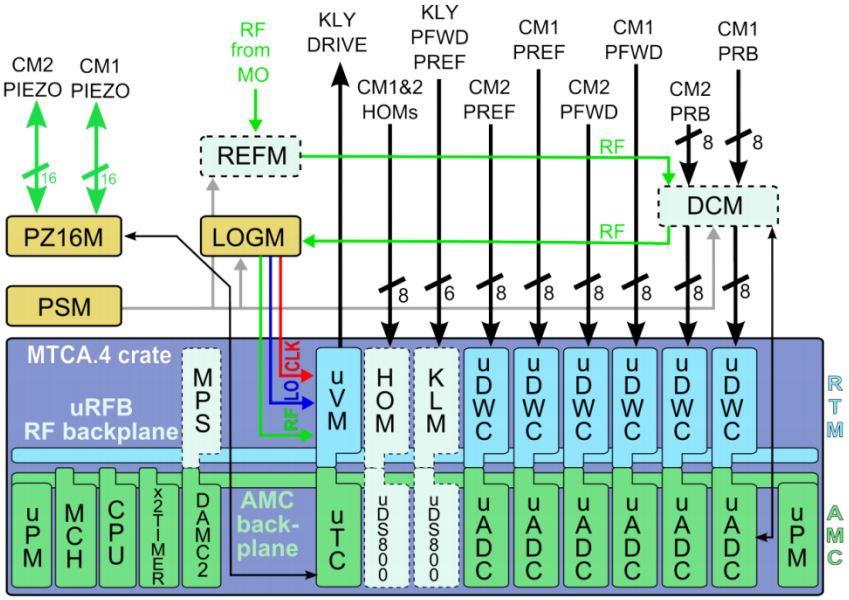
Modular LLRF System in MTCA.4

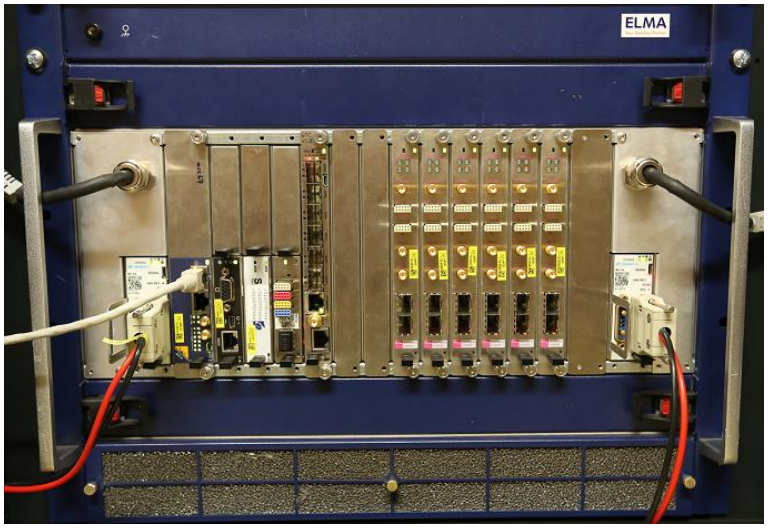
- **High frequency regulation (simplified) :**



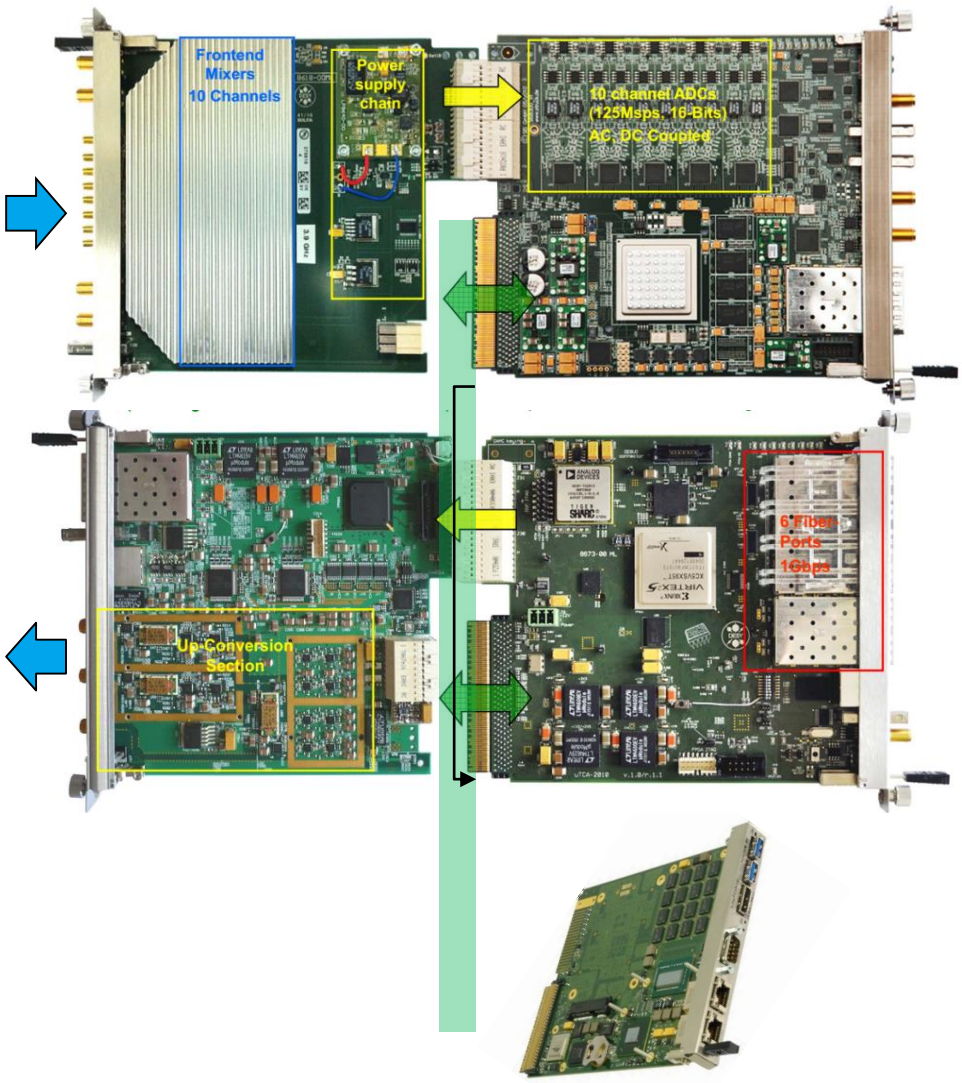
LLRF system

- One MTCA.4 crate for two accelerating cryo-modules is equipped with:
  - 6 AMC ADC boards + 6 down-converter RTM boards
  - 1 AMC controller + vector modulator RTM board
  - 1 timing module, provides synch timing on backplane
  - 1 AMC CPU (Intel i7 arch) with hard drive and Linux OS running
  - 2 power supply + management module (MCH)





Hardware



Multi- Channel fast ADC Digitizer (SIS8300L)
- 10 channel ADCs (125Msps, 16-Bits)
- Virtex6, DDR3
- FPGA pre-processing partial cavity vector sum
- 2 x MGT links via MTCA-backplane

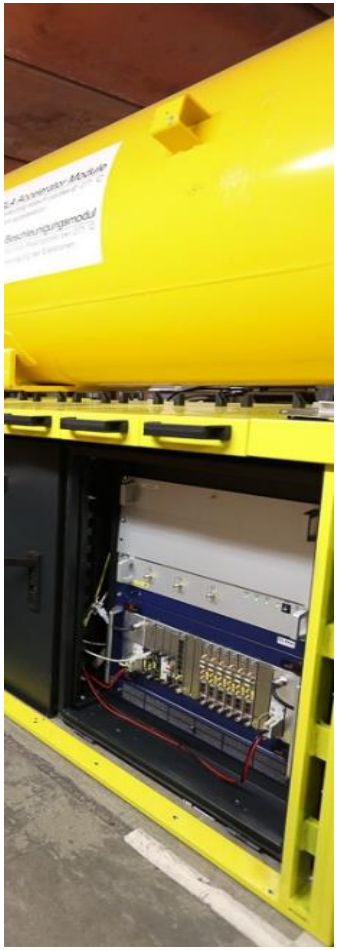
High frequency Down- Converter(uDWC)
- 10 channel field detection(1.3GHz, …,3.9GHz)
- Resolution, 0.003%, 0.003deg, < 10fs

LLRF FPGA Controller (uTC)
- LLRF Controller,
- 6 x Fiber-Ports,
- 8 x MGT links via MTCA-backplane
- FPGA(Virtex5), DSP

High frequency Klystron Driver (uVM)
- 2 channel Vector Modulator (108MHz, 216MHz, 1.3GHz…3.9GHz)
- Spartan6
- 16-bit DAC performance
- 2 Fiber-Ports, Standalone operation possible

CPU CONCURRENT AM 90x/x1x
- 4-core 2.1 GHz Intel Core i7-3612QE processor
- 4GB DDR3-1600 DRAM
- 2 x SSD in RAID

Installation at FLASH



Create for 4 modules installed in tunnel,
(the same way as will be for XFEL)

Additional sheelding against radiation

Create hight around 1meter fits to be plased under accelerating module

Control parameters

Controller parameters

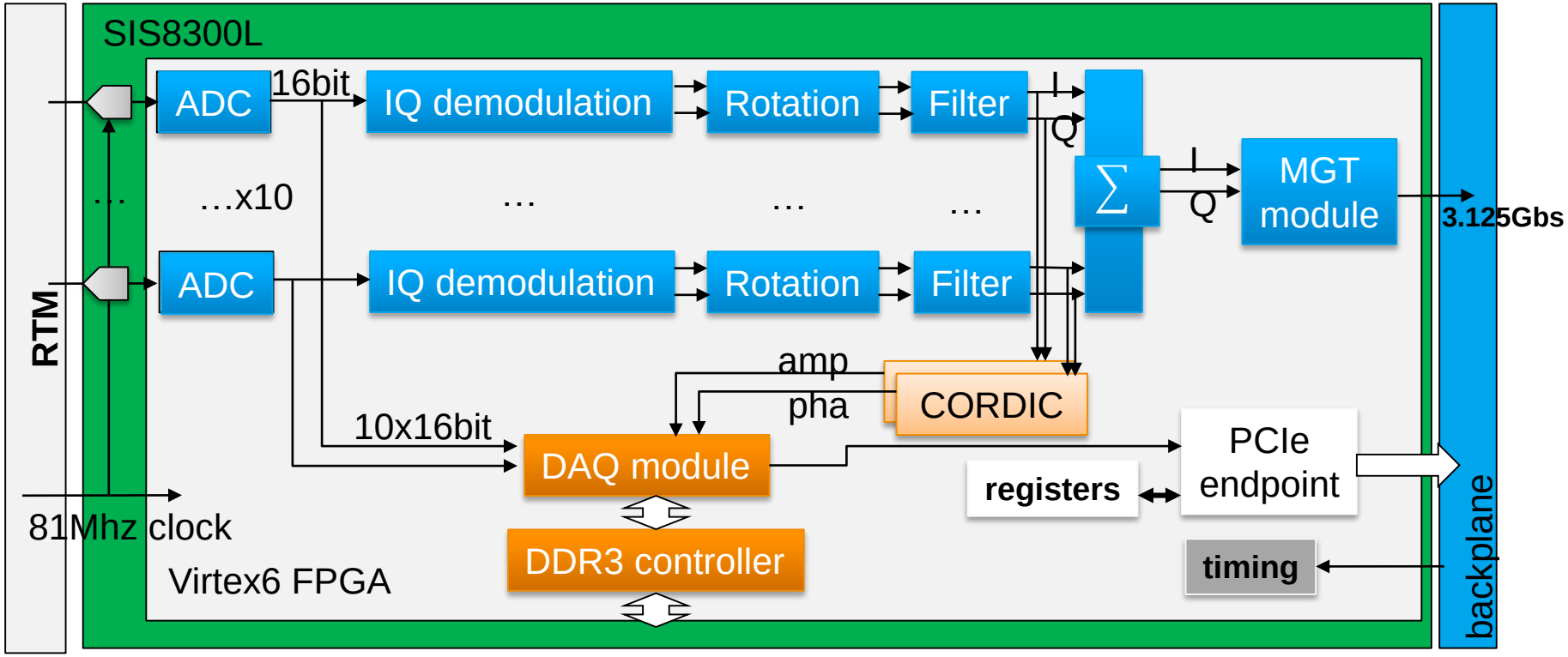
- Controller works in pulse mode
- Pulse length of max 1.5ms with 2ms DAQ window
- Pulse repetition rate currently at FLASH: 10Hz
- Controller works with 9Mhz frequency
- ADC sampling frequency and internal data processing: 81Mhz
- Digital IQ demodulation: 9 samples per one IQ value
- P – type controller (proportional) or/and MIMO – controller(multi in multi out)
- **Close loop system delay ~1µs** (ADC input -> DAC output)

Regulation parmateres

- Phas stability over pulse flattop:dP < 0.01 deg
- Apmlitude stability pulse flattop: dA/A < 0.01%

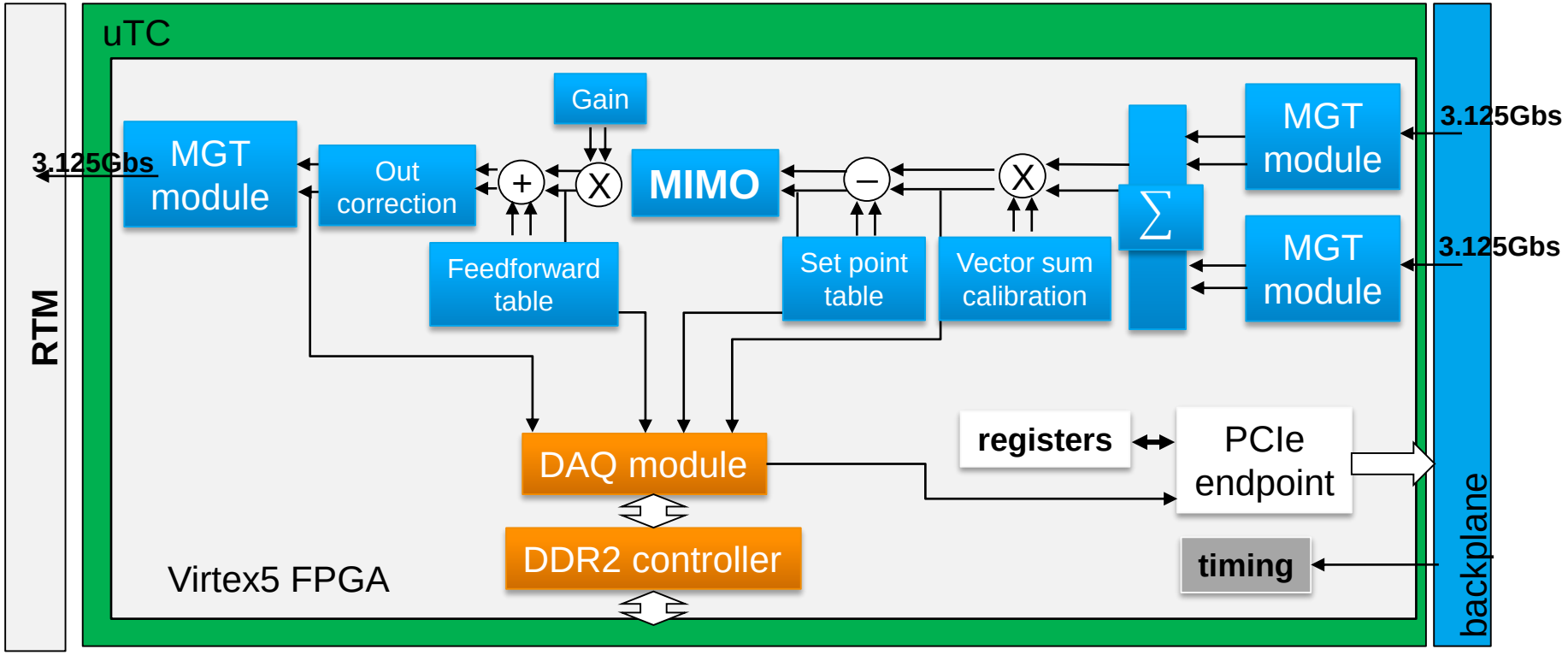
LLRF controller

- SIS8300L, ADC board firmware



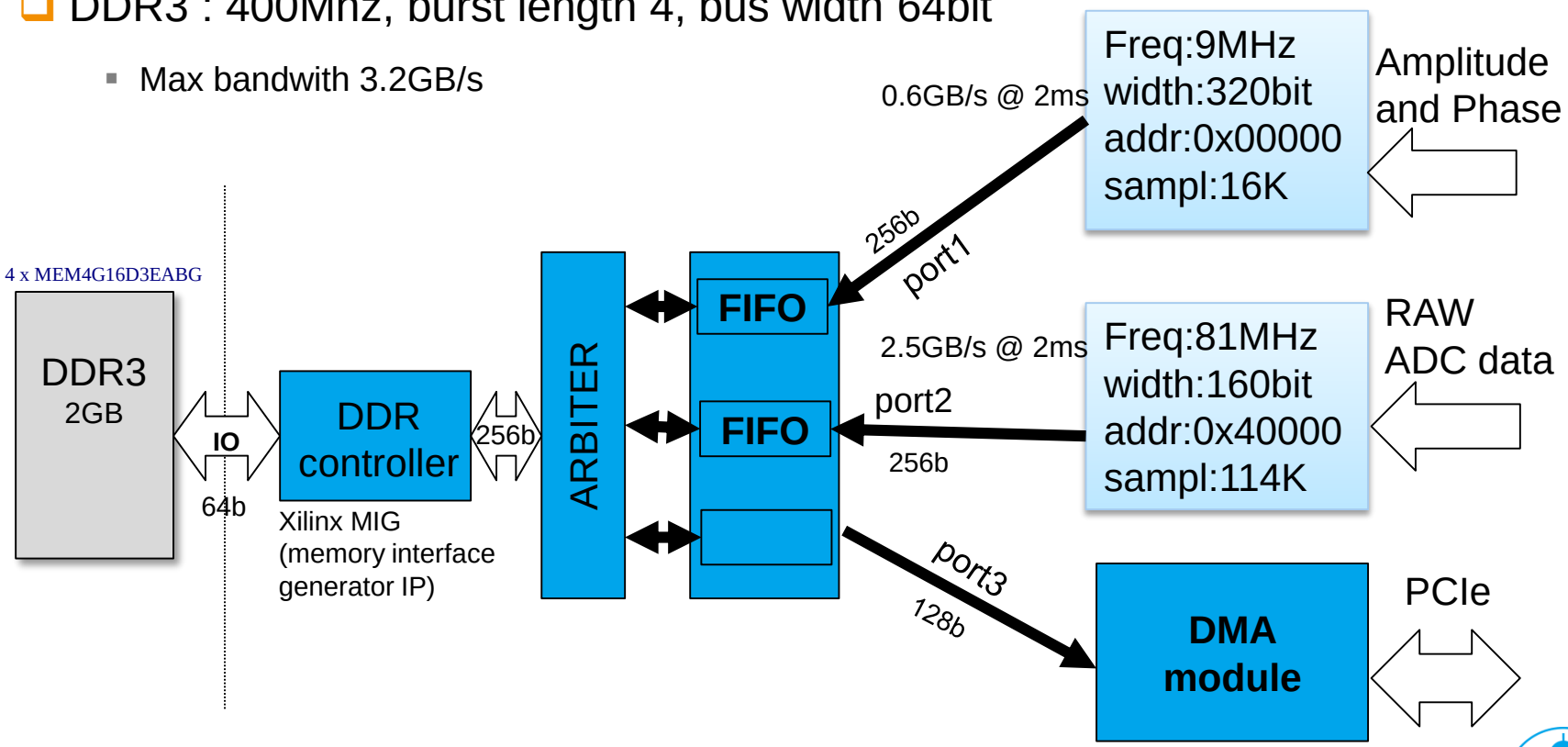
LLRF controller

- uTC controller board firmware



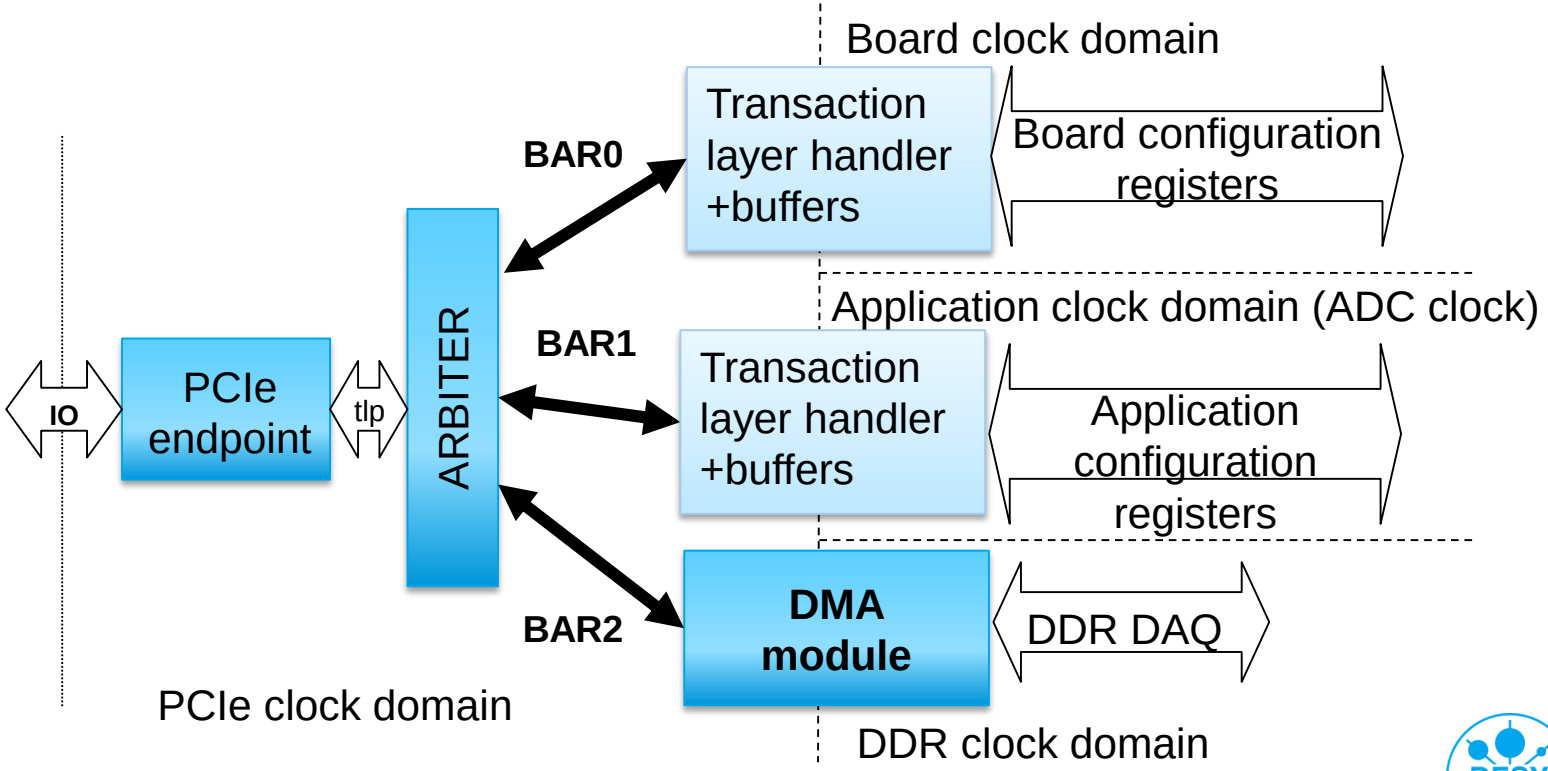
DAQ on ADC board

- Multiport access with priority arbiter to the DDR controller
- DDR controller generated using Xilinx MIG IP core
- Every port with FIFO buffers
- DDR3 : 400Mhz, burst length 4, bus width 64bit
  - Max bandwith 3.2GB/s



PCIe endpoint arbiter

- Arbiter between 3 clock domains
- Independent packet creation, every domain can generate TLP and access endpoint transaction layer.
- Separation using different BAR for different domain



DMA

- DMA transfer triggered by CPU
- Device driver allocates memory (currently 1MB per one DMA request) in OS and send request to device
- 3 information required
  - CPU address – pointer to CPU allocated memory where data should should be send,
  - DDR address – address in device from which data should be read,
  - Data amount – number of bytes that should be send by device,
- Writing those values to DMA module registers in FPGA triggers data transfer,
- When all data is send device generates PCIe interrupt telling CPU that DMA transfer was finished

DMA module

- Two separate processes

1. Reading data from DDR

Generates addresses for DDR read based on provided address and amount of data

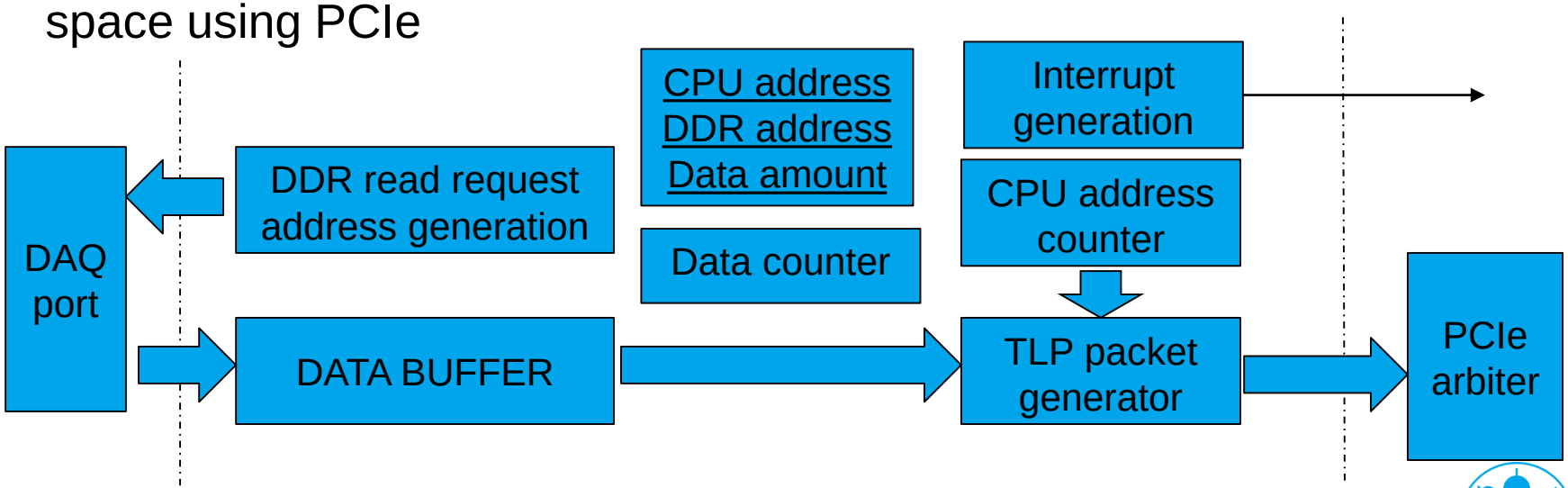
Read is done in burst, it generates up to 92 read requests in row and next wait for buffer almost empty flag

2. Generating TLP packets, Memory write requests from board.

Waiting for data in buffer, if there is enough data in buffer recalculate destination address and starts transfer,

When all data is send generates interrupt and empty buffer

- Rewrite requested part of DDR memory from board to the CPU memory space using PCIe



Results

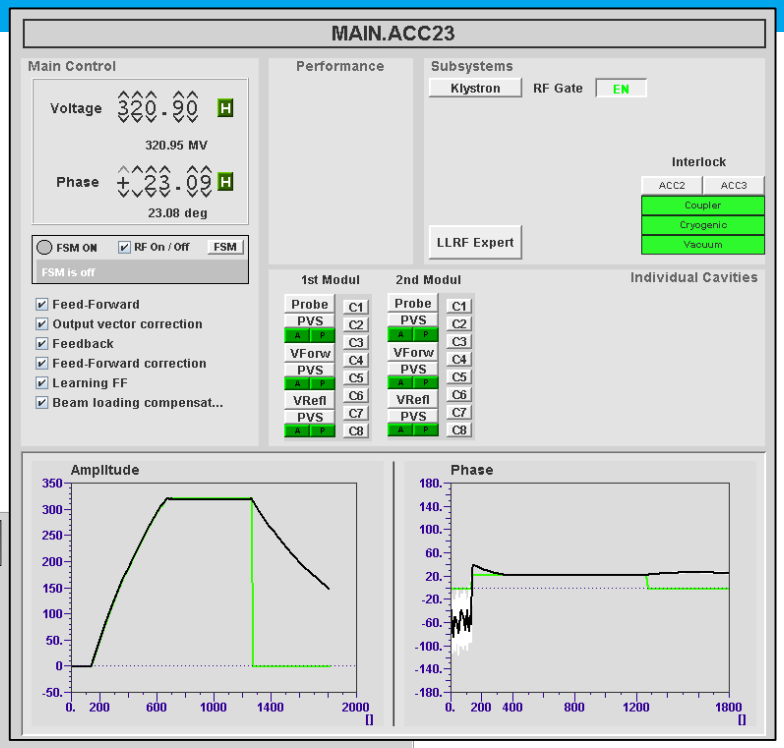
- Average data rate to the user space: 350MB/s (PCI express x4 GEN1)
  - Limitation by driver and not efficient copy to user space
  - Data rate with no copy to user space: around 800MB/s (close to PCIe x4 GEN1 spec)
  - Reading of around 4MB of data from one device:

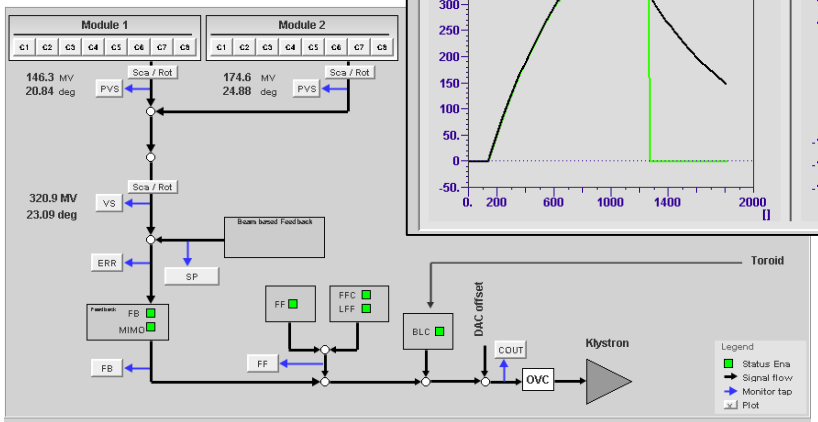
```
host:~> ./testdma /dev/llrfadcs10
ADDR: 0x0i COUNT: 1000000i (339.9 MB)
ADDR: 0x0i COUNT: 1000000i (361.3 MB)
ADDR: 0x0i COUNT: 1000000i (348.6 MB)
ADDR: 0x0i COUNT: 1000000i (354.9 MB)
```

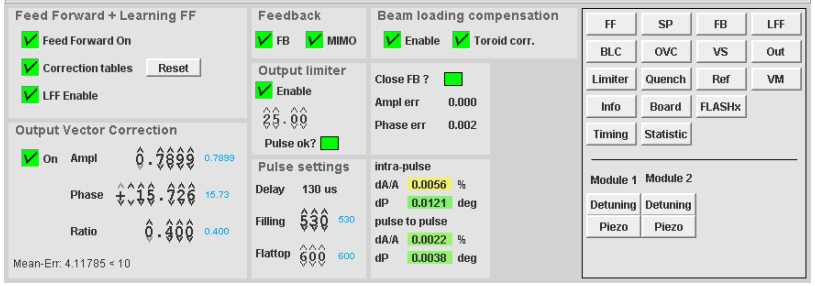
- Taking all data needed for controller operation from devices takes around 4-5ms

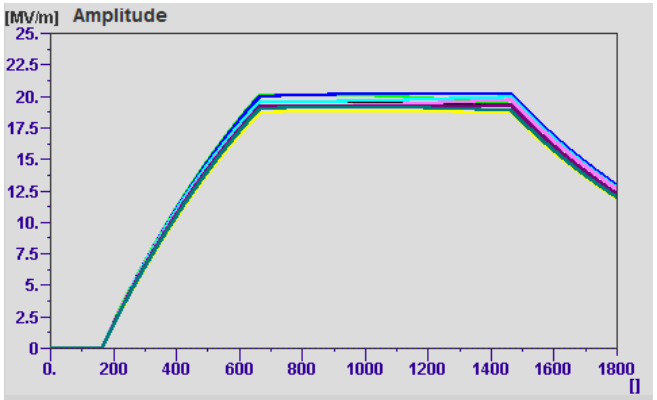
  Server has next 90ms to do data processing and send correction parameters to controller and send data to external DAQ system

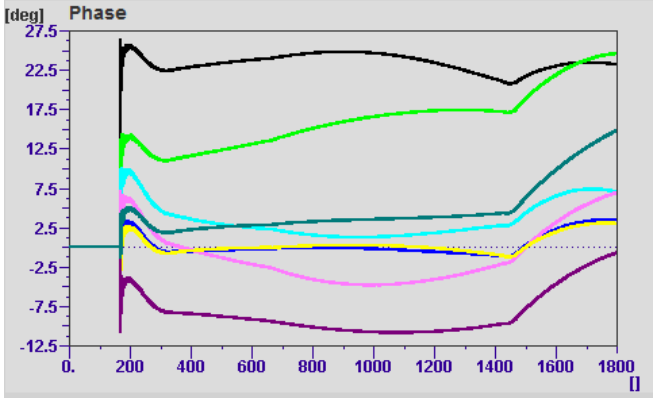
Control panels











Thank you for your attention