Front end Digitisation

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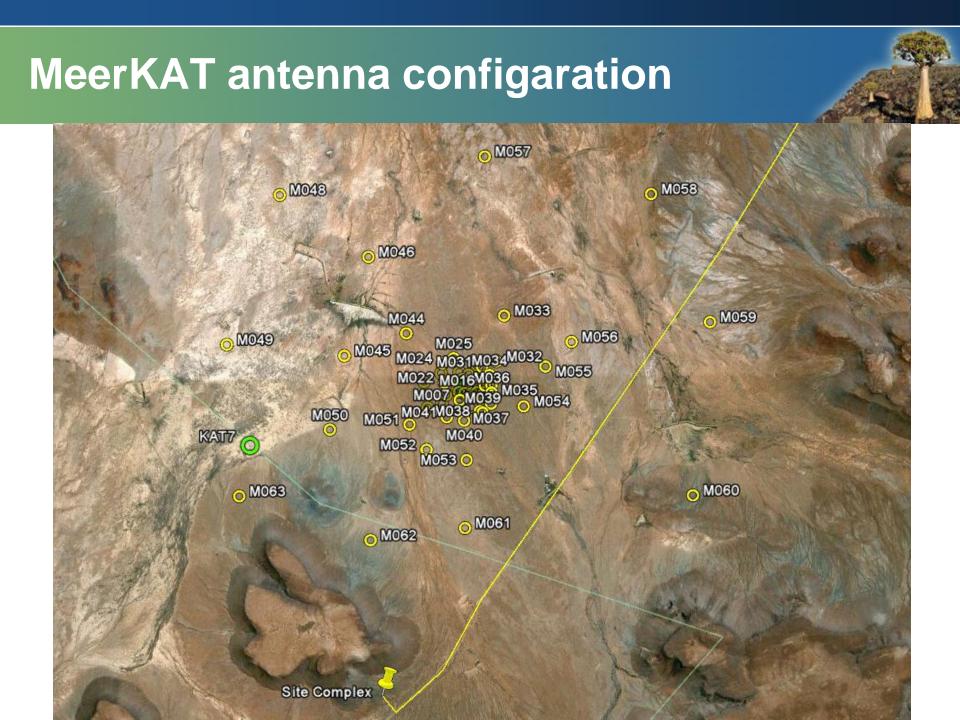
















SCOPE



- Why front end Digitisation
- Key specifications of MeerKAT Digitiser
- Block diagram of Digitiser
- RF front end
- Analogue to Digital converter
- Sample Clock Generation
- Results

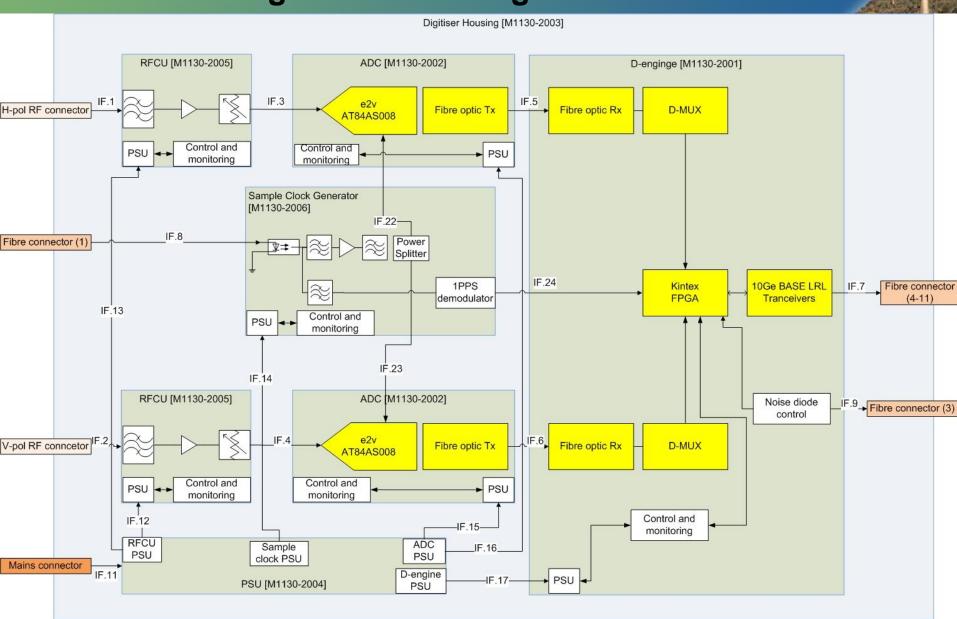
Why front end Digitisation



- Negate the need for expensive RF chains
- Reduces the number of local oscillators
- Improves channel isolation and cross talk
- Negate the need for RF over fibre links
- Improves gain and phase stability
- Digitisation can be done close to the feed

Parameter	Unit	Spe	Specification		Result
Frequency range	900 to 1670 MHz				
Stop band rejection (ambient)	dB	27			28
Nominal Gain	dB	10.5			10
Gain flatness	dB	+-2dB			+-1.9
Input matching	dB	15			19
Channels		H and V channel			
Sampling zone	2 nd Nyquist Zone				
Sampling efficiency	>98.5%				
Number of bits	10				
SFDR (-1dB full scale)	dB	>50dB			55dB
Output data	4x 10Ge BASE SR				
1PPS synchronization	<10ns				
Weight	kg	40			40
Dimensions		510x215x255mm			
Cooling	Ambient >50° C	Forced air			
	Ambient <50° C	Convection			
RFI compliance	SARAS levels for equipment installed <1m from MeerKAT receiver				
Environment	ETSI EN 300 019-1-4 V2.1.2 standard class 4.2H				
Power supply (220Vac)	VA		<125		85

Digitiser block diagram

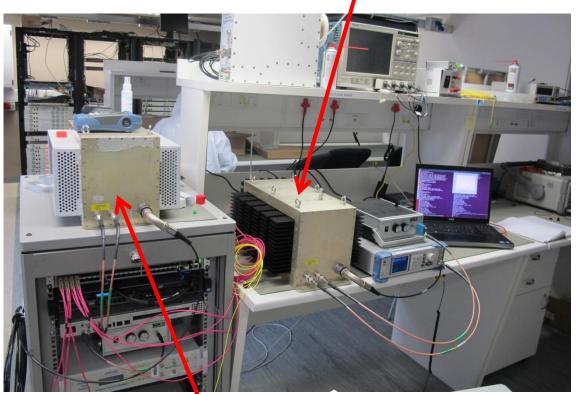


11/17/2014

HPSP 2014 - Front end Digitisation

Integrated Digitiser

Passively cooled Digitiser

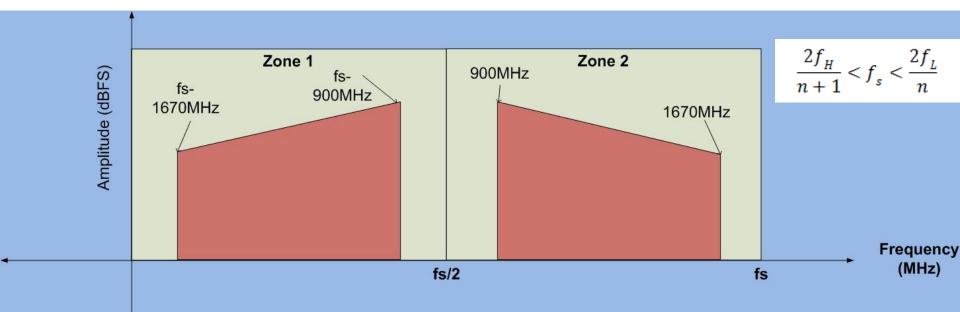


Actively cooled Digitiser



Bandpass Sampling

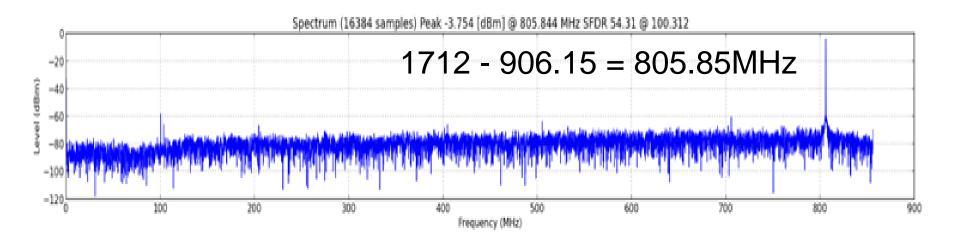


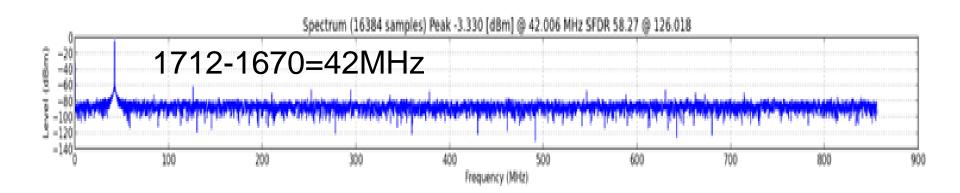


- Sample Zone 2 due to the availability ADCs capable of this sample rate while still providing the required dynamic range
- Chose to sample at1712MHz due to the Anti-aliasing filter symmetry

Down conversion for free







Sampling efficiency



SNR_{in} / SNR_{out}

Sampling efficiency ≥98%
98.8 %

99.8 %

ADC small signal to noise power ratio

$$SNR_{NF}(dB) = 10 * log_{10} \frac{\eta_{ADC}}{1 - \eta_{ADC}} = 19.14dB$$

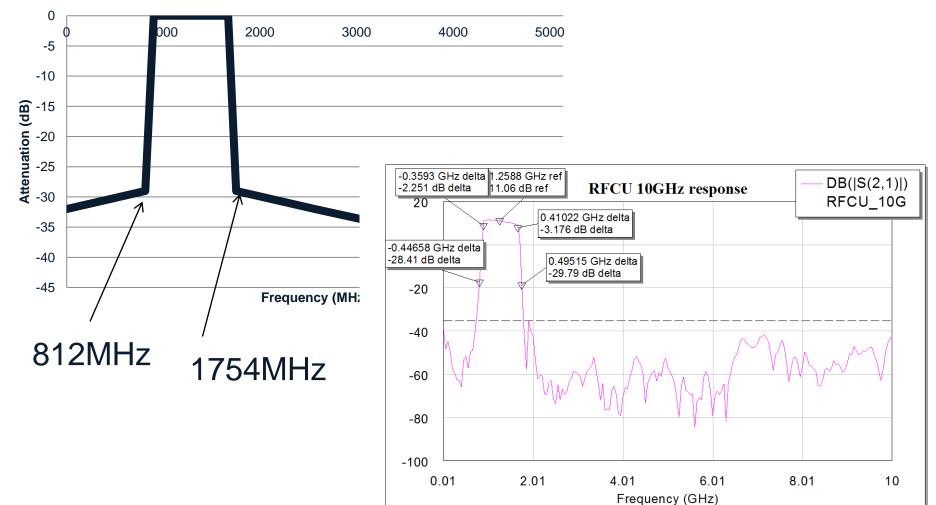
Anti –aliasing filter

$$\alpha = 10 * log \left(\frac{1}{\eta_{BPF}} - 1\right) = 27dB$$

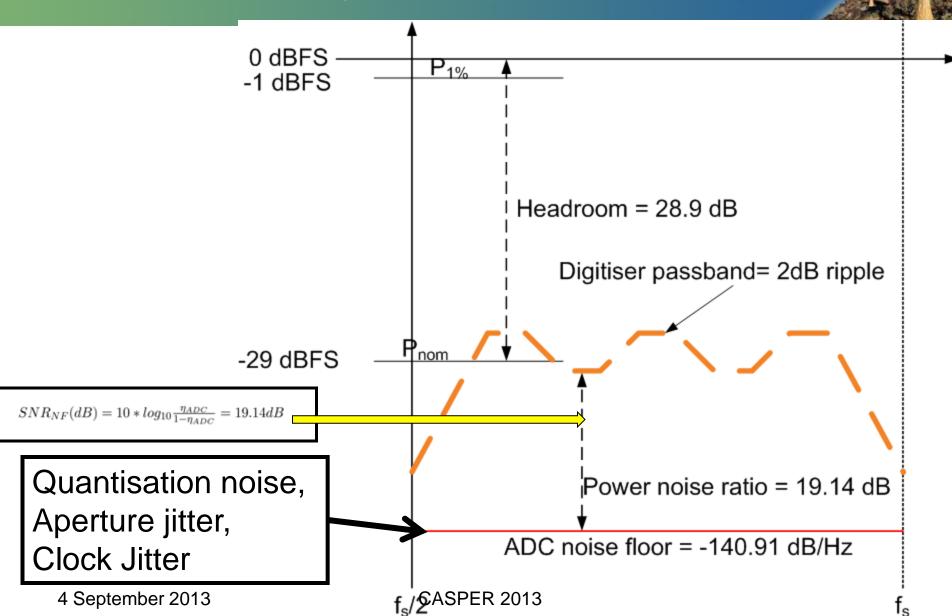
Anti-aliasing filter



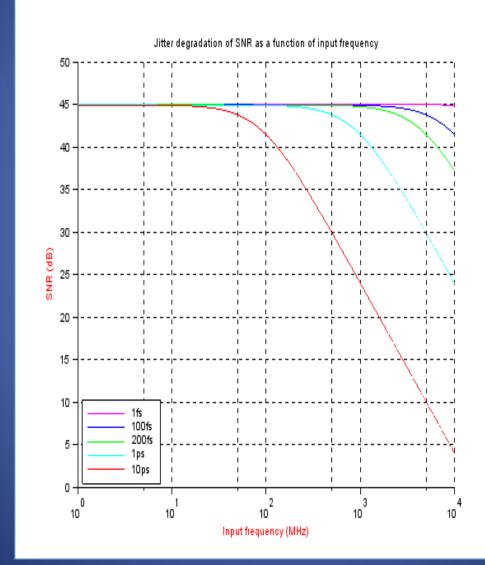




Headroom and signal to noise ratio

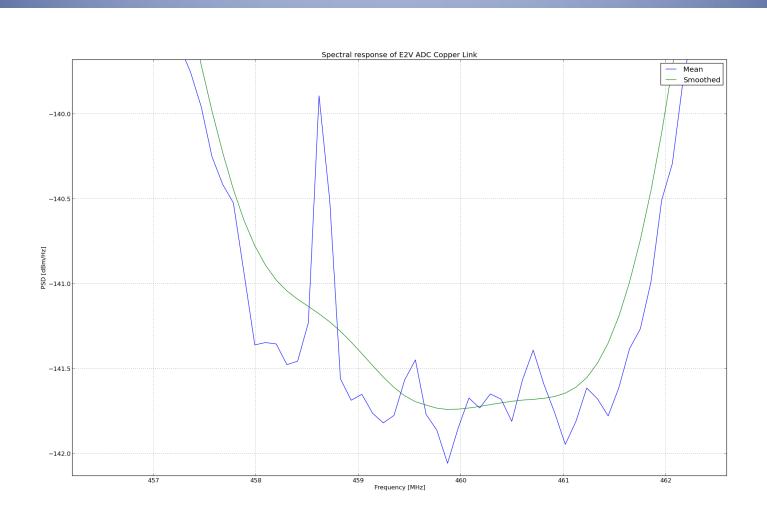


Degradation of SNR due to clock jitter



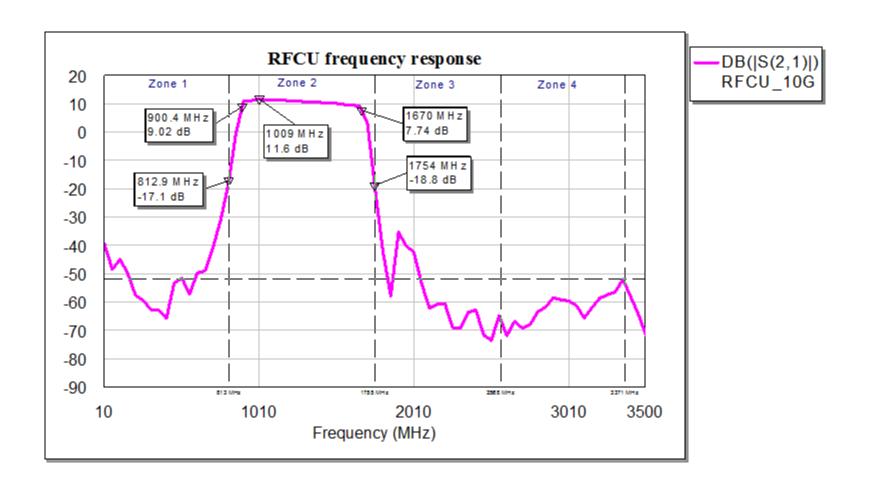
Measured ADC noise floor





RFCU frequency response

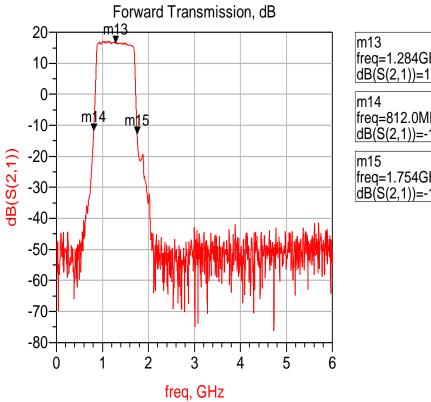




Measured Results: RF Performance



RFCU II Ser #001 Stopband Attenuation +25C (+25.8C actual) -44dBm Source Power



freq=1.284GHz dB(S(2,1))=16.509

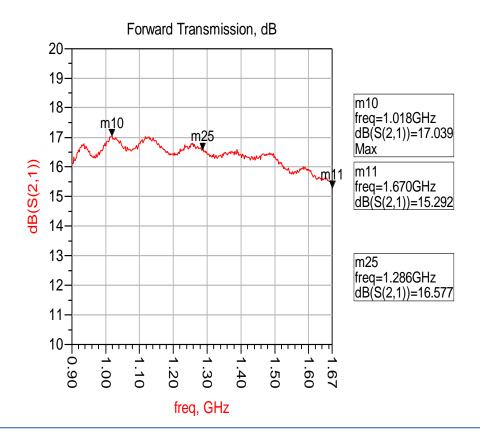
freq=812.0MHz dB(S(2,1))=-11.727

freq=1.754GHz dB(S(2,1))=-12.819

Measured Results: RF Performance

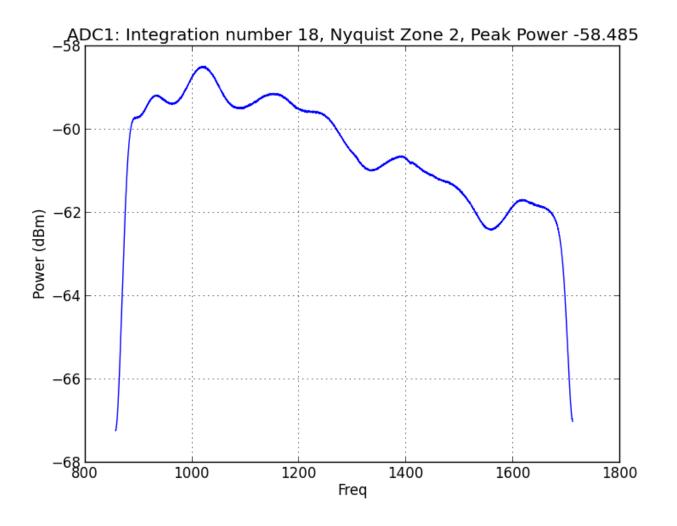


RFCU II Ser #001 Gain Flatness +25C (+25.8C actual) -44dBm Source Power

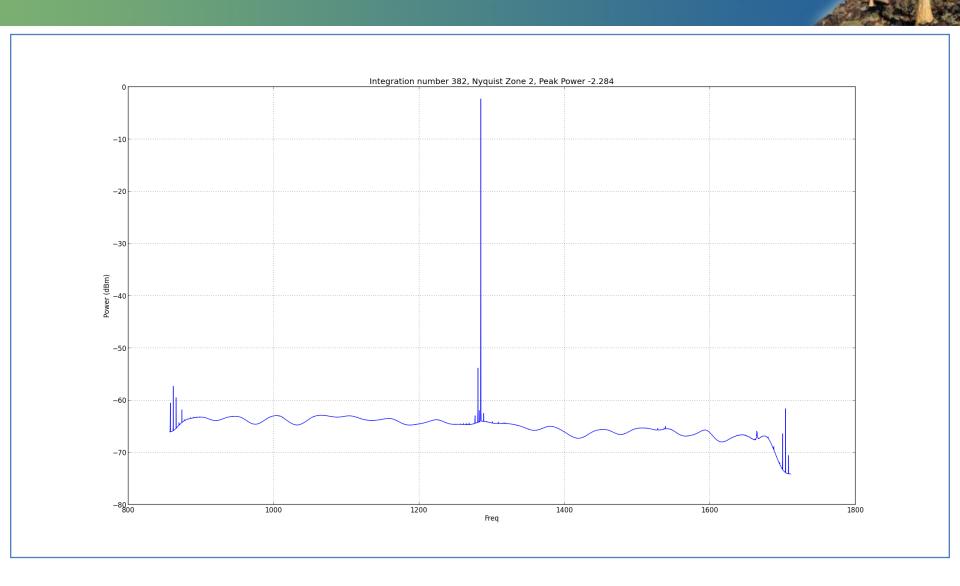


Digitiser passband





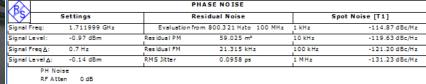
Measured Results: SFDR

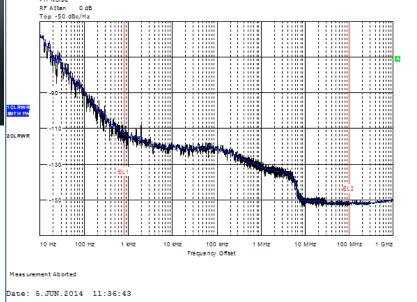


Sample clock generation

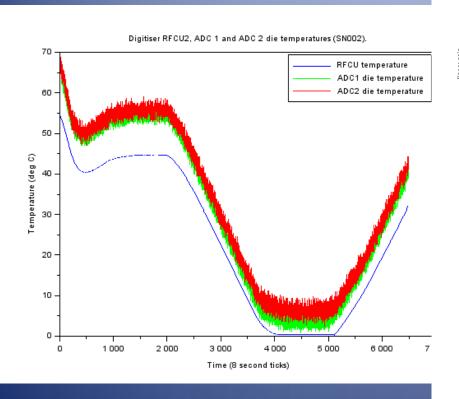


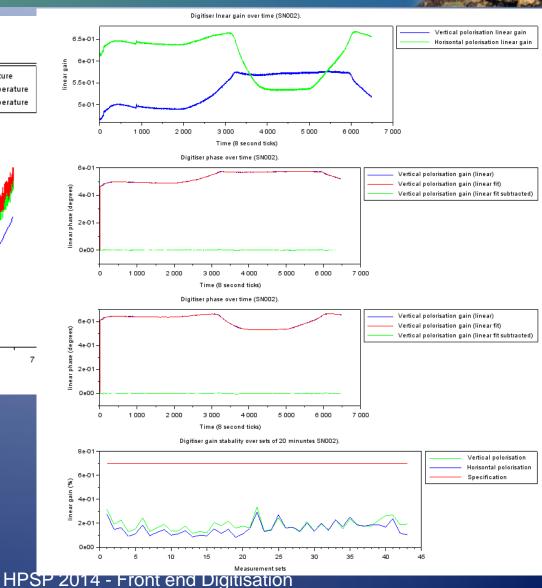




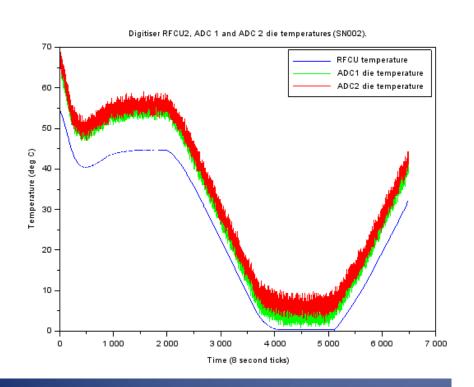


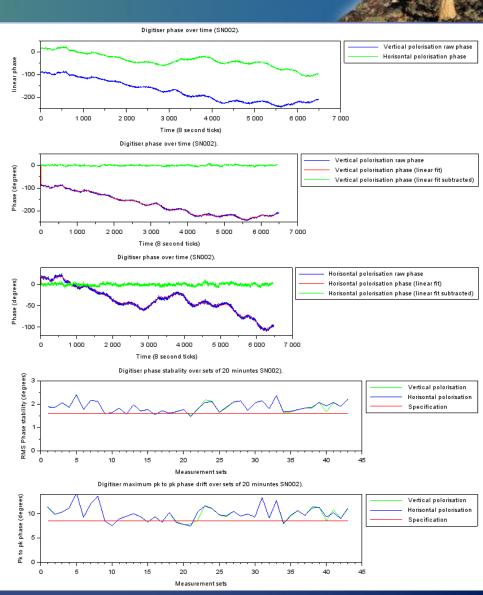
Measured Results: Gain Stability





Measured Results: Phase Stability





Questions?

















Reference signals

