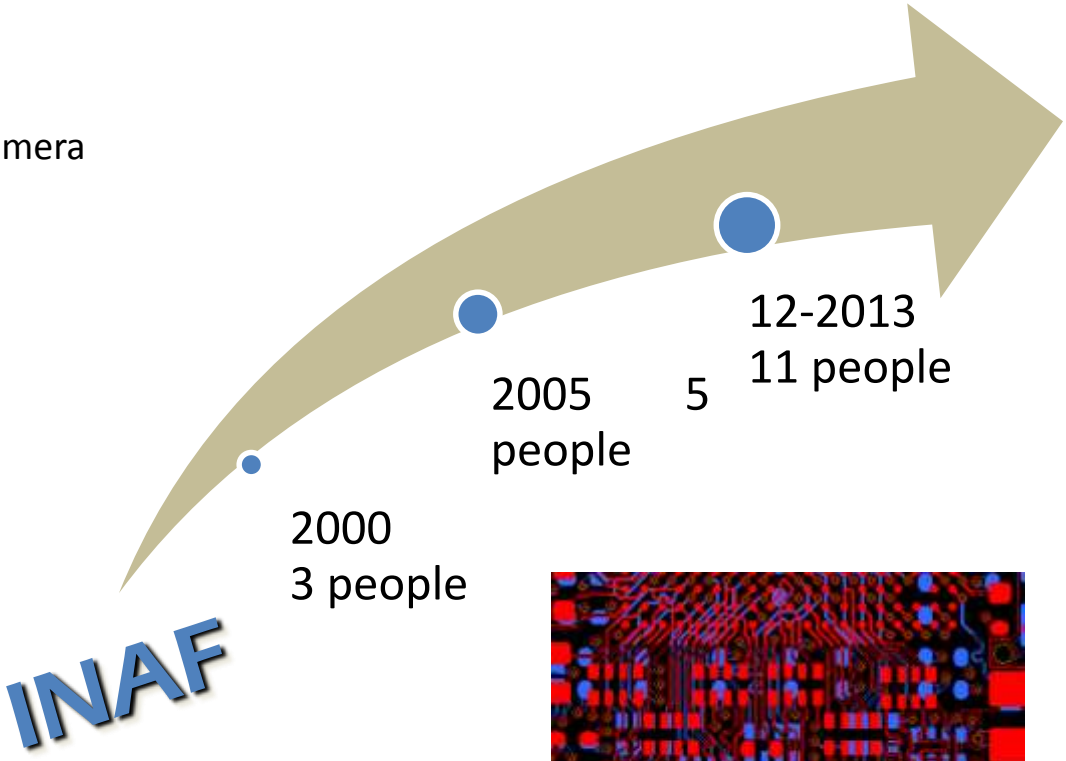
HP signal processing board for SKA LFAA

Malta , October 29th 2014

Experiences

- Industrial
  - Vision
  - Motor control
- Imaging
  - Surveillance camera & Industrial camera
  - FPGA analytics
  - Hi performance sensor
- Space and avionics
  - DO 254 development flow
  - FPGA based CPU board
  - Fault injection system
- Telecommunications
  - Ethernet QOS IP cores
- Production
  - Test and qualification process



Some success stories:

- Model of the Hi-Reliable COTS Based Computer platform

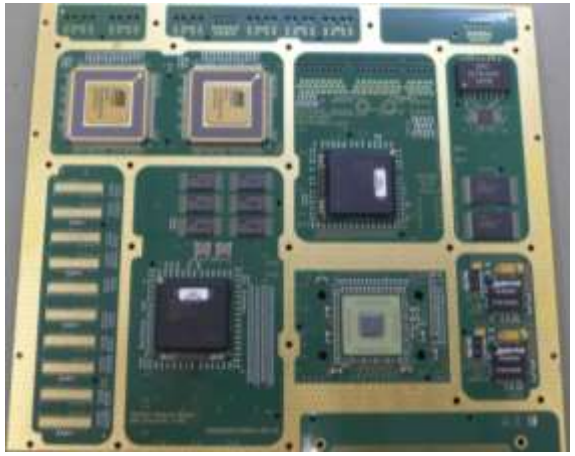
- HI REL SBC with 1GHz PPC for space application (ESA, Thales)

- 10 GBit FPGA Ethernet Board for QoS and IDS (2008-2006)

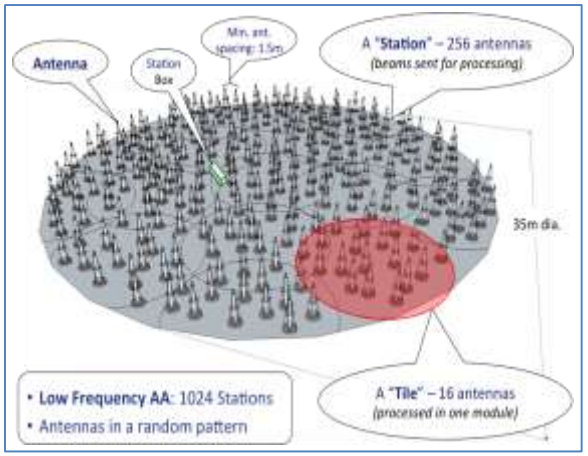
- CCD camera for industrial applications

- System for SEU fault emulation in SRAM FPGAs (INAF, ESA)

- METEOSAT - ESA satellite



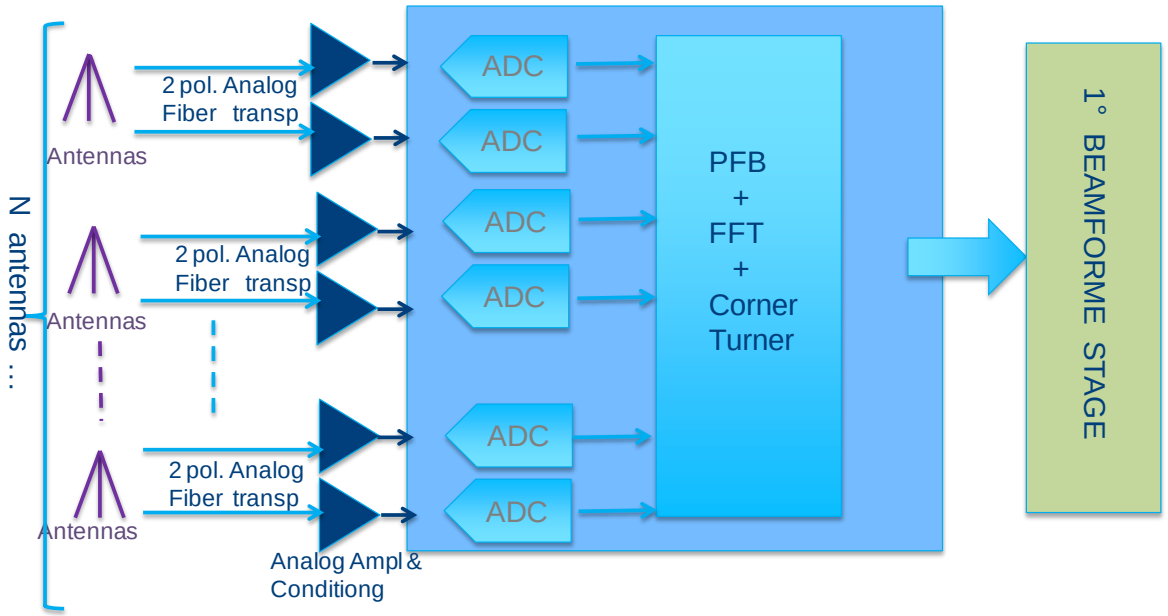
- FPGA design flow compliant with a specific avionic standard (Galileo Avionica, SELEX)



IASF-MILANO
NEWCOMERS IN SKA (LFAA TPM)

TPM Project Objective

- Design and implementation of a digital hw platform with suitable FW and SW, for the first stadium of the Low Frequency Aperture Array of the SKA telescope
- Tight requirements
  - Low power
  - Low cost
  - Fit in the Bunker
- Main spec
  - 32 Analog input
  - Up to 1 Gsample
  - Up to 65 dB SFDR
  - Up to 80 Gbit Eth Out
  - Hi performance FPGA



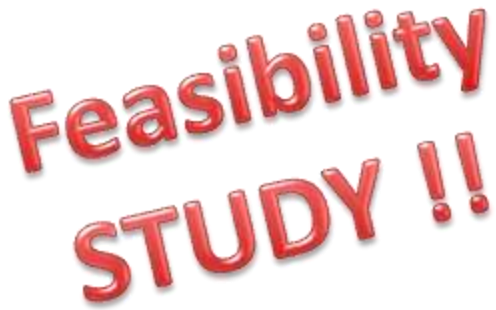
Working Groups

- INAF - IASF Milano & Sanitas EG
  - Feasibility study, Hardware design
  - Board prototyping
  - Management firmware & low level SW
- INAF - IRA (Bologna, Medicina, Noto)
  - Scientific Case
  - FPGA firmware (Arcetri Observatory)
  - Mechanical design
- SELEX-ES LTD
  - Design specification and process overview
- Analog Device
  - AD & Clocking design support, FMC prototyping for performance verification
- Xilinx
  - Ultrascale Early access program access
  - Firmware for JESD interface and 10-40 Gbit Ethernet interface

Board challenges/numbers

- Main function co-existence:
  - Board powering
  - Digital function
  - Analog to digital low noise conversion
- Mechanical specs
- Cost, testability & manufacturability
- Total power

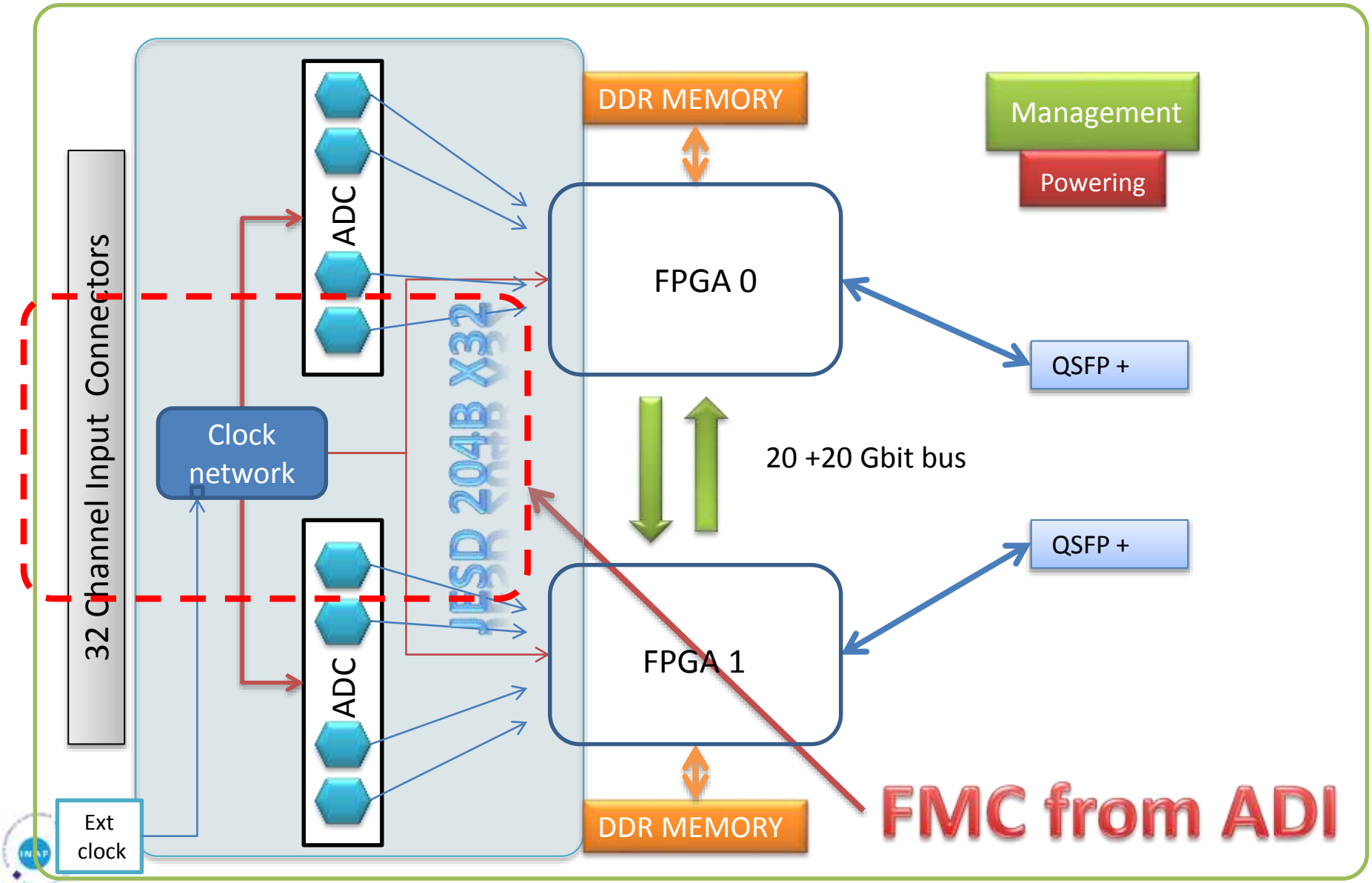
- 6U x 170 mm
- 17 large DC-DC converters, high current 20A, 5V expected
- 2 large FPGA
- 32 analog input



Feasibility output: main devices

- Direct support from market leader device supplier
  - Xilinx: state of the art 20nm Ultrascale FPGA, direct support and early access program
  - Analog Device: last devices close to release
    - JESDB 14 bit 1 GHz dual channel AD
    - JESDB PLL
    - Ultra High PSRR linear regulator for AD
    - SKA DEMO FMC board to performance evaluation

Feasibility output: board architecture

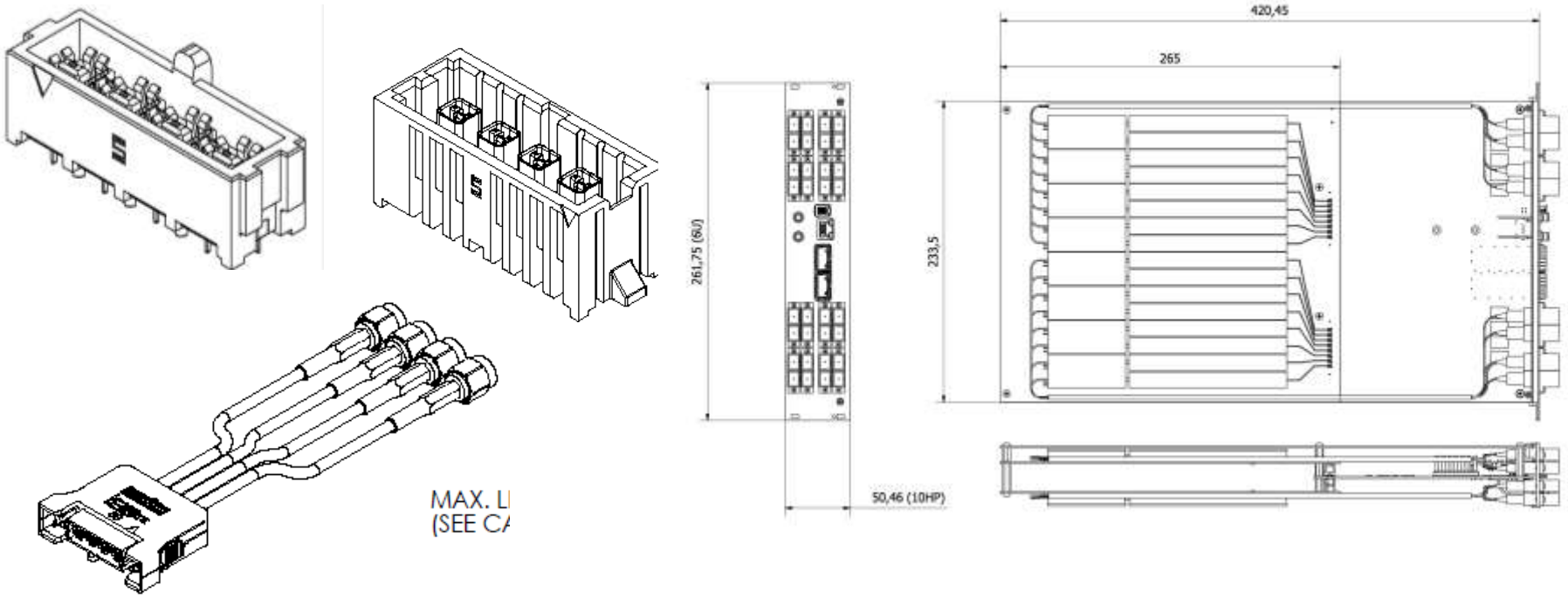


Feasibility output: mechanics and connectors

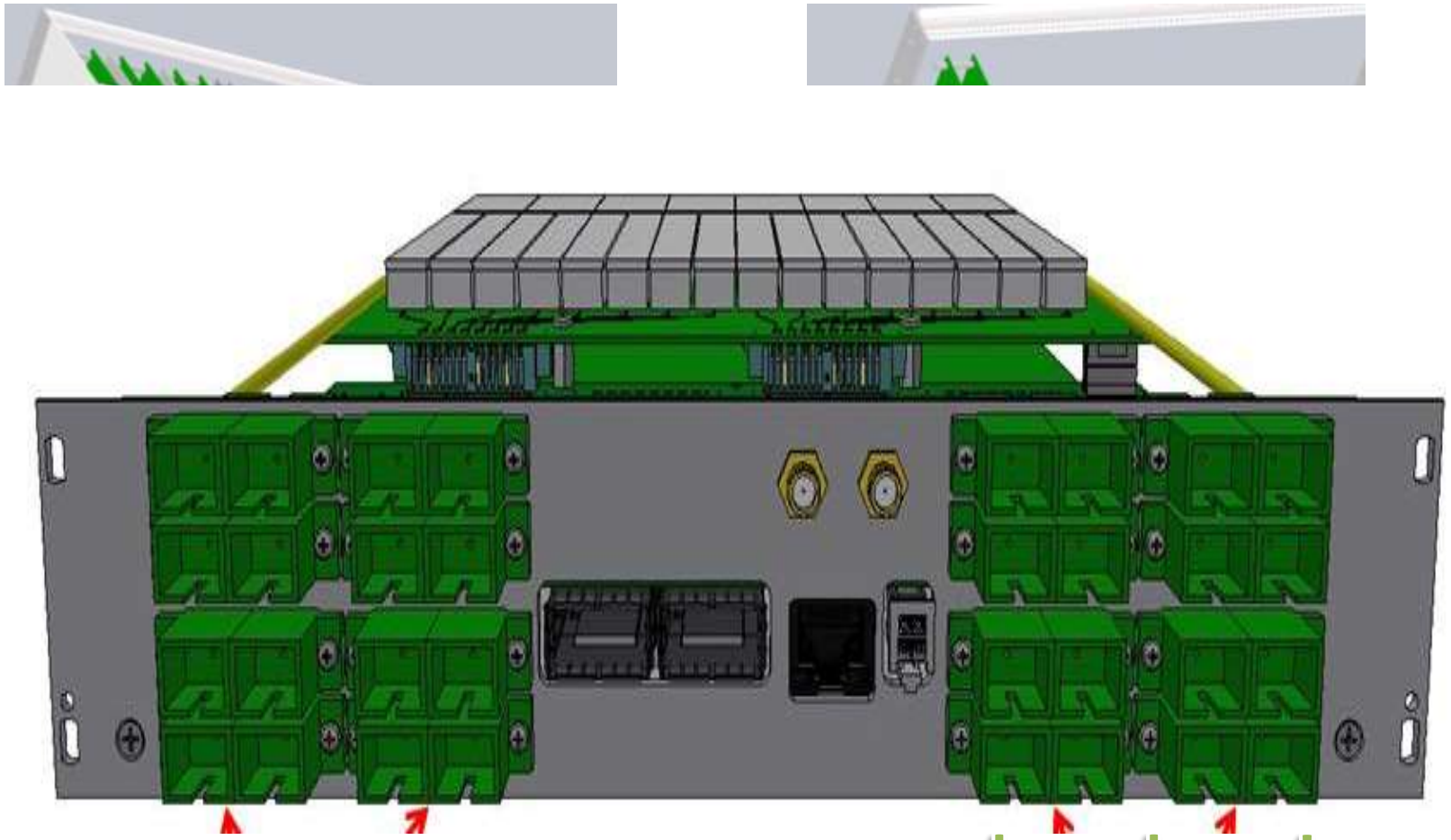
RF compact connector

8 positions, SNR > 60db
Board 2 Board : 10 mm

Board dimension: 233 x 170 mm



TPM Rack design for SKA



BOARD DESIGN

Data synchronization

- Synchronous acquisition JESD204B Subclass 1 over all 16 AD
  - Subclass 1 support ***deterministic latency*** between AD and FPGA
  - AD Sampling clock generated by PLL from External 10 MHz signal:
    - synchronous Dev Clock for AD distributed with side dedicated clock buffer 1-10
    - synchronous Dev Clock for FPGA transceiver with a scaling factor
    - synchronous Dev Clock for FPGA logic with a separate scaling factor
    - system reference event signal (SYSREF) distributed with side dedicated clock buffer 1-10 to AD and FPGA
  - FPGA generate SYNC signal to start acquisition
  - PLL input switch over external and internal oscillator
  - On Board PLL generate Lock status signal for management
    - Input PLL lock
    - FPGA PLLs lock status after configurations

FPGA Xilinx Ultrascale: 20 nm device

Part Number	XCKU040	XCKU060	XCKU075
Logic Cells	424,200	580,440	756,000
CLB Flip-Flops	484,800	663,360	864,000
CLB LUTs	242,400	331,680	432,000
Maximum Distributed RAM (Kb)	7,050	9,180	7,290
Block RAM/FIFO w/ECC (36 Kb each)	600	1,080	1,188
Block RAM/FIFO (18 Kb each)	1,200	2,160	2,376
Total Block RAM (Mb)	21.1	38.0	41.8
DSP Slices	1,920	2,760	2,592

Production
1q 2015

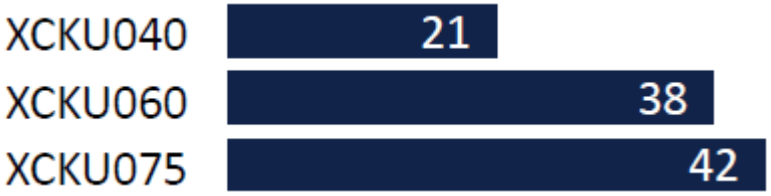
Serial Transceivers:

GTH = 16.3 Gb/s

DSP Slice Count

Speed grade	-1	-2	-3
F_{MAX} [MHz]	594	661	741
Max GMAC/s	6558	7297	8181

Block RAM Capacity (Mb):



Speed grade	-1	-2	-3
True dual-port Block RAM F_{MAX} [MHz]	525	585	660

FPGA POWER ESTIMATION

Utilization		
Registers	387.840	80%
LUTs	218.160	90%
RAMB18	1080	90%
DSP48	1728	90%

GTH Channels	20	100%

Device: XCU40
Overall Usage: 90%
Internal logic: 350 MHz
Toggle rate: 12.5% (default)
DDR3L: 32 bit 1600 MHz

Summary

Total On-Chip Power	11,2 W	
Junction Temperature	41,1 °C	
Thermal Margin	43,9°C	29,4W
Effective ΘJA	1,4 °C/W	

28%	Transceiver.....	3,147W
12%	I/O.....	1,402W
56%	Core Dynamic..	6,265W
4%	Device Static.....	0,434W
	Power supplied to off-chip devices...	0,000W

On-Chip Power

Resource	(Jump to sheet)	Power (W)	Power (%)
Core Dynamic	CLOCK	1,800	16
	LOGIC	2,917	26
	BRAM	0,238	2
	DSP	1,111	10
	PLL	0,199	2
	MMCM	0,000	0
	Other	0,000	0
	PCIE	0,000	0
I/O	IO	1,402	12
Transceiver	GTH	3,147	28
Device Static		0,434	4

Power Supply

Source	Voltage	Total (A)
V_{CCINT}	0,950	6,948
V_{CCINT_IO}	0,950	0,328
V_{CCBRAM}	0,950	0,026
V_{CCAUX}	1,800	0,139
V_{CCAUX_IO}	1,800	0,269
V_{CCO} 3.3V	3,300	
V_{CCO} 2.5V	2,500	
V_{CCO} 1.8V	1,800	
V_{CCO} 1.5V	1,500	
V_{CCO} 1.35V	1,350	0,538
V_{CCO} 1.2V	1,200	
Vcco 1.0V	1,000	
$MGTV_{CCAUX}$	1,800	0,067
$MGTAV_{CC}$	1,000	1,914
$MGTAV_{TT}$	1,200	0,664
-		
-		

Synthesis Test: Polyphase filter

```
Polifase_filter
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xcku040-ffva1156-1-c-es1

clk = 200 MHz => Met: worst slack 0.462
clk = 333 MHz => Met: worst slack 0.089
clk = 350 MHz => Met: worst slack 0.005
clk = 360 MHz => Violated : worst slack -0.134
clk = 400 MHz => Violated: worst slack -0.504ns

xcku040-ffva1156-2-e-es1
clk = 400 MHz => Violated: worst slack -0.108

xcku040-ffva1156-3-e-es1
clk = 400 MHz => MET : worst slack 0.135 ns
clk = 422 MHz (Period = 2.5 -0.135 = 2,365) => MET : worst slack 0.108 ns
clk = 444 MHz (Period = 2,257)=> MET : worst slack 0.054 ns
clk = 455 MHz (Period = 2,19) => MET : worst slack 0.075
```

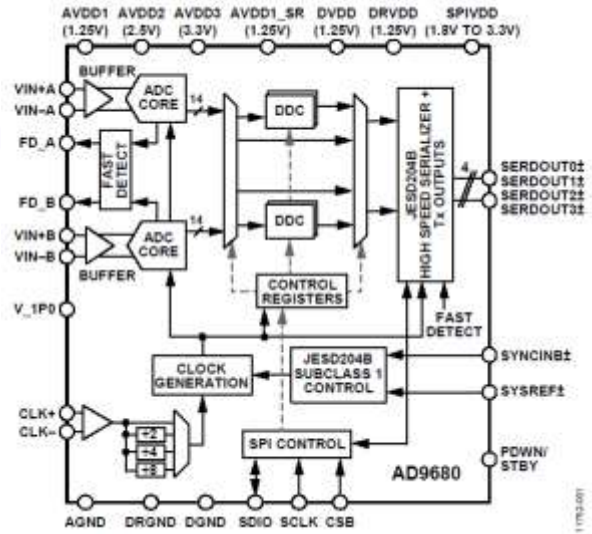
Filter occupancies
Logic: 1265 CLB, 4.2 %
DSP: 140, 7.9%

AD9680 Datasheet

ANALOG DEVICES

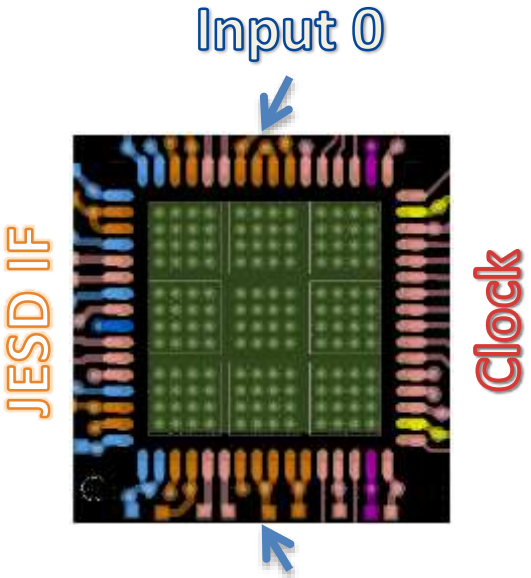
FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
- 1.65 W total power per channel at 1 GSPS (default settings)
- SFDR = 85 dBFS at 340 MHz, 80 dBFS at 1 GHz
- SNR = 65.3 dBFS at 340 MHz (A_{IN} = −1.0 dBFS), 61.4 dBFS at 1 GHz
- ENOB = 10.8 bits at 10 MHz
- DNL = ±0.5 LSB
- INL = ±2.5 LSB
- Noise density = −154 dBFS/Hz at 1 GSPS
- 1.25 V, 2.5 V, and 3.3 V dc supply operation
- No missing codes
- Internal ADC voltage reference
- Flexible input range and termination impedance
  - 1.46 V p-p to 1.94 V p-p (1.70 V p-p nominal)
  - 400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
- 2 GHz usable analog input full power bandwidth
- 95 dB channel isolation/crosstalk
- Amplitude detect bits for efficient AGC implementation
- 2 integrated wideband digital processors per channel
  - 12-bit NCO, up to 4 cascaded half-band filters
- Differential clock input
- Integer clock divide by −1, 2, 4, or 8
- Flexible JESD204B lane configurations
- Small signal dither

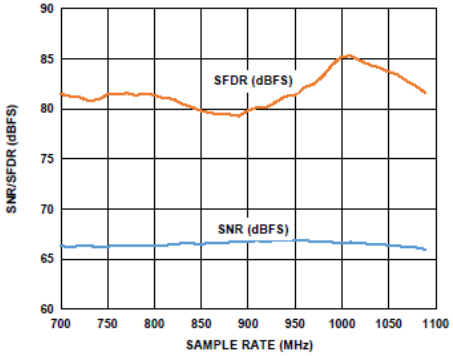


Roadmap to Lower Power

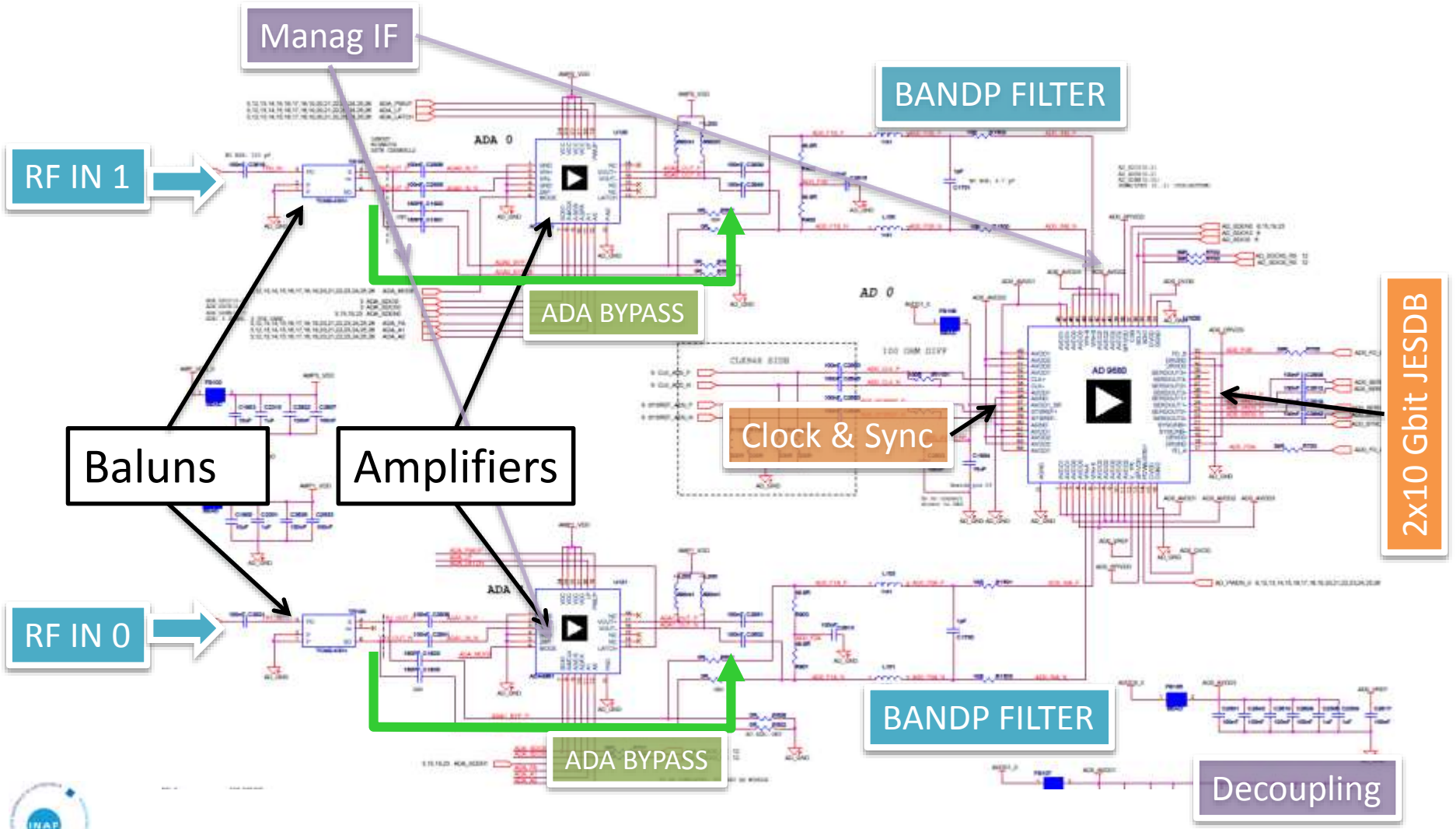
(Power Estimates in SKA Configuration)



TYPICAL PERFORMANCE CHARACTERISTICS



AD schematics



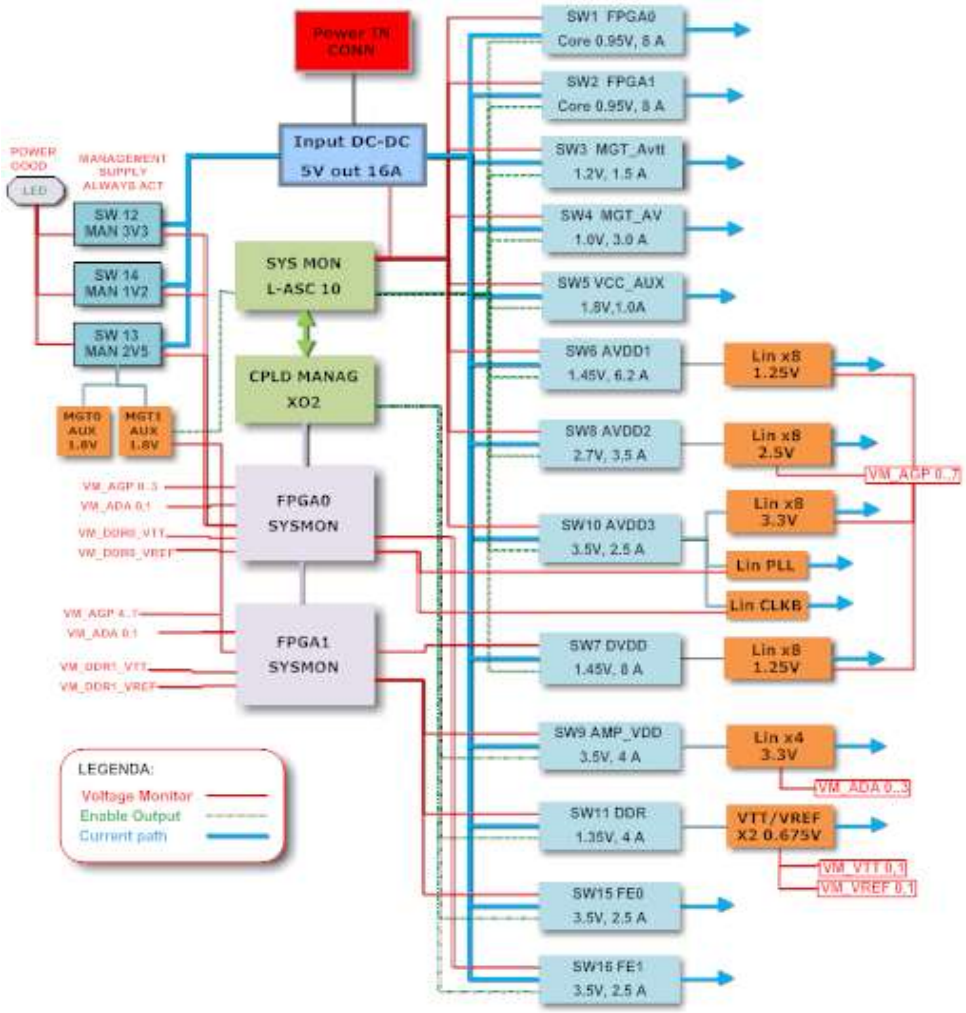
Board Powering

Multi stage PDS

- Hi range 12-48V input DC-DC:
  - Output 5V, up to 20 A
  - High Efficiency, 91-94%
- Digital supply: direct DC-DC
  - Management, FPGA, Memory
- Analog supply: DC-DC + Linear
  - PLL, ADC, Amplifier

Power manager

- Voltage /temperature monitoring
- Current monitoring
- Power sequencing



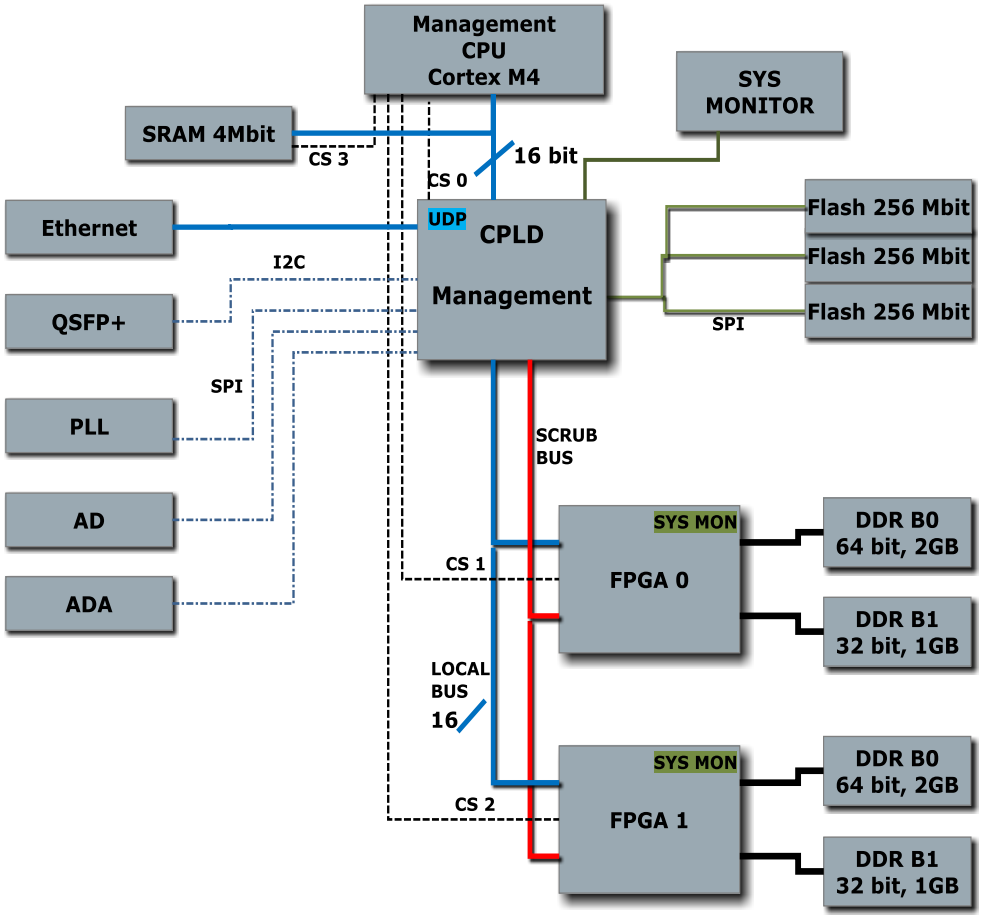
Board Power Est., 2014-2015

Device	Proto 2014	Final 2q 2015	Differences
FPGA, x2, 420 MHz	21,9	21,9	-
AD, x16, 800 MHz	37,5	18,8	New 40 nm from ADI
ADA, x32, gain amplifier	14,4	0	No populated, TBC
Clock (*1)	2,5	2,5	-
DDR3L, x8, 1Ghz	3,4	2,7	New DDR4, TBC
40 GEth & Management	2,8	2,8	-
TOTAL IC	82,7	48,8	
Front panel	16,0	16,0	
Absorbed power (5V):	**98,7**	**64,8**	
Panel absorbed , 12V:	103,9	**68,2**	

(*1) Clock power is a target, TBC

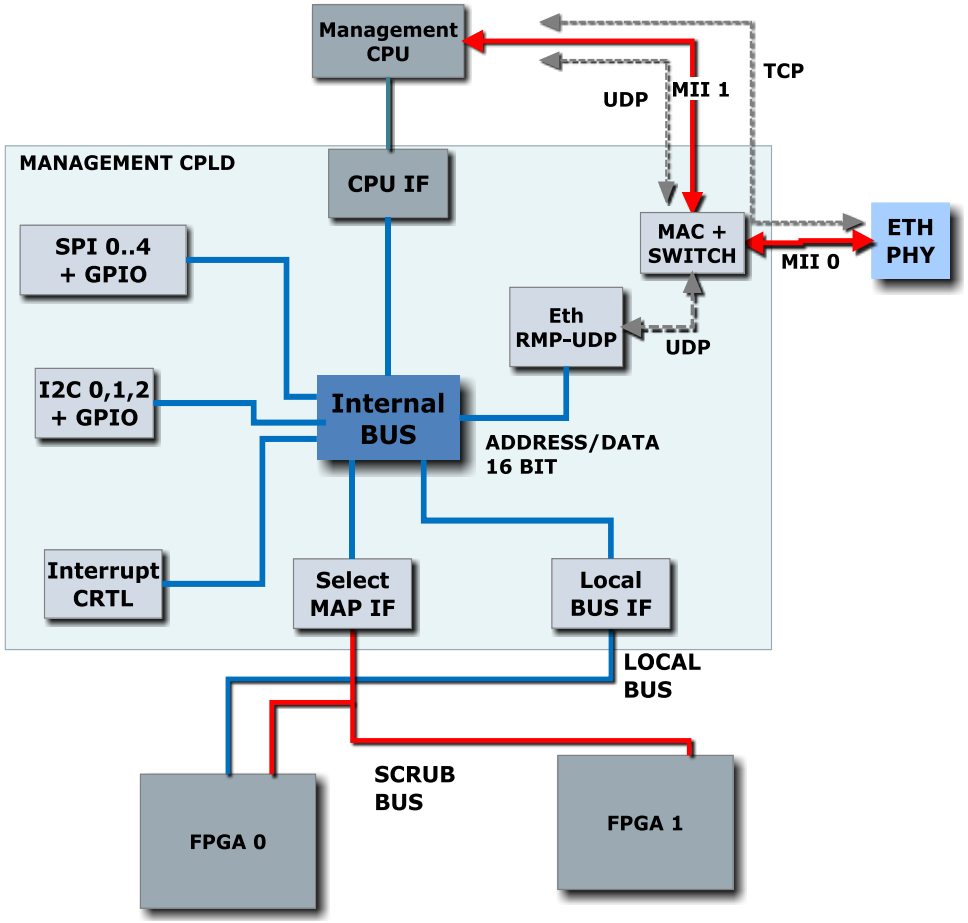
Management

- Voltage/power control
  - absorbed current
  - almost internal voltages
- Board start up
- Health monitor:
  - supply, PLL, FPGA, AD...
- System configuration
  - multiple FPGA bitsrteam
  - receiver board control
- Remote IF Eth
  - UDP direct with CPLD
  - TCP command with CPU



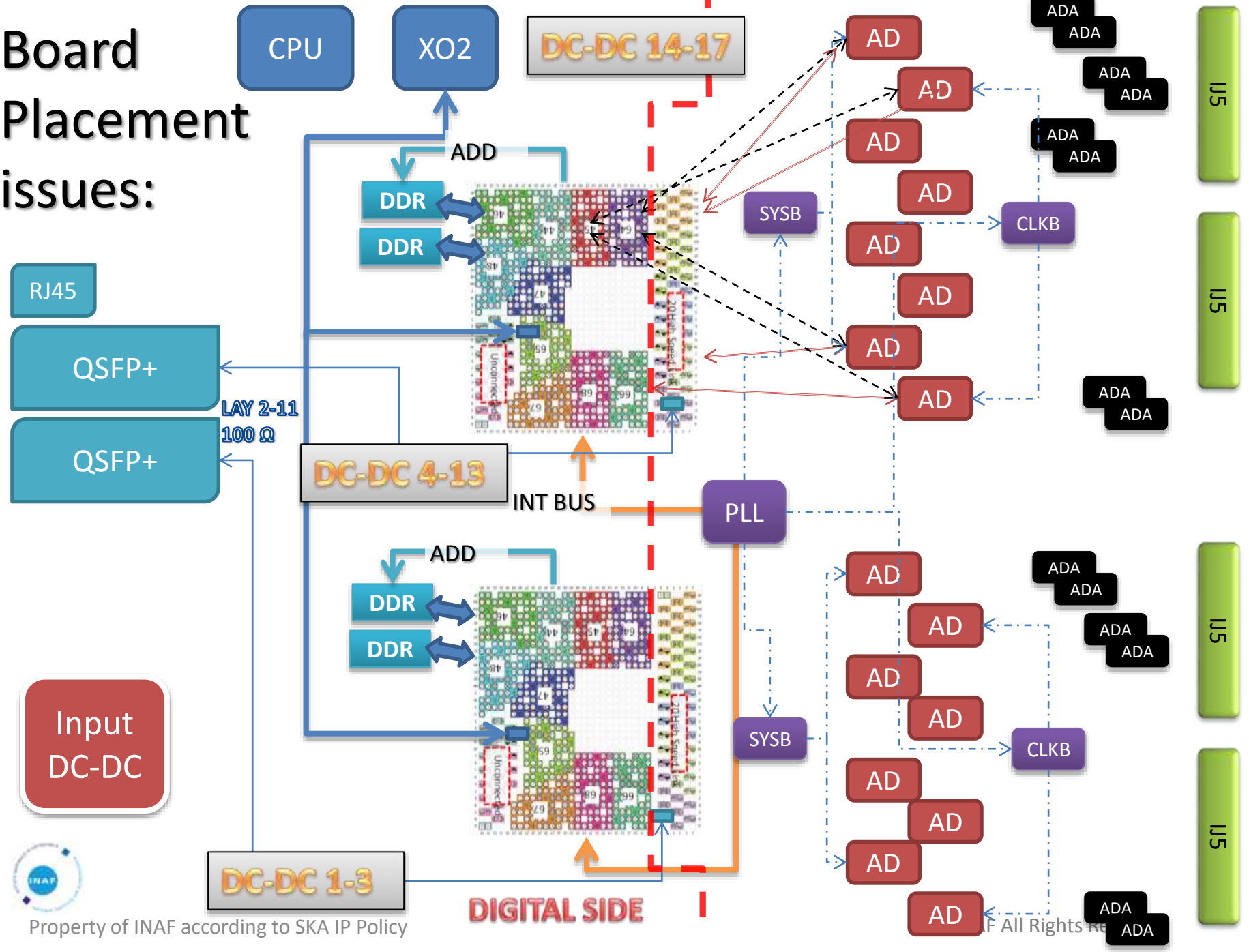
Management CPLD

- Ethernet interface:
  - UDP command with DMA
  - TCP routing to CPU
- FPGA Configuration IF (select map)
  - dynamic fast configuration
  - Radiation Effect monitoring & repair
- Slave serial interfaces
  - I2C, SPI
- Local Bus memory mapped FPGA resources
- Interrupt controller

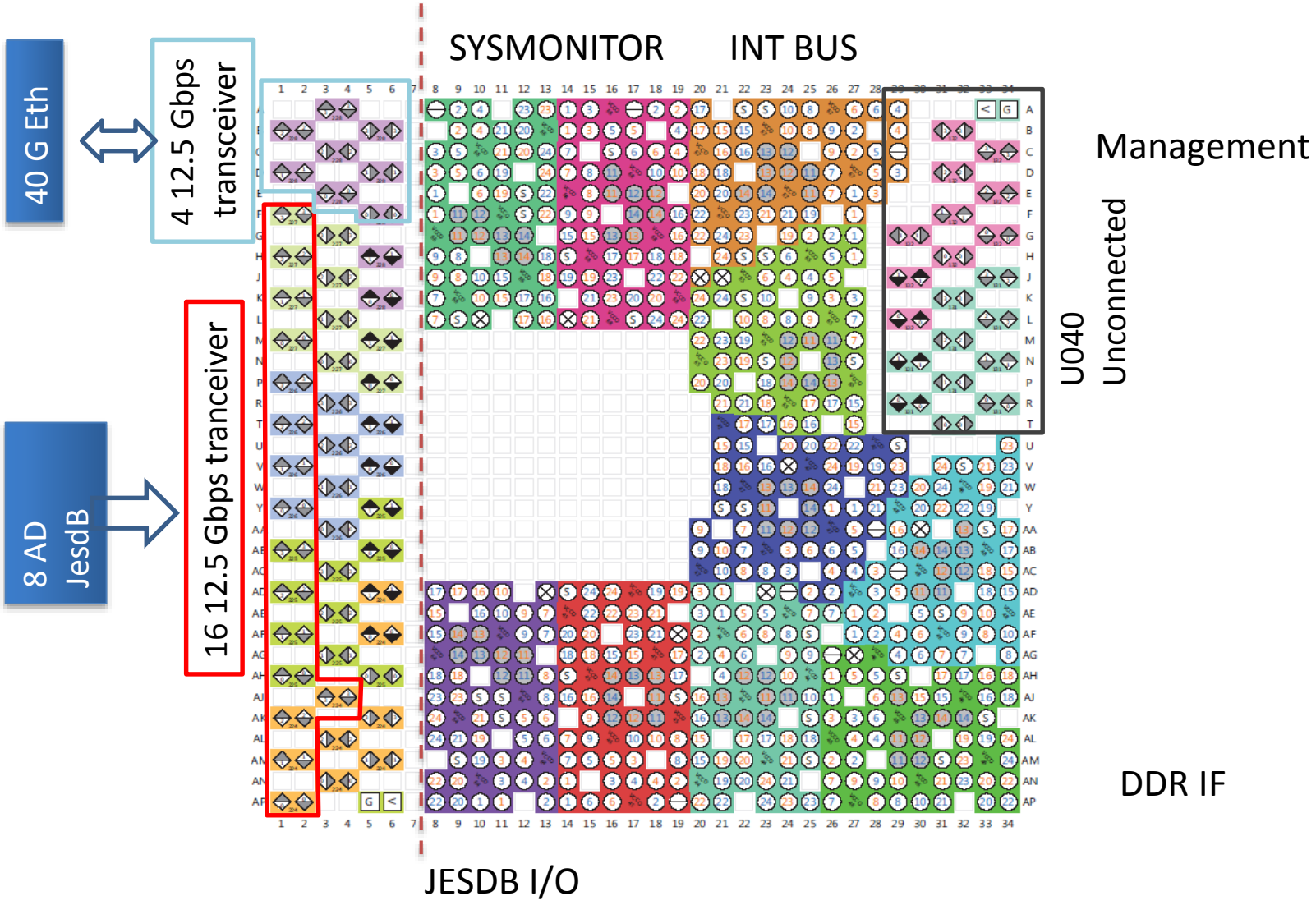


BOARD LAYOUT

Board Placement issues:

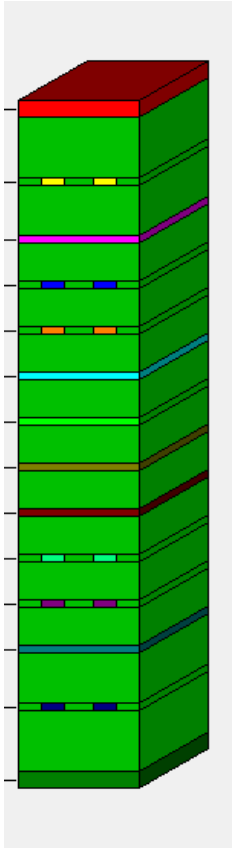


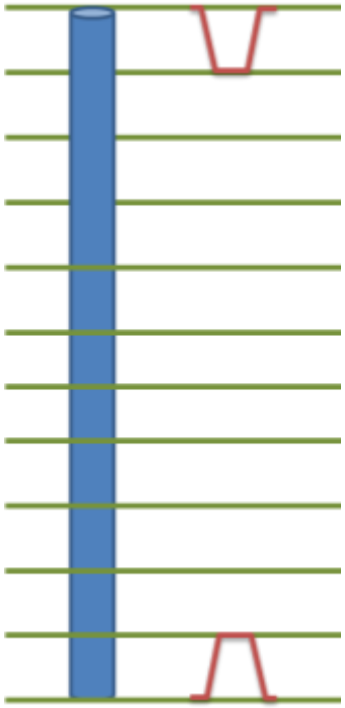
FPGA BANK ASSIGNEMENT



STACKUP (14 LAYERS)

Layer Name	Type	Usage	Thickness um	Er	Test Width um	Z0 ohm	Diff Z0 ohm	Width um	Gap um
1	Metal	Plane	35	<Auto>	150	77.6	100	193.578	100
	Dielectric	Substrate	120	3.7					
2	Metal	Signal	15	<Auto>	150	40	100	84.557	150
	Dielectric	Substrate	100	3.7					
3	Metal	Plane	15	<Auto>	1000	18.4	75	306.356	203.2
	Dielectric	Substrate	75	4.3					
4	Metal	Signal	15	<Auto>	124	39.4	86	92.078	150
	Dielectric	Substrate	75	4.3					
5	Metal	Signal	15	<Auto>	124	39.4	100	69.365	203.2
	Dielectric	Substrate	75	4.3					
6	Metal	Plane	15	<Auto>	1000	9.3	75	138.219	203.2
	Dielectric	Substrate	75	4.3					
13	Metal	Plane	15	<Auto>	254	20.1	75	94.473	203.2
	Dielectric	Substrate	75	4.3					
14	Metal	Plane	15	<Auto>	254	20.1	75	94.473	203.2
	Dielectric	Substrate	75	4.3					
7	Metal	Plane	15	<Auto>	1000	9.3	75	138.219	203.2
	Dielectric	Substrate	75	4.3					
8	Metal	Signal	15	<Auto>	124	39.4	86	98.368	203.2
	Dielectric	Substrate	75	4.3					
9	Metal	Signal	15	<Auto>	124	39.4	76	119.834	150
	Dielectric	Substrate	75	4.3					
10	Metal	Plane	15	<Auto>	1000	18.4	75	306.356	203.2
	Dielectric	Substrate	100	3.7					
11	Metal	Signal	15	<Auto>	100	49.3	90	101.457	124
	Dielectric	Substrate	120	3.7					
12	Metal	Plane	35	<Auto>	150	77.6	75	551.498	203.2

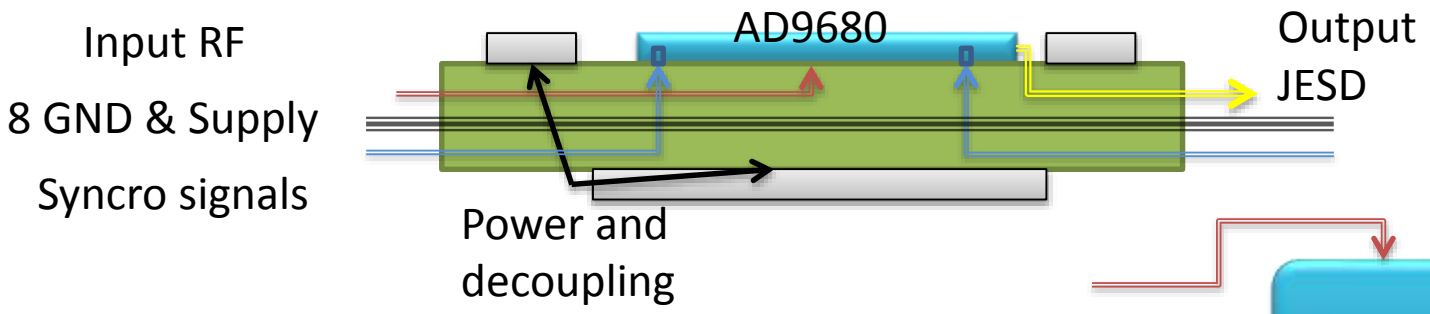




SKA TPM STACK UP AREAS

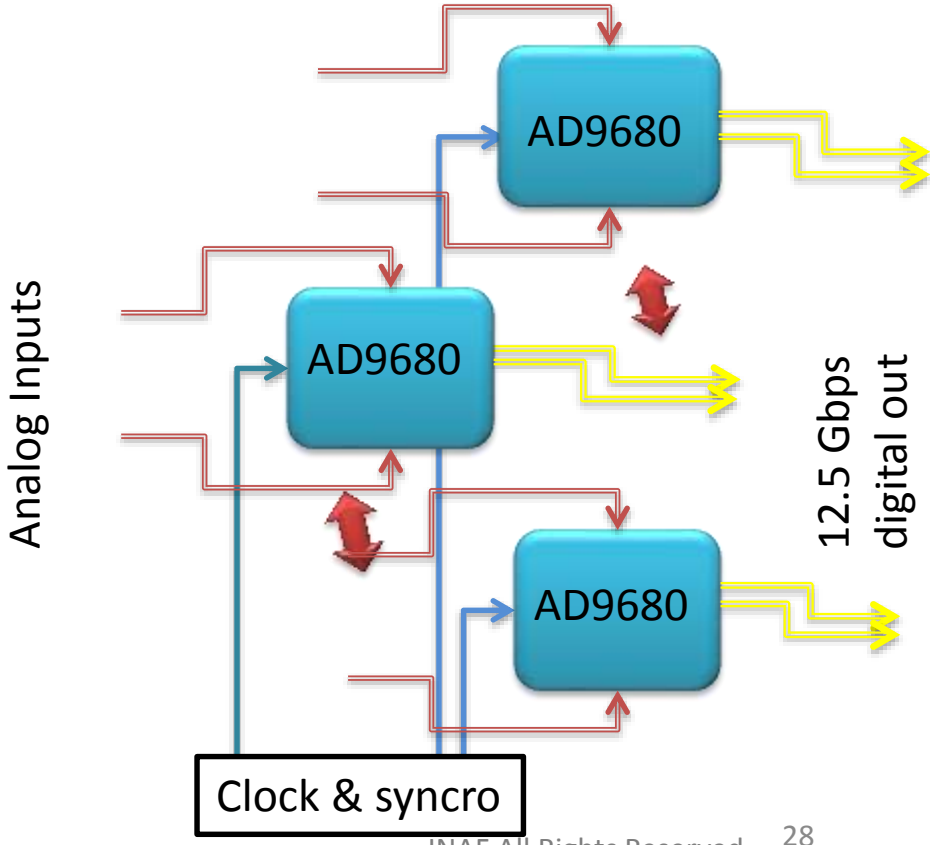
		MANAG	DDR COL.	MGT COL.	AD PDS	AD
1	SHLD/comp	SHLD/comp	SHLD/comp	SHLD/comp	SHIELD/comp	SHIELD/comp
2	50 Ω	50 Ω	Supply 0 HF	Supply 0 HF	strip 100 Ω d	strip 100 Ω d
3	GND	GND	GND	GND	AGND	AGND
4	SIGN 40 Ω	SIGN 40 Ω	SIGN 40 Ω		SW_AVDD1	AVDD1, DVDD
5	SIGN 40 Ω	SIGN 40 Ω	SIGN 40 Ω		AGND	AGND
6	Supply 1	MAN_1V2	DDR_VDD	MGT_AV	SW_AVDD2, SW_AMP_VDD	AVDD2
7	Supply 2	MAN_2V5	MAN_2V5	MGT(i)_AUX	AGND	AGND
8	Supply 3	5V0	5V0	CORE(0,1)	SW_AVDD3	AVDD3,DRVDD AMP_VDD
9	Supply 4	MAN_3V3	Vcc_AUX	MGT_AVTT	AGND	AGND
10	40 Ω /Supply 5	SIGN 40 Ω	SIGN 40 Ω		SW_DVDD	40 Ω
11	40 Ω/Supply 6	SIGN 40 Ω	SIGN 40 Ω		40 Ω	40 Ω
12	GND	GND	GND	GND	AGND	AGND
13	50 Ω/Supply 7	50 Ω			strip 100 Ω d	strip 100 Ω d
14	SHLD/comp	SHLD/comp			SHLD/comp	SHLD/comp

ADC related issues (partial)



Device specific positioning and layout issues:

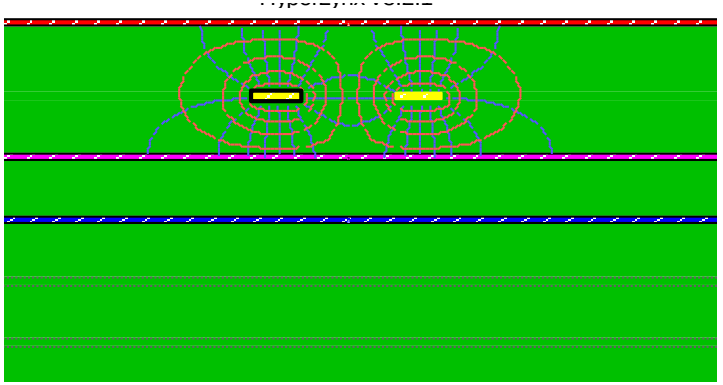
- HS signal routing (16 device in 233 mm board height)
- Staggered placement
- Clock and Sync routing

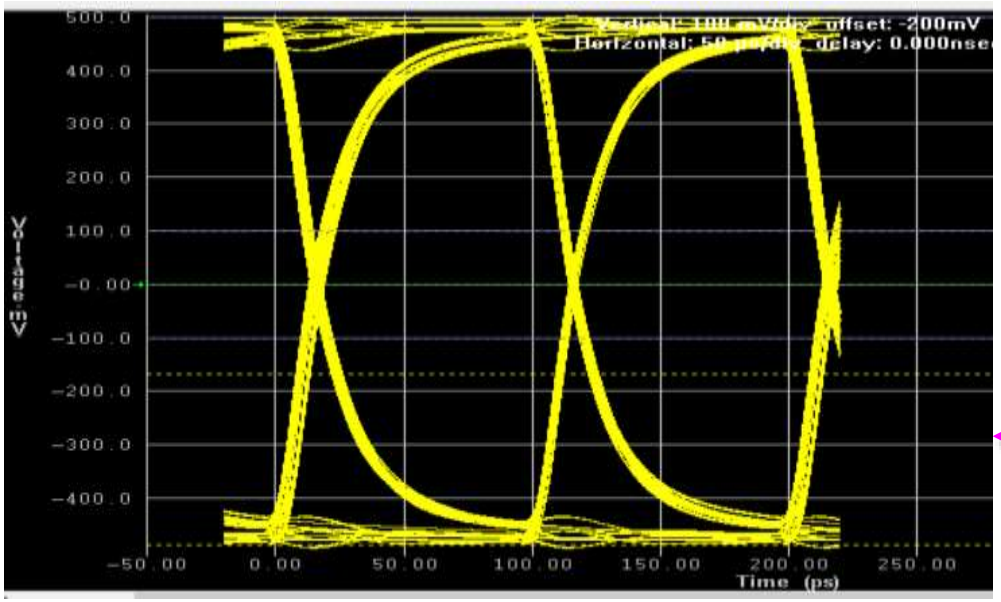


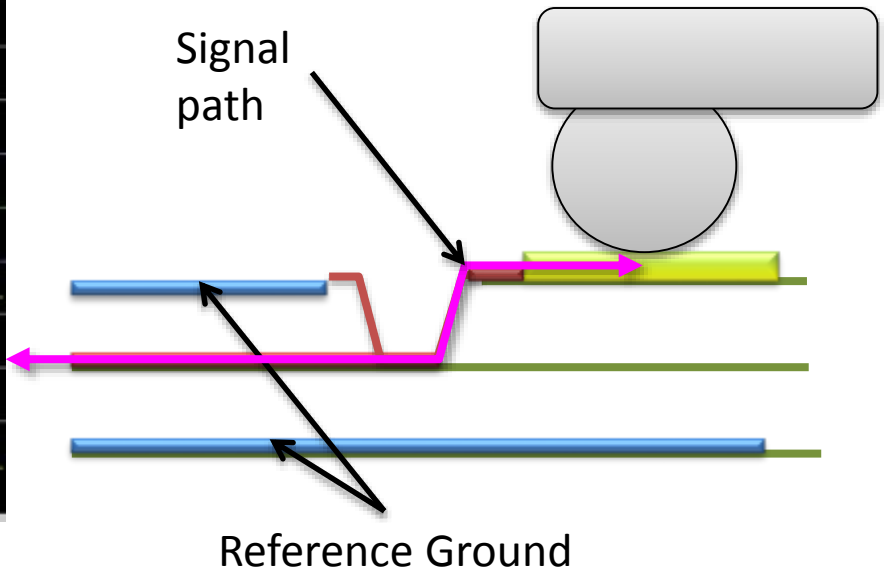
Stripline technology, 10 G JESDB, 10Geth, Analog Signal, Analog clocks

Stripline on Layer 2, 13

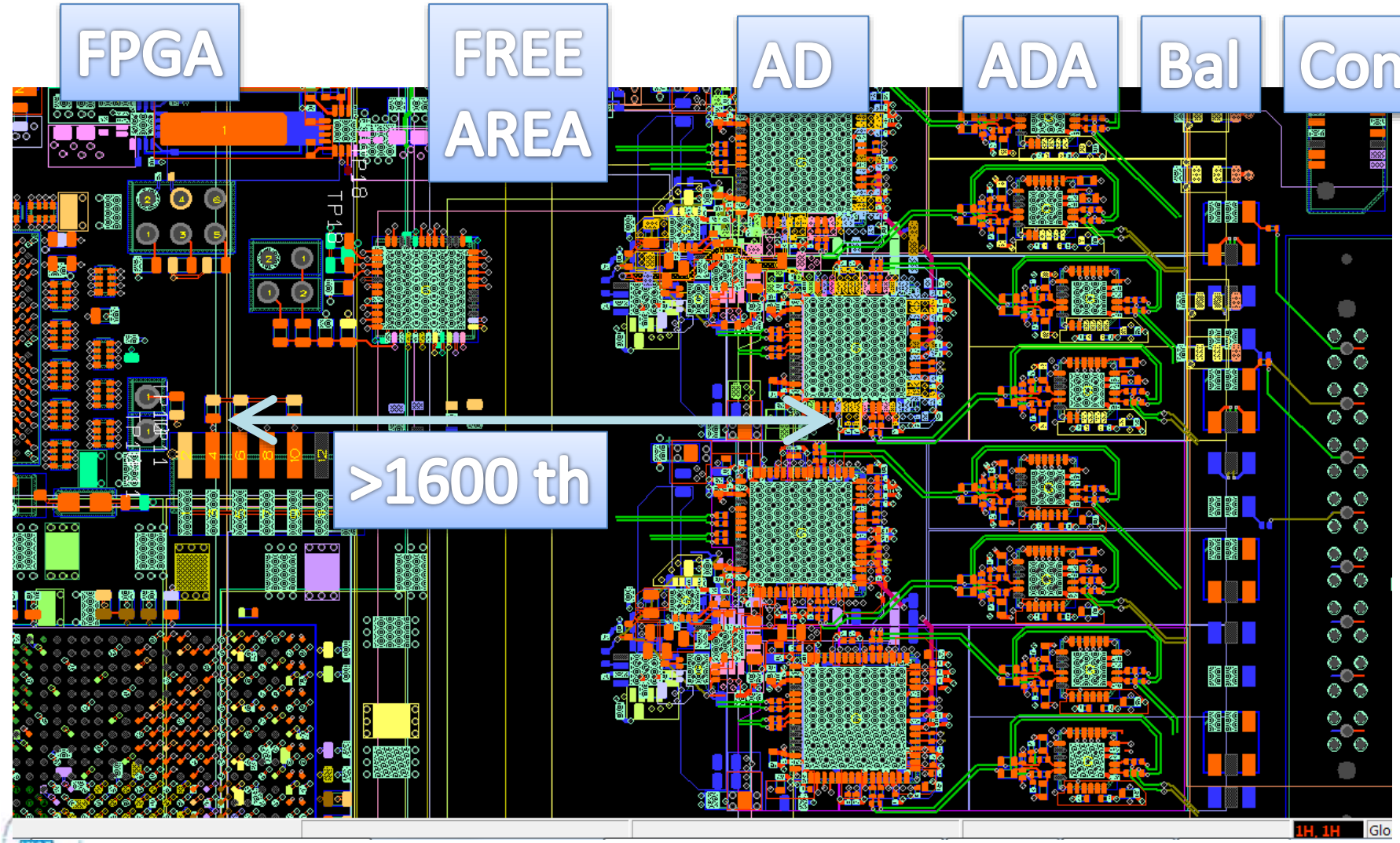
- External shield, layer 1, 14
- Reference GND plane, layer 3, 12



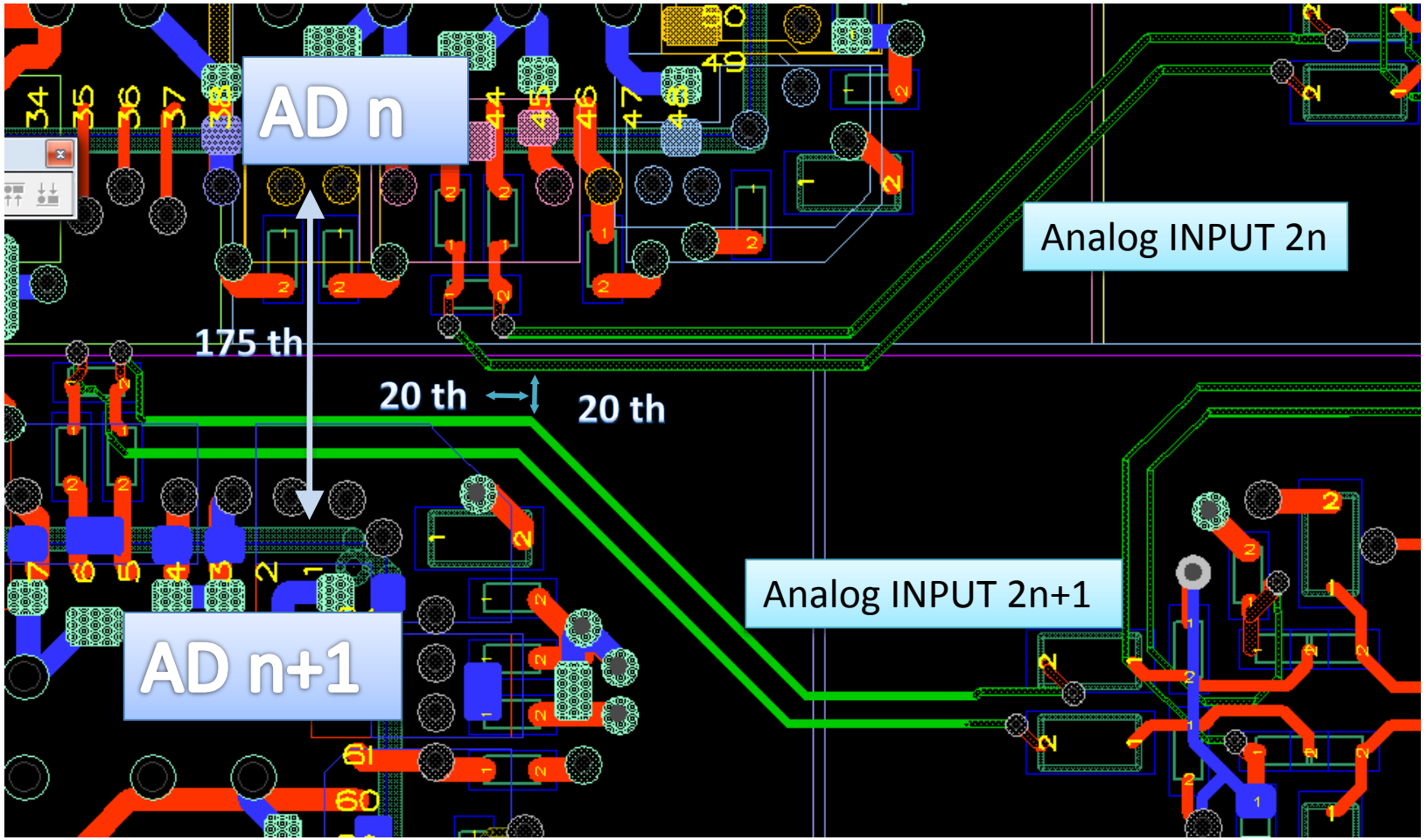




x 4 AD Layout overview



AD input details



THANKS !!!