ROACH to SKARAB

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… or …


ROACH
Reconfigurable Open Architecture
Computing Hardware

Outline

- SKA South Africa
- MeerKAT
- CASPER
- Rapid Application Development
- ROACH 1 & 2
- A wishlist for a next-generation platform...
- SKARAB

SKA S. Africa

- Bid to host SKA
- Built KAT-7
- Busy with MeerKAT
- African VLBI Network
- Other Collaborations

SKA South Africa

- Engineering Office in Cape Town
- Johannesburg Office (Infra)
- Karoo (Klerefontein, Losberg)

- Total staff complement: 182
  - Cpt: 119
  - Jhb: 28
  - Karoo: 34
  - HartRAO: 1

MeerKAT

http://roadtravelafrica.com/2010/11/26/meerkats/

MeerKAT

- Under construction
- Completion end 2016
- 64 x 13.5 m diameter Offset Gregorian Antennas
- Sub 30K T_{sys}
- Sensitivity in L band ~ 300m^2/K
- 8km baselines
- “Sensitivity is king and dynamic range is the dominant queen”

MeerKAT Science – Priority Group 1

- Priority Group 1
  - Radio Pulsar Timing: Testing Einstein's theory of gravity and gravitational radiation - Investigating the physics of enigmatic neutron stars through observations of pulsars.
  - LADUMA (Looking at the Distant Universe with the MeerKAT Array) - An ultra-deep survey of neutral hydrogen gas in the early universe.

MeerKAT Science – Priority Group 2

- MESMER (Search for Molecules in EOR)
- MeerKAT Absorption Line Survey for H and OH lines
- MHONGOOSE (MeerKAT HI Observations of Nearby Galactic Objects: Observing Southern Emitters)
- TRAPUM (Transients and Pulsars with MeerKAT)

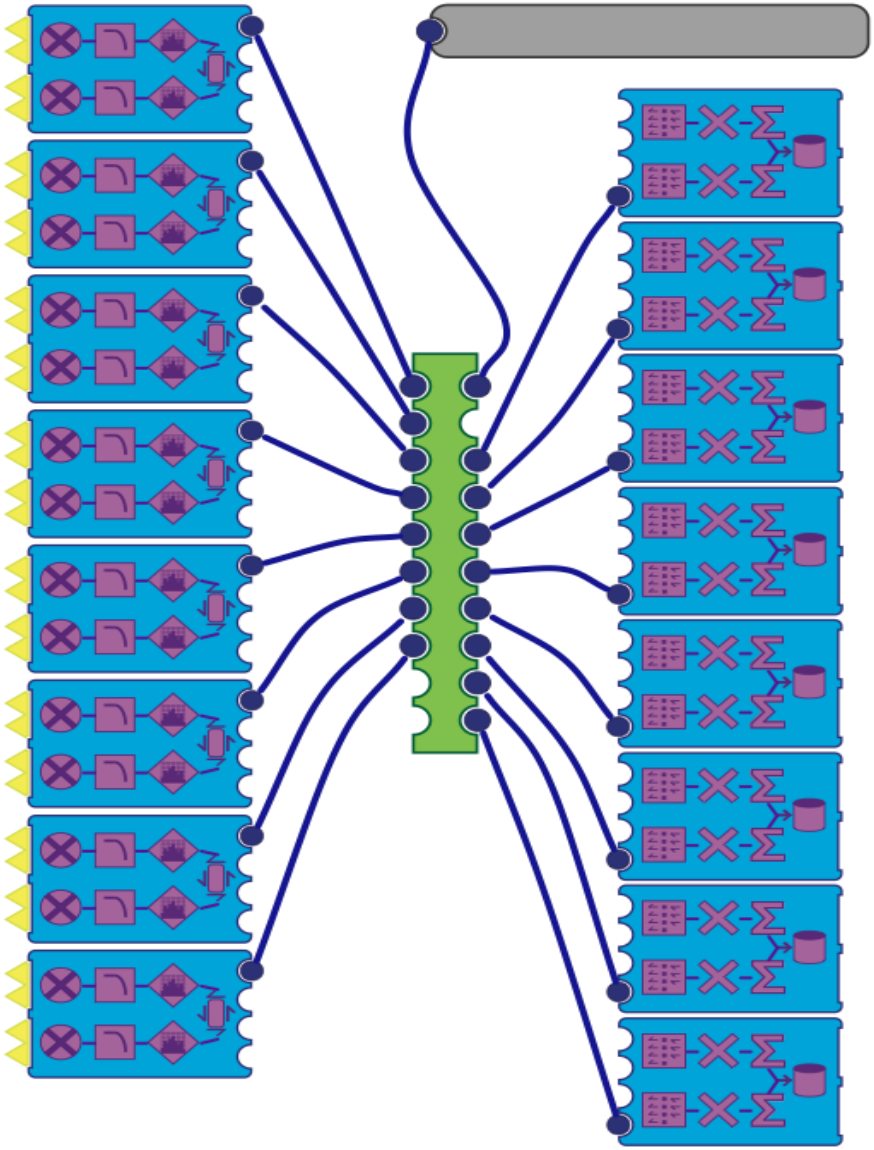
MeerKAT Science – Priority Group 2

- A MeerKAT HI Survey of the Fornax Cluster (Galaxy formation and evolution in the cluster environment).
- MeerGAL (MeerKAT High Frequency Galactic Plane Survey)
- MIGHTEE (MeerKAT International GigaHertz Tiered Extragalactic Exploration Survey)
- ThunderKAT (The Hunt for Dynamic and Explosive Radio Transients with MeerKAT)

CASPER

- Reduce development time, deploy later technology
- Common tools (HW, SW, GW)
- Freely available
- Matlab-Simulink -> Xilinx ISE (Vivado in next gen)

Lego for DSP



Sum / Integrate

Data Reorder / Transposer

Data Select / Route

Cross - Correlate

Polyphase Filterbank

To Memory Buffer

FIR Filter

Mix / Multiply

Single ADC

Dual ADC

10 GbE Switch

Commodity CPU

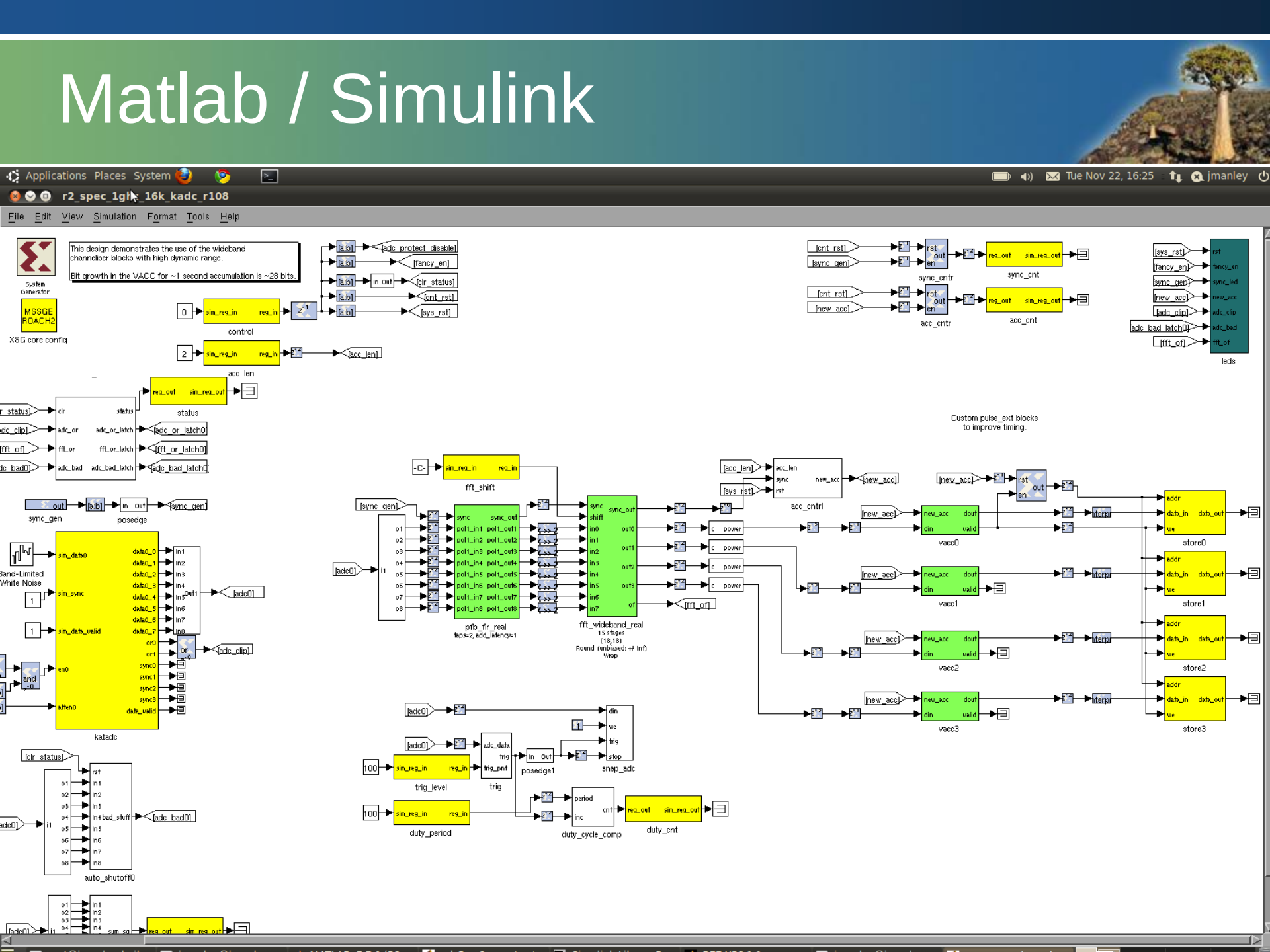
ROACH Board

Interconnect...

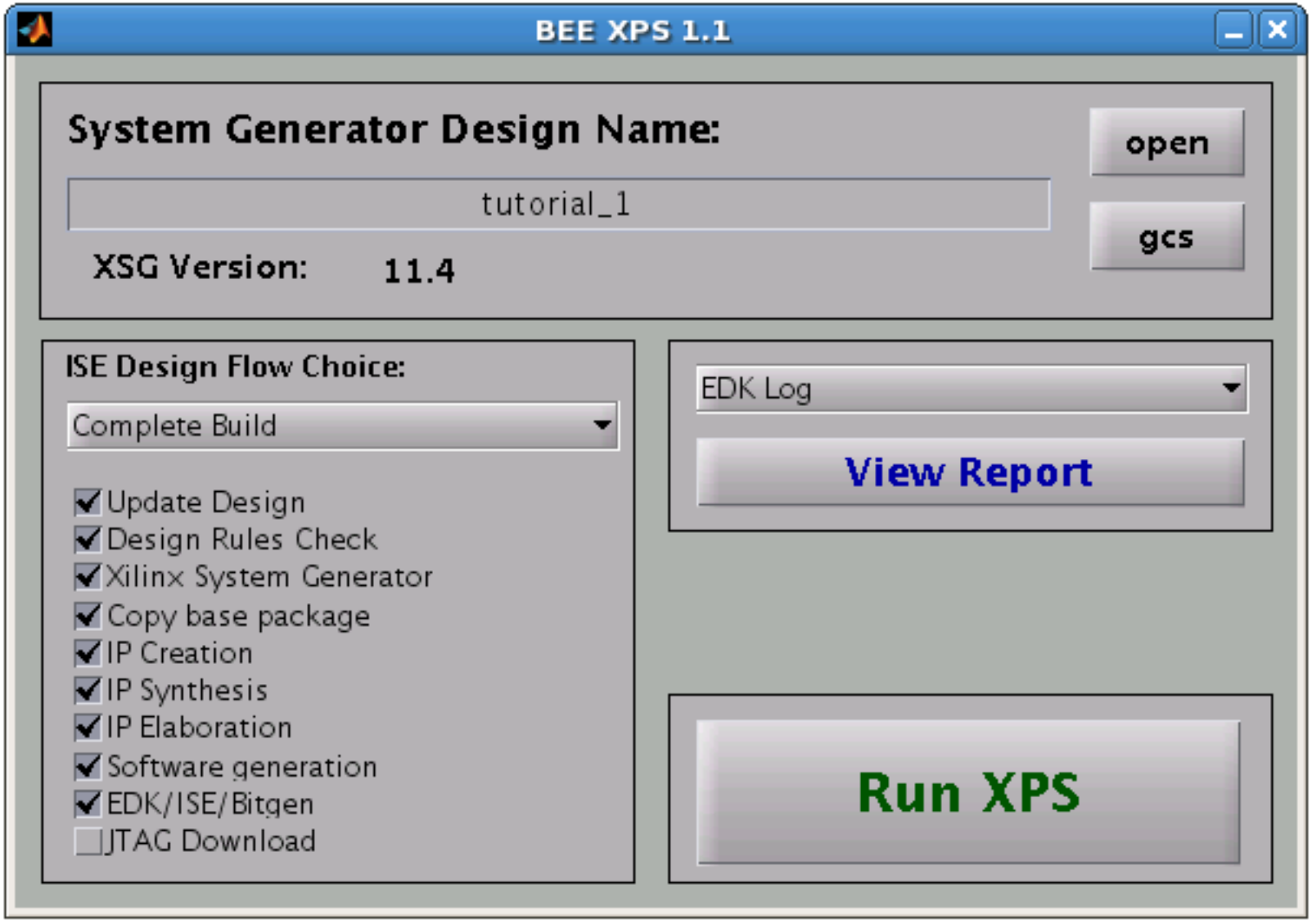
Ethernet interconnect +/-

- **Likes:**
  - **Multicasting support**
  - **Cheap to implement – FPGA's provide hard macros**
  - **Resilient to errors**
  - **Scalable and Flexible**
  - **Interface to many diverse technologies**
  - **Simplified debugging and development**
  - **Simplified Interfacing to adjacent systems**
  - **Long lifetime, enables modular upgrade > 30yr compatibility lifetime**
  - **Multiplexing and demultiplexing signal streams is trivial**
- **Dislikes:**
  - **Inherent asynchronicity complicates FPGA development**
  - **Some quirks to deal with (eg. Packet to self)**

Matlab / Simulink



One click (v 0)


BEE XPS 1.1
System Generator Design Name:
open
tutorial_1
gcs
XSG Version: 11.4
ISE Design Flow Choice:
Complete Build
Update Design
Design Rules Check
Xilinx System Generator
Copy base package
IP Creation
IP Synthesis
IP Elaboration
Software generation
EDK/ISE/Bitgen
JTAG Download
EDK Log
View Report
Run XPS

Parameterised Blocks

Function Block Parameters: pfb_fir_real

pfb_fir_real (mask)

Fold adders into DSPs: Causes adders to be absorbed into DSP blocks (supported in Virtex5)
Adder implementation: Cores using Fabric or DSP48 or behavioral HDL

Parameters

Size of PFB: (2^? pnts)

12

Total Number of Taps:

4

Windowing Function: hamming

Number of Simultaneous Inputs: (2^?)

2

Make Biplex

0

Input Bitwidth:

8

Output Bitwidth:

18

Coefficient Bitwidth:

OK Cancel Help Apply

The Good...

- **Likes:**
  - **Fantastic data oriented design language**
  - **Rapid Application Development**
  - **GUI environment**
  - **Cross-platform (OS) support for development**
  - **Configurable, parameterised, modular library**
  - **Powerful MATLAB scripting environment**
  - **Clock-cycle accurate simulations**
  - **Tunable – can trade resources between DSP/Logic/BRAM**
  - **Abstract away low-level functions**
    - **Clocks**
    - **HW/SW i/f's**
    - **One-click building**

The Bad...

- **Challenges:**
  - **GUI based third party software changes are outside our control**
  - **Vendor lock-in is hard to avoid, requires investment**
  - **No effective multi-clock domain support**
  - **Verification**
  - **Library Maintenance**
  - **Revision Control**
  - **IP management – Open Source model may not be acceptable to all?**

CASPER - ROACH

ROACH2

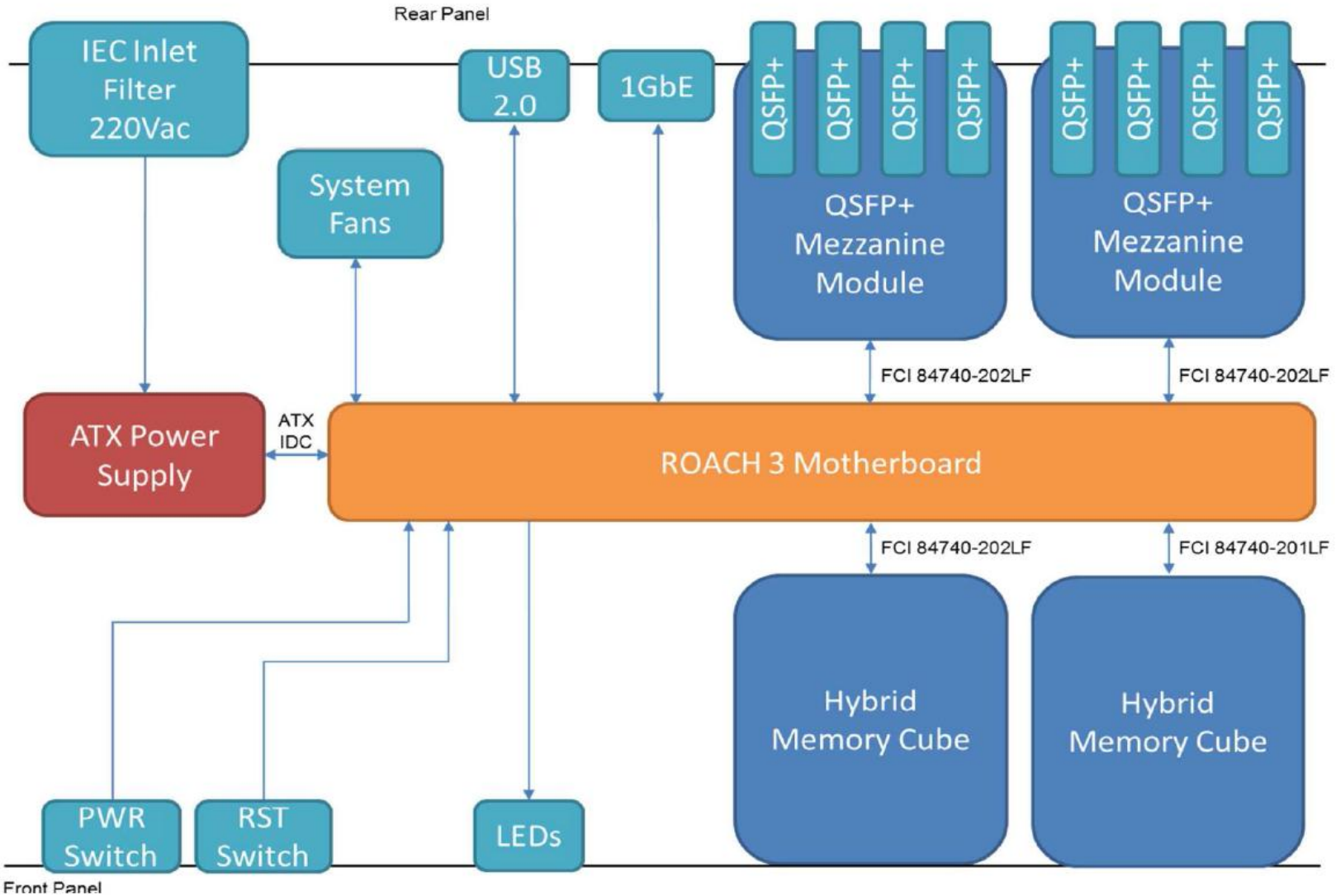
Some Lessons Learnt

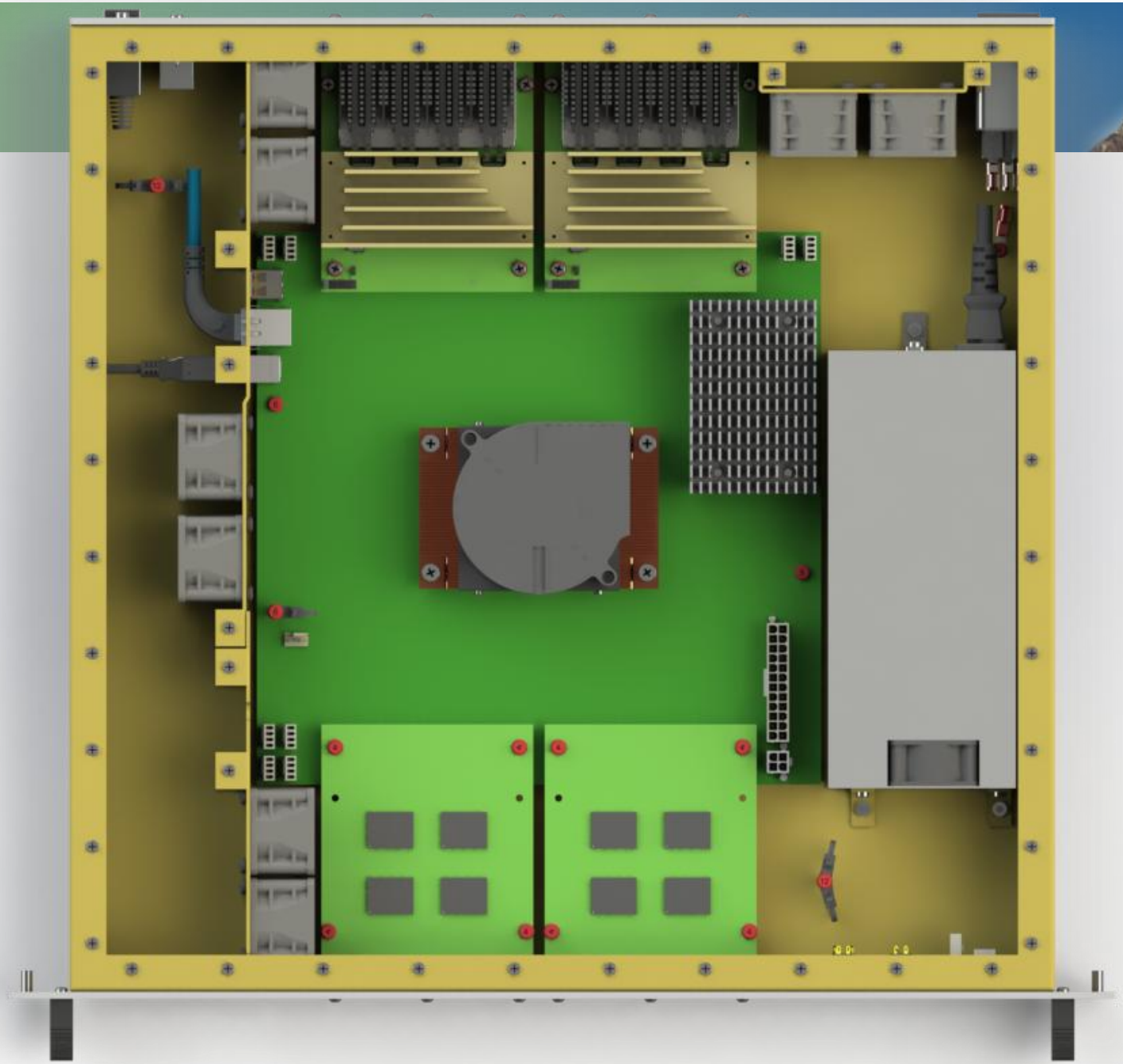
- **HW is valuable, but short-lived**
- **SW and IP investment is much larger**
- **On-FPGA processors come and go – SW investment unpredictable**
- **Must enable re-use, across institutions, devices and generations (parameterisation)**
- **Turnkey solution required, enable designers to implement instruments**
- **Production yield must be considered**
- **Scaling limits must be eliminated – in both directions if possible**

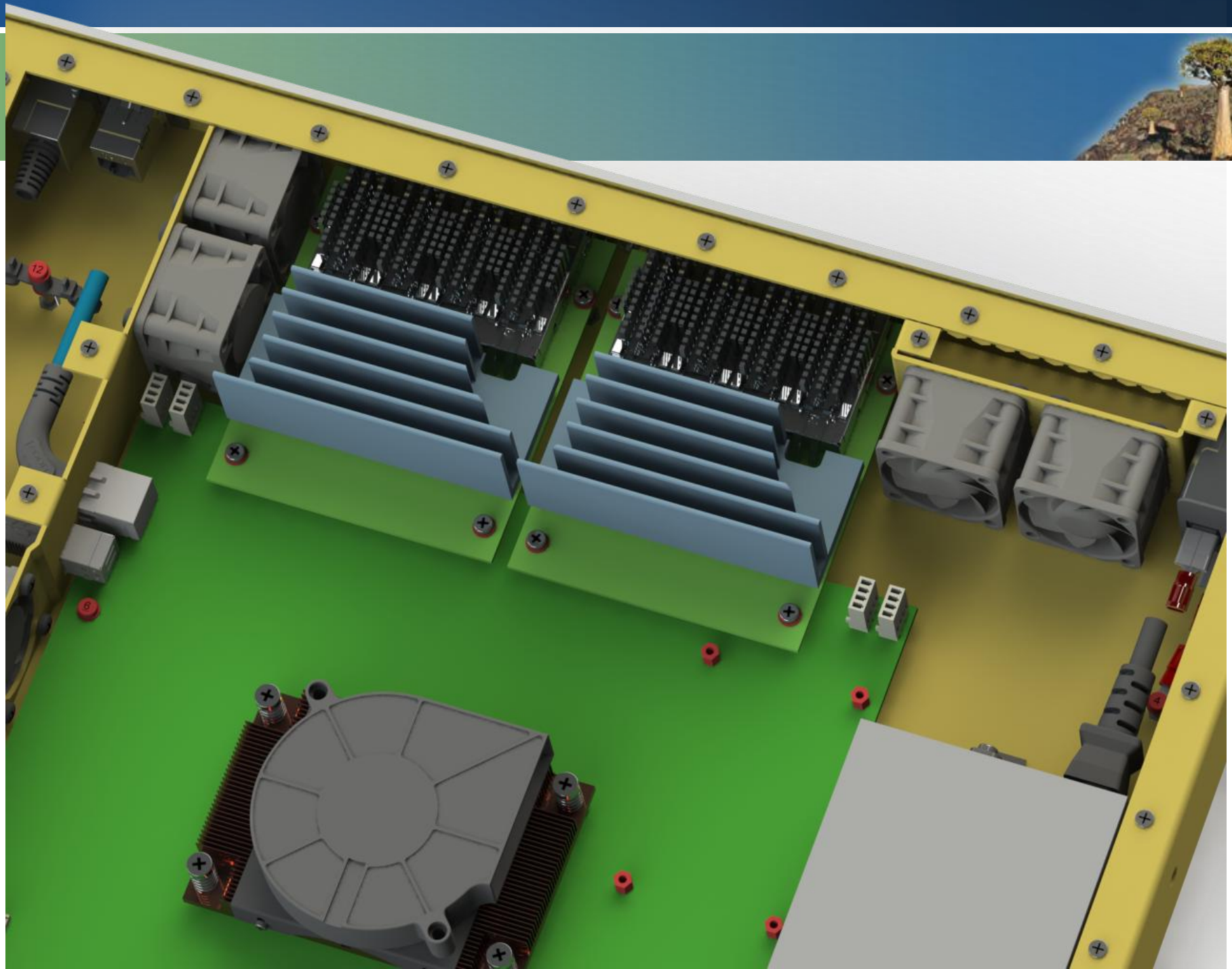
Next-gen Platform Wishlist

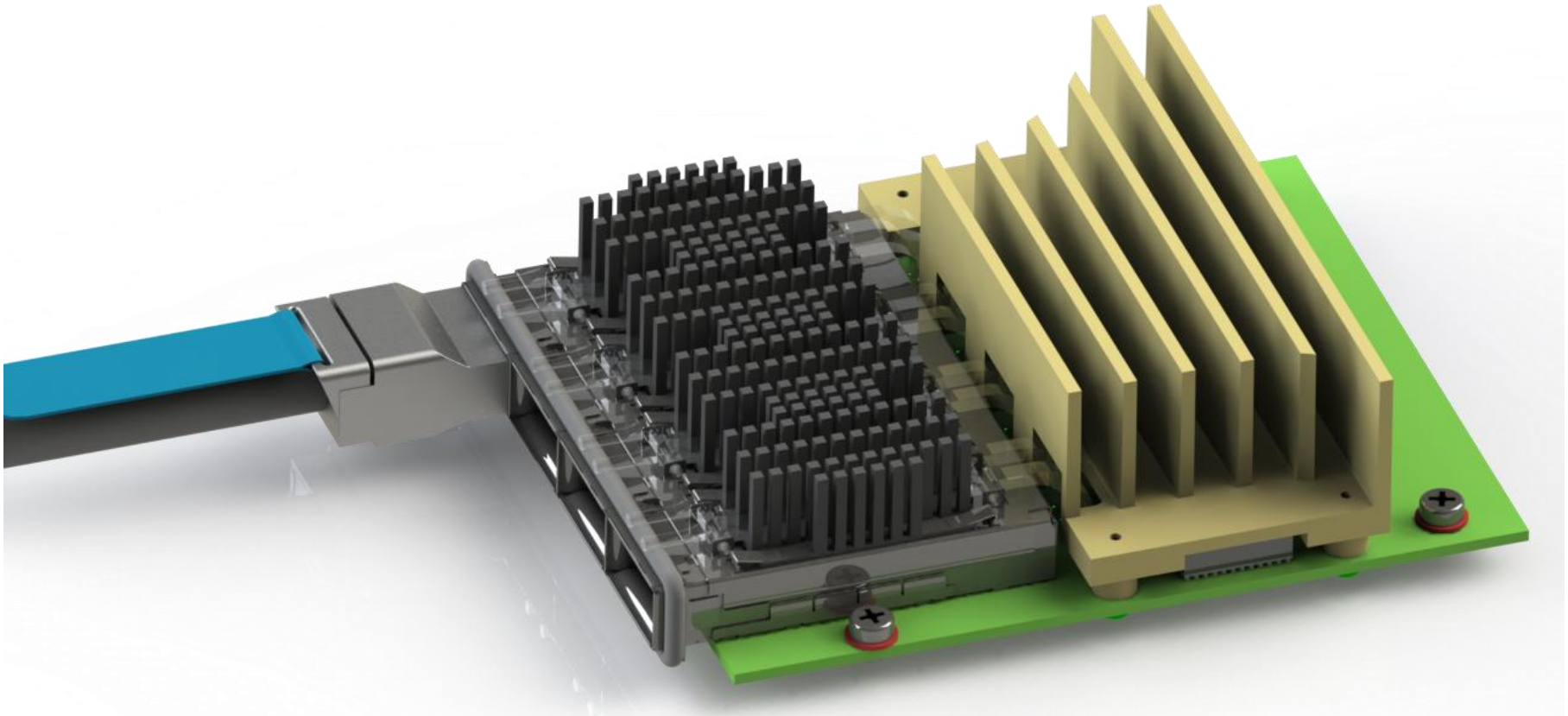
- **IO (many astronomy instruments are IO dominated)**
- **Unified Interconnect – both infra- and intra-board/chassis/rack**
- **Balanced Bandwidth – external IO and internal memory bandwidth matched**
- **Memory to Processing Ratio must be suitably high – both internal and external**
- **Prefer SRAM to DRAM**
- **Keep it simple! – 1 FPGA per board ROACH1/2/3**
- **Implement functions in hardware where possible**
- **Standalone operation is really useful – on-board processor is indispensible sometimes**
  - **Allows development on/deployment of a single board**
- **Remote reboot/reload/hw management**
- **SW support system – think ecosystem**
- **Drag and drop functions – re-use**

The Future


Rear Panel
IEC Inlet Filter 220Vac
USB 2.0
1GbE
QSFP+
QSFP+
QSFP+
QSFP+
QSFP+ Mezzanine Module
QSFP+
QSFP+
QSFP+
QSFP+
QSFP+ Mezzanine Module
System Fans
FCI 84740-202LF
FCI 84740-202LF
ATX Power Supply
ATX IDC
ROACH 3 Motherboard
FCI 84740-202LF
FCI 84740-201LF
Hybrid Memory Cube
Hybrid Memory Cube
PWR Switch
RST Switch
LEDs
Front Panel

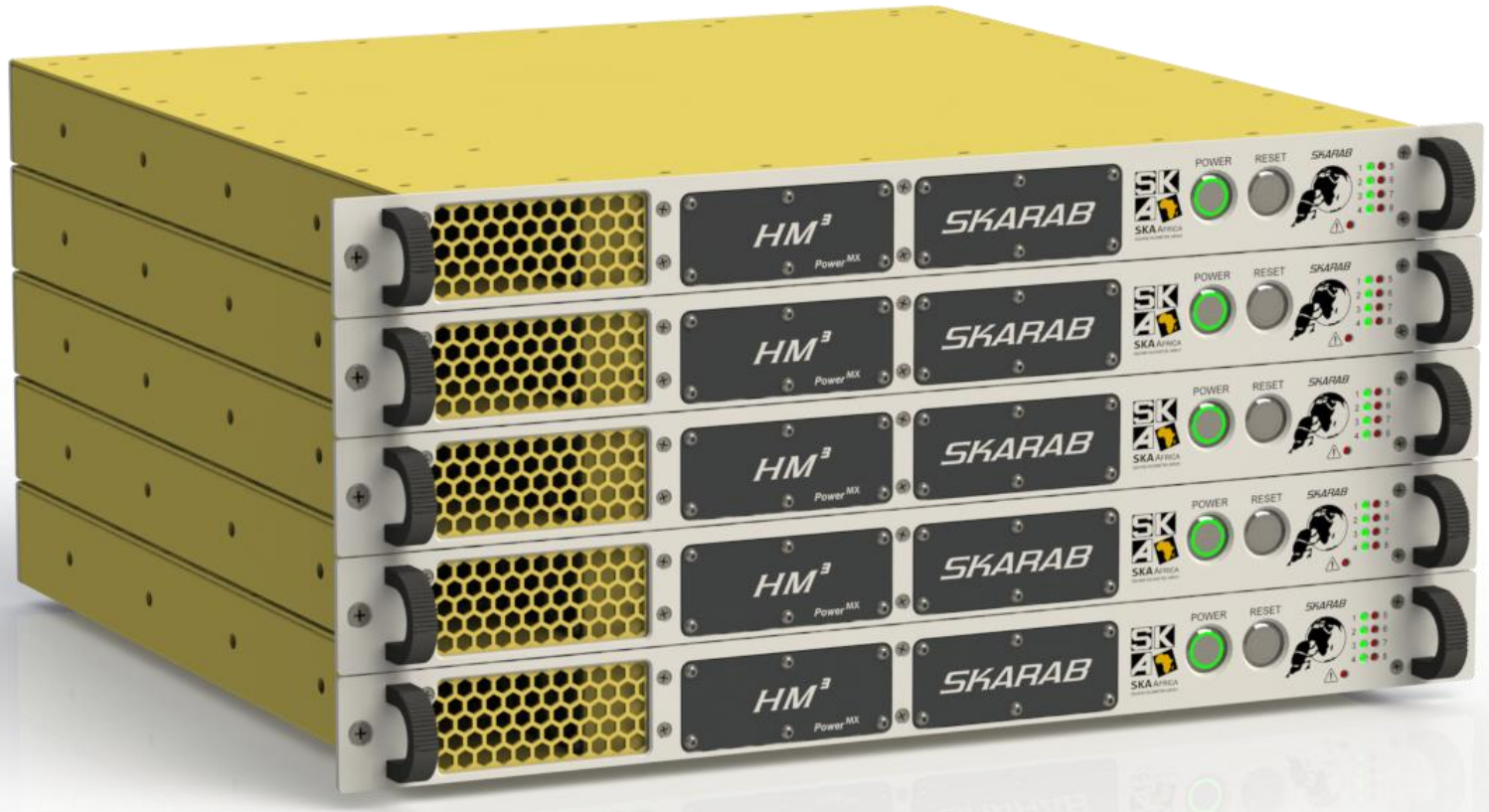






Mezzanines

- Day 1:
  - 40 GbE
    - Passive
    - Active
  - Hybrid Memory Cube
- Future
  - ADC
  - Optical i/f to ADC
  - PCIe?
  - Others?


HM³
Power MX
SKARAB
POWER
RESET
SKARAB
SKA AFRICA