High Performance Processing & Large Area Tracking systems for High Luminosity LHC

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High Performance Signal Processing 2014,

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Valleta, MALTA

Outline

- High Luminosity Large Hadron Collider at CERN: What is it, When and Why?
- The Large Area Tracking systems at LHC: now and in the next decade.
- Why do they need HPC?
- Solutions to satisfy these needs: R&D, Full custom and Collaboration with High Tech Industry
- Concluding remarks & perspectives…

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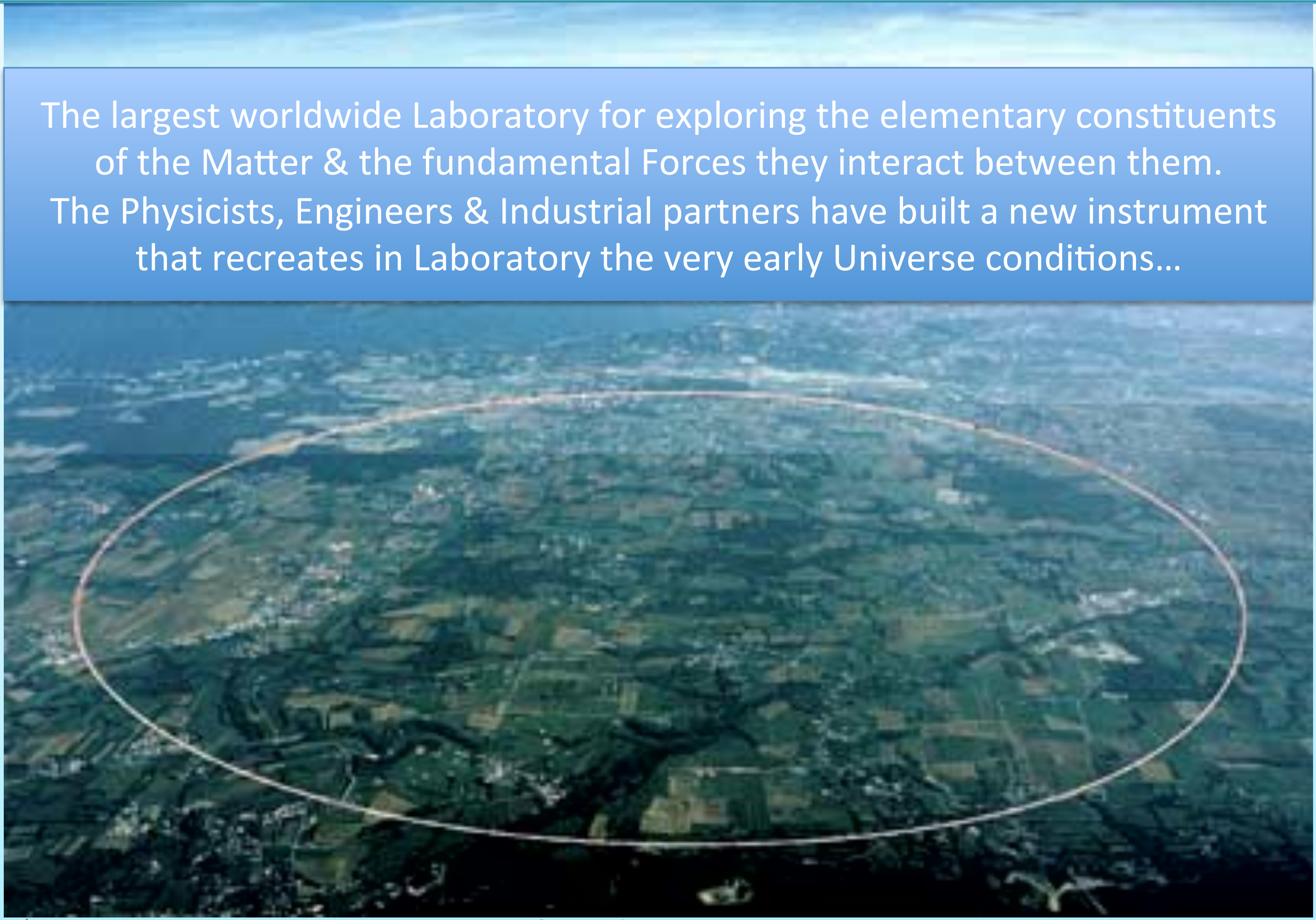
The LHC is a global enterprise

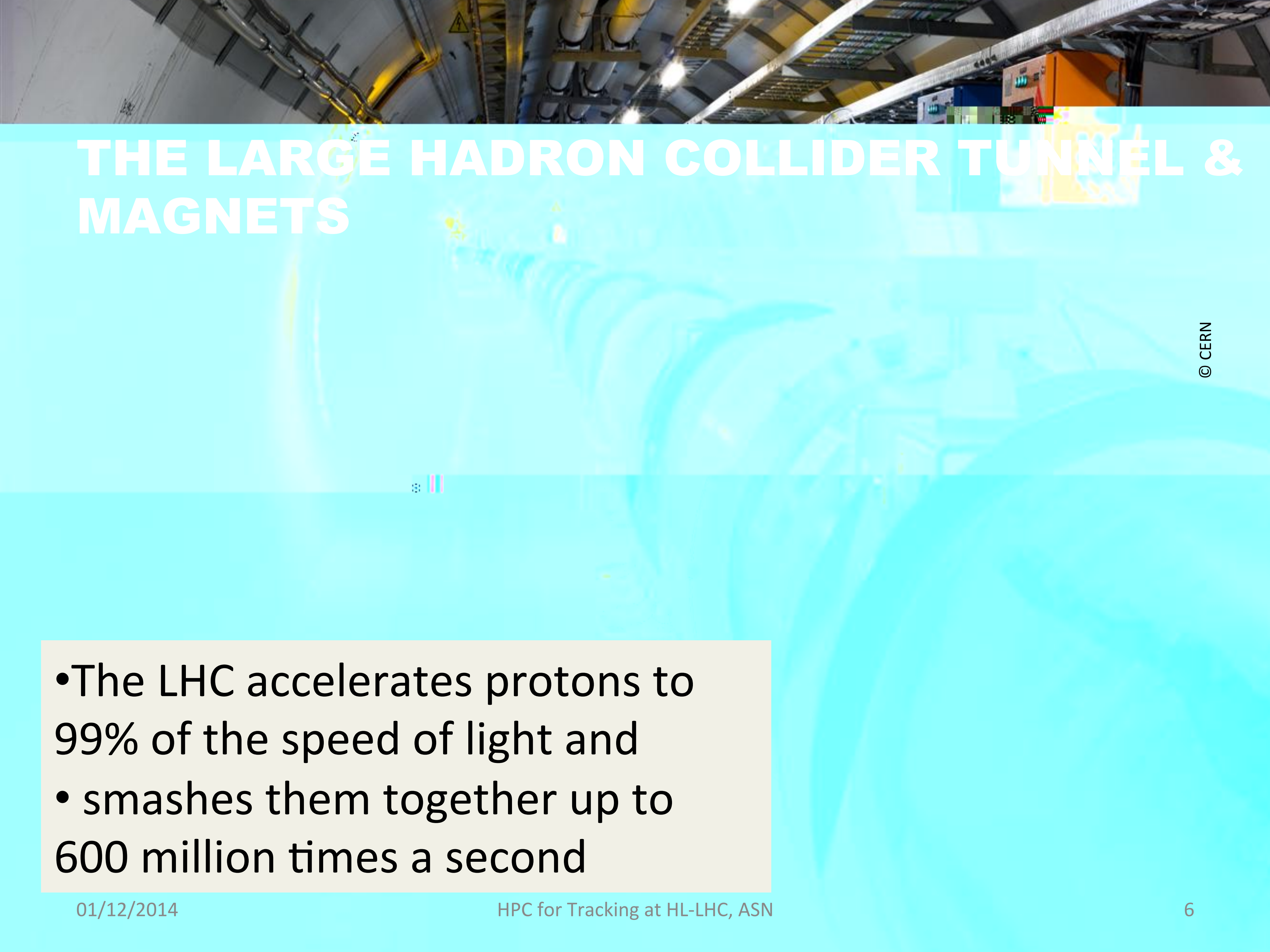
Building the LHC took 18 years and brought together 10,000 people from 60 countries.

The Large Hadron Collider at CERN also known as the Big Bang Machine

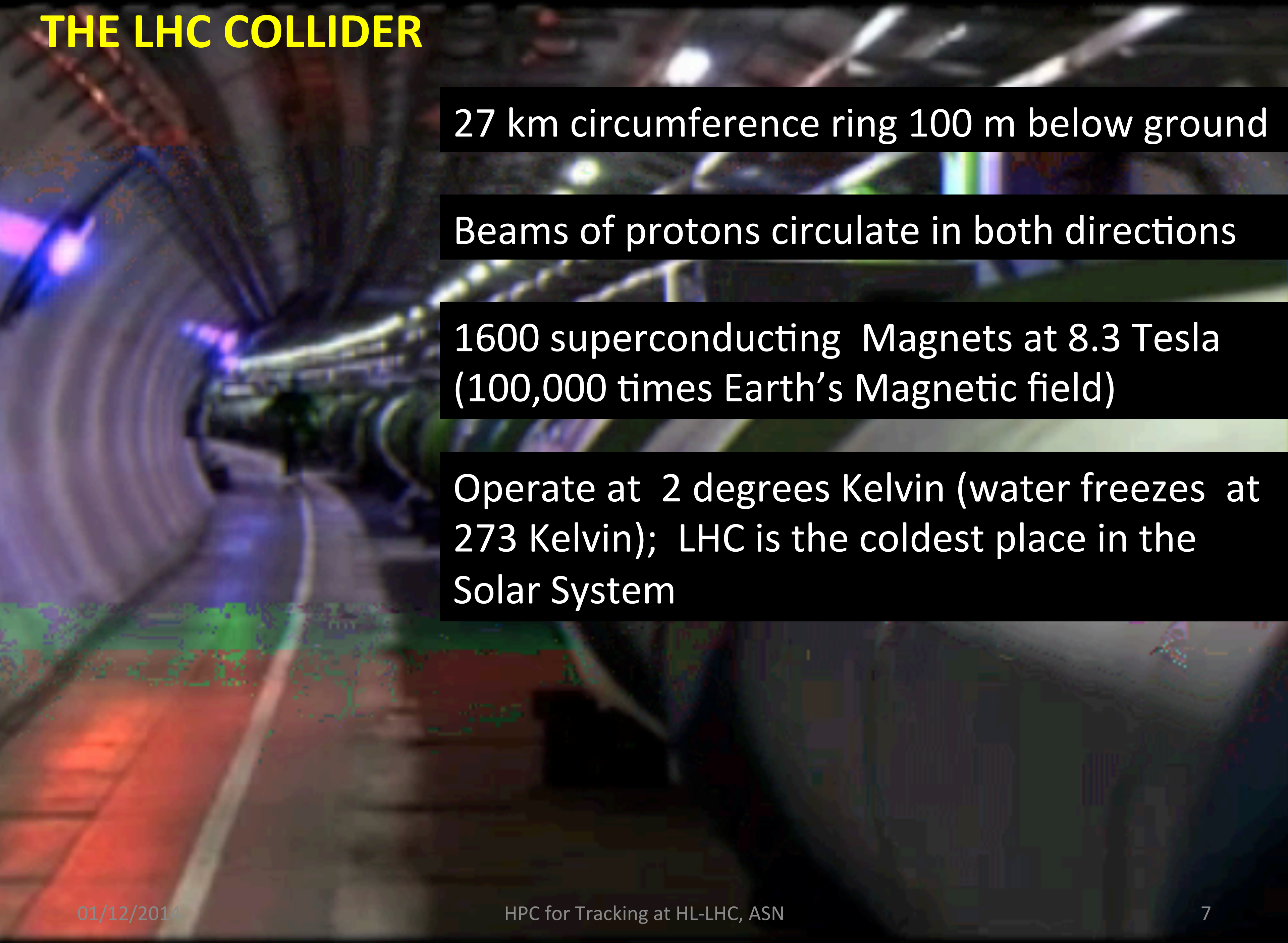
The largest worldwide Laboratory for exploring the elementary constituents of the Matter & the fundamental Forces they interact between them.
The Physicists, Engineers & Industrial partners have built a new instrument that recreates in Laboratory the very early Universe conditions…



THE LARGE HADRON COLLIDER TUNNEL & MAGNETS



- The LHC accelerates protons to 99% of the speed of light and
- smashes them together up to 600 million times a second



THE LHC COLLIDER

27 km circumference ring 100 m below ground

Beams of protons circulate in both directions

1600 superconducting Magnets at 8.3 Tesla (100,000 times Earth's Magnetic field)

Operate at 2 degrees Kelvin (water freezes at 273 Kelvin); LHC is the coldest place in the Solar System

600,000,000 collisions per second

at 14,000,000,000,000 eVolts

Proton beams stores
700 MegaJoules
Equivalent to 747
energy at takeoff
Enough to melt ½
tonne of copper

A A C E
ACCE E A
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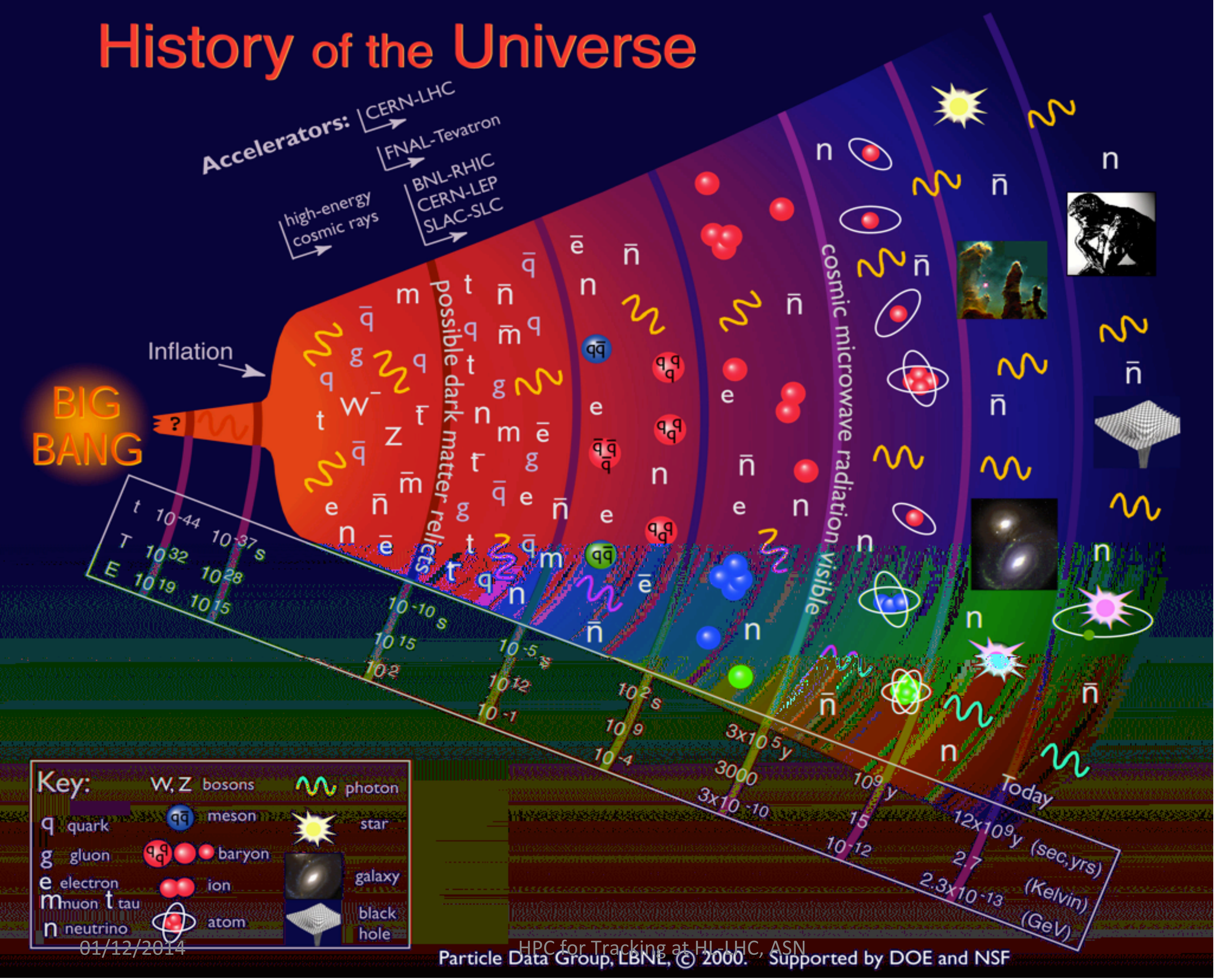
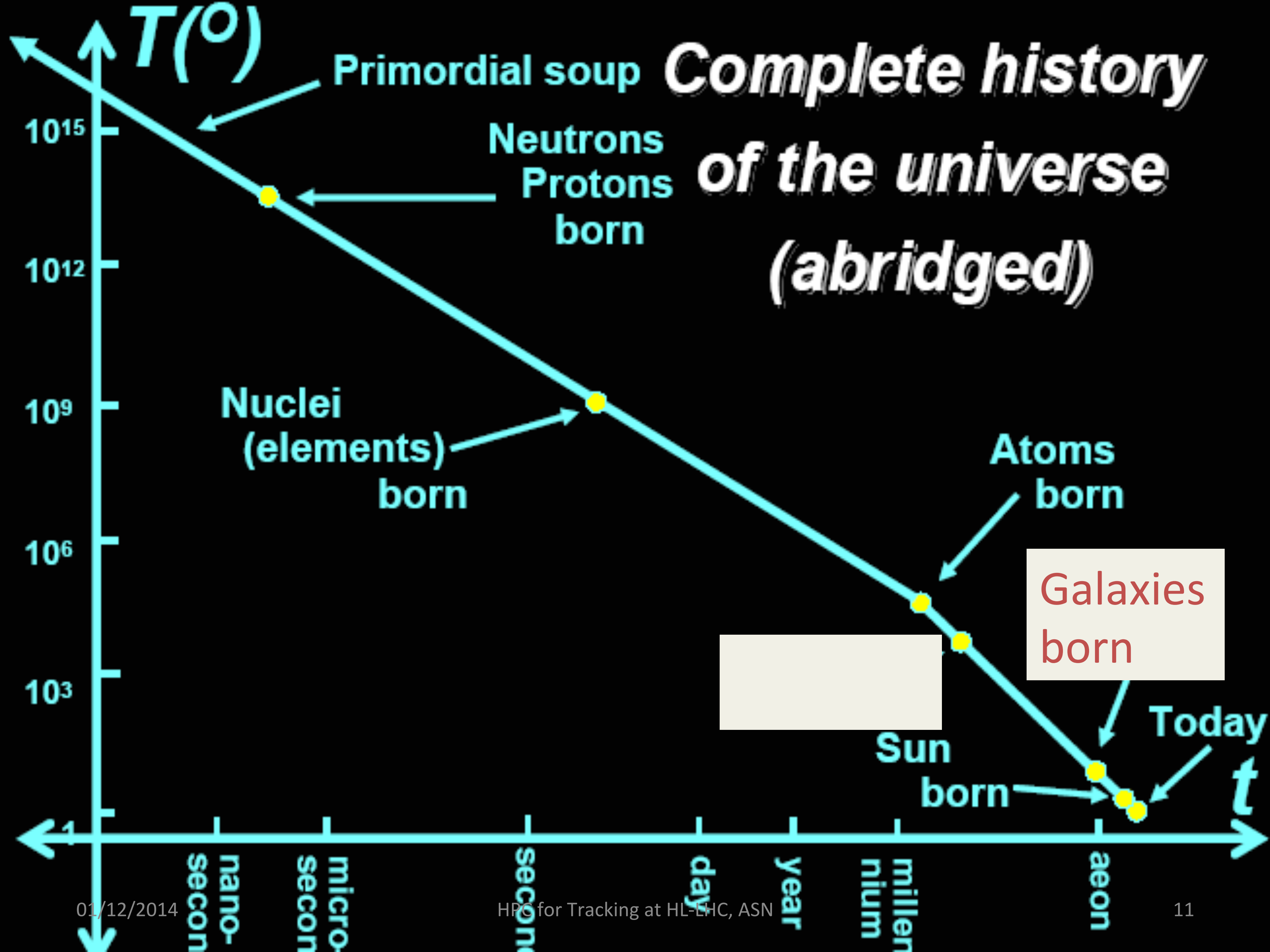

History of the Universe
Accelerators:
CERN-LHC
FNAL-Tevatron
BNL-RHIC
CERN-LEP
SLAC-SLC
high-energy cosmic rays
Inflation
BIG BANG
possible dark matter relicts
cosmic microwave radiation visible
t 10-44 10-37 s
T 1032 1028
E 1019 1015
10-10 s
1015
102
10-5 s
1012
10-1
102 s
109
10-4
3x105 y
3000
3x10-10
109 y
15
10-12
Today
12x109 y (sec, yrs)
2.7 (Kelvin)
2.3x10-13 (GeV)
Key:
W, Z bosons
photon
q quark
meson
star
g gluon
baryon
e electron
ion
galaxy
m muon t tau
n neutrino
atom
black hole
Particle Data Group, LBNL, © 2000. Supported by DOE and NSF


Complete history of the universe (abridged)
T(O)
Primordial soup
Neutrons Protons born
Nuclei (elements) born
Atoms born
Galaxies born
Sun born
Today
t
1015
1012
109
106
103
1
nano-
micro-
day
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millen
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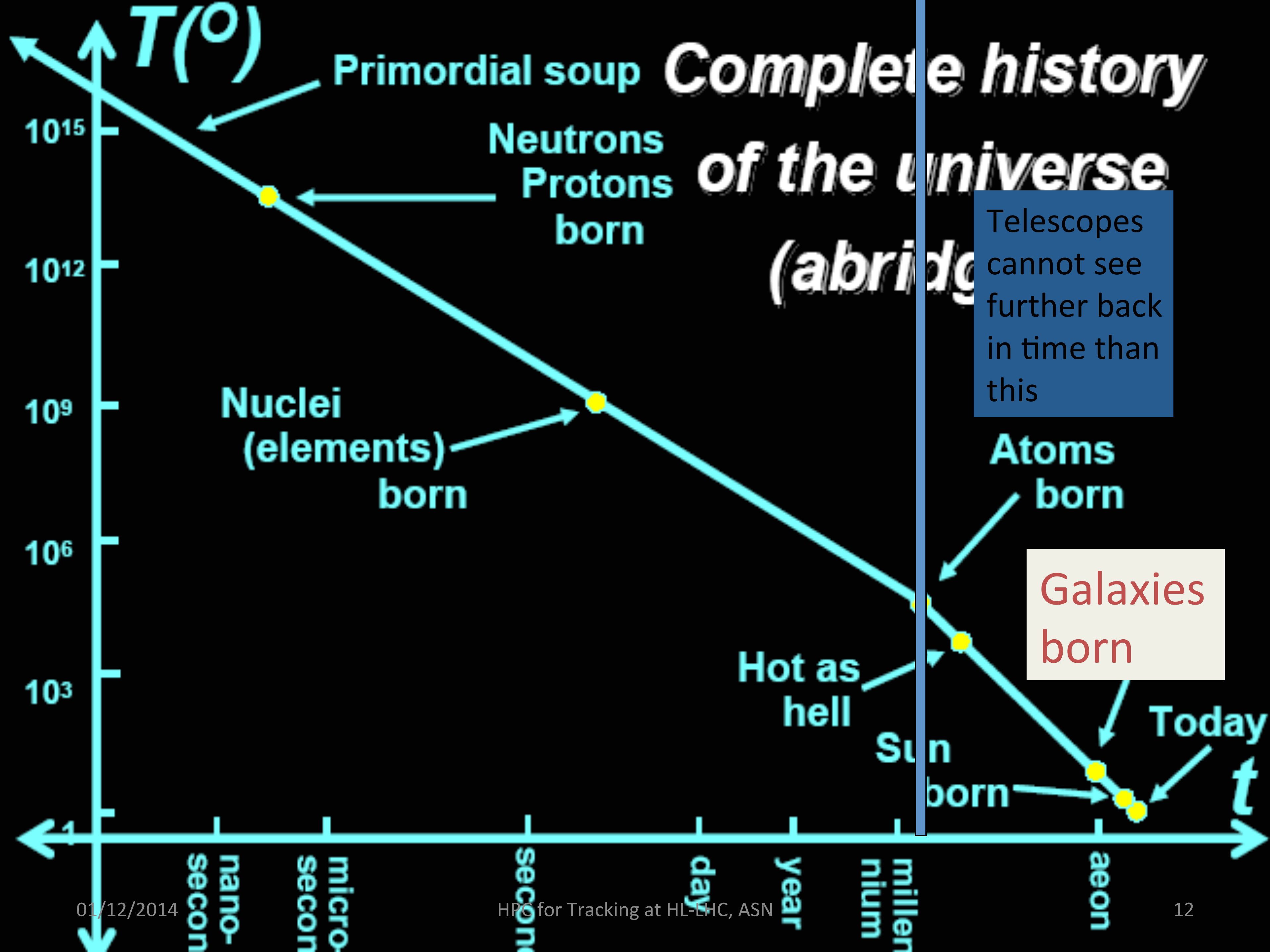
aeon


Complete history of the universe (abridg
T(O)
Primordial soup
Neutrons Protons born
Nuclei (elements) born
Telescopes cannot see further back in time than this
Atoms born
Galaxies born
Hot as hell
Sun born
Today
t
10^15
10^12
10^9
10^6
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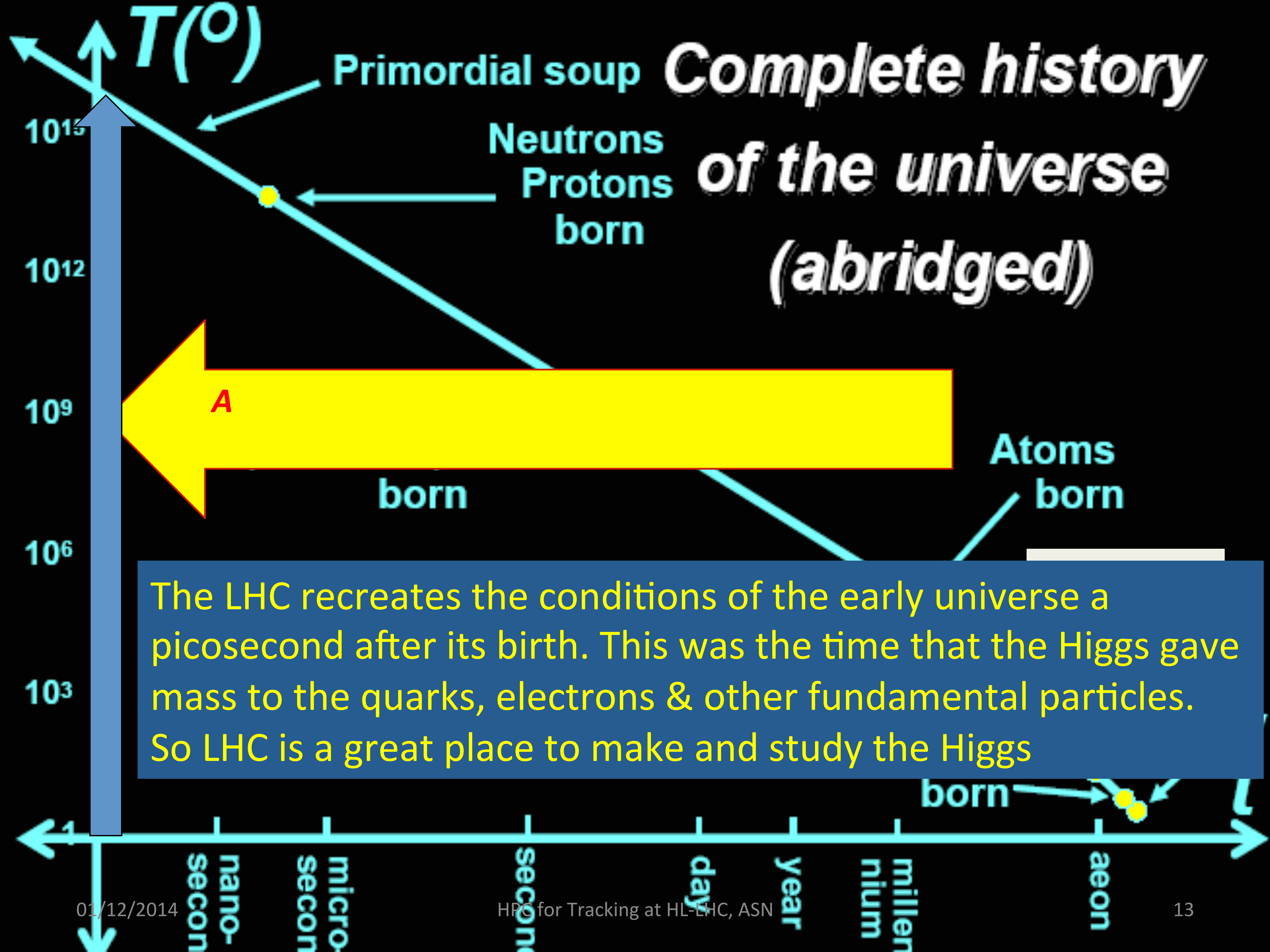
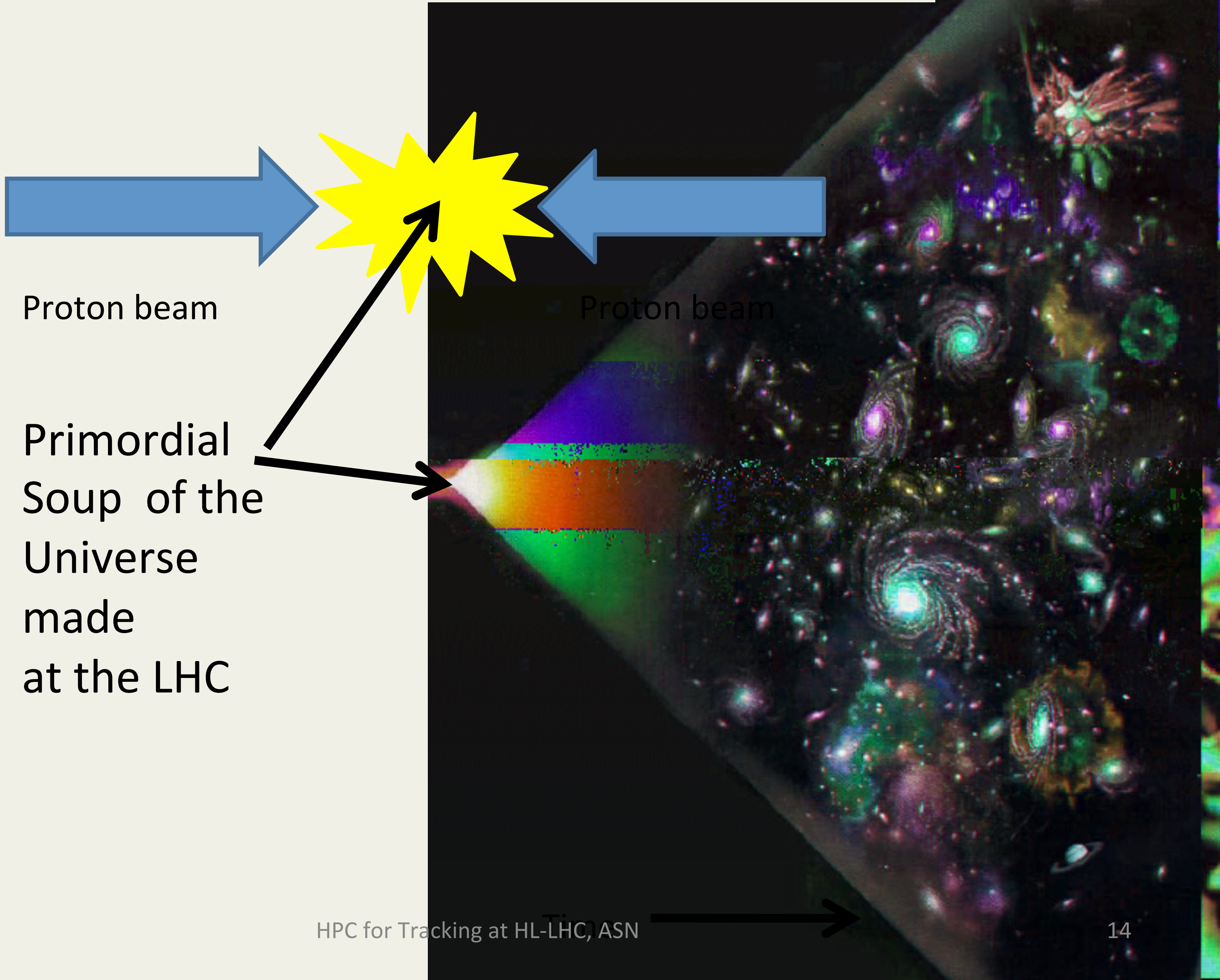
nano-
micro-
day
year
millen nium
aeon

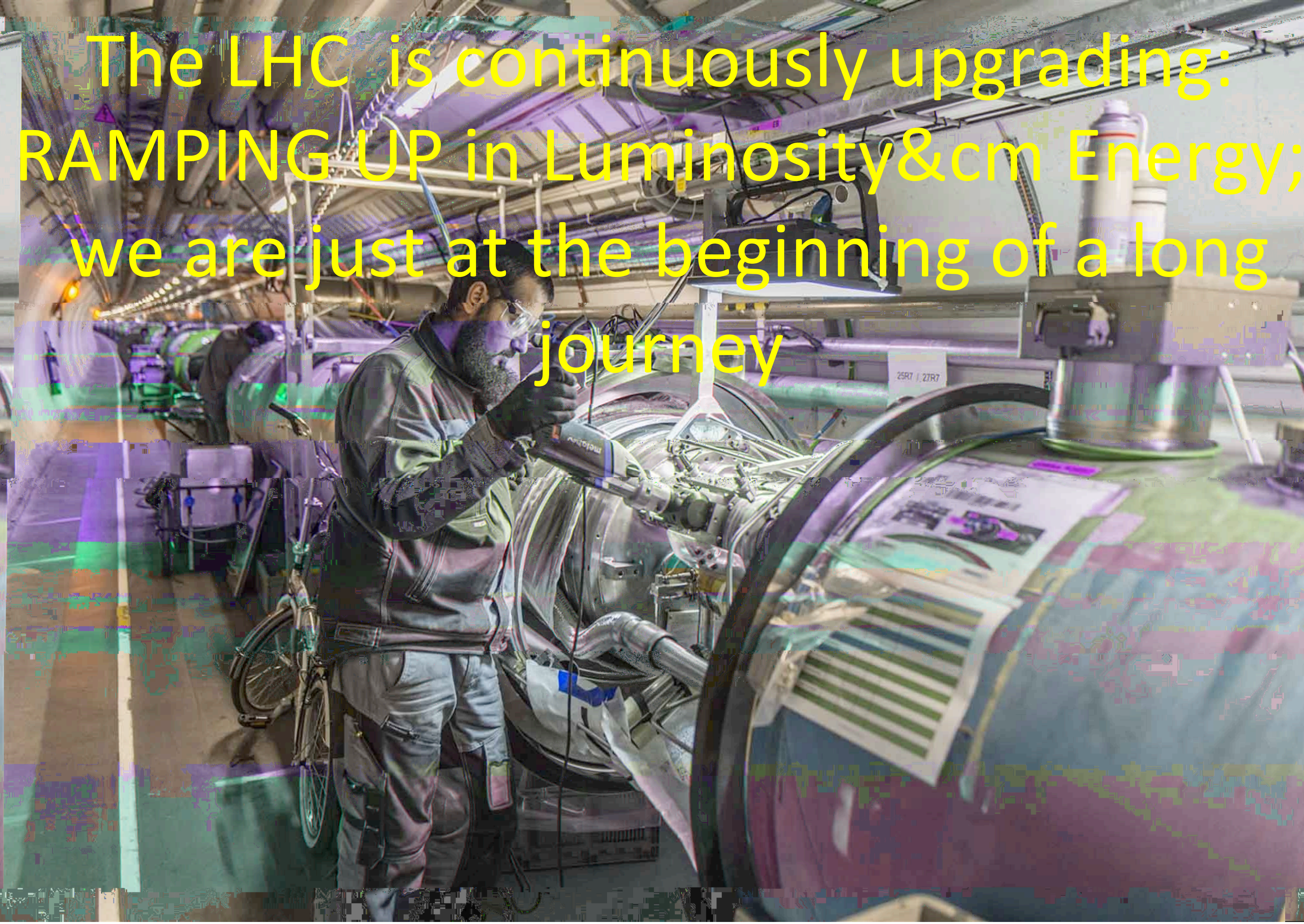


The LHC recreates the conditions of the early universe a picosecond after its birth. This was the time that the Higgs gave mass to the quarks, electrons & other fundamental particles. So LHC is a great place to make and study the Higgs

Quarks to the Cosmos

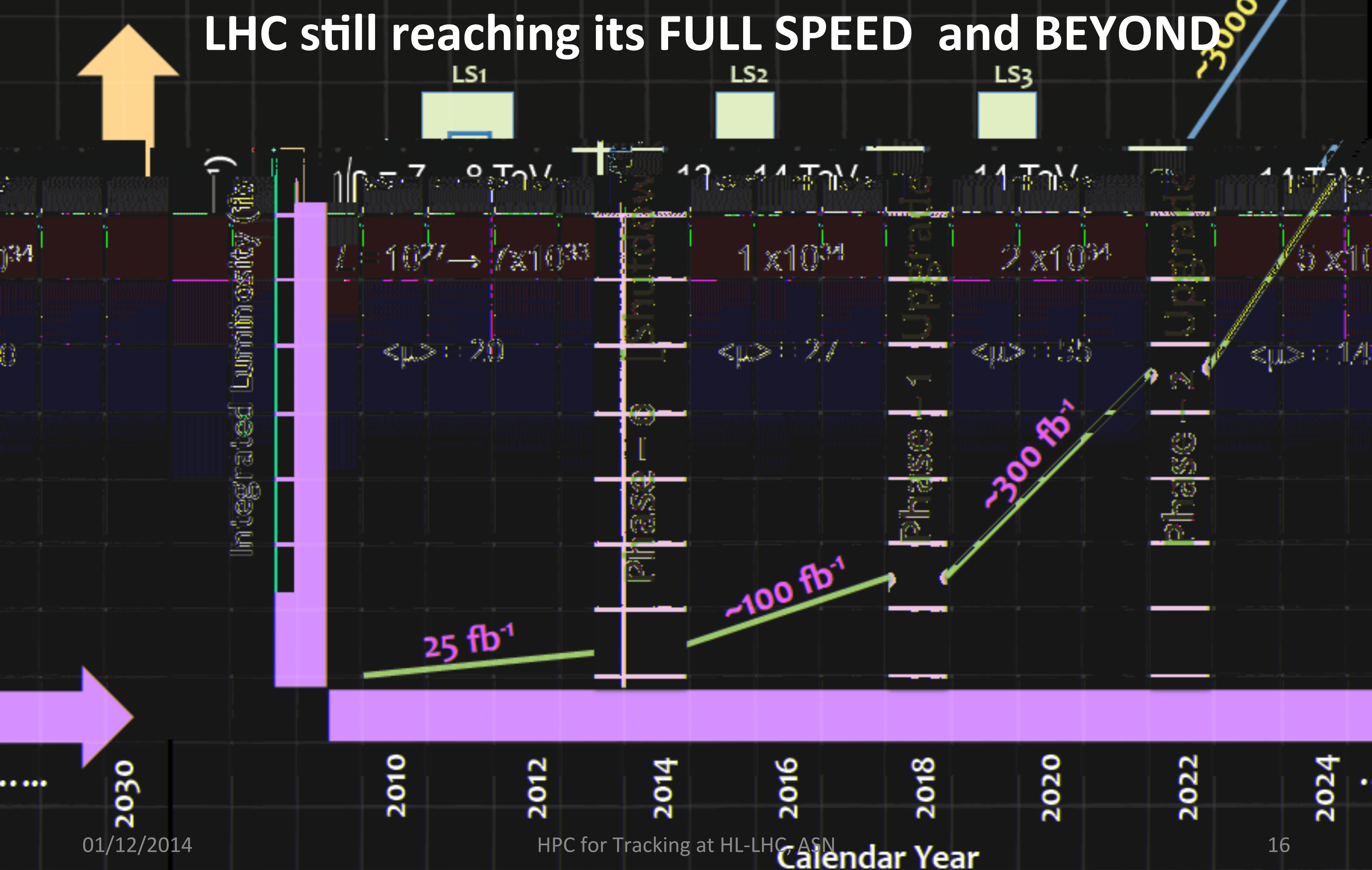


The LHC is continuously upgrading: RAMPING UP in Luminosity&cm Energy; we are just at the beginning of a long journey



Courtesy of the DOE representative's talk at Snowmass- 0 (Minnesota)

The LHC Forecast



The European Strategy for Particle Physics
Update 2013

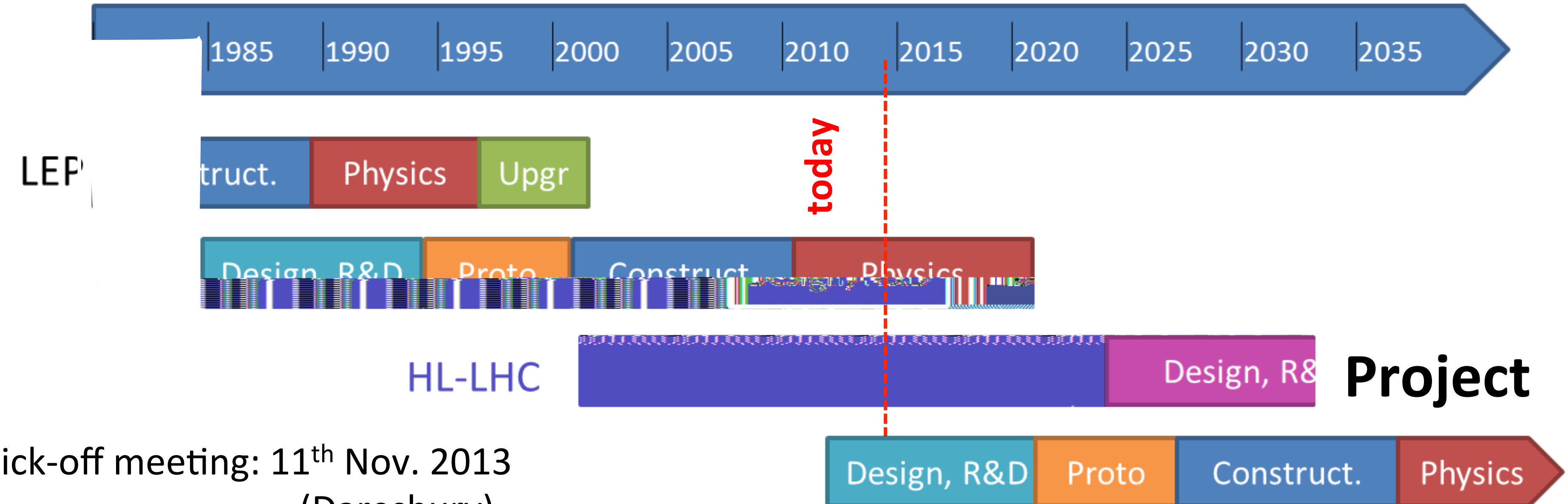
c) *Europe's top priority should be the* ***C****,* *including the high-luminosity upgrade of the machine and detectors with a view to collecting* *. This upgrade programme will also provide further exciting opportunities for the study of flavour physics and the quark-gluon plasma.*

HL-LHC from a study to a PROJECT

300 fb^{-1} → 3000 fb^{-1}

including LHC injectors upgrade **LIU** (Linac 4, Booster 2GeV, PS and SPS upgrade)

Also endorsed by the US community at the CSS 0 (Snowmass on Minnesota) July -Aug



Kick-off meeting: 11th Nov. 2013 (Daresbury)

Design Study : Very High Energy (VHE)-LHC => Future Circular Collider, FCC–ee

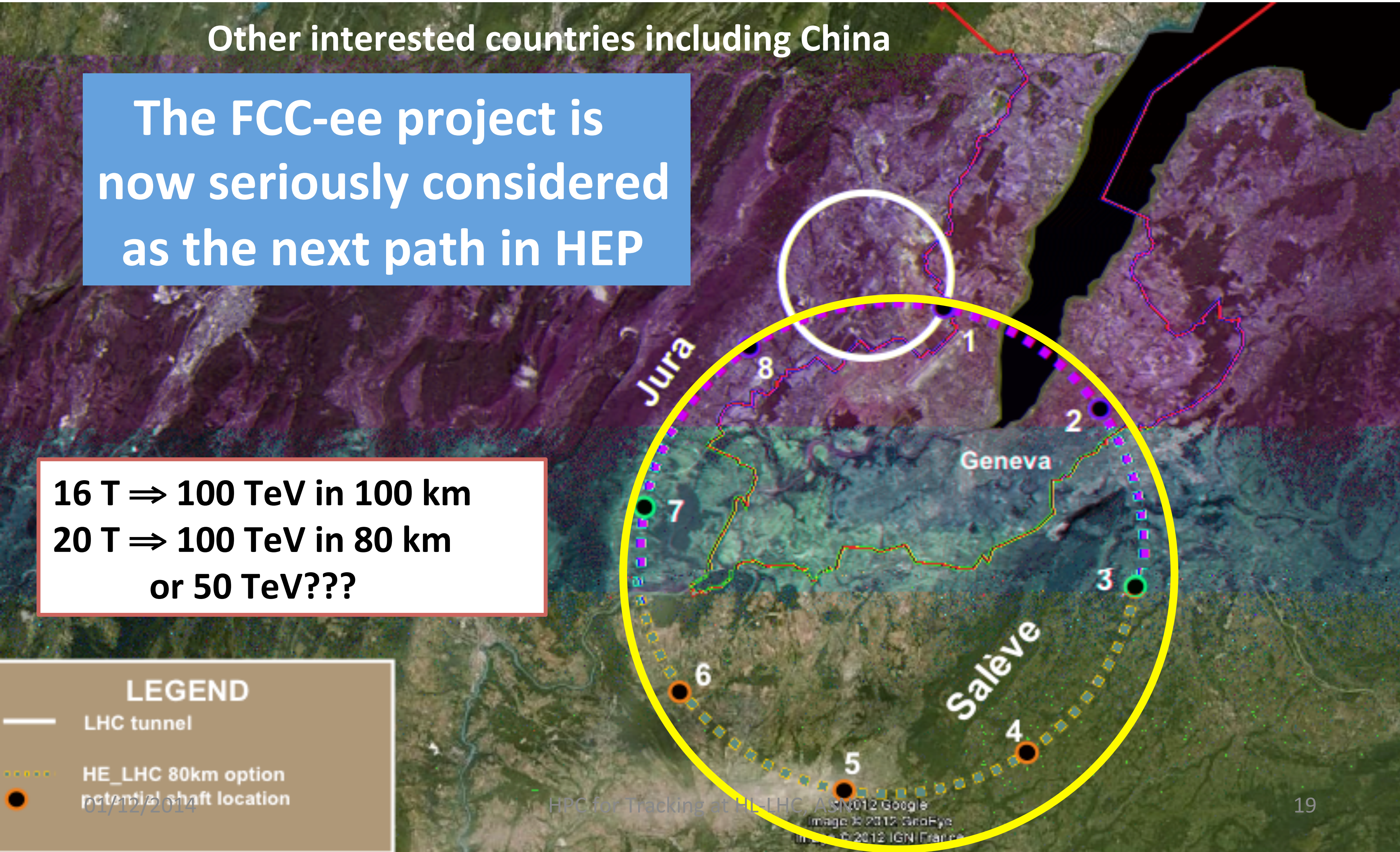
Kick-off meeting: February 2014 (CERN)
next meeting: Oct 27-29 2014 (Paris)

80-100 km tunnel in Geneva area – VHE-LHC

with possibility of e+-e- (TLEP) and p-e (VLHeC)

Other interested countries including China

The FCC-ee project is now seriously considered as the next path in HEP



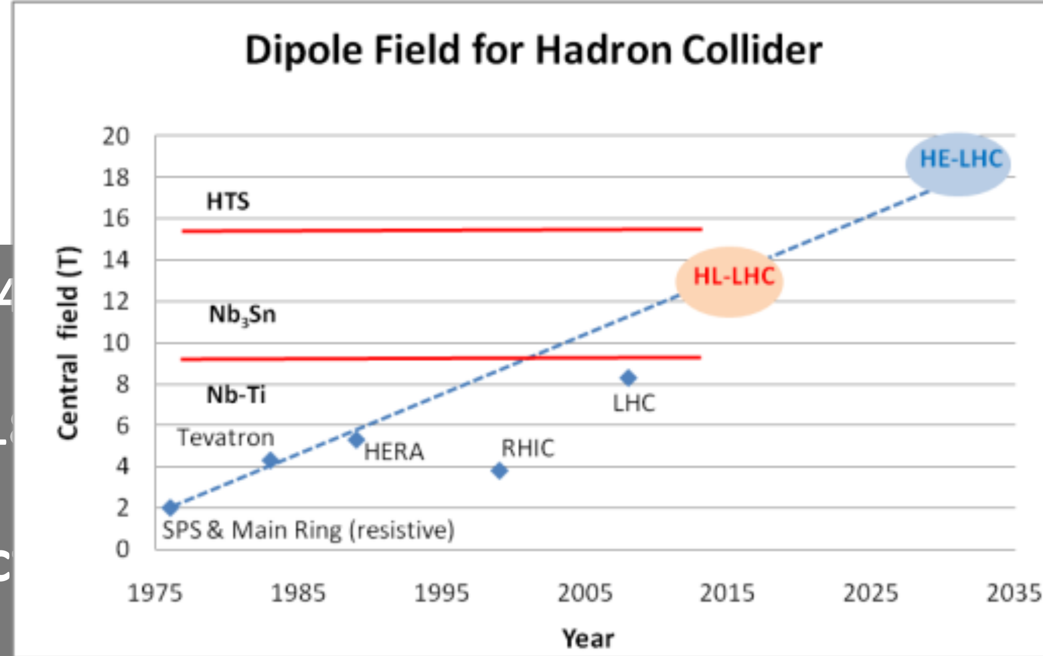
16 T $\Rightarrow$ 100 TeV in 100 km
20 T $\Rightarrow$ 100 TeV in 80 km
or 50 TeV???

Summary:

- LS1 (13-14 TeV) [2013-2014

- LS2 (higher intensity) [201

- HL-LHC : R&D => construc



- Vigorous R&D and preparation for post-LHC machine (CDR and Cost-Schedule)

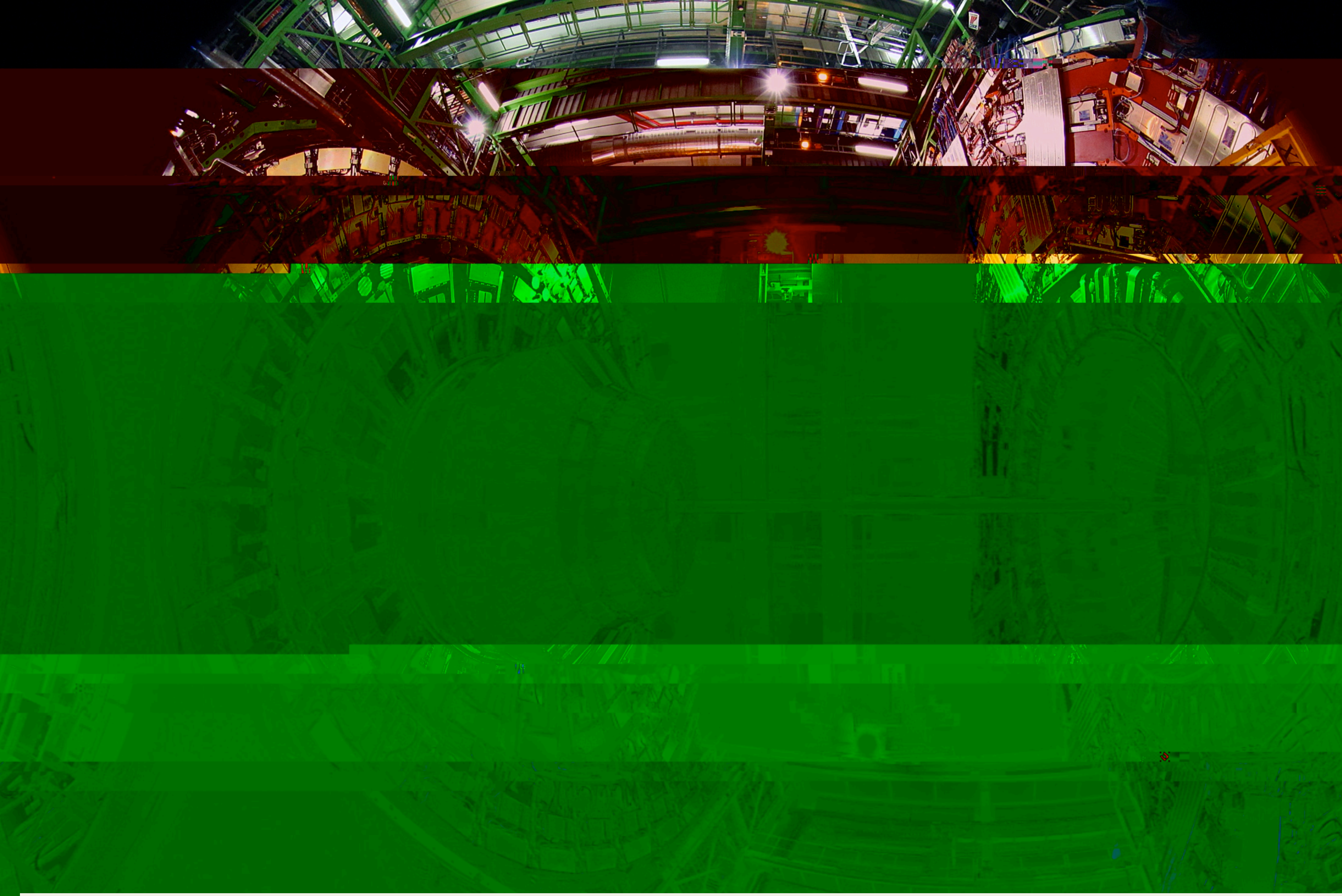
E *C* **15 to 20 T**

to be ready for the next European Strategy Update

(multi-lateral collaboration approach)

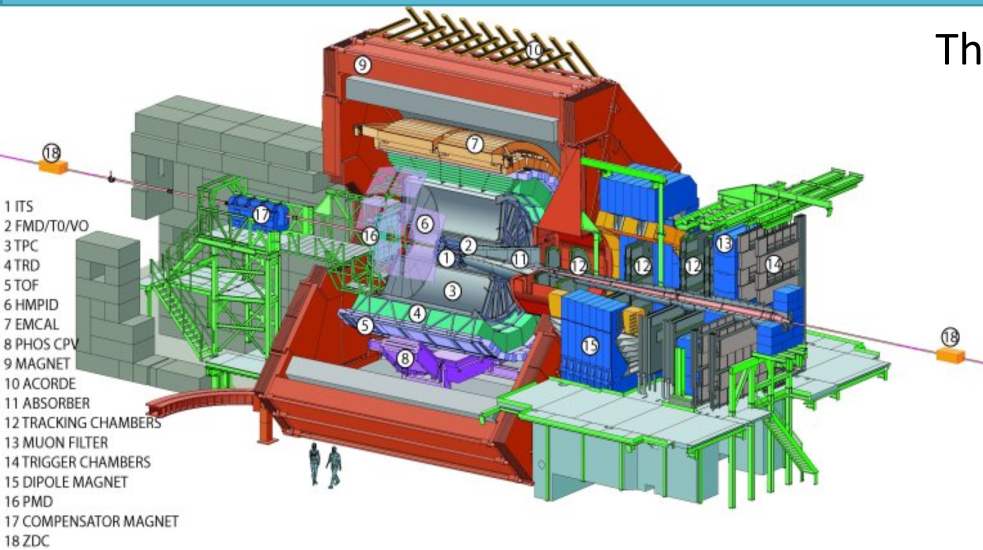
The quest for Higher Energy is motivated by the exploration of new Physics i.e. looking for new particles => allows accessing higher mass and higher cross-section, i.e. higher probability to create the new processes yet to be discovered.

The Large Hadron Collider at CERN

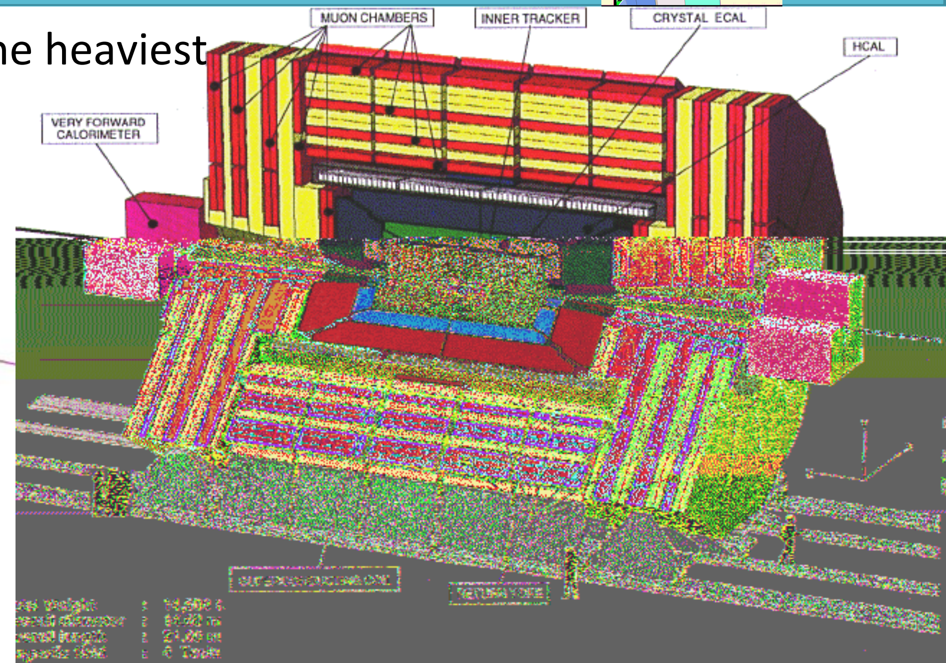


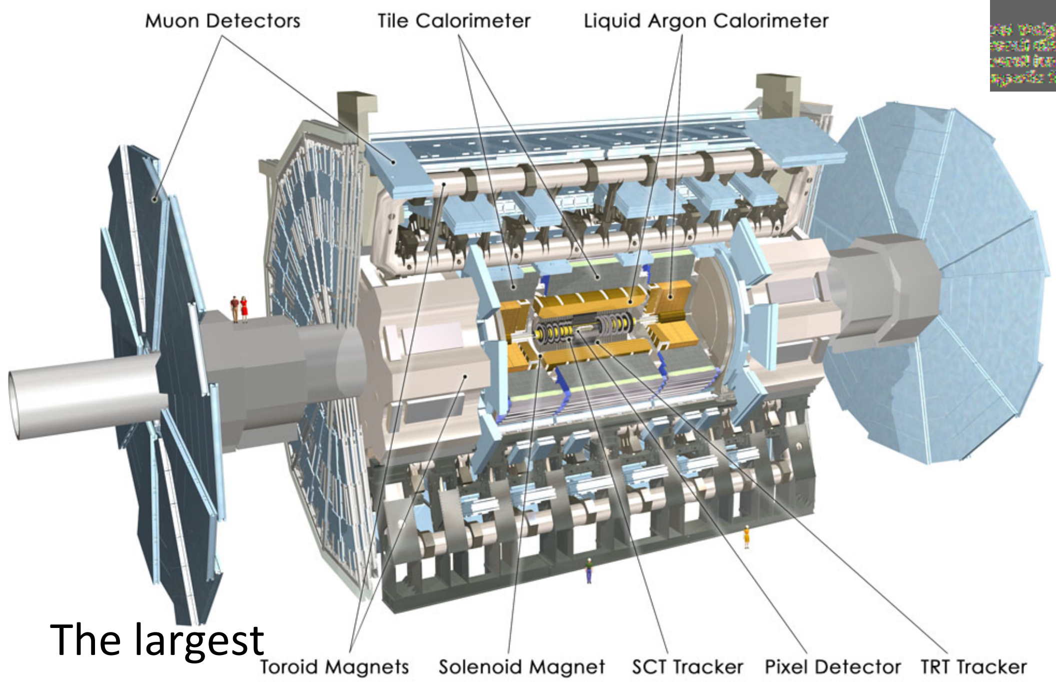
LHC experiments are like Digital Cameras the size of Cathedral

The 4 Experiments at LHC



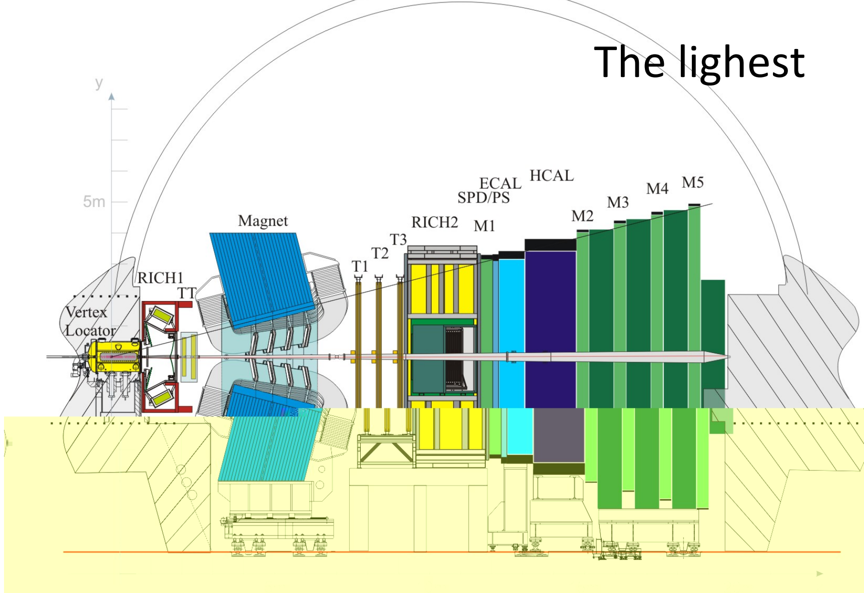
The heaviest





The largest

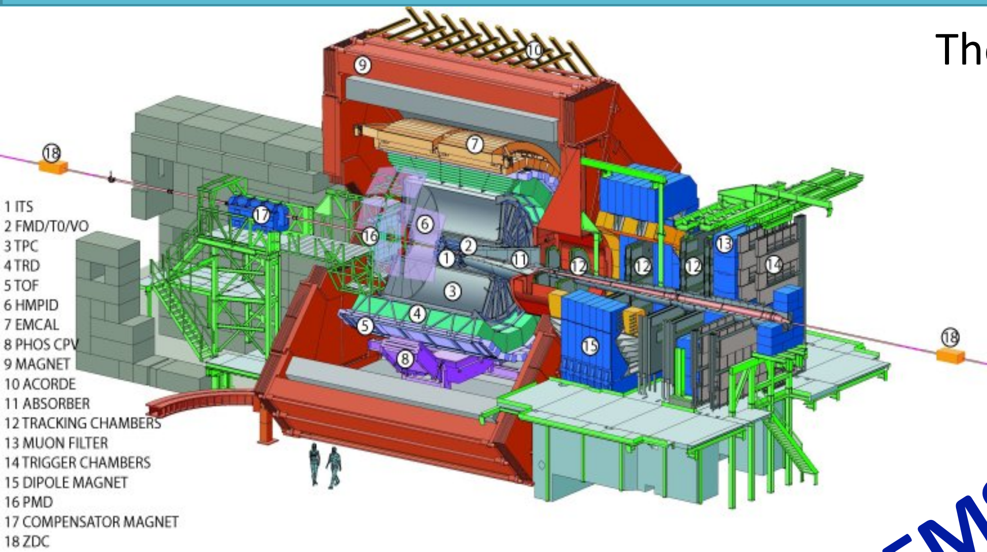
The lighest



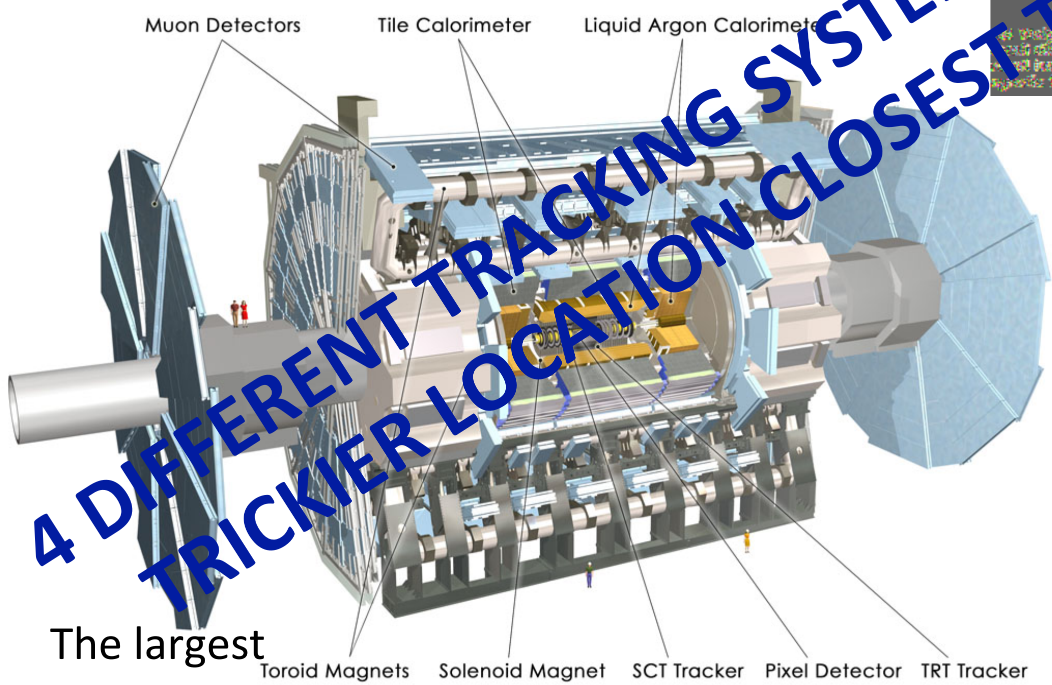
The 4 Experiments at LHC

4 DIFFERENT TRACKING SYSTEMS AT THE CORE OF THE EVENT

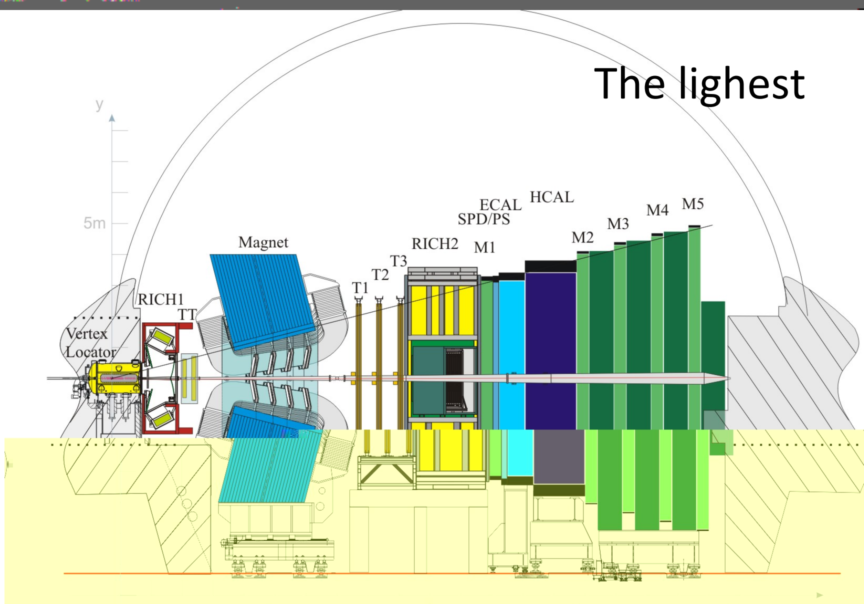
TRICKIER LOCATION CLOSEST TO THE INTERACTION POINT



The heaviest

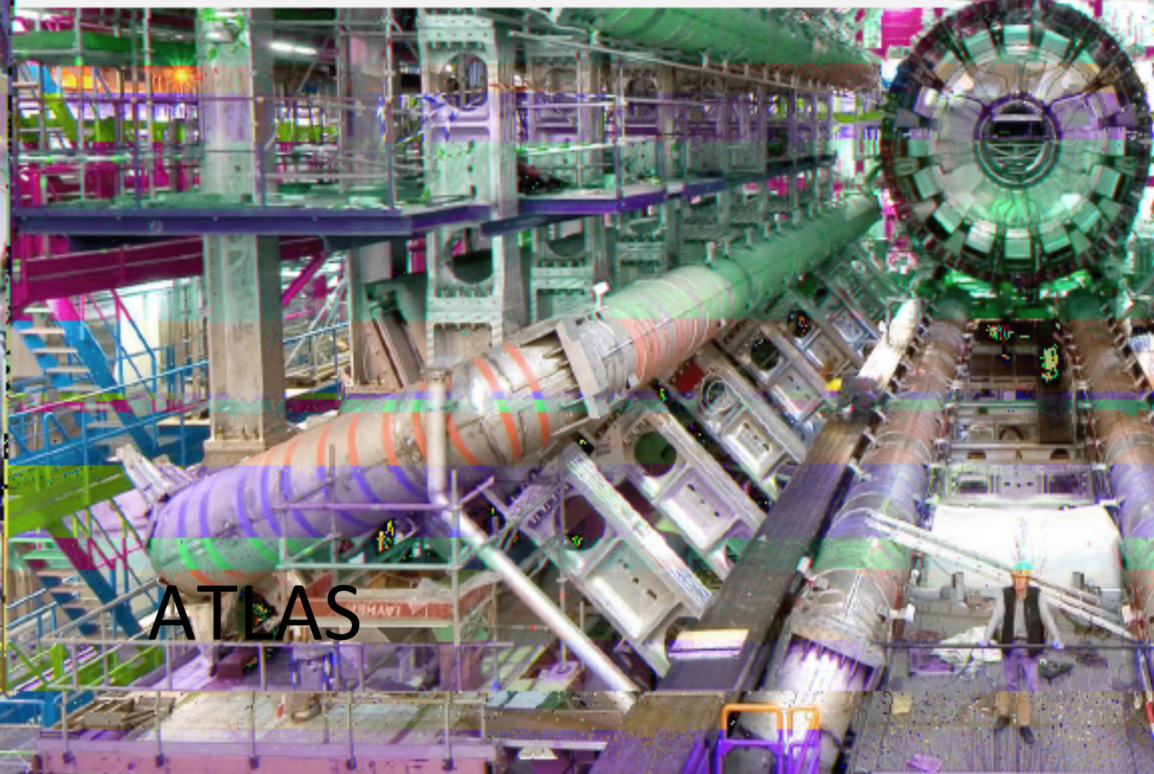


The largest

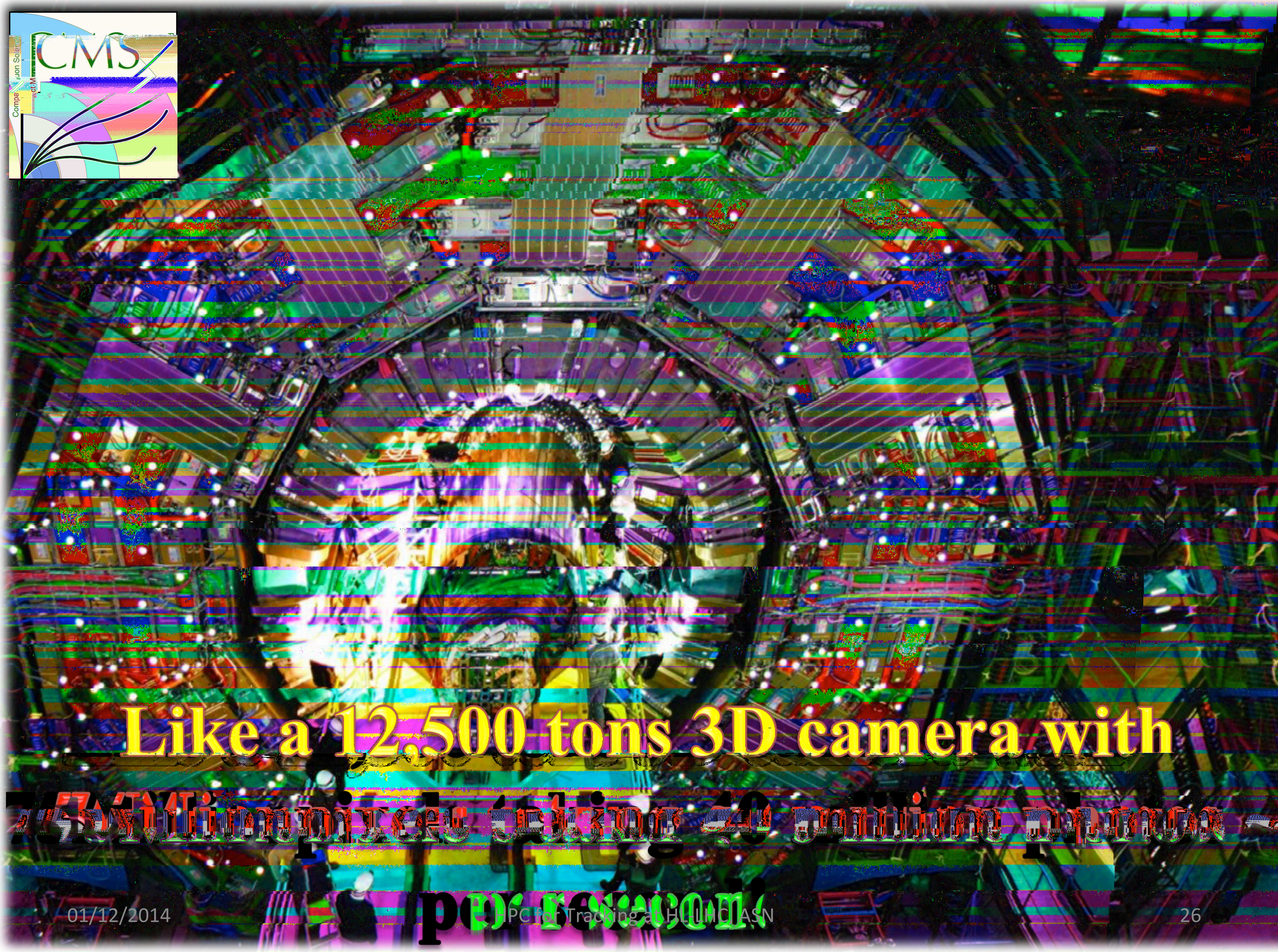


The lighest

Object	Weight (tons)
Boeing 747 [fully loaded]	200
Endeavor space shuttle	368
ATLAS	7,000
Eiffel Tower	7,300
USS John McCain	8,300
CMS	12,500



DIGITAL CAMERAS THE SIZE OF CATHEDRALS

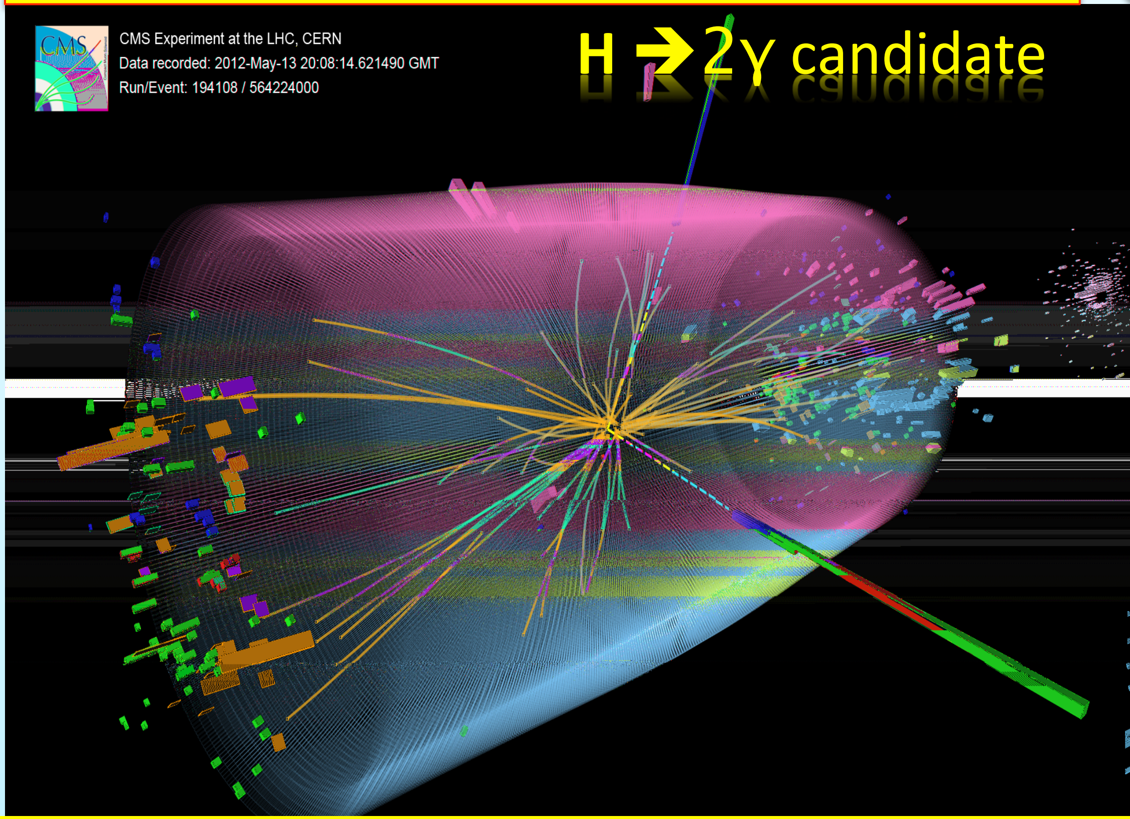


Like a 12,500 tons 3D camera with 75 Million pixels taking 40 million pictures – per second!

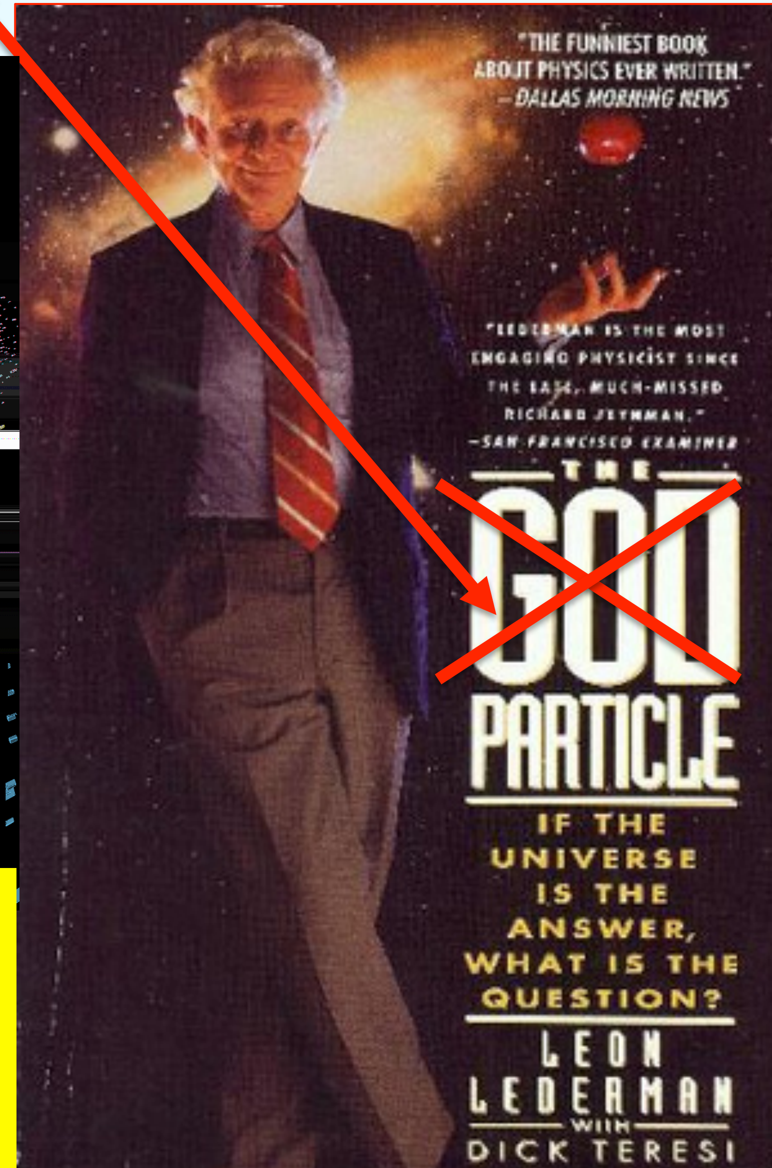

ATLAS
5TH FLOOR
CMS

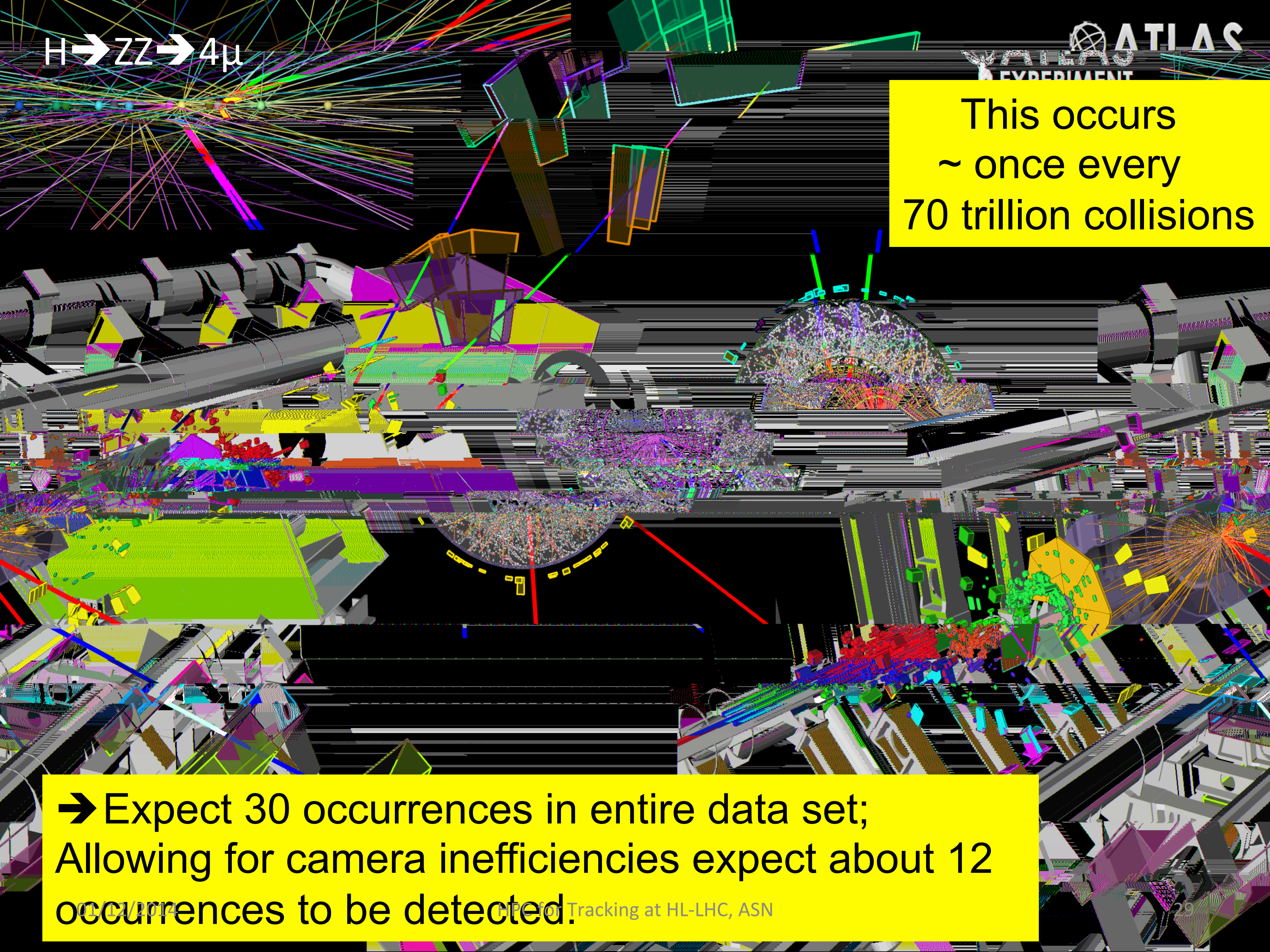
WHY? because of the particle & beyond

EXTREMELY RARE & DIFFICULT TO EXTRACT (BKGDs)



This occurs once every trillion collisions;
Allowing for the efficiency of the camera
a few hundred examples of this process to
have been recorded in the first 25fb^{-1} run.





This occurs
~ once every
70 trillion collisions

→ Expect 30 occurrences in entire data set;
Allowing for camera inefficiencies expect about 12 occurrences to be detected.

The higher the energy the higher the Lum the higher the P.U. & backgrounds to confront

The Higher the Ecm, the higher the proba to find new particles but at the same time

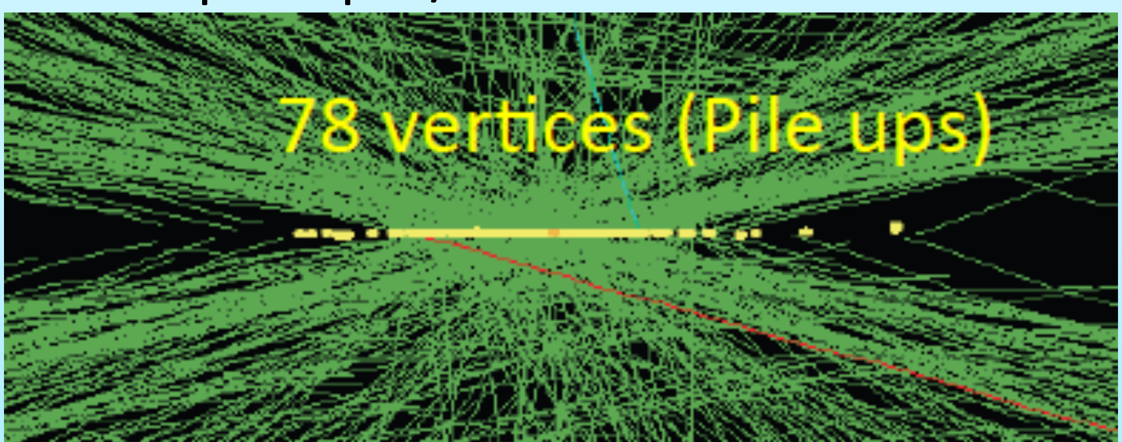
- More difficult to extract them because

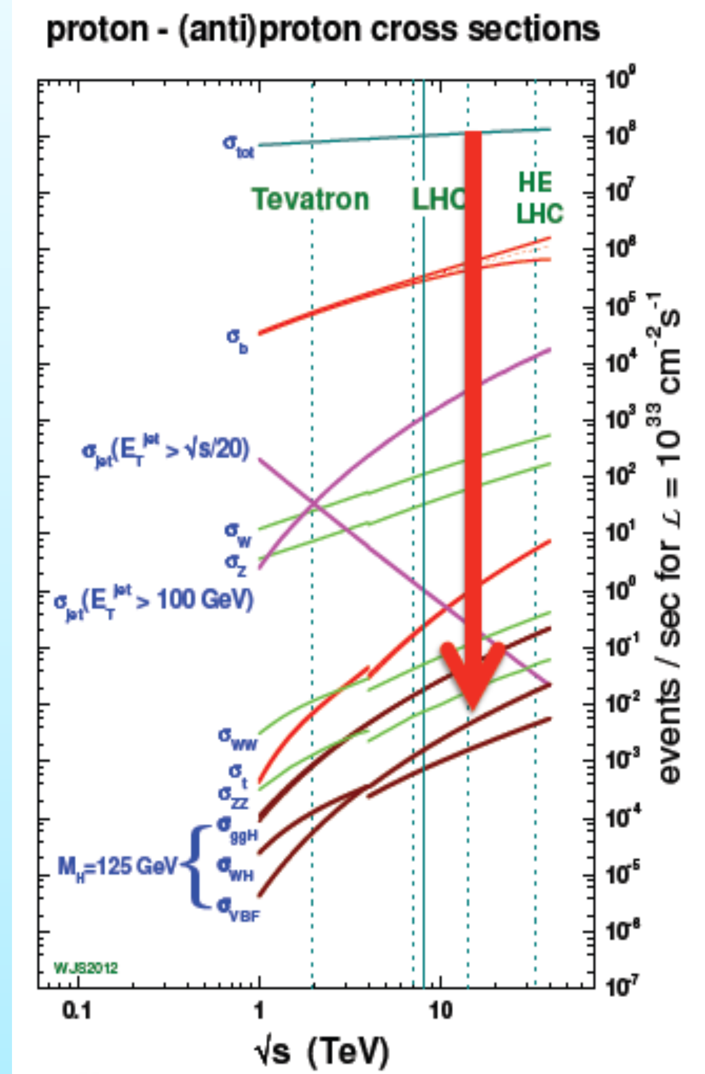
Increased physics backgrounds & Pile ups

- Events to be extracted out of O(10) orders

of magnitude events and

- With <pile ups>/event = 140-200





Outline

- High Luminosity Large Hadron Collider at CERN: What is it, When and Why?
- **The Large Area Tracking systems at LHC: now and in the next decade.**
- Why do Large Area Tracking systems need HPC?
- Solutions to satisfy these needs: R&D, Full custom and Collaboration with High Tech Industry
- Concluding remarks & perspectives …

The tracking systems: a crucial detector

- As shown in the previous slides the tracking system that allows visualizing the trajectory of the charged particles issued from the interaction between protons is a crucial detecting piece.
- The tracking technology is now predominantly based on Silicon devices made of micro strips or pixels (innermost parts).
- Developing the Si tracking technology has been instrumental for building large area tracking systems. The CMS All -Silicon tracker is a premiere with 200 m^2 total area. ATLAS is now building a new tracker for the HL-LHC also all-Si based.
- The other tracking technologies at LHC are the Track Projection Chamber (TPC), a gaseous detector (ALICE) & revisiting Sci. Fiber tracking techno read out by Si PMs (Upgrade of LHCb).

We will concentrate here on Si based tracking as main example.

Tracking systems for HL-LHV in a nutshell

- Two main parts:
  - microvertex closest to the beam pipe => interaction region, made of Si pixels
  - Outer tracker: made of larger pixels and or Si microstrips
- Very High granularity (starting of Particle Flow)=>
- Precise measurement of created charged particles trajectory & impulsion in proton-proton collision.
- FEE embedded in the detector with CMOS techno allows first stage of data processing on detector
- Essential tool to refine the data selection and thus promptly select the interesting events.

The CMS Detector as an example

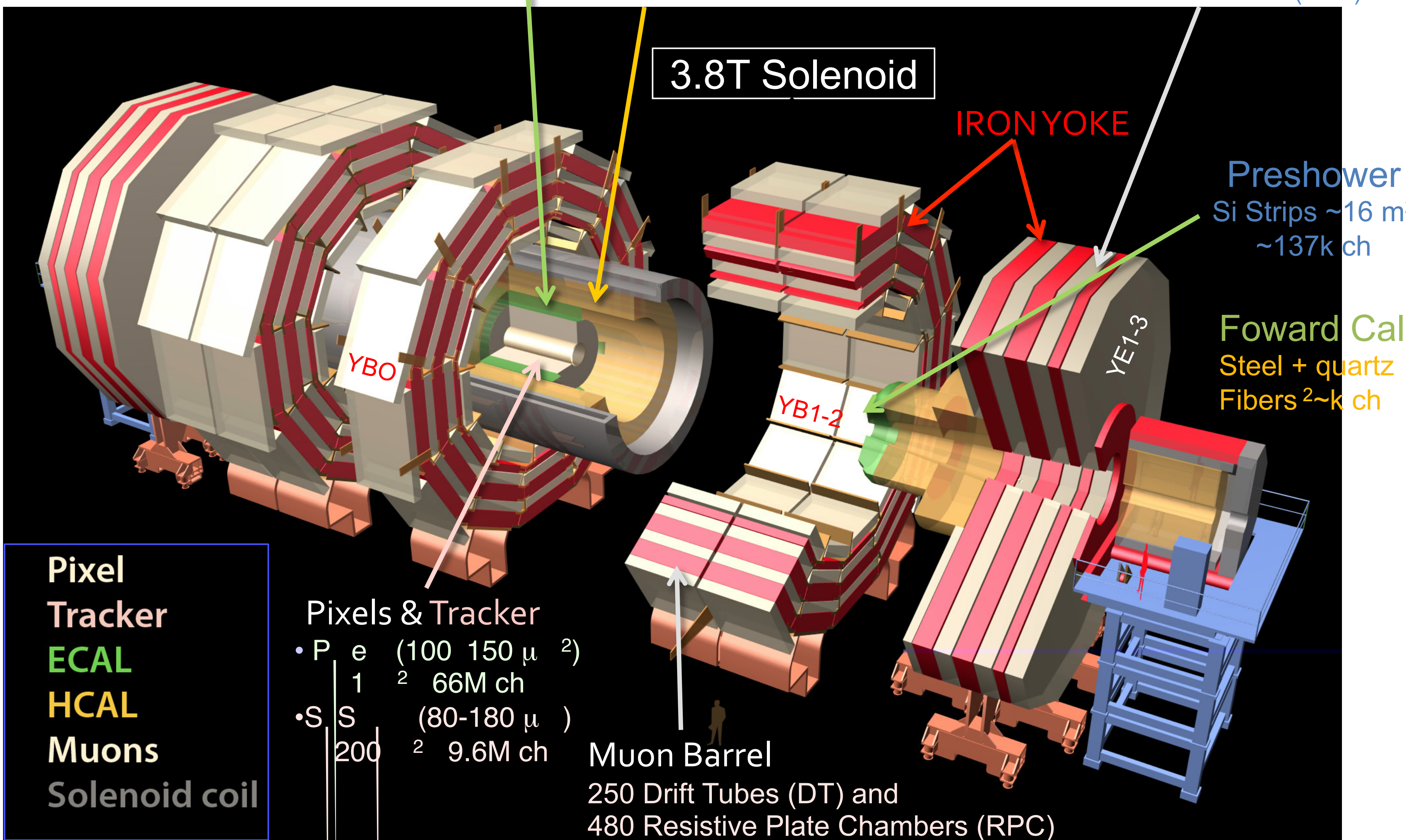
Total weight 14000 t
Overall diameter 15 m
Overall length 28.7 m

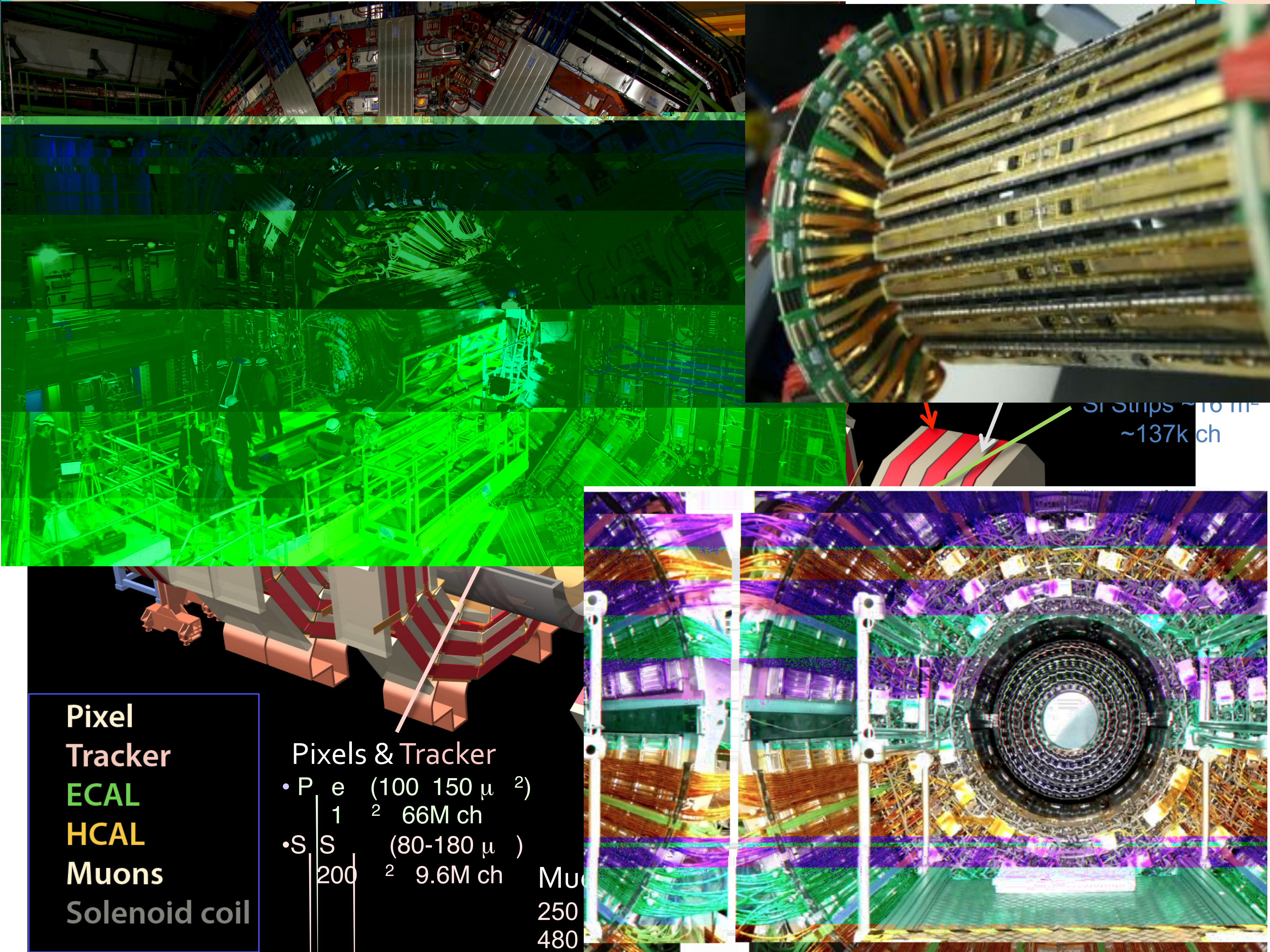
ECAL
76k scintillating
$PbWO_4$ crystals

HCAL
Scintillator/brass
Interleaved ~7k ch

(shown open)

Muon endcaps
473 Cathode Strip Chambers (CSC)
432 Resistive Plate Chambers (RPC)




~137k ch
Pixel
Tracker
ECAL
HCAL
Muons
Solenoid coil
Pixels & Tracker
• P e (100 150 μ 2)
1 2 66M ch
•S S (80-180 μ)
200 2 9.6M ch
Mu
250
480

The CMS Detector as an example

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Muon endcaps
473 Cathode Strip Chambers (CSC)
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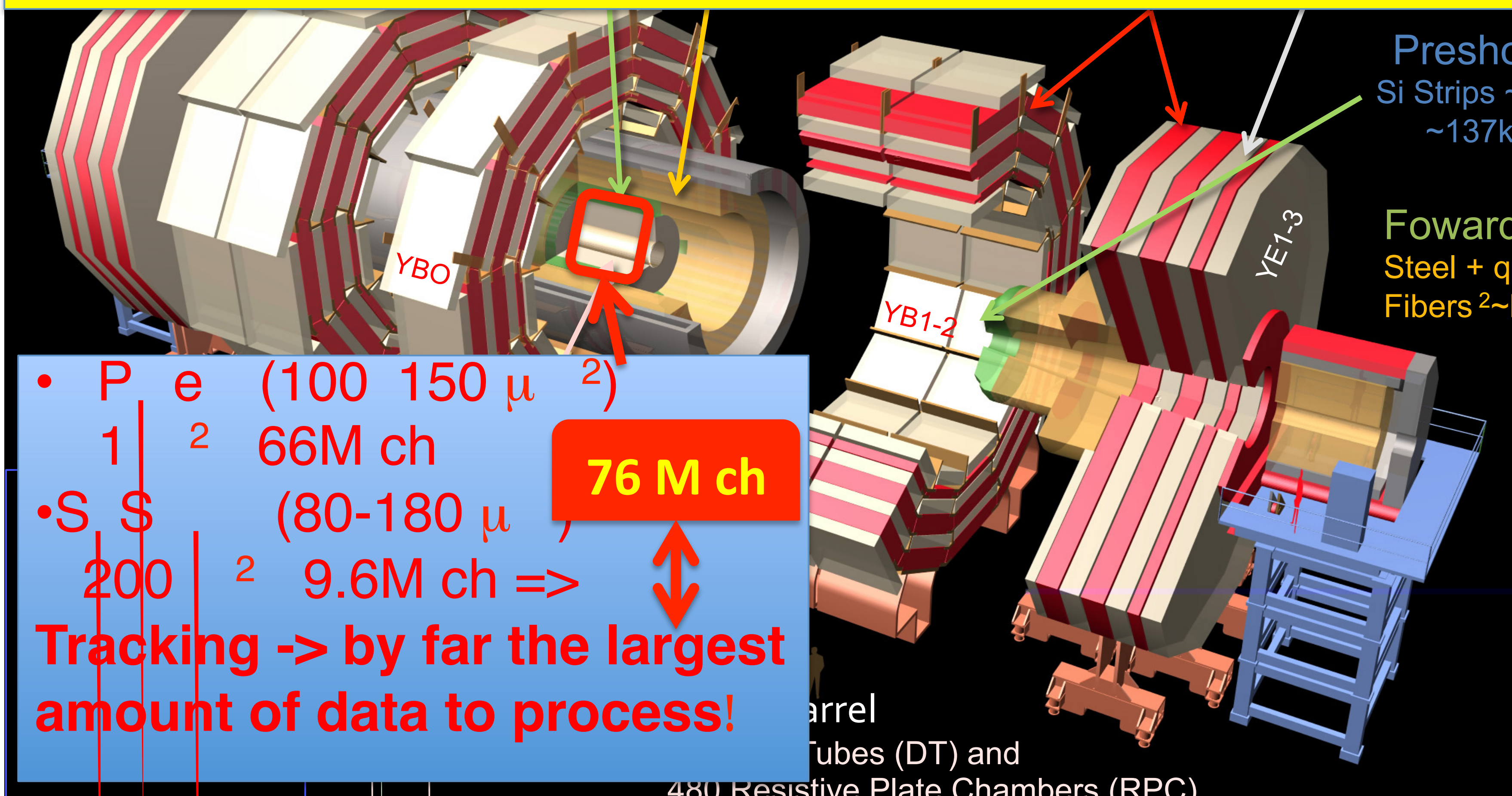
The Tracking system (especially the Microvertex) is by far (99%) responsible for the BIG DATA challenge in HEP experiments



Preshower
Si Strips ~16 m^2
~137k ch

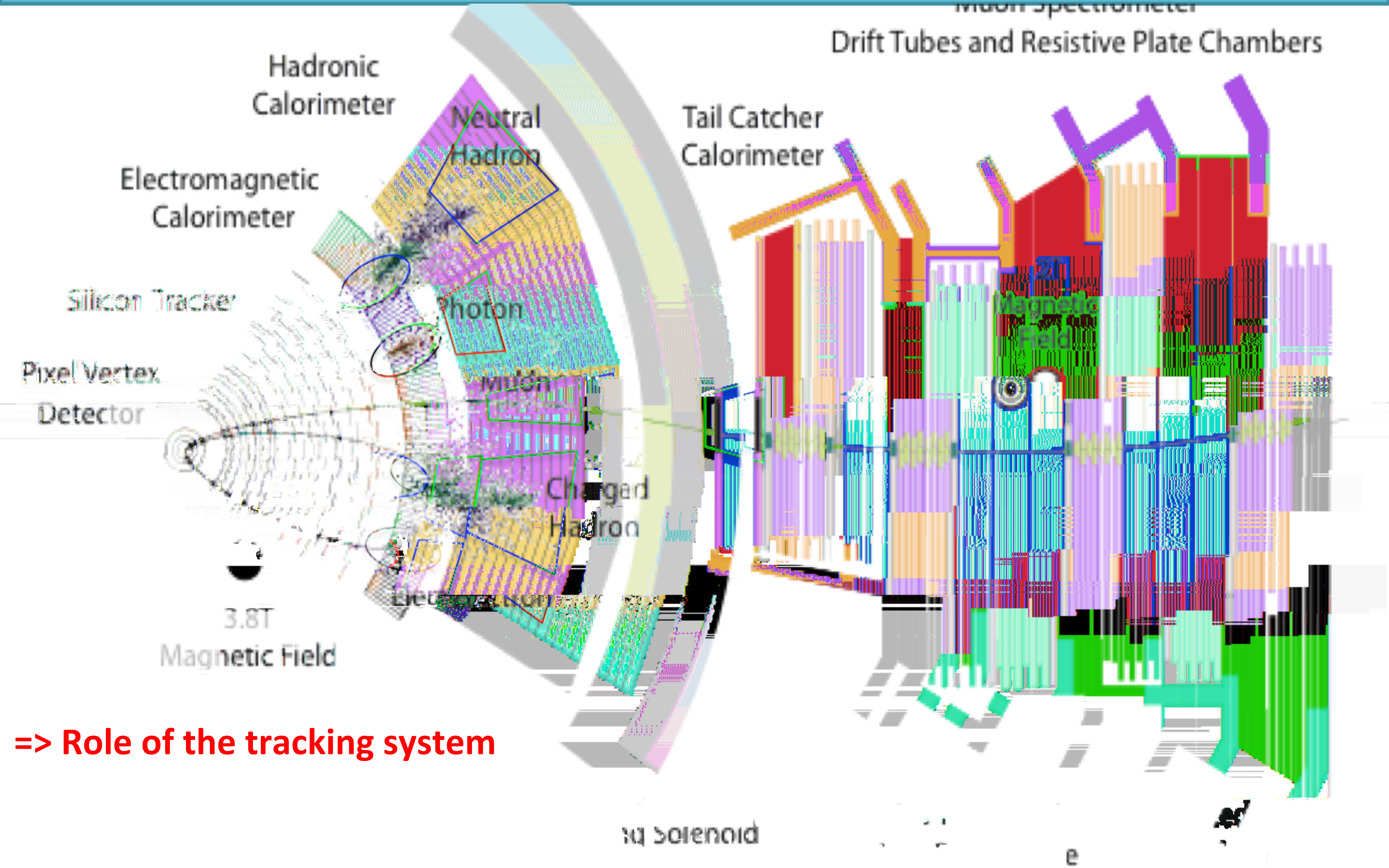
Foward Cal
Steel + quartz
Fibers 2~k ch

- P e (100 150 μ 2)
  1 2 66M ch
- S S (80-180 μ)
  200 2 9.6M ch =>

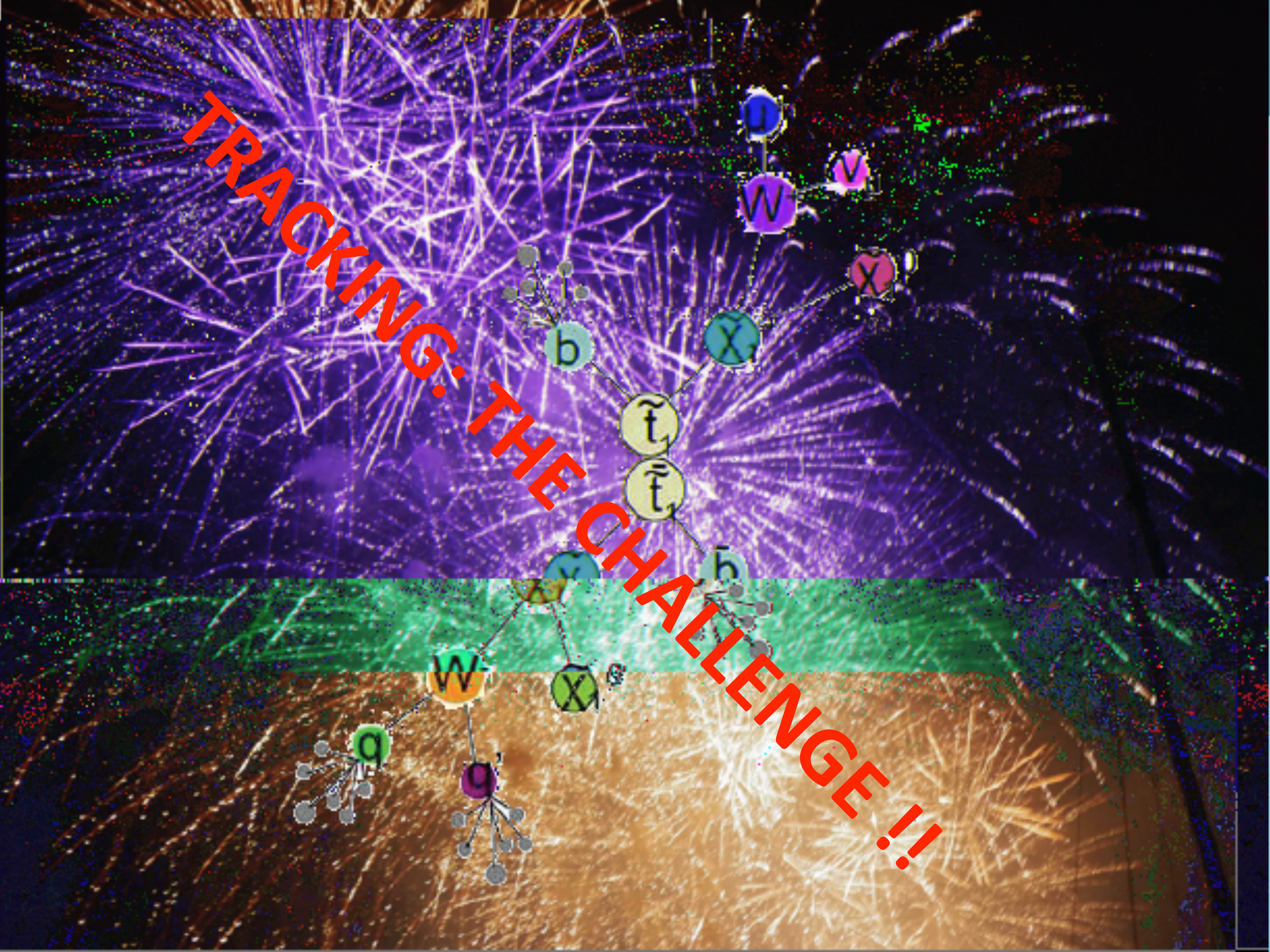
76 M ch

Tracking -> by far the largest amount of data to process!

The reconstruction of Physics objects with CMS



=> Role of the tracking system


TRACKING: THE CHALLENGE !!
b
W
ν
x
$\tilde{t}$
$\bar{\tilde{t}}$
$\bar{b}$
W
x
q
q'

Higher energy & higher luminosity => higher Physics potential reach, but much trickier & demanding detecting capabilities

To confront these challenges the Tracking system at the core of the experiment, must be upgraded with:

- finer granularity for higher precision measurements (see next slide)
- Including it in the trigger system to cope with the increase of event rates and the demands of the Physics (see next+1 slide)

To allow refined & real time selection of events

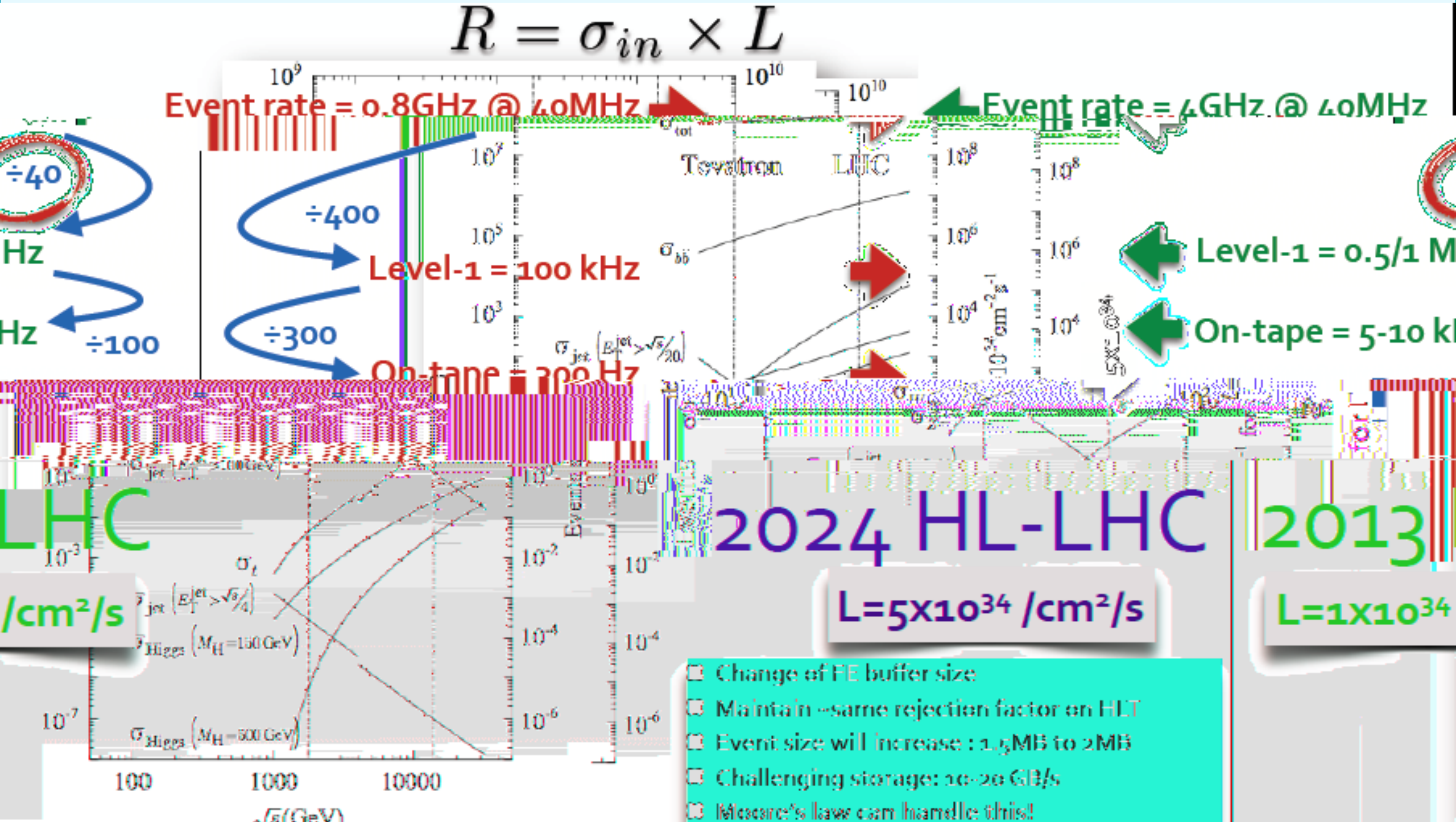
THIS IS WHY ….

Higher granularity: ex CMS case

	Current			Upgrade	
Outer	~200 m^2	Silicon		~220 m^2	Silicon
	9.3 M	Strips		47.8 M	Strips
	0	MacroPixels	**x30**	217 M	MacroPixels
	15'148	Modules		15'508	Modules
	100 kHz	readout rate		40 MHz	readout rate*
Pixel	~1 m^2	Silicon		4.6 m^2	Silicon
	66 M	Pixels	**x15**	O(1) G?	Pixels
	1440	Modules		??	??
	100 kHz	readout rate		0.5~1 MHz	readout rate

* only high-pt hits read-out

Higher trigger rates at HL-LHC



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To overcome these challenges all the LHC experiments will build new tracking systems (let's concentrate on ATLAS & CMS)

ATLAS & CMS are developing new All-Silicon tracking systems (~200 m^2 each); It implies a lot of R&D and collaboration with Industry in several high tech related aspects.

- New FEE and readout electronics digitized on detector (mix-mode 65nm CMOS based techno).
- Include the tracking system in the early selection stage of the trigger system.
- ATLAS & CMS: Different approach with some common R&D's.
- *C* *FE*
- *C*

HPC need at the intermediate stage in tracking data processing

This stage is at the interface between hardware based triggering level (Level1 or real time triggering) and the software based triggering level (High Level Triggering (HLT) based on CPUs farm).

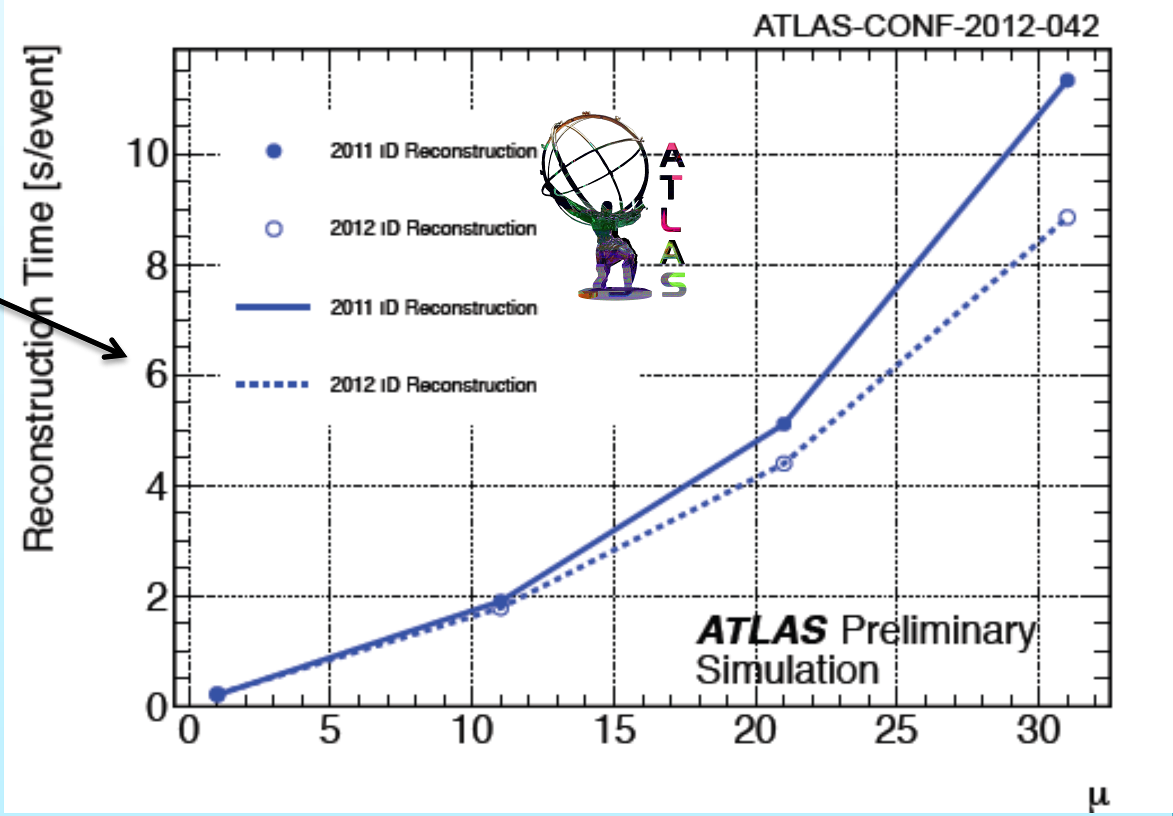
This is the so called Level 2 or pre-HLT data processing with processing time of O(100-1000 μs).

It allows including more sophisticated selection than Level1.

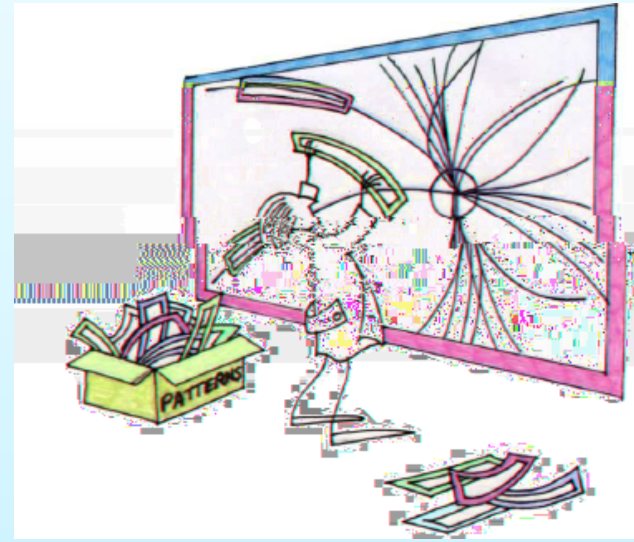
Ex: Intermediate Track Trigger approach before H.L.

The increase in Luminosity, even before HL-LHC, is very expensive in reconstruction time. This is due to the HUGE COMBINATORIAL PB, very non linear with number of interaction:

=> Use algorithms in software run on CPUs: SLOW!!



ATLAS implements a track trigger, at Level 2, **the Fast Track Trigger (FTK)** to be already implemented in 2016. FTK is expected to solve these problems with a hardware based approach: FTK => Full detector reconstruction in less than 100μs.



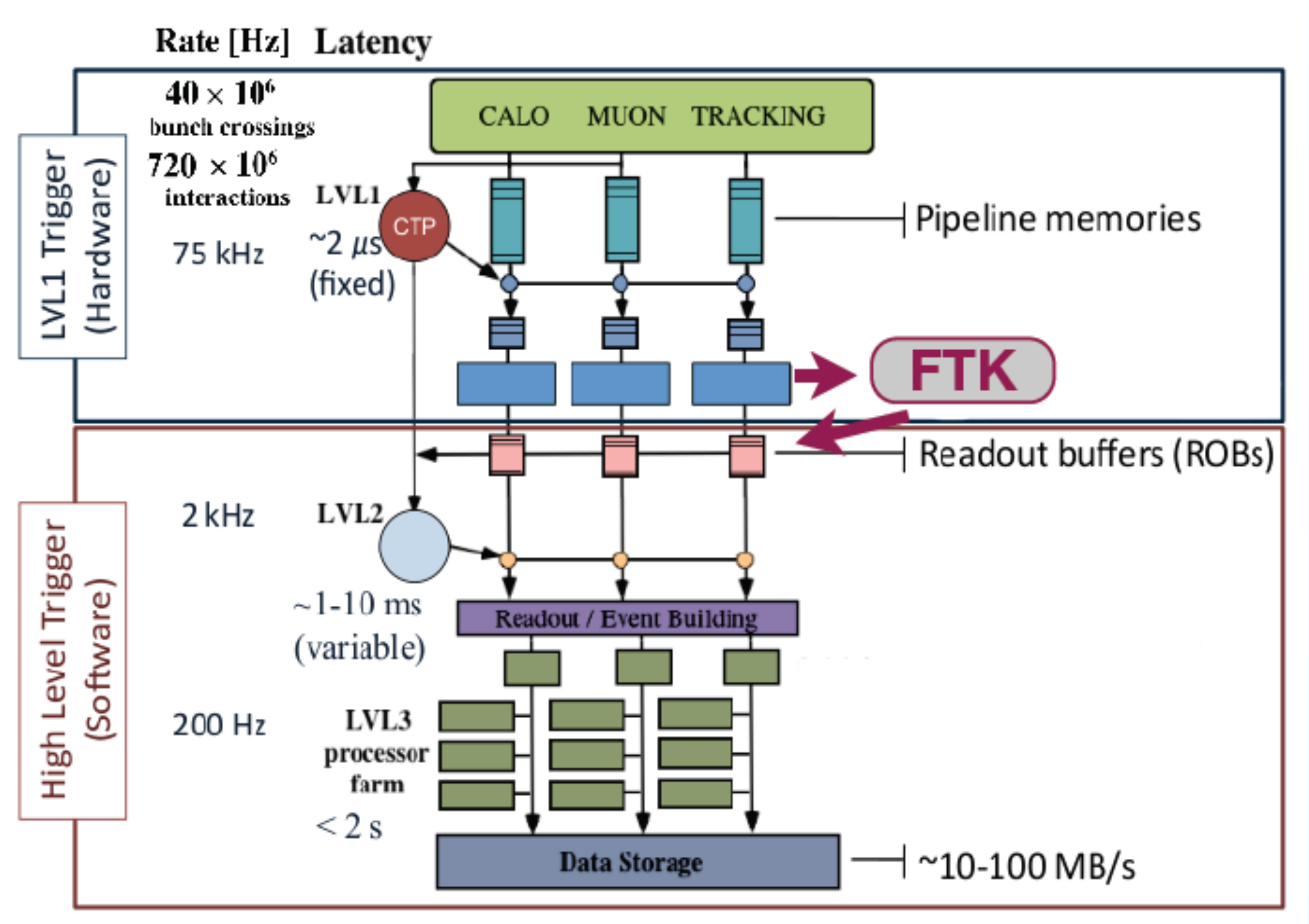
FTK: Fast Track Trigger

Derived from the Silicon Vertex Trigger (SVT) developed first by CDF at the Tevatron and successfully running (00 - 0)

The FTK concept is based on:

- Divide the detector in η-ϕ towers: **Parallelize** the pb
- Convert cluster into coarse resolution hits: **Reduce data volume**
- Compare hits to many **pre-stored track patterns** simultaneously: Eliminate costly loops
- Use a linearized fit for track candidates: **Simplify algorithms**
- All implemented in FPGAs or custom ASICs: **Hardware solution**

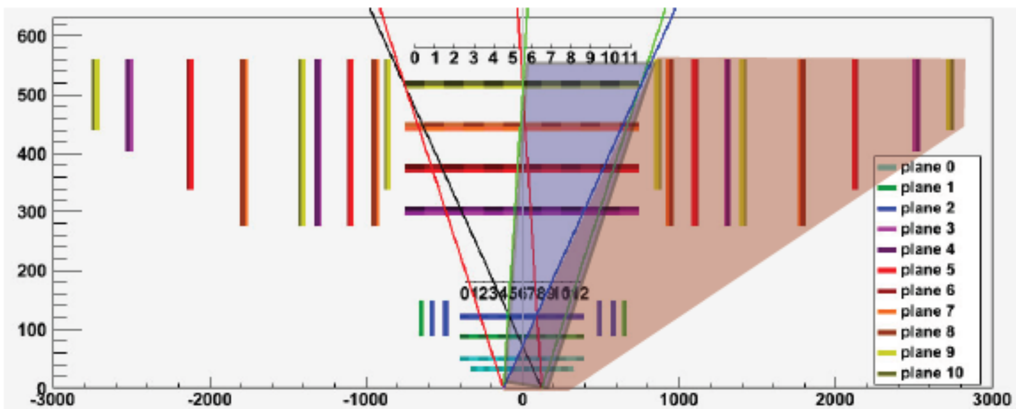
FTK in the ATLAS Trigger system

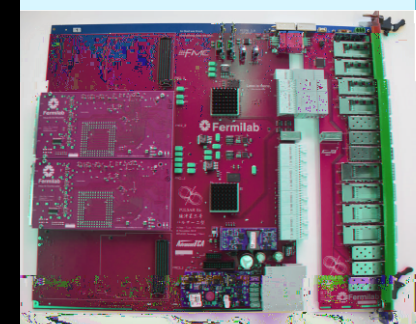


FTK - stage 1: clustering

- Receive data from silicon detectors
- Cluster pixel hits using sliding window algorithm in FPGA
- FPGAs on clustering mezzanines on Data Formatter boards

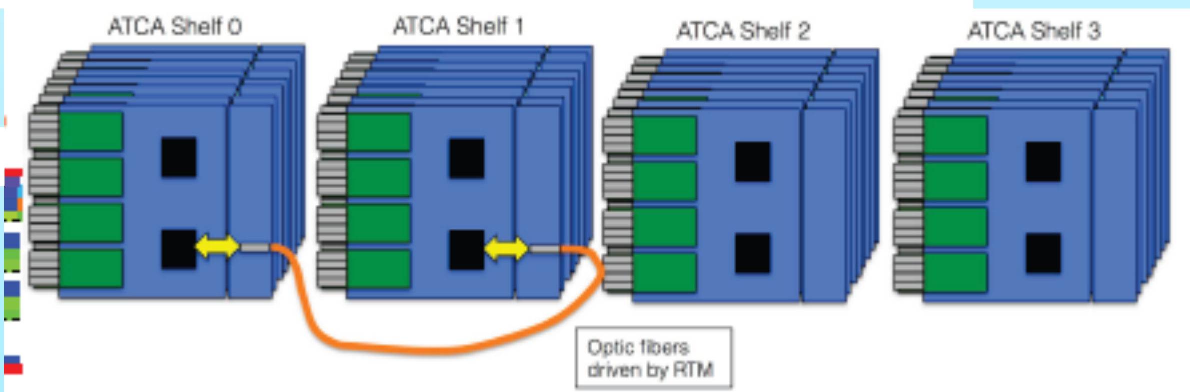
- Route clusters to FTK eta-phi towers

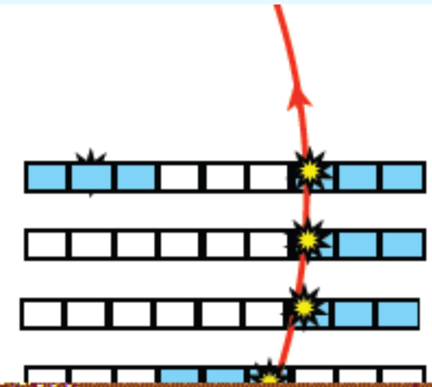




- Implemented in ATCA crates with full mesh backplane
- 32 DF boards in 4 crates

- Each DF connects to 2 towers





- Hits are ganged into Super Strips (SS)
  - Roughly 15x36 pixels/16strips per SS @ 70 int/x-ing
- Custom associative memory chips are used to compare hits to O(10 simultaneously
  - Pattern matching finished a hits are read.

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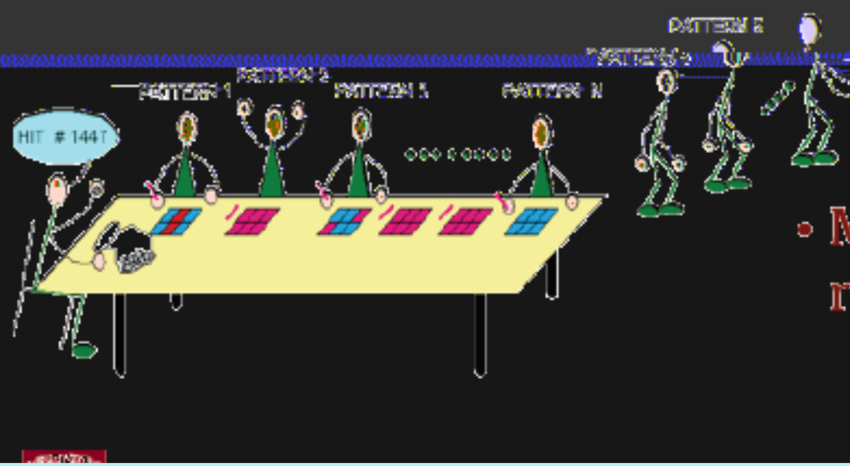

e then fit to
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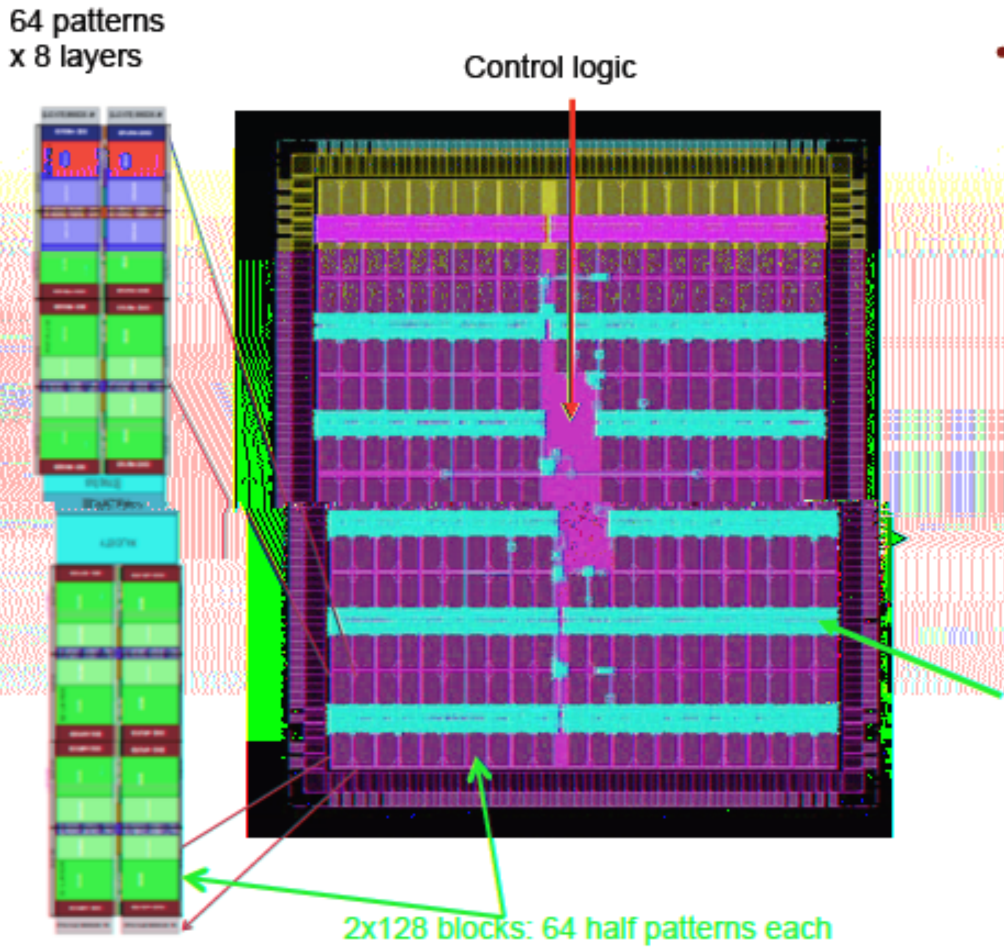
- Matched patterns (Roads) ar reject bad roads
  - Most matches are fake, nee reduce bad rate

FTK : the custom Associative Memory (AM) chips

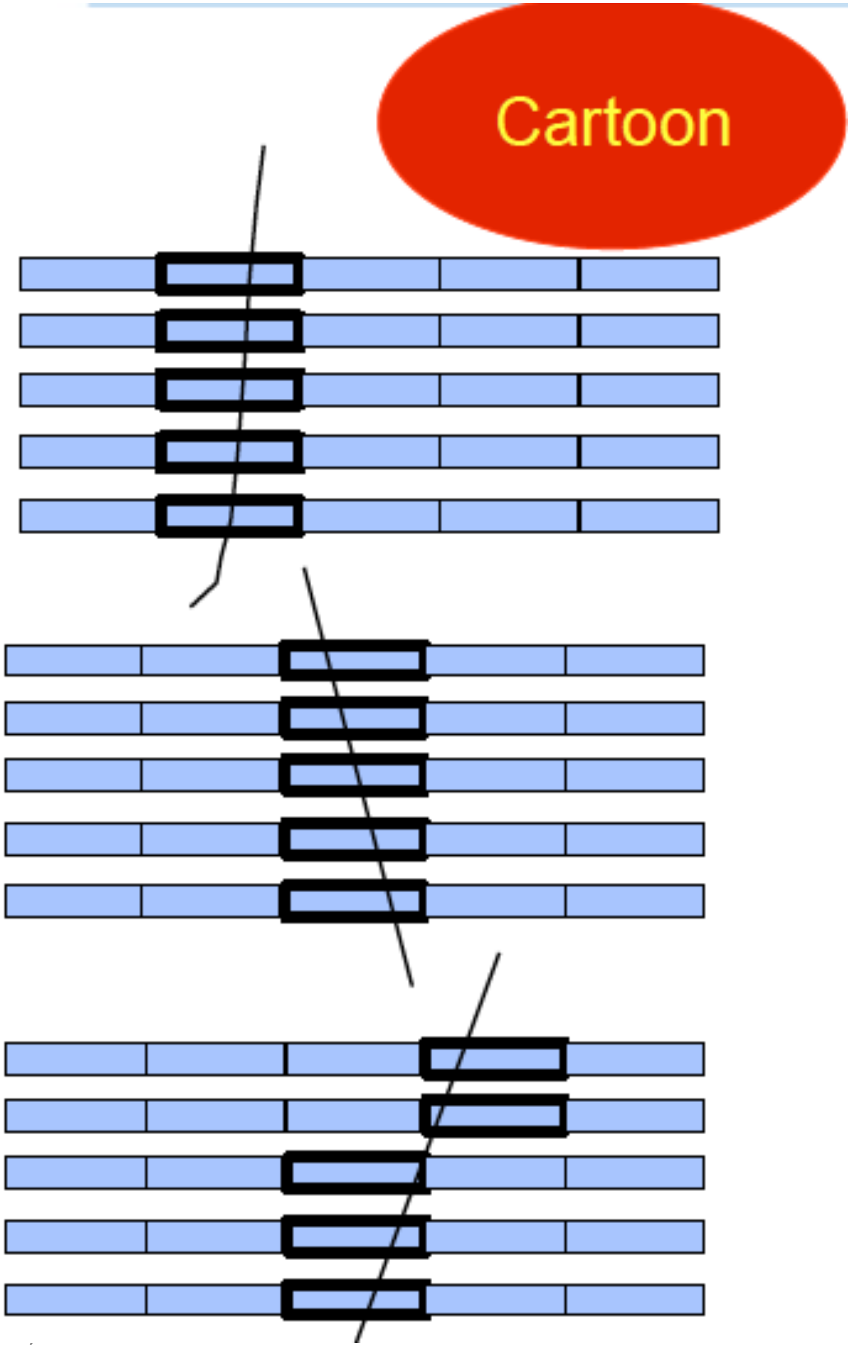


- AM Chips: 64 nm custom associative memory chips
  - 8 Layer (Pix + 4 axial SCT + 1 stereo SCT)
  - 3-6 bits for variable resolution patterns
  - Low power design: ~2W/chip, a factor 30-50 reduction in power/ pattern/MHz over predecessor SVT chip
- Functionality demonstrated in small area chips
  - 8k patterns

F. Alberti *et al* 2013 *JINST* **8 C01040**, *doi:*10.1088/1748-0221/8/01/C01040

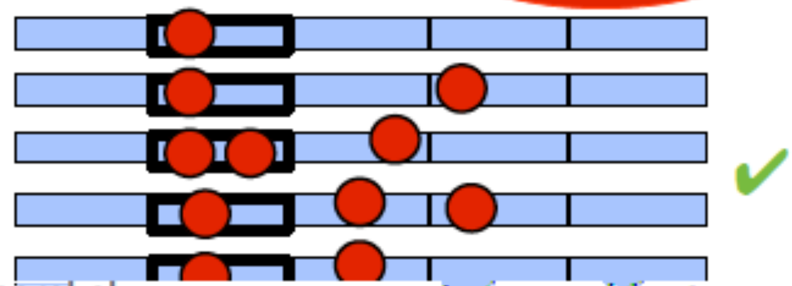
Pattern Matching

- The pattern matching uses **custom** Associative Memory (AM) ASICs pre-loaded with 1B patterns
  - All 1B patterns are matched in parallel



Pattern Matching

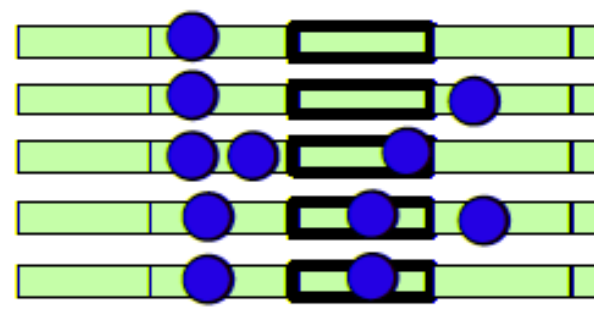
Cartoon

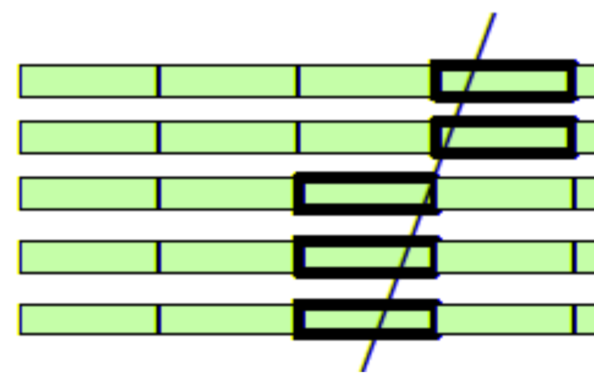


- The pattern matching uses **custom** Associative Memory (AM) ASICs pre-loaded with 1B patterns
  - All 1B patterns are matched in parallel

X

- Matching pattern IDs and the hits sent to the next stage
- Hits not matching a pattern are not passed to the next stage





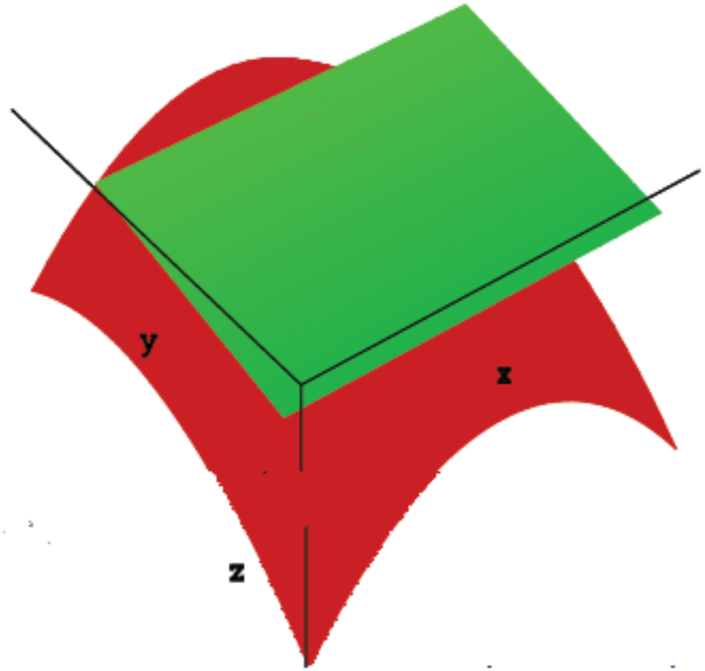
FTK-stage 3: 12 layers Track Fitting

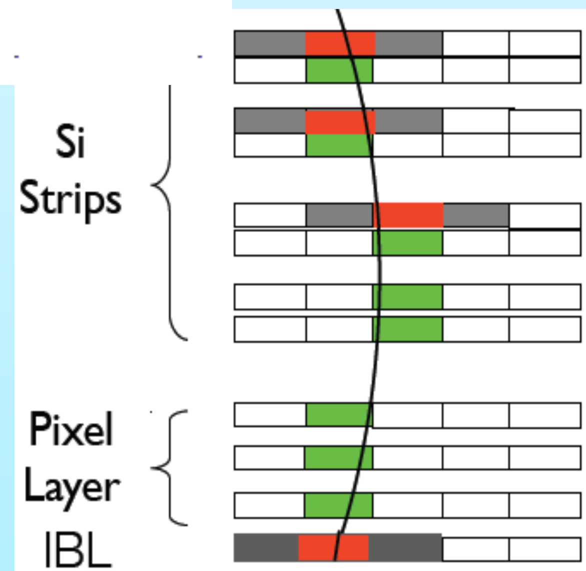
- Determine the helix parameters and χ^2
- Linear fit one module in each layer

$$p_i = \sum_{j=1}^{14} a_{ij} x_j + b_i$$

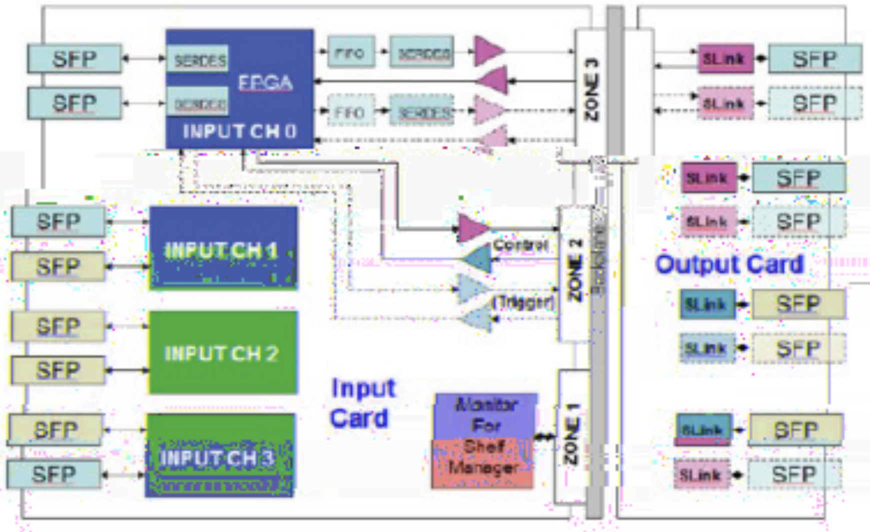
  - P_i: the helix parameters and χ^2 components

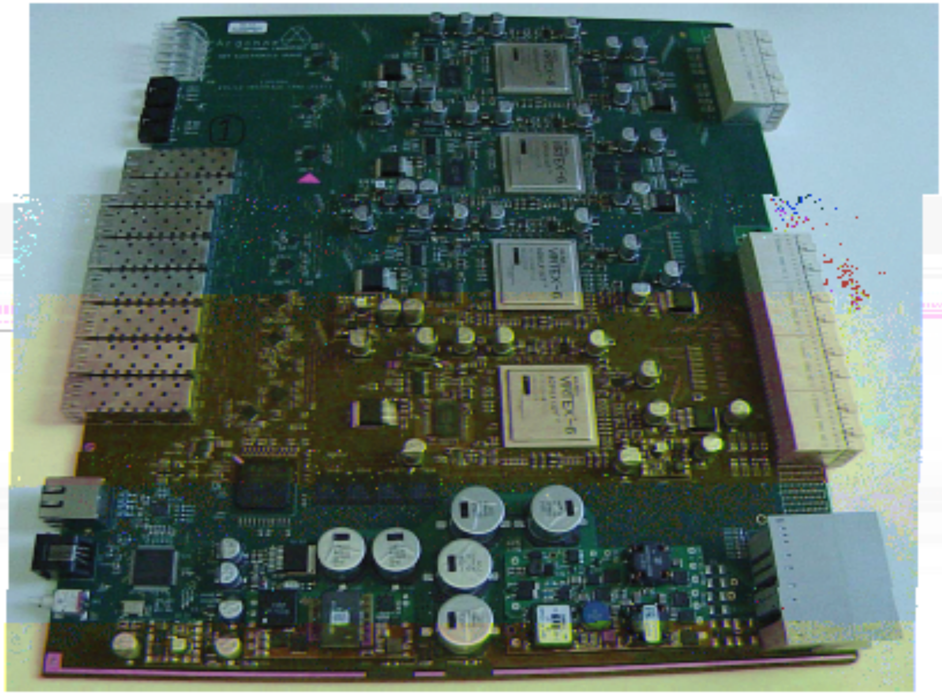
- Very fast in FPGAs (~1 ns per track)





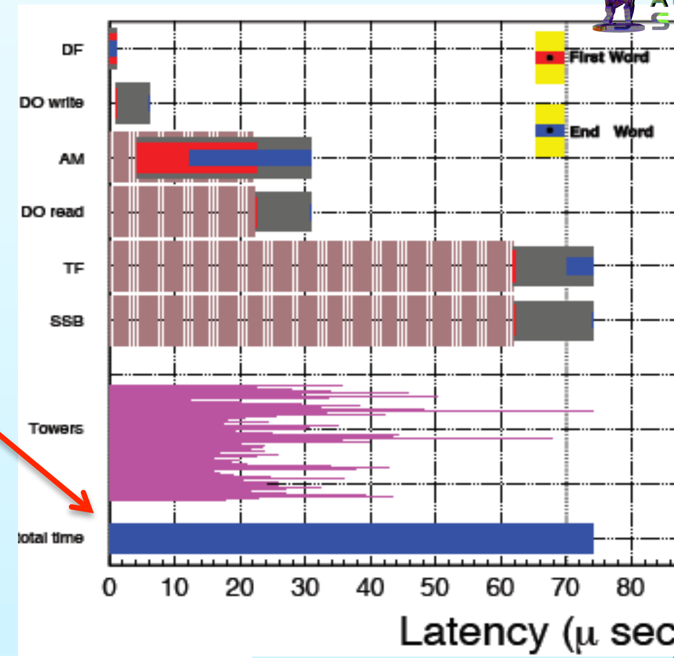
- FTK to Level 2 Interface Crate connects FTK to HLT
  - Formats data for HLT
  - Also does monitoring and control
- Uses dual-star ATCA crate
  - Will allow for local trigger processing (primary vertex finding, beamspot, MET, etc.) in the future

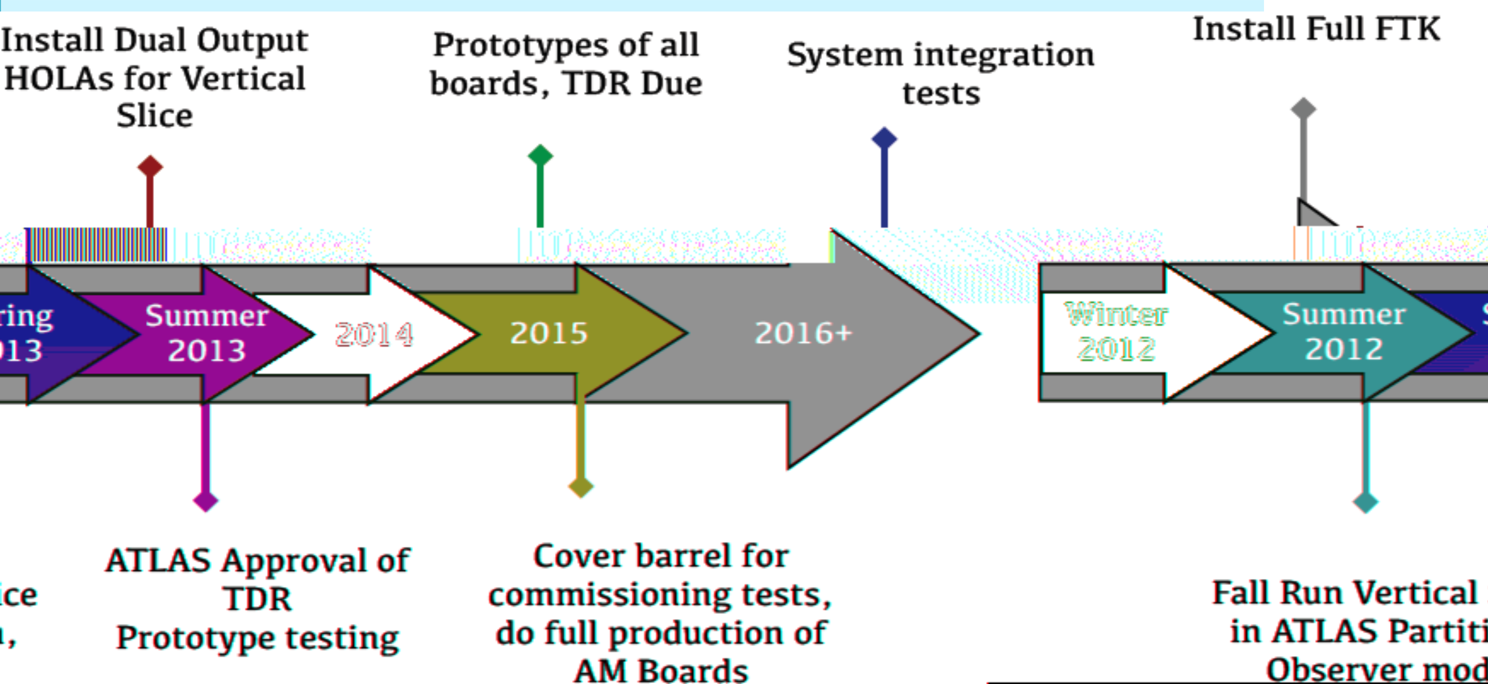




FTK timing performance & workplan/installation

- Detailed timing studies based on per-word processing times for entire system
- 100 µs latency achievable at 70 P.U. per BX
- Expected to be installed and running for the second part of Run 2 (i.e. after 2016-17)





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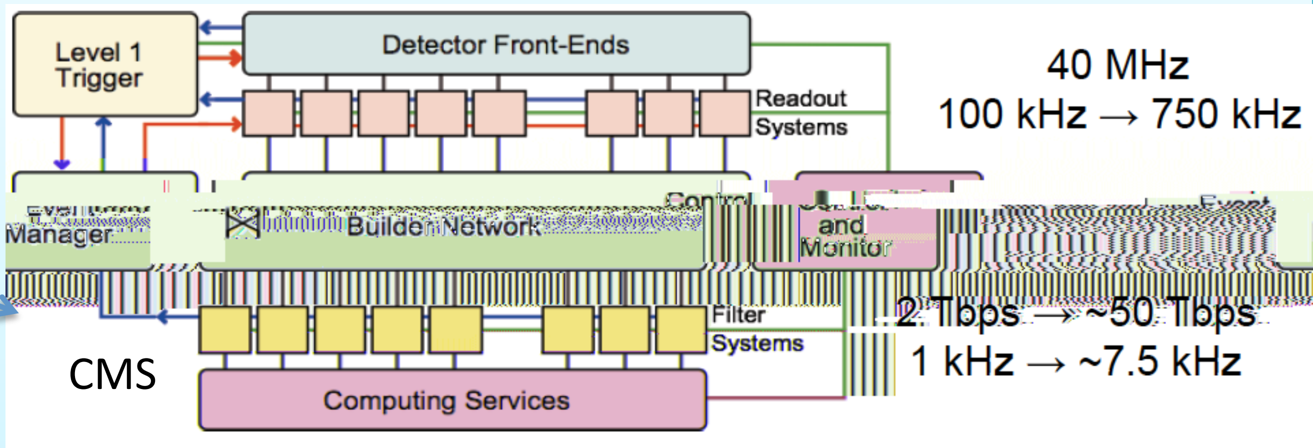
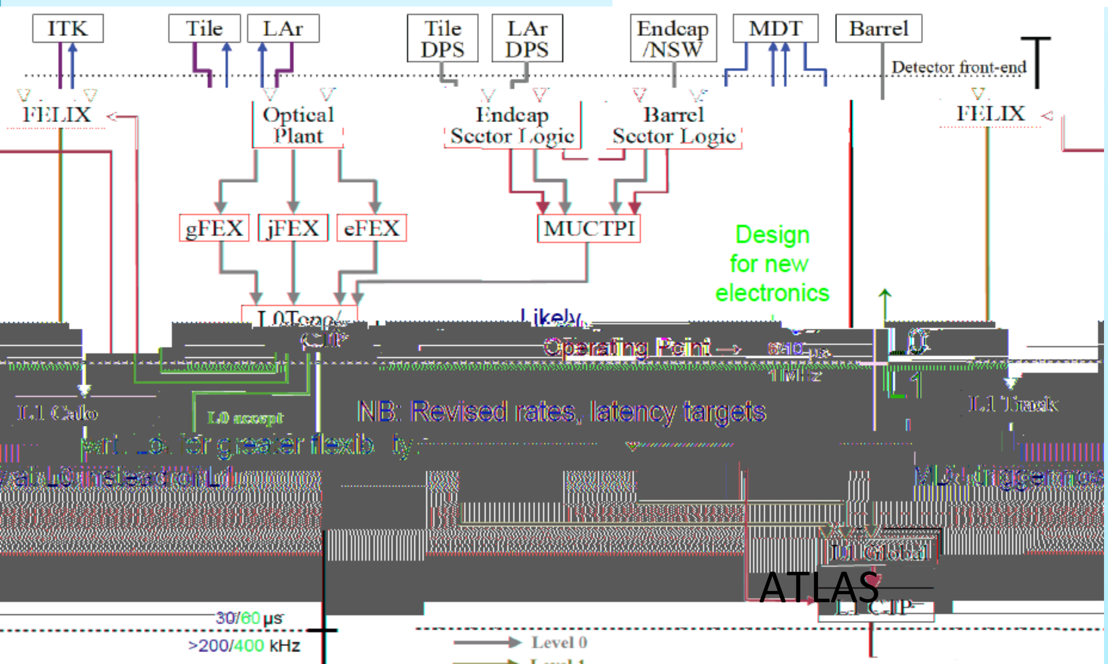
AM for Level 1 track trigger at HL-LHC ?? => Active R&D ongoing

Two different trigger strategies





Different approaches: ATLAS vs CMS:

- Different Si tracking system designs
- Different triggering architectures
- Different track trigger strategy
- CMS is relying on the use of A.M. for track triggering at L1.
- Alternative approach: Use of new FPGA and tracklets (CMS)

FTK like system for L1 at HL-LHC??

=> Ongoing R&D including heavy simulation studies load

The entire data processing flow has to be fully simulated both for:

- Developing trigger strategies at HL-LHC
- Support hardware design/finalization

NEED For HPC

VERY COSTY IN CPU & CHALLENGING

- The use of algorithms tailored for a large electronics system is resource intensive
- Memory size and access are the main challenges
  - FTK has **one billion patterns** that require about **35 GB** of memory
  - **Two million fit constants** require about **2 GB**
    - Plus smaller configuration data
  - Commissioning FTK configuration will be less demanding (0.25B patterns)
    - But still with significant memory requirements
- The simulation of such a highly parallelized system on general-purpose CPUs has inherent performance bottlenecks:
  - Limited parallelism
  - Low bandwidth access to memory: ~25 **GB/s**
    - In comparison, the AM system has the I/O bandwidth of about 25 **TB/s**

ACAT 201

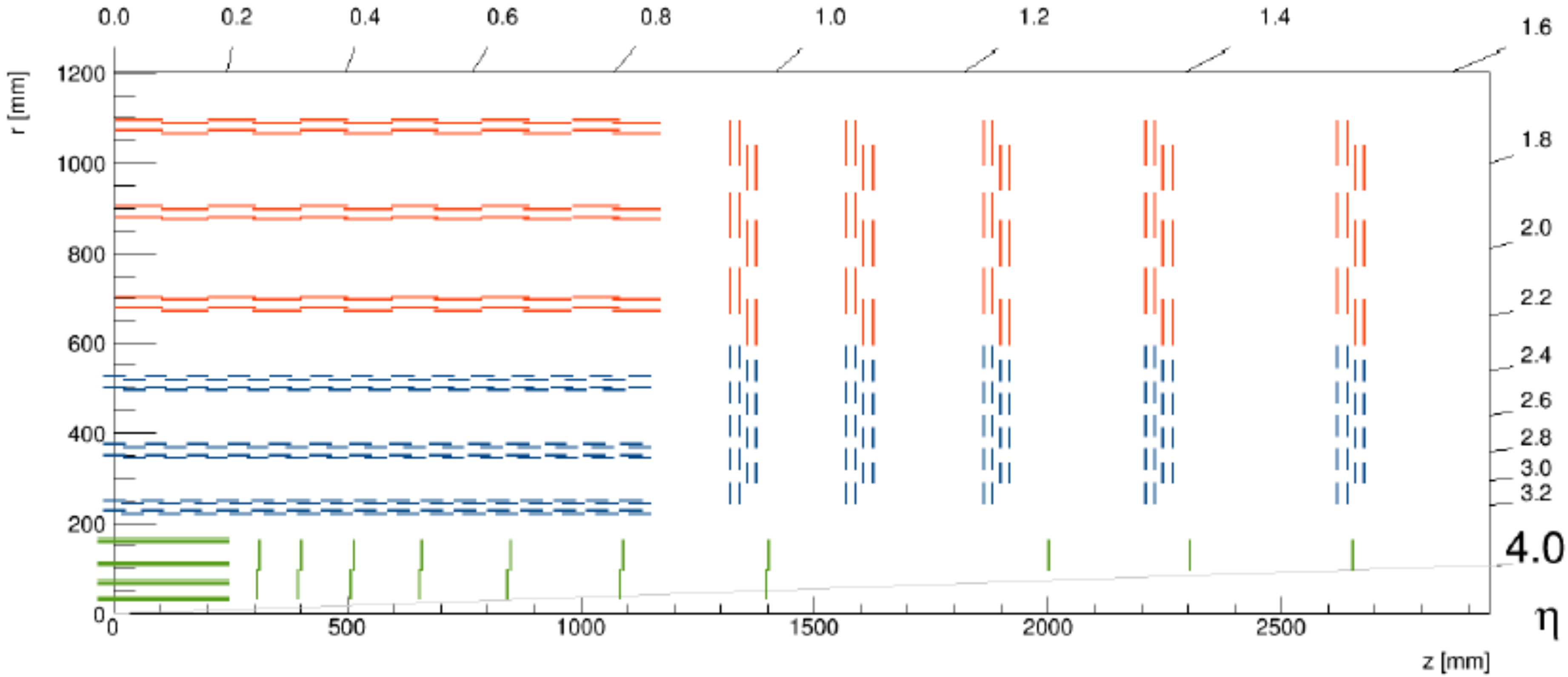
Input preparation
- RDO/RAW conversion and slimming

Associative Memory emulation
- Road finding
- CPU and RAM intensive, Large files

Track fitting
- CPU intensive

Filter tracks
- Duplicate removal
- Format conversion

L1 track trigger at HL-LHC another approach



Lower density
2S modules outside
(~8400 modules)

PS modules middle
z info in trigger
θ info in trigger
(~7100 modules)

Pixel modules inside
accurate impact parameter resolution & forward coverage

More detailed model

No detailed model: using Phase-I detector layout w/ more disks in the forward

CMS tracker has a design architecture adapted to Level 1
see next slide..

CMS tracker design is adapted to be a L1 device

Instead of RoI-based as ATLAS (PULL device), CMS tracker works in PUSH mode (as Calo or muon) i.e. in standalone mode:

Need to ship hits off detector

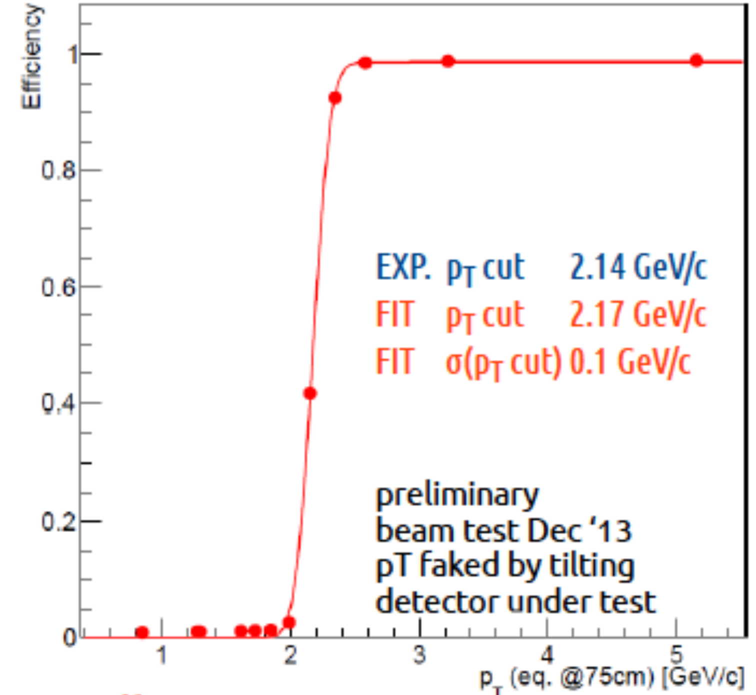
Ship all hits @ 40 MHz? No

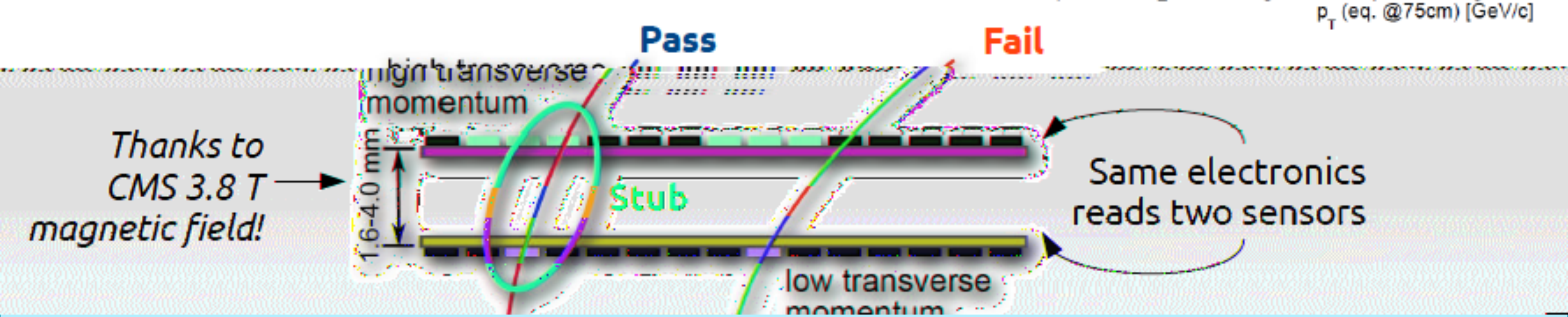
- Bandwidth needed: off by 1 order of magnitude (order of 10 Gbps per module)
- Track reconstruction ~ impossible

Solution: ship only high-pT hits (stubs)

- Threshold of ~ 2 GeV
- Data reduction of one order of magnitude or more

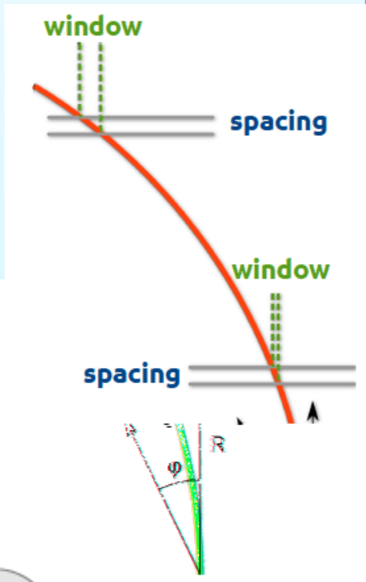
Modules with pT discrimination ("pT modules")





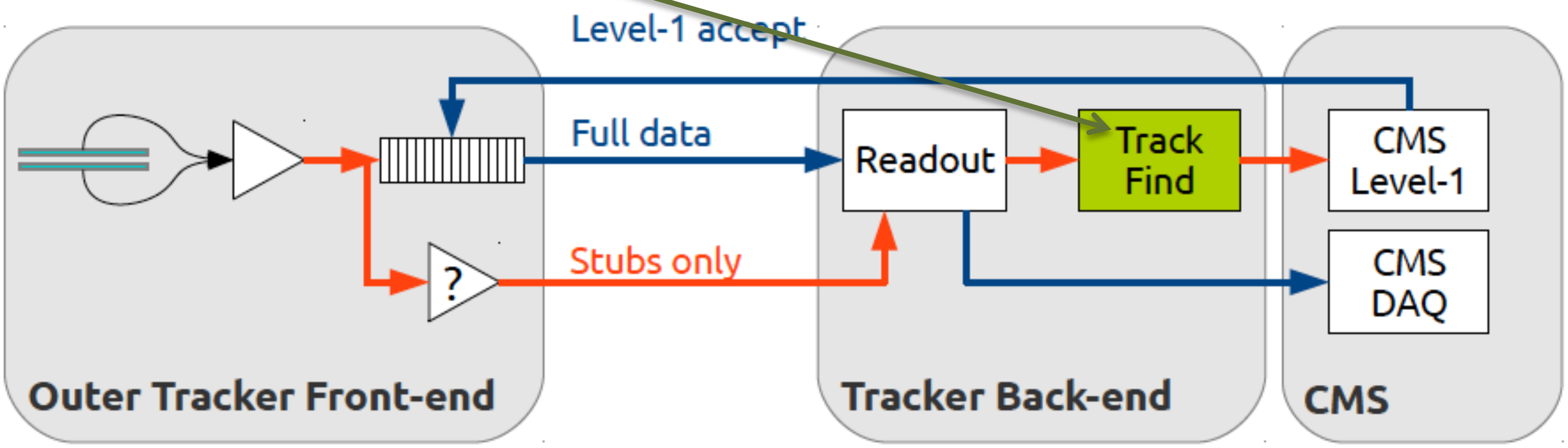
CMS tracker design is adapted to be a L1 device

The L1 stubs are processed in the back end => L1 tracks, with pT>2 GeV, contributing to CMS L1 trigger



Extreme challenge: reconstruct O(100) tracks at 40 MHz

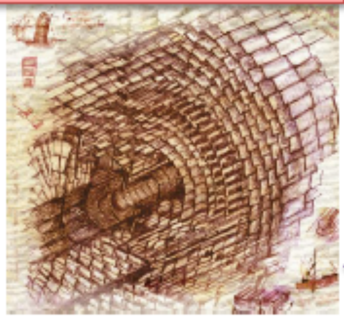
Track-finding step approach being studed



@ 40 MHz – Bunch crossing
@ 500 kHz (1 MHz) – CMS Level-1 trigger

L1 track trigger at HL-LHC: R&D

Detector design for triggering



Silicon Based Tracking Trigger

Data transfer

Data formatting → Partition detector into trigger towers (*divide and conquer*)

Pattern Recognition (PR) → Choice of PR impacts the system design

Track Fitting → Finer pattern recognition

Two PR approaches being pursued at CMS

6x8 = 48 towers	Associative Memory approach		Linearized Track Fitting
28 towers	Tracklet-based Approach		Hough transform

or Divide & conquer with massive parallelism: to process in parallel different regions of the detect for the same beam crossing *(regional multiplexing)*, and different crossings (time multiplexing).

L1 track trigger at HL-LHC: R&D

Detector design for triggering

Challenge: ***The feasibility of CMS L1 Tracking Trigger has to be demonstrated before TDR (~2017), using today's technology and then extrapolate into future …***

Emulate tracker output using HL-LHC simulation data

Data transfer

Data formatting

Partition detector into trigger towers (*divide and conquer*)

Pattern Recognition (PR)

Choice of PR impacts the system design

Track Fitting

Finer pattern recognition

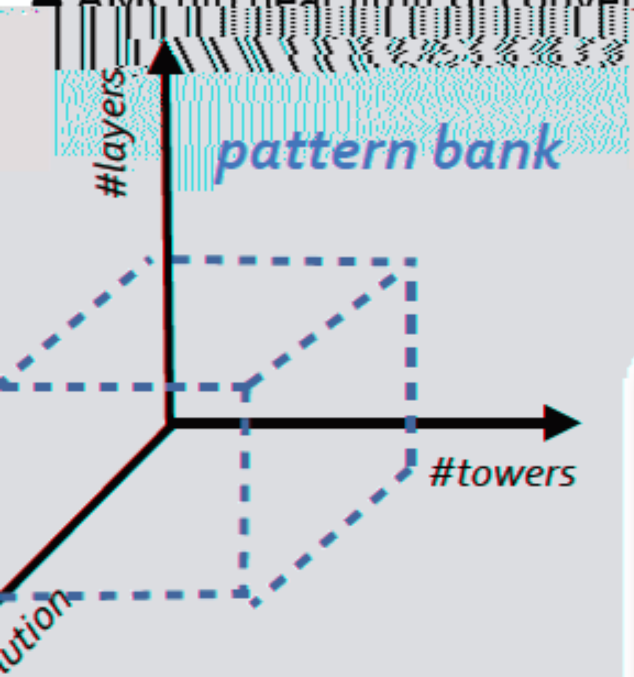
Tracks out

Processing Latency Δ t ?

Only some highlights/snapshots on recent progress/status:

L1 track trigger at HL-LHC: Limits on the AM approach

- Performance fundamentally limited by Moore's Law
- AMChip near limit of conventional associative memory densities



- Earlier studies demonstrated that ternary CAMs can be used with 10 billion patterns or more, doing a pattern lookup in < 200 ns

A challenge for HL-LHC

Increase the patterns density by 2 orders of magnitude

Increase the speed by a factor of >~ 3

while keeping similar power consumption

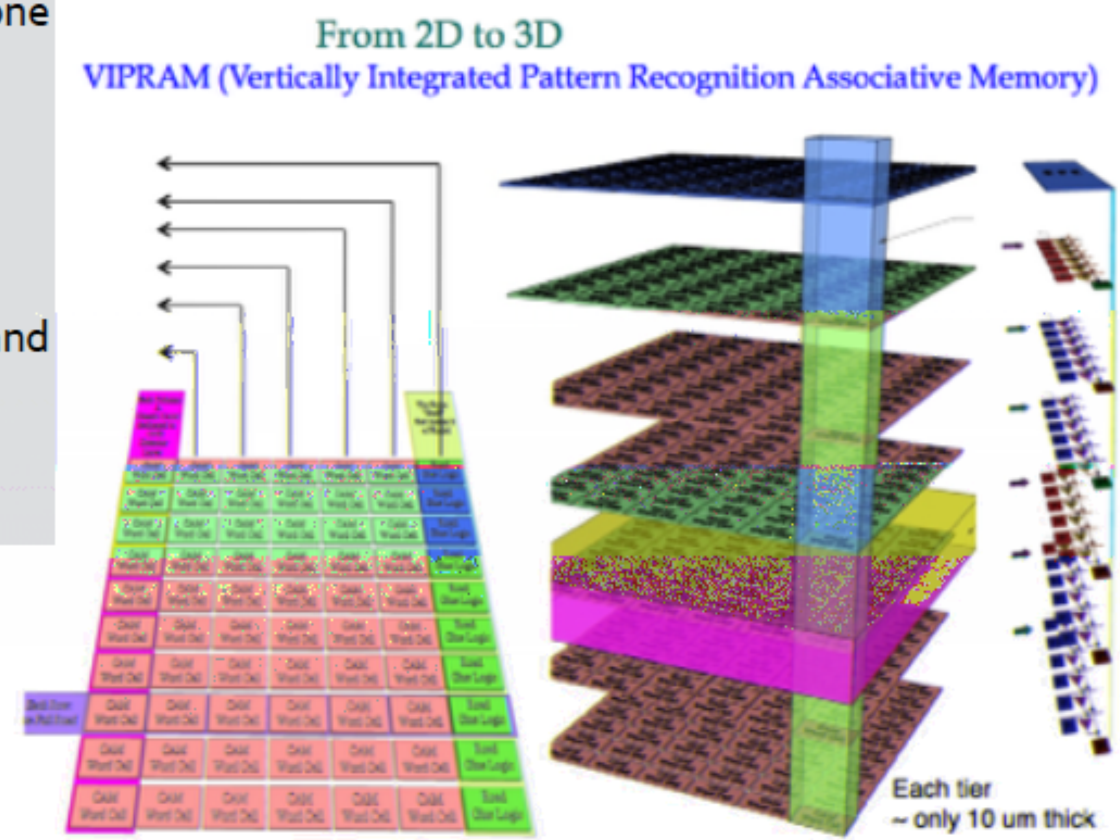
or

go to higher dimensions

Pushing the AM approach to

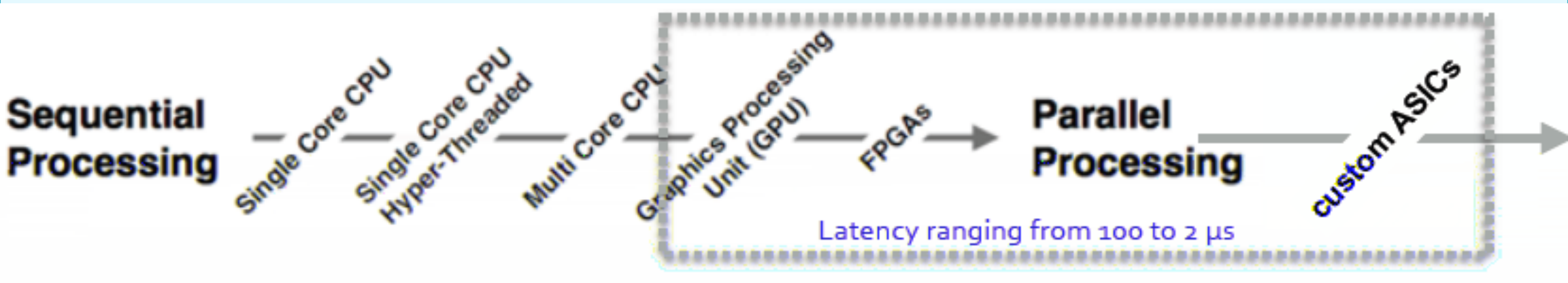
FermiLab Project VIPRAM (led by T.H. Liu) using the advanced TSV 3D integration by Tezzaron is pushing further the A.M. approach

- One cell can process N layers in about one CAM cell size ⇒ density increased by N
  - 2D with 65 nm: ~50K patterns/cm^2 (AMchip04)
  - 3D with 130 nm: ~200K patterns/cm^2
- Reduced connections ⇒ higher speed and less power density
- More flexible design



Answer = full proof for LHC to be given by 2017

Looking for other approaches => small incursion on



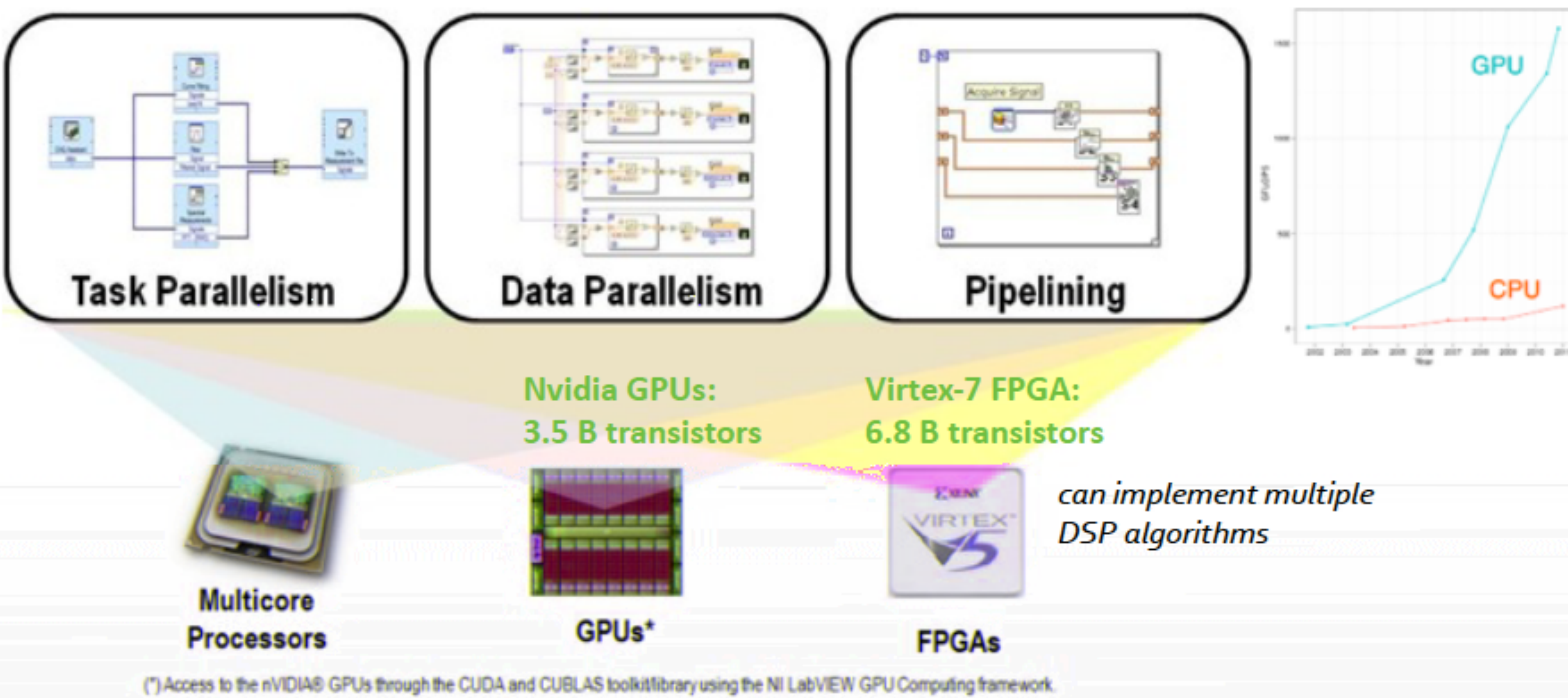
- **Follow the evolution of digital integrated circuits on a single chip**
  The request of higher complexity => higher chip density => smaller transistor and memory size (down to 10nm?)
  and profit from the 3D vertical integration revolution.

- Look for Custom ASICs (ex AM-FTK) or else **look for Off-the Shell Components**
  Specific MIC ex: INTEL Many Integrated Core Architecture: INTEL MIC => INTEL Xeon Phi or new GP GPU's (NIVIDIA Cuda or Open CL compatible)
  New FPGAs: VIRTEX 7 and more

AND follow/collaborate with ONGOING DEVELOPMENTS in INDUSTRY

The gap in performance in latency, power dissipation and cost, easiness of programming between these different devices has been closing over these last years.

Technology trends: combining techno=right choice?

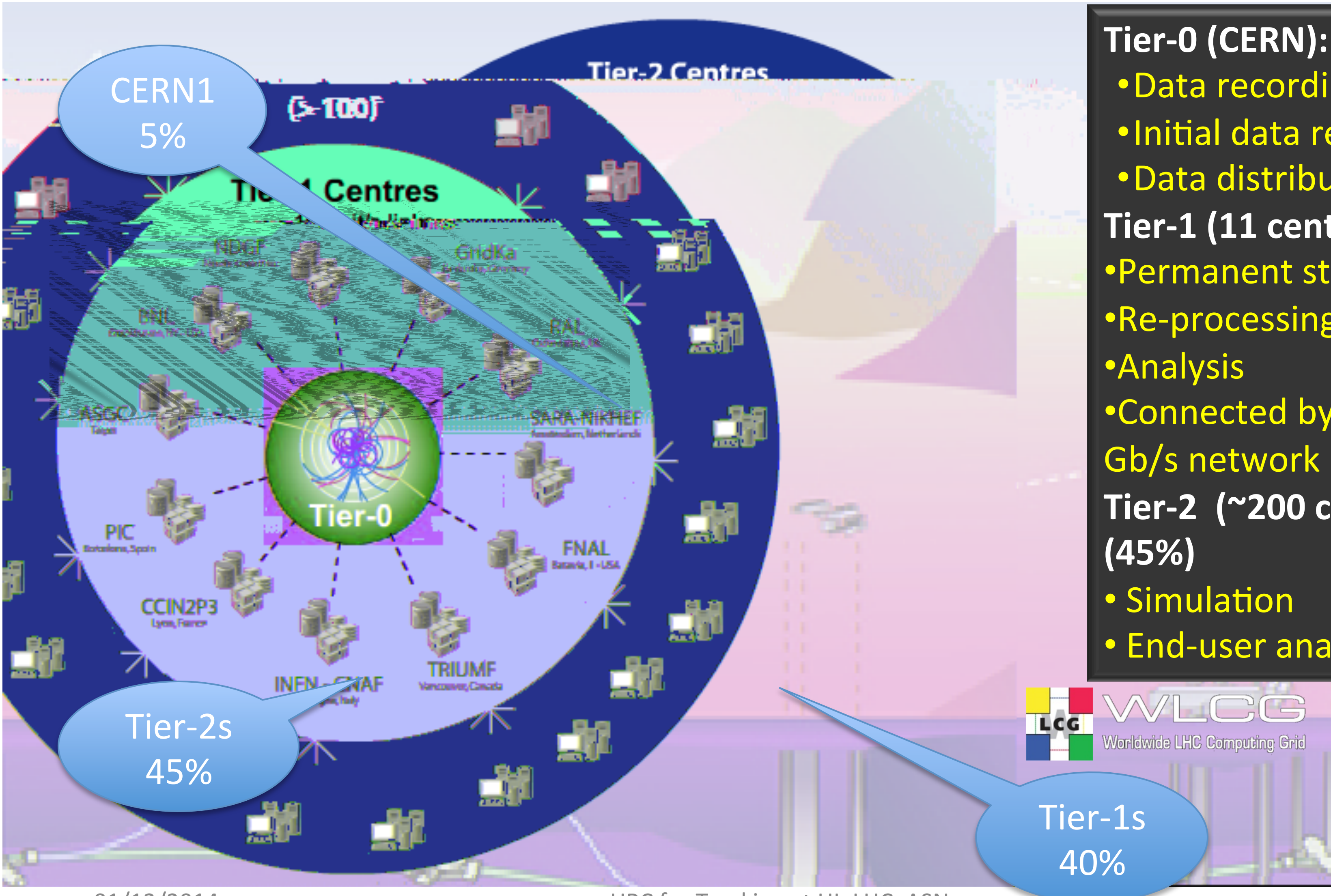


The right choice can be to combine the best of both worlds by analyzing which strengths of FPGA, GPU and CPU best fit the different demands of the application

Teams are actively studying these various alternatives in HEP especially for HL-LHC & in close collaboration with Industry

HPC at FAR-END of tracking data processing

- WLCG is a distributed computing infrastructure to provide the production and analysis environments for the LHC experiments. More than 200 centres in ~40 countries



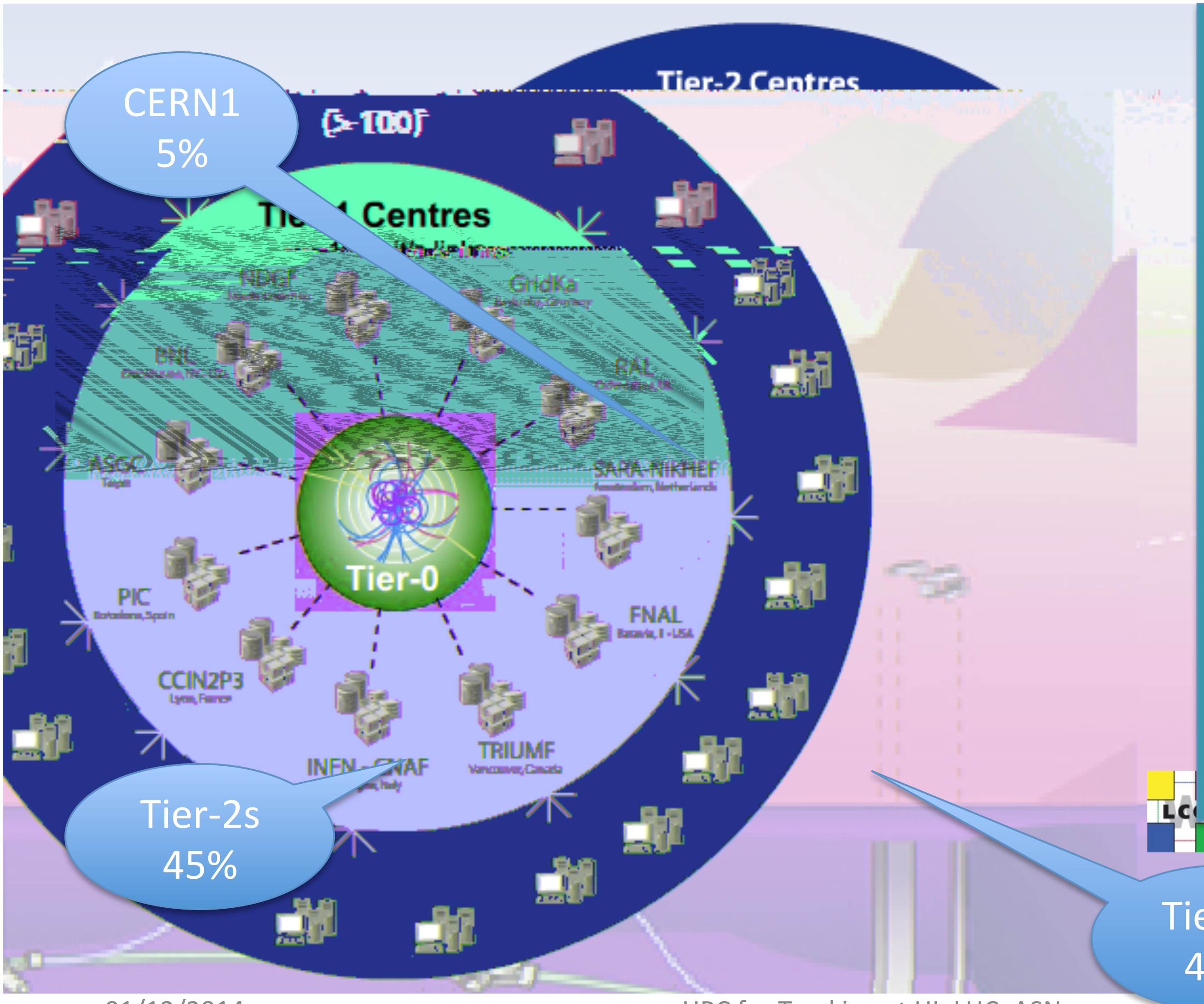
Tier-0 (CERN): (15%)
- Data recording
- Initial data reconstruction
- Data distribution

Tier-1 (11 centres): (40%)
- Permanent storage
- Re-processing
- Analysis
- Connected by direct 10 Gb/s network links

Tier-2 (~200 centres): (45%)
- Simulation
- End-user analysis

HPC at FAR-END of tracking data processing

Z!! THIS GRID-LHC COMPUTING FRAMEWORK IS ~ 20 YEARS OLD Z!!

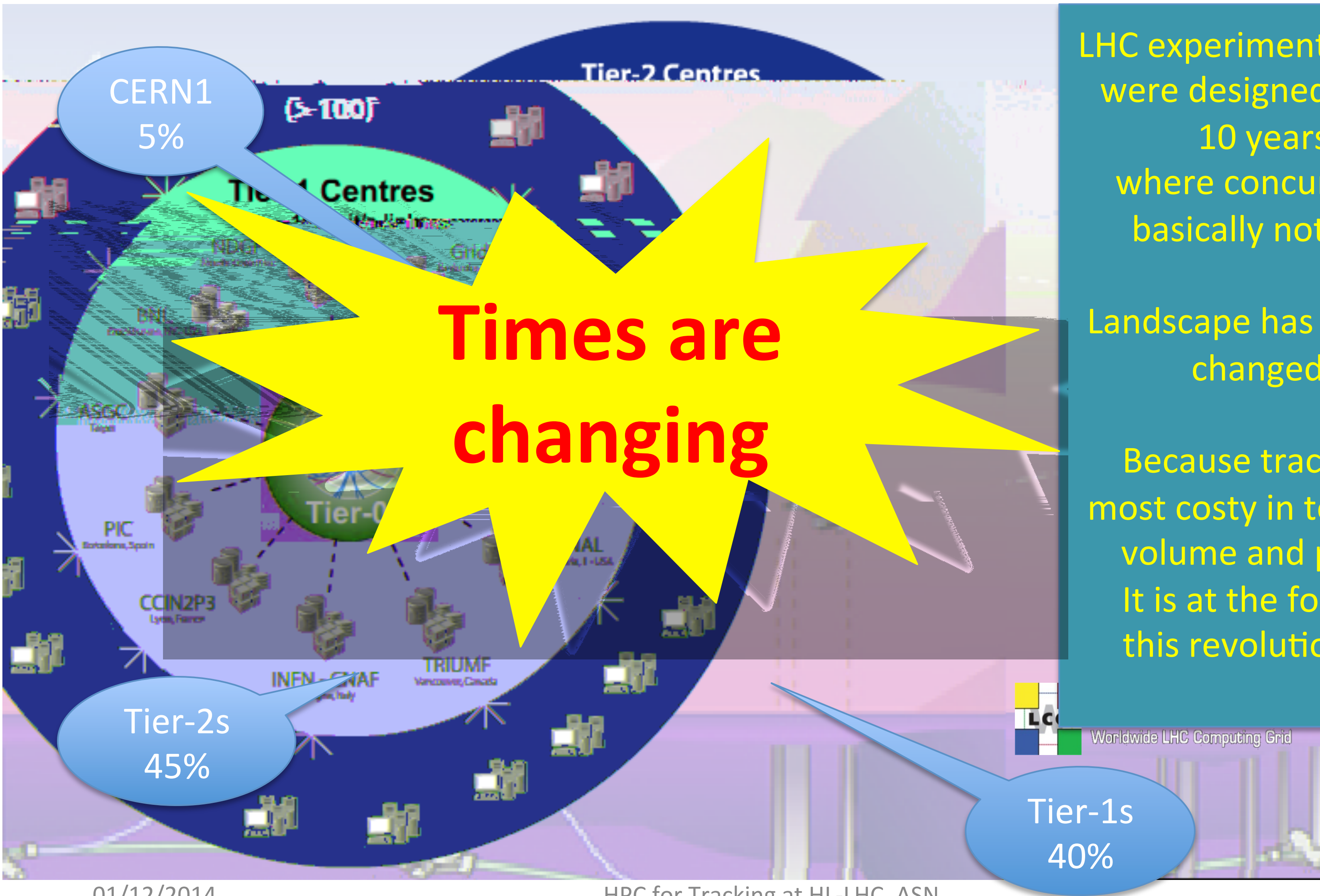


LHC experiments framework were designed more than 10 years ago, where concurrency was basically not an issue.

Landscape has dramatically changed now.

Because tracking is the most costy in terms of data volume and processing
It is at the forefront of this revolutionary time

HPC at FAR-END of tracking data processing



LHC experiments framework were designed more than 10 years ago, where concurrency was basically not an issue.

Landscape has dramatically changed now.

Because tracking is the most costy in terms of data volume and processing
It is at the forefront of this revolutionary time

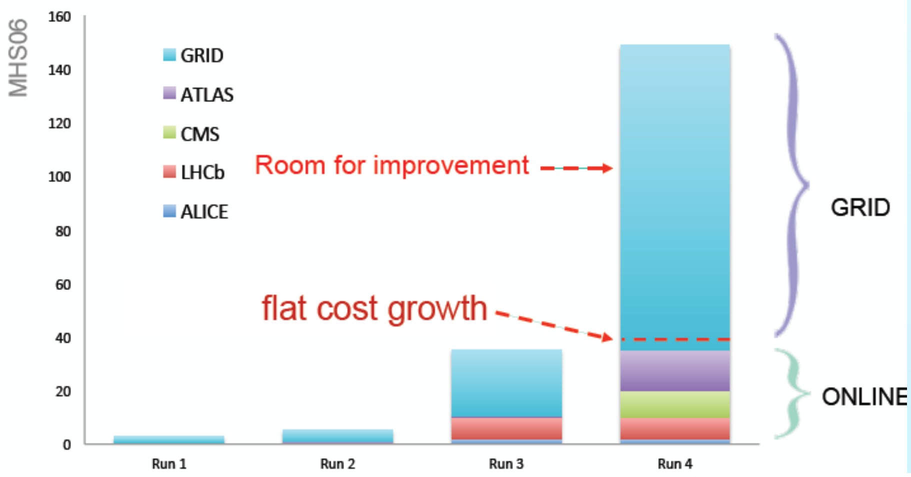
Ex: CMS computing ressources needs at HL-LHC

- CMS will record 5-7.5 KHz data => 25-37 B events/year
- Data will be more complicated to reconstruct and larger than event collected in 2015.
- Estimate is that the computing challenge will be 65 to 200 times worse than in the forthcoming Run2.
- Anticipating a factor of 8 in CPU improvements and 2 in code improvement => a deficit of 3 to 15 in CPU.
- Anticipating a factor 6 in storage improvements & having at HL-LHC events 4-5 times larger => deficit in storage of 4-5.

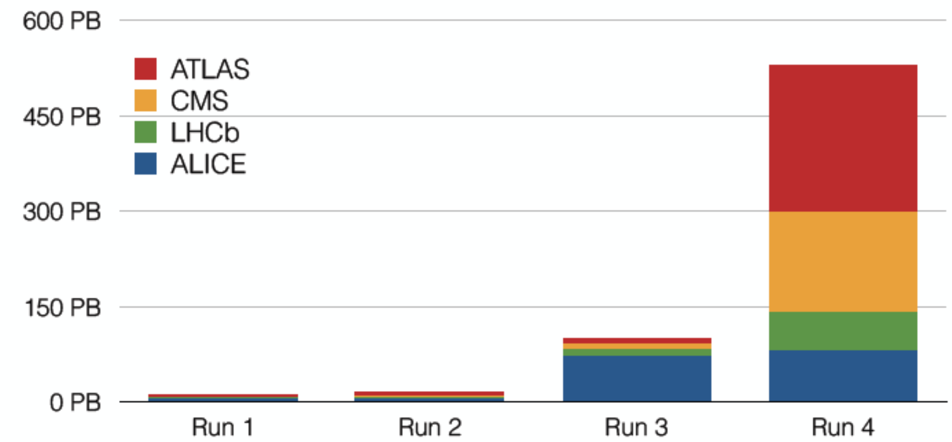
A lot of work & R&D on HEP Computing (collab with Industry ex INTEL Exascale Lab) in order to face these issues & move to the NEW COMPUTING ERA in HEP.

Computing needs @ HL-LHC: inflation, recession, crisis

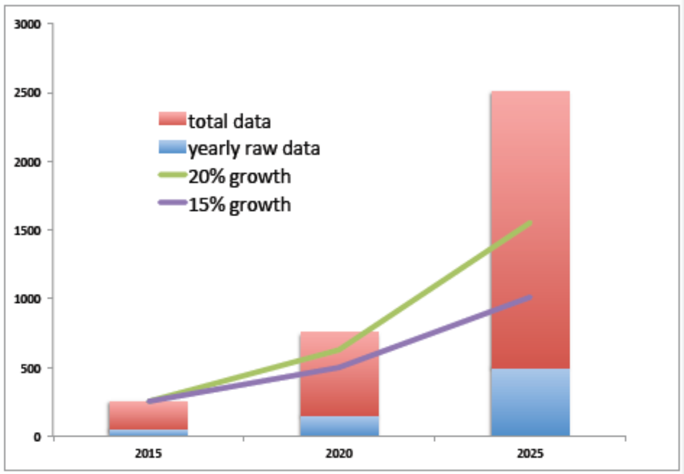
Scale of challenge: CPU



Scale of challenge: data



Active data - disk



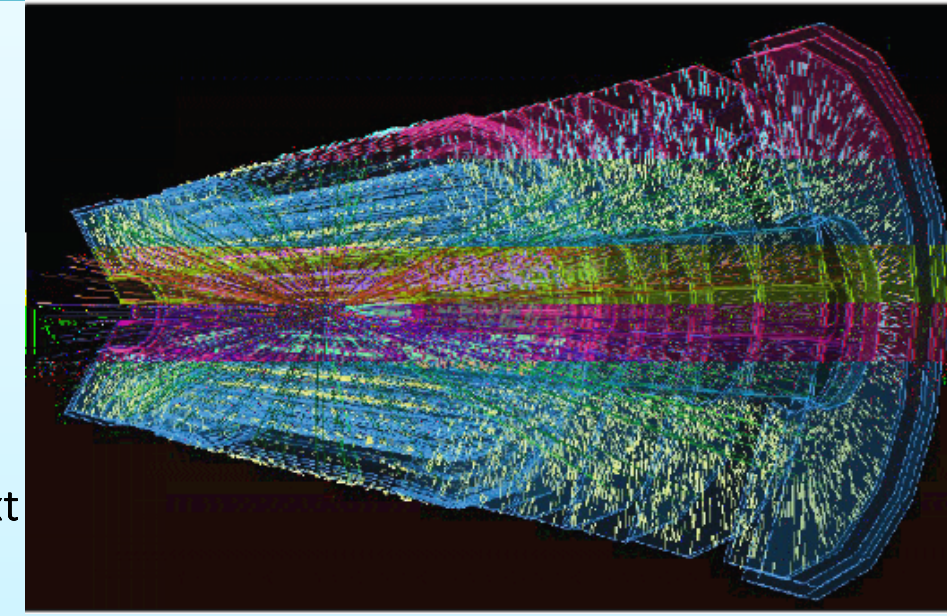
Life in a multi-core landscape

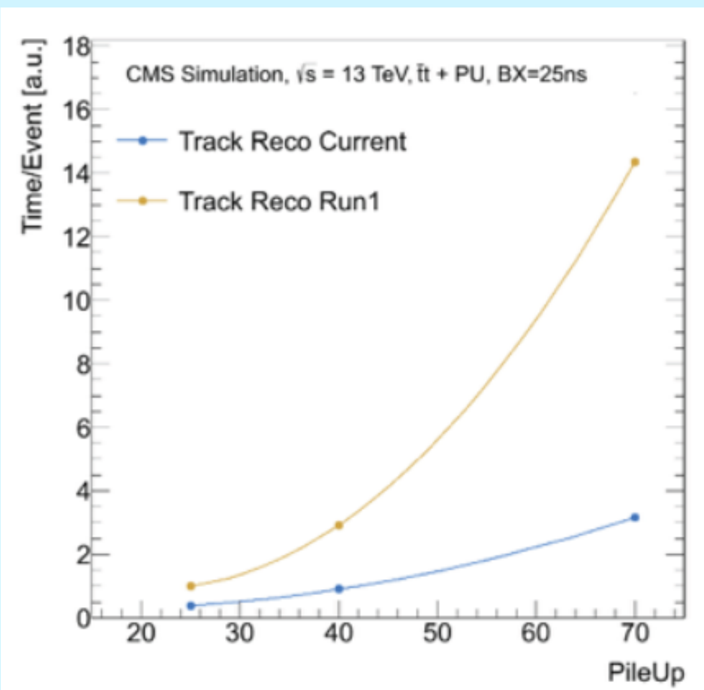
- Shift data processing paradigm to utilise the silicon more efficiently.
- Use heterogeneous systems: CPU+specialised coprocessors (FPGA+GPU).
- Adapt code where appropriate to use coprocessors.
- Multi-core utilisation.
  - Possible memory issues?
    - Multi-threading to relieve part of memory strain.
- Code optimisations:
  - e.g. vectorised code.

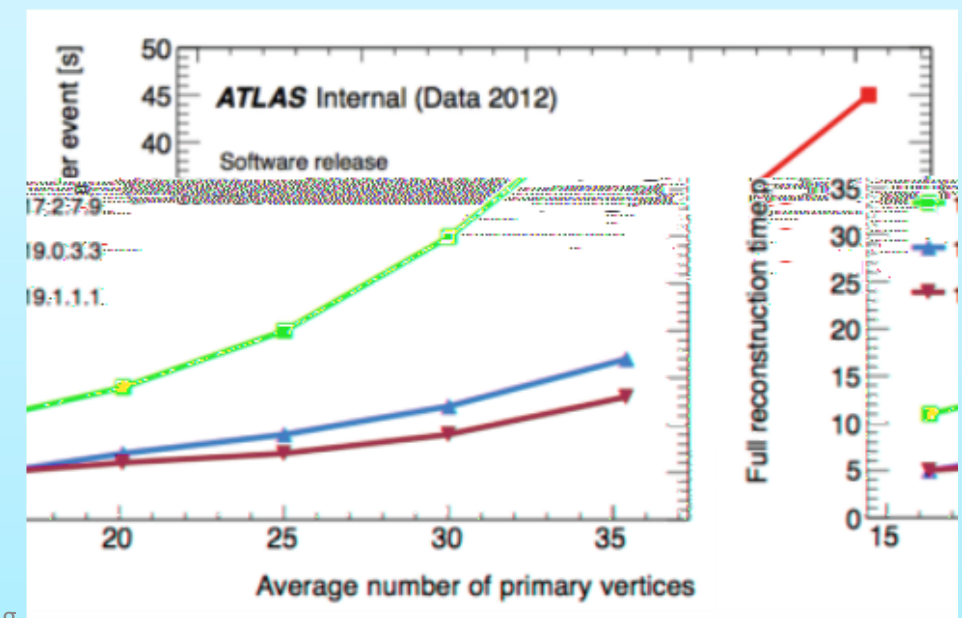
TRACKING FULL RECONSTRUCTION TIME

With increase in Luminosity and thus in P.U. the combinatorics of charged particle tracking becomes extremely challenging for General Purpose Detectors (large area tracking): ATLAS and CMS.

They both made impressive improvements In time spent in Full reconstruction, for the next Run. BUT NEED TO GO MUCH FURTHER





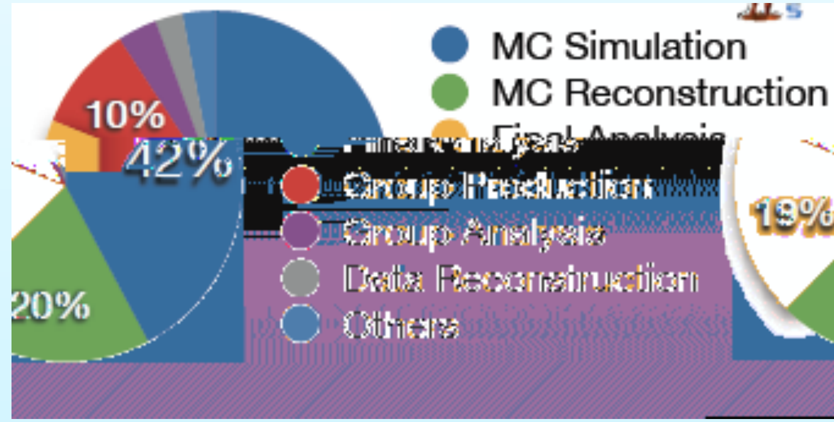


TRACKING & FULL SIMULATION TIME

Simulation is a very large consumer of offline CPU resources:

- GEANT 4 full GPDs simu:up to 1K seconds/evt
- Developed solution: adding Multi-threading support
- Future: GEANT V explores vectorization potential (INTEL Xeon Phi)

GRID CPU CONSUMPTION



TRACKING is a strong simulation consumer in several ways: most expensive part to simulate.

All studies needing full simulation & reconstruction of the tracker => All steps in Physics studies & analysis, detector design & performance studies etc.

Ex of a paricularly CRITICAL PB: simulation of A.M. by ATLAS FTK:

To simulate what AM does in 1 cycle takes CPU+DRAM millions of cycles.

[Options: Use a 2nd set of FTK hardware for FTK simulation farm

Attempt to use GPUs on HPC sites to help

Use a fast simulation to determine if FTK would have a matching track

(useful as long as fakes do not dominate FTK performance.]

HPC for Tracking at HL-LHC, ASN

Concluding remarks

- Large Area Tracking is an essential detecting device in HEP grand instruments and its role is becoming even more crucial at the HL-LHC
- It is at the forefront of HPC demands in HEP for:
  - Intelligent On detector real time processing
  - Sophisticated fast event selection using track reconstruction and matching with other detector pieces
  - For Full event reconstruction and data analysis to extract the Physics potential from HL-LHC and design the needed detector & electronic processing chain (simulation)
- It strongly relies on all the developments in HPC both HW and SW and will need a new generation of physicists able to work and further developed with these new HPC technologies. Collab with Industry is instrumental and benefitting both sides.

nirringrazzjak

Acknowlegdments

The speaker consulted a big pile of talks and documents from a number of people and thus us is very much indebted to: A. Vamachine, G. Carlino, L. Tompkins, F. Pastore, T.H. Liu, R. Patti, I. Shipsey, D. Lucchesi, R. Carlin A. Negri, V.V. Gligorov, S. Mersi, L. Rinaldi, M. Krzewicki, M. Garcia-Sciveres, G. Stewart, W.G. Smith, A.A. Grillo, J. Flynn, I. Bird…and, more generally, material from ATLAS, CMS, LHCb and ALICE collaborations for their upgrades for the High Luminosity LHC.

Apologize if anyone is missing in this already long list…