ENSC 225
LAB 4
Characterization of MOSFETs and MOS amplifier

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Part 1.1: Measurement of the I_D versus V_{GS} for the determination of V_t and K

The original plot for *n-channel* I_D versus V_{GS} is shown in Figure 1.

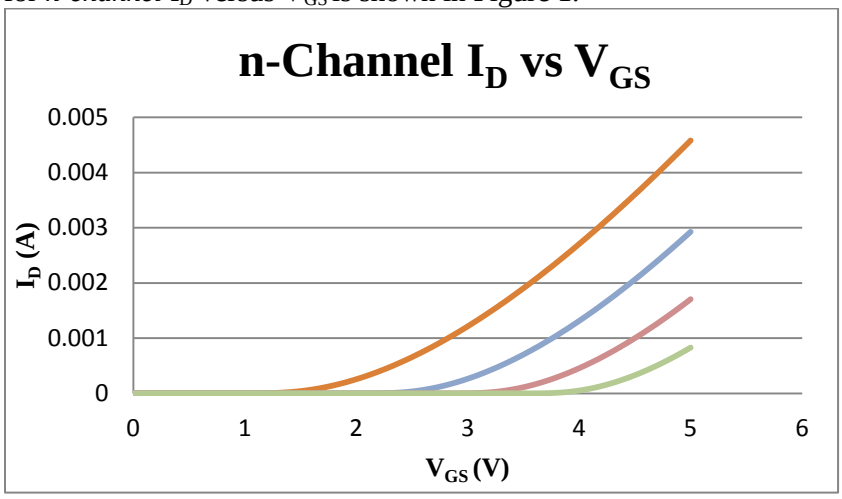

Figure 1: Gate sweep from 0 to 5V in 0.05V steps, Drain as 5v, Substrate as 0 to -3V in -1V steps

The plot for the determination for *n-channel* V_t and K is shown in Figure 2.

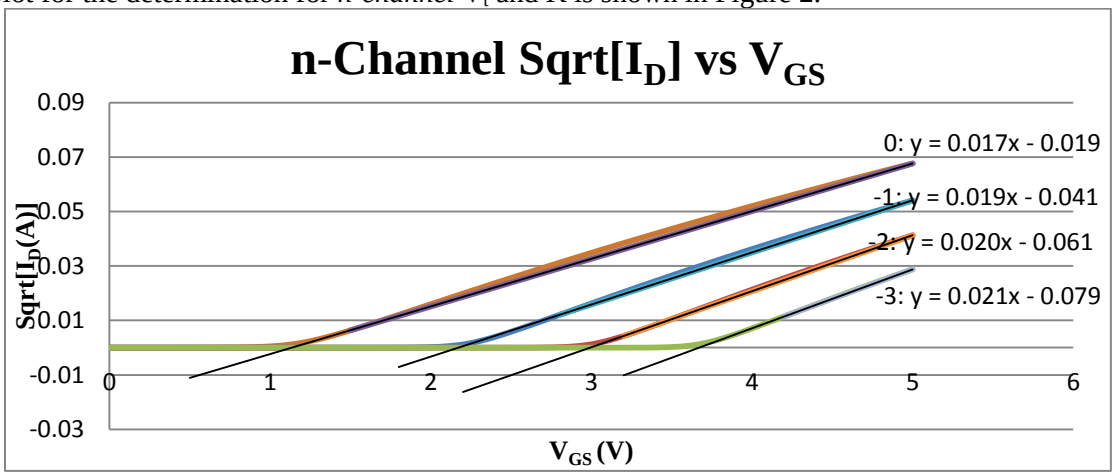

Figure 2: Gate sweep from 0 to 5V in 0.05V steps, Drain as 5v, Substrate as 0 to -3V in -1V steps

The original plot for *p-channel* I_D versus V_{GS} is shown in Figure 3.

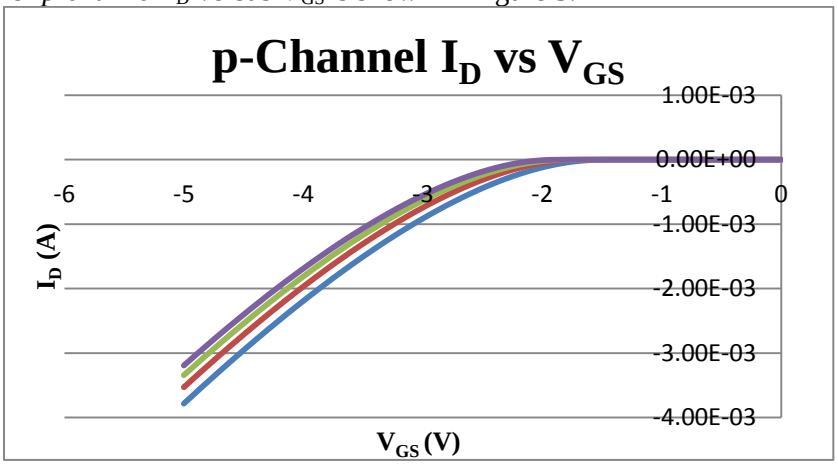

Figure 3: Gate sweep from 0 to -5V in 0.05V steps, Drain as -5v, Substrate as 0 to 3V in 1V steps

The plot for the determination for *p-channel* V_t and K is shown in Figure 4.

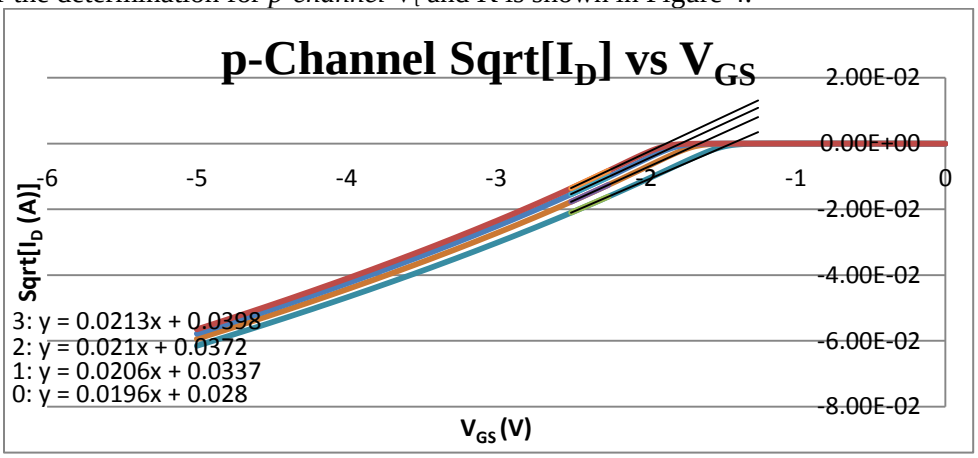

Figure 4: Squared I_D of the plot from Figure 3

Part 1.2: Measurement of the I_D versus V_{DS} for the determination of r_0

Figure 5 shows the plot of an n-channel MOSFET plotted by I_D versus V_{DS}.

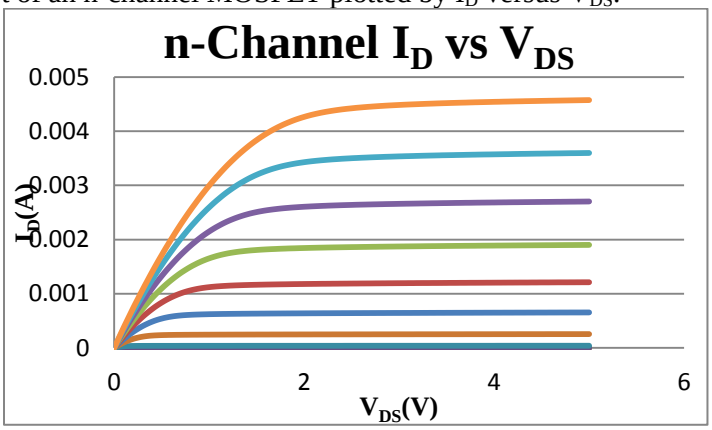

Figure 5: Drain from 0 to 5V in 0.05V steps, Gate as 0 to 5V in 0.5V steps

Figure 6 shows the plot of an n-channel MOSFET plotted by I_D versus V_{DS} that shows its early voltage (V_A) which in this case is -95.

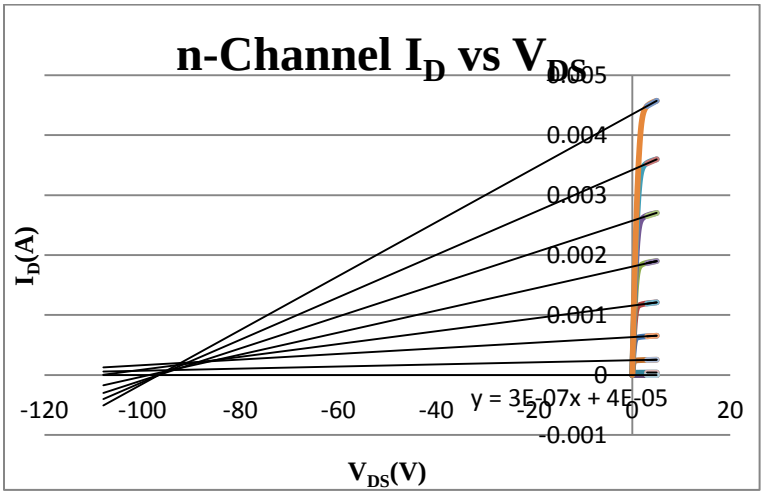

Figure 6: Finding the early voltage (V_A) of the plot from Figure 5

Figure 7 shows the plot of a p-channel MOSFET plotted by I_D versus V_{DS}.

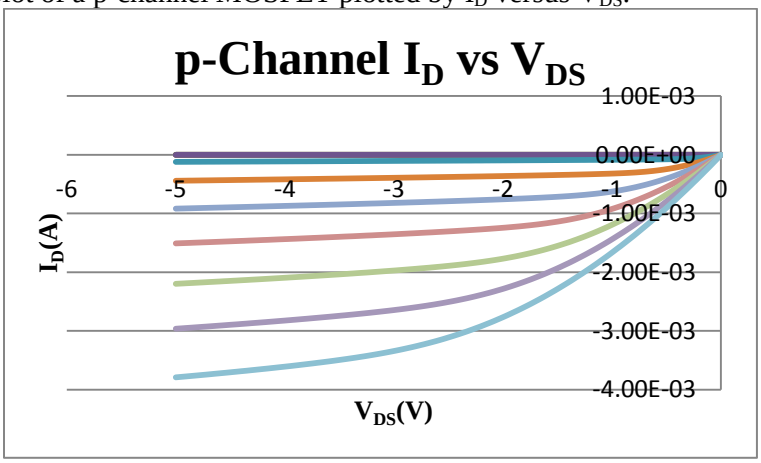

Figure 7: Drain from 0 to -5V in -0.05V steps, Gate as 0 to -5V in -0.5V steps

Figure 8 shows the plot of a p-channel MOSFET plotted by I_D versus V_{DS} that shows its early voltage (V_A) which in this case is 17.5.

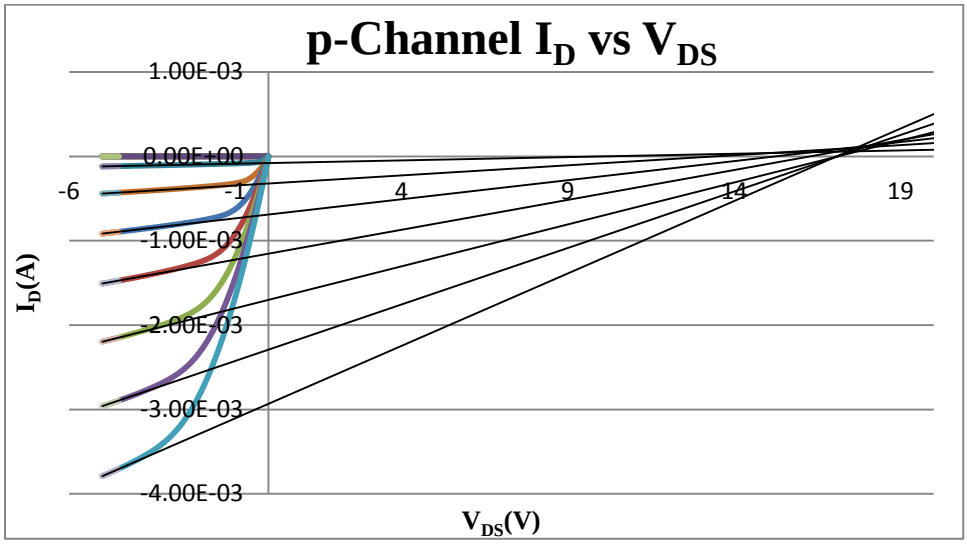

Figure 8: Finding the early voltage (V_A) of the plot from Figure 7

Part 2: Extraction of V_t and K from SPA data

The table (Figure 9) contains the V_T, K, and the V_A values of the n and p channel MOSFETs. We found the V_t for n and p channels from the x intercepts of each substrate in Figure 2 and Figure 4. We found the K from the slope*slope of each substrate in Figure 2 and Figure 4.

Substrate (±)	n-Channel (V_t)	p-Channel (V_t)	n-Channel (K)	p-Channel (K)
0	1.11765 V	-1.5 V	0.000289	0.000400
N=-1 ; P=1	2.15789 V	-1.61905 V	0.000361	0.000441
N=-2 ; P=2	3.05 V	-1.78947 V	0.000400	0.000361
N=-3 ; P=3	3.7619 V	-1.82353 V	0.000441	0.000289

Figure 9: Table of our values for V_t and K

Looking at Figure 9 we can see that for the n-channel, as the substrate voltage increases both the V_t and K increases. Then for the p-channel we can see that as the substrate decreases both the V_t and the K decreases.

Part 3: Determination of r_0

The formula for r_0 is

$$r_0 = V_A/I_D$$

From Figure 6 and 8 above we found our V_A for n and p channels. We figured out I_D from the formula

$$I_D = K*[V_{GS}-V_T]^2$$

$|V_{GS}|$ is given as 2.5V and we already have K and V_t from part 2 (using substrate 0). Therefore we can find r_0 as shown in Figure 10.

	n-Channel	p-Channel
V_A	-95 V	17.5 V
I_D	0.00055224765 A	00.64 A
r_0	172024.272 Ω	2734.375 Ω

Figure 10: Table of our values for r_0

Part 4: Experimental determination of V_t and K

When we measured our VDD we got 5.011V as shown below in Figure 11.

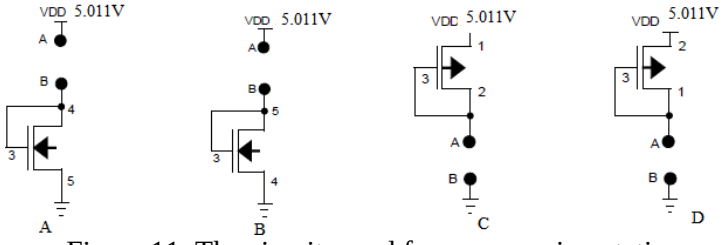

Figure 11: The circuits used for our experimentation

To find V_t we use the formula

$$V_t = V_{DD} - V_{GS}$$

We found V_{GS} from measuring A and B. Then we figured out I_D from when the 1K resistor is in parallel with the DMM as seen in Figure 12. Lastly we then figure out our K from the formula

$$I_D = K*[V_{GS}-V_T]^2$$

$$K = I_D/[V_{GS}-V_T]^2$$

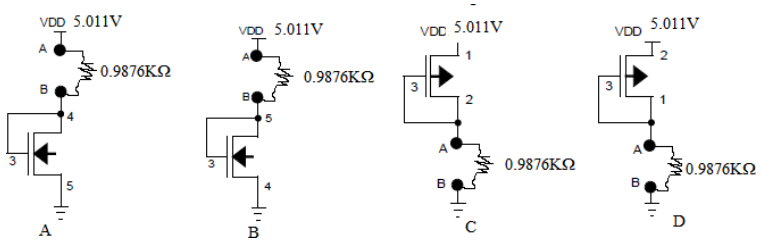

Figure 12: The circuits used for our experimentation paralleled with 1K resistor

Figure 13 is the table of values we got and includes our experimental V_t and K.

	n-Channel A	n-Channel B	p-Channel C	p-Channel D
V_{DD}	5.011 V	5.011 V	5.011 V	5.011 V
V_{GS}	4.117 V	4.1111 V	3.550 V	3.551 V
I_D	3.361 mA	3.3615 mA	3.5665 mA	3.5664 mA
V_t	0.894 V	0.9 V	-1.461 V	-1.46 V
K	0.000323	0.000326	0.000142	0.000142

Figure 13: Table of our values to find experimental V_t and K

Comparing our experimental V_t and K (Figure 13) and our SPA data V_t and K (Figure 9) we can see many differences. The Vt value for the n-Channel was a bit off 0.9 versus 1.1, but our Vt value for the p-Channel was almost exactly the same -1.461 versus -1.5. The K values on the other hand were also a bit off, for the n-Channel our experimental value was around 0.000323 versus the SPA's 0.000289 and then the p-Channel was really off as we got 0.000142 and the SPA got 0.000400. We attribute this error as that the MOSFET chip itself could be compromised or maybe we just measure the voltages wrong because it was always fluctuating on the DMM.

Part 5: Resistive Load common source NMOS amplifier

The circuit we used is shown in Figure 14.

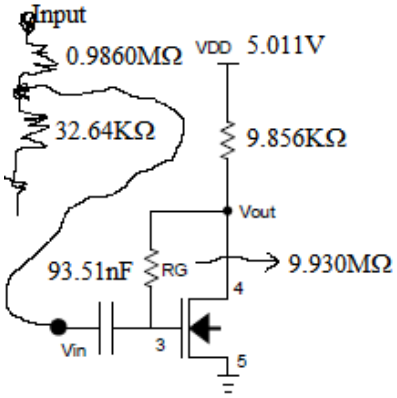

Figure 14: NMOS amplifier with a voltage divider and our exact values

From our measurements, we measured V_D = 2.0752V therefore V_{GS} = 2.0752V and V_t = 2.9358V, lastly we measured our dc I_D = 0.29787mA. To find K, again we use the formula

$$I_D = K*[V_{GS}-V_T]^2$$

$$K = I_D/[V_{GS}-V_T]^2$$

We already have all the values and our measure K for n-Channel in part 5 is K = 0.000402. From part 2 the SPA K was 0.000289 while from part 4 our experimental K was 0.000323. The K from part 5 seems to be even farther than our experimental K as compared to the SPA K from part 2.

Applying the small signal @ 1kHz as input we get from CH1 = 344mV and from CH2 = 2.04V, that is a **gain of 5.93**. Then as we increased the input signal to see the distortion, we found it at 8.68V input signal and the output pk-pk signal value was 3.10V as shown in Figure 15.

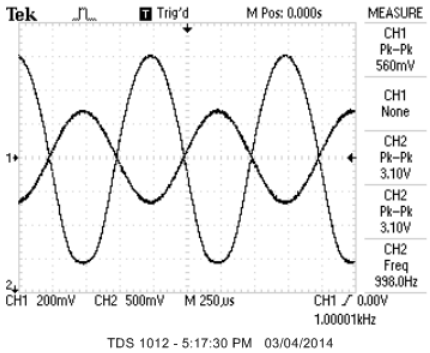

Figure 15: Distortion of the output @ 1kHz

We lowered the input back to 1.5V and swept the signal from 5Hz to 2MHz, our result is Figure 16.

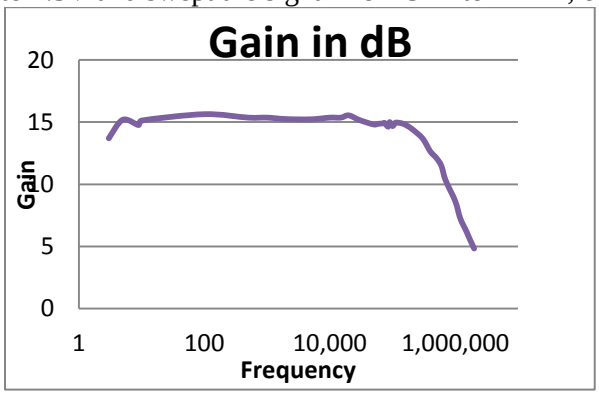

Figure 16: Plot of our gain on 1.5V pk-pk from 5Hz to 2MHz

Lastly our small signal model for our amplifier is shown in Figure 17.

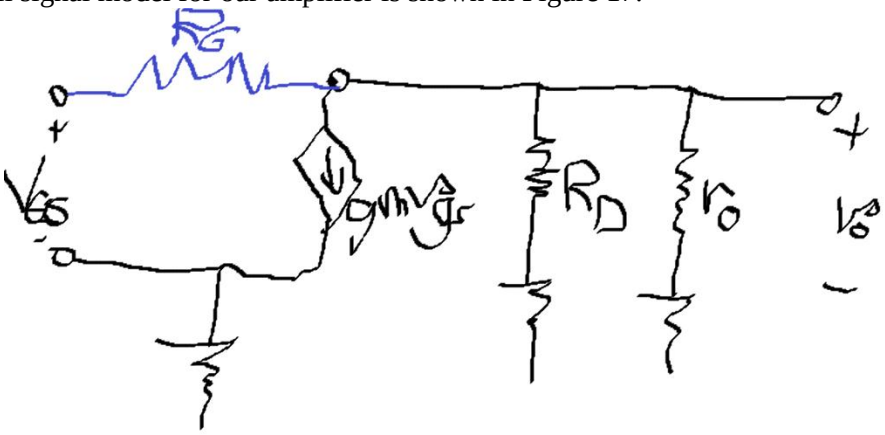

Figure 17: small signal model of CS NMOS amplifer

To find the gain, we first find gm

$$gm = K*(V_{GS}-V_t)$$

$$gm = (0.000402)(2.0752-2.9358)$$

$$gm = -0.345\ mA/V$$

Secondly we find $r_0$from the formula

$$r_0 = V_A/I_D$$

$$r_0 = (95)/(0.29787mA)$$

$$r_0 = 318.931K\Omega$$

Finally we have all the values to find gain

$$Gain = vo/vi$$

$$v_o = -gmv_i[r_0||R_D]$$

$$v_o/v_i = -gm[r_0||R_D]$$

$$v_o/v_i = -(-0.345\ mA/V)[(318.931K\Omega)||(9.856K\Omega)]$$

$$v_o/v_i = -(-0.345\ mA/V)[9560.548\Omega]$$

$$Gain = 3.298\ V/V$$

This experimental value of 3.298 gain was a bit off compared to our model gain value of 5.93 gain. We attribute the difference here to the fact that there were many calculations and measurements made and every miniscule error can get bigger and bigger as we keep calculating to find the Gain. For example our dc I_D might have been measured wrong. Even the measuring of our V_D could have been off, that would derail V_{GS}, V_t and overall the whole formula.