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Approval	Verification	Making
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Conformal-ECO use instructions

V14.20-s180

ルネサス システムデザイン株式会社

Rev. 0.00

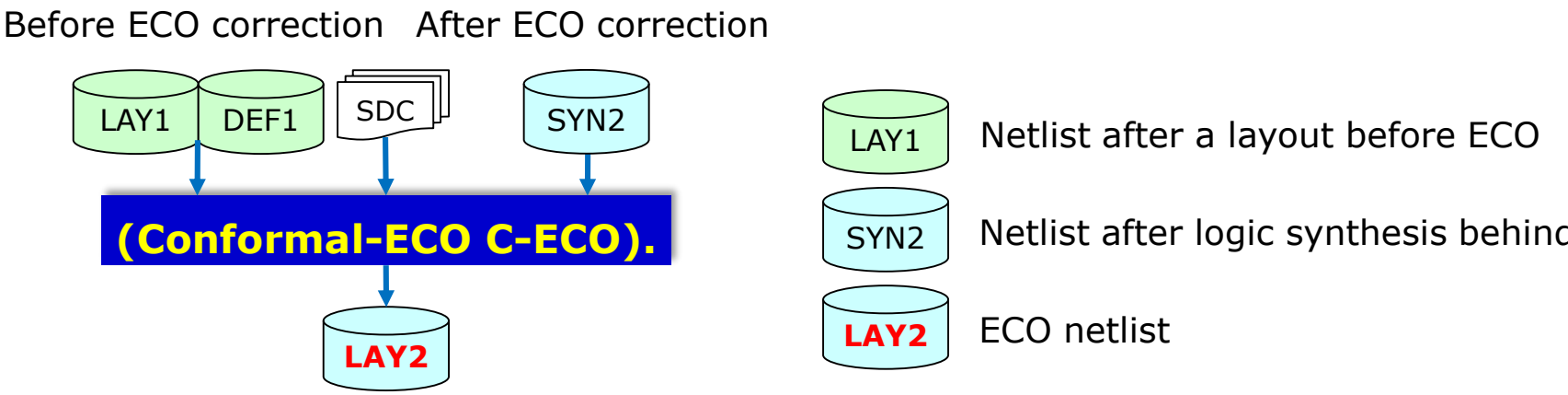
Contents

1.The outline

1-A) first.

- What is ECO
  - An abbreviation of Engineering Change Order.
  - It points at the work to which only the part of the design netlist is changed while keeping layout information on existence to the utmost with ECO.
  - In ECO, There is logic ECO with function change in the design and timing ECO with Function change isn't involved.

- Conformal - ECO is a logic ECO tool which corresponds to Pre-Mask and Post-Mask and automates conventional hand work.



1-B) support environment / 1-C) inquiry

- The support environment
  Please refer to below about the support version of Conformal ECO and RTL Compiler.

EDA-SITE/REL integrated tool information
http://eda.develop.renesas.com/cgi-bin/lv1ww/tools/cgi/to_sel_menuframe.cgi

Conformal : -> equivalent Verification-> Conformal - LEC The-> execution environment.
RTL Compiler : -> logic design and the Verification-> RTL - Compiler-> execution society.

※ A body note is the specification of Conformal LEC 14.20-s180 and RTL Compiler 11.10-s016.
It's indicated on a base.

- Inquiry
  - fv-support@lm.renesas.com

※ Please refer to 4-C) STEP3-1,3-2 for a environment configuration and initiation method.

1-D) related material

It's carried in REL integrated tool information on an EDA home page.

Logic design and Verification-> Equivalence, Verification-> Conformal - LEC [Manual]

	Documentary name	The documentary number
(1)	Encounter(R) Conformal(R) Equivalence Checking User Guide	It doesn't have that (Cadence material).
(2)	Encounter(R) Conformal(R) Equivalence Checking Reference Manual	It doesn't have that (Cadence material).

Logic design and Verification-> Equivalence, Verification-> Conformal - ECO [Related document

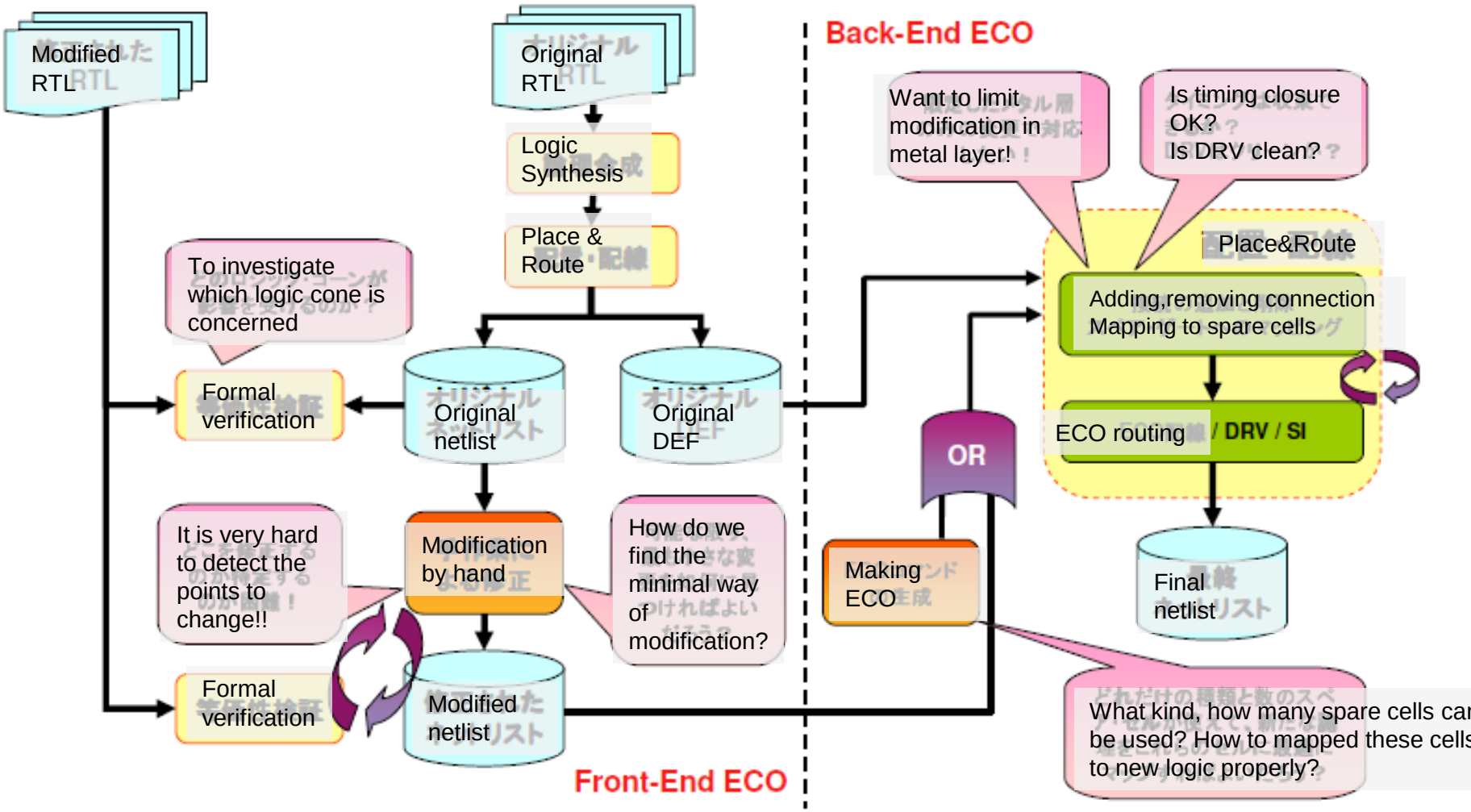
	Documentary name	The documentary number
(3)	Conformal-ECO starter guideline rev1.0	It doesn't have that (Cadence material).
(4)	Cadence company presentation material (ECO solution)	It doesn't have that (Cadence material).

1-E) the explanation of terminology and an abbreviation

Term/abbreviation	The meaning
ECO.	Abbreviation of Engineering Change Order
Logic ECO	The logic specification change/change performed to data after a layout design for a bug fix, work.
Pre-Mask ECO	Logic ECO before a mask making. It points at logic ECO which occurs to the P&R way.
Post-Mask ECO	Upper mask layer ECO. Without correcting lower mask layer, logic ECO is performed.
Spare gate Spare cell	It's used in Post-Mask ECO, the logic ECO cell prepared beforehand.

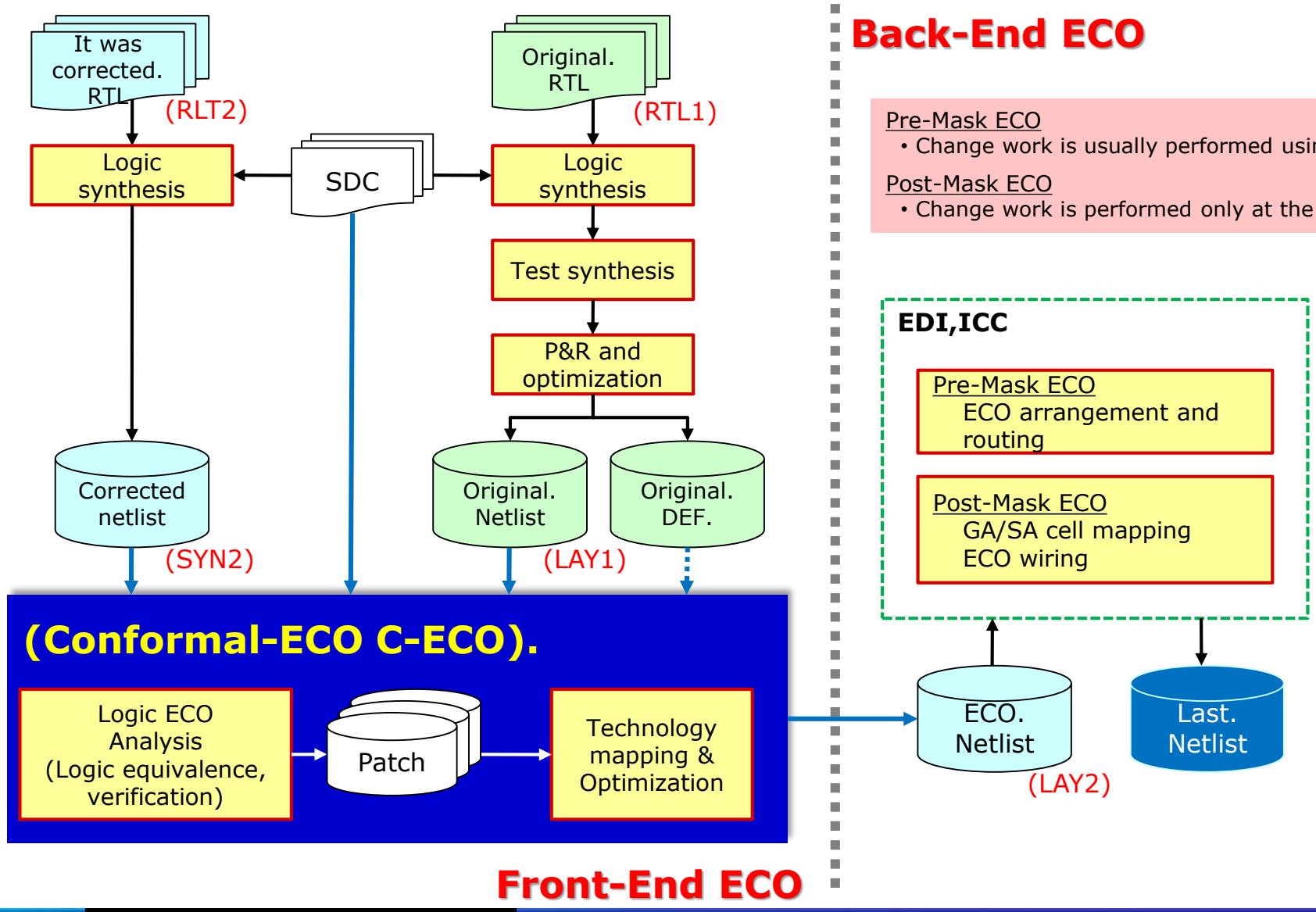
2.ECO flow

2-A) hand ECO flow

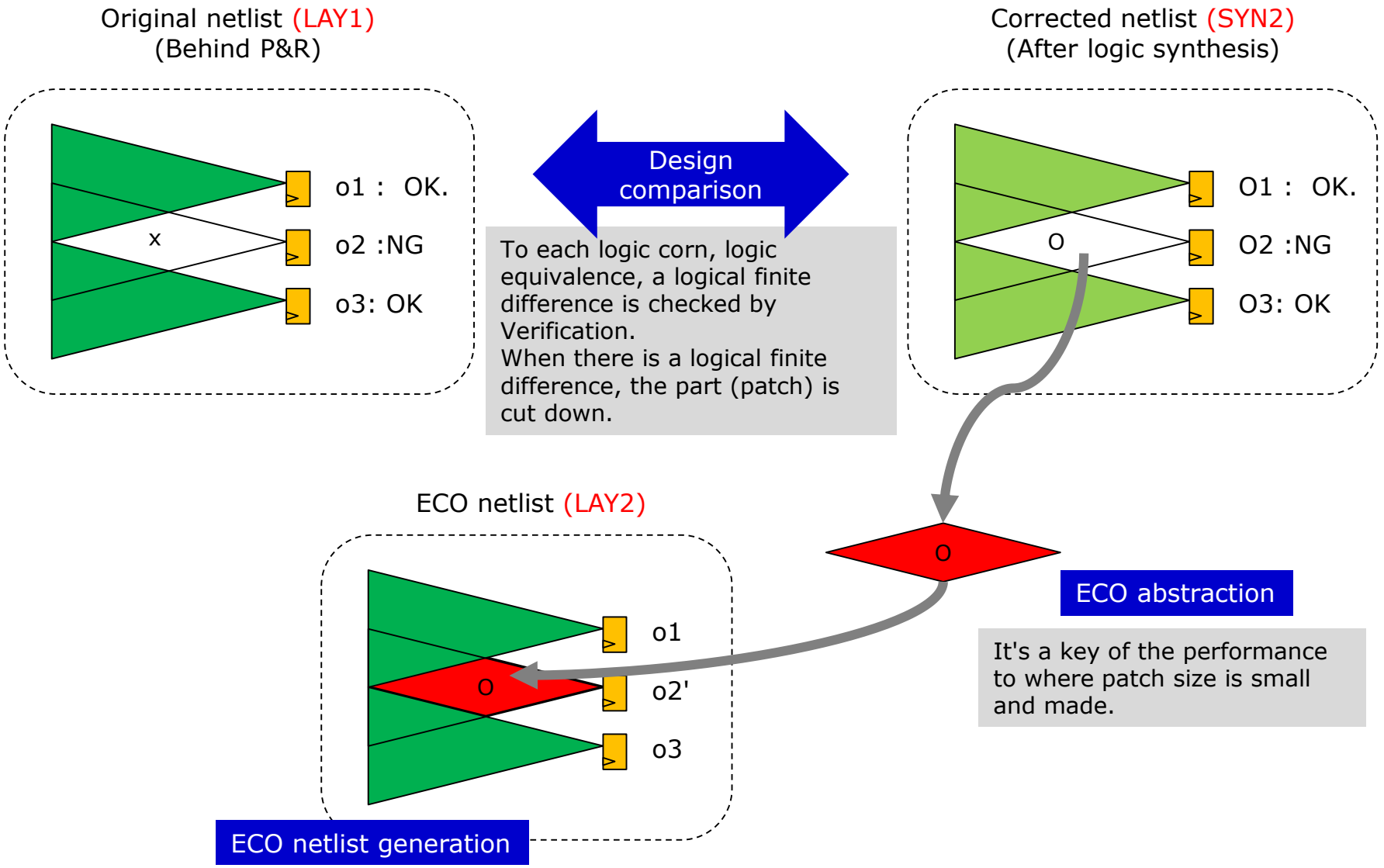


It quotes from Cadence material.

2-B) automatic logic ECO flow

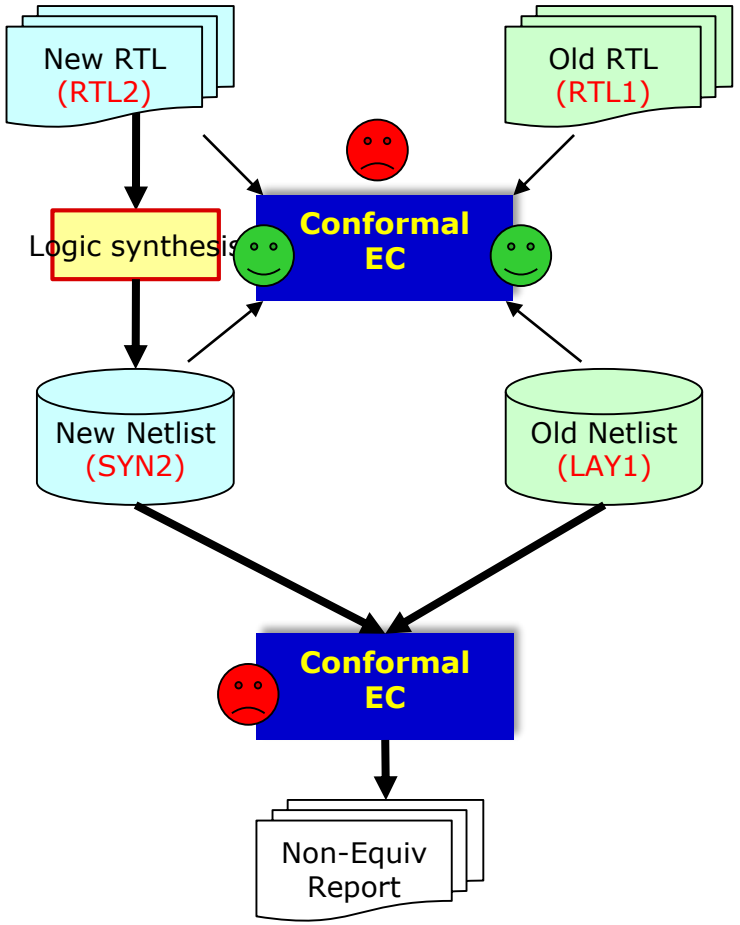


2-B) abstraction image of ECO logic



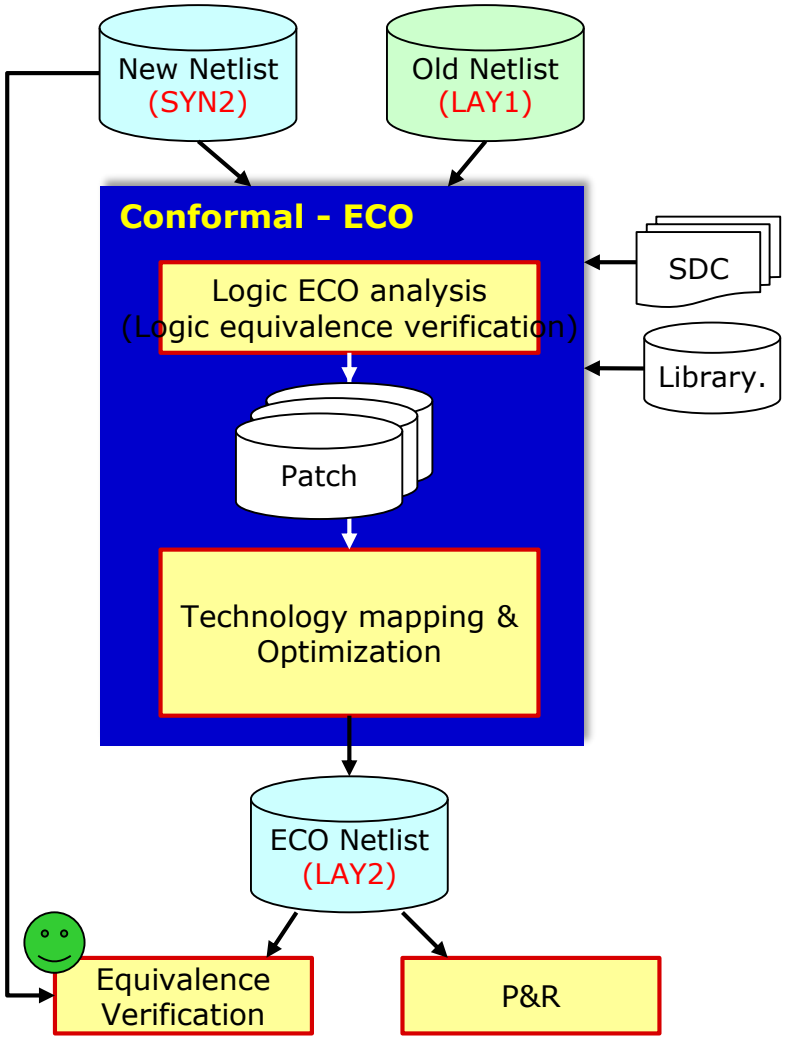
2-B) specification of ECO information (non-equivalent point)

- Comparison of an old RTL (RTL1) and old Netlist after a layout (LAY1)
  - It becomes equivalent.
    (The equivalence-lessness of the modeling dependence excludes a pseudo-error.)
- Record Netlist (SYN2) is made by logic synthesis.
  - To make them generate similar netlist structurally.
    The script used for logic synthesis of an old RTL is used.
- Comparison of a new RTL (RTL2) and record Netlist (SYN2)
  - It becomes equivalent.
- Comparison of an old RTL (RTL1) and a new RTL (RTL2)
  - It becomes non-equivalent.
  - It's equivalence-less for preparations of patch generation, a module and.
    Non-equivalent logic corn in module is specified.
- Comparison of old Netlist (LAY1) and record Netlist (SYN2)
  - It becomes non-equivalent.
  - "The equivalent point and the same evaluation point-lessness of RTL1 vs. the RTL2".
    It becomes equivalent.



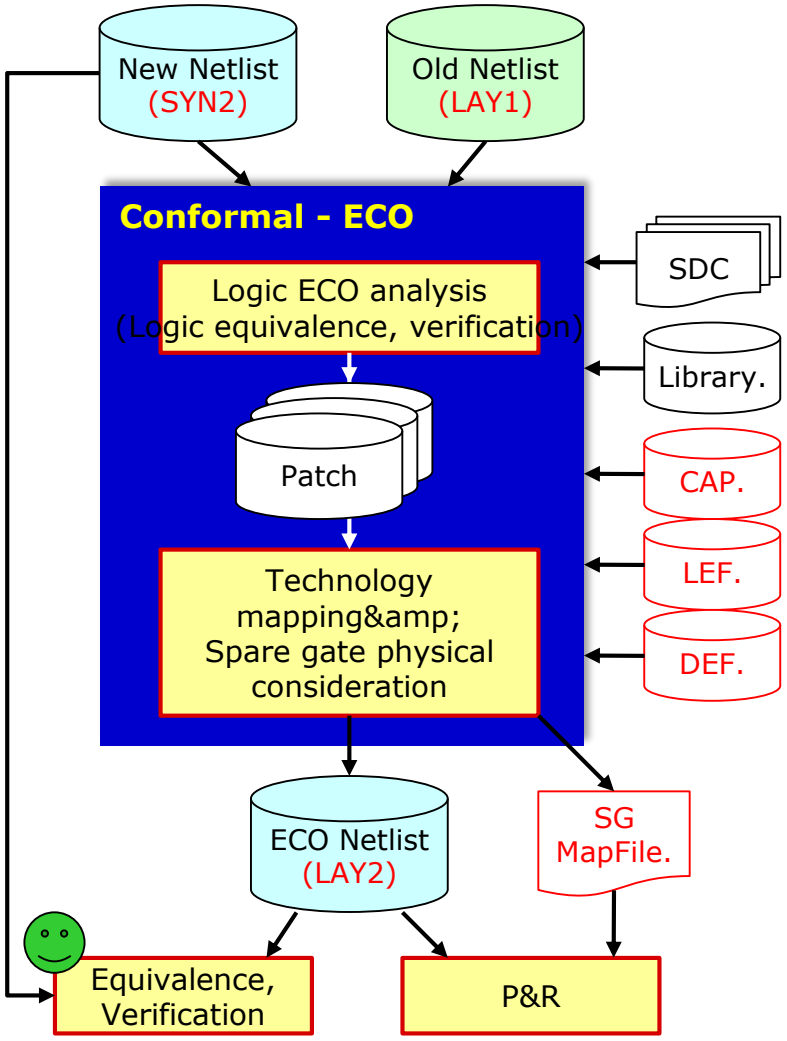
2-B) Pre-Mask ECO processing flow

- ECO patch generation
  - ECO logic abstraction between SYN2,LAY1
  - A scan chain is maintained.
  - The clock gating structure is maintained.
- Technology mapping and optimization
  - ECO logic optimization
  - ECO logic in a technology library mapping
- ECO netlist generation
  - ECO netlist (LAY2) output
- ECO netlist Verification
  - SYN2 vs. LAY2 Equivalence Verification execution



2-B) Post-Mask ECO processing flow

- The following procedure as well as a procedure of Pre-Mask ECO are needed.
  (It's achieved with a target at the spare gate.)
- Of the following information abstraction, it saves and needs DEF.
  - The type of the spare cell and the number of instances
  - Physical information on a spare cell
- Additionally the next data is needed.
  - LEF, CapTable
- The nexts are processed as well as a technology mapping.
  - The one to a spare and a feed gate of ECO logic Mapping
  - Physical arrangement consideration at the spare gate
  - Report of the insufficient spare cell resource
- When starting,**-ECOGXL option is** needed.



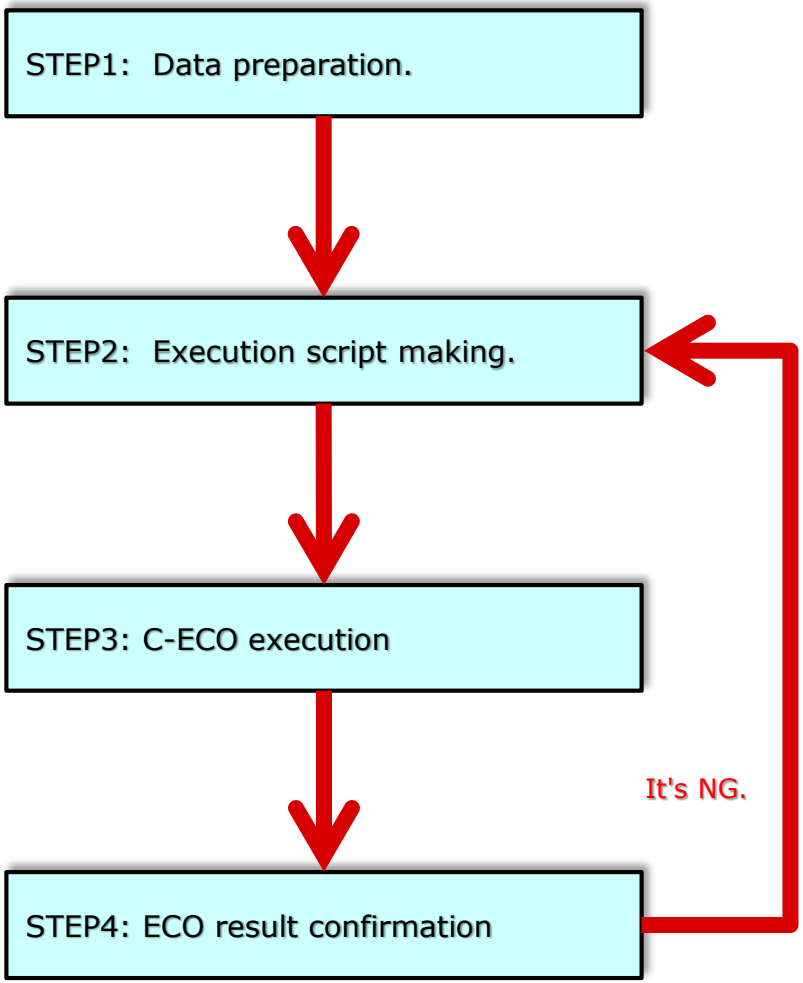
3.Careful point

3.Careful point

1. When starting,-ecogxl option is needed.
   A license Renesas possesses arranges for it and, please be sure to start in-ecogxl.
2. Before putting ECO into effect, be Conformal LEC and please confirm the logic equivalence of a net and a layout net (LAY1) after synthesis before ECO.
   Please use the terminal configulation used in the case in Conformal ECO.
3. Please be sure to confirm that a DFT circuit isn't broken in DFTCheck after ECO implementation.
   Even if a DFT circuit is corrected, it can't be detected because the logic is being confirmed only in User Mode in Conformal ECO.
4. Please confirm whether ECO of a clock line exists before ECO implementation.
   When the Enable logic of a clock is changed even when there is no correction by which a clock is itself.
   A clock line will be sometimes change.

4.Execution procedure

4.Conformal-ECO execution procedure



STEP1

- It's explained about necessary data information to execute Conformal - ECO.

STEP2

- It's explained about a script of Conformal - ECO (dofile).

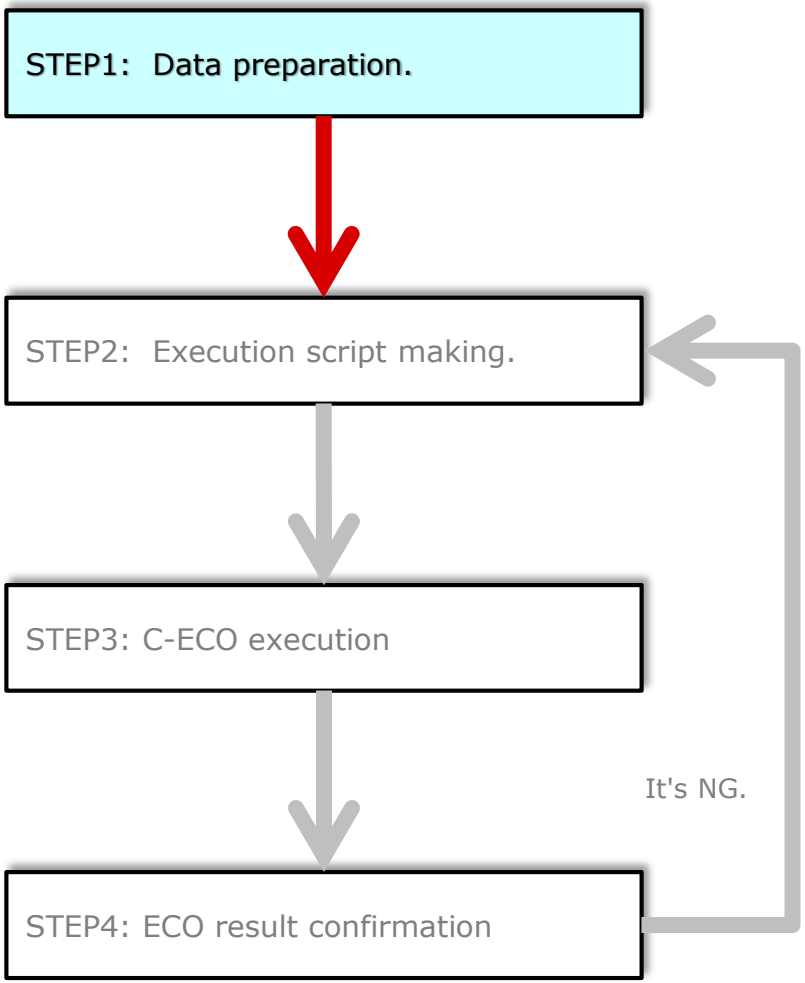
STEP3

- It's explained about an execution method of Conformal - ECO.

STEP4

- It's explained about confirmation method of Conformal-ECO execution log and Verification method to an output.

4-A) STEP1: Data preparation.



- **Confirmation of pros and cons corresponding to STEP1-1:**
  - The information to judge the adaptation propriety of Conformal - ECO is described.
- **STEP1-2: Necessary data authentication.**
  - The data it needs by Conformal-ECO execution is described.
- **STEP1-3: Preliminary execution confirmation.**
  - The necessary contents are described as preliminary preparations before Conformal-ECO execution.

4-A) confirmation for and against corresponding to STEP1-1:

- The case to which Conformal - ECO can't answer is as follows.
  For details, please see [related document (3)- ECO starter guideline].
  - The logic change which involved a retiming register
    - But, in the same case, the retiming number of done registers and a register name are prepared.
  - Scan chain of an additional register/test signal connection
    - The cashier who added it doesn't include in a scan chain.
    - When a mapping made the cashier who added it spare F/F, it's a scan chain/test signal.

    Even if it's connected already, it's eliminated.It can't be maintained by the current state.

    ※ The case and the existence scan chain in which the cashier who eliminates by ECO or grinds a mapping exists?

    It's maintained.
  - ECO in an abortion occurrence block
    - When an Verification point including ECO logic (logic corn) aborts, Conformal - ECO can't be carried out.

    ※ Further when ECO logic is unrelated to abortion corn, and it's possible to cut off and think. It can be carried out by removing an abortion point from an Verification target.
  - ECO which straddled the power domain (with CPF)

4-A) confirmation for and against corresponding to STEP1-1: (Cont.)

- It can correspond to various logic ECO, but Conformal - ECO needs attention by the following ECO change.
  For details, please see [related document (3)- ECO starter guideline].
  - Addition/correction of a clock gating cell
    - Such as connecting a clock gating cell and a register directly, a clock line of existence isn't maintained.
    - The case when the Enable logic of a clock to a certain register is changed, like.
  - Addition of a reset line/correction
    - A control logic on the reset line (logic fixing at the time of a DFT) isn't maintained.
  - The logic correction before and behind the DFT circuit by which it's for BIST
    - A patch file including the DFT circuit which should be maintained is generated.

4-A) STEP1-2: Necessary data.

The item	Detailed.	Indispensable.
RTL	Old RTL	O
	New RTL	O
Netlist	Old netlist behind P&R	◎
	New netlist after synthesis	◎
Library	Liberty library for RTL Compiler	◎
	Library for Conformal - LEC (Liberty recommendation)	
The design restrictions	DFT execution script for LEC including doing naming rules of the restrictions	O
ECO information	The module name ECO generated	O
	It comes near to ECO and adds it/eliminated port name	O
	The port name to which the name was changed by ECO	
	It comes near to ECO and adds it/it's changed/eliminated register name	
Physical. It's used in Post-Mask ECO.	Old DEF file after a layout	◎
	The physical library where it's for technology and layer information	◎
	The CapTable file as which the pin capacity was defined	
	The spare cell name which permits the specification	◎

◎:Mandatory O:Recomended(iteration may be occur without this information)

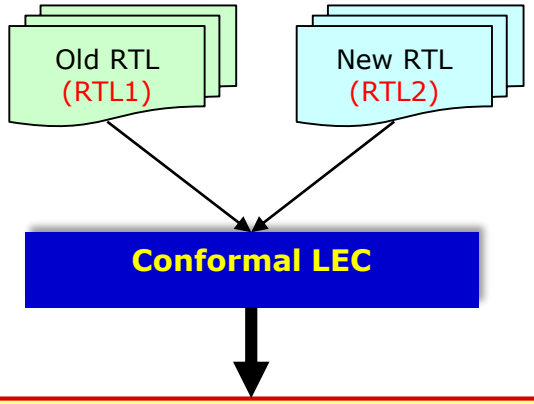
4-A) STEP1-2: Necessary data (Cont.)

- Addition matter of ECO information
  - Even if there are a module name of ECO vs. an elephant and an addition/no ECO reports of elimination port name in case of hierarchy Verification, Conformal - ECO can be carried out.But there is a possibility that iteration which carries out and makes them acquire information several times brings and advances ECO processing by wrong information.
    Therefore it's recommended to check ECO targets information beforehand.
  - When boundary optimization isn't performed when there is no information on a ECO module in case of hierarchy Verification, the next setting is also possible.
    add module attribute * -eco_module -both --noflatten
  - When using flat Verification, the configulation above-mentioned is unnecessary, but please be sure to confirm the validity of ECO target module and the addition/elimination port for execution log.

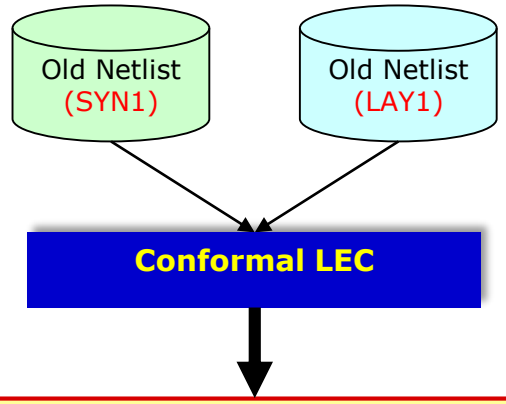
4-A) STEP1-3: Preliminary execution.

- It's necessary to give information appropriate to Conformal - ECO to avoid increase in the ECO processing time and increase of a patch file.
  Please check the contents which should be established using Conformal - LEC (equivalence, verification).

It's compared between the RTL nets before and behind ECO. A layout result is compared with a synthetic result befor



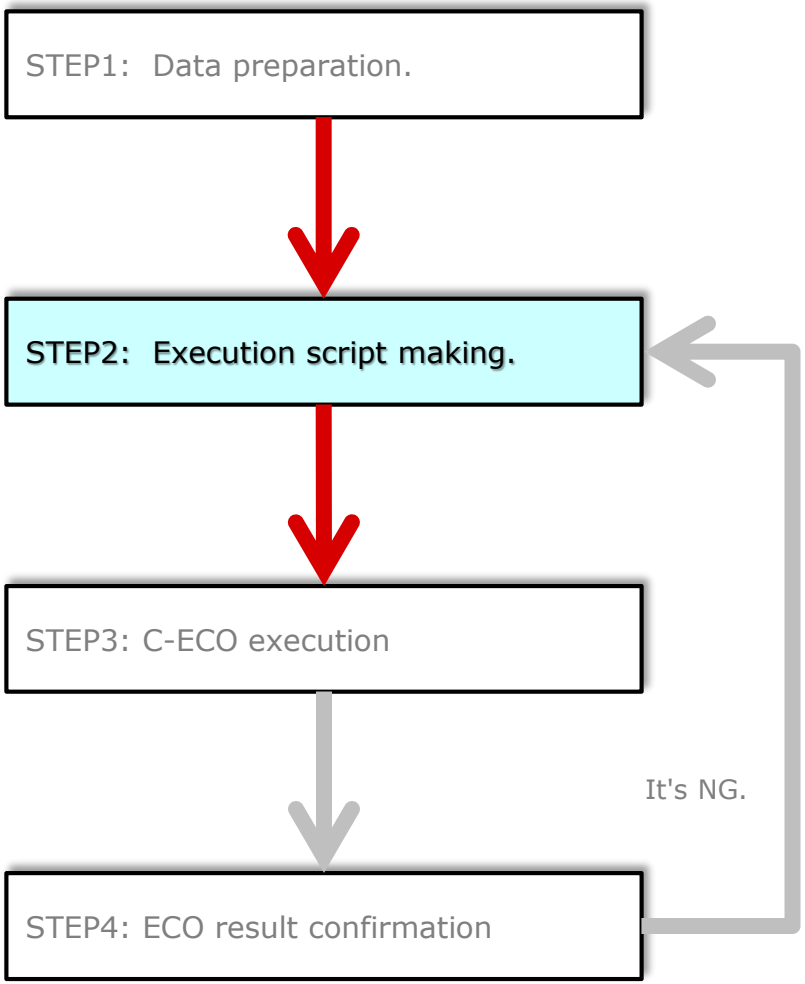
- ECO module name
  - ✓ The number with which it discords and point
- ECO addition/elimination pin



- The design restrictions
  - ✓ add pin constraint
  - ✓ add renaming rule
  - ✓ .

  (disable configulation of a DFT, indispensable)

4-B) STEP2: Execution script making.



- **STEP2-1: Model script acquisition.**
  - Acquisition method of a model script is described.
- **STEP2-1: Script edit.**
  - A processing flow of a sample script is explained.

4-B) STEP2-1: Model script acquisition.

- Procurement source of a model script

  - EDA home page (http://eda.develop.renesas.com/lv0/tools/)

REL integration EDA tool information

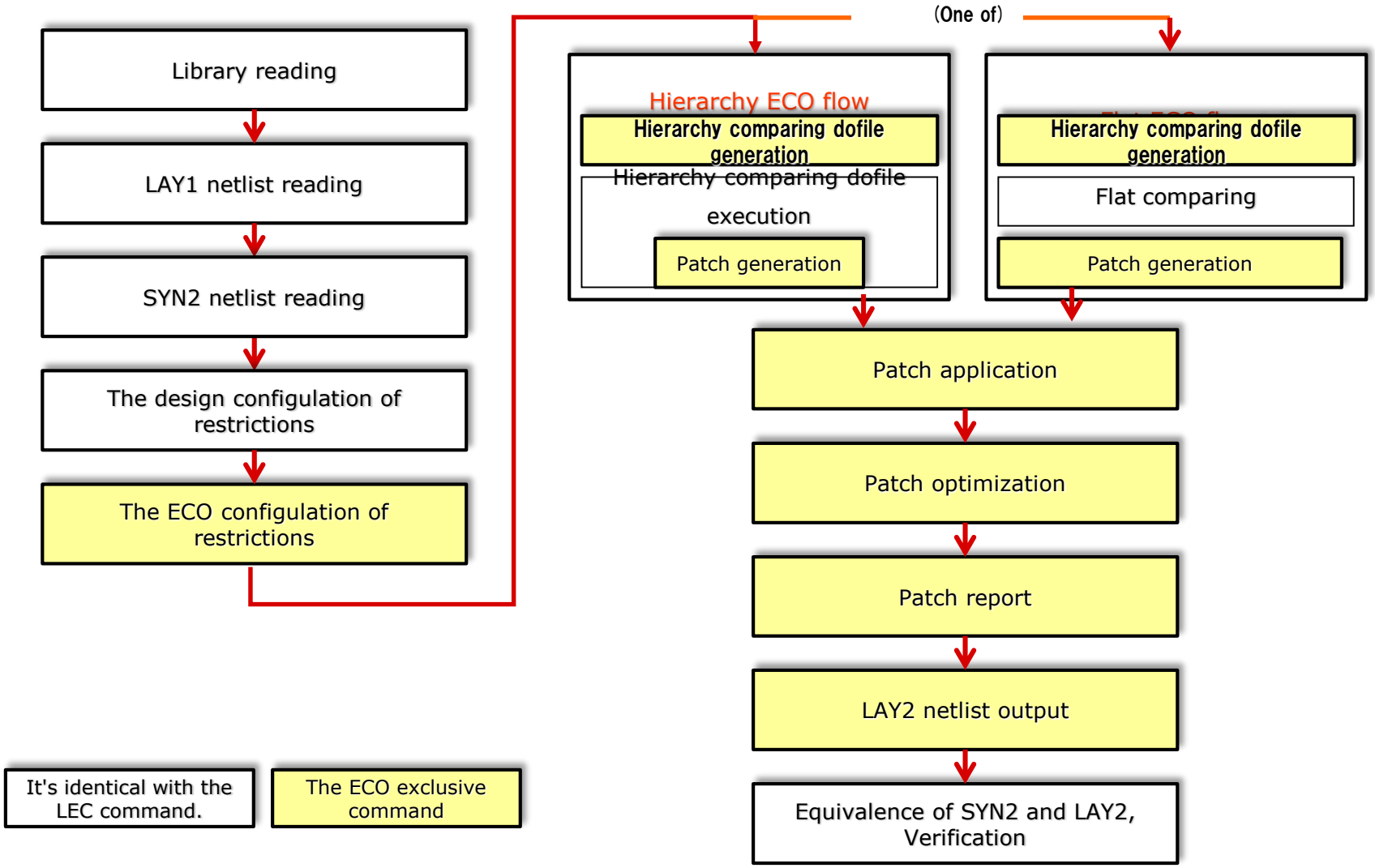
–Logic design and Verification

-Equivalent Verification-> Conformal - ECO [Release information]

Appear on the above, and please download and use a recommendation script.
Detail description of a script is the model which is being uploaded in an identical part.
Please check the script manual (.pdf).

4-B) STEP2-2: Conformal-ECO script flow

- A flow of an execution script of Conformal - ECO.



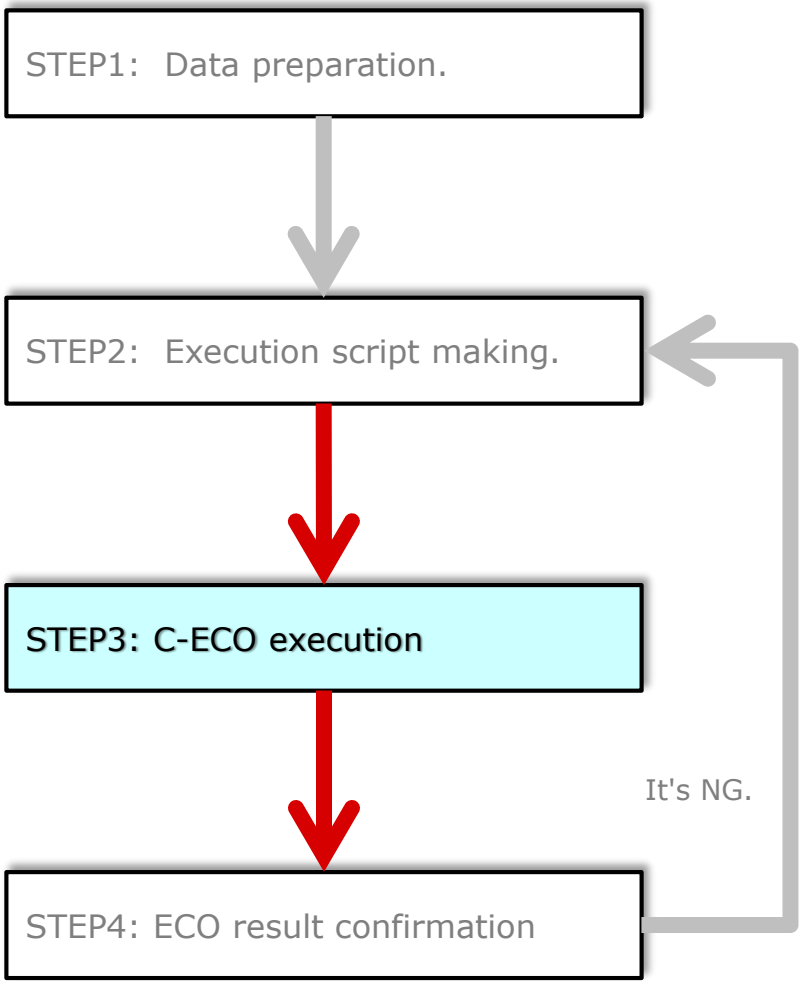
4-B) STEP2-2: Script edit.

- By establishing several required item in the header in the model script. It's possible to execute.

  - Required item
    - ECO module name (hierarchy ECO flow)
    - Netlist of LAY1 and SYN2
    - Liberty library
    - DEF, LEF, CapTable and spare cell (Post-Mask ECO)
  - The option item
    - SDC file
    - Flow configulation

- Details of configulation see the model script manual indicated in p.26, please.

4-C) STEP3: Conformal-ECO execution



- **STEP3-1: Environment configuration.**
  - The environment configuration it needs by C-ECO execution is described.
- **STEP3-2: Execution.**
  - An execution method of C - ECO is described.

4-C) STEP3-1,3-2

- STEP3-1: Environment configuration.
  - Conformal - ECO and a RTL- pass configulation of Compiler are performed.

```
setenv CDN_CFML_ROOT /common/appl/Cadence/conformal/14.20-s180
setenv CDN_SYNTH_ROOT /common/appl/Cadence/rtlcompiler/11.10-s016
set path = ($CDN_CFML_ROOT/bin $CDN_SYNTH_ROOT/bin $path)
```

    - To execute RTL-Compiler automatically inside Conformal - ECO. It needs pass configulation.

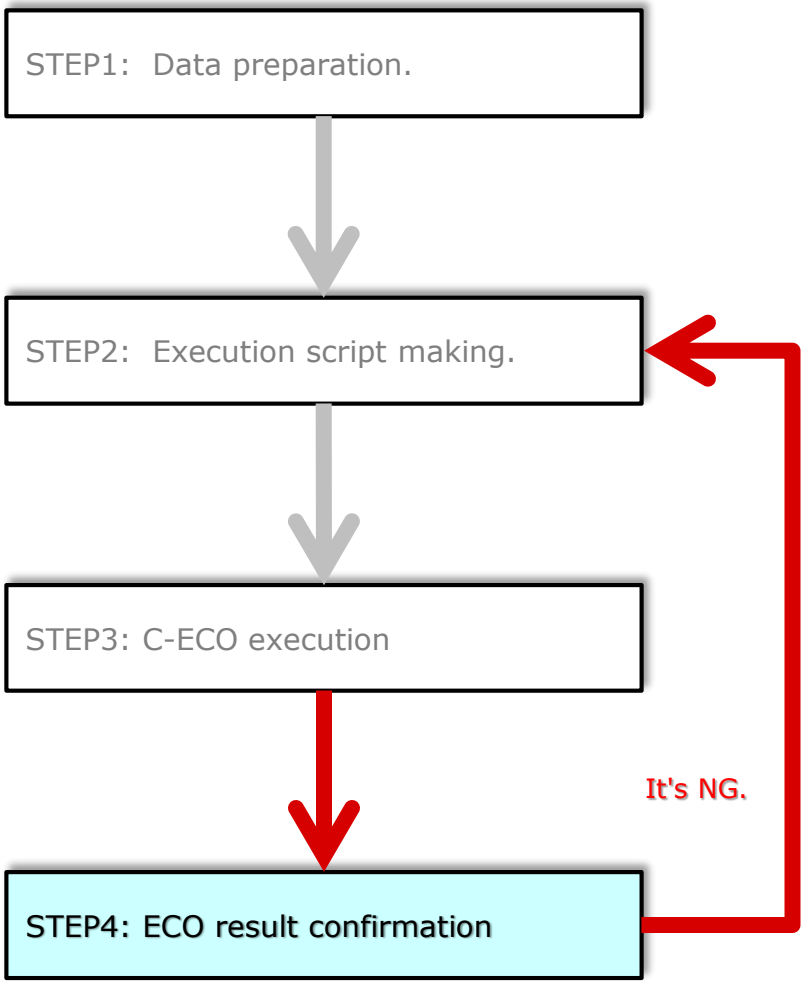
- STEP3-2: Conformal-ECO execution (in start default, 64bit edition object)
  - Pre-Mask ECO

    % lec -64 -ecogxl -nogui -dofile< execution script>

  - Post-Mask ECO

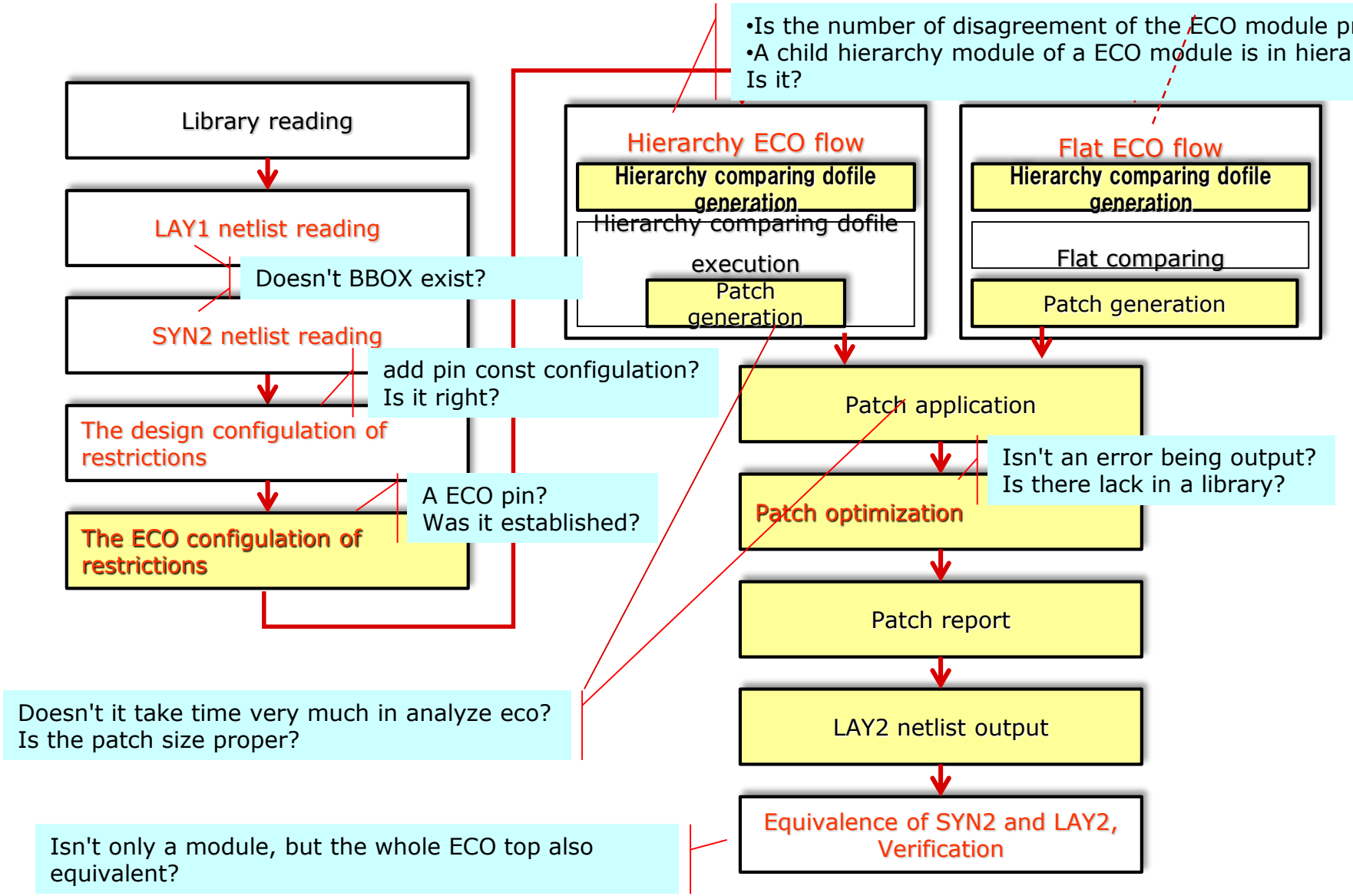
    % lec -64 -ecogxl -nogui -dofile< execution script>

4-D) STEP4: ECO result confirmation



- STEP4-1: Progress confirmation.
  - A confirmation matter of execution log is described.
- STEP4-2: The final result confirmation.
  - C-ECO success or failure judgment method is described.
- STEP4-3: Subsequent treatment Verification.
  - Necessary Verification method is described to an output.

4-D) STEP4-1: Progress confirmation.



4-D) STEP4-2: The final result confirmation.

- Equivalence of SYN2 and LAY2, please check the verification result.
  Verification result is output at the end of a logfile.
  - In case of hierarchy comparing
    Hierarchical compare : Equivalent
    Hierarchical compare : Non-equivalent
    Hierarchical compare : Inconclusive
    ↑ When Abort and Not - compared exist.
  - In case of top whole comparing
    At the end of a logfile.
    Equivalent, Non-equivalent, Abort, Not-compared
    ↑.
    "compare -noneq_stop 1"
    "add module attribute -compare_effort none"
    And so on is designated.

(※) Equivalence of SYN2 and LAY2, at the time of Verification.
Please be careful so as not to establish the following option related to ECO.
set flatten model -eco
remove - ignore_mismatch_ports

4-D) STEP4-3: Post treatment Verification.

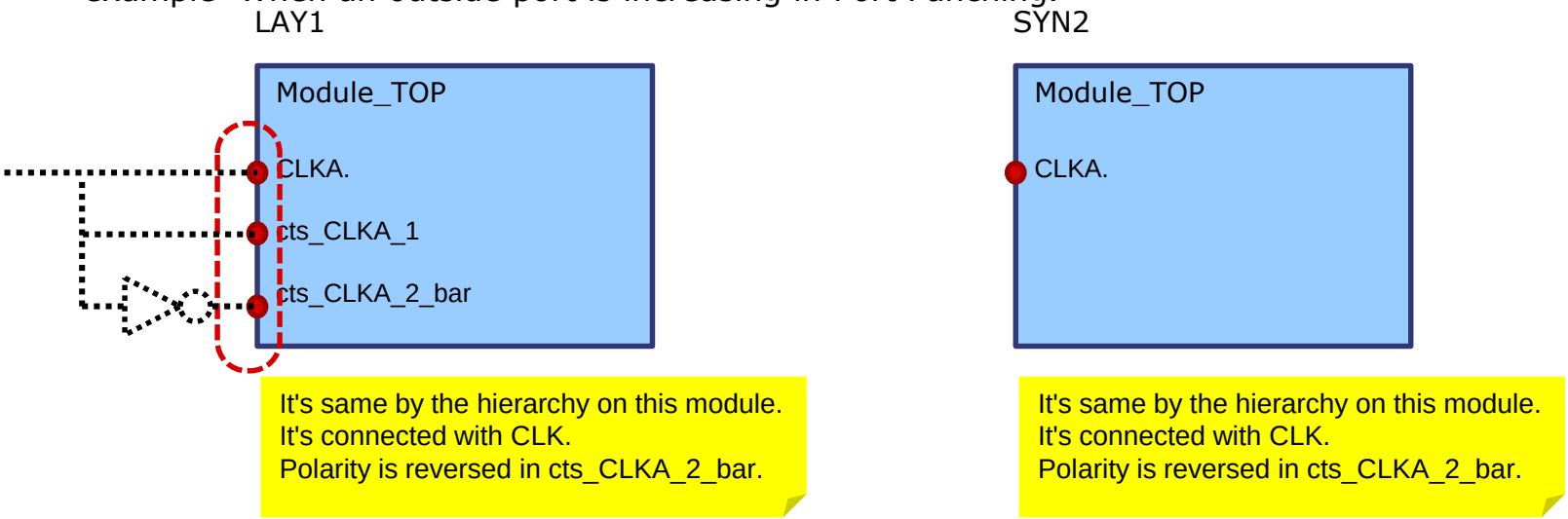
- Then the ECO netlist Verification confirmed in STEP4-2 (equivalence of SYN2 and LAY2, verification) is confirming the logical equivalence.But it's necessary to inspect as subsequent treatment because it isn't inspecting by the angle as the operation guaranteed.
  - Design rule check of netlist (DRC)
    - Please confirm that a design agreement is satisfied.
  - Clock linear trace
    - Please confirm that the clock line isn't changed.
  - Scan chain trace
    - Please confirm that a scan chain can be traced.
  - Timing check
    - Please confirm that timing isn't aggravated.
  - Additionally equivalence, confirmation in the part where a disable was done by Verification
- An Verification point is also explained by [related material (3)-Conformal-ECO starter guideline], so please check it.

Appendix The know-how collection.

A port outside LAY1 and SYN2 is put together (1/3).

When making one below some specific hierarchies (soft macro) the subject of Confomrmal ECO, LAY2 is of LAY1/SYN2 by influence of influence of a layout (Port Panching and optimization).
An outside port doesn't sometimes match.The restrictions according to the circumstances are added in that case.

< example When an outside port is increasing in Port Panching.>



CLKA in // golden (LAY1) and cts_CLKA_1 are the same logic.CLKA and cts_CLKA_2_bar are reversed logic.

vpx add pin equivalence CLKA cts_CLKA_1 --inv cts_CLKA_2_bar -golden

A port outside LAY1 and SYN2 is put together (2/3).

< example When logic is reversed, there is correction of port name.>

Inverter is just before Triple A by the dominance hierarchy.
A terminal name is different in AAA_bar.

It turns over, and the logic of Triple A of // revised (SYN2) is made AAA_bar.
set naming rule - Inverted_pin_extension_bar
add renaming rule rem_pi_1 AAA AAA_bar -type pi -revised

A port outside LAY1 and SYN2 is put together (3/3).

< example When logic is reversed, port name is same.>

Inverter is just before Triple A by the dominance hierarchy, but a terminal name is a condition of Triple A.

Please answer with the following way because there are no ways to answer to Conformal with 1 command.

1. root makes the script made a reversed mapping (remap.do) in case of Module_TOP.

```
if { [get_root_module]  == "Module_TOP"}  {
vpx delete mapped point AAA -golden
vpx add mapped point AAA AAA -invert
}.
```

2. A made script is added to the sample script.
   - After it's vpx set system mode lec (It has 3 points.)

     ```
     vpx set system mode lec
     dofile remap.do
     ```

   - It's designated by-prepend_string option in analyze hier_compare.

     ```
     vpx analyze hier_compare -dofile $ {OUTPUT_DIR}/hier. do -eco_aware \
     -replace -constraint -noexact -usage \
     -prepend_string \"dofile remap.do\"\
     -input_output_pin_equivalence -function_pin_mapping -threshold 0 -verbose
     ```

The cell used in ECO is limited.

- The cell used in ECO is limited.
  It's set as a variable of a sample script "ONLY_USE_CELLS".

- The cell which isn't used in ECO is designated.
  It's designated in--avoid in optimize patch.

  < example>
  "set AVOID_CELLS *X1 *X2".

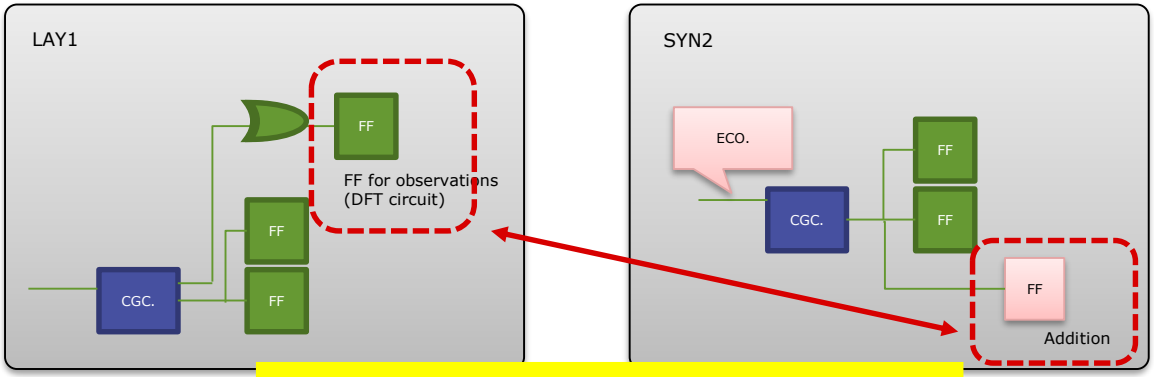
  vpx optimize patch -workdir {OUTPUT_DIR}/OPTIMIZE_PATH \
  -prelibscript $ {OUTPUT_DIR}/search_path. tcl \
  -presynscript $ {OUTPUT_DIR}/presyn. tcl \
  -library $ {LIBRARY_FILES} -nousetiecell \
  -instancenaming \"ECOinst_%d\"-netnaming \"ECOnet_%d\"\
  -sequentialnaming \"ECOreg_%s\"\
  -avoid $ {AVOID_CELLS}

The way to make a test point of a DFT non-applicable

Logic equivalence before ECO, a test point for DFTs which exist in LAY1 (control/observation, FF) is Unmapped and isn't made the target of ECO by Verification.

But a test point of LAY1 and an additional FF of SYN2 make the mapping SYN2 in the case when a FF was added, and logic related to a test point is sometimes corrected.
It can be excluded from a target of ECO by fixing input of a test point as follows in that case.

add primary input AAA/BBB/TP_REG/D
add pin constraint 0 AAA/BBB/TP_REG/D



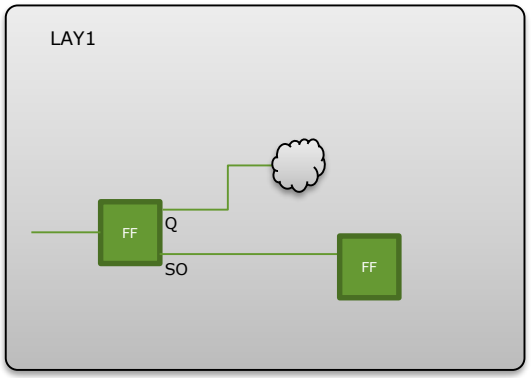
Logic equivalence, a mapping is done by Verification.
It's ECO vs. an elephant.

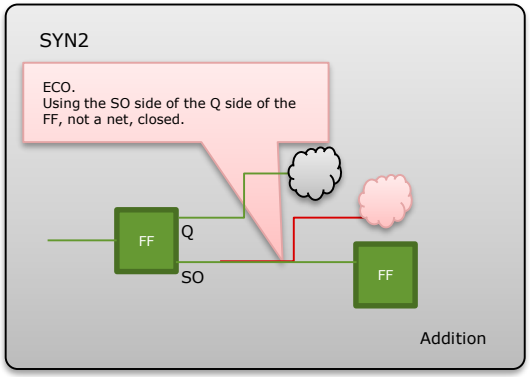
The corrective action when closing using a SO terminal for a FF

A scan chain isn't corrected by usually fixing scan Enable signal.
In the case when Q of a FF and SO output are identical logic, using SO output, ECO is sometimes put into effect.

It can be avoided by making the SO output treatment as external input and fixing 0 as follows in that case.
But, it's the previous hand that scan chains aren't ECO vs. an elephant.Please confirm that there are no problems with a DFT circuit behind ECO in DFTCheck.

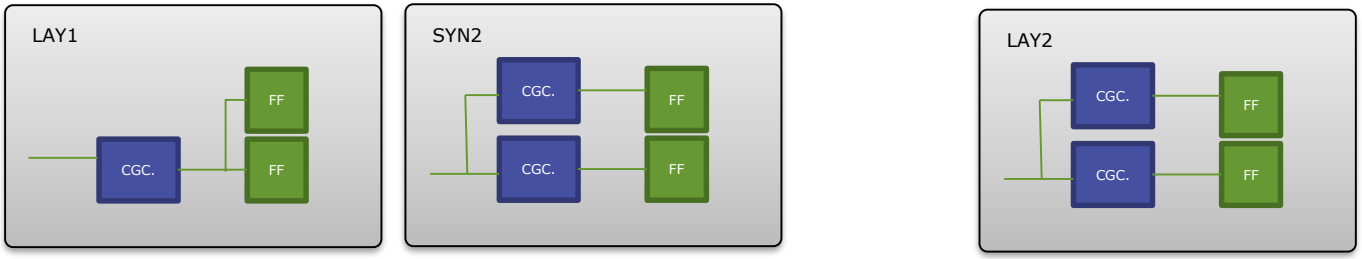
vpx add primary input *_reg/SO -pin -both
vpx add pin const 0 *_reg/SO -both



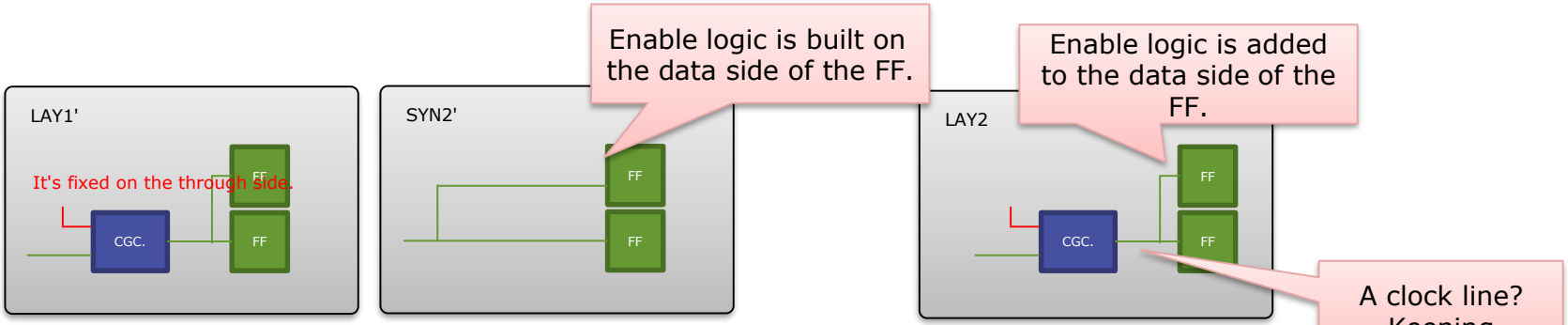


Without correcting a clock line, the structure of the clock gating cell (CGC) is corrected.

- When the structure of CGC is different in LAY1,SYN2, Conformal ECO adds CGC newly.
  -> A clock line is corrected.



- By fixing Enable of a CGC cell of LAY1 on the through side and synthesizing it without CGC in SYN2. Without correcting a clock line because Enable logic can be built by a data line of a FF, ECO, can.-> But, ECO amount is increased.



Enable signal of CGC is corrected. A relevant part is synthesized without CGC.

Using a data line of a FF. ECO.

Correspondence image by a layout at the time of PostMASK

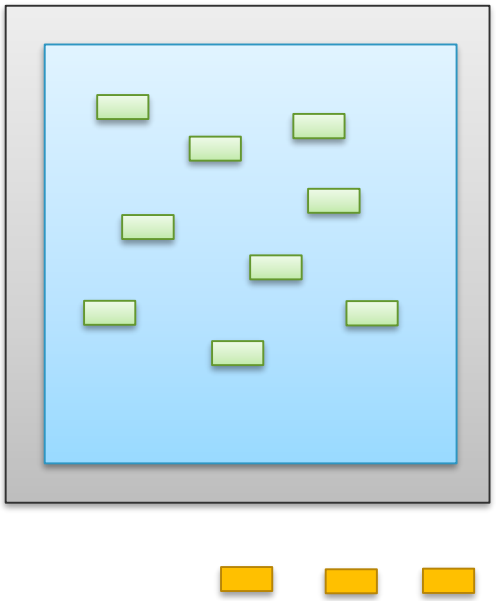
The replace command with the netlist behind ECO and the spare cell is released from Conflrmal ECO. (LAY2.v and mapfile.tcl)

① MW and record Netlist are read in an ICC.(A ECO cell is arranged outside the chip.)

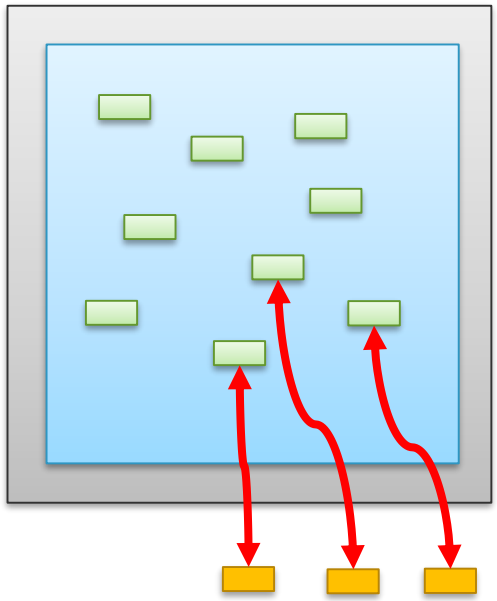
② A ECO cell and a spare cell are replaced.
(It answers with a ECO card (Of mapfile.tcl, the command is changed for ICCs.))

③ Re-wiring

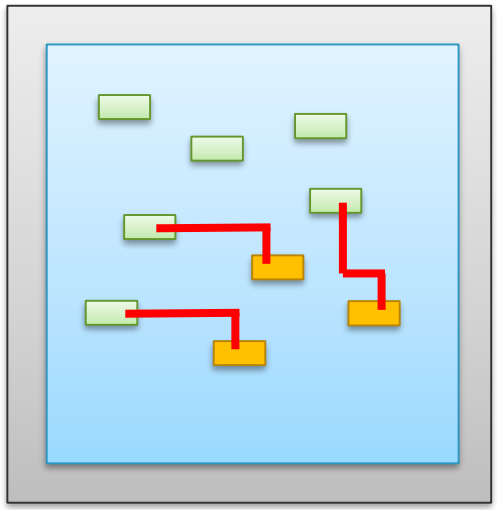
(1)



(2)



(3)



The revision history

The number of editions	Revise article			Creation date	Approval Making
	The contents	Page	Reason		
1.0.	-	All pages	New issue (corresponding to V10.10-s220) DP: WEB-0054176-01.00J	2011.10.07.	Murase Miyazawa
2.0.	The version description is changed.	p.1,2,5,30	It's changed to description corresponding to V11.10-s140.	2012.03.23.	Murase
	The explanation addition of a new function	p.15,16			
	EDA home page Uniform Resource Locator change	p.26			
	A flat Verification ECO flow is added.	p.27,32			
	The explanation addition which can't maintain a scan chain and enhancement schedule elimination of a CPF base of an additional register (v11.1 is undealt with.)	p.20			
	Restriction corresponding to hierarchy CG is eliminated.	p.21			
3.0.	Change in the version description	p.5, 16	The version is changed to the shape that it refers to EDA Site. The base is changed to description corresponding to V11.10-s400.	2012.12.21.	Saito Nakanishi
4.0.	Change in the version description An option is unified in-ecogxl.	All pages	It's changed to V14.20-s180. Influence of license configulation is reflected.	2015.3.27.	Shibatani Nakanishi
	The know-how collection is added to Appendix.	p.35-43	The contents of a question in the past are reflected.		

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