Original issue #447845

Original issue #445723: I2CU
D41MAG00I2CU0011x000_AC/DC

Added by **Le A. Kiet about 1 year** ago. Updated **7 months** ago.

Status:	Closed	**Start date:**	10/05/2017	
Priority:	Immediate	**Due date:**	10/27/2017	
Assignee:	**FE/Horishima Masayoshi**	**% Done:**		50%
Category:	DC/AC	**Spent time:**	-	
Phase:	**DC/AC debug finished**			

Gantt Chart

Display

In/Output

Note_1

Description

AISS2/BID/NguyenD-san,

This ticket is used to follow up the progress of Tester pattern D41MAG00I2CU0011x000
Please refer Wiki for guidance:
http://tdu-redmine10.eda.renesas.com:9410/redmine/projects/m3n-tester/wiki

Thank you very much.
KietLe

I2C_OSCTST_revision.png (45 KB) FE/Horishima Masayoshi , 02/08/2018 02:01 AM
RcarM3N_DC_measurement_I2CU_v3_revised.xlsx (13.9 KB) FE/Horishima Masayoshi , 02/08/2018 11:45 AM

Subtasks

Related issues

History

Updated by Le A. Kiet about 1 year ago #1

- **Phase** set to *Not released(Default state)*

Updated by Le A. Kiet about 1 year ago #2

- **Assignee** changed from *NguyenD (PER/IBUS)* to *FE/Horishima Masayoshi*
- **Phase** changed from *Not released(Default state)* to *Func debug waiting - not reviewed*
- **% Done** changed from *0* to *20*

Dear Hori-san,
cc KietL-san,

I'd like to release 4 DC patterns of I2CU & 1 DC pattern of IICD

- I2CU
  /design02/rcarm3n_sync/common/rcarm3n/VNET1/TESTER/PATTERN/I2CU/ |-- doc | |-- I2CU_M3N.tpl | |--
  R-CarM3N_Tester_pattern_specifiction_I2CU_rev1.0(template_rev1.2).xlsx -> Tester pattern specification | `-- RcarM3W_DC_measurement_I2CU_v1.xlsx
  -> DC measurement specification |-- evcd | |-- D41MAG00I2CU00110000.evcd.gz | |-- D41MAG00I2CU00120000.evcd.gz | |--
  D41MAG00I2CU00130000.evcd.gz | `-- D41MAG00I2CU00140000.evcd.gz |-- scripts | |-- D41MAG00I2CU00110000.tgcntl.gz | |--
  D41MAG00I2CU00110000.veditcntl.gz | |-- D41MAG00I2CU00120000.tgcntl.gz | |-- D41MAG00I2CU00120000.veditcntl.gz | |--
  D41MAG00I2CU00130000.tgcntl.gz | |-- D41MAG00I2CU00130000.veditcntl.gz | |-- D41MAG00I2CU00140000.tgcntl.gz | `--
  D41MAG00I2CU00140000.veditcntl.gz |-- td | |-- D41MAG00I2CU00110000.td0.gz | |-- D41MAG00I2CU00110000.td1.gz | |--
  D41MAG00I2CU00120000.td0.gz | |-- D41MAG00I2CU00120000.td1.gz | |-- D41MAG00I2CU00130000.td0.gz | |-- D41MAG00I2CU00130000.td1.gz | |--
  D41MAG00I2CU00140000.td0.gz | `-- D41MAG00I2CU00140000.td1.gz

- IICD
  /design02/rcarm3n_sync/common/rcarm3n/VNET1/TESTER/PATTERN/IICD/ |-- doc | |-- IICD_M3N.tpl | |--
  R-CarM3N_Tester_pattern_specifiction_IICD_rev1.0(template_rev1.2).xlsx -> Tester pattern specification | `-- RcarM3N_DC_measurement_IICD.xlsx -> DC
  measurement specification |-- evcd | `-- D41MAG00IICD00010000.evcd.gz |-- scripts | |-- D41MAG00IICD00010000.tgcntl.gz | `--
  D41MAG00IICD00010000.veditcntl.gz |-- td | |-- D41MAG00IICD00010000.td0.gz | `-- D41MAG00IICD00010000.td1.gz

- Note: I reviewed TPL file, Tester pattern with KietL-san

Thank you.

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Best regards. **********
Dao Khoi Nguyen (21G)
FE Dept/AISS2 Group/AIS4 Team
Phone: +84-946522247

Updated by Le A. Kiet about 1 year ago #3

Dear Hori-san,
cc KietL-san,

I'd like to release 4 DC patterns of I2CU & 1 DC pattern of IICD

- I2CU
  /design02/rcarm3n_sync/common/rcarm3n/VNET1/TESTER/PATTERN/I2CU/
  /-- doc
  / /-- I2CU_M3N.tpl
  / /-- R-CarM3N_Tester_pattern_specifiction_I2CU_rev1.0(template_rev1.2).xlsx ~~> Tester pattern specification~~
  / `-- RcarM3W_DC_measurement_I2CU_v1.xlsx ~~> DC measurement specification~~
  /-- evcd
  / /-- D41MAG00I2CU00110000.evcd.gz
  / /-- D41MAG00I2CU00120000.evcd.gz
  / /-- D41MAG00I2CU00130000.evcd.gz
  / `-- D41MAG00I2CU00140000.evcd.gz
  /-- scripts
  / /-- D41MAG00I2CU00110000.tgcntl.gz
  / /-- D41MAG00I2CU00110000.veditcntl.gz
  / /-- D41MAG00I2CU00120000.tgcntl.gz
  / /-- D41MAG00I2CU00120000.veditcntl.gz
  / /-- D41MAG00I2CU00130000.tgcntl.gz
  / /-- D41MAG00I2CU00130000.veditcntl.gz
  / /-- D41MAG00I2CU00140000.tgcntl.gz
  / `-- D41MAG00I2CU00140000.veditcntl.gz
  /-- td
  / /-- D41MAG00I2CU00110000.td0.gz
  / /-- D41MAG00I2CU00110000.td1.gz
  / /-- D41MAG00I2CU00120000.td0.gz
  / /-- D41MAG00I2CU00120000.td1.gz
  / /-- D41MAG00I2CU00130000.td0.gz
  / /-- D41MAG00I2CU00130000.td1.gz
  / /-- D41MAG00I2CU00140000.td0.gz
  / `-- D41MAG00I2CU00140000.td1.gz
- IICD
  /design02/rcarm3n_sync/common/rcarm3n/VNET1/TESTER/PATTERN/IICD/
  /-- doc
  / /-- IICD_M3N.tpl
  / /-- R-CarM3N_Tester_pattern_specifiction_IICD_rev1.0(template_rev1.2).xlsx ~~> Tester pattern specification~~
  / `-- RcarM3N_DC_measurement_IICD.xlsx ~~> DC measurement specification~~
  /-- evcd
  / `-- D41MAG00IICD00010000.evcd.gz
  /-- scripts
  / /-- D41MAG00IICD00010000.tgcntl.gz
  / `-- D41MAG00IICD00010000.veditcntl.gz
  /-- td
  / /-- D41MAG00IICD00010000.td0.gz
  / `-- D41MAG00IICD00010000.td1.gz
- Note: I reviewed TPL file, Tester pattern with KietL-san

Thank you.

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Best regards. **********
Dao Khoi Nguyen (21G)
FE Dept/AISS2 Group/AIS4 Team
Phone: +84-946522247

Updated by Le A. Kiet about 1 year ago #4

- **Status** changed from *New* to *In progress*
- **Assignee** changed from *FE/Horishima Masayoshi* to *NguyenD (PER/IBUS)*
- **Phase** changed from *Func debug waiting - not reviewed* to *Func debug - confirming result*

Dear Nguyen-san,
CC Hori-san,

Your pattern got Fail result in function debug following email:
[prj-cis-rcm3n:19983] Re: [M3N] Release tester pattern of GPIO

Would you please perform debugging ?

Thank you very much.
KietLe.

Updated by NguyenD (PER/IBUS) about 1 year ago #5

Dear Kiet-san, Hori-san

There is no log file of this pattern in debug result folder.
Could you help to check it ?

Thank you.

Updated by Le A. Kiet about 1 year ago #6

- **Assignee** changed from *NguyenD (PER/IBUS)* to *FE/Horishima Masayoshi*
- **Phase** changed from *Func debug - confirming result* to *Func debug waiting - not reviewed*

Dear Dao-san,
Cc Hori-san,

Please help to change the Phase and Assignee after you update the ticket.
I updated the ticket for this time.

Thank you very much.
KietLe

Updated by Le A. Kiet about 1 year ago #7

- **Subject** changed from *D41MAG00I2CU0011x000* to *D41MAG00I2CU0011x000_AC/DC*

Updated by Noguchi Takafumi about 1 year ago #8

- **Assignee** changed from *FE/Horishima Masayoshi* to *NguyenD (PER/IBUS)*

Dear NguyenD-san,

I would like to confirm DCP measurement steps.
Could you tell me measurement steps?

Best regards,
ASOC4/Noguchi

Updated by NguyenD (PER/IBUS) about 1 year ago #9

- **Assignee** changed from *NguyenD (PER/IBUS)* to *FE/Horishima Masayoshi*

Dear Takafumi-san, Hori-san

I already define measurement steps in this document. Could you refer it ?
/design02/rcarm3n_sync/common/rcarm3n/VNET1/TESTER/PATTERN/I2CU/doc/RcarM3W_DC_measurement_I2CU_v1.xlsx

BTW, this pattern got fail Shmoo in rev016. Could you send me fail log for debugging ?

Thank you.

Updated by Le A. Kiet about 1 year ago #10

- **Assignee** changed from *FE/Horishima Masayoshi* to *NguyenD (PER/IBUS)*

Updated by Le A. Kiet about 1 year ago #11

- **Phase** changed from *Func debug waiting - not reviewed* to *Func debug - confirming result*

Dear NguyenD-san,
CC Okoshi-san,Chi-san,
CC Noguchi-san, Hori-san,

Your patterns got fail result at rev16:
/design02/rcarm3n_sync/common/rcarm3n/VNET1/TESTER/DEBUG_RESULT/20171019_rev016

Please give your debugging plan.

Thank you very much.
KietLe

Updated by NguyenD (PER/IBUS) about 1 year ago #12

- **Phase** changed from *Func debug - confirming result* to *Func debug waiting - not reviewed*

Dear KietL-san,

As I feedback, there is no fail log of I2C in this folder.

/design02/rcarm3n_sync/common/rcarm3n/VNET1/TESTER/DEBUG_RESULT/20171019_rev016

Thank you.

Updated by FE/Horishima Masayoshi about 1 year ago #13

- **Phase** changed from *Func debug waiting - not reviewed* to *DC/AC debug - confirming result*

Dear NguyenD-san, Cc: Okoshi-san,

DC measurement trial with D41MAG00I2CU00110000 to D41MAG00I2CU00140000 was held.
However, VIL and VIH measurement failed.

Even though input voltage is changed to illegal value, pattern doesn't fail.

I looked into /design02/rcarm3n_sync/common/rcarm3n/VNET1/TESTER/PATTERN/I2CU/doc/R-CarM3N_Tester_pattern_specifiction_I2CU_rev1.0 (template_rev1.2).xlsx.

In the timing chart of OSCTST, step 22 should be input cycle.
At input cycle, input signal should propagates from PAD to CIN.
At step 22, SD1_CD(PAD) is "0".
So the CTS1_N(CIN1) output value should be L, in my opinion. But it's H.

How do you think about this point?

Best regards,
Horishima

Updated by NguyenD (PER/IBUS) about 1 year ago #14

Dear Hori-san, Okoshi-san

Very sorry. I misunderstood about these patterns.
The target pins should be CIN pins, not PAD pins.

Actually, CIN pins were masked in veditcntl file
I will correct the TP spec & release these patterns again.

> *So the CTS1_N(CIN1) output value should be L, in my opinion. But it's H.*

I think H is correct one following the true table.

Thank you.

Updated by FE/Horishima Masayoshi about 1 year ago #15

Dear NguyenD-san,

> *The target pins should be CIN pins, not PAD pins.*

Yes. In case of VIH/L measurement, CIN pins should have expected values.

> *I think H is correct one following the true table.*

I'm sorry I misunderstood the specificaiton.

VIH/VIL measruement steps should be
"(E) Test external 0 and 1 input are transferred to internal CIN when STBN is disabled & I is enabled"

CIN value of Step 27, 35 looks OK.

Updated by FE/Horishima Masayoshi about 1 year ago #16

Dear NguyenD-san,

Could you tell me when you release the updated pattern?

Best regards,
Horishima

Updated by NguyenD (PER/IBUS) about 1 year ago #17

Dear Hori-san,
cc KietL-san

All data is available (except OSCTST pattern of I2C4)
I will release them after reviewing with KietL-san (this afternoon)

About OSCTST pattern of I2C4, CIN pins (RX2 & TX2) are controlled by tfmode signal, so I need to modify the model a little.
I plan to release it by tomorrow afternoon.

Thank you.

Updated by NguyenD (PER/IBUS) about 1 year ago #18

- **Assignee** changed from *NguyenD (PER/IBUS)* to *FE/Horishima Masayoshi*
- **Phase** changed from *DC/AC debug - confirming result* to *Func debug waiting - not reviewed*

Dear Hori-san,
cc KietL-san,

I'd like to update 4 DC patterns of I2CU

/design02/rcarm3n_sync/common/rcarm3n/VNET1/TESTER/PATTERN/I2CU/ |-- doc | |-- I2CU_M3N.tpl | |-- R-CarM3N_Tester_pattern_specifiction_I2CU_rev1.1 (template_rev1.2).xlsx | `-- RcarM3N_DC_measurement_I2CU_v2.xlsx |-- evcd | |-- D41MAG00I2CU00111000.evcd.gz | |-- D41MAG00I2CU00121000.evcd.gz | |-- D41MAG00I2CU00131000.evcd.gz | `-- D41MAG00I2CU00141000.evcd.gz |-- scripts | |-- D41MAG00I2CU00111000.tgcntl.gz | |-- D41MAG00I2CU00111000.veditcntl.gz | |-- D41MAG00I2CU00121000.tgcntl.gz | |-- D41MAG00I2CU00121000.veditcntl.gz | |-- D41MAG00I2CU00131000.tgcntl.gz | |-- D41MAG00I2CU00131000.veditcntl.gz | |-- D41MAG00I2CU00141000.tgcntl.gz | `-- D41MAG00I2CU00141000.veditcntl.gz |-- td | |-- D41MAG00I2CU00111000.td0.gz | |-- D41MAG00I2CU00111000.td1.gz | |-- D41MAG00I2CU00121000.td0.gz | |-- D41MAG00I2CU00121000.td1.gz | |-- D41MAG00I2CU00131000.td0.gz | |-- D41MAG00I2CU00131000.td1.gz | |-- D41MAG00I2CU00141000.td0.gz | `-- D41MAG00I2CU00141000.td1.gz

- Note: I reviewed Tester pattern spec with KietL-san

Thank you.

Updated by Le A. Kiet 12 months ago #19

- **Assignee** changed from *FE/Horishima Masayoshi* to *NguyenD (PER/IBUS)*
- **Phase** changed from *Func debug waiting - not reviewed* to *Func debug - confirming result*

Dear NguyenD-san,
CC Noguchi-san, Hori-san,

This pattern was fail at rev047:
/design02/rcarm3n_sync/common/rcarm3n/VNET1/TESTER/DEBUG_RESULT/20171228_rev047

Could you please give the debugging plan ?

Thank you very much.
KietLe

Updated by NguyenD (PER/IBUS) 12 months ago #20

- **Assignee** changed from *NguyenD (PER/IBUS)* to *FE/Horishima Masayoshi*
- **Phase** changed from *Func debug - confirming result* to *Func debug waiting - not reviewed*

Dear Hori-san,
cc KietL-san

I'd like to release 4 updated DC patterns of I2C

/design02/rcarm3n_sync/common/rcarm3n/VNET1/TESTER/PATTERN/I2CU/ |-- doc | |-- ACSPEC_LIST_I2CU_M3N.csv | |-- I2CU_M3N.tpl | |-- R-CarM3N_Tester_pattern_specifiction_I2CU_rev1.2(template_rev1.2).xlsx | `-- RcarM3N_DC_measurement_I2CU_v2.xlsx |-- evcd | |-- D41MAG00I2CU00112000.evcd.gz | |-- D41MAG00I2CU00122000.evcd.gz | |-- D41MAG00I2CU00132000.evcd.gz | `-- D41MAG00I2CU00142000.evcd.gz |-- scripts | |-- D41MAG00I2CU00112000.tgcntl.gz | |-- D41MAG00I2CU00112000.veditcntl.gz | |-- D41MAG00I2CU00122000.tgcntl.gz | |-- D41MAG00I2CU00122000.veditcntl.gz | |-- D41MAG00I2CU00132000.tgcntl.gz | |-- D41MAG00I2CU00132000.veditcntl.gz | |-- D41MAG00I2CU00142000.tgcntl.gz | `-- D41MAG00I2CU00142000.veditcntl.gz |-- td | |-- D41MAG00I2CU00112000.td0.gz | |-- D41MAG00I2CU00112000.td1.gz | |-- D41MAG00I2CU00122000.td0.gz | |-- D41MAG00I2CU00122000.td1.gz | |-- D41MAG00I2CU00132000.td0.gz | |-- D41MAG00I2CU00132000.td1.gz | |-- D41MAG00I2CU00142000.td0.gz | `-- D41MAG00I2CU00142000.td1.gz
`-- tm |-- I2C0_TESTMODE_PIN_CHK |-- I2C3_TESTMODE_PIN_CHK |-- I2C4_TESTMODE_PIN_CHK
`-- I2C5_TESTMODE_PIN_CHK

Note: I reviewed Tester pattern spec with KietL-san

Thank you.

Updated by Le A. Kiet 12 months ago #21

Dear Kobayashi-san, Noguchi-san, Hori-san,
CC NguyenD-san, Chi-san,

I confirmed Nguyen-san performed review.

Thank you very much.
KietLe

Updated by FE/Horishima Masayoshi 12 months ago #22

- **Assignee** changed from *FE/Horishima Masayoshi* to *NguyenD (PER/IBUS)*
- **Phase** changed from *Func debug waiting - not reviewed* to *Func debug - confirming result*

Dear NguyenD-san,

I checked differences between D41MAG00I2CU00111000 and D41MAG00I2CU00112000.

```
STB_SAMP_1            134500 0 ;
    STB_SAMP_2            19500 0 ;
    STB_DEF             13000 0 ;
    STB_DEF_1             143000 0 ;
    STB_DEF_2             28000 0 ;
```

You added STB_SAMP2 and STB_DEF_2.
Could you tell me the background of this change?
I mean the changes in updated pattern should solve the fail.
Please show me the logical evidence of your solution.

Best regards,
Horishima

Updated by NguyenD (PER/IBUS) 12 months ago #23

Dear Hori-san,
cc KieL-san

Sorry, I cannot hear your voice clearly via telephone
I'd like to answer your concern as below.
- In case we use TR = 15 ns, the default veditcntl file will mask 1 cycles of LSI pins when output value changes.
- In case we use TR = 500 ns (OSCTST pattern), we comment out these lines to measure VIH/L value
//nguyen CTS1_N = 1 hlz01mask mode(CTS1_N , ioc) ;
//nguyen CTS1_N = hlz01mask mode(CTS1_N , oic) ;
Actually, the transition time of these pins may cause the tester result failed. To solve this problem, we modify the tgcntl file to strobe these pin 15ns later.

- Note: in STA report, the transition time of CIN pins < 10ns

If have further concern, please tell me.

Thank you.

Updated by FE/Horishima Masayoshi 12 months ago #24

Dear NguyenD-san,

I'm sorry for the poor network condition then.
Thank you for the answer.

> *- In case we use TR = 15 ns, the default veditcntl file will mask 1 cycles of LSI pins when output value changes.*

It's not correct.
The default veditcntl file masks 1 cycle when **IO direction is changed.**
"ioc" is the condition of "I->O direction Change". "oic" is "O->I direction Change".

> *Actually, the transition time of these pins may cause the tester result failed. To solve this problem, we modify the tgcntl file to strobe these pin 15ns later.*

You changed strobe time of CTS1_N and TX1 from 143ns to 28ns.
It has contradiction with what you said above.

Please give me a reasonable explanation about your update.

Best regards,
Horishima

Updated by FE/Horishima Masayoshi 12 months ago #25

Dear NguyenD-san,

Who were the reviwers of yesterday's pattern update?

Best regards,
Horishima

Updated by NguyenD (PER/IBUS) 12 months ago #26

Dear Hori-san,

> *You changed strobe time of CTS1_N and TX1 from 143ns to 28ns.*
> *It has contradiction with what you said above.*

No, I didn't. 143ns is strobe time of SD1_WP & SD1_CD
I changed strobe time of CTS1_N & TX1 from 13ns to 28ns to overcome the transition time (H->L & L->H)

> *Who were the reviwers of yesterday's pattern update?*

KietL-san reviewed for me.

Thank you.

Updated by FE/Horishima Masayoshi 12 months ago #27

Dear NguyenD-san,

Now I understand the strobe timing of CTS1_N and TX1 was STB_DEF=13ns in the previous pattern.
I misunderstood it was 143ns in the previous pattern.

I'm sorry to bothering you. I have accepted your update.
Let's wait for the debug result.

BTW, the strobe of CTS1_N and TX1 is better to set near the end of a test rate from the begining.

Best regards,
Horishima

Updated by FE/Horishima Masayoshi 12 months ago #28

- **Assignee** changed from *NguyenD (PER/IBUS)* to *HiICS/Kobayashi 小林 Nobuyuki*

Updated by HiICS/Kobayashi 小林 Nobuyuki 11 months ago #29

- **Assignee** changed from *HiICS/Kobayashi 小林 Nobuyuki* to *FE/Horishima Masayoshi*

Dear Horishima-san,
Thank you for your cooperates.

D41MAG00I2CU00112000 was released Tester yesterday.
So may I change phase to "Func debug waiting - converted"?

HiICS/Nobuyuki Kobayashi

Updated by FE/Horishima Masayoshi 11 months ago #30

Dear Kobayashi-san,

> *So may I change phase to "Func debug waiting - converted"?*

Yes, you can.

Best regards,
Horishima

Updated by HiICS/Kobayashi 小林 Nobuyuki 11 months ago #31

- **Assignee** changed from *FE/Horishima Masayoshi* to *HiICS/Kobayashi 小林 Nobuyuki*
- **Phase** changed from *Func debug - confirming result* to *Func debug waiting - test*

Updated by FE/Horishima Masayoshi 11 months ago #32

- **Assignee** changed from *HiICS/Kobayashi 小林 Nobuyuki* to *NguyenD (PER/IBUS)*
- **Priority** changed from *Normal* to *Immediate*
- **Phase** changed from *Func debug waiting - test* to *Func debug - confirming result*

Dear NguyenD-san,

All updated 4 paterns failed with same fail steps.

Please update pattern with the below idea.

> *BTW, the strobe of CTS1_N and TX1 is better to set near the end of a test rate from the begining.*

The strobe of such output signals could be 450ns or someothing.
I expect you to update ASAP. Due to DC measurement debug will be held next week.

Best regards,
Horishima

Updated by FE/Horishima Masayoshi 11 months ago #33

Dear Nghia-san, Kiet-san,

If NguyenD-san cannot secure time to update pattern (just timing set update) Jan/12th, please let me know.

Best regards,
Horishima

Updated by FE/Horishima Masayoshi 11 months ago #34

Dear NguyenD-san,

> •*Note: in STA report, the transition time of CIN pins < 10ns*

You are missing to think about path delay related to OSCTST logic.

Best regards,
Horishima

Updated by (RVC/FE/RCPD) NghiaTran 11 months ago #35

Dear Hori-san,
Cc NguyenD-san, KietL-san,

He had plan for M3N tester today.
I think he can update these patterns.

@NguyenD-san,
If you face difficulty, please me know.

Thank you.

Updated by NguyenD (PER/IBUS) 11 months ago #36

Dear Hori-san,
cc KietL-san, NghiaT-san

> *You are missing to think about path delay related to OSCTST logic.*

I understand it.

I can release updated DC patterns today.

Sorry for this inconvenience.

Updated by FE/Horishima Masayoshi 11 months ago #37

Dear NguyenD-san,

Thank you for your understaning. Let me wait for your updated pattern.

Dear Nghia-san,

Thank you for your support.

Horishima

Updated by NguyenD (PER/IBUS) 11 months ago #38

- **Assignee** changed from *NguyenD (PER/IBUS)* to *FE/Horishima Masayoshi*
- **Phase** changed from *Func debug - confirming result* to *Func debug waiting - not reviewed*

Dear Hori-san,
cc KietL-san

I'd like to release 4 updated DC patterns of I2C

```
/design02/rcarm3n_sync/common/rcarm3n/VNET1/TESTER/PATTERN/I2CU/
/-- doc
/ |-- I2CU_M3N.tpl
/ |-- R-CarM3N_Tester_pattern_specifiction_I2CU_rev1.3(template_rev1.2).xlsx
/ `-- RcarM3N_DC_measurement_I2CU_v2.xlsx
/-- evcd
/ |-- D41MAG00I2CU00113000.evcd.gz
/ |-- D41MAG00I2CU00123000.evcd.gz
/ |-- D41MAG00I2CU00133000.evcd.gz
/ `-- D41MAG00I2CU00143000.evcd.gz
/-- scripts
/ |-- D41MAG00I2CU00113000.tgcntl.gz
/ |-- D41MAG00I2CU00113000.veditcntl.gz
/ |-- D41MAG00I2CU00123000.tgcntl.gz
/ |-- D41MAG00I2CU00123000.veditcntl.gz
/ |-- D41MAG00I2CU00133000.tgcntl.gz
/ |-- D41MAG00I2CU00133000.veditcntl.gz
/ |-- D41MAG00I2CU00143000.tgcntl.gz
/ `-- D41MAG00I2CU00143000.veditcntl.gz
/-- td
/ |-- D41MAG00I2CU00113000.td0.gz
/ |-- D41MAG00I2CU00113000.td1.gz
/ |-- D41MAG00I2CU00123000.td0.gz
/ |-- D41MAG00I2CU00123000.td1.gz
/ |-- D41MAG00I2CU00133000.td0.gz
/ |-- D41MAG00I2CU00133000.td1.gz
/ |-- D41MAG00I2CU00143000.td0.gz
/ `-- D41MAG00I2CU00143000.td1.gz
/-- tm
/-- I2C0_TESTMODE_PIN_CHK
/-- I2C3_TESTMODE_PIN_CHK
/-- I2C4_TESTMODE_PIN_CHK
/-- I2C5_TESTMODE_PIN_CHK
```

Note: I reviewed Tester pattern spec with KietL-san

Thank you.

Updated by FE/Horishima Masayoshi 11 months ago #39

- **Assignee** changed from *FE/Horishima Masayoshi* to *HiICS/Kobayashi 小林 Nobuyuki*

Dear NguyenD-san,

I confirmed the updated tgcntl files are OK.
Thsnk you for the release.

Dear Kobayashi-san,

Please release those updated patterns to Nanao-san.

Best regards,
Horishima

Updated by HiICS/Kobayashi 小林 Nobuyuki 11 months ago #40

Dear KietL-san, Horishima-san,
cc: Noguchi-san,

Sorry for late.
I think it needs to get an announce of reviewer as review completed.
Will KietL-san announce?
Please consider it.

HiICS/Nobuyuki Kobayashi

Updated by Le A. Kiet 11 months ago #41

Dear Hori-san, Noguchi-san, Kobayashi-san,
CC Nguyen-san,

I confirmed NguyenD-san performed review.

Thank you very much.
KietLe.

Updated by FE/HiICS/hatakeyama akiyoshi 11 months ago #42

- **Phase** changed from *Func debug waiting - not reviewed* to *Func debug waiting - test*

Updated by HiICS/Kobayashi 小林 Nobuyuki 11 months ago #43

- **Phase** changed from *Func debug waiting - test* to *Func debug - confirming result*

Dear NguyenD-san,

Sorry for late.
I got Tester result as Rev057.
Please see RVC side sync directory.

Many thanks,
HiICS/Nobuyuki Kobayashi

Updated by Le A. Kiet 11 months ago #44

- **Phase** changed from *Func debug - confirming result* to *28770*
- **% Done** changed from *20* to *50*

Dear NguyenD-san,
Dear Hori-san, Noguchi-san, Kobayashi-san,

Your pattern was passed, no problem in shmoo at rev057.
And this is DC pattern. Therefore, I would like to change phase to "DC/AC debug waiting - reviewed".

Thank you very much.
KietLe.

Updated by Le A. Kiet 11 months ago #45

- **Phase** changed from *28770* to *DC/AC debug tesing*

Updated by FE/Horishima Masayoshi 11 months ago #46

- **File I2C_OSCTST_revision.png** added
- **Assignee** changed from *HiICS/Kobayashi 小林 Nobuyuki* to *NguyenD (PER/IBUS)*
- **Phase** changed from *DC/AC debug tesing* to *DC/AC debug - confirming result*

Dear NguyenD-san,

DC measurement with I2C OSCTST pattenn is not stable due to mistakes in the measurment specifications.
I corrected only for D41MAG00I2CU00113000 as the attached picture.
The orange color cells are corrected cells.

- Column-K: Cell name of CIN value output pins are wrong.

- Column-L/M: Hiz must be measured when "STBN = high" = IO cell stanby is disabled = "(B)" in the waveform.

- Column-N to Q: VIL/VIH is judged by pattern PASS/FAIL by changing input voltage. Pattern stop at a certain step is not necessary

- Column-R/S: VOL only checks I2C IO cell pin.

- Column-T/U: VOH is not supported by I2C IO cell.

If you have questions about the above opnioin, please let me know.
Is no questions, please update patten specificaiton ASAP.

Best regards,
Horishima

Updated by FE/Horishima Masayoshi 11 months ago #47

Dear NguyenD-san,

I and Okoshi-san will review the updated specification document before official release.

Best regards,
Horishima

Updated by FE/Horishima Masayoshi 11 months ago #48

Dear NguyenD-san,

Update infomation for other I2CU OSCTST pattern, too.

Best regards,
Horishima

Updated by NguyenD (PER/IBUS) 11 months ago #49

- **Assignee** changed from *NguyenD (PER/IBUS)* to *FE/Horishima Masayoshi*
- **Phase** changed from *DC/AC debug - confirming result* to *DC/AC debug tesing*

Dear Horishima-san,
cc Okoshi-san,

I updated DC measurement spec of I2C.
Could you review it ?
/design02/rcarm3n_sync/common/rcarm3n/VNET1/TESTER/PATTERN/I2CU/doc/RcarM3N_DC_measurement_I2CU_v3.xlsx

Thank you.

Updated by FE/Horishima Masayoshi 11 months ago #50

- **File RcarM3N_DC_measurement_I2CU_v3_revised.xlsx** added

Dear NguyenD-san,

I found 2 mistakes in the v3.2

- 2nd pin's HiZ cycle 44 --> 45, or 64 --> 65 for each pattern
- Step information of L output for VIL for each pattern

The corrected cells are colored orange in the attached file.
Please overwrite this file as v3.

Best regards,
Horishima

Updated by FE/Horishima Masayoshi 11 months ago #51

- **Assignee** changed from *FE/Horishima Masayoshi* to *NguyenD (PER/IBUS)*

Updated by NguyenD (PER/IBUS) 11 months ago #52

- **Assignee** changed from *NguyenD (PER/IBUS)* to *FE/Horishima Masayoshi*

Dear Hori-san,

I corrected & overwritten as v3

Thank you.

Updated by FE/Horishima Masayoshi 9 months ago #53

- **Category** set to *DC/AC*

Updated by NguyenD (PER/IBUS) 7 months ago #54

- **Status** changed from *In progress* to *Closed*
- **Phase** changed from *DC/AC debug tesing* to *DC/AC debug finished*

Dear Kobayashi-san, Hori-san
cc KietL-san

Following this ticket, we can judge AC measurement of this pattern as "Pass"
http://tdu-redmine10.eda.renesas.com:9410/redmine/issues/447851

So I'd like to close this ticket.

Thank you.