

Lab Report:

Name: Le Thien Nam Nguyen

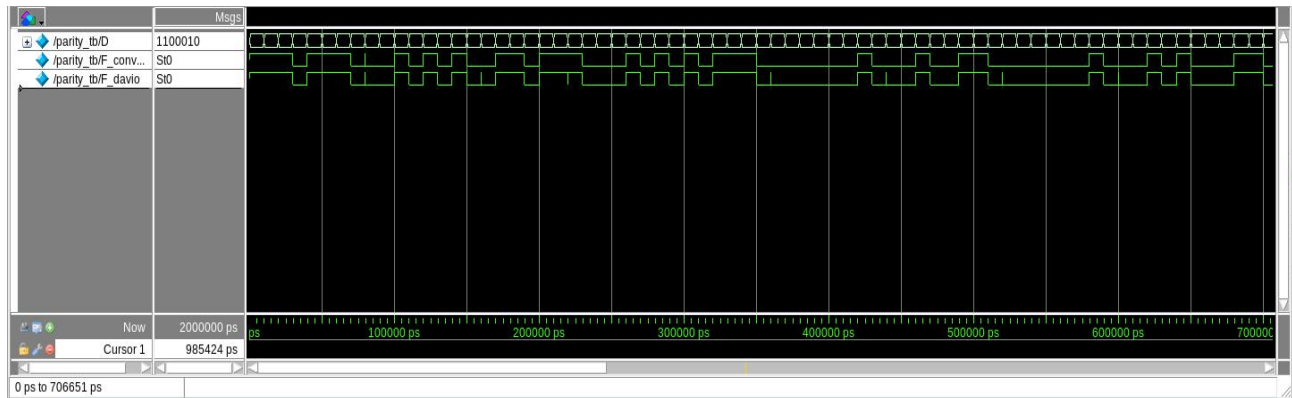
NISD: nln157

Student number: 11161522

Class: CME 433 Lab

Lab 1

1. Explain the differences between using case statement and if/else statement
 - The main difference between case statement and if/else statement is the trade off between time and space:
 - The case statement is executed in parallel. Therefore, it takes less time to finish but it takes more space or area.
 - The if/else statement is executed in serial. Therefore, the critical path is longer and it takes more time to finish. However, it takes up a small space or area.
 - ⇒ In conclusion, if you want to trade space for time, you can choose the case statement. If you want to trade time for space, you can choose the if/else statement.
2. Explain how my design can be optimized for performance, and how it can be optimized for (minimum) size/area.
 - My design can be optimized for performance in time and space, which means that I can optimize my design so that the optimized design can run faster and take less time than the original one. I can apply technology mapping, case statement and if/else statement.
 - My design can be optimized for (minimum) size/area by switching all case statements to if/else statements.
3. I have included the parity_davio code and testbench in the folder
4. Verify with testbench and pictures



- From the screen shot, we can observe that the waveforms of both convention and davio are identical. These small lines are not values but they indicate the change of inputs.
- I also have an if/else statement to verify the values convention and davio. If they are the same → Verify. If they are different → Error. Here is the result:

```
# VERIFY F_davio is functionally equivalent to the conventional method
# ** Note: $stop : /home/nln157/engr-ece/fourth_year_labs/CME433_labs/lab1_Basic_FPGA/simulation/modelsim/parity_tb.sv(21)
# Time: 2 us Iteration: 0 Instance: /parity_tb
# Break in Module parity_tb at /home/nln157/engr-ece/fourth_year_labs/CME433_labs/lab1_Basic_FPGA/simulation/modelsim/parity_tb.sv line 21
```

5. Optimization strategy

	Davio	Convention
Balance	7 LE	8 LE
Performance	7 LE	8 LE
Power	7 LE	8 LE
Area	7 LE	8 LE

- The Davio is better than the Convention with 1 LE. The reason that Balance, Performance, Power and Area are the same is because the Quartus compiler is too advanced. Therefore it makes no difference even though we change the setting.