Vending Machine bases on DE10-Lite

Abstract

In this project, the team members used the Verilog Hardware Description Language to implement the Intel DE10-Lite FPGA board and a 4x4 matrix keyboard. Our team designed a vending machine that can take three 3 kinds of currencies, which are dime, quarter and dollar. And there is a total of 5 items with different prices (i.g. item A is 50 cents, item B is 80 cents, etc.) can be delivered by the vending machine. The user can choose a max amount of 3 items each time. The vending machine can also display how much money, in cents, the user has inserted on the 7-segment display LED, it also displays the amount of money to be returned if the user confirms the transaction.

Keyword: Verilog Design, Vending Machine, FPGA

1 Introduction

There are two buttons in the vending machine, one is a cancel button and the other is a continue button. When the cancel button is pressed, a cancel signal will be sent, and the vending machine will cancel the transaction and return all the money the user inserts. The customer is able to select the required amount of product and insert money after an item is selected. After the collected coins exceed the price, the system will display the change automatically. The system will hold until the continue button is pressed, a confirm signal will be detected, the vending machine returns to the idle state and wait for the user to conduct another purchase.

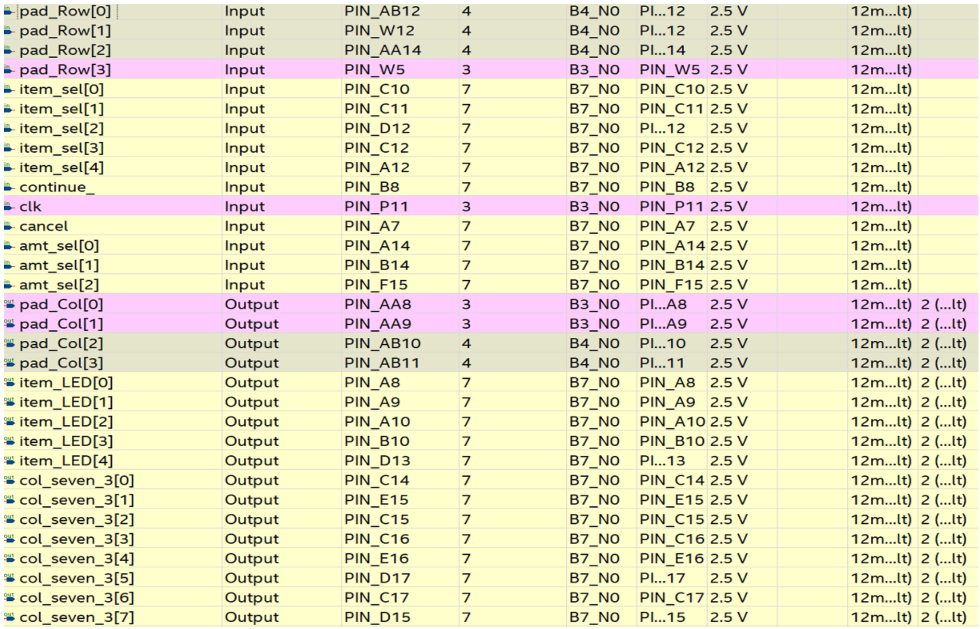
On the FPGA board, there are a total of 6 7-segment LED lights. The right 3 LEDs are used to display how much money the user has input, and the left 3 are used to show how much change the user may get.

The team members used a 50 MHz input clock to implement a slower clock used for checking the inserted currency and driving the combinational logic in the state machine. The implemented clock is 20 Hz.

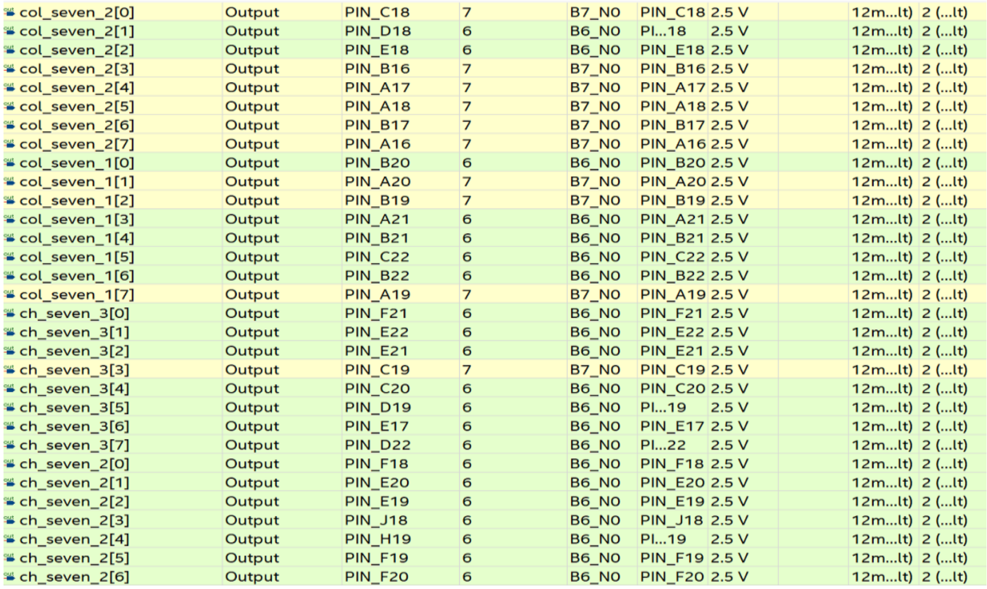
The team members also used a 4x4 keyboard to simulate the money inserted.

2 Working

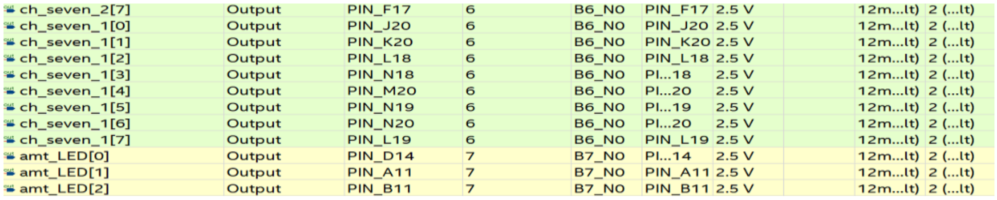
In our design, we debugged at first, and after four versions of the revision, we finally got the current version that could run. In the design process, the clock is the most complicated processing. In the stage of the compile clock, because of the time setting problem, during the input of the keyboard, when the key is pressed, the money invested in the simulation will continuously increase, leading to the operation trip. We made several clock adjustments in the coin-inserting process, and the clock in the keyboard input process match each other finally. The following figures show the vending machine in action. First, let's define the access part of the pins.



pad_Row[0]	Input	PIN_AB12	4	B4_N0	PI...12	2.5 V		12m...lt)	
pad_Row[1]	Input	PIN_W12	4	B4_N0	PI...12	2.5 V		12m...lt)	
pad_Row[2]	Input	PIN_AA14	4	B4_N0	PI...14	2.5 V		12m...lt)	
pad_Row[3]	Input	PIN_W5	3	B3_N0	PIN_W5	2.5 V		12m...lt)	
item_sel[0]	Input	PIN_C10	7	B7_N0	PIN_C10	2.5 V		12m...lt)	
item_sel[1]	Input	PIN_C11	7	B7_N0	PIN_C11	2.5 V		12m...lt)	
item_sel[2]	Input	PIN_D12	7	B7_N0	PI...12	2.5 V		12m...lt)	
item_sel[3]	Input	PIN_C12	7	B7_N0	PIN_C12	2.5 V		12m...lt)	
item_sel[4]	Input	PIN_A12	7	B7_N0	PIN_A12	2.5 V		12m...lt)	
continue_	Input	PIN_B8	7	B7_N0	PIN_B8	2.5 V		12m...lt)	
clk	Input	PIN_P11	3	B3_N0	PIN_P11	2.5 V		12m...lt)	
cancel	Input	PIN_A7	7	B7_N0	PIN_A7	2.5 V		12m...lt)	
amt_sel[0]	Input	PIN_A14	7	B7_N0	PIN_A14	2.5 V		12m...lt)	
amt_sel[1]	Input	PIN_B14	7	B7_N0	PIN_B14	2.5 V		12m...lt)	
amt_sel[2]	Input	PIN_F15	7	B7_N0	PIN_F15	2.5 V		12m...lt)	
pad_Col[0]	Output	PIN_AA8	3	B3_N0	PI...A8	2.5 V		12m...lt)	2 (...lt)
pad_Col[1]	Output	PIN_AA9	3	B3_N0	PI...A9	2.5 V		12m...lt)	2 (...lt)
pad_Col[2]	Output	PIN_AB10	4	B4_N0	PI...10	2.5 V		12m...lt)	2 (...lt)
pad_Col[3]	Output	PIN_AB11	4	B4_N0	PI...11	2.5 V		12m...lt)	2 (...lt)
item_LED[0]	Output	PIN_A8	7	B7_N0	PIN_A8	2.5 V		12m...lt)	2 (...lt)
item_LED[1]	Output	PIN_A9	7	B7_N0	PIN_A9	2.5 V		12m...lt)	2 (...lt)
item_LED[2]	Output	PIN_A10	7	B7_N0	PIN_A10	2.5 V		12m...lt)	2 (...lt)
item_LED[3]	Output	PIN_B10	7	B7_N0	PIN_B10	2.5 V		12m...lt)	2 (...lt)
item_LED[4]	Output	PIN_D13	7	B7_N0	PI...13	2.5 V		12m...lt)	2 (...lt)
col_seven_3[0]	Output	PIN_C14	7	B7_N0	PIN_C14	2.5 V		12m...lt)	2 (...lt)
col_seven_3[1]	Output	PIN_E15	7	B7_N0	PIN_E15	2.5 V		12m...lt)	2 (...lt)
col_seven_3[2]	Output	PIN_C15	7	B7_N0	PIN_C15	2.5 V		12m...lt)	2 (...lt)
col_seven_3[3]	Output	PIN_C16	7	B7_N0	PIN_C16	2.5 V		12m...lt)	2 (...lt)
col_seven_3[4]	Output	PIN_E16	7	B7_N0	PIN_E16	2.5 V		12m...lt)	2 (...lt)
col_seven_3[5]	Output	PIN_D17	7	B7_N0	PI...17	2.5 V		12m...lt)	2 (...lt)
col_seven_3[6]	Output	PIN_C17	7	B7_N0	PIN_C17	2.5 V		12m...lt)	2 (...lt)
col_seven_3[7]	Output	PIN_D15	7	B7_N0	PI...15	2.5 V		12m...lt)	2 (...lt)



col_seven_2[0]	Output	PIN_C18	7	B7_N0	PIN_C18	2.5 V		12m...lt)	2 (...lt)
col_seven_2[1]	Output	PIN_D18	6	B6_N0	PI...18	2.5 V		12m...lt)	2 (...lt)
col_seven_2[2]	Output	PIN_E18	6	B6_N0	PIN_E18	2.5 V		12m...lt)	2 (...lt)
col_seven_2[3]	Output	PIN_B16	7	B7_N0	PIN_B16	2.5 V		12m...lt)	2 (...lt)
col_seven_2[4]	Output	PIN_A17	7	B7_N0	PIN_A17	2.5 V		12m...lt)	2 (...lt)
col_seven_2[5]	Output	PIN_A18	7	B7_N0	PIN_A18	2.5 V		12m...lt)	2 (...lt)
col_seven_2[6]	Output	PIN_B17	7	B7_N0	PIN_B17	2.5 V		12m...lt)	2 (...lt)
col_seven_2[7]	Output	PIN_A16	7	B7_N0	PIN_A16	2.5 V		12m...lt)	2 (...lt)
col_seven_1[0]	Output	PIN_B20	6	B6_N0	PIN_B20	2.5 V		12m...lt)	2 (...lt)
col_seven_1[1]	Output	PIN_A20	7	B7_N0	PIN_A20	2.5 V		12m...lt)	2 (...lt)
col_seven_1[2]	Output	PIN_B19	7	B7_N0	PIN_B19	2.5 V		12m...lt)	2 (...lt)
col_seven_1[3]	Output	PIN_A21	6	B6_N0	PIN_A21	2.5 V		12m...lt)	2 (...lt)
col_seven_1[4]	Output	PIN_B21	6	B6_N0	PIN_B21	2.5 V		12m...lt)	2 (...lt)
col_seven_1[5]	Output	PIN_C22	6	B6_N0	PIN_C22	2.5 V		12m...lt)	2 (...lt)
col_seven_1[6]	Output	PIN_B22	6	B6_N0	PIN_B22	2.5 V		12m...lt)	2 (...lt)
col_seven_1[7]	Output	PIN_A19	7	B7_N0	PIN_A19	2.5 V		12m...lt)	2 (...lt)
ch_seven_3[0]	Output	PIN_F21	6	B6_N0	PIN_F21	2.5 V		12m...lt)	2 (...lt)
ch_seven_3[1]	Output	PIN_E22	6	B6_N0	PIN_E22	2.5 V		12m...lt)	2 (...lt)
ch_seven_3[2]	Output	PIN_E21	6	B6_N0	PIN_E21	2.5 V		12m...lt)	2 (...lt)
ch_seven_3[3]	Output	PIN_C19	7	B7_N0	PIN_C19	2.5 V		12m...lt)	2 (...lt)
ch_seven_3[4]	Output	PIN_C20	6	B6_N0	PIN_C20	2.5 V		12m...lt)	2 (...lt)
ch_seven_3[5]	Output	PIN_D19	6	B6_N0	PI...19	2.5 V		12m...lt)	2 (...lt)
ch_seven_3[6]	Output	PIN_E17	6	B6_N0	PIN_E17	2.5 V		12m...lt)	2 (...lt)
ch_seven_3[7]	Output	PIN_D22	6	B6_N0	PI...22	2.5 V		12m...lt)	2 (...lt)
ch_seven_2[0]	Output	PIN_F18	6	B6_N0	PIN_F18	2.5 V		12m...lt)	2 (...lt)
ch_seven_2[1]	Output	PIN_E20	6	B6_N0	PIN_E20	2.5 V		12m...lt)	2 (...lt)
ch_seven_2[2]	Output	PIN_E19	6	B6_N0	PIN_E19	2.5 V		12m...lt)	2 (...lt)
ch_seven_2[3]	Output	PIN_J18	6	B6_N0	PIN_J18	2.5 V		12m...lt)	2 (...lt)
ch_seven_2[4]	Output	PIN_H19	6	B6_N0	PI...19	2.5 V		12m...lt)	2 (...lt)
ch_seven_2[5]	Output	PIN_F19	6	B6_N0	PIN_F19	2.5 V		12m...lt)	2 (...lt)
ch_seven_2[6]	Output	PIN_F20	6	B6_N0	PIN_F20	2.5 V		12m...lt)	2 (...lt)



ch_seven_2[7]	Output	PIN_F17	6	B6_N0	PIN_F17	2.5 V		12m...lt)	2 (...lt)
ch_seven_1[0]	Output	PIN_J20	6	B6_N0	PIN_J20	2.5 V		12m...lt)	2 (...lt)
ch_seven_1[1]	Output	PIN_K20	6	B6_N0	PIN_K20	2.5 V		12m...lt)	2 (...lt)
ch_seven_1[2]	Output	PIN_L18	6	B6_N0	PIN_L18	2.5 V		12m...lt)	2 (...lt)
ch_seven_1[3]	Output	PIN_N18	6	B6_N0	PI...18	2.5 V		12m...lt)	2 (...lt)
ch_seven_1[4]	Output	PIN_M20	6	B6_N0	PI...20	2.5 V		12m...lt)	2 (...lt)
ch_seven_1[5]	Output	PIN_N19	6	B6_N0	PI...19	2.5 V		12m...lt)	2 (...lt)
ch_seven_1[6]	Output	PIN_N20	6	B6_N0	PI...20	2.5 V		12m...lt)	2 (...lt)
ch_seven_1[7]	Output	PIN_L19	6	B6_N0	PIN_L19	2.5 V		12m...lt)	2 (...lt)
amt_LED[0]	Output	PIN_D14	7	B7_N0	PI...14	2.5 V		12m...lt)	2 (...lt)
amt_LED[1]	Output	PIN_A11	7	B7_N0	PIN_A11	2.5 V		12m...lt)	2 (...lt)
amt_LED[2]	Output	PIN_B11	7	B7_N0	PIN_B11	2.5 V		12m...lt)	2 (...lt)

Figure 1 Pin for Vending machine

Figure 1 shows our pin connection. From the DE10-Lite manual, we successfully connect our project to the FPGA board.

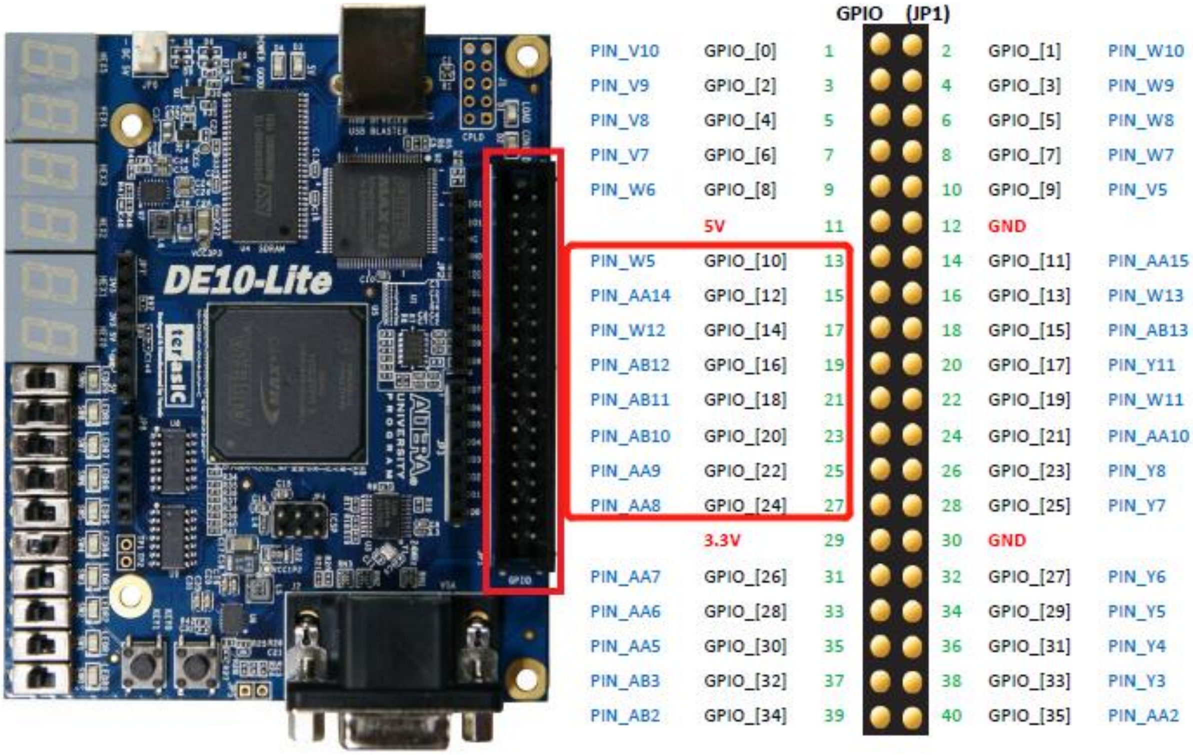

DE10-Lite
GPIO (JP1)
PIN_V10 GPIO_[0] 1 2 GPIO_[1] PIN_W10
PIN_V9 GPIO_[2] 3 4 GPIO_[3] PIN_W9
PIN_V8 GPIO_[4] 5 6 GPIO_[5] PIN_W8
PIN_V7 GPIO_[6] 7 8 GPIO_[7] PIN_W7
PIN_W6 GPIO_[8] 9 10 GPIO_[9] PIN_V5
5V 11 12 GND
PIN_W5 GPIO_[10] 13 14 GPIO_[11] PIN_AA15
PIN_AA14 GPIO_[12] 15 16 GPIO_[13] PIN_W13
PIN_W12 GPIO_[14] 17 18 GPIO_[15] PIN_AB13
PIN_AB12 GPIO_[16] 19 20 GPIO_[17] PIN_Y11
PIN_AB11 GPIO_[18] 21 22 GPIO_[19] PIN_W11
PIN_AB10 GPIO_[20] 23 24 GPIO_[21] PIN_AA10
PIN_AA9 GPIO_[22] 25 26 GPIO_[23] PIN_Y8
PIN_AA8 GPIO_[24] 27 28 GPIO_[25] PIN_Y7
3.3V 29 30 GND
PIN_AA7 GPIO_[26] 31 32 GPIO_[27] PIN_Y6
PIN_AA6 GPIO_[28] 33 34 GPIO_[29] PIN_Y5
PIN_AA5 GPIO_[30] 35 36 GPIO_[31] PIN_Y4
PIN_AB3 GPIO_[32] 37 38 GPIO_[33] PIN_Y3
PIN_AB2 GPIO_[34] 39 40 GPIO_[35] PIN_AA2

Figure 2 Pin for Keyboard

Similarly, we successfully set keyboard pins of our project, we used GPIO 13 to 27 as keyboard Row inputs and Column outputs.

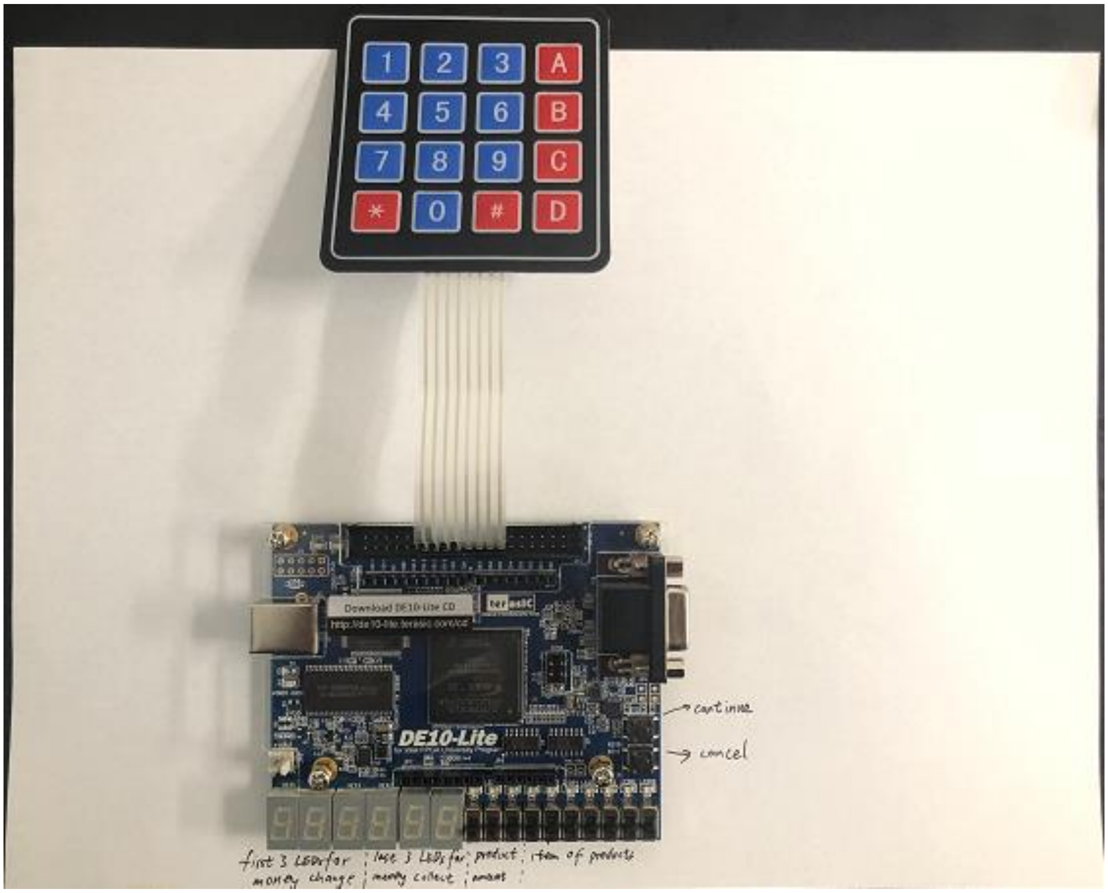


Figure 3 Project display

Figure 3 shows our design, as we mentioned in pin part above, from HEX5 to HEX3 indicated the money back to customers; HEX2 to HEX0 indicated the money customers inserted; SW9 to SW7 indicated the amount of the products; SW6 to SW2 indicated product A to E. Also, KEY0 indicated continue options; KEY1 indicated cancel options. More details in our Demo Video.

3 Schematic

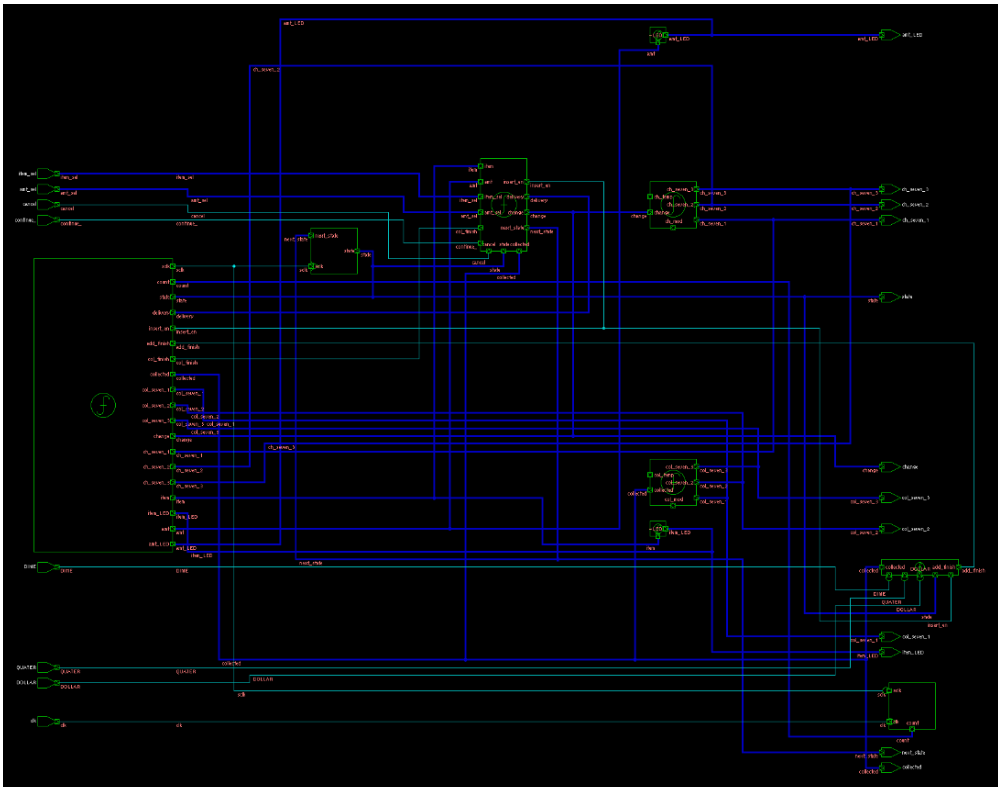


Figure 4 Vending Machine Schematic

Figure 4 shows our schematic for the vending machine.

4 State Diagram

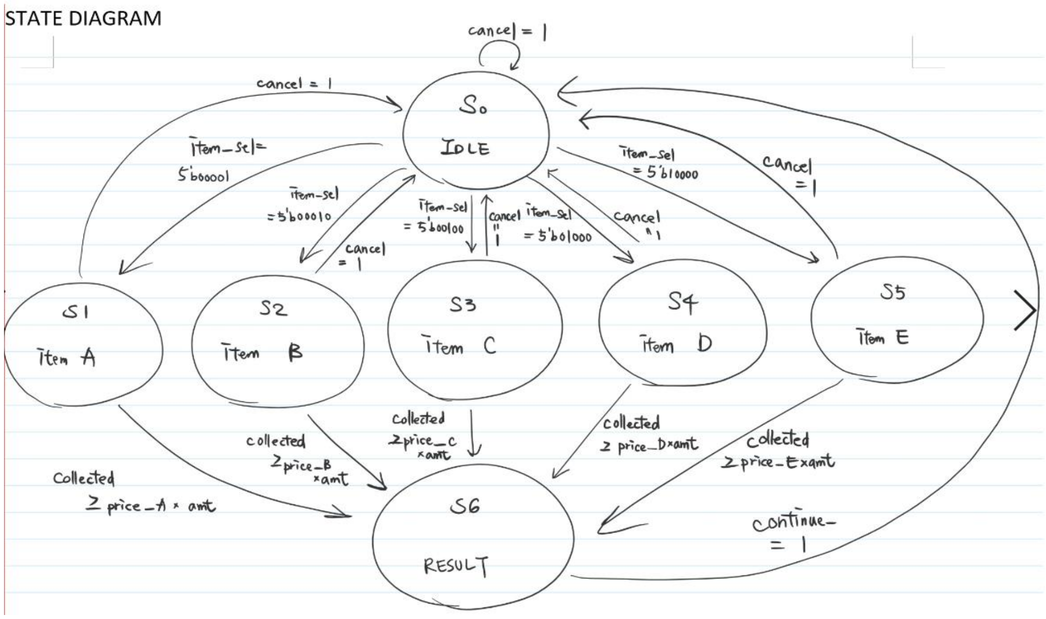
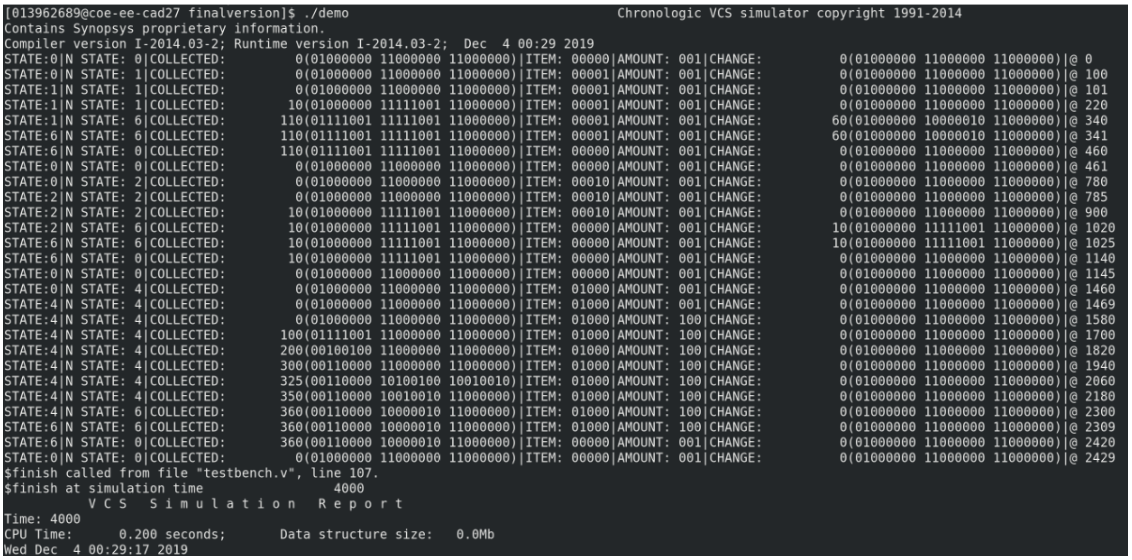


Figure 5 State Diagram

In the state diagram, we set up seven states: S0~S6. S0 represents the beginning of the machine and is an idle state. S1~S5 represents the five products set by us. In these five states, we implement a cancel key. When the user wants to cancel the purchase, he/she can press the cancel button, and the money inserted will be returned. S6 state is the final processing stage, where the machine will deliver the goods and display the details of the purchase(item, amount, change).

5 Simulation Results



```
[013962689@coe-ee-cad27 finalversion]$ ./demo                            Chronologic VCS simulator copyright 1991-2014
Contains Synopsys proprietary information.
Compiler version I-2014.03-2; Runtime version I-2014.03-2;  Dec  4 00:29 2019
STATE:0|N STATE: 0|COLLECTED:          0(01000000 11000000 11000000)|ITEM: 00000|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 0
STATE:0|N STATE: 1|COLLECTED:          0(01000000 11000000 11000000)|ITEM: 00001|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 100
STATE:1|N STATE: 1|COLLECTED:          0(01000000 11000000 11000000)|ITEM: 00001|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 101
STATE:1|N STATE: 1|COLLECTED:         10(01000000 11111001 11000000)|ITEM: 00001|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 220
STATE:1|N STATE: 6|COLLECTED:        110(01111001 11111001 11000000)|ITEM: 00001|AMOUNT: 001|CHANGE:         60(01000000 10000010 11000000)|@ 340
STATE:6|N STATE: 6|COLLECTED:        110(01111001 11111001 11000000)|ITEM: 00001|AMOUNT: 001|CHANGE:         60(01000000 10000010 11000000)|@ 341
STATE:6|N STATE: 0|COLLECTED:        110(01111001 11111001 11000000)|ITEM: 00000|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 460
STATE:0|N STATE: 0|COLLECTED:          0(01000000 11000000 11000000)|ITEM: 00000|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 461
STATE:0|N STATE: 2|COLLECTED:          0(01000000 11000000 11000000)|ITEM: 00010|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 780
STATE:2|N STATE: 2|COLLECTED:          0(01000000 11000000 11000000)|ITEM: 00010|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 785
STATE:2|N STATE: 2|COLLECTED:         10(01000000 11111001 11000000)|ITEM: 00010|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 900
STATE:2|N STATE: 6|COLLECTED:         10(01000000 11111001 11000000)|ITEM: 00000|AMOUNT: 001|CHANGE:         10(01000000 11111001 11000000)|@ 1020
STATE:6|N STATE: 6|COLLECTED:         10(01000000 11111001 11000000)|ITEM: 00000|AMOUNT: 001|CHANGE:         10(01000000 11111001 11000000)|@ 1025
STATE:6|N STATE: 0|COLLECTED:         10(01000000 11111001 11000000)|ITEM: 00000|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 1140
STATE:0|N STATE: 0|COLLECTED:          0(01000000 11000000 11000000)|ITEM: 00000|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 1145
STATE:0|N STATE: 4|COLLECTED:          0(01000000 11000000 11000000)|ITEM: 01000|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 1460
STATE:4|N STATE: 4|COLLECTED:          0(01000000 11000000 11000000)|ITEM: 01000|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 1469
STATE:4|N STATE: 4|COLLECTED:          0(01000000 11000000 11000000)|ITEM: 01000|AMOUNT: 100|CHANGE:          0(01000000 11000000 11000000)|@ 1580
STATE:4|N STATE: 4|COLLECTED:        100(01111001 11000000 11000000)|ITEM: 01000|AMOUNT: 100|CHANGE:          0(01000000 11000000 11000000)|@ 1700
STATE:4|N STATE: 4|COLLECTED:        200(00100100 11000000 11000000)|ITEM: 01000|AMOUNT: 100|CHANGE:          0(01000000 11000000 11000000)|@ 1820
STATE:4|N STATE: 4|COLLECTED:        300(00110000 11000000 11000000)|ITEM: 01000|AMOUNT: 100|CHANGE:          0(01000000 11000000 11000000)|@ 1940
STATE:4|N STATE: 4|COLLECTED:        325(00110000 10100100 10010010)|ITEM: 01000|AMOUNT: 100|CHANGE:          0(01000000 11000000 11000000)|@ 2060
STATE:4|N STATE: 4|COLLECTED:        350(00110000 10010010 11000000)|ITEM: 01000|AMOUNT: 100|CHANGE:          0(01000000 11000000 11000000)|@ 2180
STATE:4|N STATE: 6|COLLECTED:        360(00110000 10000010 11000000)|ITEM: 01000|AMOUNT: 100|CHANGE:          0(01000000 11000000 11000000)|@ 2300
STATE:6|N STATE: 6|COLLECTED:        360(00110000 10000010 11000000)|ITEM: 01000|AMOUNT: 100|CHANGE:          0(01000000 11000000 11000000)|@ 2309
STATE:6|N STATE: 0|COLLECTED:        360(00110000 10000010 11000000)|ITEM: 00000|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 2420
STATE:0|N STATE: 0|COLLECTED:          0(01000000 11000000 11000000)|ITEM: 00000|AMOUNT: 001|CHANGE:          0(01000000 11000000 11000000)|@ 2429
$finish called from file "testbench.v", line 107.
$finish at simulation time                 4000
           V C S   S i m u l a t i o n   R e p o r t
Time: 4000
CPU Time:      0.200 seconds;       Data structure size:   0.0Mb
Wed Dec  4 00:29:17 2019
```

Figure 6 Simulation Result

6 Waveform

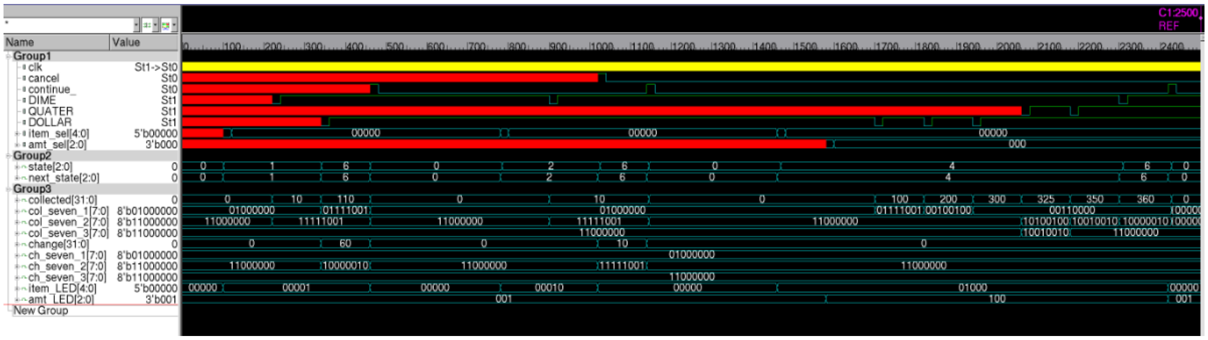


Figure 7 Waveform

7 Conclusion

In this project, our team learned how to work as a team to tackle tough problems. We also learned how to use Verilog to design and debug the FPGA board. We put what we learn in the classroom into a practical project by using the software provided in the EE289 Lab. Our team not just simulated the schematic and waveforms as the instruction given in class we also figured out how to read the DE10-Lite Board handbook and connect the designed pin to the real FPGA board. During the project, our FPGA board fail to work many times, and we have to spend a long time working on the debugging phase, and in the end, the board is working incredibly fine, which makes us feel so rewarding.

Appendix

I Individual Contributions

I-Da (Yida) Chung[013962689]: Vending Machine design and debug.
Yang Liu [013849784]: Vending Machine verification and keyboard design.
Zaixin Mu[012527450]: Hardware design and report revise.

II References

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