JL11x1 Datasheet

Fast Ethernet PHY

Doc No.: DS008-JL11x1-v1.10 (Apr 9, 2021)

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Chapter 1. Overview

The JL11x1 is a Fast Ethernet PHY Transceiver. It is small form factor required for space sensitive applications in embedded systems.

The JL11x1 offers performance far exceeding the IEEE specifications, with superior interoperability and industry leading performance beyond 200 meters of Cat-V cable. The JL11x1 also offers Auto-MDIX to remove cabling complications. JL11x1 has superior ESD protection, greater than 8 kV Human Body Model, providing extremely high reliability and robust operation, ensuring a high-level performance in all applications.

The JL11x1 is offered in small QFN 32-pin package and is ideal for surveillance industry, industrial controls, building/factory automation, transportation, test equipment and wireless base stations.

1.1. Feature List

- 100Base-TX IEEE 802.3u Compliant
- 10Base-T IEEE 802.3 Compliant
- Supports MII mode
- Supports RMII mode
- Full/Half Duplex Operation
- Twisted pair or Fiber mode output
- Supports Auto-Negotiation
- Supports Power Down mode
- Supports Link Down Power Saving
- Supports Base Line Wander (BLW) compensation
- Supports Auto-MDIX
- Supports Interrupt function
- Supports Wake-On-LAN (WOL)
- Adaptive Equalization
- Automatic Polarity Correction
- LEDs for Network Status
- Supports 25MHz External Crystal or OSC
- Supports 50MHz External OSC Clock Input
- Provides 50MHz Clock Source for MAC
- 32-pin MII/RMII QFN 5mm × 5mm Package
- Low Power Consumption
  - 116 mW for 100Base-TX

- 3.3V/2.5V/1.8V MAC Interface VDDIO power supply
- Single 3.3V power supply use integrated LDO or external 1.2V supply for DVDD

1.2. Applications

- Video Surveillance
- Industrial controls and Industrial automation
- Power Acquisition System
- Access Control System

1.3. Device Features Comparisons

Features	JL1111	JL1101
RMII to Copper	Yes	Yes
MII to Copper	Yes	Yes
RMII to Fiber	Yes	Yes
MII to Fiber	Yes	Yes
IEEE 802.3az EEE	Yes	Yes
Reference Clocks	25MHz/50MHz	25MHz/50MHz
Wake on Lan(WoL)	Yes	Yes
I/O voltage(DVDDIO)	3.3V/2.5V/1.8V	3.3V/2.5V/1.8V
Disable Internal LDO	Yes	No
Temperature Grade	C/I/E	C
Package	32-pin QFN, 5 mm x 5 mm	32-pin QFN, 5 mm x 5 mm

Chapter 2. Revision History

Revision	Date	Details
1.05	2020-Oct-29	• Describe differences between JL1101 and JL1111 • Fixbug: EN_DLDO should be 1 when use external 1.2V power supply. • Other minor typo fix.
1.06	2020-Nov-09	• Strap: fix PHY Address strap pin description. • Update loopback latency for 100Base-X and 10Base-T.
1.07	2020-Nov-10	• MMD: EEE Advertise default is 0 • Package diagram is top view • Add Clock Requirements
1.08	2020-Dec-3	• Fix package outline figure. • Update order information diagram.
1.09	2020-Dec-23	• JL1101 also support 2.5/1.8V DVDDIO power supply. • Update RMS Jitter Requirements. • MDC/MDIO are internal pulled-up.
1.10	2021-Apr-09	• Add DC Characteristics: V_{OH} V_{OL} V_{IH} V_{IL} I_{IH} I_{IL}. • Change the DVDDIO DVDD1V2 AVDD3V3 OtherIOs description in Absolute Maximum Ratings table • Remove Load Capacitance Conditon "Duty Cycle" in 25MHz Crystal Specification table • Remove $V_{ODiffSym}$ Unit from MDI PMD Output Characteristics table • Remove the RX_DV function description in RMII bus • Split Mac data interface to two table include "MII Interface table" and "RMII Interface tabel" • Edit the description of "Signal Quality Indicator" in register "INTSQI", from "higher is better" to "lower is better"

Chapter 3. Pin Configuration and Functions

3.1. Package Pin Assignments

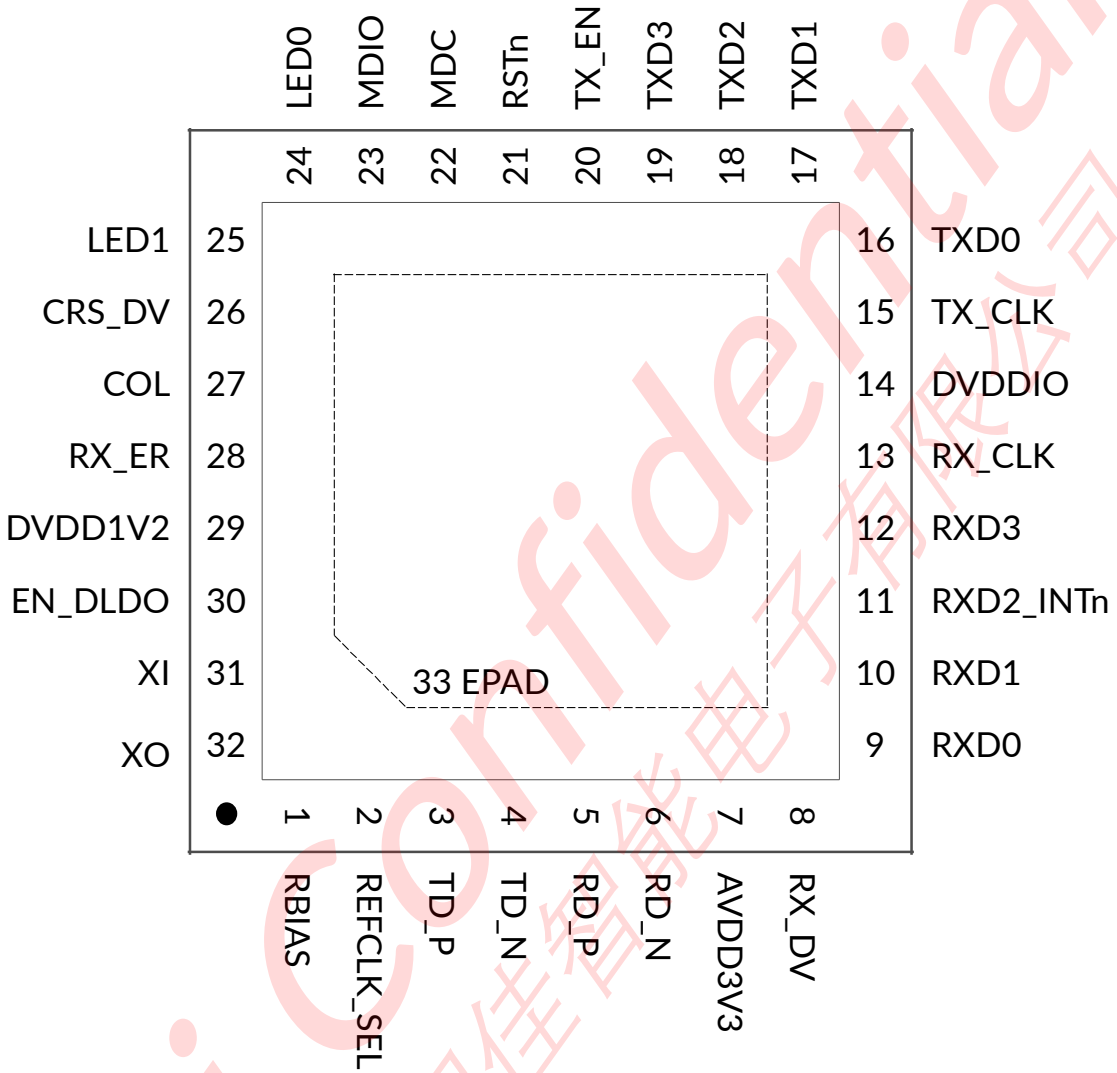


Figure 1. Package 32-Pin (Top View)

Table 1. Package Pin Assignments

Pin No.	Pin Name	Type	Strap	Description
1	RBIAS	I		Transmit Bias Resistor Connection
2	REFCLK_SEL	I	50/25MHz RefClk Selection	Reference Clock Input Selection
3	TD_P	I/O		Transmit Output
4	TD_P	I/O		Transmit Output

Pin No.	Pin Name	Type	Strap	Description
5	RD_P	I/O		Receive input
6	RD_N	I/O		Receive input
7	AVDD3V3	P		3.3V Analog Power Supply
8	RX_DV	LI/O	MII/RMII Selection	Receive Data Valid
9	RXD0	O		Receive Data
10	RXD1	LI/O	LED/WOL Selection	Receive Data
11	RXD2_INTn	O		Receive Data
12	RXD3	LI/O	RMII Clock Direction	Receive Data
13	RX_CLK	O		Receive Clock
14	DVDDIO	P		Digital I/O Power Supply
15	TX_CLK	O		MII TX_CLK output or RMII REFCLK input/output
16	TXD0	I		Transmit Data
17	TXD1	I		Transmit Data
18	TXD2	I		Transmit Data
19	TXD3	I		Transmit Data
20	TX_EN	I		Transmit Enable
21	RSTn	I		PHY Reset, Active Low
22	MDC	I		Management Data Clock
23	MDIO	I/O		Management Data Input/ Output
24	LED0	O	PHYAD[0]	LED0
25	LED1	O	PHYAD[1]	LED1
26	CRS_DV	O		Carrier Sense/Receive Data Valid
27	COL	O		Collision Detect
28	RX_ER	LI/O		Receive Error, 1:Fiber mode 0:UTP mode
29	DVDD1V2	P		1.2V Digital Power Supply
30	EN_DLDO	I	DLDO 1.2V Enable	3.3V Digital LDO Enable
31	XI	I		25MHz Crystal Input
32	XO	I/O		25MHZ Crystal Input
33	EPAD	GND		Ground

3.1.1. Serial Management Interface

Table 2. Serial Management Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
MDC	22	I/PU	Management Data Clock: Synchronous clock to the MDIO management data input/output serial interface which may be asynchronous to transmit and receive clocks. The maximum clock rate is 12.5 MHz with no minimum clock rate.

PIN NAME	PIN NO.	I/O	DESCRIPTION
MDIO	23	I/O/PU	Management Data Input/ Output: Bi-directional management instruction/ data signal that may be sourced by the station management entity or the PHY.

3.1.2. MAC Data Interface

Table 3. MII Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
TX_CLK	15	I/O	MII TRANSMIT CLOCK: 25MHz transmit clock output in 100Mbps mode or 2.5 MHz in 10Mbps mode.
TX_EN	20	I	MII TRANSMIT ENABLE: Active high input indicates the presence of valid data inputs on TXD[3:0].
TXD0	16	I	MII TRANSMIT DATA: Transmit data MII input pins, TXD[3:0], that accept data synchronous to the TX_CLK (2.5 MHz in 10Mbps mode or 25 MHz in 100Mbps mode).
TXD1	17		
TXD2	18		
TXD3	19		
RX_CLK	13	O	MII RECEIVE CLOCK: Provides the 25MHz recovered receive clocks for 100Mbps mode and 2.5 MHz for 10Mbps mode.
RX_DV	8	O, LI, PD	MII RECEIVE DATA VALID: Asserted high to indicate that valid data is present on the corresponding RXD[3:0].
RX_ER	28	O, LI, PD	MII RECEIVE ERROR: Asserted high synchronously to RX_CLK to indicate that an invalid symbol has been detected.
RXD0	9	O	MII RECEIVE DATA: Nibble-wide receive data signals driven synchronously to the RX_CLK (25 MHz for 100Mbps mode, 2.5 MHz for 10Mbps mode). RXD[3:0] signals contain valid data when RX_DV is asserted.
RXD1	10	O, LI, PD	
RXD2_INTn	11	O	
RXD3	12	O, LI, PD	
CRS_DV	26	O	MII CARRIER SENSE: Asserted high to indicate the receive medium is non-idle.
COL	27	O	MII COLLISION DETECT: Asserted high to indicate detection of a collision condition (simultaneous transmit and receive activity) in 10Mbps and 100Mbps Half Duplex Modes.

Table 4. RMII Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
TX_CLK	15	I/O	RMII REFERENCE CLOCK: 50MHz input or output for both transmit and receive in RMII mode.
TX_EN	20	I	RMII TRANSMIT ENABLE: Active high input indicates the presence of valid data on TXD[1:0].
TXD0	16	I	RMII TRANSMIT DATA: Transmit data RMII input pins, TXD[1:0], that accept data synchronous to the 50MHz RMII reference clock (pin TX_CLK).
TXD1	17		
RXD0	9	O	RMII RECEIVE DATA: 2-bits receive data signals, RXD[1:0], driven synchronously to the RMII reference clock (pin TX_CLK), 50 MHz. RXD2_INTn will could be configured to interrupt pin when RMII mode is enabled.
RXD1	10	O, LI, PD	
CRS_DV	26	O	RMII CARRIER SENSE/RECEIVE DATA VALID: This signal combines the RMII Carrier and Receive DataValid indications. For a detailed description of this signal, see the RMII Specification.

3.1.3. Clock Interface

Table 5. Clock Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
XI	31	I	25MHz crystal input or 25MHz/50MHz external oscillator clock input
XO	32	I/O	25MHz crystal output

3.1.4. LED Interface

Table 6. LED Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
LED0	24	O, LI, PU	LED0
LED1	25	O, LI, PD	LED1

3.1.5. Reset

Table 7. Reset

PIN NAME	PIN NO.	I/O	DESCRIPTION
RSTn	21	I	Active Low Chip Reset

3.1.6. Strap Options

Table 8. Strap Options

PIN NAME	PIN NO.	I/O	DESCRIPTION
RXDV	8	O, LI, PD	0: MII, 1: RMII mode
RXD1	10	O, LI, PD	0: LED, 1: WOL
LED0	24	O, LI, PU	PHY address will be set to 00000 to 00011
LED1	25	O, LI, PD	
RXD3	12	O, LI, PD	0: RMII TXCLK output, 1: RMII TXCLK input
RX_ER	28	O, LI, PD	0: UTP Mode, 1: Fiber Mode
EN_DLDO	30	I, PU	0: Pulled-down to Ground will use external 1.2V power supply, internal DLDO will be disabled, 1: Pulled-up to AVDD3V3 or floating will enable internal 1.2V LDO for digital
REFCLK_SEL	2	I, PU	0: 50MHz, 1: 25MHz

3.1.7. 10Mbps and 100Mbps PMD Interface

Table 9. 10Mbps and 100Mbps PMD Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
TD_P	3	IO	Differential common driver transmit output (PMD Output Pair). These differential outputs are automatically configured to either 10BASE-T or 100BASE-TX signaling. In Auto-MDIX mode of operation, this pair can be used as the Receive Input pair. 100Base-FX also share the pins to connect to the fiber module.+ These pins require 3.3V bias for operation.
TD_N	4	IO	
RD_P	5	IO	Differential receive input (PMD Input Pair). These differential inputs are automatically configured to accept either 100BASE-TX or 10BASE-T signaling. In Auto-MDIX mode of operation, this pair can be used as the Transmit Output pair. 100Base-FX also share the pins to connect to the fiber module.+ These pins require 3.3V bias for operation.
RD_N	6	IO	

3.1.8. Power Supply Pins

Table 10. Power Supply Pins

PIN NAME	PIN NO.	I/O	DESCRIPTION
AVDD3V3	7	P	3.3V Analog Power Input
DVDDIO	14	P	Digital I/O Power Input
DVDD1V2	29	P	1.2V Digital Power Output
EPAD	33	GND	Ground

3.1.9. Special Connections

Table 11. Special Connections

PIN NAME	PIN NO.	I/O	DESCRIPTION
RBIAS	1	I	Transmit Bias Resistor Connection. A 2.49kΩ 1% resistor should be connected from RBIAS to GND

Chapter 4. Specifications

4.1. Absolute Maximum Ratings

		MIN	MAX	UNIT
DVDDIO	Digital IO supply voltage	-0.5	3.63	V
DVDD1V2	Digital core supply voltage	-0.5	1.32	V
AVDD3V3	Analog supply voltage	-0.5	3.63	V
Other IOs	Other input pins withstand voltage	-0.5	3.63	V
$T_{Storage}$	Storage temperature		150	°C
$T_{Junction}$	Operating junction temperature	-40	125	°C
T_{Lead}	Lead temperature (soldering 10 seconds)		260	°C
T_{FL}	Floor Life (25°C/60% RH)		168	Hours

4.2. ESD Ratings

ESD Requirements	NOTE	VALUE	UNIT
Human Body Model (ANSI/ESDA/JEDEC JS-001-2017)	For MDI Pins	> 8000	V
	For non-MDI Pins	2000	
Charge Device Model (ANSI/ESDA/JEDEC JS-002-2014)	/	500	

4.3. Recommended Operating Conditions

	Description	MIN	MAX	UNIT
V_{CC} (AVDD3V3)	Analog Supply Voltage	2.97	3.63	V
V_{CC} (DVDDIO, 3.3V Mode)	Digital I/O Supply Voltage	2.97	3.63	V
V_{CC} (DVDDIO, 2.5V Mode)	Digital I/O Supply Voltage	2.25	2.75	V
V_{CC} (DVDDIO, 1.8V Mode)	Digital I/O Supply Voltage	1.71	1.89	V
V_{CC} (DVDD1V2)	Digital Core Supply Voltage with Internal DLDO Disabled	1.14	1.26	V
$T_{Operation}$	Ambient operating temperature ++	-40	105	°C
$T_{Junction}$	Maximum junction temperature	-40	125	

++: JL1101 only support 0~70°C

4.4. Oscillator and Crystal Requirements

Table 12. 25MHz Oscillator Specification

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
Frequency		25		MHz	
Frequency Tolerance			±50	ppm	Operational Temp

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
Frequency Stability			±50	ppm	5 year aging
Rise/Fall Time			6	nsec	10% - 90%
Cycle to Cycle Jitter			500	ps	short term (peak to peak value)
RMS Jitter(1)			100	ps	long term (RMS value)
Symmetry	40%		60%		Duty Cycle

Note:

1. integrated range from 10kHz to 12.5MHz

Table 13. 50MHz Oscillator Specification

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
Frequency		50		MHz	
Frequency Tolerance			±50	ppm	Operational Temp
Frequency Stability			±50	ppm	5 year aging
Rise/Fall Time			3	nsec	10% - 90%
Cycle to Cycle Jitter			500	ps	short term (peak to peak value)
RMS Jitter(1)			100	ps	long term (RMS value)
Symmetry	40%		60%		Duty Cycle

Note:

1. integrated range from 10kHz to 25MHz

Table 14. 25MHz Crystal Specification

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
Frequency		25		MHz	
Frequency Tolerance			±50	ppm	Operational Temp
Frequency Stability			±50	ppm	5 year aging
Load Capacitance	6		27	pF	

4.5. Power consumption

Table 15. Power consumption

DVDD1V2 Power Supply Source	DVDDIO Power Supply Voltage	Power Consumption @ 100Base-TX	Power Consumption @ 10Base-T	Power Consumption @ 10Base-Te
Internal LDO (EN_ELDO = 1)	3.3 V	174 mW	188 mW	162 mW
External LDO (EN_ELDO = 0)	3.3 V	150 mW	173 mW	
External LDO (EN_ELDO = 0)	2.5 V	127 mW	154 mW	

DVDD1V2 Power Supply Source	DVDDIO Power Supply Voltage	Power Consumption @ 100Base-TX	Power Consumption @ 10Base-T	Power Consumption @ 10Base-Te
External LDO (EN_ELDO = 0)	1.8 V	116 mW	142 mW	

Note:

1. May varies with PCB trace loading
2. Test under full activities.

4.6. DC Specifications

PARAMETER		MIN	TYP	MAX	UNITS	CONDITION
DVDDIO 3.3V Mode DC Characteristics						
V_{OH}	High Level Output Voltage	2.4			V	I_{OH}=-12mA DVDDIO=3.3V±10%
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL}=12mA DVDDIO=3.3V±10%
V_{IH}	High Level Input Voltage	1.7			V	DVDDIO=3.3V±10%
V_{IL}	Low Level Input Voltage			0.8	V	DVDDIO=3.3V±10%
I_{IH}	Input High Current	-120		120	μA	VIN=DVDDIO
I_{IL}	Input Low Current	-120		120	μA	VIN=GND
$V_{IH(Reset)}$	Reset Pin Relese Voltage	2.85			V	DVDDIO=3.3V±10%
$V_{IL(Reset)}$	Reset Pin Reset Voltage			1.2	V	DVDDIO=3.3V±10%
DVDDIO 2.5V Mode DC Characteristics						
V_{OH}	High Level Output Voltage	2.0			V	I_{OH}=-12mA DVDDIO=2.5V±5%
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL}=12mA DVDDIO=2.5V±5%
V_{IH}	High Level Input Voltage	1.5			V	DVDDIO=2.5V±5%
V_{IL}	Low Level Input Voltage			0.7	V	DVDDIO=2.5V±5%
I_{IH}	Input High Current	-80		80	μA	VIN=VDDIO
I_{IL}	Input Low Current	-80		80	μA	VIN=GND
$V_{IH(Reset)}$	Reset Pin Relese Voltage	2.05			V	DVDDIO=2.5V±5%
$V_{IL(Reset)}$	Reset Pin Reset Voltage			1.0	V	DVDDIO=2.5V±5%
DVDDIO 1.8V Mode DC Characteristics						
V_{OH}	High Level Output Voltage	1.4			V	I_{OH}=-6mA DVDDIO=1.8V±5%
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL}=6mA DVDDIO=1.8V±5%
V_{IH}	High Level Input Voltage	1.3			V	DVDDIO=1.8V±5%
V_{IL}	Low Level Input Voltage			0.5	V	DVDDIO=1.8V±5%
I_{IH}	Input High Current	-40		40	μA	VIN=DVDDIO

PARAMETER		MIN	TYP	MAX	UNITS	CONDITION
I_{IL}	Input Low Current	-40		40	μA	VIN=GND
$V_{IH(Reset)}$	Reset Pin Relese Voltage	1.45			V	DVDDIO=1.8V±5%
$V_{IL(Reset)}$	Reset Pin Reset Voltage			0.7	V	DVDDIO=1.8V±5%
DC Characteristics						
$I_{IH(Reset)}$	Reset Pin Input High Current	-1		1	μA	VIN=DVDDIO
$I_{IL(Reset)}$	Reset Pin Input Low Current	-1		1	μA	VIN=GND

4.7. AC Specifications

4.7.1. Power Up and Reset Timing

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	First SMI command send to JL11x1 after all power up requirements are met, power up requirements include: 1. AVDD3V3 is ready 2. DVDD1V2 is ready, only when use external 1.2V power supply (EN_DLDO = 0) 3. DVDDIO is ready 4. RSTn has been deasserted	5			ms
t_2	Assert RSTn pin to low to reset the JL11x1 should be stable for mininal of 200 ns.	200			ns

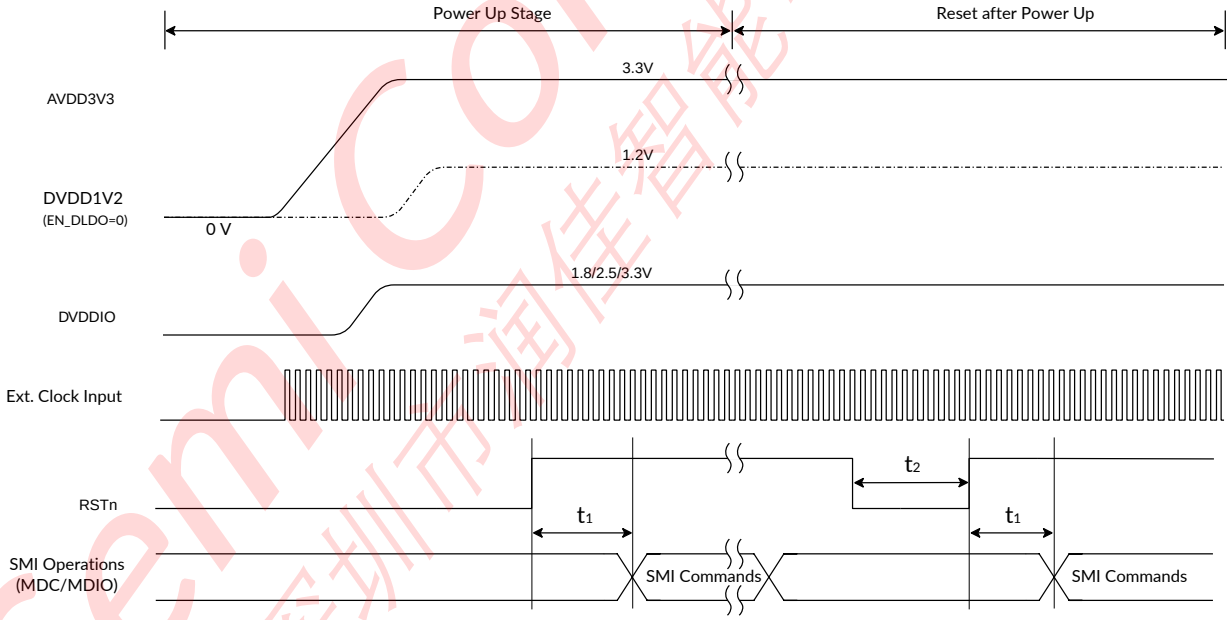


Figure 2. Power Up Sequence

4.7.2. Serial Management Interface(SMI) Timing

DESCRIPTION	MIN	TYP	MAX	UNIT
MDC to MDIO (output) delay time	0		60	ns
MDIO (input) to MDC setup time	10			ns
MDIO (input) to MDC hold time	10			ns
MDC frequency			12.5	MHz

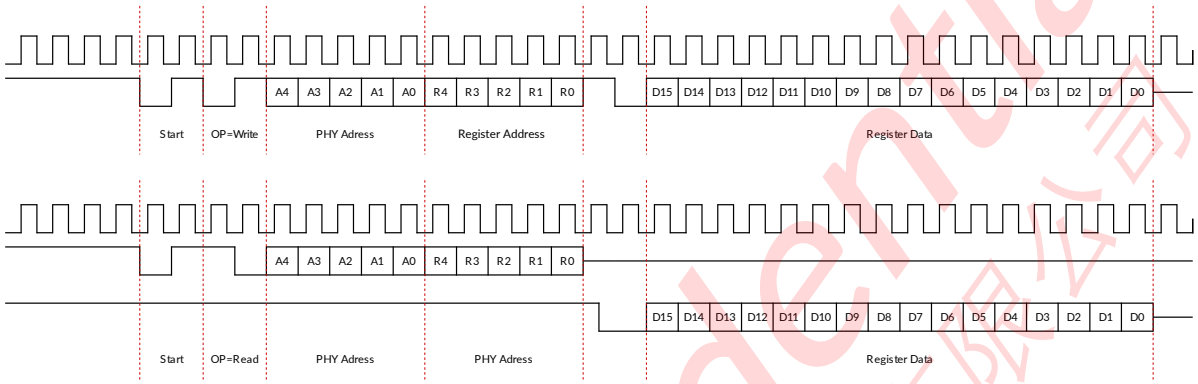


Figure 3. SMI Timing

4.7.3. MDI PMD Output Characteristics

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{ODiff}	MDI 10Base-T	4.4	4.8	5.2	V_{pp}
V_{ODiff}	MDI 100Base-TX	1.9	2.0	2.1	V_{pp}
$V_{ODiffSym}$	MDI 100Base-TX voltage symmetry	98%	100%	102%	
V_{ODiff}	MDI 100Base-FX	0.6	0.8	1.0	V_{pp}

4.7.4. 100Mbps MII Transmit Timing

PARAMETER	DESCRIPTION	NOTES	MIN	TYP	MAX	UNIT
t_1	TX_CLK high/low time	100Mbps Normal mode	14	20	26	ns
t_2	TXD[3:0], TX_EN data setup to TX_CLK	100Mbps Normal mode	10			ns
t_3	TXD[3:0], TX_EN data hold from TX_CLK	100Mbps Normal mode	1			ns

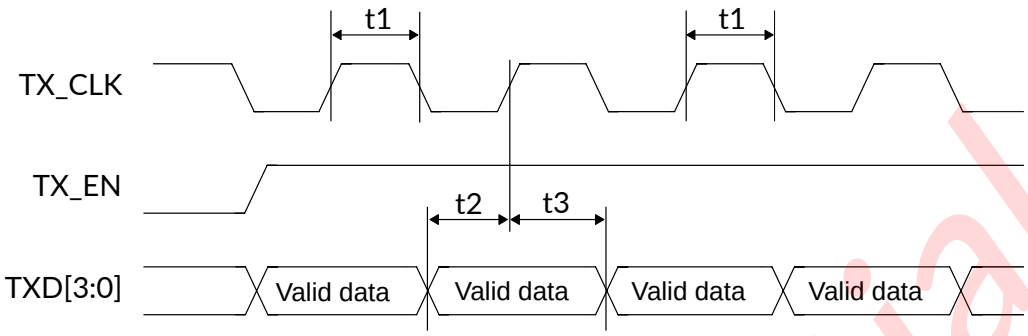


Figure 4. 100-Mbps MII Transmit Timing

4.7.5. 100Mbps MII Receive Timing

PARAMETER	DESCRIPTION	NOTES	MIN	TYP	MAX	UNIT
t_1	RX_CLK high/low time	100Mbps Normal mode	14	20	26	ns
t_2	RX_CLK to RXD[3:0], RX_DV, RX_ER delay	100Mbps Normal mode	10		30	ns

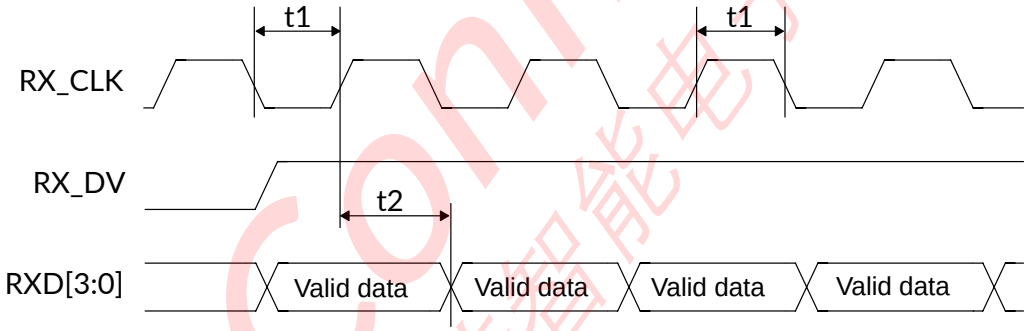


Figure 5. 100-Mbps MII Receive Timing

4.7.6. 100BASE-TX Transmit Packet Latency Timing

PARAMETER	DESCRIPTION	NOTES[1]	MIN	TYP	MAX	UNIT
t_1	TX_CLK to PMD output pair latency	100Mbps Normal mode		9		bits

1. 1 bit time = 10 ns in 100-Mbps mode.

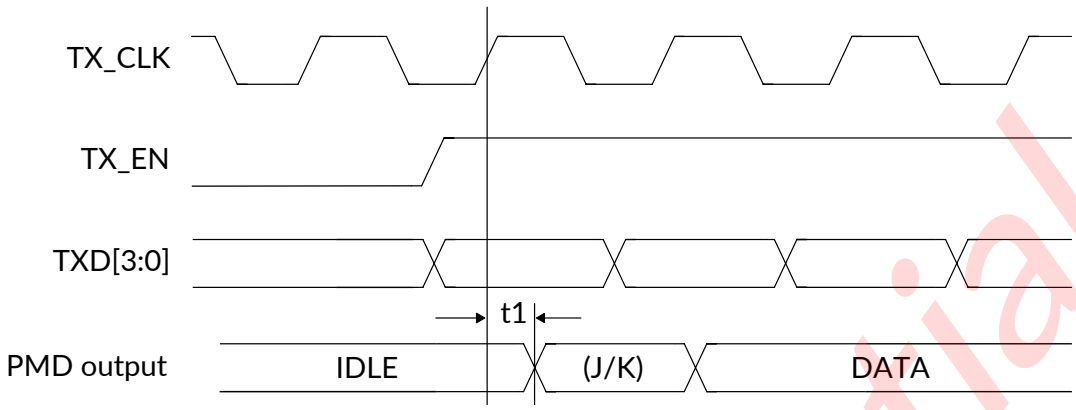


Figure 6. 100BASE-TX Transmit Packet Latency Timing

4.7.7. 100BASE-TX Transmit Packet Deassertion Timing

PARAMETER	DESCRIPTION	NOTES[1]	MIN	TYP	MAX	UNIT
t_1	TX_CLK to PMD output pair deassertion	100Mbps Normal mode		9		bits

1. 1 bit time = 10 ns in 100-Mbps mode.

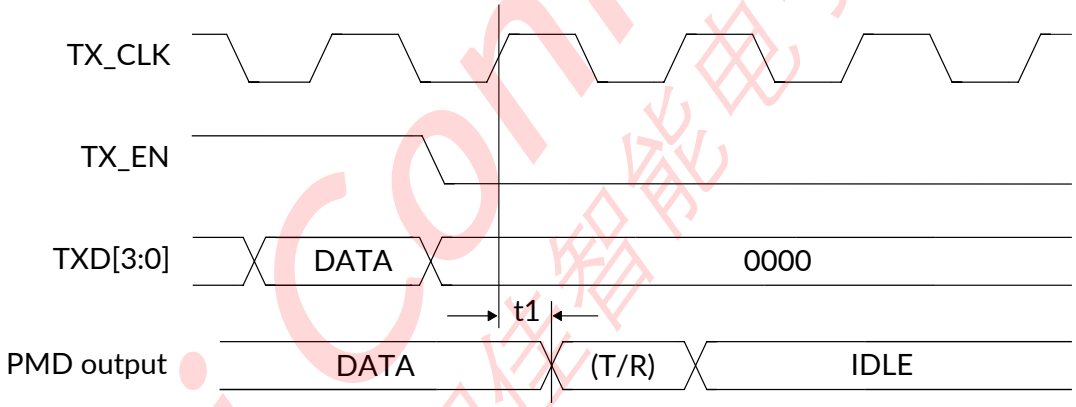


Figure 7. 100BASE-TX Transmit Packet Deassertion Timing

4.7.8. 100BASE-TX Receive Packet Latency Timing

PARAMETER	DESCRIPTION	NOTES	MIN	TYP	MAX	UNIT
t_1	Receive data latency	100Mbps Normal mode		23		bits[1]

1. 1 bit time = 10 ns in 100-Mbps mode.

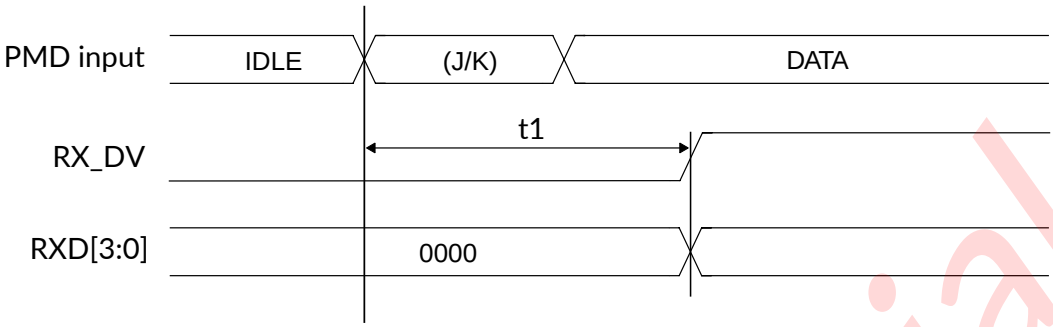


Figure 8. 100BASE-TX Receive Packet Latency Timing

4.7.9. 10Mbps MII Transmit Timing

PARAMETER	DESCRIPTION	NOTES(1)	MIN	TYP	MAX	UNIT
t_1	TX_CLK high/low time	10Mbps MII mode	140	200	260	ns
t_2	TXD[3:0], TX_EN data setup to TX_CLK	10Mbps MII mode	10			ns
t_3	TXD[3:0], TX_EN data hold from TX_CLK	10Mbps MII mode	1			ns

1. An attached Mac should drive the transmit signals using the positive edge of TX_CLK. As shown above, the MII signals are sampled on the falling edge of TX_CLK.

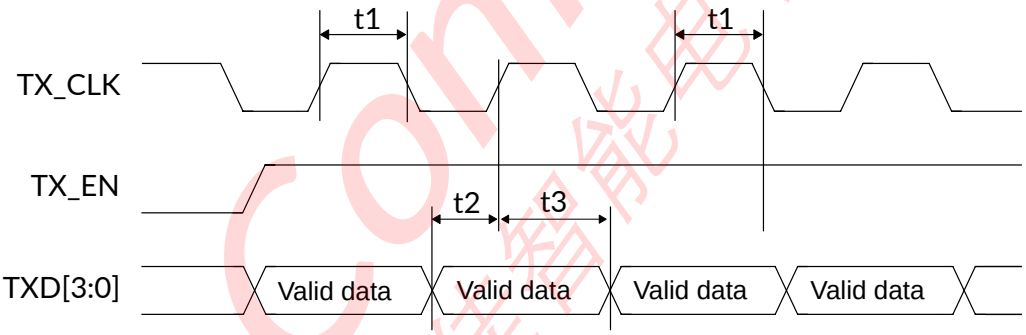


Figure 9. 10Mbps MII Transmit Timing

4.7.10. 10Mbps MII Receive Timing

PARAMETER	DESCRIPTION	NOTES(1)	MIN	TYP	MAX	UNIT
t_1	RX_CLK high/low time		160	200	240	ns
t_2	RX_CLK to RXD[3:0], RX_DV delay	10Mbps MII mode	100		300	ns

1. RX_CLK may be held low for a longer period of time during transition between reference and recovered clocks. Minimum high and low times will not be violated.

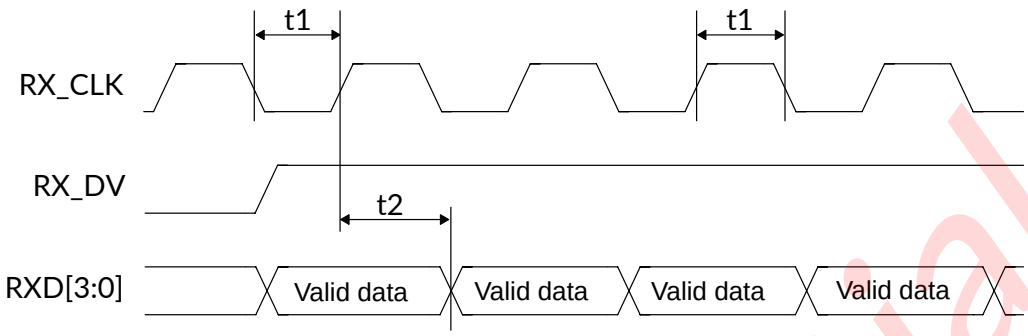


Figure 10. 10Mbps MII Receive Timing

4.7.11. 10BASE-T Transmit Timing (Start of Packet)

PARAMETER	DESCRIPTION	NOTES	MIN	TYP	MAX	UNIT
t_1	Transmit output delay from the falling edge of TX_CLK	10Mbps MII mode		530		ns

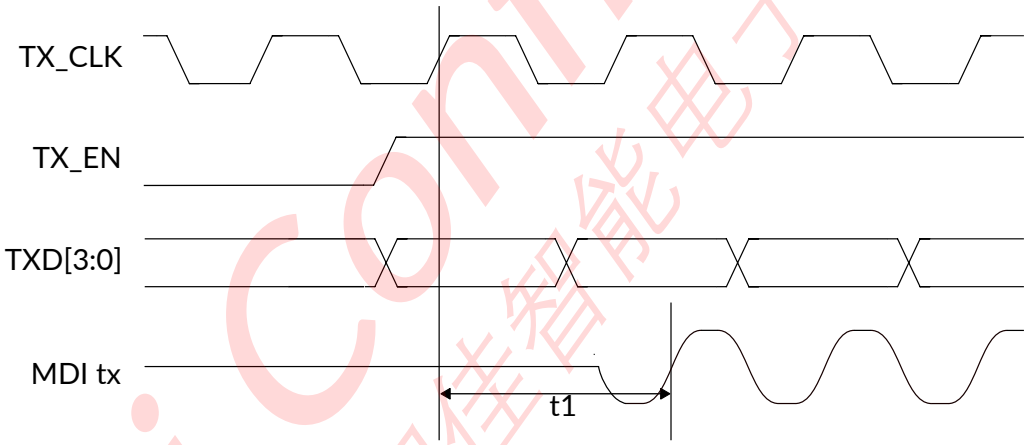


Figure 11. 10Mbps Transmit Start of Packet Timing

4.7.12. 10BASE-T Transmit Timing (End of Packet)

PARAMETER	DESCRIPTION	NOTES	MIN	TYP	MAX	UNIT
t_1	End of packet high time (with '0' ending bit)		250	300		ns
t_2	End of packet high time (with '1' ending bit)		250	300		ns

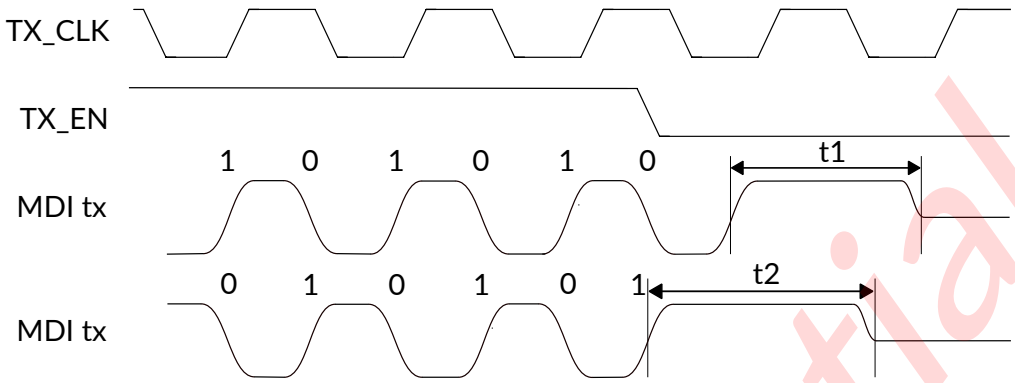


Figure 12. 10base-T Transmit End of Packet Timing

4.7.13. 10BASE-T Receive Timing (Start of Packet)

PARAMETER	DESCRIPTION	NOTES[1] [2]	MIN	TYP	MAX	UNIT
t_1	RX_DV latency			8000		ns

1. 10BASE-T RX_DV Latency is measured from first bit of preamble on the wire to the assertion of RX_DV.
2. 1 bit time = 100 ns in 10Mbps mode.

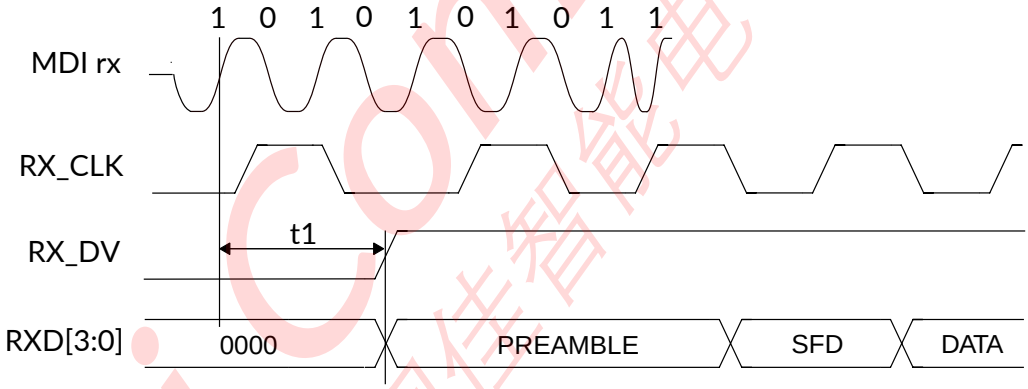


Figure 13. 10base-T Receive Start of Packet Timing

4.7.14. 10Mbps Jabber Timing

PARAMETER	DESCRIPTION	NOTES	MIN	TYP	MAX	UNIT
t_1	Jabber activation time			100		ms
t_2	Jabber deactivation time			500		ms

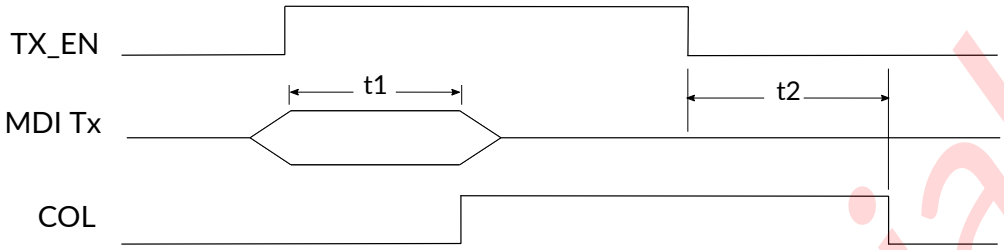


Figure 14. 10base-T Jabber Timing

4.7.15. 10BASE-T Normal Link Pulse Timing

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	Pulse width		100		ns
t_2	Pulse period		16		ms

1. These specifications represent transmit timing.

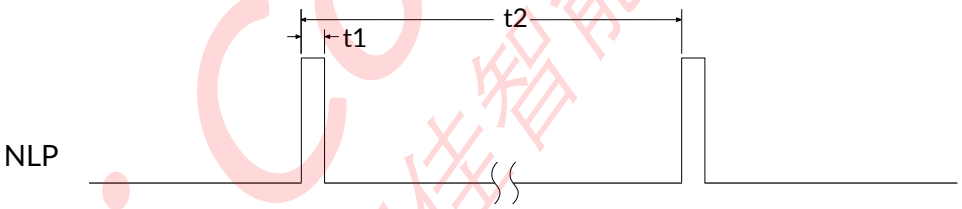


Figure 15. 10base-T Normal Link Pulse Timing

4.7.16. Auto-Negotiation Fask Link Pulse (FLP) Timing

PARAMETER	DESCRIPTION	NOTES	MIN	TYP	MAX	UNIT
t_1	Clock, data pulse width			100		ns
t_2	Clock pulse to clock pulse period			126		µs
t_3	Clock pulse to data pulse period	Data = 1		63		µs
t_4	Burst width			2		ms

PARAMETER	DESCRIPTION	NOTES	MIN	TYP	MAX	UNIT
t_5	FLP burst to FLP burst perio			16		ms

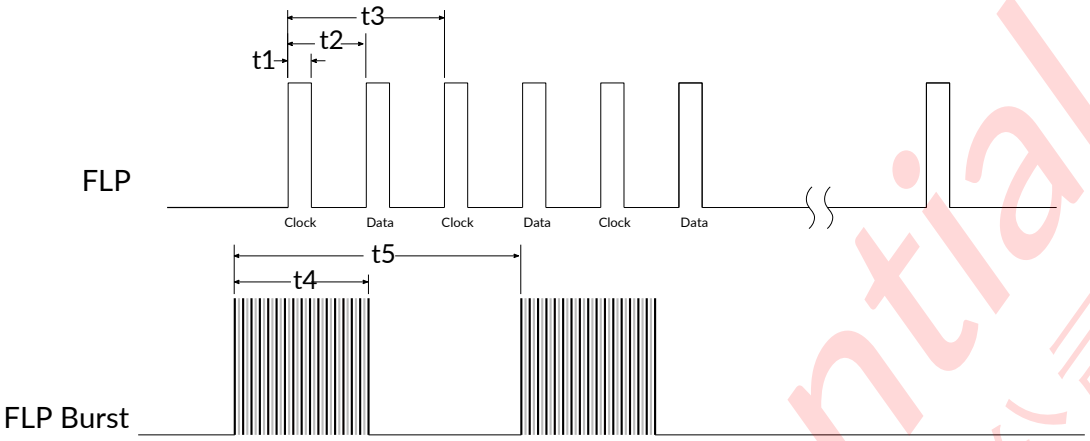


Figure 16. Auto-Negotiation Fast Link Pulse (FLP) Timing

4.7.17. 100Mbps Internal Loopback Timing

PARAMETER	DESCRIPTION	NOTES[1] [2]	MIN	TYP	MAX	UNIT
t_1	TX_EN to RX_DV loopback	100Mbps internal loopback mode			450	ns

1. Due to the nature of the descrambler function, all 100BASE-TX Loopback modes will cause an initial dead time of up to 550 µs, during which no data will be present at the receive MII outputs. The 100BASE-TX timing specified is based on device delays after the initial 550-µs dead time.
2. Measurement is made from the first rising edge of TX_CLK after assertion of TX_EN.

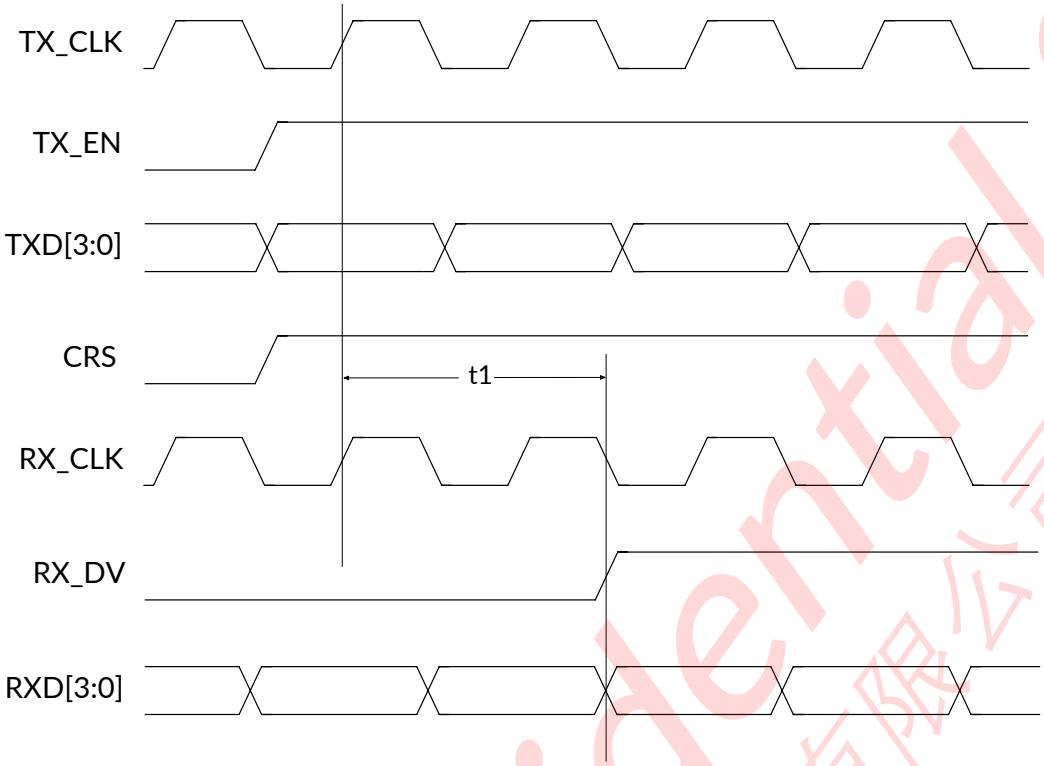


Figure 17. 100Mbps Internal Loopback Timing

4.7.18. 10Mbps Internal Loopback Timing

PARAMETER	DESCRIPTION	NOTES(1)	MIN	TYP	MAX	UNIT
t_1	TX_EN to RX_DV loopback	10Mbps internal loopback mode			11	μs

1. Measurement is made from the first rising edge of TX_CLK after assertion of TX_EN.

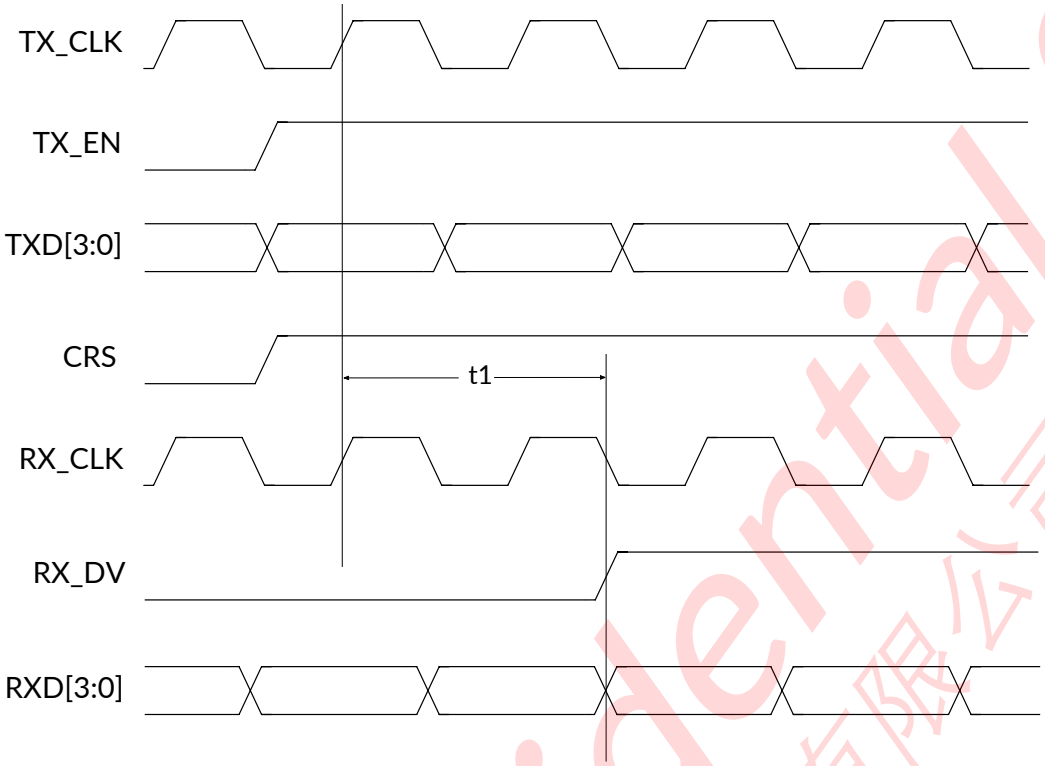


Figure 18. 10Mbps Internal Loopback Timing

4.7.19. RMII Transmit Timing

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	REFCLK(pin TX_CLK) clock period		20		ns
t_2,t_3	REFCLK(pin TX_CLK) clock duty cycle	35	50	65	%
t_4	TXD[1:0], TX_EN, data setup to REFCLK(pin TX_CLK) rising	5			ns
t_5	TXD[1:0], TX_EN, data hold from REFCLK(pin TX_CLK) rising	2			ns

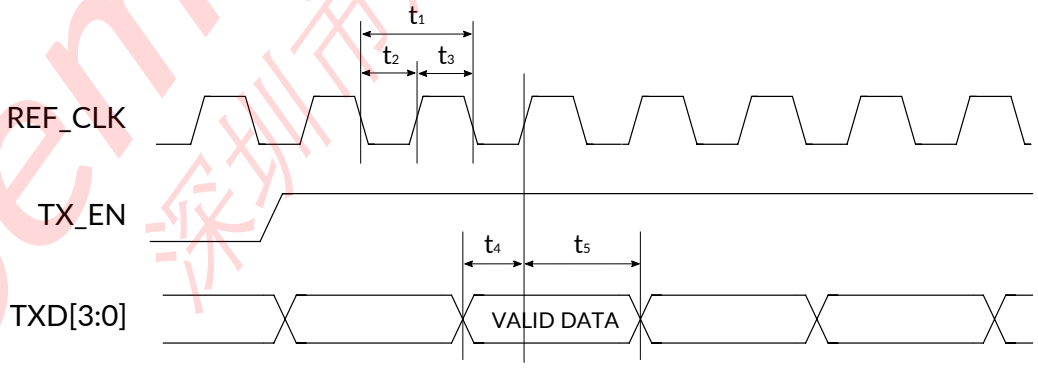


Figure 19. RMII Transmit Timing

4.7.20. RMII Receive Timing

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	REFCLK(pin TX_CLK) clock period		20		ns
t_2,t_3	REFCLK(pin TX_CLK) clock duty cycle	35	50	65	%
t_4	RXD[1:0], CRS_DV output delay from REFCLK(pin TX_CLK) rising	2		16	ns

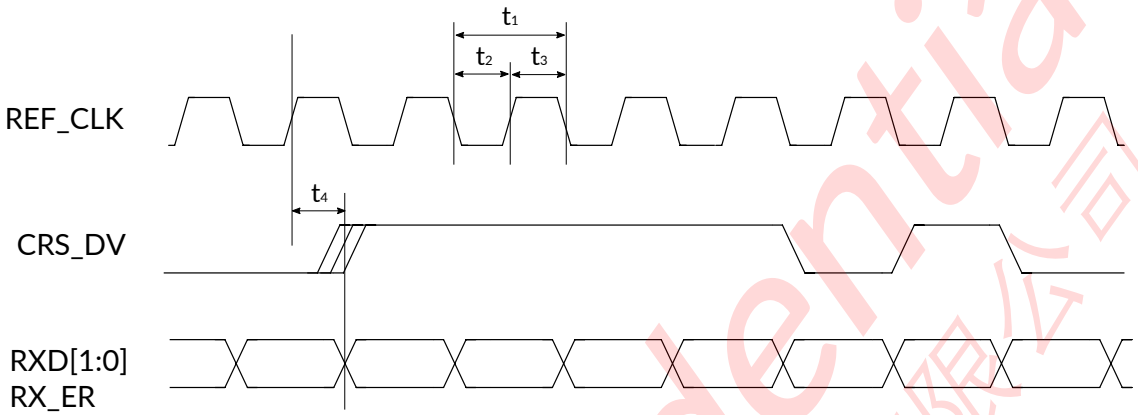


Figure 20. RMII Receive Timing

Chapter 5. Functional Description

5.1. Overview

5.2. Functional Block Diagram

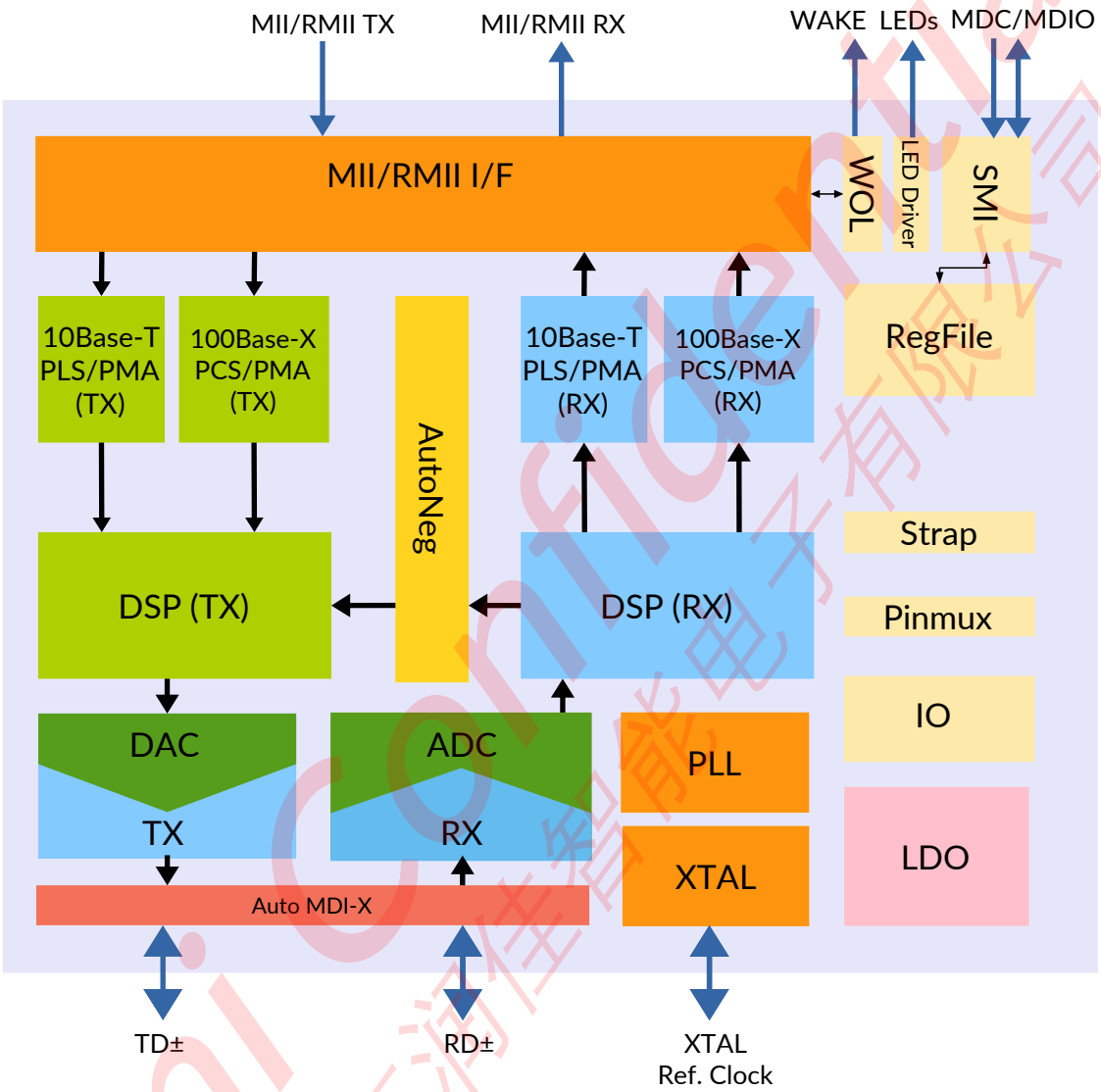


Figure 21. Functional Block Diagram

5.3. Feature Description

5.3.1. Auto-Negotiation

Auto-Negotiation function is to exchange information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities, refer to Clause 28 of the IEEE 802.3u specification.

The basic mechanism to achieve Auto-Negotiation is to pass information encapsulated within a burst of closely spaced link integrity test pulses that individually meet the 10BASE-T Transmitter Waveform for Link Test Pulse. This burst of pulses is referred to as a Fast Link Pulse (FLP) Burst.

The Auto-Negotiation function allows the devices to switch between the various operational modes in an ordered fashion, permits management to disable or enable the Auto-Negotiation function, and allows management to select a specific operational mode. The Auto-Negotiation function also provides a Parallel Detection function to allow 10BASE-T and 100BASE-TX compatible devices to be recognized, even though they may not provide Auto-Negotiation.

5.3.2. LED Functional

The JL11x1 supports two configurable LED pins. The Device supports LED's Link, Speed and Activity configurations. Functions are controlled through Page 7 Register 19, bits[5:4]

LED Functional Selection	00	01	10	11 (Default)
LED0	Blink for 10/100 Activity	On for 10/100 Link/Blink for 10/100 Activity	On for 10 Link/Blink for 10/100 Activity	On for 10 Link/Blink for 10 Activity
LED1	On for 100 Link	On for 100 Link	On for 100 Link	On for 100 Link/Blink for 100 Activity

The PHYAD strap options share the LED output pins, the external combinations required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD strap input upon power-up/reset.

if a given PHYAD input is resistively pulled high then the corresponding output will be configured as an active low driver. if a gien PHYAD input is resistively pulled low then the corresponding output will be configured as an active high driver. the PHY address configuration pins should not be connected to GND or VCC directly, but must be pulled high or low through a resistor (e.g., 4.7KΩ). if no LED indications are needed, the components of the LED path can be removed.

the JL11x1 support EEE blinking mode. this function can be enabled/disabled via Page 7 Register 18, bits[1:0].

When the eee blinking mode is enabled, the LED behave continuous slow blinking in eee idle mode and the LED behave fast and slow blinking on packet transmission and reception in eee active mode.

5.3.3. Auto-MDIX

Automatic MDI/MDI-X Configuration is intended to eliminate the need for crossover cables between similar devices. This implementation complies with the corresponding IEEE 802.3 Auto-Negotiation and Crossover Specifications.

Auto-MDIX is enabled by default and can be configured via register(register 28, page 0), bits [2:1].

5.3.4. Automatic Polarity Correction

JL11x1 suport automatic polarity detection and correction when working at 10Base-T mode. JL11x1 will detect the polarity of Normal Link Pulse (NLP) to derermte the polarity of cable.

100Base-TX and 100Base-FX are non-related to cable polarity.

5.3.5. Reset Operation

JL11x1 supports two types of reset operation: Hardware Reset and Software Reset.

An internal Power-On-Reset circuit has been implemented in JL11x1, assertion of reset is not needed explicitly after power up.

Hardware Reset

A hardware reset is accomplished by asserting the RSTn pin with low level for at least 1 ms. All registers will be reset to default values and the strap configration will be re-latched.

Software Reset

A software reset is accomplished by writing BMCR[15] Reset register to 1. All registers will be reset to default values and the strap configration will NOT be re-latched. Software need wait 100us to start other SMI operation.

5.3.6. Wake-On-LAN (WOL)

Wake-On-LAN provides a mechanism to detect specific frames and notify the connected MAC through either a register status change, or an interrupt flag. Wake-on-LAN is implemented using a specially designed frame called a magic packet. When a qualified WOL frame is received, the JL11x1 WOL logic circuit is able to generate a user-defined event through a status interrupt flag to inform a connected controller that a wake event has occurred.

Magic Packet Structure

When configured for Wake-On-LAN mode, the JL11x1 will check all incoming frames for identifying the Magic Packet frame.

A Magic Packet frame must also meet the basic requirements for the Ethernet Frame.

The specific Magic Packet sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6 bytes of FFh.

Destination (6 bytes)
Source (6 bytes)
MISC (X bytes, X >= 0)
FFFFFFFFFFFF (6 bytes)
Destination*16 (6*16 bytes)
MISC (X bytes, X >= 0)
CRC (4 bytes)

Figure 22. Magic Packet Structure

Chapter 6. Register Descriptions

Table 16. Register Map

Page	Register	Addr	Tag	Desc
0	0	0x0	BMCR	Basic Mode Control Register (Page 0, Register 0, BMCR)
0	1	0x1	BMSR	Basic Mode Status Register (Page 0, Register 1, BMSR)
0	2	0x2	PHYIDR1	PHY Identifier Register 1 (Page 0, Register 2, PHYIDR1)
0	3	0x3	PHYIDR2	PHY Identifier Register 2 (Page 0, Register 3, PHYIDR2)
0	4	0x4	ANAR	Auto-Negotiation Advertisement Register (Page 0, Register 4, ANAR)
0	5	0x5	ANLPAR	Auto-Negotiation Link Partner Ability Register (Page 0, Register 5, ANLPAR)
0	6	0x6	ANER	Auto-Negotiation Expansion Register (Page 0, Register 6, ANER)
0	13	0xD	MMDAC	MMD Access Control Register (Page 0, Register 13, MMDAC)
0	14	0xE	MMDAAD	MMD Access Address Data Register (Page 0, Register 14, MMDAAD)
0	28	0x1C	FMLR	Fiber Mode and Loopback Register (Page 0, Register 28, FMLR)
0	30	0x1E	INTSQI	Interrupt Indicators and Signal Quality Indicator Register (Page 0, Register 30, INTSQI)
0	31	0x1F	PAGESEL	Page Select Register (Page 0, Register 31, PAGESEL)
4	16	0x90	EEECER	EEE Capability Enable Register (Page 4, Register 16, EEECER)
4	21	0x95	EEECR	EEE Capability Register (Page 4, Register 21, EEECR)
7	16	0xf0	RMSR	RMII Mode Setting Register (Page 7, Register 16, RMSR)
7	18	0xf2	LEDER	EEE LEDs Enable Register (Page 7, Register 18, LEDER)
7	19	0xf3	WOLEN	Interrupt WOL Enable and LEDs Function Registers (Page 7, Register 19, WOLEN)

6.1. Basic Mode Control Register (Page 0, Register 0, BMCR)

Field	Name	Type	Default	Desc
15	Reset	SC	0x0	1: PHY reset 0: normal operation
14	Loopback	RW	0x0	This bit enables loopback of transmit data nibbles TXD3:0 to the receive data path. 1: enable loopback mode 0: disable loopback mode
13	Speed Selection [0]	RW	0x1	Speed Selection 1 : 100 Mb/s 0 : 10 Mb/s
12	Auto-Negotiation Enable	RW	0x1	1: Enable auto-negotiation, bits 0:13 and 0:8 will be ignored 0: Disable auto-negotiation, bits 0:13 and 0:8 will determine the link speed and the data transfer mode
11	Power Down	RW	0x0	This bit turns down the power of the PHY chip. The MDC, MDIO is still alive for accessing the MAC. 1: Power down 0: Normal operation

Field	Name	Type	Default	Desc
10	Isolate	RW	0x0	1: Electrically isolate the PHY from MII/RMII PHY is still able to respond to MDC/MDIO. 0: Normal operation
9	Restart AutoNeg	SC	0x0	1: restart Auto-Negotiation process 0: normal operation
8	Duplex Mode	RW	0x1	1: full duplex 0: half duplex
7	Collision Test	RW	0x0	Collision Test. 1: Collision test enabled 0: Normal operation When set, this bit will cause the COL signal to be asserted in response to the TXEN assertion within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the TXEN de-assertion.
6	Speed Selection [1]	RW	0x0	Reserved
5:0	reserved	RW	0x0	Write as 0

6.2. Basic Mode Status Register (Page 0, Register 1, BMSR)

Field	Name	Type	Default	Desc
15	Base100_T4_1	RO	0x0	1: Enable 100Base-T4 support 0: Suppress 100Base-T4 support
14	Base100_TX_FD_1	RO	0x1	1: Enable 100Base-TX full duplex support 0: Suppress 100Base-TX full duplex support
13	Base100_TX_HD_1	RO	0x1	1: Enable 100Base-TX half duplex support 0: Suppress 100Base-TX half duplex support
12	Base10_TX_FD	RO	0x1	1: Enable 10Base-T full duplex support 0: Suppress 10Base-T full duplex support
11	Base10_TX_HD	RO	0x1	1: Enable 10Base-T half duplex support 0: Suppress 10Base-T half duplex support
10:7	Reserved	RO	0x0	Reserved
6	MDIO_MFPS	RO	0x1	
5	AutoNeg Complete	RO	0x0	1: Auto-negotiation process completed 0: Auto-negotiation process not completed
4	Remote Fault	RC	0x0	1: Remote fault condition detected (cleared on read) 0: No remote fault condition detected
3	AutoNeg Ability	RO	0x1	1: PHY is able to perform auto-negotiation 0: PHY is not able to perform auto-negotiation
2	Link Status	RO	0x0	1: Valid link established 0: No valid link established
1	Jabber Detect	RC	0x0	1: Jabber condition detected 0: No jabber condition detected
0	Ext Cap	RO	0x1	1: Extended register capable (permanently=1) 0: Not extended register capable

6.3. PHY Identifier Register 1 (Page 0, Register 2, PHYIDR1)

Field	Name	Type	Default	Desc
15:0	OUI MSB	RO	0x937c	JLSemi OUI is 0x24DF10 0010 0100 1101 1111 0001 0000 bit 1.....bit24 Register 2.[15:0] show bits 3 to 18 of OUI 1001 0011 0111 1100 bit3.....bit18

6.4. PHY Identifier Register 2 (Page 0, Register 3, PHYIDR2)

Field	Name	Type	Default	Desc
15:10	OUI LSB	RO	Always 010000	Organizationally Unique Identifier bits 19:24 01 0000 bit19....bit24
9:4	Model Number	RO	Always 000010	Model Number
3:0	Revision Nnumber	RO	See Desc	Contact JLSemi FAEs for information on the device revision number

6.5. Auto-Negotiation Advertisement Register (Page 0, Register 4, ANAR)

Field	Name	Type	Default	Desc
15	Next Page	RW	0x0	Next Page Bit. 0: Transmitting the primary capability data page 1: Transmitting the protocol specific data page
14	Acknowledge	RO	0x0	1: Acknowledge reception of link partner capability data word 0: Do not acknowledge reception
13	Remote Fault	RO	0x0	1: Advertise remote fault detection capability 0: Do not advertise remote fault detection capability
12	Reserved	RO	0x0	
11	Asymmetric PAUSE	RO	0x0	1: Advertise asymmetric pause support 0: No support of asymmetric pause
10	Pause	RO	0x0	Reserved
9	100Base-T4	RO	0x0	1: 100Base-T4 is supported by local node 0: 100Base-T4 not supported by local node
8	100Base-TX-FD	RW	0x1	1: 100Base-TX full duplex is supported by local node 0: 100Base-TX full duplex not supported by local node
7	100Base-TX	RW	0x1	1: 100Base-TX is supported by local node 0: 100Base-TX not supported by local node
6	10Base-T-FD	RW	0x1	1: 10Base-T full duplex supported by local node 0: 10Base-T full duplex not supported by local node
5	10Base-T	RW	0x1	1: 10Base-T is supported by local node 0: 10Base-T not supported by local node
4:0	Selector Field	RO	0x1	Binary Encoded Selector Supported by This Node. Currently only CSMA/CD 00001 is specified. No other protocols are supported.

6.6. Auto-Negotiation Link Partner Ability Register (Page 0, Register 5, ANLPAR)

Field	Name	Type	Default	Desc
15	Next Page	RO	0x0	Next Page Bit. 0: Transmitting the primary capability data page 1: Transmitting the protocol specific data page
14	Acknowledge	RO	0x0	1: Link partner acknowledges reception of local node's capability data word 0: No acknowledgement
13	Remote Fault	RO	0x0	1: Link partner is indicating a remote fault 0: Link partner is not indicating a remote fault
12	Reserved	RO	0x0	
11	Asymmetric PAUSE	RO	0x0	1: Asymmetric Flow control supported by Link Partner 0: No Asymmetric flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability.
10	Pause	RO	0x0	1: Flow control supported by Link Partner 0: No flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability (read only).
9	100Base-T4	RO	0x0	1: 100Base-T4 is supported by link partner 0: 100Base-T4 not supported by link partner
8	100Base-TX-FD	RO	0x0	1: 100Base-TX full duplex is supported by link partner 0: 100Base-TX full duplex not supported by link partner
7	100Base-TX	RO	0x0	1: 100Base-TX is supported by link partner 0: 100Base-TX not supported by link partner
6	10Base-T-FD	RO	0x0	1: 10Base-T full duplex is supported by link partner 0: 10Base-T full duplex not supported by link partner
5	10Base-T	RO	0x0	1: 10Base-T is supported by link partner 0: 10Base-T not supported by link partner
4:0	Selector Field	RO	0x1	Link Partner's Binary Encoded Node Selector. Currently only CSMA/CD 00001 is specified.

6.7. Auto-Negotiation Expansion Register (Page 0, Register 6, ANER)

Field	Name	Type	Default	Desc
15:5	Reserved	RO	0x0	
4	Parallel Detection Fault	RC	0x0	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function
3	Link Partner Next Page Ability	RO	0x0	1: Link Partner is Next Page able 0: Link Partner is not Next Page able
2	Local Next Page Ability	RO	0x0	1: Next Page is able 0: Not Next Page able
1	Page Received	RC	0x0	1: A New Page has been received 0: A New Page has not been received
0	Link Partner Auto-Negotiaton Ability	RO	0x0	If Auto-Negotiation is Enabled, This Bit Means: 1: Link Partner is Auto-Negotiation able 0: Link Partner is not Auto-Negotiation able

6.8. MMD Access Control Register (Page 0, Register 13, MMDAC)

Field	Name	Type	Default	Desc
15:14	MMD Function	RW	0x0	00: address 01: data, no post increment 10: data, post increment on reads and writes 11: data, post increment on writes only
13:5	Reserved	RW	0x0	Write as 0, ignore on read
4:0	MMD DEVAD	RW	0x0	Device address

6.9. MMD Access Address Data Register (Page 0, Register 14, MMDAAD)

Field	Name	Type	Default	Desc
15:0	MMD Address Data	RW	0x0	If MMDAC[15:14] = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register

6.10. Fiber Mode and Loopback Register (Page 0, Register 28, FMLR)

Field	Name	Type	Default	Desc
15	Reserved	RW	0x0	Be sure 0 when write
14:6	Reserved	RO	0x0	Reserved
5	Fiber Mode	RW	0x0	0: Copper Mode 1: Fiber Mode
4:3	Reserved	RO	0x0	Reserved
2	Auto MDI-X Enable	RW	0x1	Enable Auto MDI-X Function.
1	MDI Mode	RW	0x1	Force MDI/MDI-X Mode. when auto_mdix_en function is 0: 1: Force to MDI Mode 0: Force to MDI-X Mode
0	Reserved	RO	0x0	Reserved

6.11. Interrupt Indicators and Signal Quality Indicator Register (Page 0, Register 30, INTSQI)

Field	Name	Type	Default	Desc
15	AutoNeg Error	RC	0x0	Auto-Negotiation Error Interrupt. 1: Enable 0: Disable
14:12	Reserved	RO	0x0	Reserved
11	Link Status Change	RC	0x0	Link Status Change Interrupt. 1: Enable 0: Disable
10:5	Reserved	RO	0x0	Reserved
4:0	Signal Quality Indicator	RO	0x0	Signal Quality Indicator, lower is better. The value is only valid in 100Base-TX mode and its link status is ON

6.12. Page Select Register (Page 0, Register 31, PAGESEL)

Field	Name	Type	Default	Desc
15:8	Reserved	RO	0x0	Reserved
7:0	Page Selection	RW	0x0	

6.13. EEE Capability Enable Register (Page 4, Register 16, EEECER)

Field	Name	Type	Default	Desc
15:10	Reserved	RO	0x0	Reserved
9	TX Quiet Enable	RW	0x1	Enable Ability to Turn Off Power 100Base-TX when TX in Quiet State. This bit is recommended to be set to 1 when EEE is enabled
8	RX Quiet Enable	RW	0x1	Enable Ability to Turn Off Power 100Base-TX when RX in Quiet state. This bit is recommended to be set to 1 when EEE is enabled
7:0	Reserved	RO	0x0	Reserved

6.14. EEE Capability Register (Page 4, Register 21, EEECR)

Field	Name	Type	Default	Desc
15:1	Reserved	RO	0x0	Reserved
0	Link Partner EEE Cap	RO	0x0	Link partner supports EEE 100Base-TX after auto neg process

6.15. RMII Mode Setting Register (Page 7, Register 16, RMSR)

Field	Name	Type	Default	Desc
15	Reserved	RW	0x1	Reserved
14	Reserved	RW	0x1	Reserved
13	RMII RX_ER in RXD	RW	0x0	For Non-Bad-SSD rx_er, RXD will be 01
12	RMII Clock Direction	RW	0x1	Clock Direction of TX_CLK in RMII Mode. 0: 50MHz Output 1: 50MHz Input
11:8	RMII TX Skew	RW	0xf	Adjust RMII TX Interface Timing
7:4	RMII RX Skew	RW	0xf	Adjust RMII RX Interface Timing
3	MII/RMII Mode Selection	RW	0x0	0: MII Mode 1: RMII Mode
2	RMII CRS_DV Functional	RW	0x0	0: CRS/CRS_DV pin is CRS_DV signal 1: CRS/CRS_DV pin is RXDV signal
1	RMII RXD Bad SSD Enable	RW	0x1	0: RMII data only 1: RMII data with SSD Error
0	Reserved	RO	0x0	Reserved

6.16. EEE LEDs Enable Register (Page 7, Register 18, LEDER)

Field	Name	Type	Default	Desc
15:2	Reserved	RO	0x0	Reserved
1	EEE LED1 Enable	RW	0x0	Enable LED1 special Blink Mode in EEE/LPI Mode
0	EEE LED0 Enable	RW	0x0	Enable LED0 special Blink Mode in EEE/LPI Mode

6.17. Interrupt WOL Enable and LEDs Function Registers (Page 7, Register 19, WOLEN)

Field	Name	Type	Default	Desc
15:14	Reserved	RO	0x0	Reserved
13	Link Status Interrupt	RW	0x0	Link Status Interrupt 1: Interrupt enable 0: Interrupt disable
12	Reserved	RO	0x0	Reserved
11	AutoNeg Error Interrupt	RW	0x0	Auto Neg Interrupt 1: Interrupt enable 0: Interrupt disable
10:6	Reserved	RO	0x0	Reserved
5:4	LED Functional Selection	RW	0x3	check Functional Descrption for more details
3:0	Reserved	RO	0x0	Reserved

6.18. MMD Register Mapping and Definition

Table 17. MMD Register Map

Device	Offset	Addr	Name	Desc
0x3	0x1	0x0001	EEEPS1R	PCS Status 1 Register MMD Device 3
0x3	0x14	0x0014	EEECR	EEE Capability Register Register MMD Device 3
0x7	0x3c	0x003c	EEEAR	EEE Advertisement Register Register MMD Device 7
0x7	0x3d	0x003d	EEELPAR	EEE Link Partner Ability Register Register MMD Device 7

6.18.1. EEEPS1R (PCS Status 1 Register MMD Device 3) (addr=0x0001)

Field	Name	Type	Default	Desc
15:12	Reserved	RO	0x0	Reserved
11	TX_LPI Received Flag	ROLH	0x0	EEE/LPI signal has been received for TX
10	RX_LPI Received Flag	ROLH	0x0	EEE/LPI signal has been received for RX
9	TX_LPI Indication	RO	0x0	EEE/LPI signal is receiving for TX
8	RX_LPI Indication	RO	0x0	EEE/LPI signal is receiving for RX
7:0	Reserved	RO	0x0	Reserved

6.18.2. EEECR (EEE Capability Register Register MMD Device 3) (addr=0x0014)

Field	Name	Type	Default	Desc
15:2	Reserved	RO	0x0	Reserved
1	Base100_TX_EEE Cap	RO	0x1	1: EEE is supported for 100Base-TX EEE 0: EEE is not supported for 100Base-TX EEE
0	Reserved	RO	0x0	Reserved

6.18.3. EEEAR (EEE Advertisement Register Register MMD Device 7) (addr=0x003c)

Field	Name	Type	Default	Desc
15:2	Reserved	RW	0x0	Reserved
1	Base100_TX_EEE Advertisement	RW	0x0	Advertise 100Base-TX EEE Capability. 1: Advertise 0: Do not advertise
0	Reserved	RW	0x0	Reserved

6.18.4. EEELPAR (EEE Link Partner Ability Register Register MMD Device 7) (addr=0x003d)

Field	Name	Type	Default	Desc
15:2	Reserved	RO	0x0	Reserved
1	Base100_TX_EEE LP Ability	RO	0x0	1: Link Partner is capable of 100Base-TX EEE 0: Link Partner is not capable of 100Base-TX EEE
0	Reserved	RO	0x0	Reserved

Chapter 7. Design Guide

7.1. Power Supply and Internal LDO

The JL11x1 digital domain needs a 1.2V supply, an on-chip LDO has been integrated for simplicity.

To use the internal LDO, the pin "EN_DLDO" must be pulled up to AVDD3V3 (3.3V), and a low-ESR ceramic capacitor (0.1uF) should be placed at the pin "DVDD1V2" (close to chip as possible).

If an external 1.2V is supplied, the pin "EN_DLDO" must be pulled down to ground to avoid conflict. (This feature is for JL1111 Only)

The JL11x1 use 3.3V supply for analog domain, while the digital IO supports 1.8/2.5/3.3V supply for different EMI requirements.

7.2. Clock Requirements

There are 3 different ways to enable the reference clock:

1. A 25MHz XTAL could be connected to pin "XI" and "XO", and it is recommended that the pin "REFCLK_SEL" is connected to a bypass cap (a 100K Ohm pull-up resistor is already implemented on chip) or floating.
2. External 25MHz clock could be directly connected to pin "XI" by dc couple, leaving "XO" floating, and it is recommended that the pin "REFCLK_SEL" is connected to a bypass cap or floating.
3. External 50MHz clock could be directly connected to pin "XI" by dc couple, leaving "XO" floating, and the pin "REFCLK_SEL" must be pulled down to ground with a resistor less than 10KΩ.

7.3. Layout Guide

7.3.1. Stack-up

In order to reduce the reflection of high speed signals, the impedance of the signal trace routed in PCB should be matched from source to sink. To meet this requirement, at least Four-Layer PCB is recommended. Below stack-up is for reference.

Stackup(4 Layer)	
soldermask	20um
L1(High Speed Signal)	43um
PP	112um
GND02	18um
CORE	1180um
Power03	18um
PP	112um
L4(High Speed Signal)	43um
soldermask	20um

Total: 1600um

In this stack-up, high speed signal is preferential to route in top Layer compared to bottom layer for the signal have a direct reference to the ground layer. If it is desirable to route high speed signal in bottom layer, Layout engineer can swap the usage of ground and power on layer 2 and 3.

7.3.2. Power Supply

For every power supply pin of IC, it is better to place a individual bypass capacitor as close as possible. Keep the trace short and wide. It is preferable that the current first passes the bypass capacitor and the enters the supply pin.

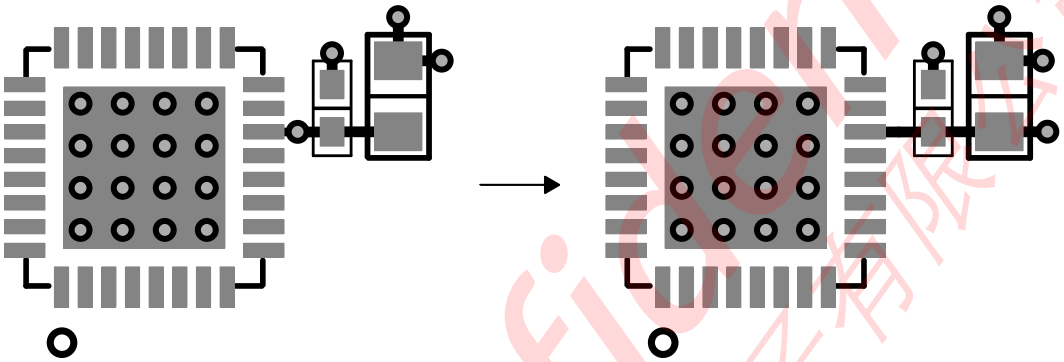


Figure 23. Power_Supply

Pay attention to the integrity of power and ground planes.Sometimes,the voids signal vias caused in these planes may lead to current density increasing. These areas are also called hot spots. It is important to arrange the place of the vias to avoid these hot spots. Often a good approach is to place the vias in a grid that leaves enough space between the vias for the power plane to pass.

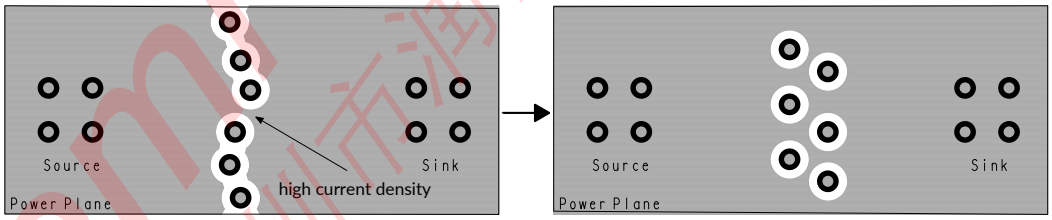


Figure 24. Avoid Copper Plane Hot Spots

7.3.3. Signal Trace

Impedance

Critical signals are required impedance control generally.The value is 50Ω single-ended and 100Ω differential if without specially mentioned.Take care to ensure impedance is controlled throughout.Impedance discontinuities will cause reflections leading to emissions and signal integrity issues,for example,crosstalk,ringing... Recording to the result of simulation with 3D field tools,via introduce a huge discontinuity in impedance.If possible, reduce the amount of placed vias to a minimum.

Stub

Long stub traces can act as antennas and therefore increase problems complying with EMC standards. Stub traces can also produce reflections which negatively impacts signal integrity. Common sources for stubs are pull-up or pull-down resistors on high speed signals. If such resistors are required, route the signals as a daisy chain.

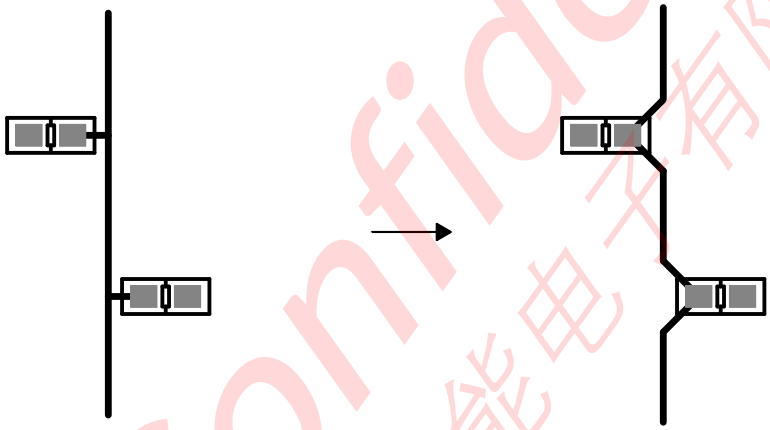


Figure 25. Avoid Stub Traces by Daisy Chain Routing

Length match

High speed interface need to match the length of signal trace. For example, in a high speed parallel bus, all data signals need to arrive within a time period in order to meet the setup and hold time requirements of the receiver. Length matching is also important for MAC interface (MII,RMII,GMII,RGMII..) connections. All transmit signal traces should be length matched to each other and all receive signal traces should be length matched to each other.

Differential pairs

Differential pair signals need to be routed in parallel with a same width and a same specific, constant distance between the two traces. This width and distance is required in order to obtain the specified differential impedance. Differential pair signals often require a very tight delay skew between the positive and negative signal traces. In other word, the length of positive and negative signal traces need to be matched. When using serpentine to compensate length differences, it is better to choose starting in the place which differences occur.

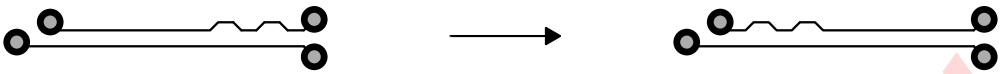
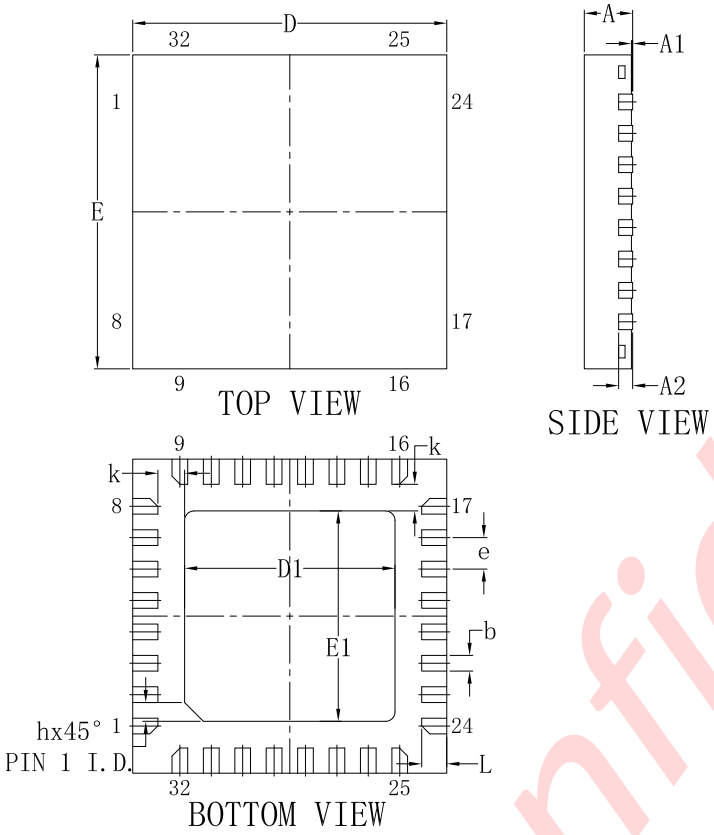


Figure 26. Differential pair

Chapter 8. Mechanical, Packaging

8.1. Packaging Information

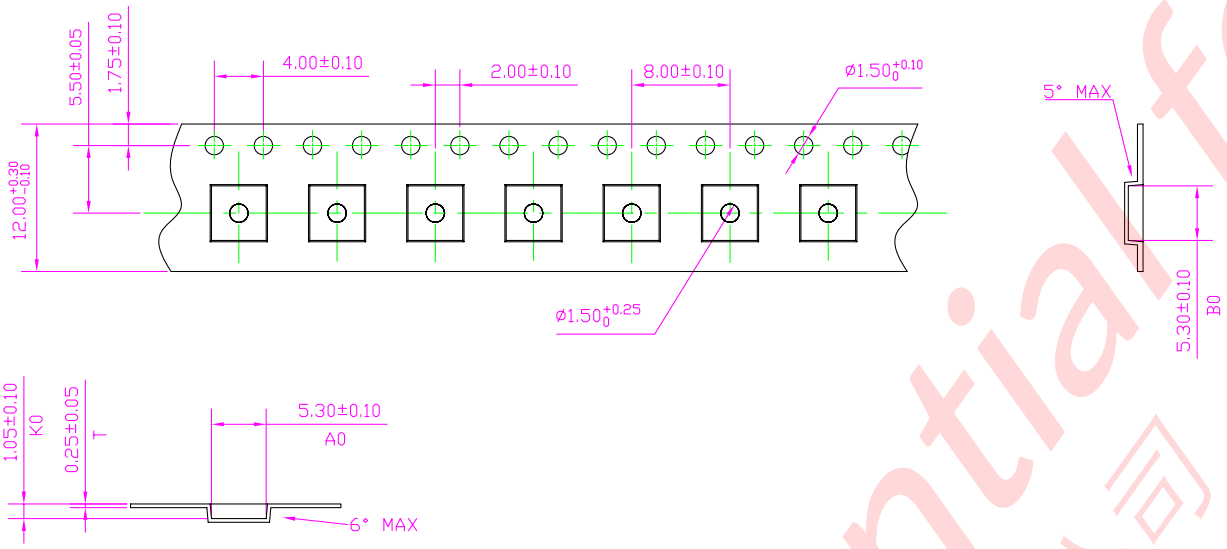


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	/	0.050
A2	0.173	0.203	0.253
b	0.200	0.250	0.300
D	4.950	5.000	5.050
D1	3.300	3.350	3.400
E	4.950	5.000	5.050
E1	3.300	3.350	3.400
e	0.450	0.500	0.550
h	0.250	0.300	0.350
k	0.375	0.425	0.475
L	0.350	0.400	0.450

Figure 27. QFN 32 5mm x 5mm

8.2. Tape and Reel Information

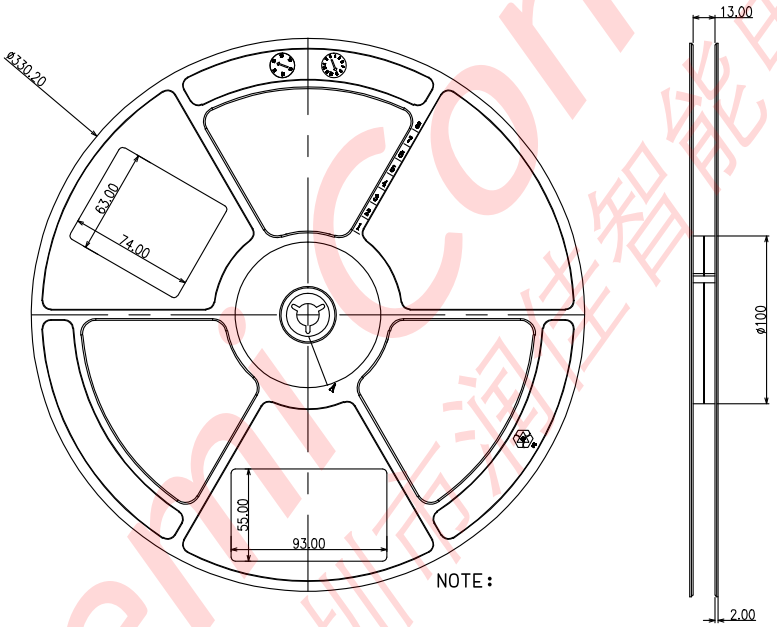


NOTE:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
2. CARRIER CAMBER IS 1MM IN 100M
3. ALL DIMENSIONS MEET EIA-481-3 REQUIREMENTS

UNIT: mm

Figure 28. Tape Information



NOTE:

1. Material: HIPS
2. Unit: mm

Available Reel Sizes(mm)		
Tape Width	B±0.5mm	W+1mm
12mm	Ø100mm	13mm
16mm		17mm
24mm		25mm
32mm		33mm
44mm		45mm
56mm		57mm

Figure 29. Reel Information

Chapter 9. Order Information and Support

Table 18. Ordering Guide

Model	Temperature Range	Package Description
JL1101-N032C	0 ~ 70°C	32-Pin QFN (RoHS 2.0 Compliant)
JL1111-N032C	0 ~ 70°C	32-Pin QFN (RoHS 2.0 Compliant)
JL1111-N032I	-40 ~ 85°C	32-Pin QFN (RoHS 2.0 Compliant)
JL1111-N032E	-40 ~ 105°C	32-Pin QFN (RoHS 2.0 Compliant)

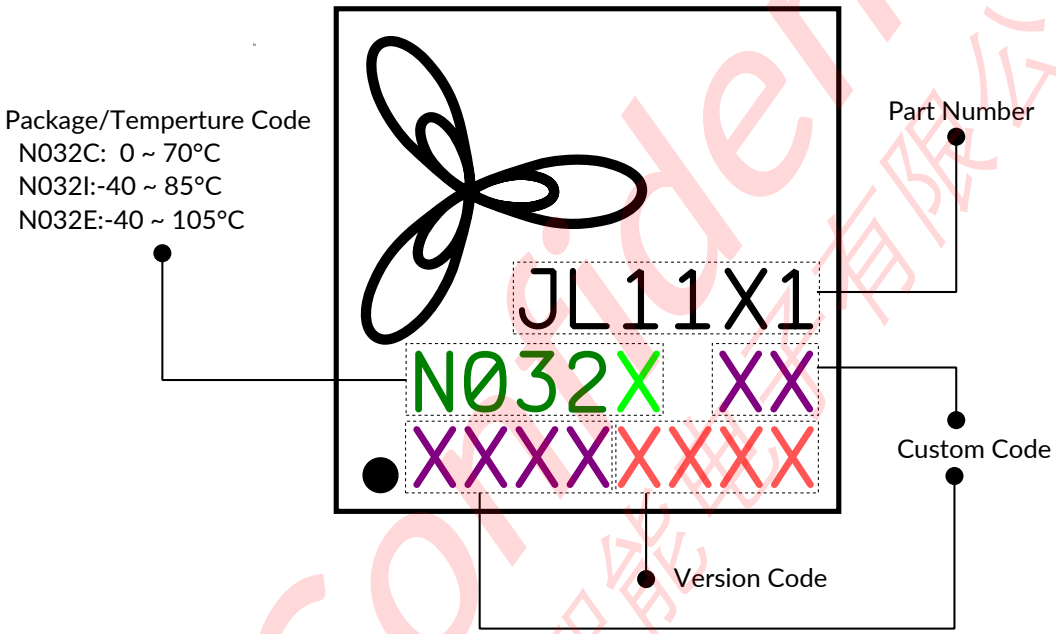


Figure 30. Part Description