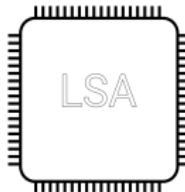


Breaking the microchip monopoly

leviathan/talamon
(Lanceville Technology)

January 7, 2018



Libre Silicon Alliance

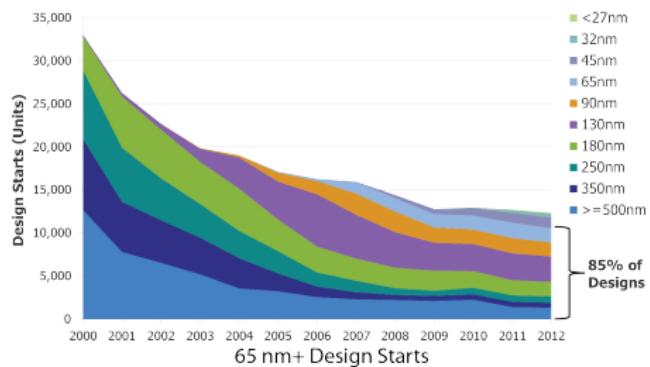
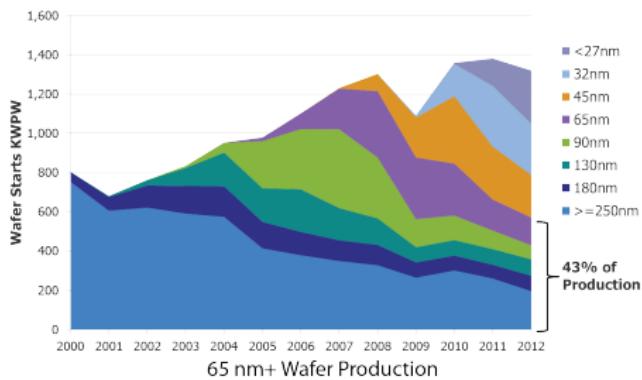
What we do

- We make **free silicon**
- Breaking the monopoly of big semiconductor manufacturers
- Eliminating the vendor lock-in to big semiconductor manufacturers
- Making semiconductor development super quick and inexpensive
- Introducing the LSPL (LibreSilicon public license)
- Attracting commercial design houses to develop **free silicon**

Why are we doing this?

- MPWs cost around 20'000 USD nowadays
- MPWs take around 2-9 months nowadays
- All manufacturers want NDAs (some NDAs even have NDAs!)
- Your design for a vendor process contains process specific design quirks (also under NDA!)
- No manufacturer provides the GDS2 files in order to manufacture the designs in your basement (there is **no** free silicon yet)
- You can't even publish your own designs!

Closed silicon market



¹<http://semimd.com/favre/2016/08/24>

Community projects



Icarus Verilog

Yosys Open SYnthesis Suite



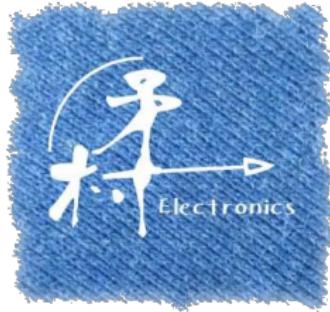
Companies and institutions



香港科技大學
THE HONG KONG
UNIVERSITY OF SCIENCE
AND TECHNOLOGY



efabless^{.com}



Reward IP developers

- Chip designer is rewarded when IP is used on collaboration platforms
- Smart contracts track usage and pay contributors
- Hash of IP + desired return value

How we do it

- Introducing an open source chip manufacturing process standard specification
- Introducing a fully integrated free EDA for ASIC design¹
- Renting the clean room and manufacturing equipment at HKUST every 2 weeks for around 12 hours



¹<https://github.com/leviathanch/qtflow>

Libre Silicon EDA Tools

- QtFlow EDA²
 - EDA suite written in Qt5
 - Wave viewer
 - Planned:
 - Integration of higher level HDLs (CLash)
 - Plugins through PythonQt
- Icarus Verilog simulation³
- QRouter maze router⁴
- GrayWolf floor planner⁵

²<https://github.com/leviathanch/qtflow>

³<http://iverilog.icarus.com>

⁴<https://github.com/leviathanch/qrouter>

⁵<https://github.com/leviathanch/graywolf>

QtFlow screen shots

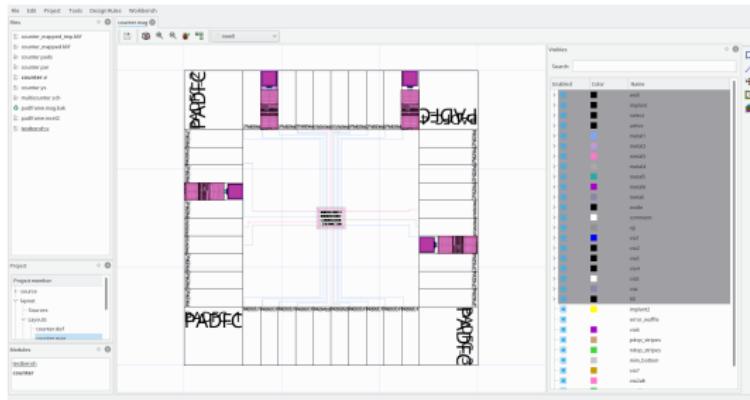
The screenshot shows the QtFlow software interface. The main window has a menu bar with File, Edit, Project, Tools, Design Rules, and Workbench. The left sidebar displays the project structure under 'Project' (Project member, source, layout, Sources, Layouts, Schematics) and 'Modules' (testbench, counter). The central area is a code editor showing Verilog code for a counter module. The code defines a module counter(d, q, clk, clr) with inputs d (8-bit), clk, clr, and outputs q (8-bit). It contains two always blocks: one for the clock edge where r is updated from 0 to 10101010 or 0 to 00000000 based on the clear signal, and another for the next clock edge where q is updated to q + r. The right sidebar includes tabs for Line 1, Column 1, INSERT, Tab Size: 8, UTF-B, Verilog, and a Python Console tab which is currently active.

```
File Edit Project Tools Design Rules Workbench
counter.v
module counter(d, q, clk, clr);
    input [7:0] d;
    input clk;
    input clr;
    output [7:0] q;
    reg [7:0] r;
    reg [7:0] q;
    always @ (posedge clk)
        if(clr==1)
            r <= 8'b10101010;
        else begin
            r[0] <= r[0];
            r[1] <= r[1];
            r[2] <= r[2];
            r[3] <= r[3];
            r[4] <= r[4];
            r[5] <= r[5];
            r[6] <= r[6];
            r[7] <= r[7];
        end
    always @ (posedge clk)
        if(clr==1)
            q <= 8'b00000000;
        else begin
            q <= q + r;
        end
endmodule
Line 1, Column 1 INSERT Tab Size: 8 UTF-B Verilog Python Console
Py>
```

QtFlow screen shots



QtFlow screen shots

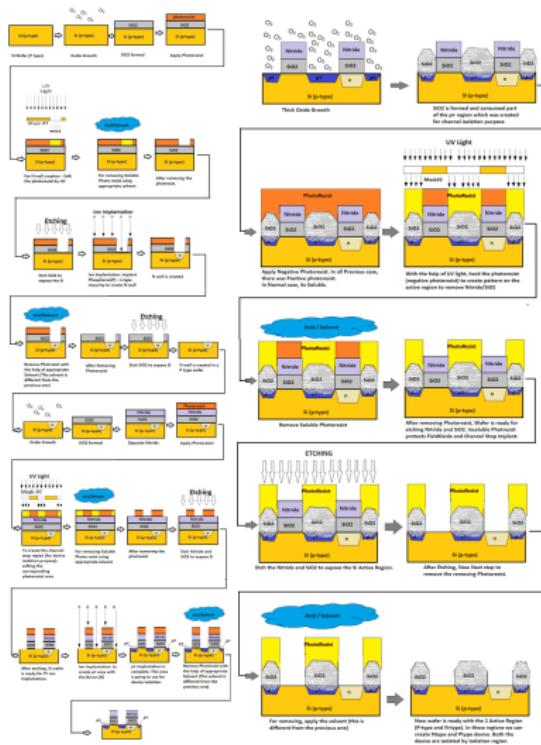


Process

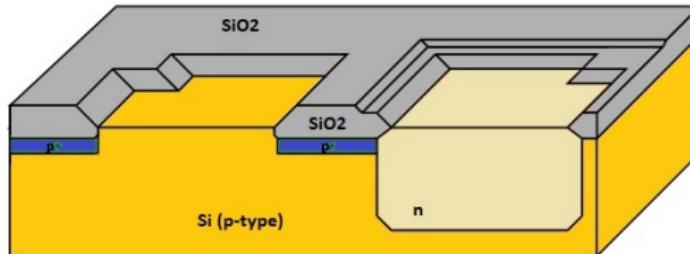
- We start with a simple CMOS process⁶
- We will verify the process
- We will improve based on it

⁶<http://www.vlsi-expert.com/2014/09/fabrication-steps-cmos-processing-part-1.html>

Process

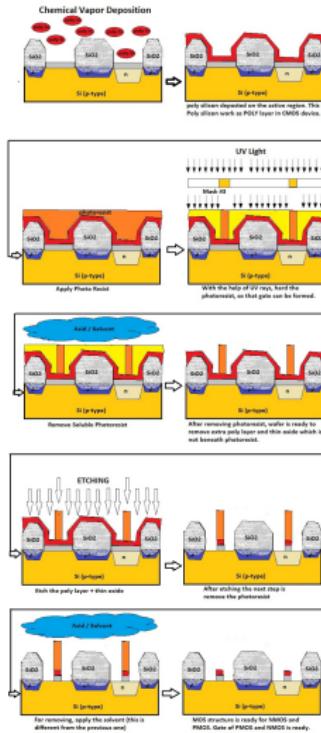


Process

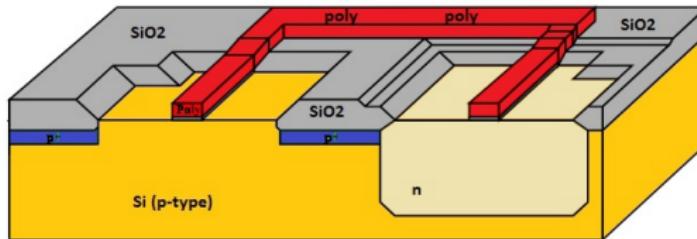


3D Diagram of the Silicon Wafer - for better understanding.

Process

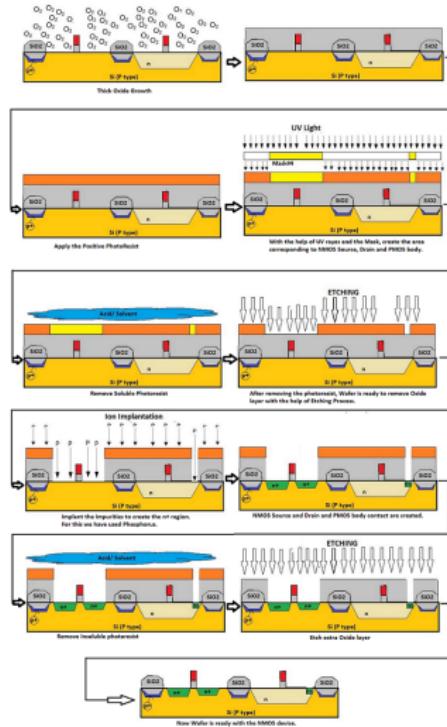


Process

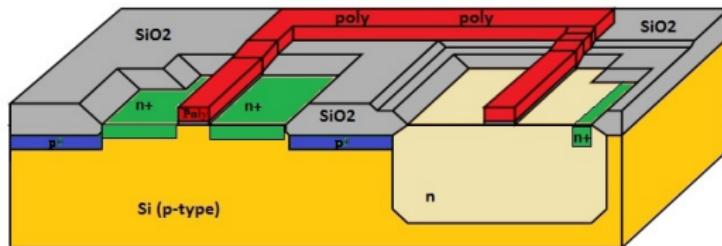


3D view of the Silicon Wafer after depositing the Poly layer. There are 2 Active Region (For PMOS and NMOS), Isolation Region (which consists Field Oxide), Gate Oxide and Poly layer.

Process

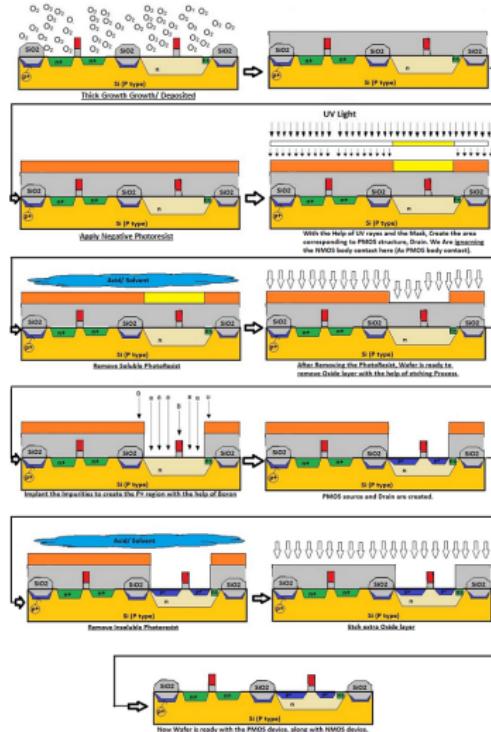


Process

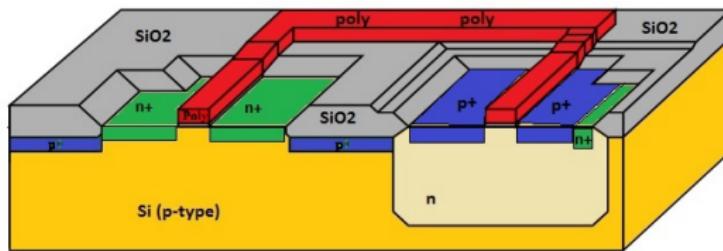


Final View of the Silicon Wafer. Now we have NMOS device ready.

Process

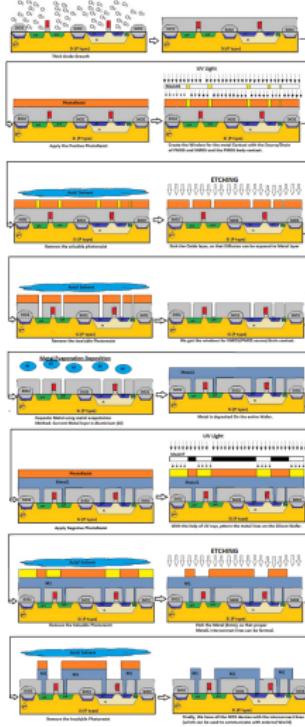


Process

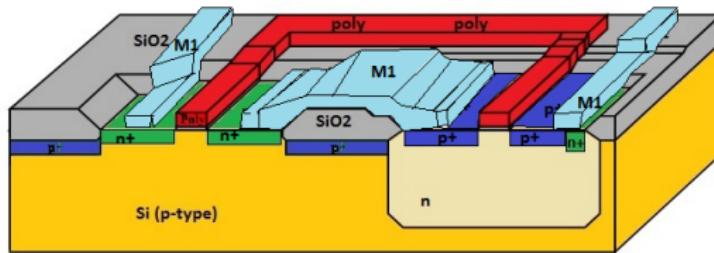


3D view of silicon wafer. Now we have PMOS and NMOS Device.

Process



Process



Final Wafer with NMOS + PMOS devices with Metal 1 Interconnects.
The combination of NMOS and PMOS as per above structure is
known as CMOS (Complementary Metal Oxide Semiconductor)

Help needed

- Work on developing QtFlow
 - GrayWolf issues⁷
 - QRouter issues⁸
 - Front end issues⁹
- Work on the LibreSilicon process¹⁰ and technologies¹¹
 - Work on the standard logic cells
 - Work on developing FreeFLASH
 - Work on developing FreeDRAM
 - Develop ADCs and stuff
- Financial contributions/Investments

⁷<https://github.com/leviathanch/graywolf>

⁸<https://github.com/leviathanch/qrouter>

⁹<https://github.com/leviathanch/qtflow>

¹⁰<https://github.com/leviathanch/libresiliconprocess>

¹¹<https://github.com/leviathanch/lso18>

Contact

leviathan

CEO and founder of Lanceville Technologies

Full name: David Lanzendörfer

E-Mail (please use GnuPG if possible): david.lanzendoerfer@lanceville.cn

Riot ID: @leviathanch:matrix.org

Phone/NSA Chat(WhatsApp): +852 6672 2499

talamon

Full name: Andreas Westerwick

E-Mail (please use GnuPG if possible): andreas.westerwick@o2s.ch

Mumble: murmur.lanceville.hk

Thank you!

**Thank you very much!
Vielen herzlichen Dank!**

