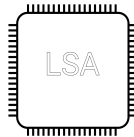


## Breaking the microchip monopoly

leviathan/talamon

December 17, 2017



Libre Silicon Alliance

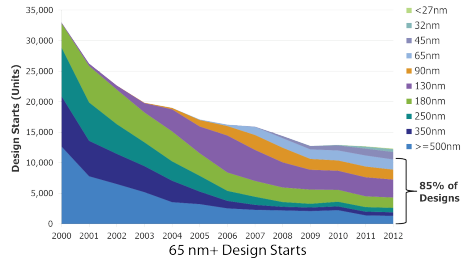
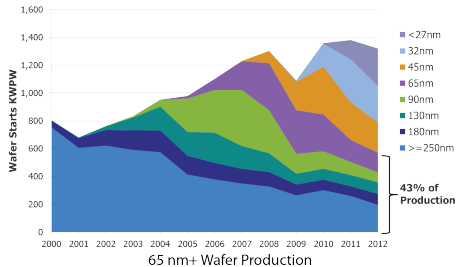
## What we do

- Breaking the monopoly of big semiconductor manufacturers
- Eliminating the vendor lock-in to big semiconductor manufacturers
- Making semiconductor development super quick and inexpensive
- Introducing the LSPL (LibreSilicon public license)
- Attracting commercial design houses to develop free silicon

## Why are we doing this?

- MPWs cost around 20'000 USD nowadays
- MPWs take around 2-9 months nowadays
- All manufacturers want NDAs (some NDAs even have NDAs!)
- Your design for a vendor process contains process specific design quirks (also under NDA!)
- No manufacturer provides the GDS2 files in order to manufacture the designs in your basement (there is **no** free silicon yet)
- You can't even publish your own designs!

# Closed silicon market



<sup>1</sup><http://semimd.com/favre/2016/08/24>

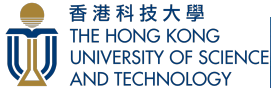
## Community projects



Yosys Open SYnthesis Suite



## Companies and institutions



**efabless**.com



## Reward IP developers

- Chip designer is rewarded when IP is used on collaboration platforms
- Smart contracts track usage and pay contributors
- Hash of IP + desired return value

## How we do it

- Introducing an open source chip manufacturing process standard specification
- Introducing a fully integrated free EDA for ASIC design<sup>1</sup>
- Renting the clean room and manufacturing equipment at HKUST every 2 weeks for around 12 hours



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<sup>1</sup><https://github.com/leviathanch/qtflow>



## Libre Silicon EDA Tools

- QtFlow EDA<sup>2</sup>
- Icarus Verilog simulation<sup>3</sup>
- QRouter maze router<sup>4</sup>
- GrayWolf floor planner<sup>5</sup>

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<sup>2</sup><https://github.com/leviathanch/qtflow>

<sup>3</sup><http://iverilog.icarus.com>

<sup>4</sup><https://github.com/leviathanch/qrouter>

<sup>5</sup><https://github.com/leviathanch/graywolf>

## Help needed

- Work on developing QtFlow
  - GrayWolf issues<sup>6</sup>
  - QRouter issues<sup>7</sup>
  - Front end issues<sup>8</sup>
- Work on the LibreSilicon process<sup>9</sup> and technologies<sup>10</sup>
  - Work on the standard logic cells
  - Work on developing FreeFLASH
  - Work on developing FreeDRAM
  - Develop ADCs and stuff
- Financial contributions/Investments

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<sup>6</sup><https://github.com/leviathanch/graywolf>

<sup>7</sup><https://github.com/leviathanch/qrouter>

<sup>8</sup><https://github.com/leviathanch/qtflow>

<sup>9</sup><https://github.com/leviathanch/libresiliconprocess>

<sup>10</sup><https://github.com/leviathanch/ls018>

## Contact

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Thank you!

Thank you very much!  
Vielen herzlichen Dank!  
非常感谢你们!

