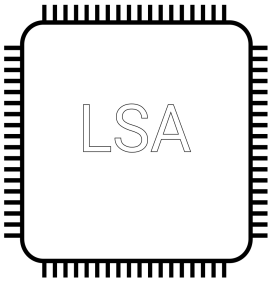
Libre Silicon Alliance

leviathan/talamon

December 15, 2017

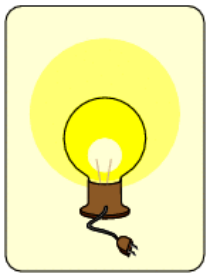


What we do

- Breaking the monopoly of big semiconductor manufacturers
- Eliminating the vendor lock-in to big semiconductor manufacturers
- Making semiconductor development super quick and inexpensive (a few weeks and 50-100 USD per run)

Community projects

Yosys Open SYnthesis Suite



Companies and institutions

香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

NFF
Nanoelectronics Fabrication Facility

efabless.com

Electronics

How we do it

- Introducing an open source chip manufacturing process standard specification
- Introducing an fully integrated free EDA for ASIC design[1]

[1] https://github.com/leviathanch/qtflow

Why are we doing this?

- MPWs cost around 20'000 USD nowadays
- MPWs take around 2-9 months nowadays
- No manufacturer provides the GDS2 files in order to manufacture the designs in your basement (there is **no** free silicon yet)

Help needed

- Help developing QtFlow[2]
- Help with the LibreSilicon process[3]
- Work on the standard logic cells
- Work on developing FreeFLASH
- Work on developing FreeDRAM
- Donations

[2] https://github.com/leviathanch/qtflow
[3] https://github.com/leviathanch/libresiliconprocess

Thank you!