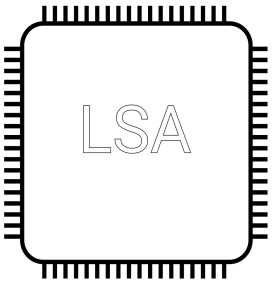
Breaking the microchip monopoly

leviathan/talamon

December 18, 2017



Libre Silicon Alliance

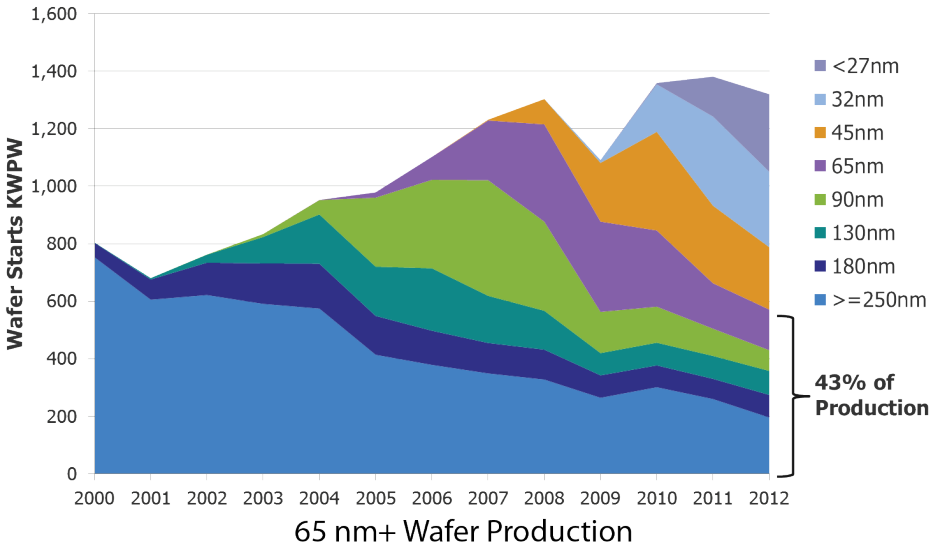
What we do

- We make **free silicon**
- Breaking the monopoly of big semiconductor manufacturers
- Eliminating the vendor lock-in to big semiconductor manufacturers
- Making semiconductor development super quick and inexpensive
- Introducing the LSPL (LibreSilicon public license)
- Attracting commercial design houses to develop **free silicon**

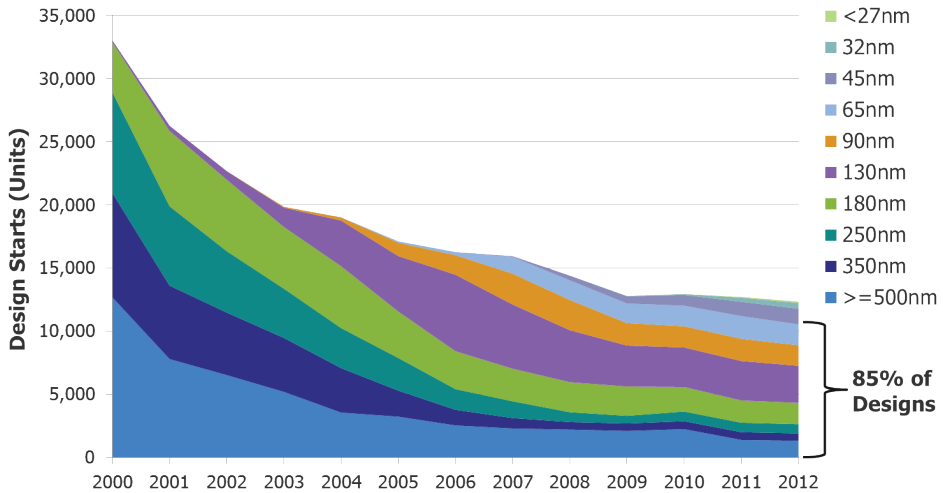
Why are we doing this?

- MPWs cost around 20'000 USD nowadays
- MPWs take around 2-9 months nowadays
- All manufacturers want NDAs (some NDAs even have NDAs!)
- Your design for a vendor process contains process specific design quirks (also under NDA!)
- No manufacturer provides the GDS2 files in order to manufacture the designs in your basement (there is **no** free silicon yet)
- You can't even publish your own designs!

Closed silicon market



65 nm+ Wafer Production



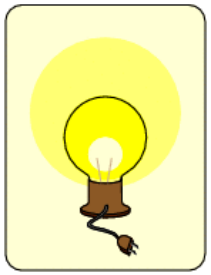
65 nm+ Design Starts

[1] http://semimd.com/favre/2016/08/24

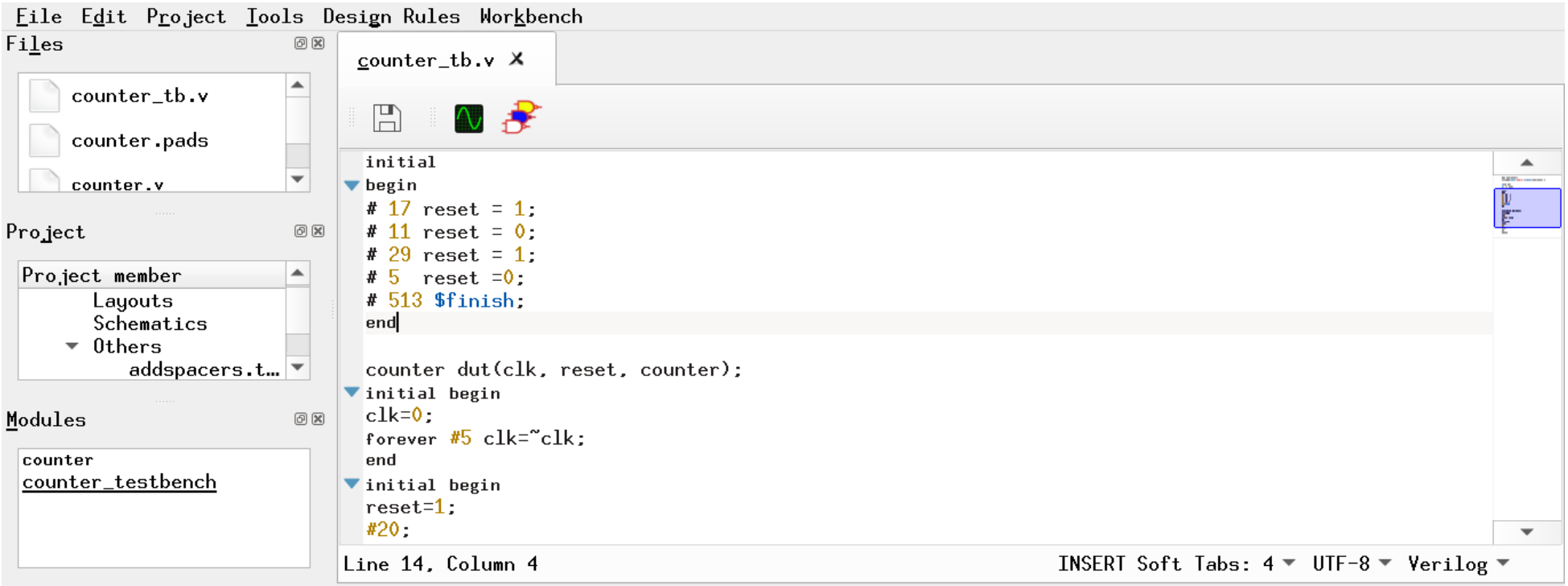
Community projects

Icarus Verilog

Yosys Open SYnthesis Suite



QtFlow


File Edit Project Tools Design Rules Workbench
Files
counter_tb.v
counter.pads
counter.v
Project
Project member
Layouts
Schematics
Others
addspacers.t...
Modules
counter
counter_testbench
counter_tb.v
initial
begin
# 17 reset = 1;
# 11 reset = 0;
# 29 reset = 1;
# 5 reset =0;
# 513 $finish;
end
counter dut(clk, reset, counter);
initial begin
clk=0;
forever #5 clk=~clk;
end
initial begin
reset=1;
#20;
Line 14, Column 4
INSERT Soft Tabs: 4
UTF-8
Verilog
Python Console
16.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \counter..
Creating internal representation of mux trees.
No muxes found in this module.

QtFlow

- QtFlow: EDA suite written in Qt5
- Wave viewer

QtFlow (planned)

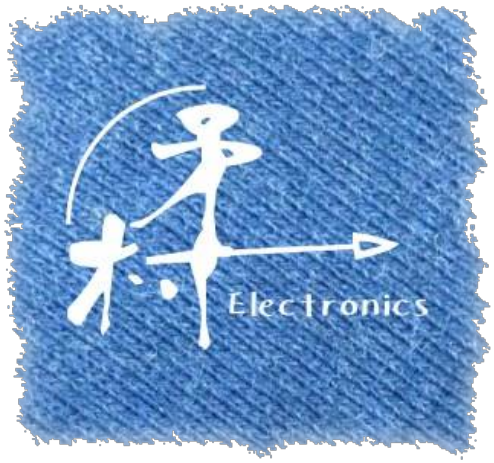
- Integration of higher level HDLs (CLash)
- Plugins through PythonQt

Companies and institutions

香港科技大學
THE HONG KONG
UNIVERSITY OF SCIENCE
AND TECHNOLOGY

NFF
Nanoelectronics Fabrication Facility

efabless.com

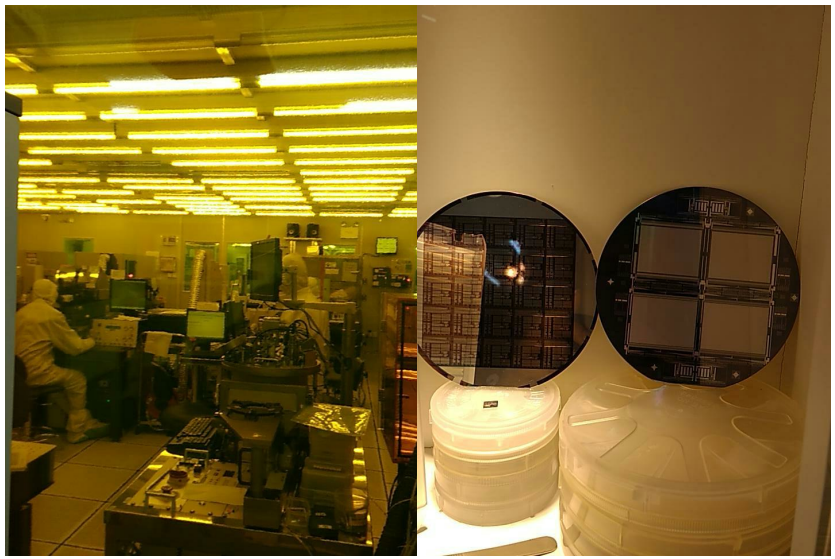


Reward IP developers

- Chip designer is rewarded when IP is used on collaboration platforms
- Smart contracts track usage and pay contributors
- Hash of IP + desired return value

How we do it

- Introducing an open source chip manufacturing process standard specification
- Introducing a fully integrated free EDA for ASIC design[1]
- Renting the clean room and manufacturing equipment at HKUST every 2 weeks for around 12 hours



[1] https://github.com/leviathanch/qtflow

Libre Silicon EDA Tools

- QtFlow EDA[2]
- Icarus Verilog simulation[3]
- QRouter maze router[4]
- GrayWolf floor planner[5]

[2] https://github.com/leviathanch/qtflow
[3] http://iverilog.icarus.com
[4] https://github.com/leviathanch/qrouter
[5] https://github.com/leviathanch/graywolf

Help needed

- Work on developing QtFlow
  - GrayWolf issues[6]
  - QRouter issues[7]
  - Front end issues[8]
- Work on the LibreSilicon process[9]and technologies[10]
  - Work on the standard logic cells
  - Work on developing FreeFLASH
  - Work on developing FreeDRAM
  - Develop ADCs and stuff
- Financial contributions/Investments

[6] https://github.com/leviathanch/graywolf
[7] https://github.com/leviathanch/qrouter
[8] https://github.com/leviathanch/qtflow
[9] https://github.com/leviathanch/libresiliconprocess
[10] https://github.com/leviathanch/ls018

Contact

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Thank you!

Thank you very much!
Vielen herzlichen Dank!
非常感谢你们!