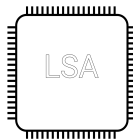


Libre Silicon Alliance

leviathan/talamon

December 15, 2017



What we do

- Breaking the monopoly of big semiconductor manufacturers
- Eliminating the vendor lock-in to big semiconductor manufacturers
- Making semiconductor development super quick and inexpensive

Community projects



Icarus Verilog

Yosys Open SYnthesis Suite



Companies and institutions

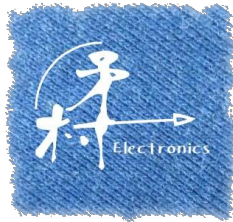


香港科技大學
THE HONG KONG
UNIVERSITY OF SCIENCE
AND TECHNOLOGY

NFF

Nanoelectronics Fabrication Facility

efabless.com



How we do it

- Introducing an open source chip manufacturing process standard specification
- Introducing a fully integrated free EDA for ASIC design¹
- Renting the clean room and manufacturing equipment at HKUST every 2 weeks for around 12 hours



¹<https://github.com/leviathanch/qtflow>

Why are we doing this?

- MPWs cost around 20'000 USD nowadays
- MPWs take around 2-9 months nowadays
- All manufacturers want NDAs (some NDAs even have NDAs!)
- Your design for a vendor process contains process specific design quirks (also under NDA!)
- No manufacturer provides the GDS2 files in order to manufacture the designs in your basement (there is **no** free silicon yet)
- You can't even publish your own designs!

Help needed

- Work on developing QtFlow²
- Work on the LibreSilicon process³
- Work on the standard logic cells
- Work on developing FreeFLASH
- Work on developing FreeDRAM
- Financial contributions/Investments

²<https://github.com/leviathanch/qtflow>

³<https://github.com/leviathanch/libresiliconprocess>

Thank you!

Thank you very much!
Vielen herzlichen Dank!
非常感谢你们!

