Abstract

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This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells[1] and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing $1\mu m$ only!** But further releases which will have been tested with smaller structure sizes can be expected.

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[1] `https://git.libresilicon.com/?p=redmine/standard-cell-lib.git;a=summary`

Contents

Libre Silicon process steps

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August 18, 2019

The general flow chart of the overall process flow can be seen in Figure 1. These process steps will be discussed within the following sections.
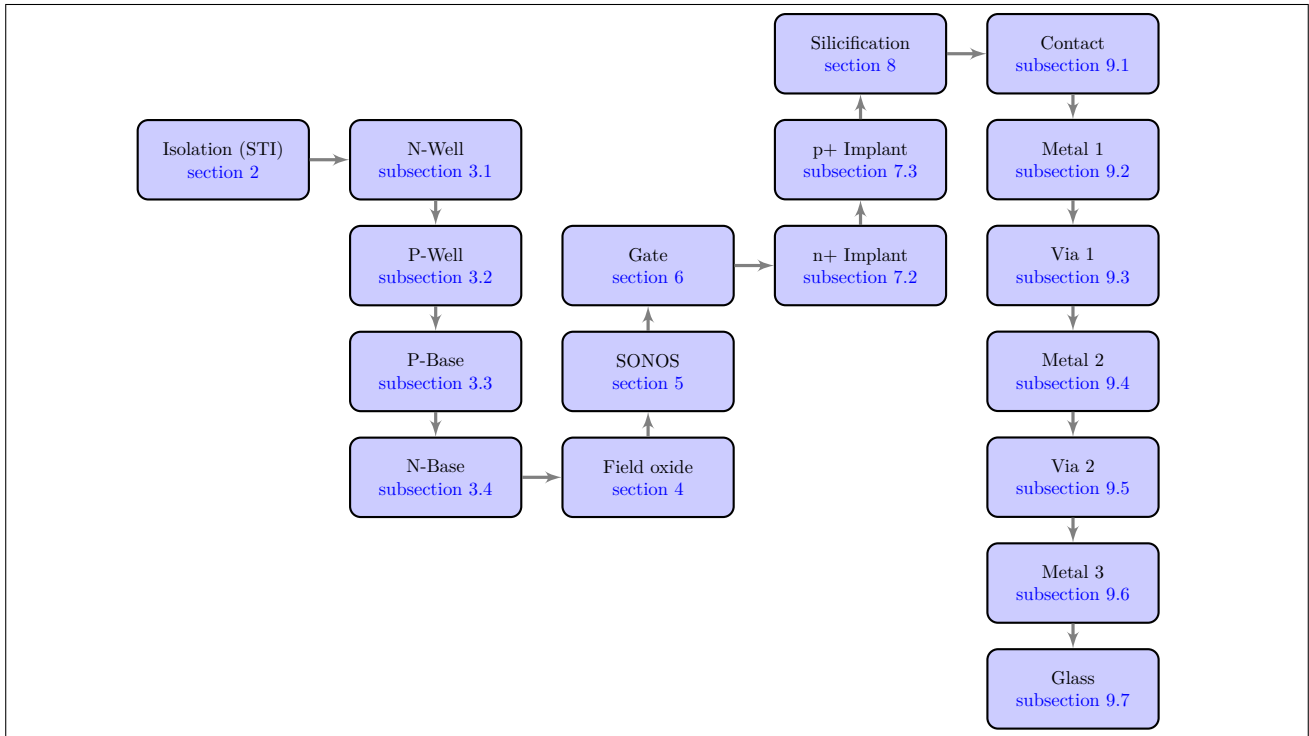

Figure 1: Frontend and backend process flow

The six overall process steps are part of an active part of the technology, while the final metal (respectively contact) layers will be used for making a contact between the logic gates and macro cells and making them available to the exterior world.

For this process p-substrate is the required basic substrate, but forks and modifications will be very well possible based on a Graphene substrate or alike, still under the LSPL. The starting material is a p-type, <100> oriented silicon with a doping concentration of $\approx 9 \times 10^{14} cm^{-3}$.

Machines required:

- Ion implanter

- Plasma etcher

- Sputter engine (Metal deposition)

- Diffusion furnace

- CVD/LPCVD machine

- Exposure unit

1 Alignment marks

The very first thing which has to be done when receiving a bunch of new wafers from the supplier, is to clean them with hot sulfuric acid and to remove native oxide on top, by dipping it into HF. The time for the HF dip depends on the concentration.

After that one has to etch some kind of alignment marks into the silicon, which allows the stepper to match the different mask layers to each other during exposure.
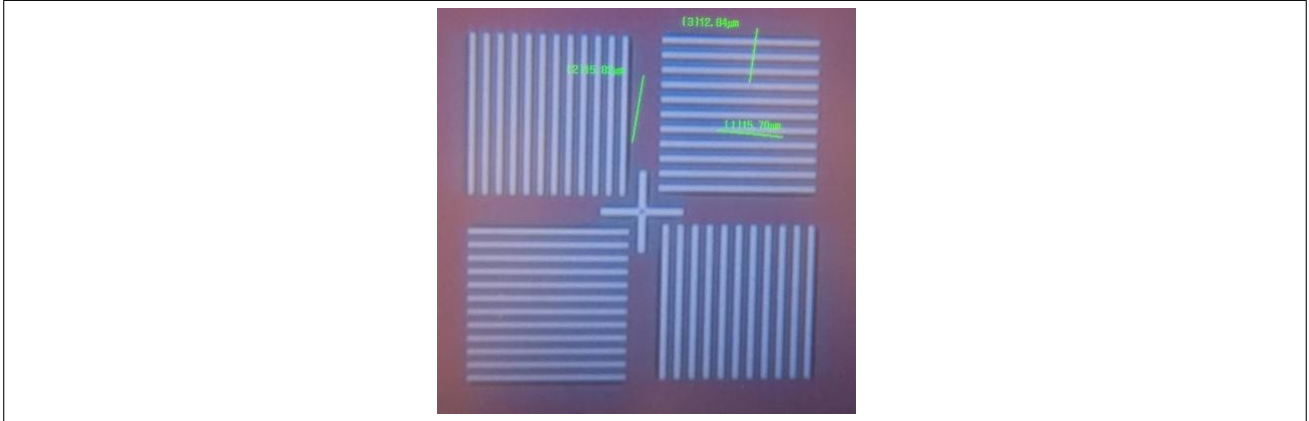

Figure 2: Picture of an alignment mark

How such an alignment mark might look like is being shown in Figure 2, which is the ASML mark used for the ASML stepper units.

Depending on the alignment strategy there can be two or more alignment marks being etched into the substrate, and the positioning entirerly depends on the pattern recognition software and alignment strategy of the specific machine.

The depth of this silicon etching is usually around 200nm or so, but is nothing really critical to support LibreSilicon but more something stepper aligner specific.

The manufacturer of the stepper aligner usually provides pre made masks for this step and provide requirements for the depth of those marks inside the silicon.

The ASML stepper has two alignment marks left and right of the wafer, which, when connected to a line, are in parallel to the notch.

Those marks are critical for aligning the patterns correctly above each other during all the further manufacturing steps, so it should be taken care, that those markers stay always visible, so that the machine can find them and orient itself on it.

2 Shallow trench isolation

The geometry of a substrate with STI implemented can be seen in Figure 3.
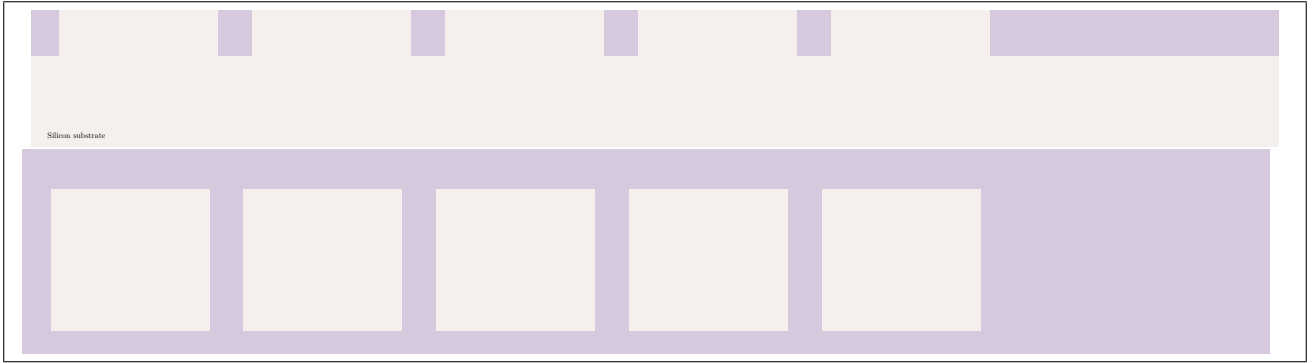

Silicon substrate

Figure 3: Shallow trench isolation target geometry

As can be seen in Figure 9, the STI trench is supposed to have approximately half the depth of the N-well.
Because the N-well will be $\approx 4\mu m$ in depth, so we have to match this with our trench depth.
I order to allow a sufficiently low resistance of the ESD diode but at the same time a sufficient isolation of between the standard cells a trade-off has been done.
The targeted depth of the box isolation is $\approx 2\mu m$.
The STI area will be everywhere, where no well areas are.
We use a dry etching method for cutting into the silicon substrate and making the active area become islands with trenches in between.
After that we fill the trenches with LTO and polish the wafer until the LTO surface and the silicon island surface are sufficiently on the same level.
Our minimum width and height as well as the space between the active areas comes from the line space constrain of the silicon etcher and of course the optical limitations of the stepper which are as well $0.5\mu m$.

2.1 CMP end stop

In order to prevent irreversible damage to the crystal lattice of the active area, we need to provide a CMP end stop on top of those areas.
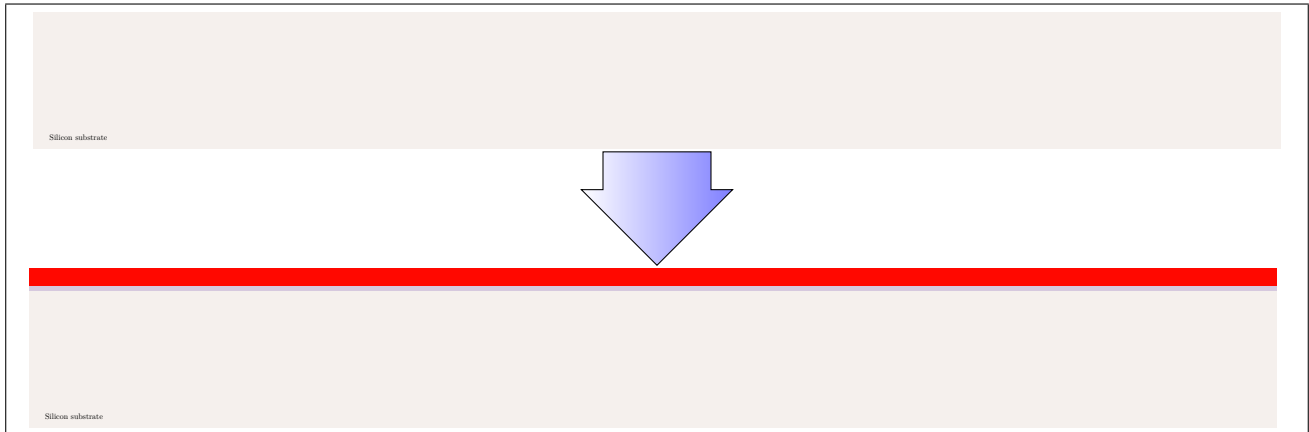

Figure 4: End stop

The wafer is cleaned by being put into sulfuric acid at $120°C$ and afterwards HF dipped in order to remove the native oxide. After that a more uniform and very thin film of thermal oxide is being grown, the thickness can be around 10nm, this can be achieved by putting the wafer into a furnace at $1000°C$ for 15 minutes in an O_2 environment (dry oxidation). On top of this pad oxide, a layer of around 100nm of nitride is being deposited, using chemical vapor deposition.

2.2 Silicon etching

The trench depth has to be at least 2 microns and less than 4 microns deep, in order to have a sufficiently good isolation for preventing latchup effects and at the same time still good enough ESD diode behaviour.
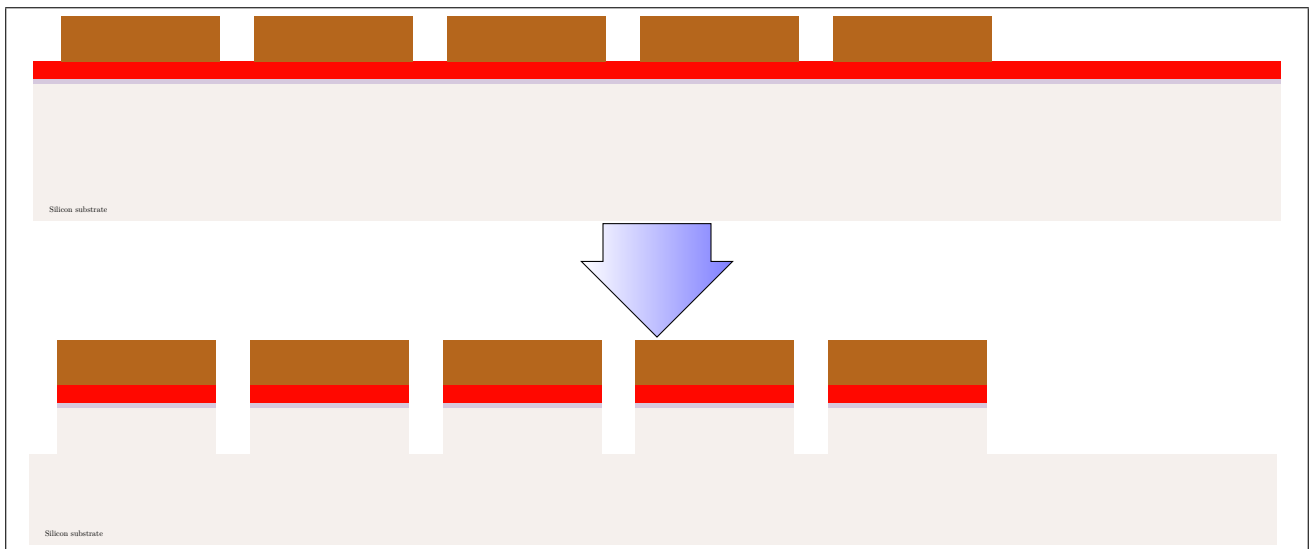

Figure 5: Trench etching

After patterning the STI layout the resist is being hard baked and the nitride+pad oxide is being etched, using plasma etching for nitride+oxide.
After etching the nitride and oxide we use a DRIE etcher and set the number of cycles in a way that it results in around 2 microns trench depth.
Adding to the over etch from the previous etch step, this will result in a depth a little bit deeper than 2 microns.

2.3 Liner oxide

In order to improve the interface properties of the LTO deposited in subsection 2.4 to the side walls of the silicon islands a thin layer of thermal oxide is being grown after DRIE etching.
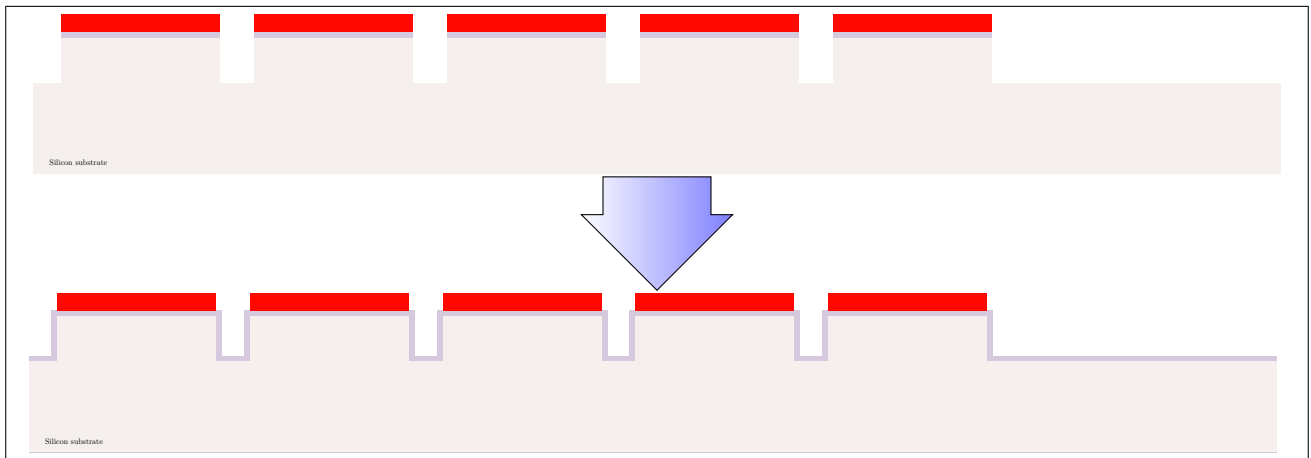

Figure 6: Liner oxide

The interface oxide, as the pad oxide, only has to be a few nanometers in thickness, this can be achieved by putting the wafer again into a furnace at $1000°C$ for 15 minutes in an O_2 environment (dry oxidation).

2.4 LTO deposition

Now we fill up the trenches we've etched before with LTO for further planarization in subsection 2.5
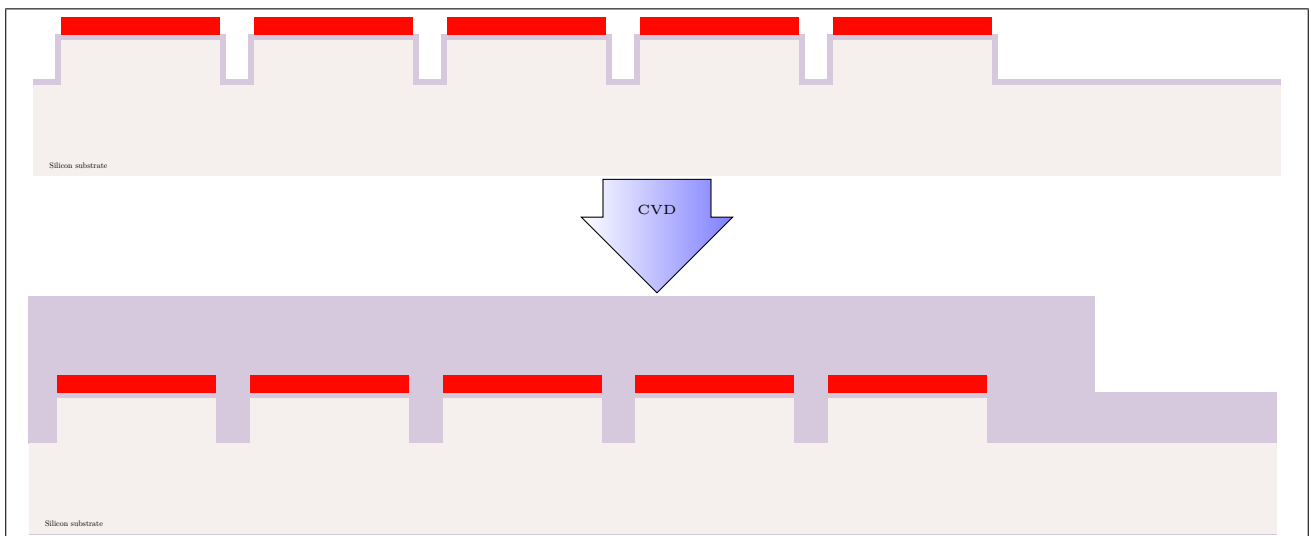

Figure 7: Oxide deposition

The easiest method is to put the wafer into a CVD furnace in order to deposit around 2 microns of LTO.
Better uniformity of the LTO film can be achieved by getting the boat out after every deposited 500nm, rotating it 90 degrees and putting it back in for another deposition round.
Also remember to measure the thickness of the deposited LTO under a spectroscope, in order to calculate the approximate CMP time!

2.5 CMP step

Now the LTO needs to be planarized until a sufficiently low height differential between the oxide surface and the silicon surface is being met.
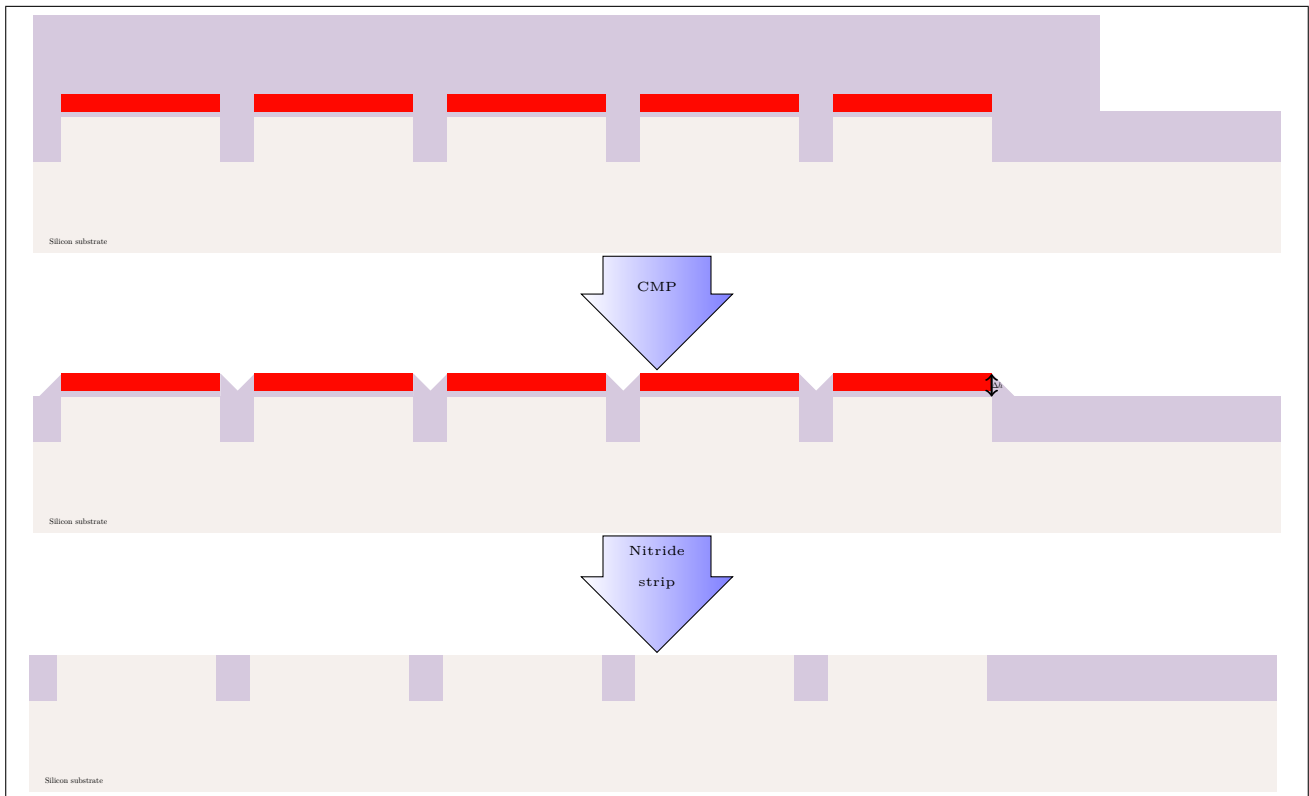

Figure 8: After CMP

A CMP is performed, based on a rough time calculation, based on the thickness measurement from [subsection 2.4](#), until a height differential (See Δh in graphics) below 200nm is being reached, which can be determined by using a surface profiler.

If available the slurry "SRS-985" should be used because it can significantly increase the yield by reducing the dishing as a study has found[1].

After the planarization the wafer needs to be cleaned in hot ammonia and with RCA solution and wafers should kept wet in DI water after CMPing and should not dry out before being cleaned, because this would make particles get stuck in the oxide permanently and will destroy the sample.

After cleaning the LTO has to be annealed in order to increase the etching time when removing the pad oxide: The sample is being put into a furnace for 30 minutes at $850°C$ in an inert atmosphere (N_2/Ar).

The densification is being performed before nitride strip, because the Phosphoric acid also attacks oxide, and by hardening the LTO first, we can reduce the amount of oxide, which is being removed alongside the nitride.

After the annealing the nitride is first stripped in a suitable nitride etchant like Phosphoric acid or the like.

After that the pad oxide beneath is being removed by being put into BOE for a few minutes until the pad oxide has been removed.

In this process, the sharp corners of the craters in the oxide, where the nitride used to be will also be smothened out, which is a nice side effect.

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[1] `https://download.libresilicon.com/papers/10.1.1.567.8814.pdf`

3 Tripple Well

In order to build BiCMOS we need nested wells for getting the vertical diode structures which form the bi junction transistors.

A vertical isolation, which allows us to have some bulk areas on a higher potential than others, and isolated FETs come along from this tripple well architecture for free.

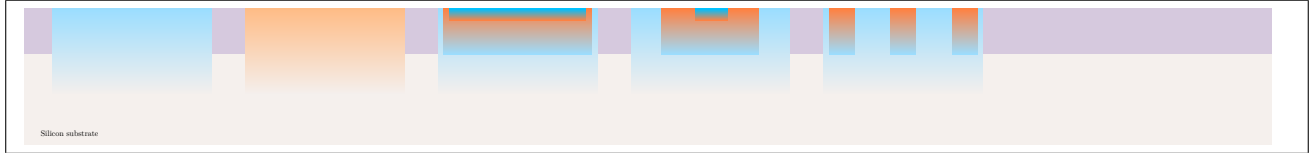The cross section of the targeted geometry are shown in Figure 9

Silicon substrate

Figure 9: Tripple well target geometry

Since the diffusion constant variates with the concentration of background dopants, we have to make sure that the thermal budget has enough slack during every single tripple well formation step, in order to avoid the consumption of one of the wells during further processing.
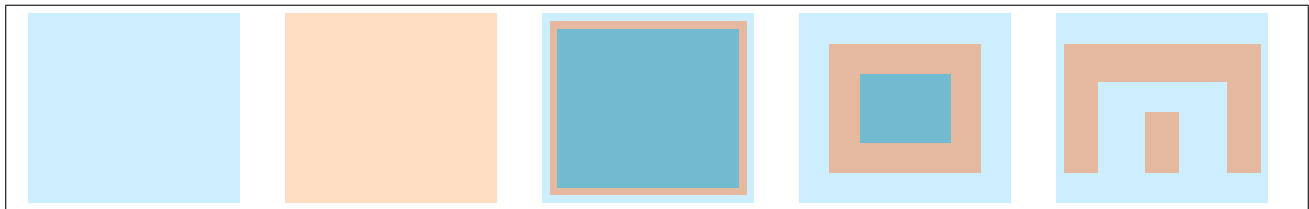

Figure 10: Tripple well layout

In Figure 10 the layout of the well and base regions on top of the active area region can be seen.

The implant values are as calculated in the documentation of the process design leading to these steps[2].

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[2]https://download.libresilicon.com/process/v1/process_design.pdf

3.1 N-well

In order to build CMOS on the same substrate, an N-well is required for building the complementary P-channel transistor for a NFET+PFET logic circuitry.
The cross section as well as the top view of the targeted geometry are shown in Figure 11
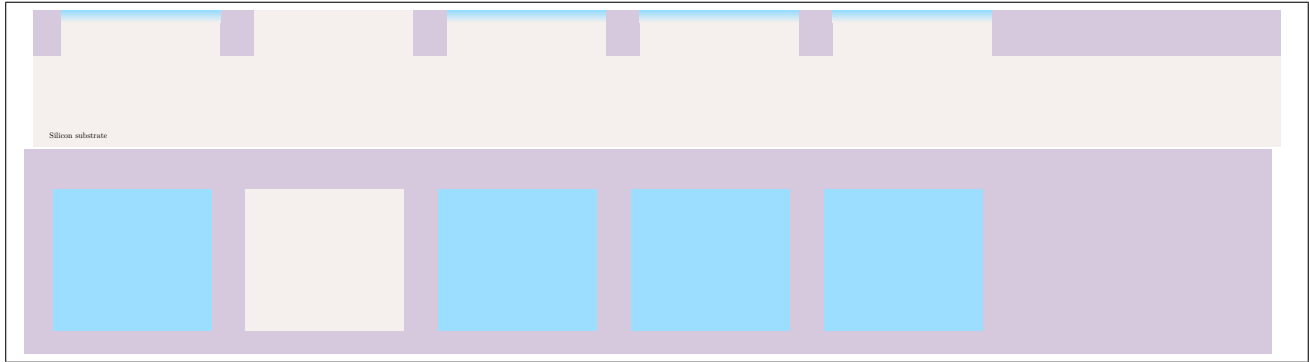

Figure 11: N-well target geometry

The N-well will serve us as an island of N-doped substrate within the P-doped basis substrate.
The P-dopant concentration of our prime grade, p-type, single side polished, four inch wafers is between $8.76 \cdot 10^{14} \frac{1}{cm^3}$ and $5.23 \cdot 10^{14} \frac{1}{cm^3}$
This means we need a dose of $2.33 \times 10^{12} cm^{-2}$ Phosphorus at 70 keV.
The concentration will need adjustment when the used substrate has different properties!

3.2 P-well

In order to build CMOS on the same substrate, a P-well is required for building the complementary N-channel transistor for a NFET+PFET logic circuitry.
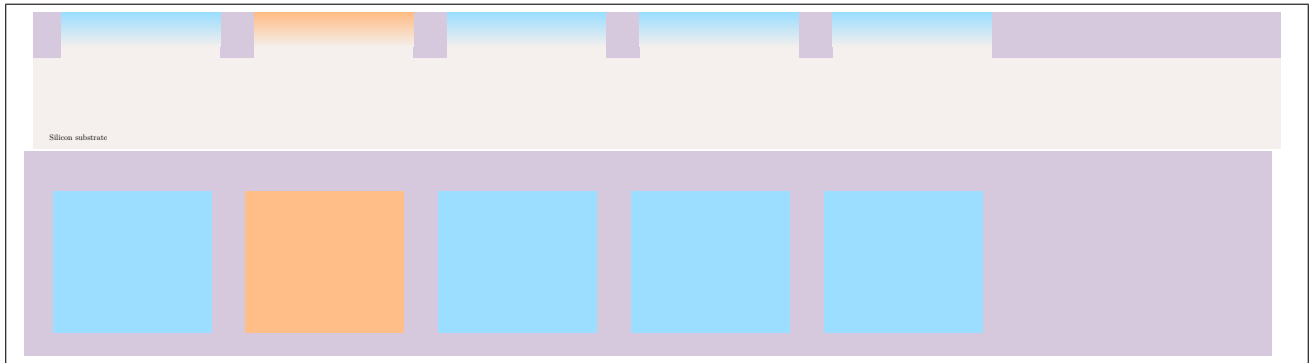The cross section as well as the top view of the targeted geometry are shown in Figure 11

Figure 12: P-well target geometry

The "P-well" will serve us as an island of higher p-doped substrate within the slightly p-doped basis substrate and gives us more flexibility with suppliers, because we can just adjust the doping in case the concentration might be different with another supplier.
The P-dopant concentration of our prime grade, p-type, single side polished, four inch wafers is between $8.76 \cdot 10^{14} \frac{1}{cm^3}$ and $5.23 \cdot 10^{14} \frac{1}{cm^3}$
This means we need a dose of $1.93 \times 10^{12} cm^{-2}$ Boron atoms at 40 keV.
The concentration will need adjustment when the used substrate has different properties!
After the implantation we perform a drive-in in inert atmosphere at 1050°C for two hours and don't have to worry about the substrate anymore.

3.3 P-base

In order to build BiCMOS on the same substrate, a nested P-well within the N-well (now it's twin well) is required for building the bipolar junction transistors.

The cross section as well as the top view of the targeted geometry are shown in Figure 13
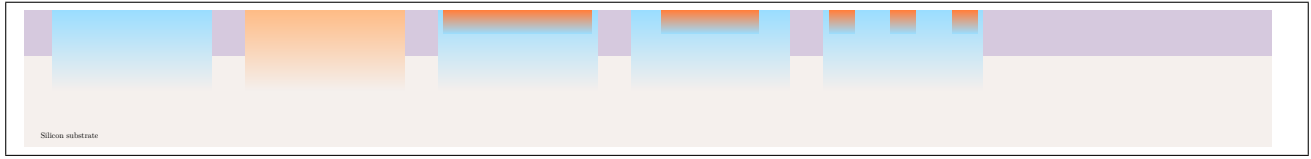

Figure 13: P-base cross section

The P-base will serve us as an island of higher P-doped substrate within the slightly N-well basis substrate, which will result in a isolated area by forming PN junction versus PN junction.

The dopant dose will be $1.93 \times 10^{12} cm^{-2}$ at 40 keV.

The P-base can very well cover the N-well area since the expansion mostly is vertical, but it should be kept in mind, that there is also a lateral diffusion when placing contacts also on N-well around the P-base.

After the implantation we perform a drive-in in inert atmosphere at 1050°C for one hour.

3.4 N-base

In order to build BiCMOS on the same substrate, another N-well within the P-Base (tripple well!) is required for building the complementary isolated P-channel transistor for a n-p-channel logic circuitry as shown above in the example section.

The cross section as well as the top view of the targeted geometry are shown in Figure 14
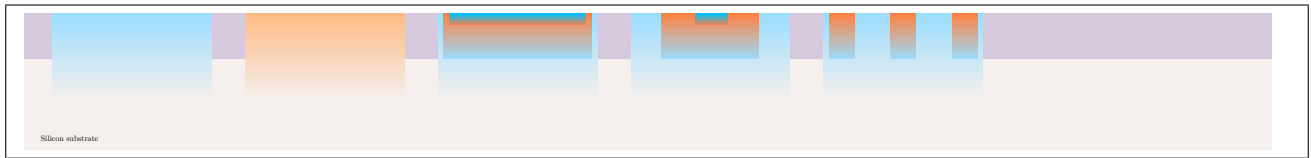

Figure 14: N-base target geometry

The N-well will serve us as an island of N-doped substrate within the P-doped basis substrate.

The dopant dose will be $2.33 \times 10^{12} cm^{-2}$ at 70 keV.

After the implantation we perform a drive-in in inert atmosphere at 1050°C for 30 minutes.

4 Field oxide

The geometry of a substrate with the field oxide filling the shallow trenches from section 2 now needs to be made.
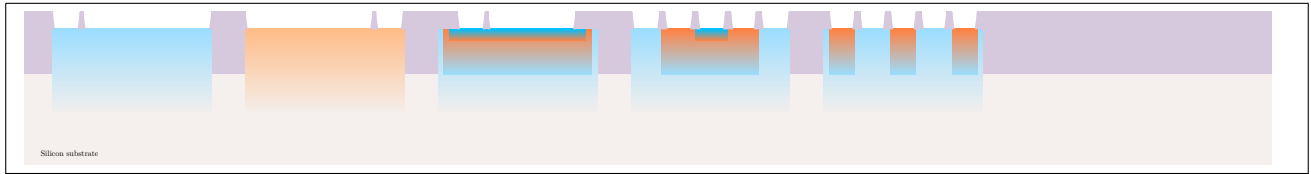

Figure 15: Shallow trench isolation target geometry

As can be seen in Figure 15, the islands need to be covered with silicon oxide and windows need to be etched into the oxide so that the gate can be constructed later on.

The covering oxide and windows are needed so that the poly silicon is far enough away from the non-active areas so that the threshold voltage of the parasitic FETs is so high that they will never switch.

Only within the active areas we want to allow the poly layer to touch down closer to the silicon.

The mask is called "fox" on the mask set.

The LTO thickness has been chosen to be 200nm which is thin enough for the polysilicon gates to overcome the height difference without damage and still being enough for eliminating parasitic effects.

4.1 Oxide deposition

Now we need to deposit the silicon dioxide which will provide a spacer between the non active area and the polysilicon gate layer within the non-active areas.
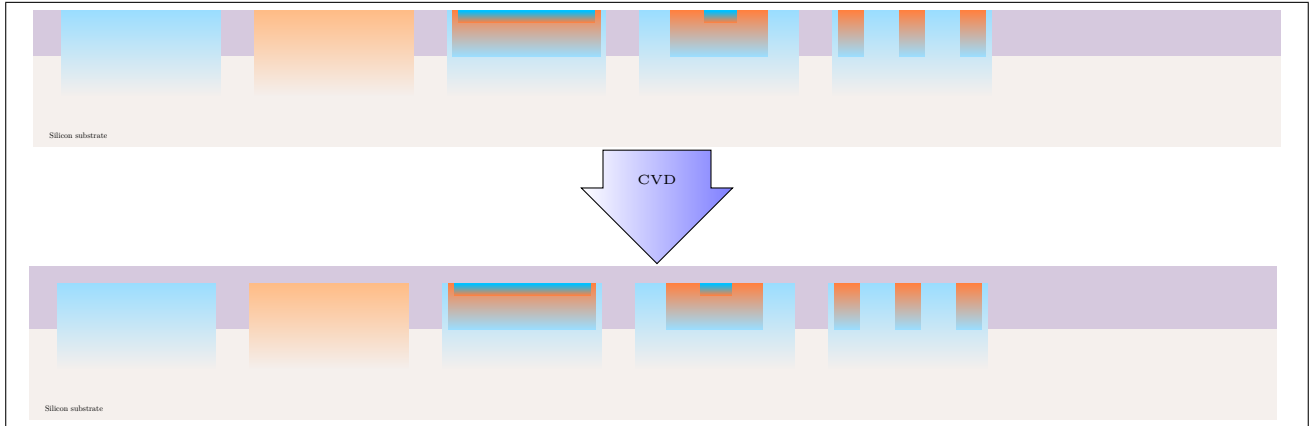

Figure 16: LTO deposition

We deposit a roughly 200nm thick layer of LTO by putting the wafer into the LPCVD furnace.

4.2 FOX opening formation

We open the access to the silicon inside of the active areas in order to touch down with the polysilicon further on.
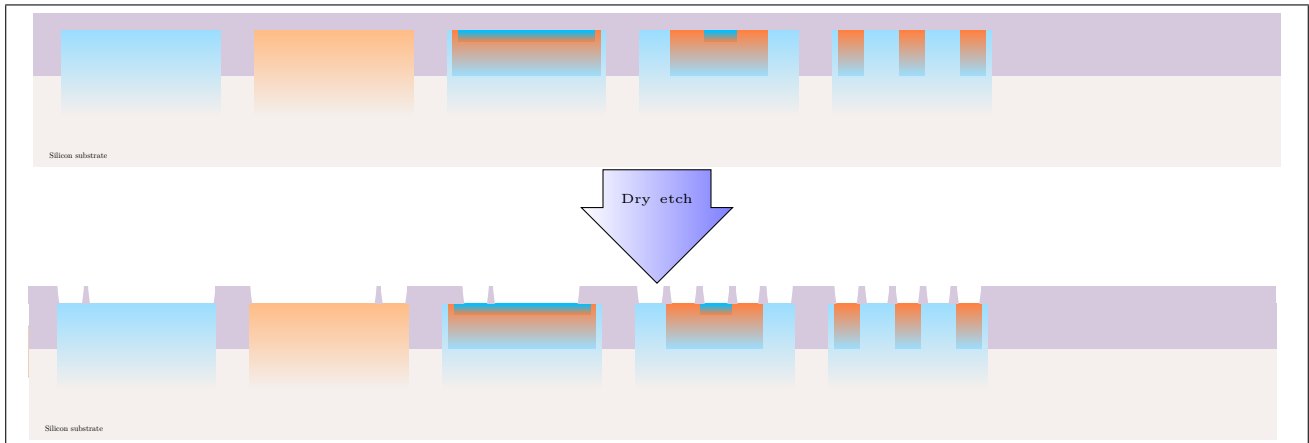

Figure 17: LTO etching

The etching time variates from machine to machine and recipe to recipe. Do the math.

After having etched through the LTO we have to make sure that the etching time goes up compared to the undensified LTO+nitride, which will be etched in section 5. For this reason, we put the wafer into the furnace and anneal the LTO for 30 minutes at $850°C$ in inert atomsphere (N_2/Ar).

5 SONOS

Before we can construct the gate, we have to put some pads of oxide-nitride-oxide sandwich roughly in the area where the SONOS (silicon oxide nitride oxide silicon) gates will be located.

Later on, during etching of the polysilicon gates, the SONOS gate oxide sandwich will be automatically aligned with the gate because excess SONOS sandwich material will be etched away with the normal gate oxide.
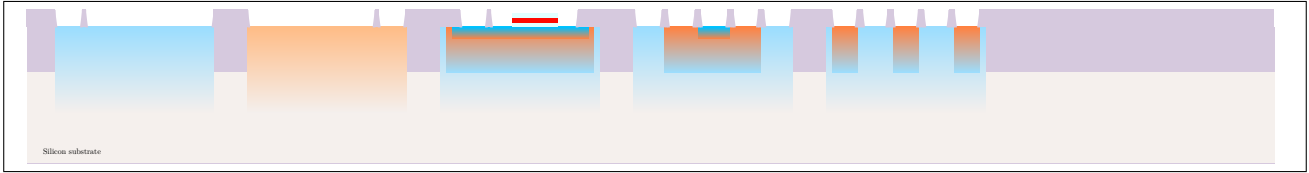

Figure 18: SONOS sandwich pad

The line spacing of the SONOS shape has to be at least $0.5\mu m$ because of the resolution of the stepper and also because of the etching process which has $0.5\mu m$ as the minimum line spacing.

Also there has to be at least one lambda on each site to compensate for offsets, so the SONOS mask is bloated by $0.5\mu m$.

The SONOS gate oxide is comprised of a stack of oxide covered with nitride covered with oxide.

The upper and lower oxide layers are the so called tunnel oxides which allow electrons during the programming phase to be tunneled into the nitride, where they get trapped and shift the threshold voltage of the transistor. This way information can be stored and erased by tunelling the electrons back out of the nitride.

This ONO (oxide nitride oxide) pad will prevent the additional thin oxide from forming during the gate oxide formation in subsection 6.1 and instead the LTO under and above the nitride will be densified during the process step.

5.1 Lower oxide deposition

Now we have to deposit the lower part of the SONOS sandwich by depositing LTO.
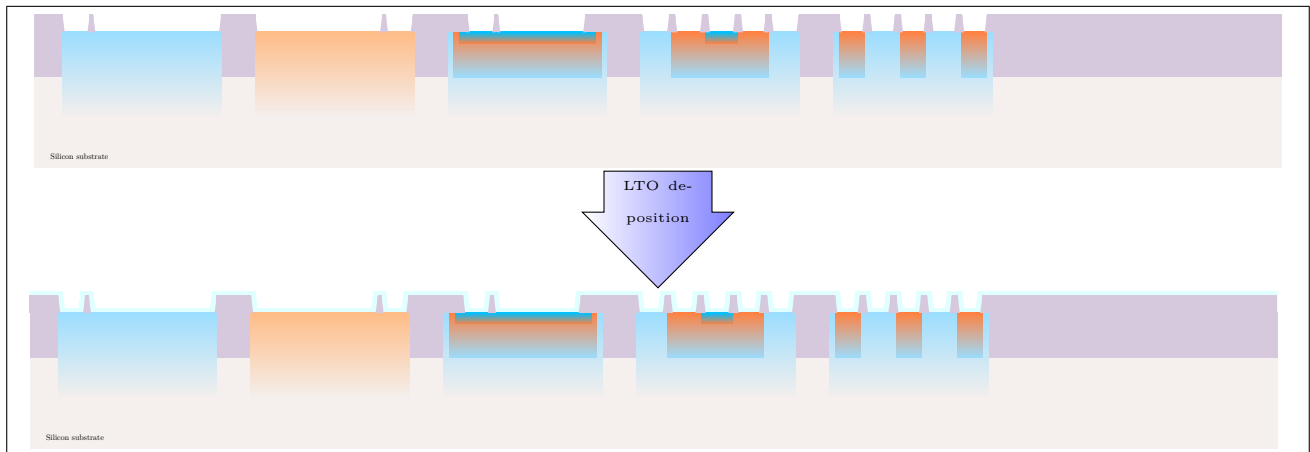As designed in the process design document, the layer will be around 5nm thick.

Figure 19: Thin oxide

This might be difficult depending on the CVD machine used. Typically a reduced pressure can reduce the deposition rate, do not reduce the temperature however, since this can cause the formation of grains.

5.2 Silicon nitride deposition

Now we need to add the nitride layer for forming the SONOS sandwich.
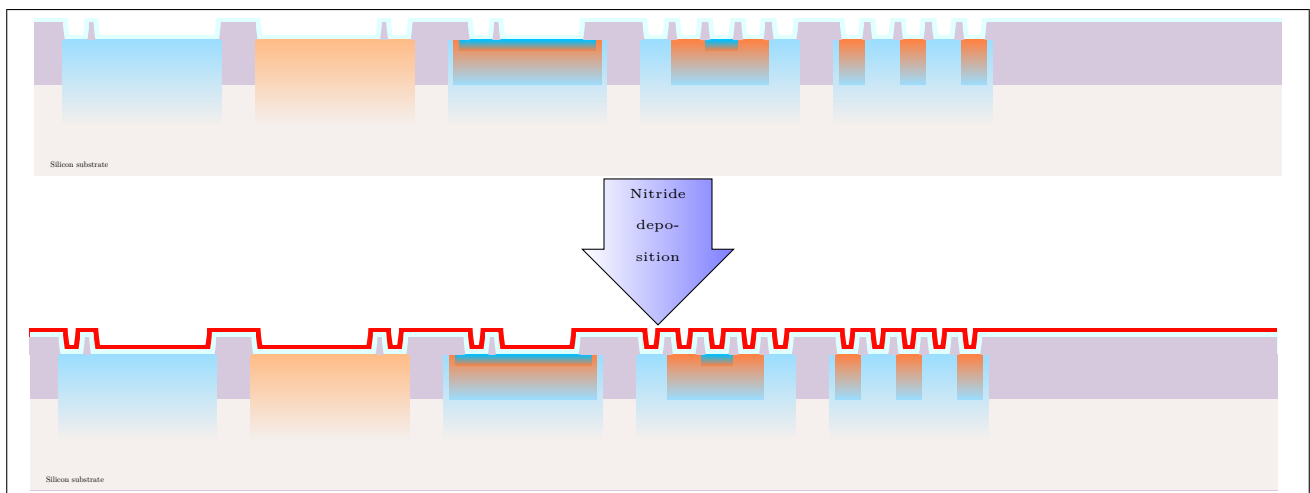

Figure 20: Polysilicon

We use the LPCVD machine and deposit a layer of around 7nm nitride.
Since the deposition rate of nitride in a CVD furnace is by nature quite slow (usually 2nm per minute) we have a much better control over this thickness.

5.3   Upper oxide deposition

Now we have to deposit the upper part of the SONOS sandwich by depositing LTO.
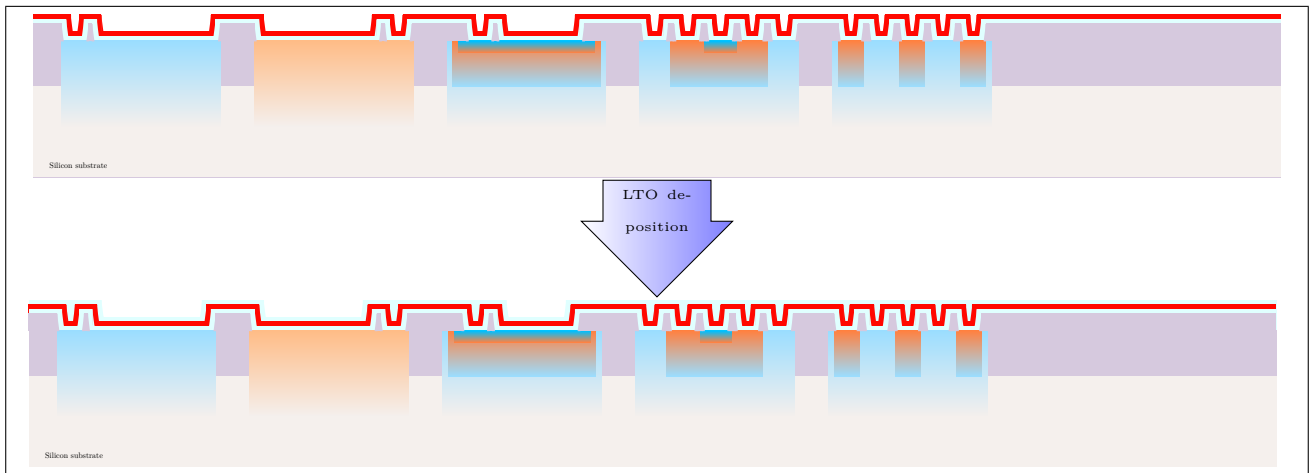As designed in the process design document, the layer will be around 5nm thick.

Figure 21: Thin oxide

It's exactly the same recipe as for the first oxide deposition step.

5.4   Etching

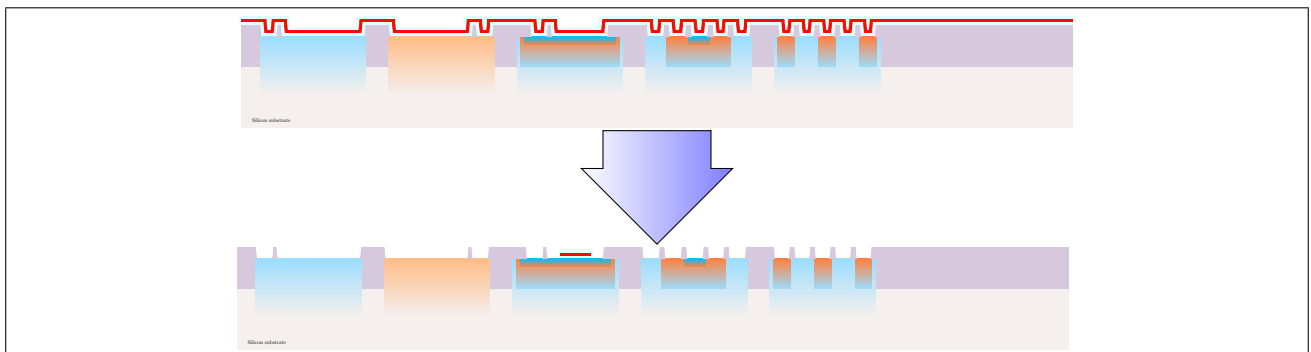Now we've got to etch the SONOS structures.

Figure 22: Resist

The etching time depends on the dry etcher and recipe used.

6 Gate

Now we have to build the initial gate structure which contains of the 40nm thick dielectric (in our case just silicon dioxide) and the polysilicon electrode.
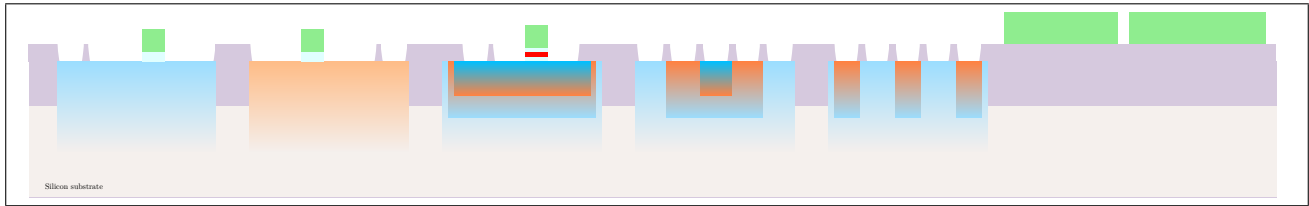

Figure 23: Poly silicon gate contacts with gate oxide

The line spacing of the polysilicon electrode shape has to be at least $0.5\mu m$ because of the resolution of the stepper and also because of the etching process which has $0.5\mu m$ as the minimum line spacing.

The underlying ONO sandwich, which has been formed in section 5, which has a spacing of at least a lambda on each side, towards the gate structure, in order to compensate for alignment errors will first get its LTO densified during the gate oxide formation phase, and will afterwards experience an alignment with the gate structure during dry etching and its over etching phase.

6.1 Gate oxide formation

Now we have to deposit the dielectric isolator between the gate electrode and the channel. As designed in the process design document, the layer will be 40nm thick.
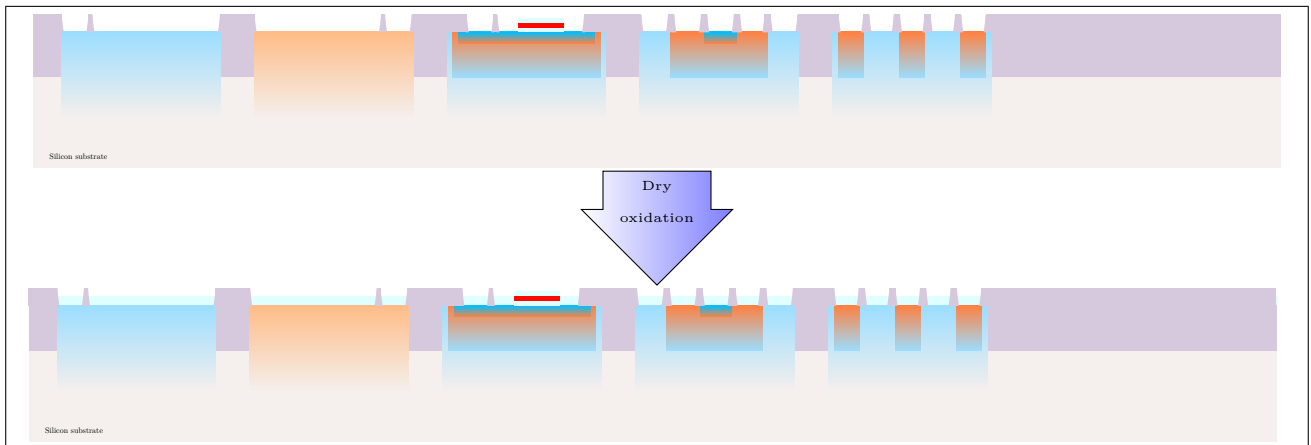

Figure 24: Thin oxide

The thickness of this layer decides over many critical key properties of the transistor, hence there should be little to no variation in the thickness of the gate oxide layer. For that reason we put the wafer into the diffusion furnace and perform dry oxidation at $1050°C$ for 33 minutes and 14 seconds.[3]

6.2 Polysilicon deposition

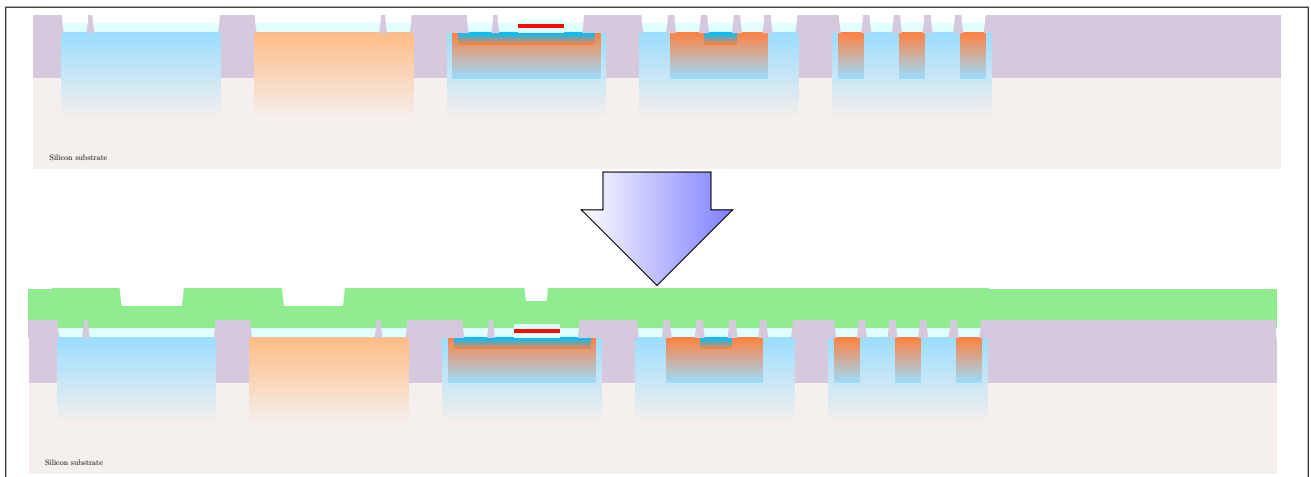Now we need to add the polysilicon layer for forming the gate structure after etching.

Figure 25: Polysilicon

We use a LPCVD machine or CVD furnace and deposit a layer of around 250-300nm polysilicon.

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[3]http://cleanroom.byu.edu/OxideTimeCalc

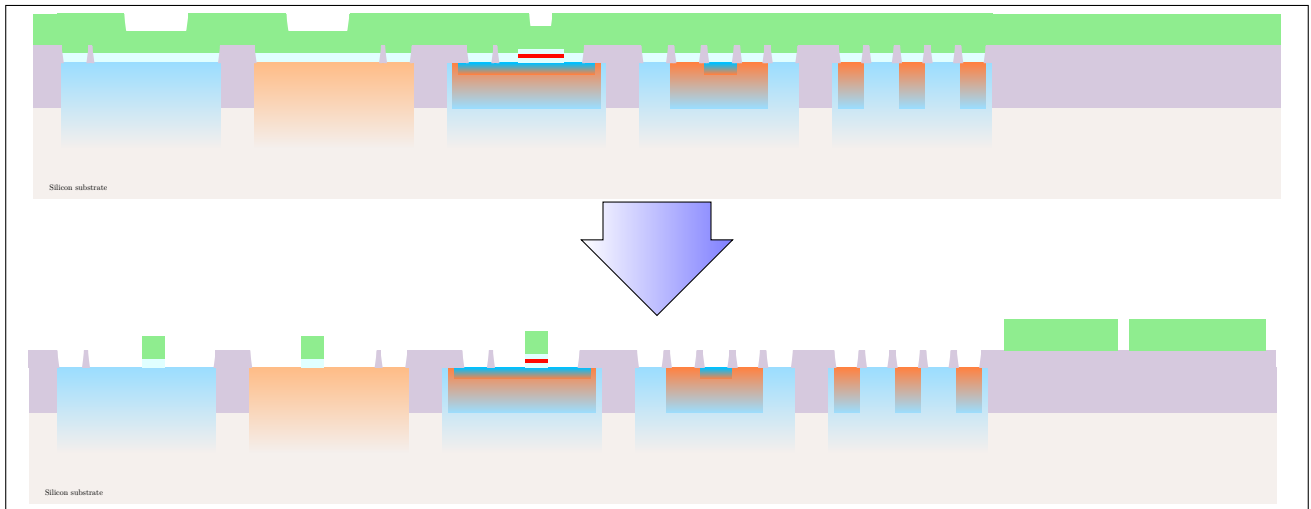## 6.3 Etching

Now we've got to etch the gate structures.

Figure 26: Resist

In order to avoid sidewall residue of polysilicon, which might lead to short circuits, you over etch sufficiently by adding the etch time for the height differential for the etch rate of polysilicon.

7 Junction implants

After we've etches the gate structures and have implemented the implant stop structures we perform the junction implants in subsection 7.3 and subsection 7.2.

Thanks to the implant stop mask we have a nice control over channel lenghts because the implant stop structure compensates for alignment issues, which is crucial for Polysilicon diodes for instance.
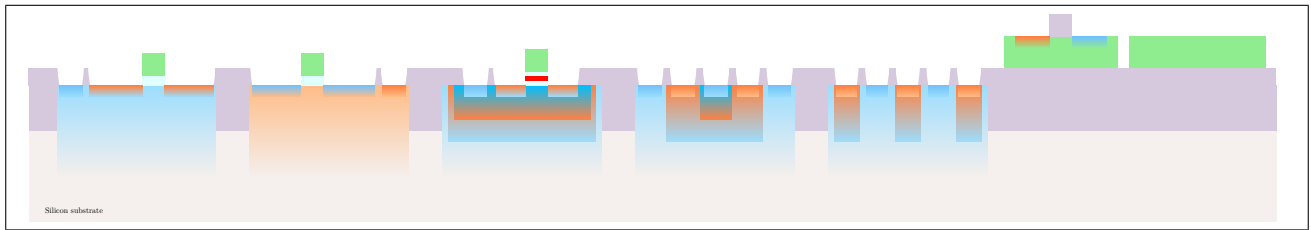

Figure 27: P+ and N+ junctions

After implantation we have to drive in the shallow junction implants in order to form the pn-junctions in the polysilicon gates and to increase the depth of the junctions to a degree so that it won't be fully consumed during the silicide formation(section 8) step later on.

After we've implanted the Boron and Phosphorus, we will drive the whole thing in for 30 minutes at $900°C$ and at the same time oxidize it with O_2 (dry oxidation) so that we can form the pad oxide needed to deposit the nitride for the side wall spacers later on in subsection 8.1.

7.1 Implant stop

In order to have a control on where the junction dopants from subsection 7.2 and subsection 7.3 are being placed in the active area we use a layer of oxide as a hard mask. This is important for controlling the Zener diode break down voltage.
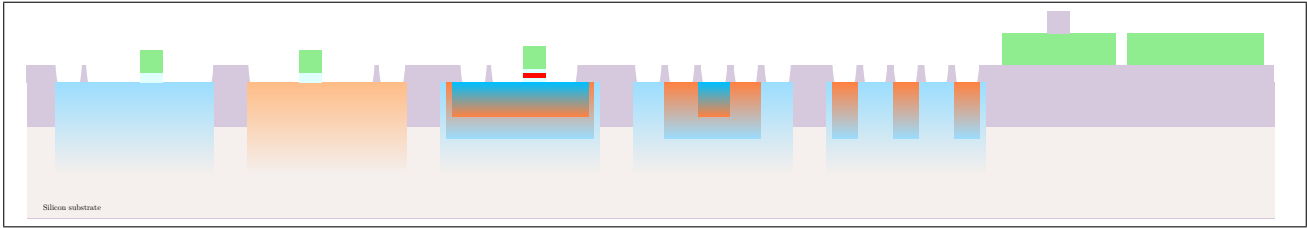

Figure 28: Implant stop target

Because of the energy, with which the dopants are implanted (range straggle), a thickness of 200nm is being chosen for the LTO deposition, in order to make sure, that all the dopants are being absorbed within the LTO.

7.2 n+ Implant

For the bulk of the PMOS transistors and for the source and drain of the NMOS transistors highly doped n+ areas are required.
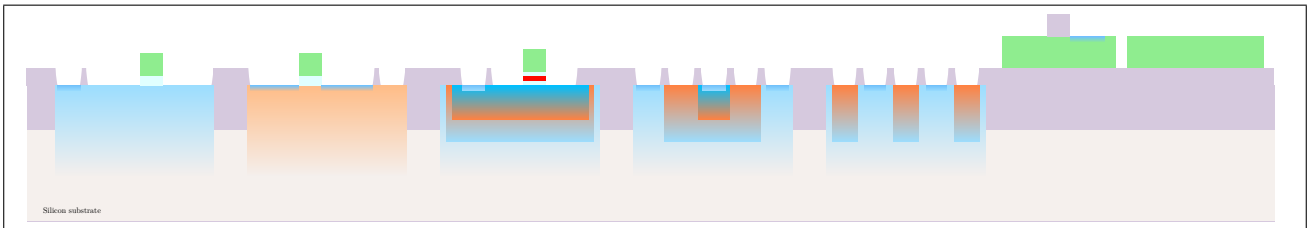In this step we're going to build these.

Figure 29: N+ implant geometry target

The tricky thing here is to have a reasonable implant depth but not too deep because the deeper the junction, the higher the junction capacity which in turn limits the switching performance of the CMOS circuitry.
Also important to notice is that the implantation energy must not be too high, otherwise the dopants may leak through the polysilicon gate.
The nselect is implanted with a Phosphorus (P^{31}) dose of $2.5 \times 10^{12} cm^{-2}$ at an energy of 30 keV (43nm±18nm deep)

7.3 p+ Implant

For the bulk of the NMOS transistors and for the source and drain of the PMOS transistors highly doped p+ areas are required.
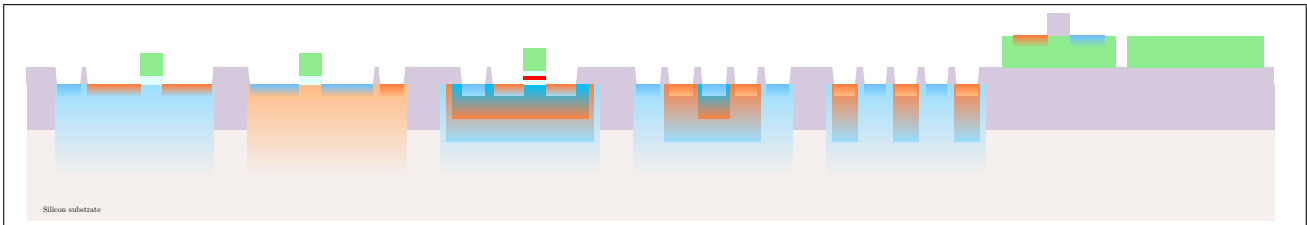In this step we're going to build these.

Figure 30: P+ implant geometry target

The tricky thing here is to have a reasonable implant depth but not too deep because the deeper the junction, the higher the junction capacity which in turn limits the switching performance of the CMOS circuitry.
Also important to notice is that the implantation energy must not be too high, otherwise the dopants may leak through the polysilicon gate.
The pselect is implanted with a Boron (B^{11}) dose of $2.5 \times 10^{12} cm^{-2}$ at an energy of 20 keV (43nm±18nm deep)

8 Silicification

Titanium silicide is one of the first SALICIDE material introduced in ULSI devices owing to its low resistivity, high thermal stability, ease in deposition and compatibility with silicon processes. Titanium has been one of the familiar materials in ULSI productions, which is also an important advantage in practical use of titanium SALICIDE.[4]
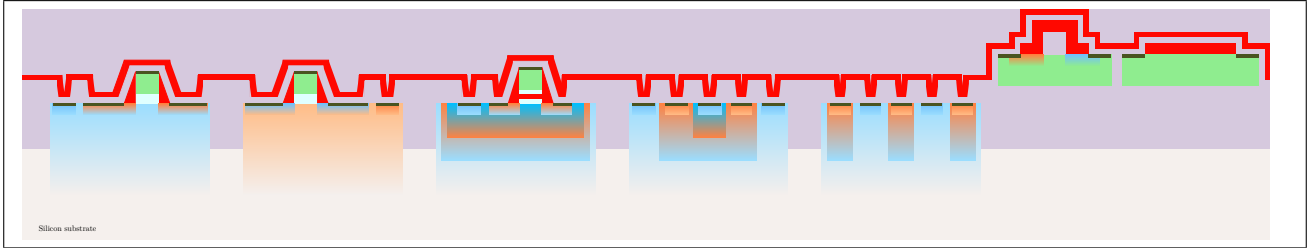

Figure 31: Silicide geometry target

In order to reduce the gate contact resistance as well as the source and drain resistance and in order to provide a more effective etch stop when plasma etching the contact windows to drain, source and gate, silicide/polycide is being added to the wafer as shown in Figure 31.

The side walls[5] are required in order avoid short circuits between the junction and the gate.

When titanium and silicon are brought into contact and heated at temperatures above 800 °C (in the presence of excess silicon) $TiSi_2$ forms.

The $TiSi_2$ has a resistivity of $12 - 20\mu\Omega - cm$.

The basic formation process of titanium SALICIDE is as follows:

A thin titanium film of roughly 30 nm thickness is deposited on an entire wafer with MOSFETs structure.

The deposited Ti film reacts with the exposed silicon areas such as the source/drain area and polysilicon gate electrodes during the annealing at 800°C in Argon atmosphere.

Then, the unreacted titanium film on the dielectric layer such as SiO_2 or SiN is selectively etched by RCA-1 (Ammonia and Hydrogen Peroxide Mixture) solution for around 2-3 minutes.

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[4]A Study on Formation of High Resistivity Phases of Nickel Silicide at Small Area and its Solution for Scaled CMOS Devices, 07D53437, Ryuji Tomita

[5]http://www.fujitsu.com/jp/group/mifs/en/resources/news/library/tech-intro/process/side-wall.html

8.1 Nitride deposition

The thickness of this CVD deposited nitride layer will be the width of the spacer after having used highly anisotropic etching in the next few steps, for this reason the thickness of the nitride decides over the distance between the silicide and the gate oxide.

Considering, due to the edge effects during dry etching, the thickness of the nitride has to be less than 25% of the polysilicon thickness, we choose 50nm for the nitride thickness.
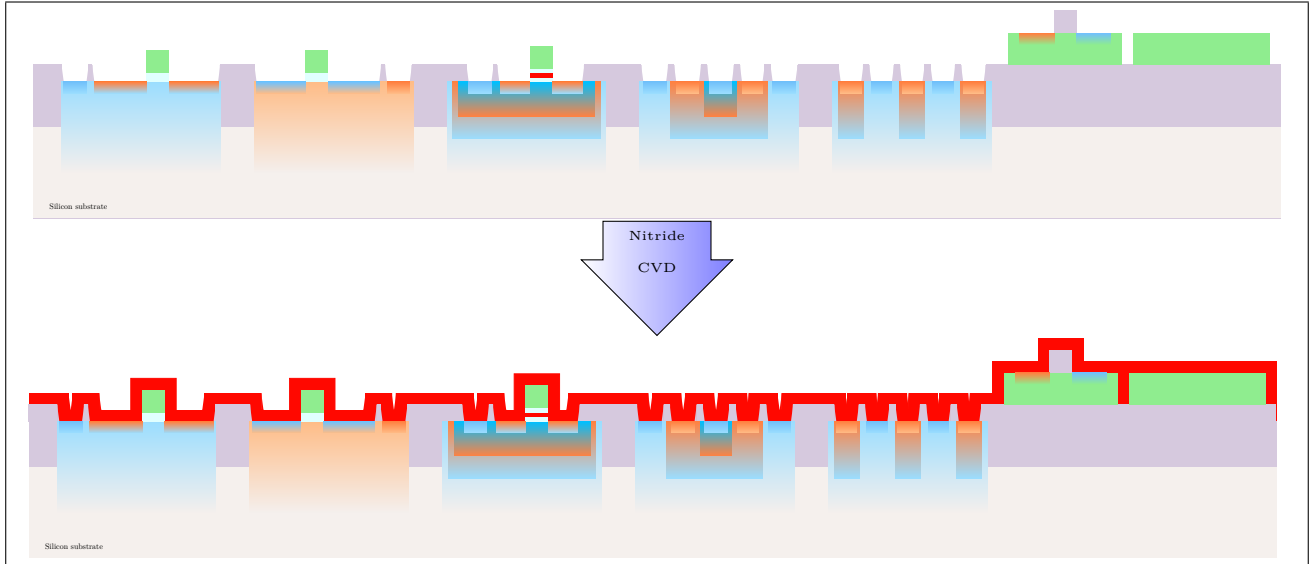

Figure 32: Nitride layer

The deposition rates might variate between LPCVDs and recipes. It's at the discretion of the operation engineer to achieve those 50nm.

8.2 Spacer etching

Now we have to etch our nitride as anisotropic as possible.

This means that the etching mostly only comes "from above" with a few to nearly none horizontal etching.

Thit means the etching process only "sees" the sidewall as a "thicker layer" and starts etching downward.
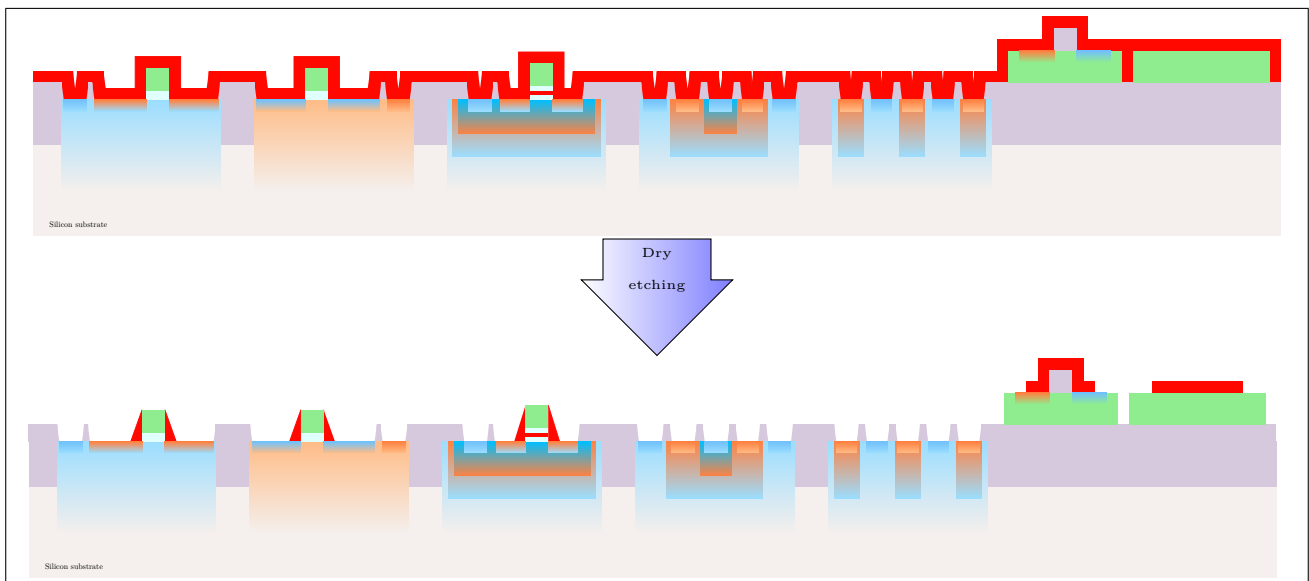

Figure 33: Anisotropic etching

After that we will have our desired spacer geometry forming as well as any potentially resist covered area from the silicide block mask patterns, which will allow us to control in which areas we reduce the sheet resistance in which we don't.

8.3 Titanium deposition

We deposit a layer of titanium with a thickness of between 30nm to 50nm which will then be reacted into titanium-silicide and titanium-polycide respectively in the further steps.
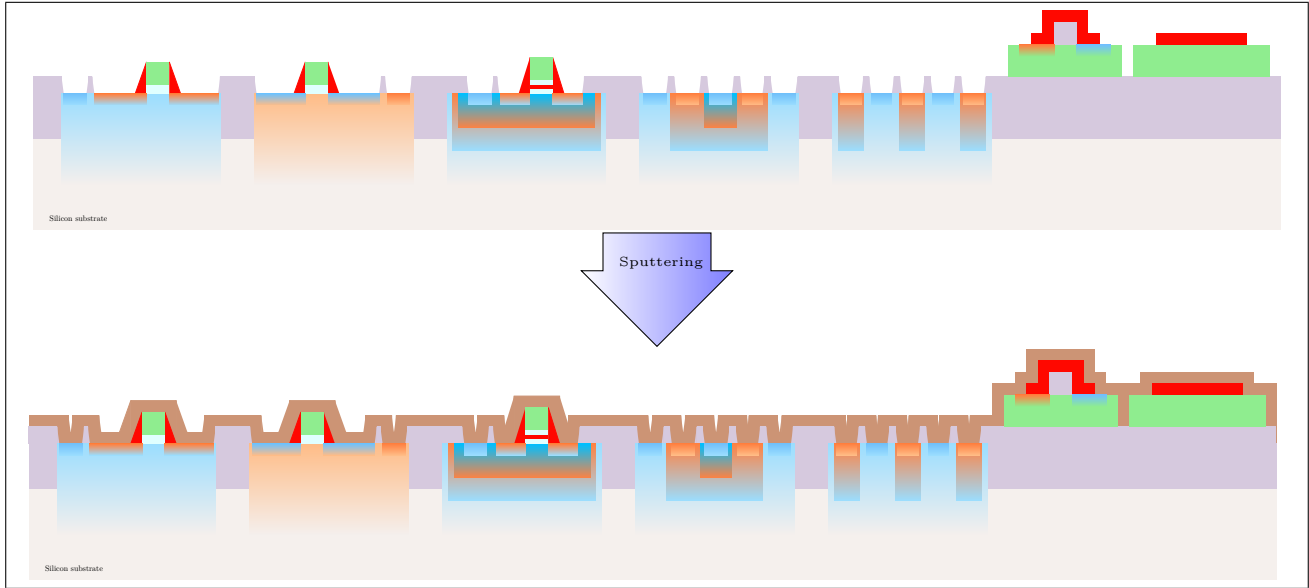

Figure 34: Titanium deposition

The titanium can either be applied by sputtering or by chemical deposition.
Depending on the technique of sputtering or deposition, the capabilities to deposit only 30nm may not be given. It should however be avoided to deposit too much titanium (more than 100nm or so), because the etch rate of RCA-1 at room temperature has a very good selectivity towards titanium compared to $TiSi_2$ but is not 100% perfect, which might lead to partial etching of the $TiSi_2$ film which might negatively impact the sheet resistance properties of the devices.

8.4 Silicide formation

The deposited Ti film reacts with the exposed silicon areas such as the source/drain area and polysilicon gate electrodes during RTP (Rapid Thermal Processing) at $800°C$ in Argon ambient for 30 seconds.
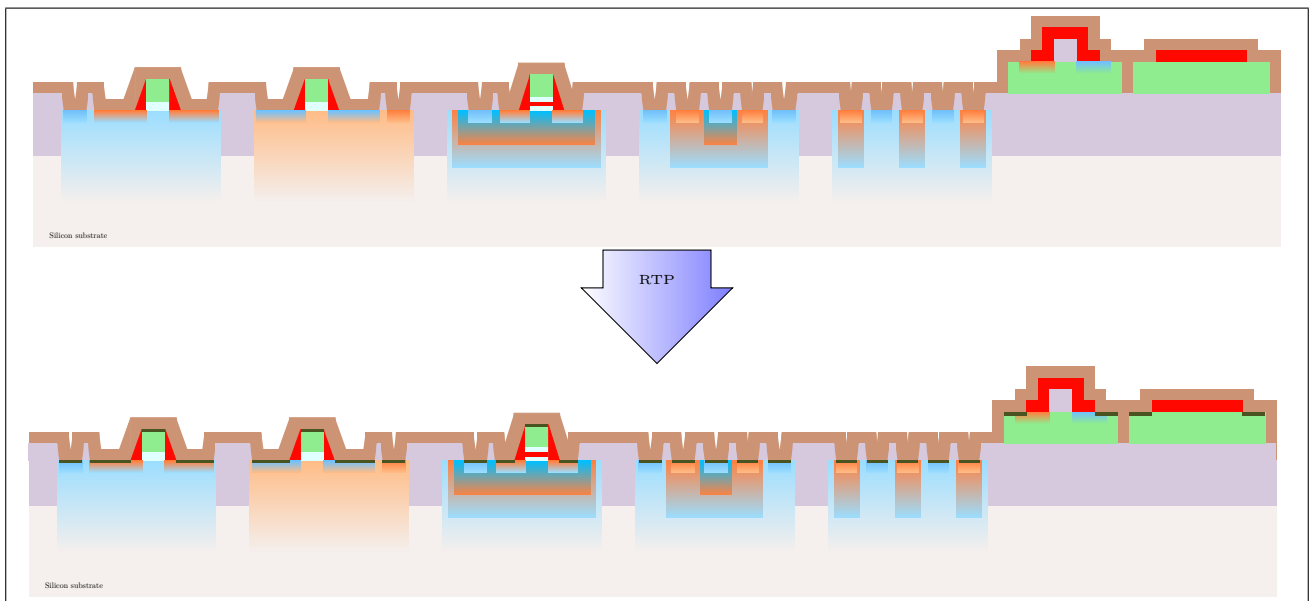In this annealing step the $TiSi_2$ is formed.

Figure 35: RTP treatment

The resulting $TiSi_2$ film will be around 77nm in tickness with around 20nm unreacted titanium left on top.

A color change into a slightly brownish color from originally silver metallic can be observed of the titanium on top of the oxide.

8.5 Metal removal

The unreacted titanium film on the dielectric layer such as SiO_2 or SiN is selectively etched by RCA-1 (Ammonia and Hydrogen Peroxide Mixture) solution.
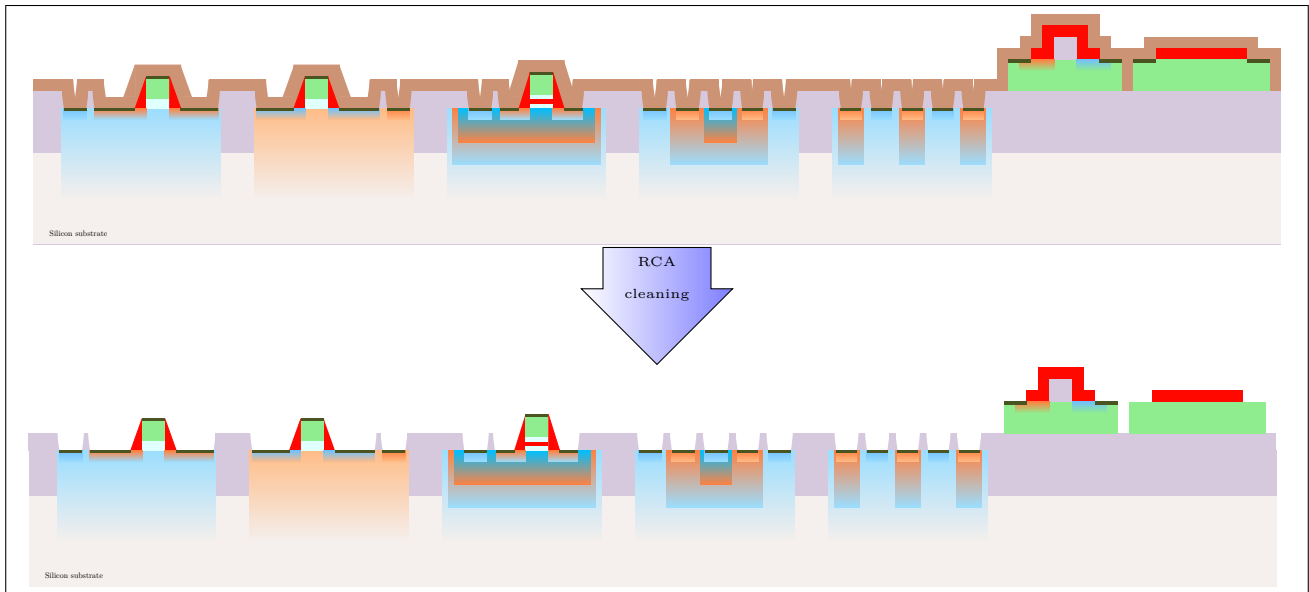

Figure 36: Titanium etch

After 2-3 minutes in RCA-1, at room temperature, with a bit mechanical help, all the unreacted Titanium should be gone and the oxide should become visible again. Under **no circumstance** use a solvent containing HF, since $TiSi_2$ dissolves in HF or any other Fluoride containing solutions.

Better cleaning results can be achieved by adding mechanical stress to the unreacted metal while having it inside the RCA-1 solution, so if you can put it into an ultrasonic bath, the RCA-1 cleaning results can be improved by this.

8.6 CMP

After we formed all the active devices and added the silicide in order to reduce the sheet resistance of junctions and contacts we have to make sure that our devices will not be damaged during the planarization phase in order to contact through to them with the first metal layer.
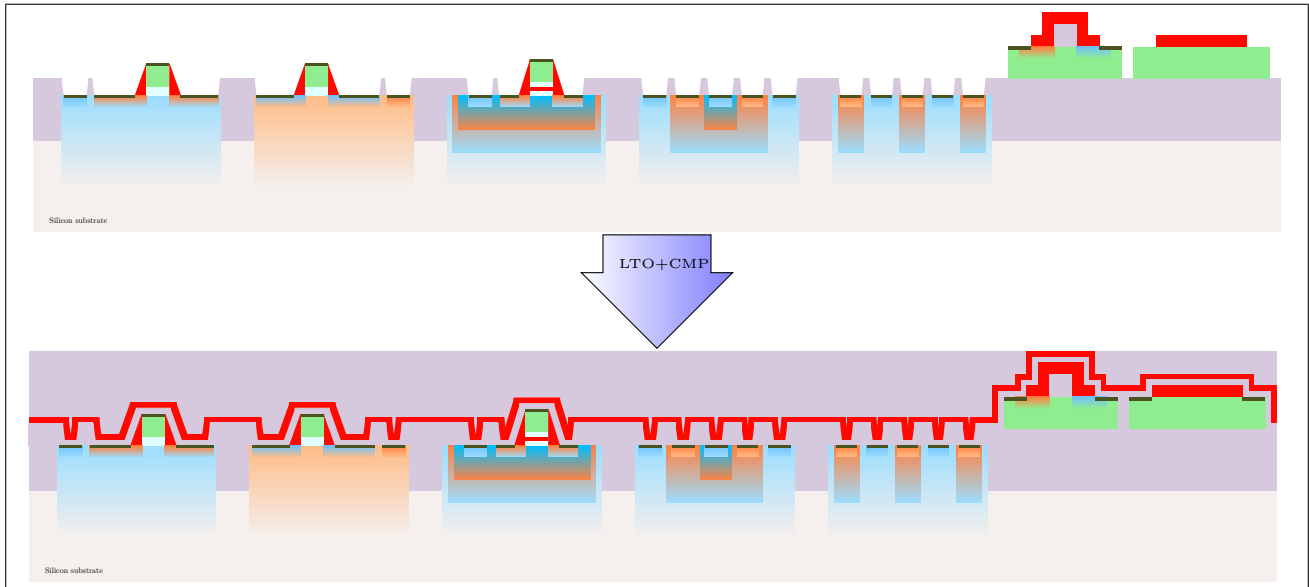

Figure 37: CMP, contact preparation

First we deposit around 100nm LTO as a pad oxide layer below the 100nm nitride, which serves as the CMP stop hard mask. Then we deposit $1\mu m$ LTO and CMP away the height differential of the active devices translated to the oxide.

LTO was chosen because the silicide becomes unstable in the thermal ranges where phosphorus silicate glass becomes viscous enough for evening out the height differential by evening out by seeking its level during annealing.

A thickness of $1\mu m$ of the LTO will make it less likely, that the dishing effect of the CMP pad causes devices to get damaged through an over consumption of the nitride hard mask.

The best approach for depositing this LTO layer is to split the deposition into 4 steps at each 250nm and rotating the sample 90 degrees between the steps in order to improve uniformity of the LTO layer.

9 Interconnect

Now that we've built all the devices, we've got to put wires on them in order to make them do something useful.
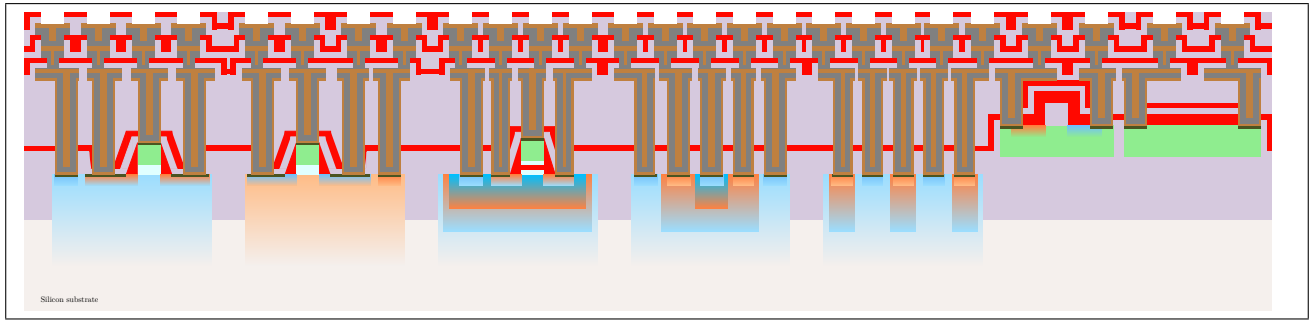

Figure 38: Interconnect geometry target

From here on it's basically just always the same game:

1. Deposit roughly 100nm LTO

2. Deposit 100nm nitride for CMP end stop

3. Deposit roughly $1\mu m$ LTO

4. CMP away 200nm oxide (regulated by CMP end stop)

5. Etch vias

6. Sputter metal

7. Etch wires

8. Go to 1

As can be seen in Figure 38, we have the holes where we sputter the metal into.

All the oxide holes which are subsection 9.1, subsection 9.3, subsection 9.5 and subsection 9.7, are basically the same, except that the glass layer is the top oxide opening and doesn't get any more metal sputtered on it.

An example of the general flow can be seen in subsection 8.6 where it already has been performed for the interface area between back end and front end process.

We deposit $1\mu m$ LTO, CMP it and etch holes into it, in order to contact through to the lower layer.

For the first metal layer (subsection 9.2), the etch stop is silicide and we have to sputter Nickel, as a diffusion barrier, before we sputter any Aluminum, because the $TiSi_2$ would react with the Aluminum to an high resistivity material.

For simplicity reasons Nickel has been chosen as the passivation material on top of the Aluminum as well, because then we have less different sputter sources.

For the other two layers, subsection 9.4 and subsection 9.6, it's only the Aluminum and then the Nickel passivation.

Argon plasma etching with 5% Chlorine gas added, with an output power of 500 Watts or more has been prooven very effective, for etching Nickel and Aluminium alike.

For the oxide hole etching, any oxide etching machine can be used, or one could even use just buffered oxide etchant (BOE).

9.1 Contacts

Now we have to build the first set of vias connecting the first metal layer to the active area. These vias are in the fringe between front-end and back-end process.
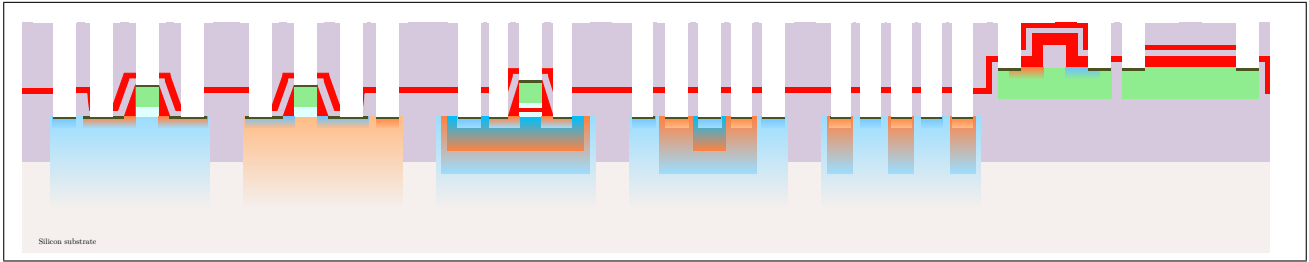

Figure 39: Contact geometry target

In subsection 8.6 we have already prepared the CMPed LTO which gives a well planarized oxide surface to etch through.
As can be seen in Figure 39, the goal of this step is purely get the holes into it, down to the silicide and polyside in order to form wires later on.
We do not wanna etch down anywhere else than the silicide/polycide areas because these function as etch stoppers, while everywhere else we might etch further than desired with small variations in etching time which might result in a drastic variation in sheet resistance of the junctions and gate.

9.2 Metal 1

Now we've got to build the first interconnect wires, connecting the contact vias to the "metal1" wires, which will provide a way to contact to them with the via1 contact layout.
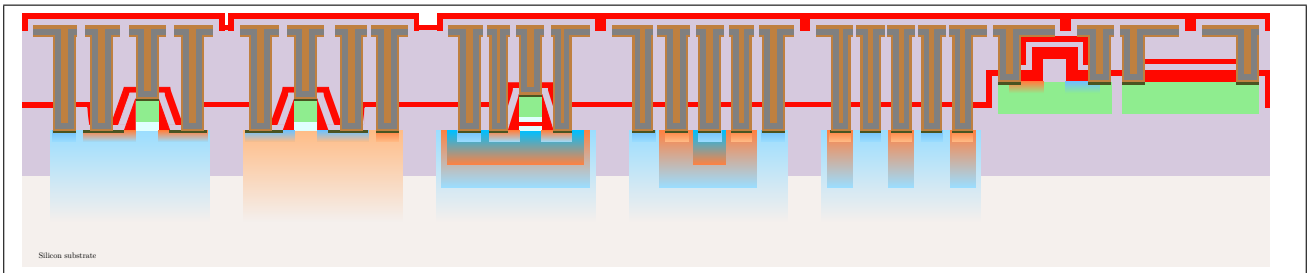

Figure 40: Metal geometry target

In later iterations of this process we might be switching to Tungsten as the metal material for this step so the etching method might change in further releases.
First we sputter around 50nm Nickel, then 100nm Aluminum and at the end again around 50nm Nickel for passivation, all in the same vacuum.

9.3 Via 1

Now we have to build an additional set of vias connecting the first metal layer to the next metal layer. Those vias are already part of the front-end process.
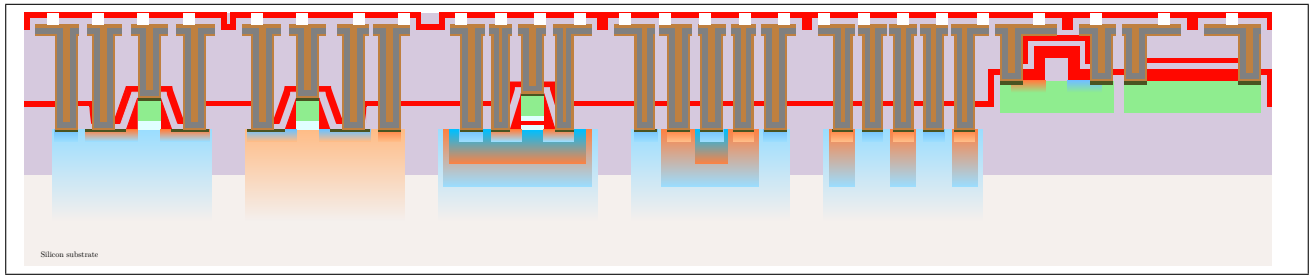

Figure 41: Contact geometry target

As can be seen in Figure 41, the goal of this step is purely to deposit a layer of isolation oxide, get the holes into it, down to the metal1 layer below in order to form wires later on.

9.4 Metal 2

Now we've got to build the more interconnect wires, connecting the "metal1" to the "metal2" wires, which will provide a way to contact to them with the via2 contact layout.
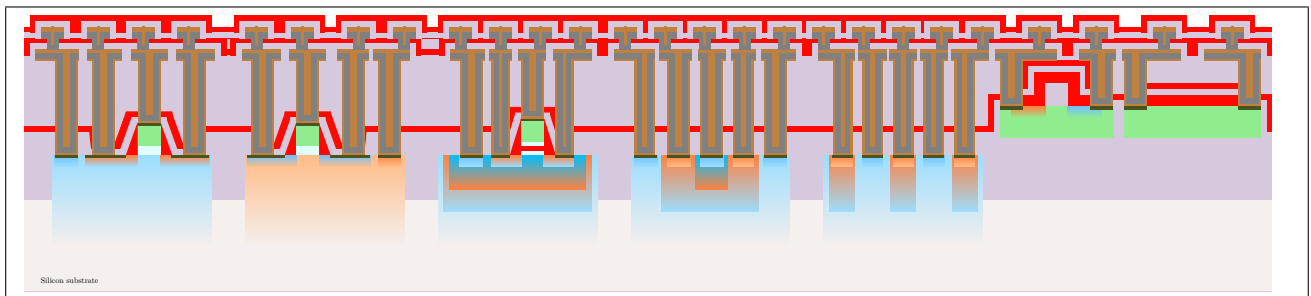

Figure 42: Metal geometry target

As can be seen in Figure 42, the goal of this step is purely to etch the wire structure for the additional metal layer into the in Figure 40 deposited metal layer, and form wires by doing so.

In a later iterations of this process we might be switching to Copper as the metal2 material for this step which will result in a variation of this step because the usage of damascene method.

For now first we sputter 100nm Aluminum and then around 50nm Nickel for passivation, all in the same vacuum.

9.5 Via 2

Now we have to build an additional set of via1. connecting the first metal layer to the next metal layer. These via1. are already part of the front-end process.
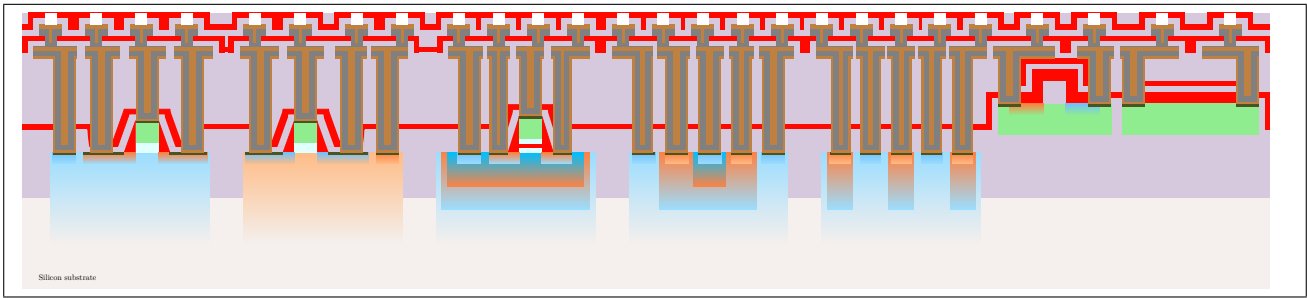

Figure 43: Contact geometry target

As can be seen in Figure 43, the goal of this step is purely to deposit a layer of isolation oxide, get the holes into it, down to the metal layer below in order to form wires later on.

In a later iterations of this process we might be switching to Copper as the metal material for this step which will result in a variation of this step because the usage of damascene method.

9.6 Metal 3

Now we've got to build the more interconnect wires, connecting the "metal2" to the "metal3" wires, which will provide us the contact pads exposed by the glass layer.

This surface will not be covered any further and will be the surface where we touch down with the test probes and bond our wires onto.
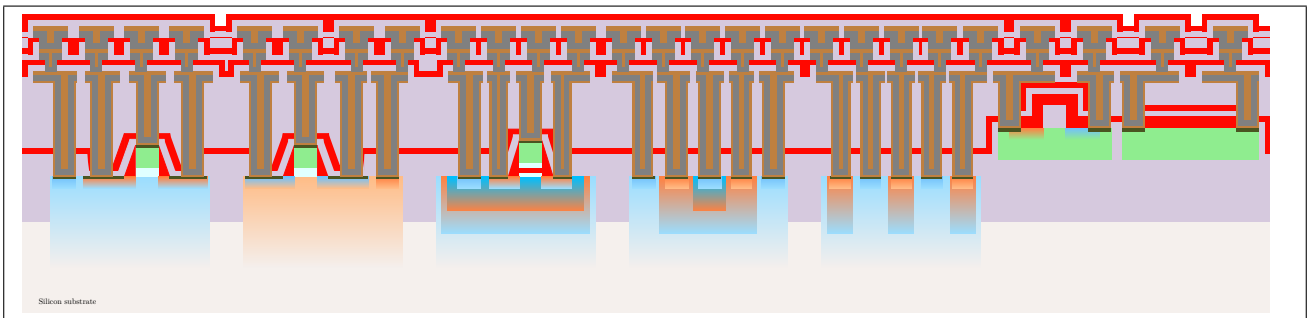

Figure 44: Metal geometry target

As can be seen in Figure 44, the goal of this step is purely to etch the wire structure for the additional metal layer into the in Figure 42 deposited metal layer, and form wires by doing so.

In a later iterations of this process we might be switching to Copper as the metal3 material for this step which will result in a variation of this step because the usage of damascene method.

For now first we sputter 100nm Aluminum and then around 50nm Nickel for passivation, all in the same vacuum.

9.7 Glass

This is the final oxide layer, which serves as a passivation for the metal3 wires and exposes the bonding and test pads to the outside world.
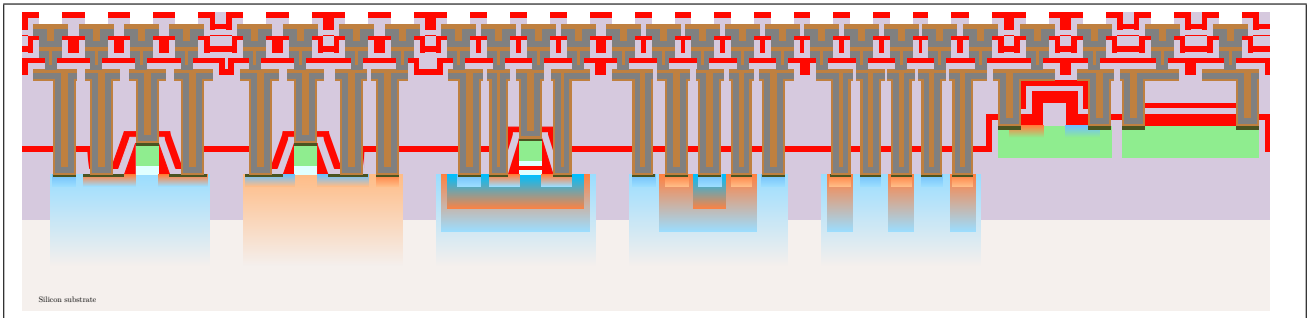

Figure 45: Glass geometry target

As can be seen in Figure 45, the goal of this step is purely to deposit a layer of isolation oxide, get the holes into it, down to the metal layer below in order to form wires later on.

In a later iterations of this process we might be switching to Copper as the metal material for this step which will result in a variation of this step because the usage of damascene method.