SHARP
SERVICE MANUAL

MODEL CE-122

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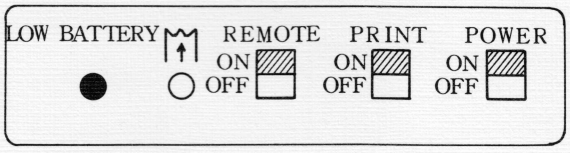
The CE-122 is the option printer designed for PC-1210/1211 and contains the printer interface and cassette interface in addition to printer mechanism.

1. SPECIFICATIONS

1) Switch layout



2) Functions

- Printer function
  Program contents is printed with the LIST command and alphanumeric characters are printed with the PRINT command during program execution.
- Cassette interfacing function
  As the reproduction signal is received from the cassette tape recorder, the cassette interface identifies "0" and "1" of the data and convert it into corresponding phase signal.

3) Power supply

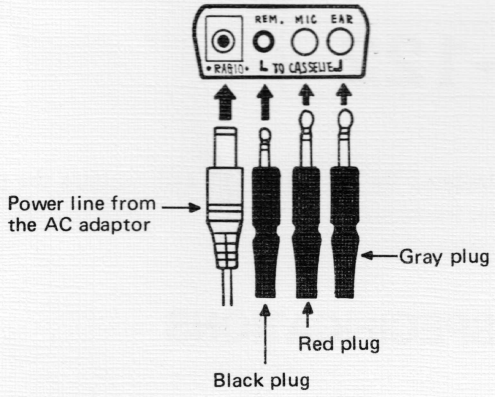
Driven by the Ni-Cd battery power which consists of 4X type AA batteries (UBATZ2064CCZZ), and recharged by the recharger EA11E.

- Battery life: About 8,000 lines
  Recharging time: About 15 hours.
  Low battery indicator: The low battery indicator will start flickering when the voltage from the Ni-Cd battery drops below the level the printer action is impeded. (Note that the printer won't start operation when the Ni-Cd battery is in low level, even though the power is turned on after connecting the AC adaptor.)
  Power consumption: 4.8V, 1.84W

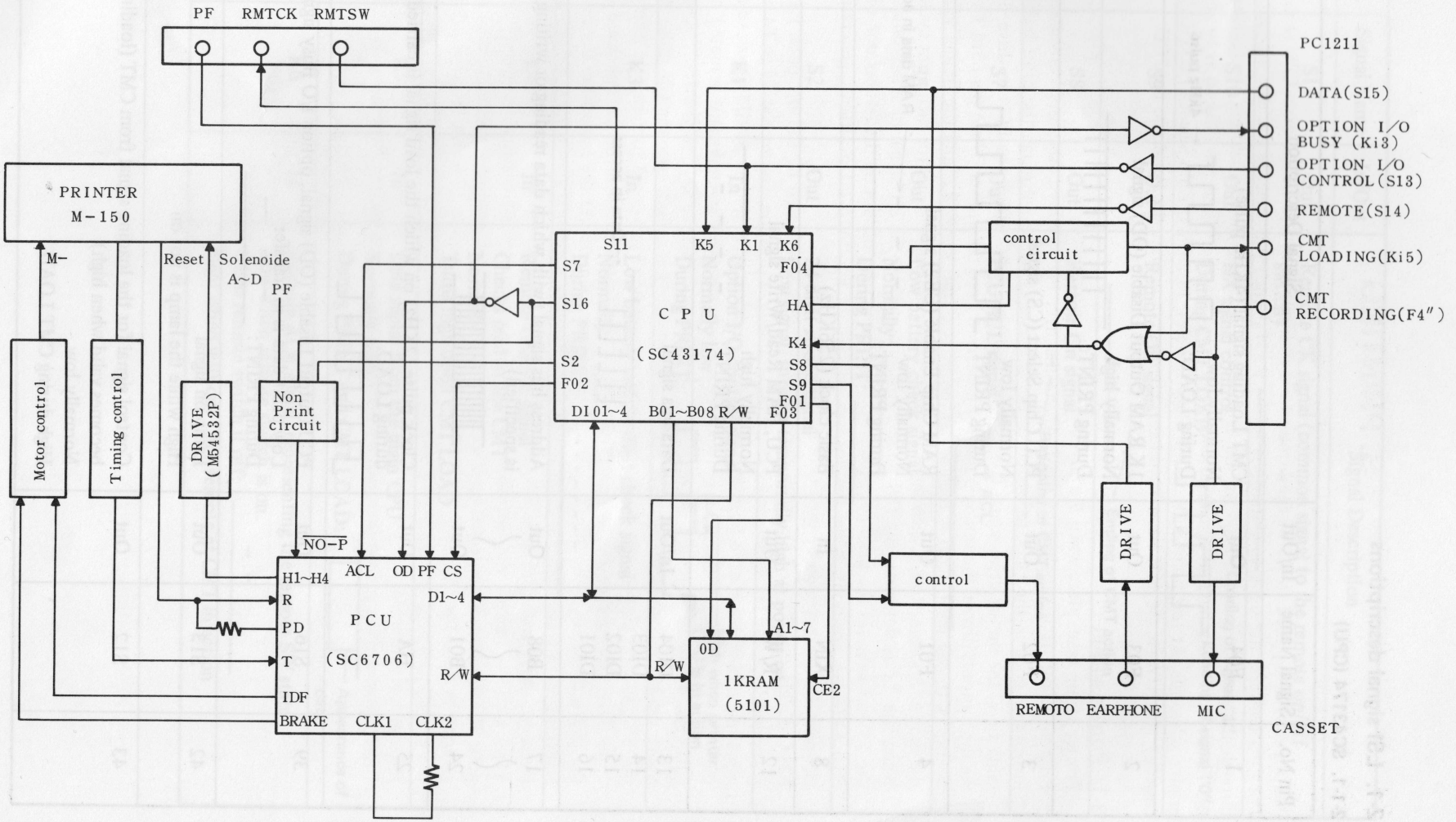
4) Printer

Printer	M-150 dot printer (KI-OB0054CCZZ)
Print positions:	16 digits
Dot structure:	5 x 7 dot matrix
Print speed:	About 1 line/second
Recording paper:	45mm(W) x 25mm(OD), max. ordinary paper
Ink ribbon:	Cartridge ribbon (EA-800R)
Ribbon life:	About 10,000 lines

5) Connector

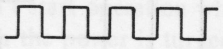
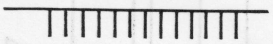
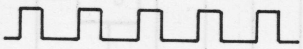
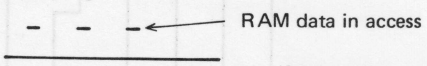
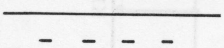
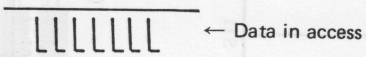
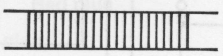
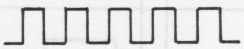


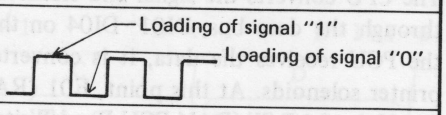
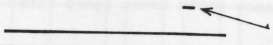
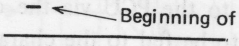
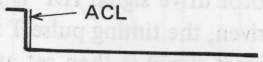
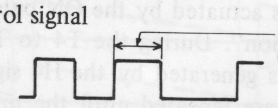
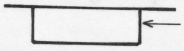
2. BLOCK DIAGRAM



2-1. LSI signal descriptions

2-1-1. SC43174 (CPU)

Pin No.	Signal Name	In/Out	Signal Description
1	F04	Out	CMT Loading signal (4KHz pulse) Normally low During LOAD:  ← 4kHz pulse
2	F03	Out	1K RAM Output Disable (OD) signal Normally high During PRINT: 
3	F02	Out	PCU Chip Select (CS) signal Normally low During PRINT: 
4	F01	Out	RAM Chip Enable (CE2) signal Normally low During PRINT:  RAM data in access
8	XIN	In	Basic clock (256KHz)
12	R/W	Out	PCU, RAM Read/Write signal Normally high During PRINT: 
13 14 15 16	DI04 DI03 DI02 DI01	In/Out	Data bus signal  ← Data in access
17 〉 〈 24	B08 〉 〈 B01	Out 〉 〈 Out	Address bus signal (with which data reading or writing address is specified) 
25	HA	Out	Clock pulse (2KHz) on which the load signal is carried on during LOAD. 
39	S16	Out	PCU Output Disable (OD) signal, option I/O Busy signal Low print data is in transfer During PRINT:
42	S13	Out	Lamp on signal High while the lamp is not on
43	S12	Out	Control signal for the loading signal from CMT (loading signal) becomes valid when high) Normally low High during CMT LOAD

Pin No.	Signal Name	In/Out	Signal Description
44	S11	Out	Remote CK signal (common signal to the remote on/off switch)
45	S10	Out	HA signal control During CMT LOAD: 
46	S9	Out	Remote Off signal 
47	S8	Out	Remote On signal 
48	S7	Out	PCU ACL signal 
49	S6	Out	Low battery check signal Normally: During PRINT:
53	S2	Out	24-digit strobe signal Low signal, turning temporarily high at power on.
55	K1	In	Option I/O control signal Normally low During PRINT: 
56	K3	In	Low battery and 24-digit check signal Normally: During PRINT:
57	K4	In	Remote CSAVE signal Checks read in the CMT Normally low Turns high upon CMT LOAD
58	K5	In	Data signal from the main CPU Normally high During PRINT and CMT LOAD: 
59	K6	In	Remote ACK signal, representing the remote SW state Low when remote switch is on. When remote switch if off: High when without CMT remote at CMT in action

3. PRINTING

Printing data is supplied to K5 of the printer CPU (P-CPU) from S15 of the main CPU as data signal. The CPU converts the signal and transfers to the RAM (which functions as the data accessing buffer) through the data bus, DI01~DI04 on the basis of the address shown by address bus (B01~B08). As the PCU receives the data, it is converted into H1~H4 via the CG in the PCU so as to actuate the printer solenoids. At this point, F01 (RAM Chip Enable), F02 (PCU Chip Select), F03 (RAM Output Disable), and R/W (RAM PCU Read/Write) are generated to operate the RAM and the PCU.

3-1. Printer action

Printer action takes place when the OD of the PCU is in high level.

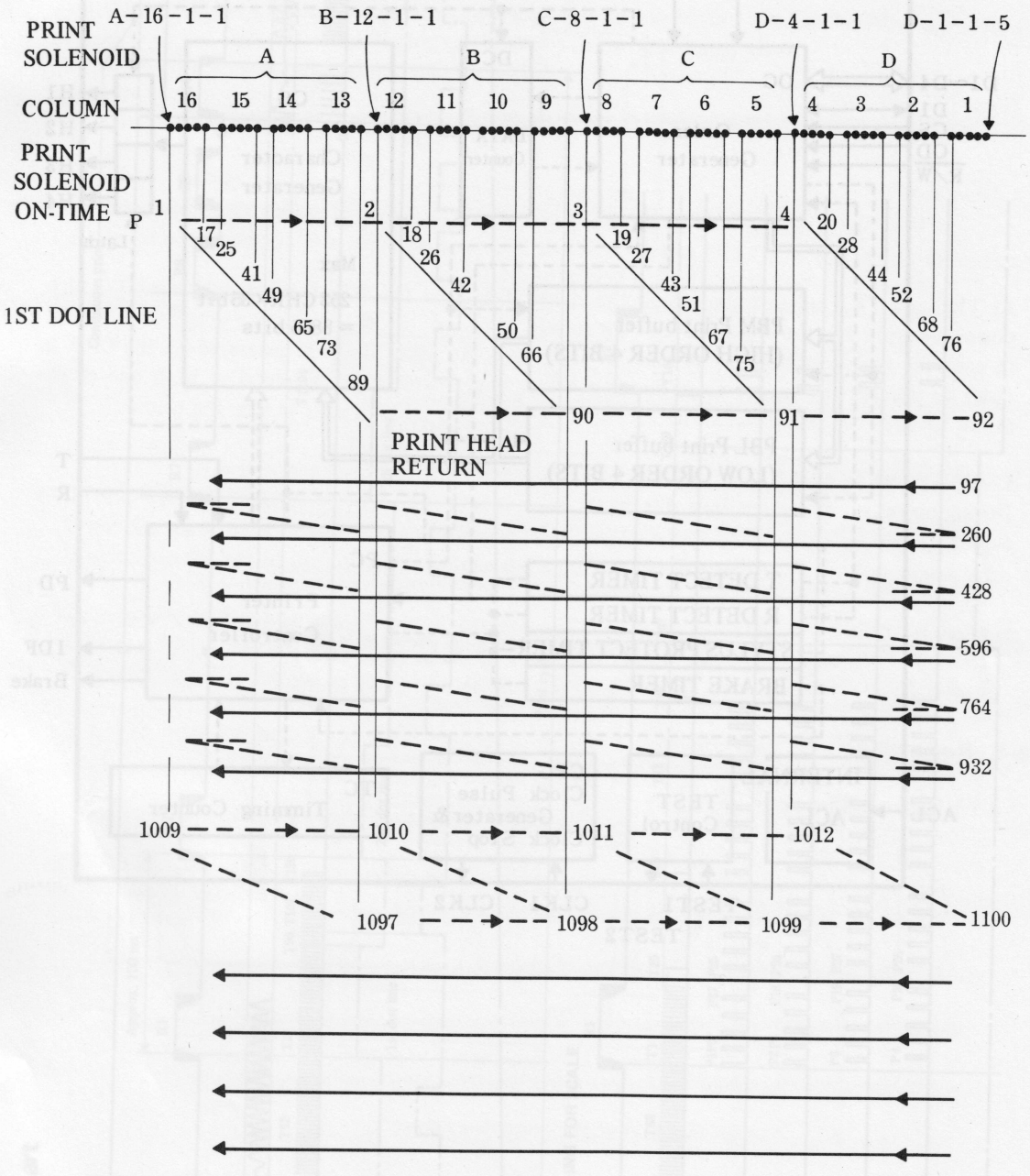
Printout contents is supplied to the PCU via the data bus (DI01~DI04) and converted into the instruction code in the PCU, to be fed to the character generator through the print buffer. At the same time, the motor drive signal IDF is generated by the PC within the PCU to drive the motor. As the motor is driven, the timing pulse T is generated from the printer. When the 63rd T is counted by the PCU, the reset signal is then set as the printer start signal R1, and the timing signal T1, at the time of R1 detection, is then set as the dot position reference signal for each print cycle.

When the T1 is detected, the ON pulse P1 is generated by the H1 signal in synchronization with the T1 and actuates the print solenoid A to print the uppermost dot on the left column of the 16th digit (A16-1-1 position). When the dot was omitted on the "A16-1-1 position", generation of the ON pulse P1 is suppressed by the CG in the CPU.

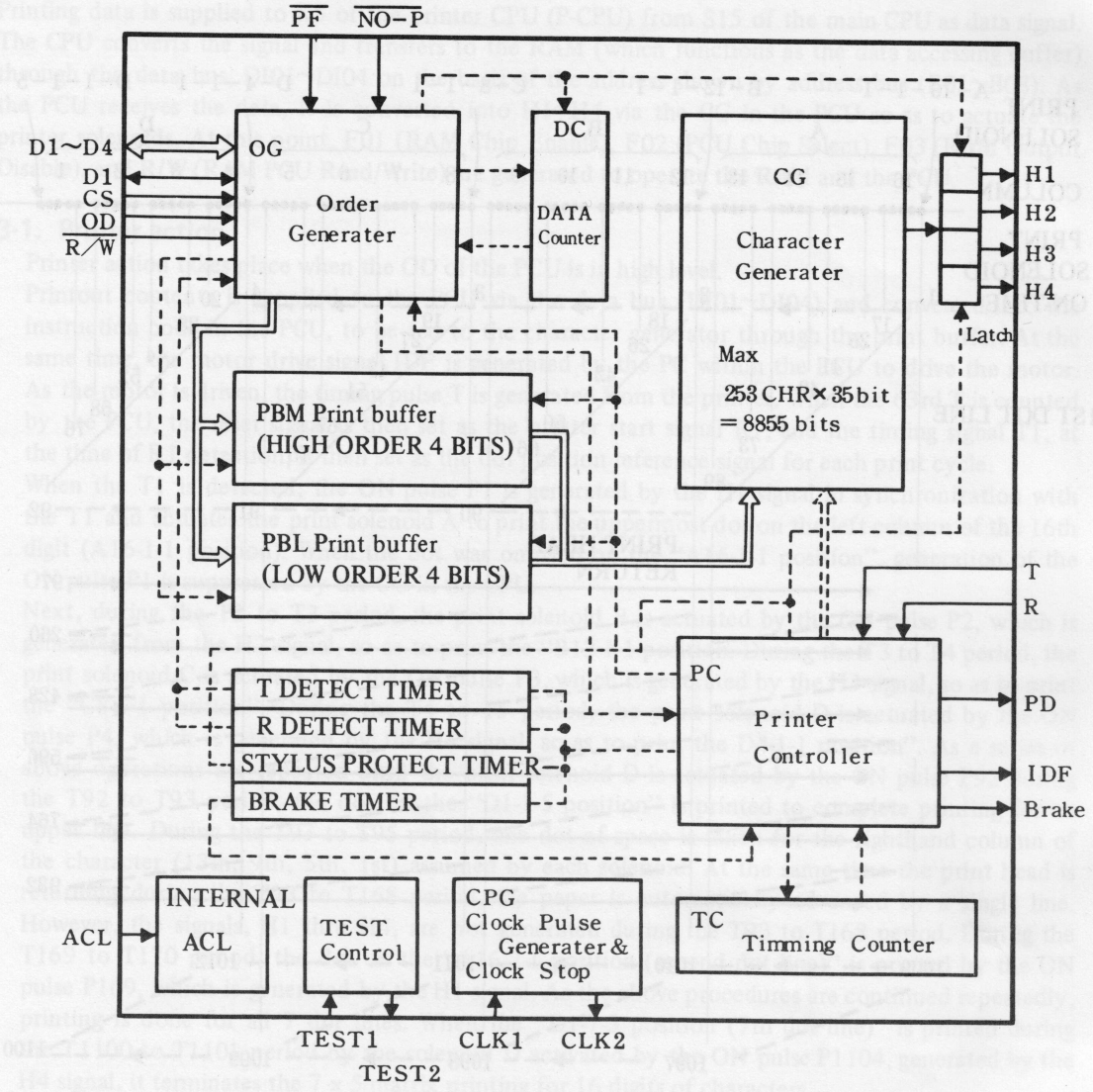
Next, during the T2 to T3 period, the print solenoid B is actuated by the ON pulse P2, which is generated from the H2 signal, so as to print the "B12-1-1 position. During the T3 to T4 period, the print solenoid C is actuated by the ON pulse P3, which is generated by the H3 signal, so as to print the "C8-1-1 position". During the T4 to T5 period, the print solenoid D is actuated by the ON pulse P4, which is generated by the H4 signal, so as to print the D4-1-1 position". As a series of above operations are repeated until the print solenoid D is actuated by the ON pulse P92 during the T92 to T93 period, the dot on the "D1-1-5 position" is printed to complete printing for an upper line. During the T93 to T95 period, one dot of space is taken for the righthand column of the character (13th, 9th, 5th, 1st) assumed by each solenoid. At the same time the print head is returning during the T93 to T168 period, the paper is automatically advanced by a single line. However, the signals, H1 thru H4, are not generated during the T93 to T168 period. During the T169 to T170 period, the dot on the "A16-2-1 position (second dot line)" is printed by the ON pulse P169, which is generated by the H1 signal. As the above procedures are continued repeatedly, printing is done for all 7 dot lines. When the "D1-7-5 position (7th dot line)" is printed during the T1100 to T1101 period by the solenoid D activated by the ON pulse P1104, generated by the H4 signal, it terminates the 7 x 5 matrix printing for 16 digits of characters.

Finally, line spacing is done for 3 dot spaces and terminates a complete printing cycle.

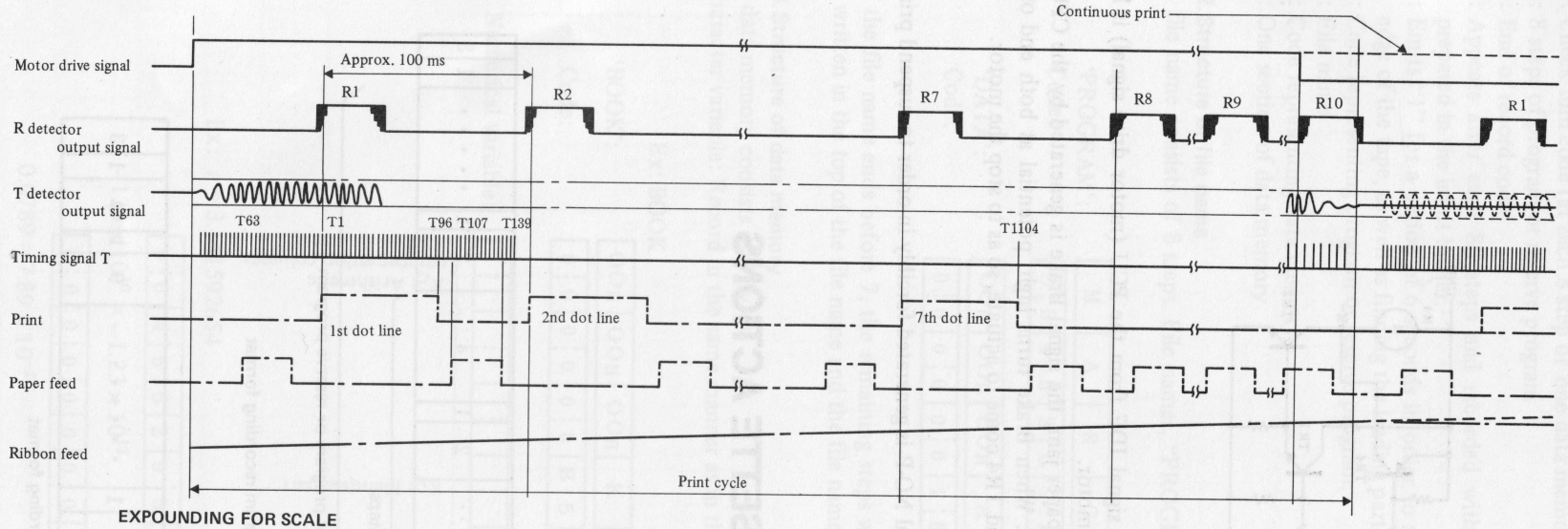
DETAIL OF PULSE DISTRIBUTION (IN THE CASE OF 5 x 7 DOT MATRIX, 3 DOT SPACINGS FOR THE LINE SPACE



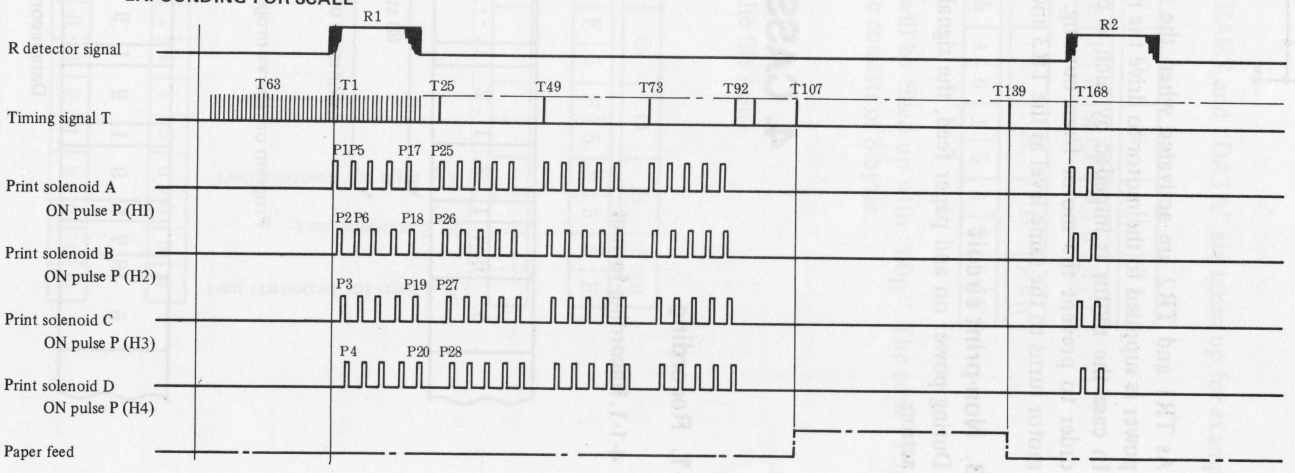
• PCU BLOCK DIAGRAM



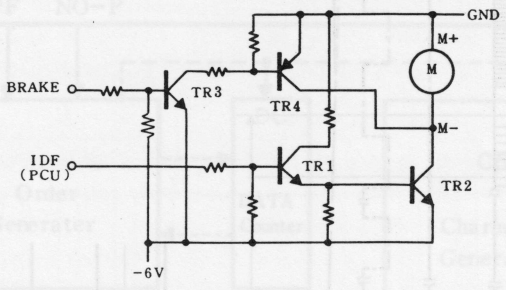
• Print Time Chart



EXPOUNDING FOR SCALE



3-2. Motor drive circuit



As TR1 and TR2 are activated when the signal IDF from the PCU (motor drive signal) is high, power is supplied to the motor to drive the motor.
In case the motor is impeded by such as paper jam, the signal Brake is generated by the CPU, in order to prevent the motor from burning. When Brake turns high, potential at both end of the motor turns to the same level as the TR3 and TR4 come to actuate, so as to stop the motor.

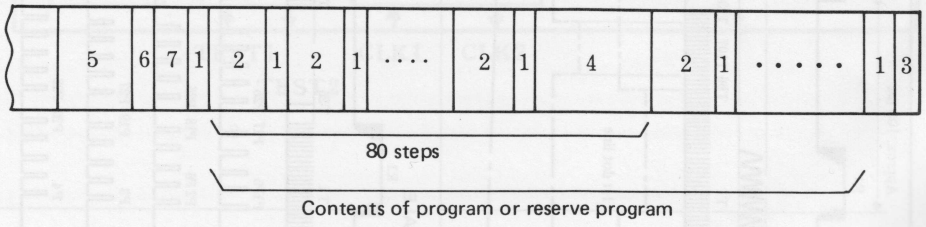
3-3. Non-print circuit

During power on and paper feed, the signal NO-P is generated forcibly in order to suspend printing action.

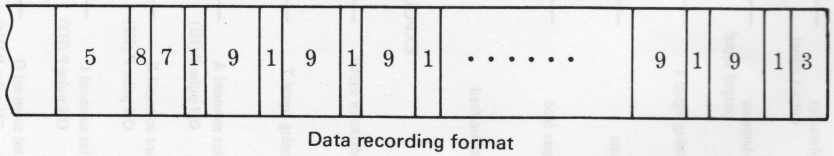
4. CASSETTE ACTIONS

4-1. Recording

4-1-1. Recording format



Program or reserve program recording format



Data recording format

1: Check-sum code (at each 8 step or one data memory)
2: 8 steps of program or reserve program
3: End of record code
4: Appears after each 80 steps and recorded with "1". And next 80 steps to be recorded are prepared in the input buffer.
5: Emits "1" for a period of 6 seconds in order to avoid recording disabled portion at the leading edge of the tape, as well as finding the leading part of recording.
6: Code representing program or reserve program.
7: File name
8: Code representing data memory.
9: One section of data memory

4-1-2. Structure of file name

A file name consists of 8 steps. File names, "PROGRAM" and "DATA" are taken up for example.

'PROGRAM':

M	A	R	G	O	R	P	F5H

Code:

D	5	1	5	2	6	7	5	F	5	2	6	0	6	5	F

'DATA':

00H	00H	00H	A	T	A	D	F5H

Code:

0	0	0	0	0	0	1	5	4	6	1	5	4	5	5	F

If the file name ends before 7, the remaining steps will be filled up with "00_H". The code "$F5_H$" is written in the top of the file name and the file name consists of 8 bytes.

4-1-3. Structure of data memory

A data memory consists of 8 bytes.

Character variable: Record in the same manner as in the file name.

Ex: BOOK

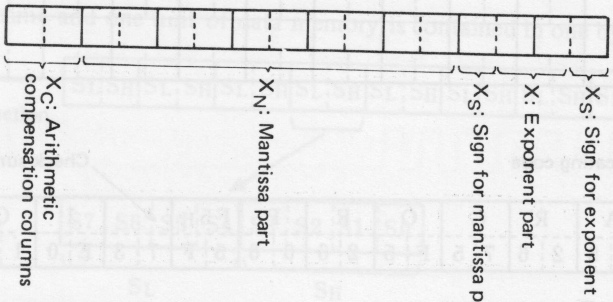
'BOOK':

00H	00H	00H	K	O	O	B	F5H

Code:

0	0	0	0	0	0	B	5	F	5	F	5	2	5	5	F

Numerical variable:



Ex: $\pi = 3.141592654$

0	0	4	5	6	2	9	5	1	4	1	3	0	0	0	0

$-123 \times 10^{10} = -1.23 \times 10^{12}$

0	0	0	0	0	0	0	0	0	3	2	1	8	2	1	0

$0.0789 = 7.89 \times 10^{-2}$

0	0	0	0	0	0	0	0	0	0	9	8	7	8	9	9

Effective digits for numeric is 10 digits (shown by X_N). One unit of numerical variable consists of X_C, X_N, X_S, X, and X_S. (See figure above.)
Sign for the numeric value is represented by X_S; "0" is stored for a plus sign and "8" for a minus sign. Exponent of numerical value is stored in X and its sign is represented by X_S. Two digits are reserved for X. Numerical value is stored in a form of exponential. When the absolute value of the numeric is smaller than 1, number deduced by 100 is stored in X_S and X.

4-1-4. Recording of program

Program line number requires two steps of program memory.

Ex: Line number 1:

E	0	0	1

Line number 12:

E	0	1	2

Line number 123:

E	1	2	3

As shown in above, the first bit in the leading one byte is "E" all the time.
For an example, when the program described below is stored into the computer, it will be stored in the program memory as illustrated further below.

```
10 INPUT A,B
20 C=√(A*A+B*B)
30 PRINT C
40 END
```

1	0	INPUT	A	,	B	ENTER	2	O	C	=	√	(	A	*	A
E 0	1 0	C 2	5 1	1 B	5 2	0 0	E 0	2 0	5 3	3 4	1 A	3 0	5 1	3 7	5 1
+	B	*	B	)	ENTER	3	0	PRINT	C	ENTER	4	0	END	ENTER	
3 5	5 2	3 7	5 2	3 1	0 0	E 0	3 0	C 1	5 3	0 0	E 0	4 0	D 4	0 0	

Program indicating code

Check-sum code

	M	A	R	G	O	R	P	F5H		1	O	INPUT	A	,	B
8 0	D 5	1 5	2 6	7 5	F 5	2 6	0 6	5 F	7 3	E 0	1 0	C 2	5 1	1 B	5 2

Check-sum code

Check sum code

ENTER	2		O	C	=	√	(	A	*	A		+	B	*	B
0 0	E 0	4 7	2 0	5 3	3 4	1 A	3 0	5 1	3 7	5 1	7 C	3 5	5 2	3 7	5 2

When this program is recoded by "CSAVE 'PROGRAM'", it will be recorded in the following sequence. The file name is recorded in the reverse sequence and the recording sequence of one byte in the file name is done from the lower 4 bit. And, differs from the program indicating code, program step or check sum code.

4-1-5. Reserve program

For instance, when "RUN" is memories in the 2 key and "SIN A" in the A key, the contents of the reserve program will be as follows:

SHIFT A		RUN		SHIFT A		SIN		A					
F	A	B	0	E	1	A	0	5	1				

Such a reservecode like "SHIFT Z" and "SHIFT A" shares one byte of area.

4-1-6. File name and data name recording

Shown in the following is the recording direction of a file name and data memory.

File name 'PROGRAM' ←

M		A		R		G		O		R		P		F5H	
D	5	1	5	2	6	7	5	F	5	2	6	0	6	5	F

Character variable 'BOOK' ←

OOH		OOH		OOH		K		O		O		B		F5H	
0	0	0	0	0	0	B	5	F	5	F	5	2	5	5	F

Numerical variable '3.141592654' ←

OO		4 5		6 2		9 5		1 4		1 3		O O		O O	
0	0	4	5	6	2	9	5	1	4	1	3	0	0	0	0

4-1-7. Recording of one byte

Program, reserve program, and check-sum code, and the code representing the program or reserve program, the code $8F_H$ representing the data memory, and the end of record code $F0_H$ is contained in one byte shown below.

S : | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |

S_H S_L

Upper four bits Lower four bits

On the other hand, file name and one unit of data memory is contained in one byte shown below.

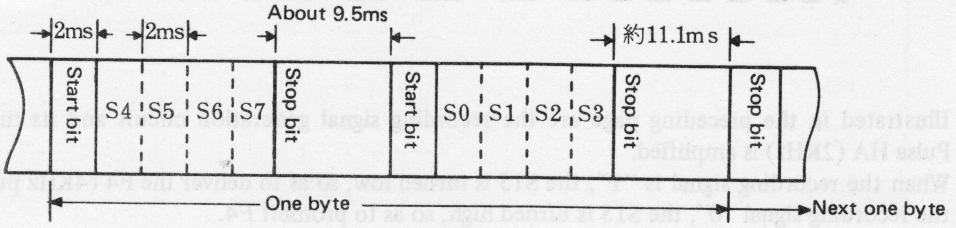
Recorded direction ←

SL	SH	SL	SH	SL	SH	SL	SH	SL	SH	SL	SH	SL	SH	SL	SH

S : | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |

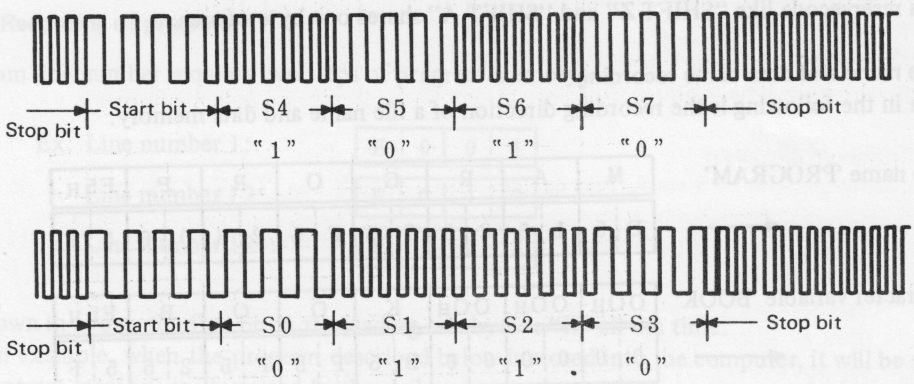
S_L S_H

And one byte of information S is recorded in the following format.

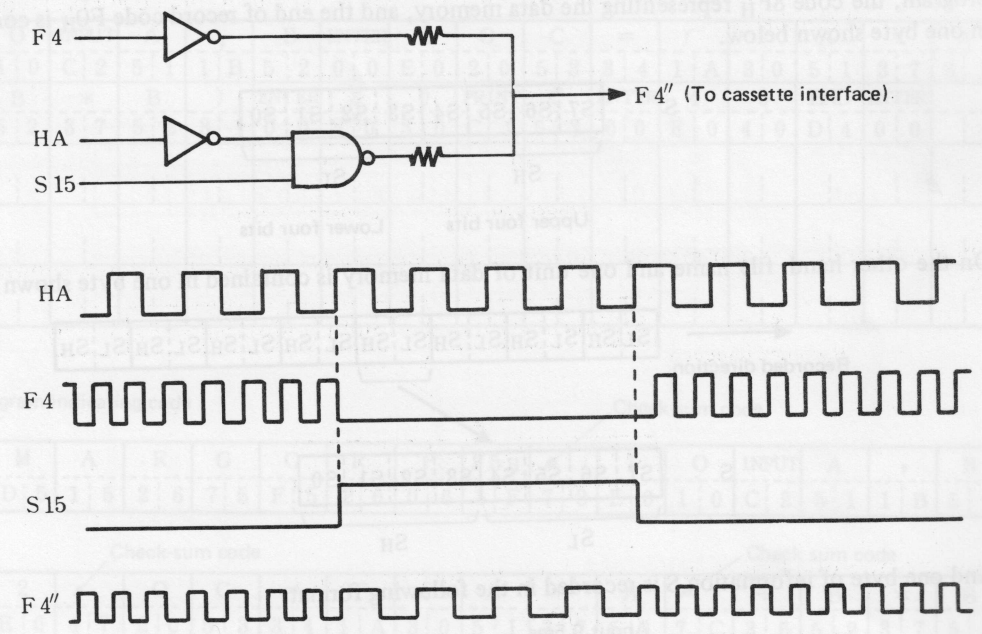


4-1-8. Recording signal

When the contents of the start bit and data are "0", four 2KHz pulses are recorded within 2msec.
When the data bit is "1", eight 4KHz pulses are recorded within 2msec.
Shown below is an example when the contents of S (1 byte) is "01010110".



4-1-9. Recording signal generation circuit

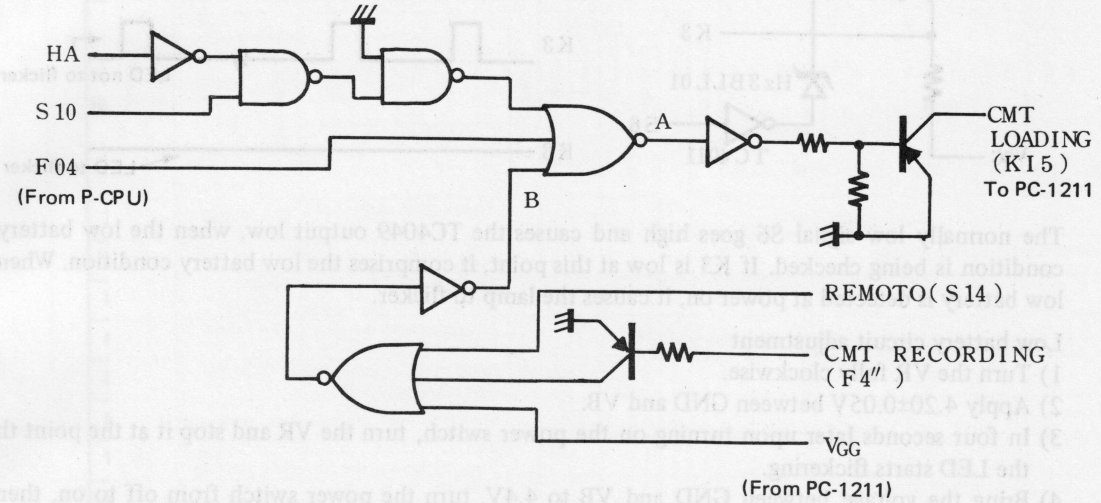


Illustrated in the preceding page are the recording signal generation circuit and its timing chart.
Pulse HA (2KHz) is amplified.
When the recording signal is "1", the S15 is turned low, so as to deliver the F4 (4KHz pulse). When the recording signal "0", the S15 is turned high, so as to prohibit F4.

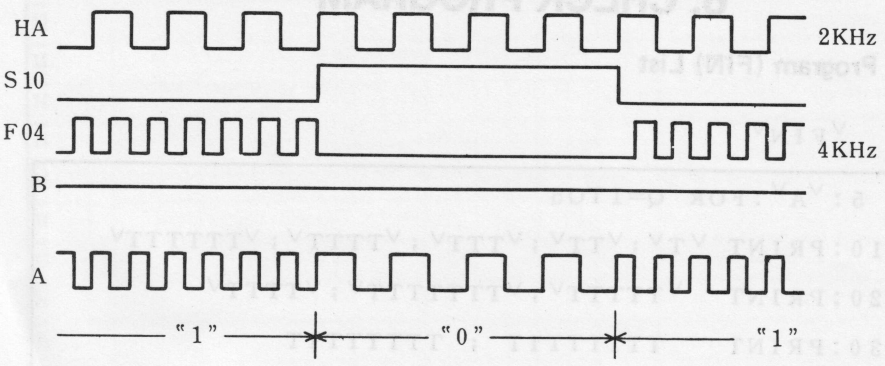
4-2. Loading

On the contrary, loading is done by supplying cassette output to K5 of P-CPU via the amplifier, and this signal is converted into loading signal by the P-CPU.

4-2-1. Loading signal (Ki5) generation circuit

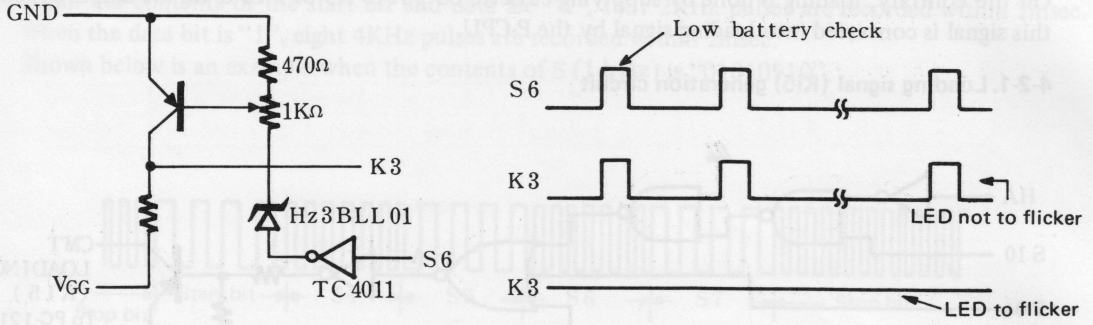


When loading is done:



Same as in recording, the signal S10 is turned low for the bit "1", so as to output F04 (4KHz). For the bit "0", the signal S10 is turned high, so as to output HA (2KHz). The point B, however, is low during loading. In otherwise condition, the point B is turned high so as to prohibit output completely off.

5. LOW BATTERY DETECT CIRCUIT



The normally low signal S6 goes high and causes the TC4049 output low, when the low battery condition is being checked. If K3 is low at this point, it comprises the low battery condition. When low battery is detected at power on, it causes the lamp to flicker.

Low battery circuit adjustment

1) Turn the VR fully clockwise.
2) Apply 4.20±0.05V between GND and VB.
3) In four seconds later upon turning on the power switch, turn the VR and stop it at the point th the LED starts flickering.
4) Bring the voltage between GND and VB to 4.4V, turn the power switch from off to on, then make sure that the LED does not flicker.

6. CHECK PROGRAM

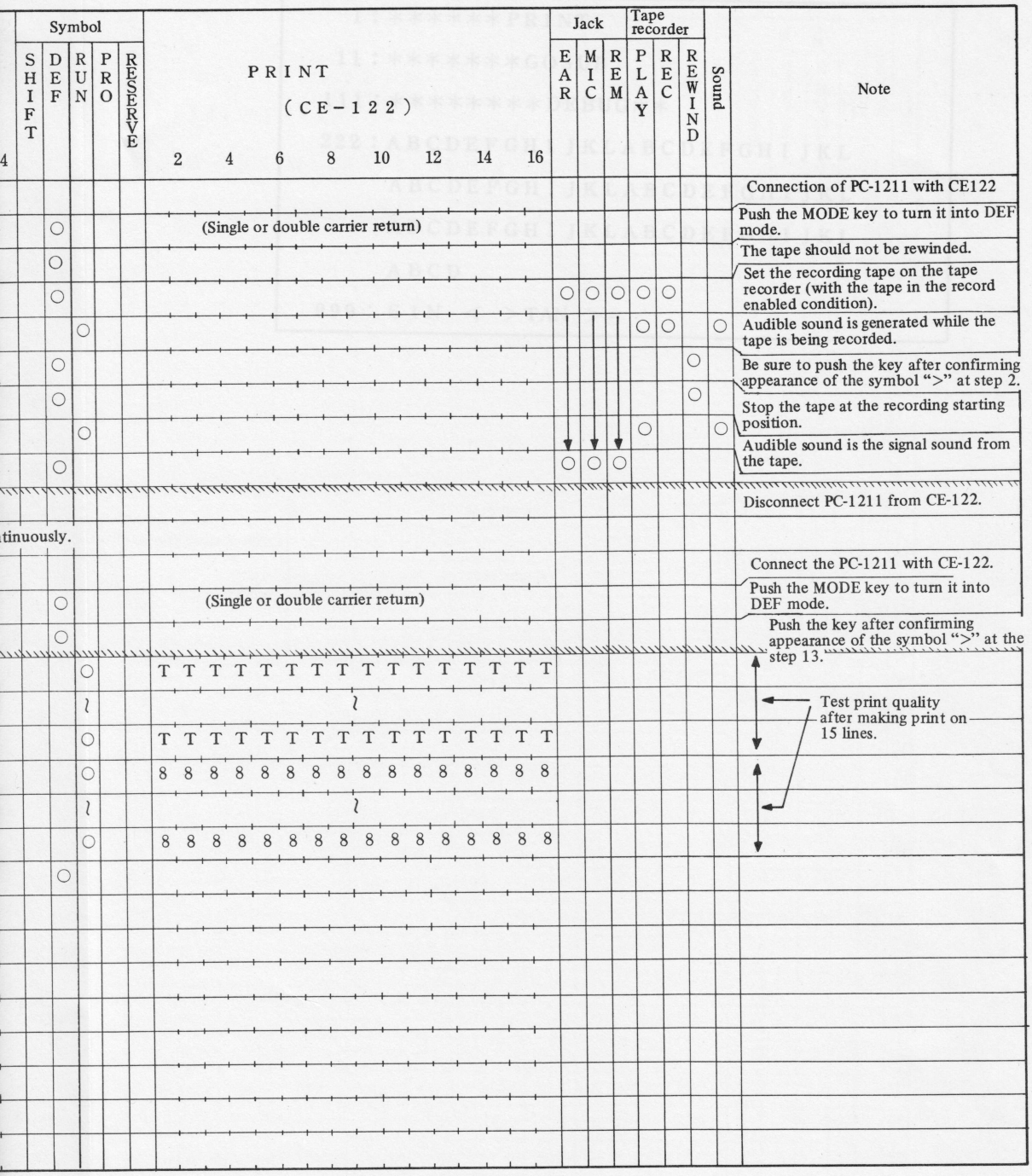
6-1. Check Program (FIN) List

```
^FIN^

  5:^A^:FOR Q=1TO5
 10:PRINT ^T^;^TT^;^TTT^;^TTTT^;^TTTTTT^
 20:PRINT  ^TTTTT^;^TTTTTTT^;^TTTT^
 30:PRINT   TTTTTTTT ; TTTTTTTT
 40:NEXT Q
 50:FOR W=1TO 5
 60:PRINT  ^888888^;^8888^;^888^;^88^;^8^
 70:PRINT  ^88888888^;^88888888^
 80:PRINT  ^88888^;^888888^;^88888^
 90:NEXT  W:END
100:^B^:A(160)=100,A(161)=11
110:PRINT #^DATARAM^;A(160):END
120:^C^:INPUT #^DATARAM^;X
130:Z=X+Y:IF Z=111END
140:PAUSE  ^ERROR!^:GOTO 140
```

6-2. FIN List Operation

No.	Switching	SW	SW REMOTE	SW PRINT	SW POWER	READ IN	DISPLAY (PC-1210 or 1211) 2 4 6 8 10 12 14 16 18 20 22 24	Symbol SHIFT	Symbol DEF	Symbol RUN
1			OFF	OFF	OFF		(Lamp, out)			
2			ON	ON	ON	ON	>		○	
3						ON	>		○	
4							>		○	
5						SHIFT B	(Lamp out)			○
6							>		○	
7			OFF				>		○	
8			ON			SHIFT C	(Lamp out)			○
9							>		○	
10					OFF	OFF	(Lamp out)			
11							Omitted when the check is carried out continuously.			
12							(Lamp out)			
13				ON	ON	ON	>		○	
14						ON	>		○	
15						SHIFT A	(Lamp out)			○
16										≀
17										○
18										○
19										≀
20										○
21							>		○	
22			OFF	OFF	OFF	OFF				
23										
24										
25										
26										
27										
28										
29										


Symbol
SHIFT
DEF
RUN
PRO
RESERVE
PRINT
(CE-122)
2 4 6 8 10 12 14 16
Jack
EAR
MIC
REM
Tape recorder
PLAY
REC
REWIND
Sound
Note
Connection of PC-1211 with CE122
Push the MODE key to turn it into DEF mode.
(Single or double carrier return)
The tape should not be rewinded.
Set the recording tape on the tape recorder (with the tape in the record enabled condition).
Audible sound is generated while the tape is being recorded.
Be sure to push the key after confirming appearance of the symbol ">" at step 2.
Stop the tape at the recording starting position.
Audible sound is the signal sound from the tape.
Disconnect PC-1211 from CE-122.
tinuously.
Connect the PC-1211 with CE-122.
Push the MODE key to turn it into DEF mode.
(Single or double carrier return)
Push the key after confirming appearance of the symbol ">" at the step 13.
T T T T T T T T T T T T T T T T
T T T T T T T T T T T T T T T T
8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8
8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8
Test print quality after making print on 15 lines.

6-3. Check Program (LST) List

```
vLSTv
```

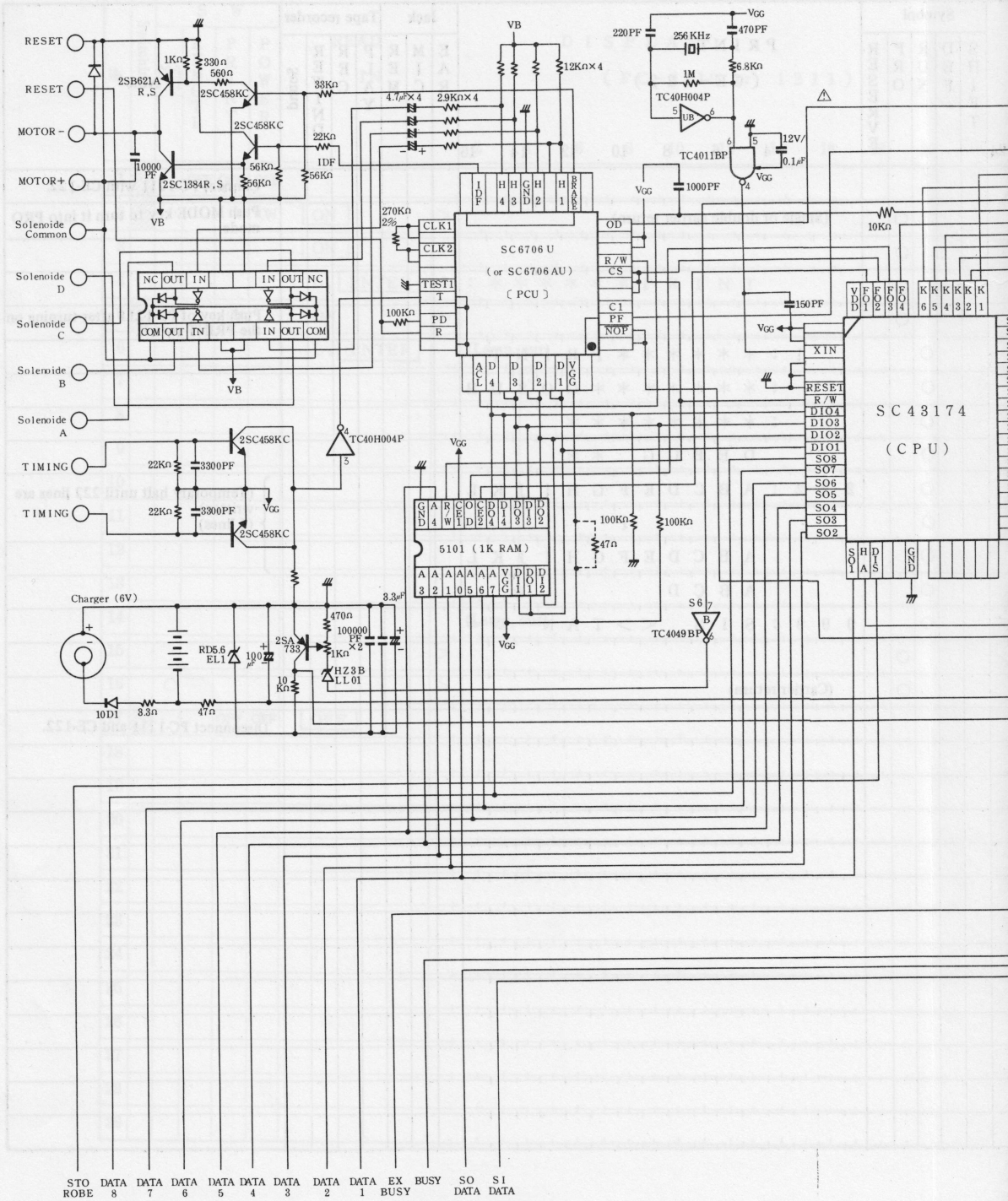
```
  1 : ******PRINT
 11 : *******GOSUB
111 : ********DEBUG**
222 : ABCDEFGHIJKLABCDEFGHIJKL
      ABCDEFGHIJKLABCDEFGHIJKL
      ABCDEFGHIJKLABCDEFGHIJKL
      ABCD
999 : SIN < >TAN >=
```

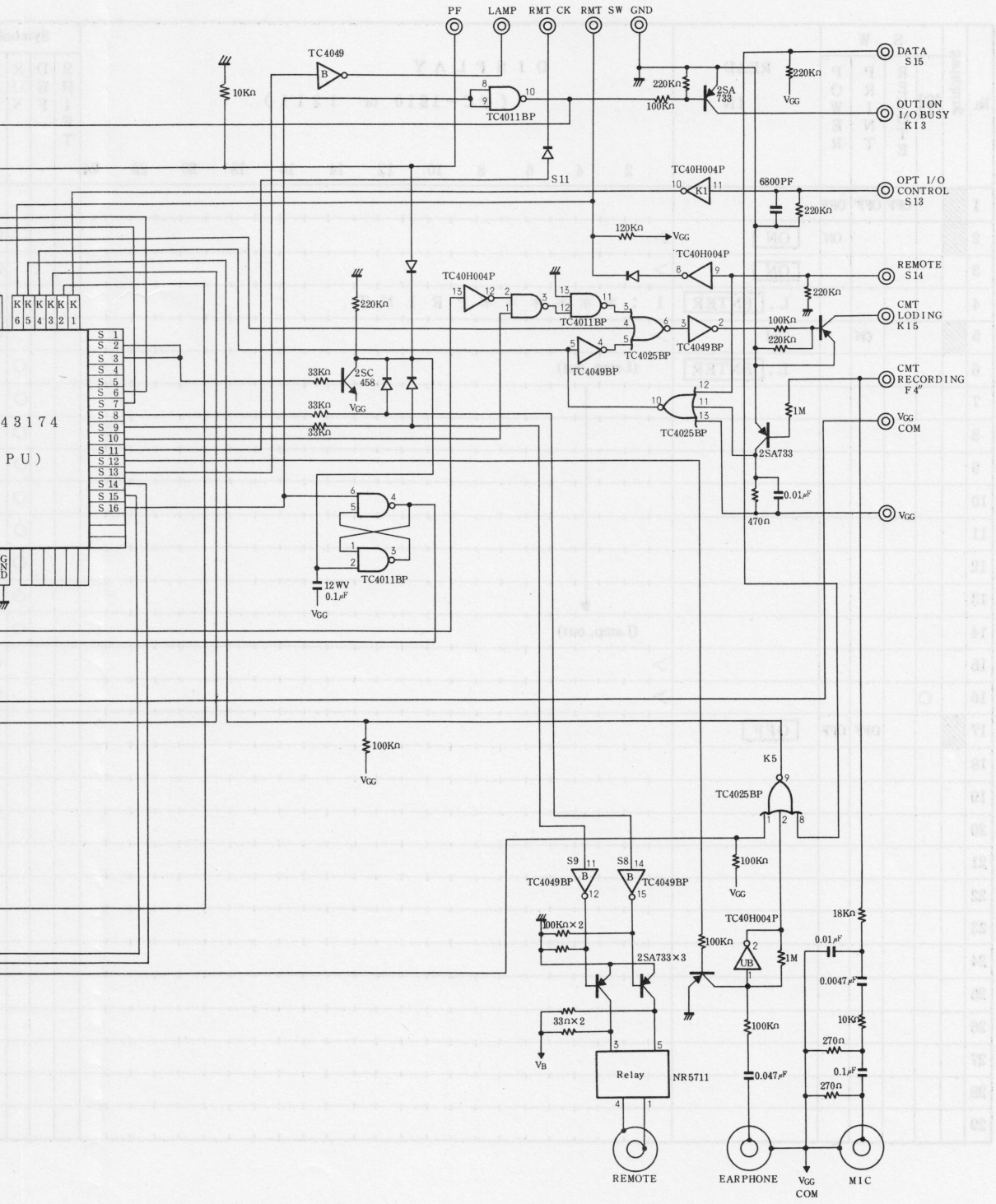
6-4. LST List Operation

No.	Switching	S W			READ IN	DISPLAY (PC-1210 or 1211)	Symbol		
		REMOTE	PRINT	POWER		2 4 6 8 10 12 14 16 18 20 22 24	SHIFT	DEF	RUN
1	▨	OFF	OFF	OFF					
2	▨			ON	[ON]	>			○
3					[ON]	>			○
4					L. [ENTER]	1 : ＊＊＊＊＊＊PRINT			○
5	▨		ON		ON	>			○
6					L. [ENTER]	(Lamp, out)		○	
7								○	
8								○	
9								○	
10								○	
11								○	
12								○	
13								○	
14						(Lamp, out)		○	
15						>			○
16		○				>			○
17	▨		OFF	OFF	[OFF]				
18									
19									
20									
21									
22									
23									
24									
25									
26									
27									
28									
29									

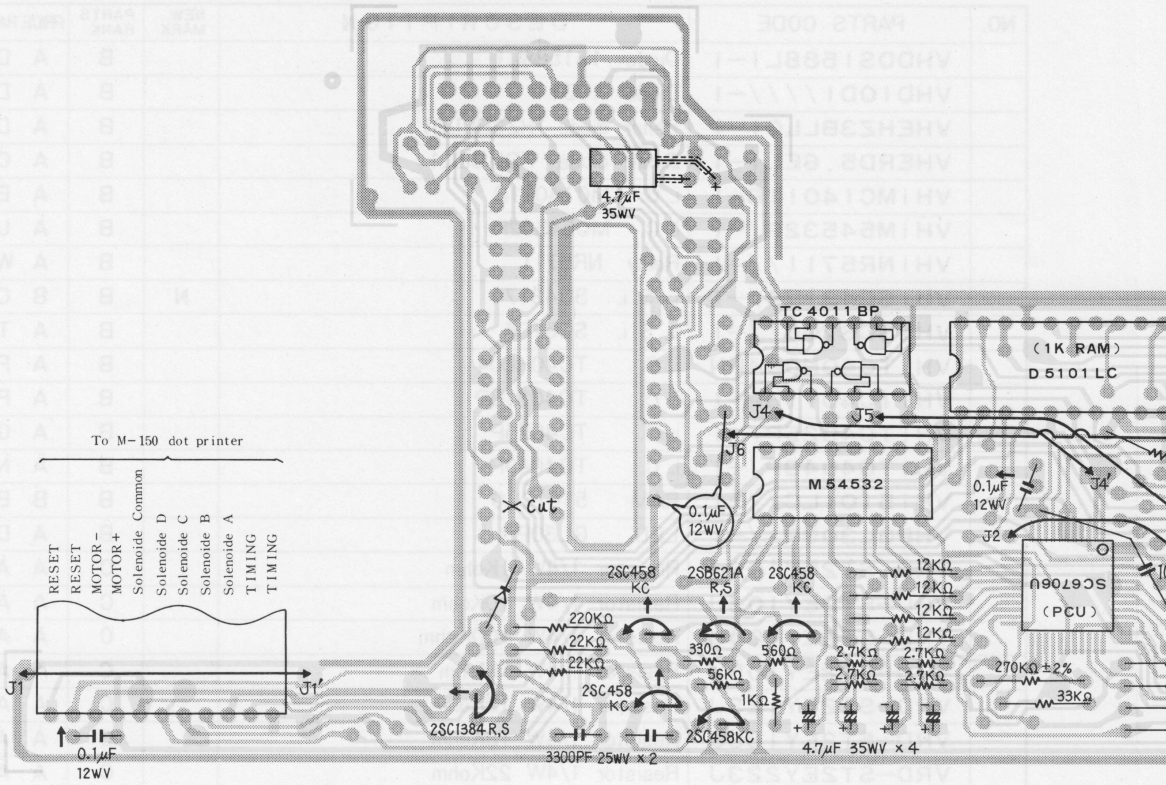
Symbol					PRINT (CE-122) 4 6 8 10 12 14 16	Jack			Tape recorder				Note
SHIFT	DEF	RUN	PRO	RESERVE		EAR	MIC	REM	PLAY	REC	REWIND	Sound	
			○		(Single or double carrier return)								Connect PC-1211 with CE-122.
			○										Push MODE key to turn it into PRO mode.
			○										
			○										
		○			1 : * * * * * * * PRINT								Push key of PC-1211 after turning on the PRINT switch.
		○			: * * * * * * * * GOSUB								
		○			: * * * * * * * * *								
		○			DEBUG * *								
		○			2 2 2 : A B C D E F G H I J K L								(Temporary halt until 222 lines are written) (6 lines)
		○			≀								
		○			A B C D E F G H I J K L								
		○			A B C D								
		○			9 9 9 : S I N < > T A N > =								
			○										
			○		(Carrier return)								
													Disconnect PC-1211 and CE-122.

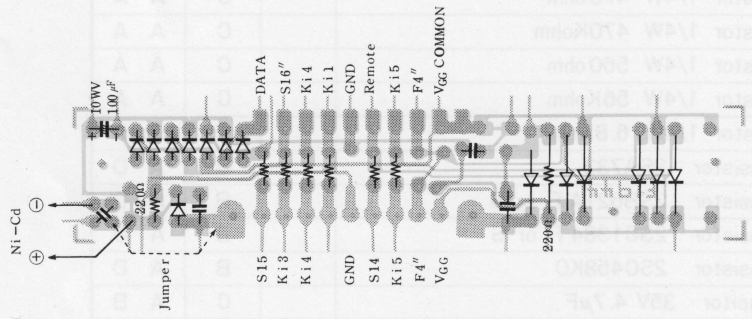
7. CIRCUIT DIAGRAM

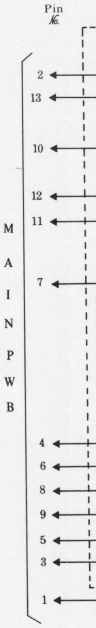


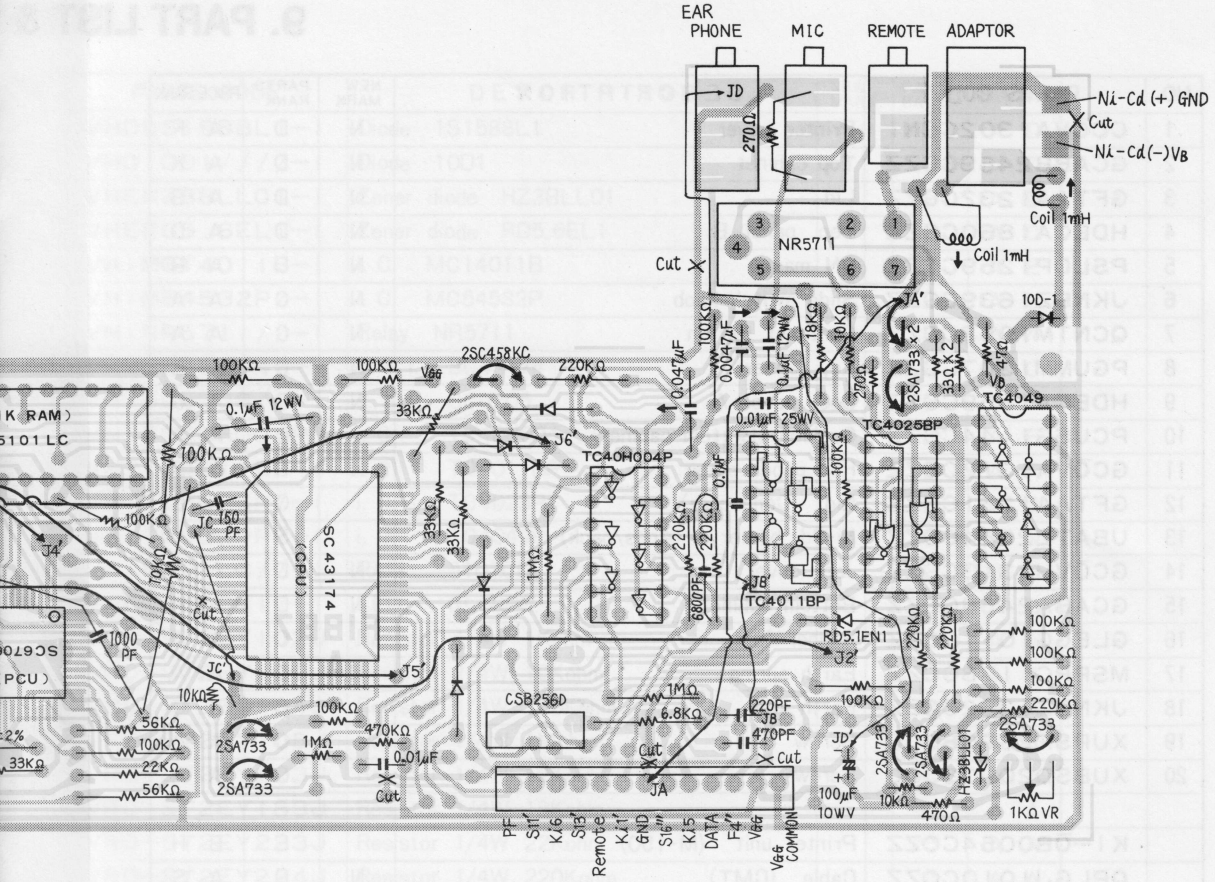

PF
LAMP
RMT CK
RMT SW
GND
TC4049
B
10KΩ
TC4011BP
S11
220KΩ
100KΩ
2SA 733
VGG
DATA S15
OUTION I/O BUSY KI3
TC40H004P
K1
6800PF
OPT I/O CONTROL S13
120KΩ
REMOTE S14
CMT LODING K15
CMT RECORDING F4
VGG COM
TC4049BP
TC4025BP
2SA733
0.01μF
470Ω
33KΩ
2SC 458
12 WV 0.1μF
S 1
S 2
S 3
S 4
S 5
S 6
S 7
S 8
S 9
S 10
S 11
S 12
S 13
S 14
S 15
S 16
K6 K5 K4 K3 K2 K1
43174
PU)
K5
S9
S8
2SA733×3
100KΩ×2
33Ω×2
18KΩ
0.01μF
0.0047μF
10KΩ
270Ω
0.1μF
0.047μF
Relay
NR5711
REMOTE
EARPHONE
MIC
COM

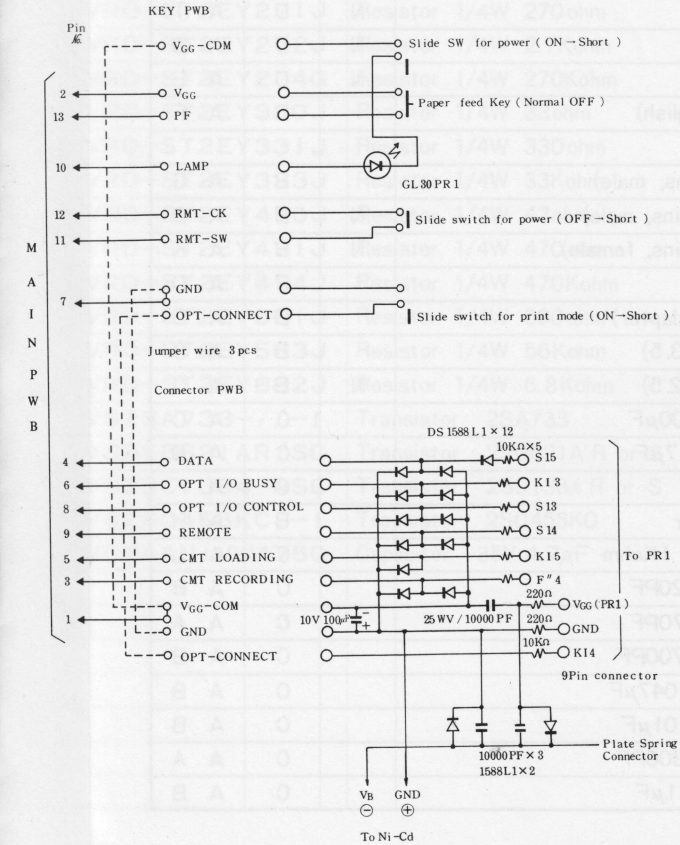
8. PARTS & SIGNAL POSITION








EAR PHONE
MIC
REMOTE
ADAPTOR
Ni-Cd (+) GND
Cut
Ni-Cd (-) VB
Coil 1mH
NR5711
Coil 1mH
Cut
JA'
10D-1
2SC458KC
TC40H004P
TC4049
TC4025BP
TC4011BP
SC43174 (CPU)
2SA733
RD5.1EN1
CSB256D
HZ33BLL01
1KΩ VR
JA
PF
SI1'
KI6
SI3'
Remote
KI1'
GND
SI6''
KI5
DATA
F4'
VGG
COMMON

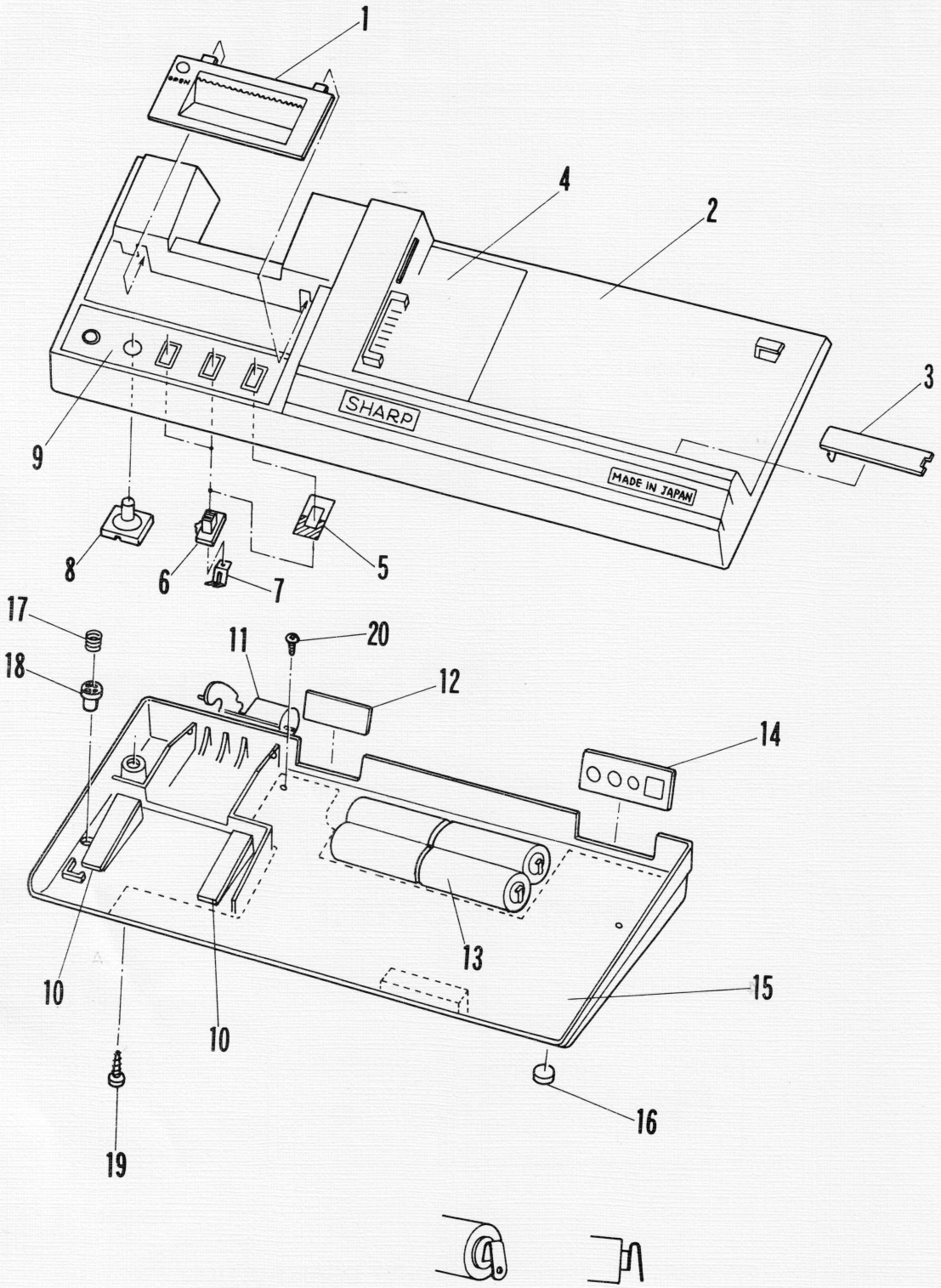

KEY PWB
Pin No.
VGG-CDM
Slide SW for power (ON → Short)
VGG
PF
Paper feed Key (Normal OFF)
LAMP
GL30PR1
RMT-CK
RMT-SW
Slide switch for power (OFF → Short)
GND
OPT-CONNECT
Slide switch for print mode (ON → Short)
Jumper wire 3pcs
Connector PWB
MAIN PWB
DS1588L1×12
DATA
OPT I/O BUSY
OPT I/O CONTROL
REMOTE
CMT LOADING
CMT RECORDING
VGG-COM
GND
OPT-CONNECT
S15
KI3
S13
S14
KI5
F''4
VGG (PR1)
GND
KI4
To PR1
9Pin connector
Plate Spring of Connector
10000PF×3
1588L1×2
VB
GND
To Ni-Cd

9. PART LIST &

NO.	PARTS CODE	DESCRIPTION	NEW MARK	PARTS RANK	PRICE RANK
1	CCŌVA1302CCN1	Printer cover	N	D	A F
2	GCABB2459CCZZ	Top cabinet	N	D	A K
3	GFTAA1232CCZZ	Lid	N	D	A B
4	HDECA1860CCZZ	Dec. panel B	N	D	A D
5	PSLDP1259CCZZ	ON mask	N	D	A B
6	JKNBZ1639CCZZ	Slide switch knob	N	C	A A
7	QCNTM1053CCZZ	Contanct switch	N	C	A A
8	PGUMM1307CCZZ	Key rubber	N	C	A B
9	HDECA1859CCZZ	Dec. panel A	N	D	A C
10	PCUSG1144CCZZ	Cushion (Bottom cabinet)		C	A A
11	GCŌVA1312CCZZ	Roll paper cover	N	D	A D
12	GFTAA1251CCZZ	Lid (Connector)		C	A B
13	UBATZ2064CCZZ	Ni-Cd battery (4pcs/pack)		S	A Y
14	GCŌVH131B3CCZZ	Jack cover	N	D	A C
15	GCABA2458CCZZ	Bottom cabinet	N	D	A K
16	GLEGG1011CCZZ	Rubber foot		C	A A
17	MSPRC1178CCZZ	Earth spring	N	C	A A
18	JKNBZ1362CCZZ	Earth knob		C	A C
19	XUPSF26P08000	Screw		C	A A
20	XUBSD20P05000	Screw		C	A A
	Ki—ŌB0054CCZZ	Printer unit (M-150)		E	B H
	QPLGJ1010CCZZ	Cable (CMT)	N	D	A S
	UBAGC1252CCZZ	Carring case	N	D	A T
	SPAKA5756CCZZ	Packing cushion	N	D	A D
	SPAKC5760CCZZ	Packing case	N	D	A E
	TiNSE3059CCZZ	Inst. book (English)		D	A F
	QCNCM1260CC0i	Connector (9pins, male)		B	A G
	QCNCM1280CC1C	Connector (13pins, male)	N	B	A D
	QCNCW1279CC01	Connector (13pins, female)	N	B	A K
	QCNW—1131CCZZ	Jumper wire		C	A D
	QJAKC1003CCZZ	Jack socket (Adapter)		B	A D
	QJAKC1013CCZZ	Jack socket (ϕ3.5)		B	A C
	QJAKC1016CCZZ	Jack socket (ϕ2.5)	N	B	A C
	RC—EZ1011CCZZ	Capacitor 10V 100μF		C	A C
	RC—EZ475ACC1V	Capacitor 35V 4.7μF		C	A B
	RCiLZ1022CCZZ	Coil (1mH)		C	A F
	RCRSP1024CCZZ	Ceramic oscillater		B	A H
	RVR—MI316CCZZ	Variable resistor 1Kohm		C	A L
	VCKYPU1HB221K	Capacitor 50V 220PF		C	A B
	VCKYPU1HB471K	Capacitor 50V 470PF		C	A A
	VCQYKU1HM472K	Capacitor 50V 4700PF		C	A B
	VCQYKU1HM473K	Capacitor 50V 0.047μF		C	A B
	VCTYPU1EX103M	Capacitor 25V 0.01μF		C	A B
	VCTYPU1EX332M	Capacitor 25V 3300PF		C	A A
	VCTYPU1NX104M	Capacitor 12V 0.1μF		C	A B

LIST & GUIDE

NO.	PARTS CODE	DESCRIPTION	NEW MARK	PARTS RANK	PRICE RANK
	VHDDS1588L1-1	Diode 1S1588L1		B	A D
	VHD10D1////-1	Diode 10D1		B	A D
	VHEHZ3BLL01-1	Zener diode HZ3BLL01		B	A D
	VHERD5.6EL1-1	Zener diode RD5.6EL1		B	A C
	VHiMC14011B-1	i. C. MC14011B		B	A E
	VHiM54532P/-1	i. C. MC54532P		B	A U
	VHiNR5711//-1	Relay NR5711		B	A W
	VHiSC43174/-1	L. S. i. SC43174	N	B	B C
	VHiSC6706//-1	L. S. i. SC6706		B	A T
	VHiTC40H004PN	i. C. TC40H004		B	A F
	VHiTC4011BP-1	i. C. TC4011BP		B	A F
	VHiTC4025P/-1	i. C. TC4025P		B	A G
	VHiTC4049P/-1	i. C. TC4049P		B	A N
	VHi5101LC//-1	RAM 5101CLC		B	B B
	VHPGL309R1/-1	LED GL30PR		B	A D
	VRD-ST2EY102J	Resistor 1/4W 1Kohm		C	A A
	VRD-ST2EY103J	Resistor 1/4W 10Kohm		C	A A
	VRD-ST2EY104J	Resistor 1/4W 100Kohm		C	A A
	VRD-ST2EY105J	Resistor 1/4W 1Mohm		C	A A
	VRD-ST2EY123J	Resistor 1/4W 12Kohm		C	A A
	VRD-ST2EY183J	Resistor 1/4W 18Kohm		C	A A
	VRD-ST2EY223J	Resistor 1/4W 22Kohm		C	A A
	VRD-ST2EY224J	Resistor 1/4W 220Kohm		C	A A
	VRD-ST2EY271J	Resistor 1/4W 270ohm		C	A A
	VRD-ST2EY272J	Resistor 1/4W 2.7Kohm		C	A A
	VRD-ST2EY274G	Resistor 1/4W 270Kohm		C	A A
	VRD-ST2EY330J	Resistor 1/4W 33ohm		C	A A
	VRD-ST2EY331J	Resistor 1/4W 330ohm		C	A A
	VRD-ST2EY333J	Resistor 1/4W 33Kohm		C	A A
	VRD-ST2EY470J	Resistor 1/4W 47ohm		C	A A
	VRD-ST2EY471J	Resistor 1/4W 470ohm		C	A A
	VRD-ST2EY474J	Resistor 1/4W 470Kohm		C	A A
	VRD-ST2EY561J	Resistor 1/4W 560ohm		C	A A
	VRD-ST2EY563J	Resistor 1/4W 56Kohm		C	A A
	VRD-ST2EY682J	Resistor 1/4W 6.8Kohm		C	A A
	VS2SA733-//-1	Transistor 2SA733		B	A D
	VS2SB621AR/SC	Transistor 2SB621A R or S		B	A D
	VS2SC1384-RSC	Transistor 2SC1384 R or S		B	A D
	VS2SC458KC/-1	Transistor 2SC458KC		B	A D
	VCEAAU1VW475Q	Capacitor 35V 4.7μF		C	A B


1
4
2
3
9
SHARP
MADE IN JAPAN
8
6
7
5
17
18
11
20
12
14
13
10
10
15
16
19

SHARP CORPORATION
Industrial Instruments Group
Reliability & Quality Control Department
Yamatokoriyama, Nara 639-11, Japan
1981 February Printed in Japan