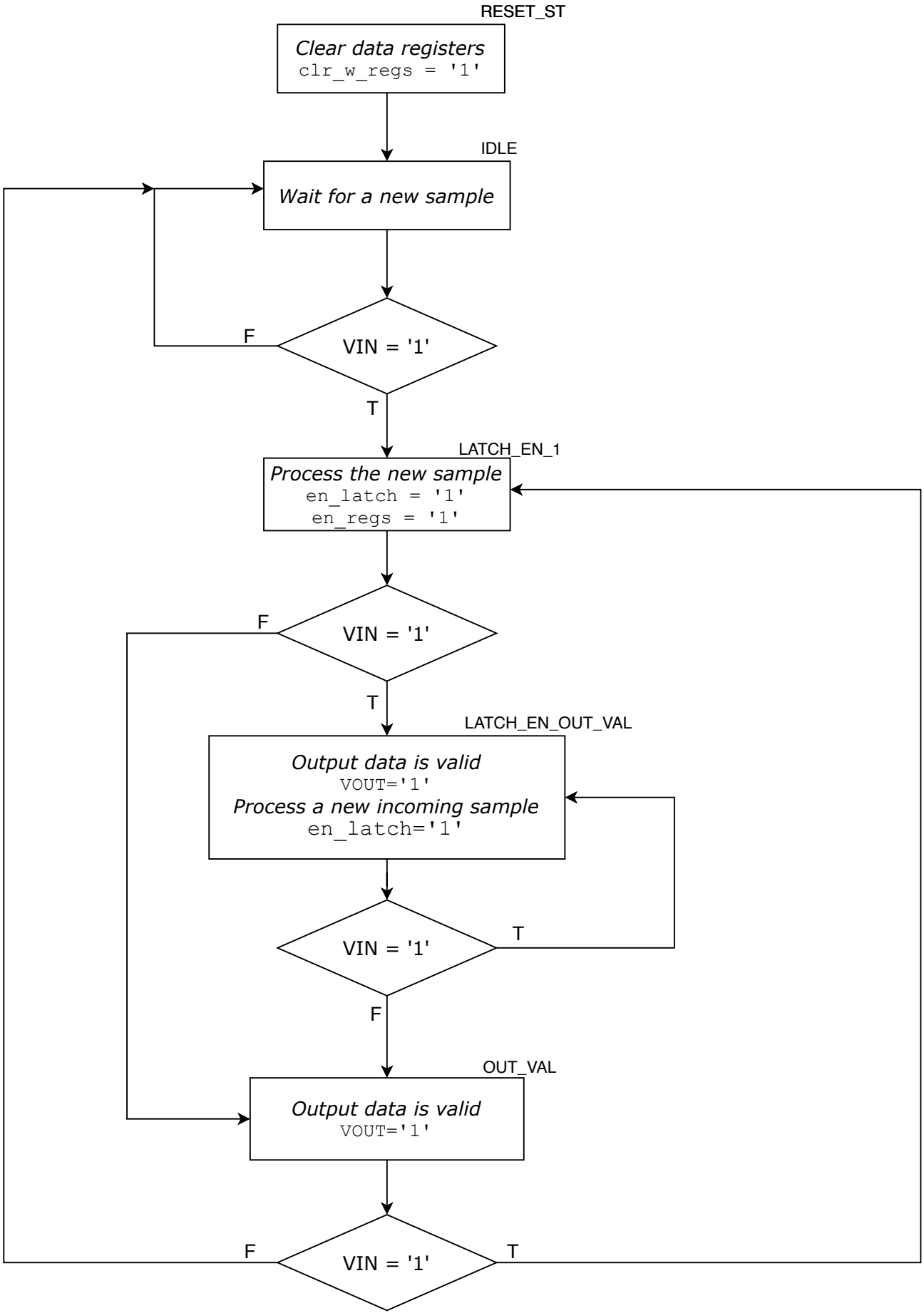
RESET_ST
Clear data registers
clr_w_regs = '1'
IDLE
Wait for a new sample
F
VIN = '1'
T
LATCH_EN_1
Process the new sample
en_latch = '1'
en_regs = '1'
F
VIN = '1'
T
LATCH_EN_OUT_VAL
Output data is valid
VOUT='1'
Process a new incoming sample
en_latch='1'
VIN = '1'
T
F
OUT_VAL
Output data is valid
VOUT='1'
F
VIN = '1'
T