Figure 1: Week 1, starting wafer.

Figure 2: Week 2, field oxidation, 0.52 μm

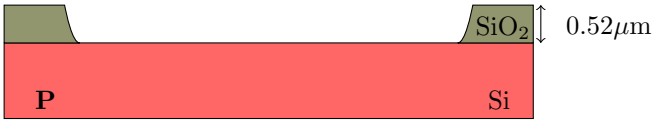

Figure 3: Week 3, ACTV photolithography and etch

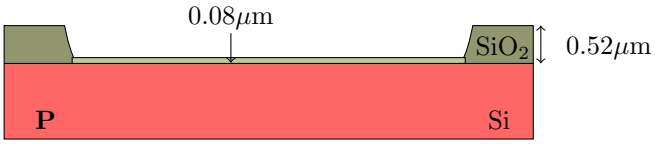

Figure 4: Week 4, gate oxidation. Gate oxide thickness is 0.08μm

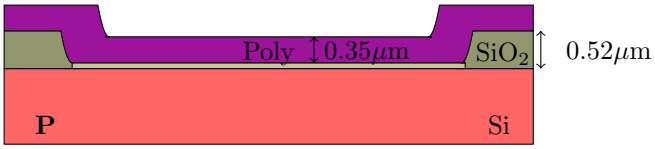

Figure 5: Week 5b, polysilicon CVD.

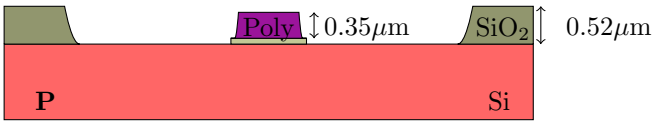

Figure 6: Week 6, polysilicon lithography and etch, Source/Drain clear

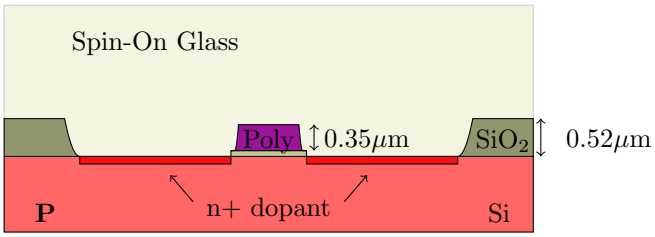

Figure 7a: Week 7a, spin-on glass and source/drain predeposition

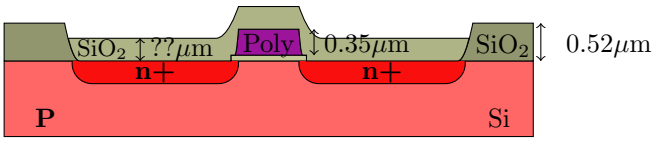

Figure 7b: Week 7b, drive-in and intermediate oxidation

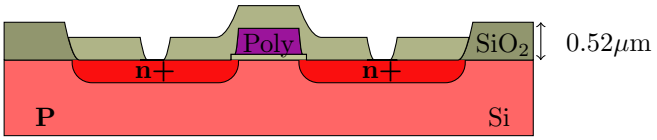

Figure 8: Week 8, contact hole lithography and etch

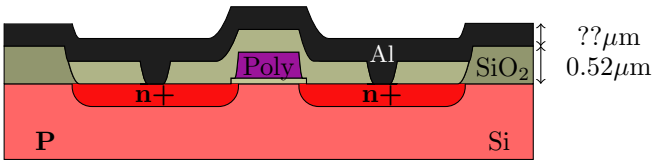

Figure 9: Week 9, aluminum evaporation

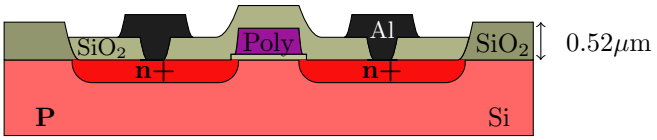

Figure 10: Week 10, metal lithography and etch