1 Profiles & Layout

1.1 MOSFET (test structure 8) cross-section

Draw cross-sectional profiles of a MOSFET (test structure 8) after each of the steps

Figure 1: W1: Starting Wafer

Figure 2: W2: Field Oxidation

Figure 3: W3: ACTV Photolithography and Etch

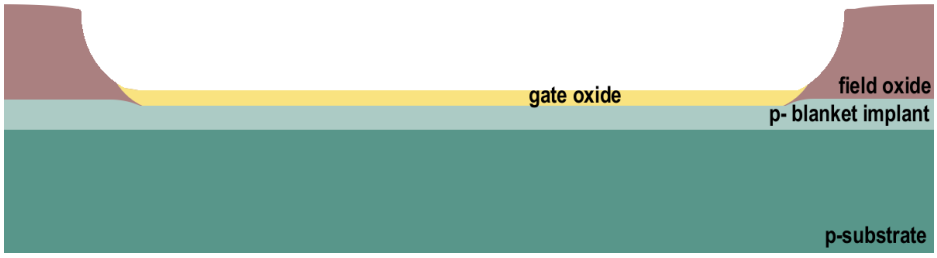

Figure 4: W4: Gate Oxidation

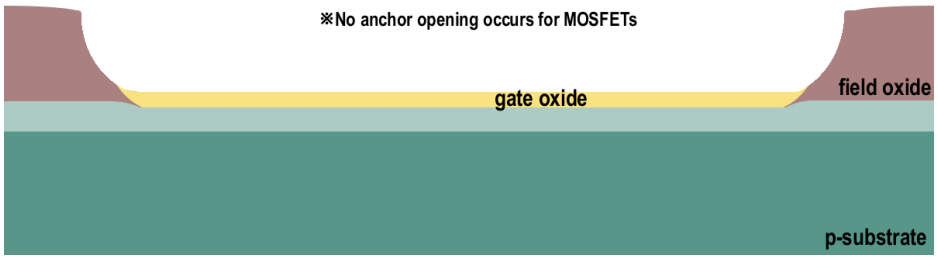

Figure 5: W5a: Anchor Opening Photolithography for MEMS

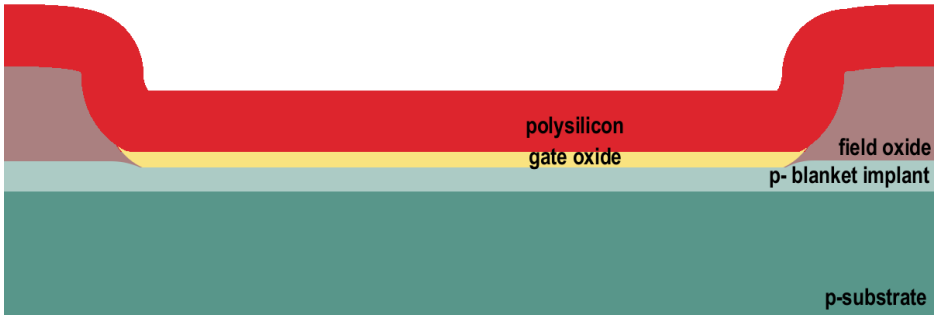

Figure 6: W5b: Polysilicon CVD

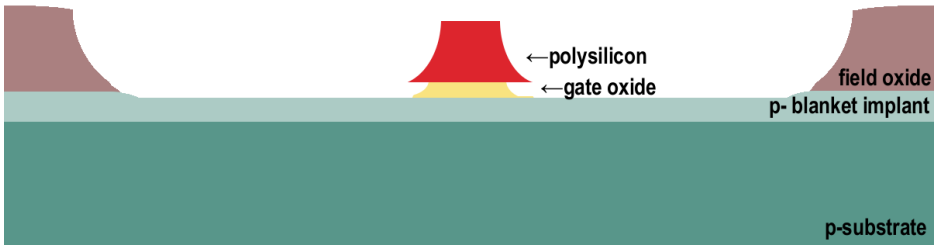

Figure 7: W6: POLY Lithography and Etch, Source/Drain Clear

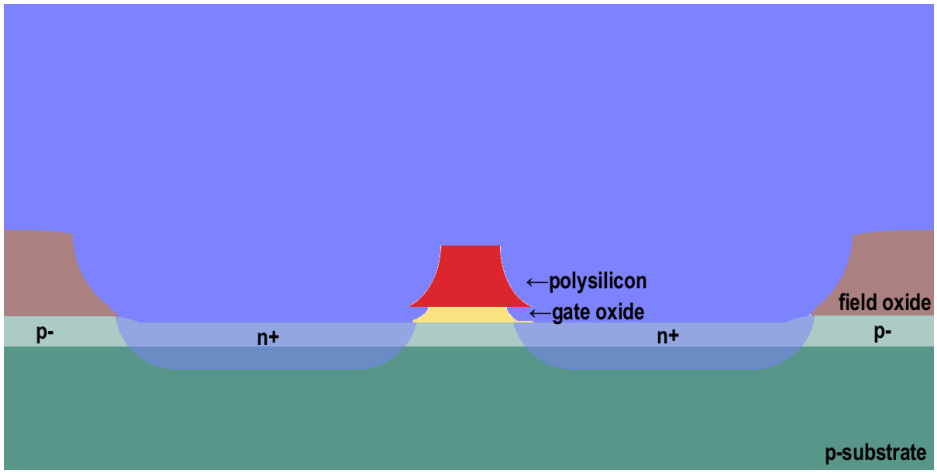

Figure 8: W7a: Spin-On Glass + Sourace/Drain Pre-diffusion

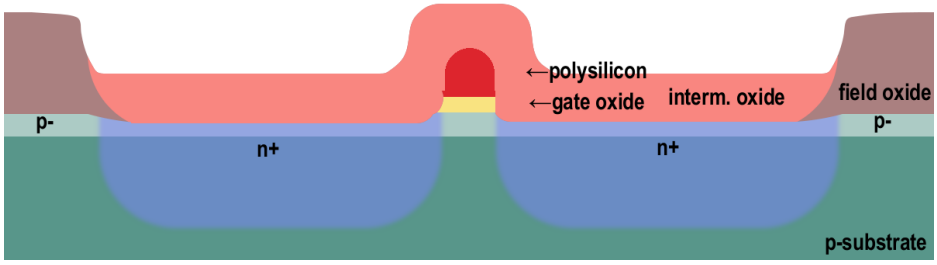

Figure 9: W7b: Source/Drain Drive-in + Intermediate Oxidation

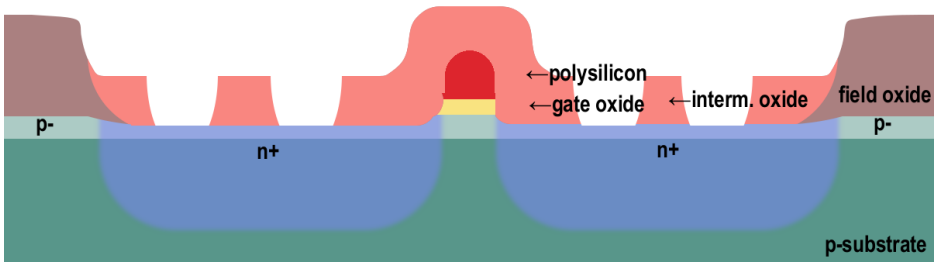

Figure 10: W8: CONT Photolithograph and Etch

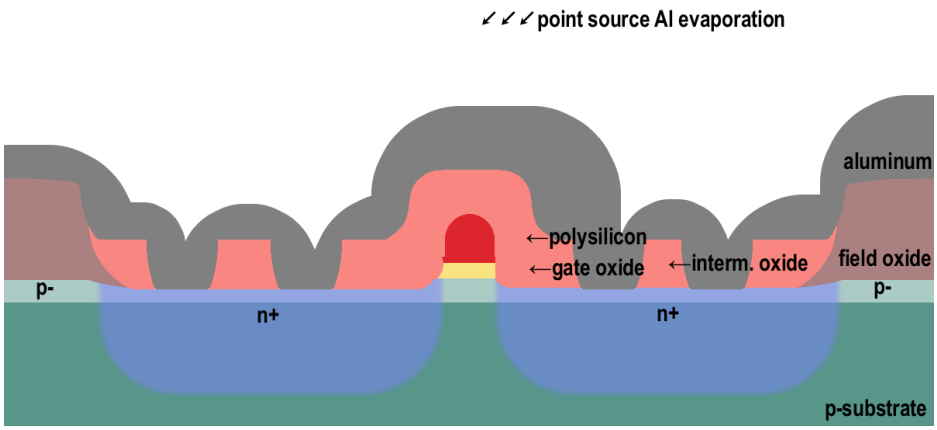

Figure 11: W9: Aluminum Evaporation

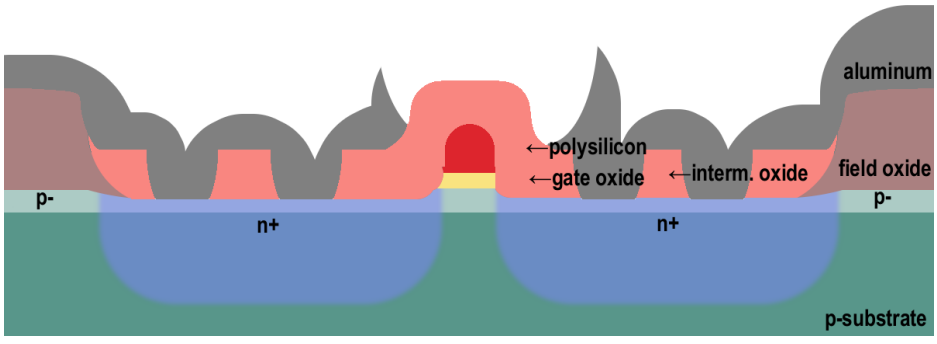

Figure 12: W10: METL Photolithography + Etch

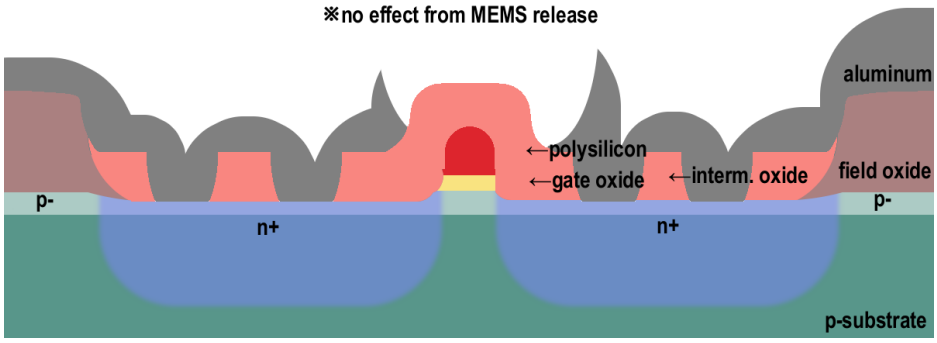

Figure 13: W11: MEMS Comb-drive Structure Release Photolithography + Etch

1.2 MOSFET (test structure 8) top-down view

Draw top views of the same thin-oxide MOSFET (test structure 8) after each of the four photolithography steps. [ACTV, POLY, CONT, METL] (4 Points)

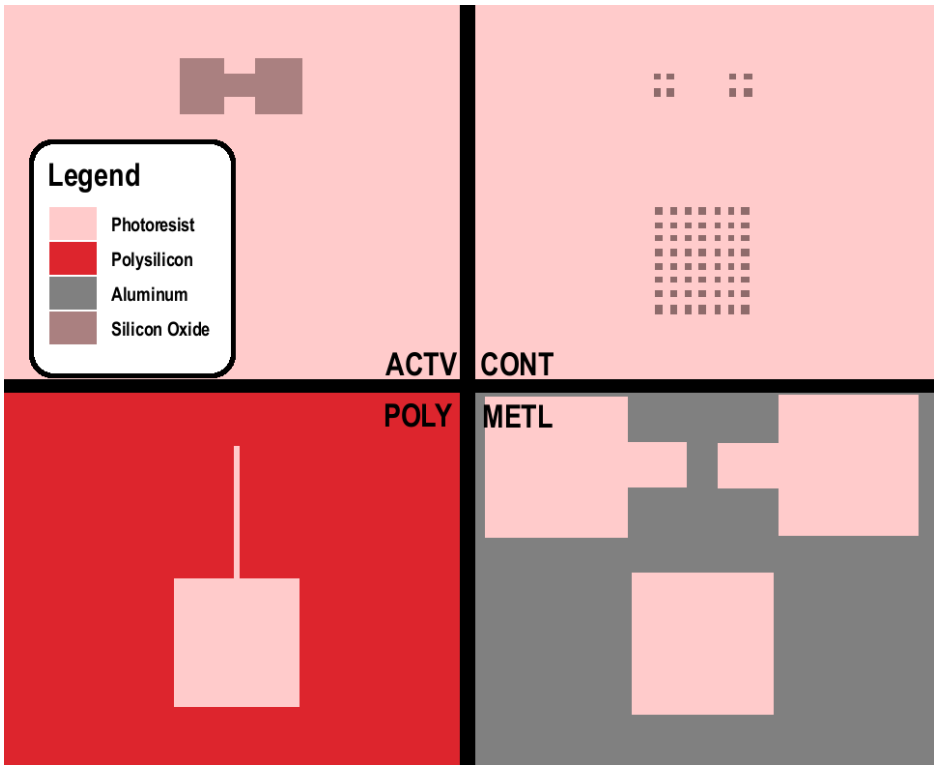

Figure 14: Top-down view of the MOSFET (test structure 8)

1.3 MEMS cross-section (test structure 22)

Draw cross-sectional profiles of the comb-drive (MEMS - test structure 22) after each of the 12 major processing steps, in the same fashion that you did for the MOSFET. See the diagram below for the exact cross-sections in question. The line runs through the anchor hole of the polystructure. (5 Points)

Figure 15: W1: Starting Wafer

Figure 16: W2: Field Oxidation

Figure 17: W3: ACTV Photolithography and Etch

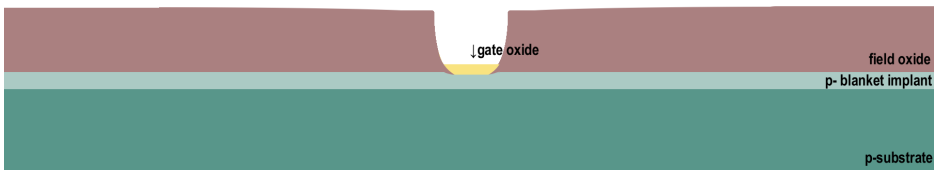

Figure 18: W4: Gate Oxidation

Figure 19: W5a: Anchor Opening Photolithography for MEMS

Figure 20: W5b: Polysilicon CVD

Figure 21: W6: POLY Lithography and Etch, Source/Drain Clear

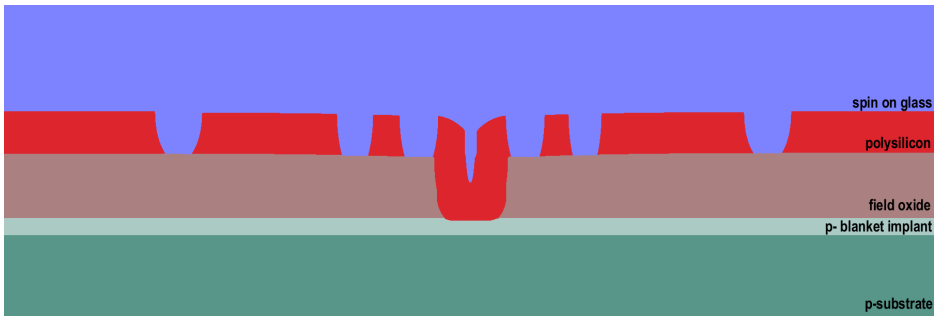

Figure 22: W7a: Spin-on Glass + Source/Drain Pre-diffusion

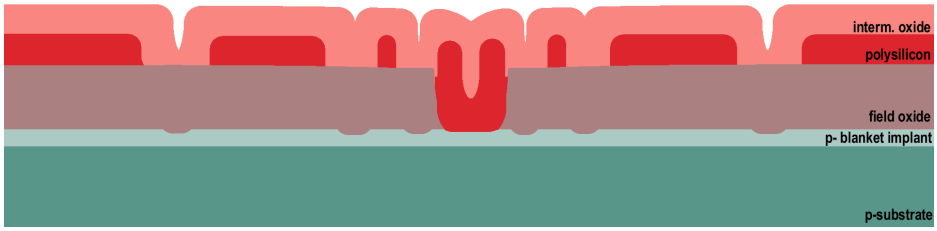

Figure 23: W7b: Source/Drain Drive-in + Intermediate Oxidation

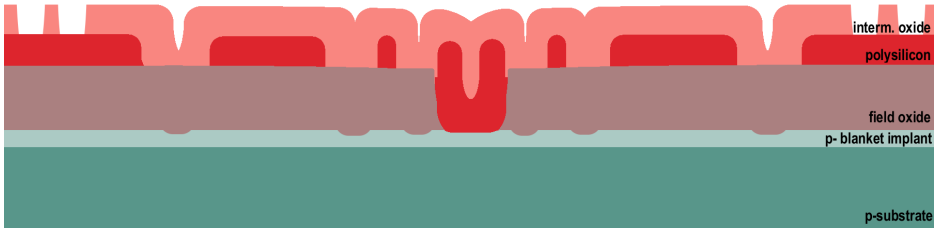

Figure 24: W8: CONT Photolithography and Etch

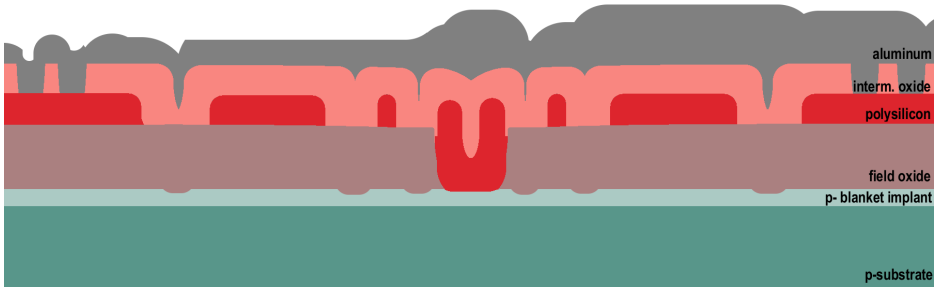

Figure 25: W9: Aluminum Evaporation

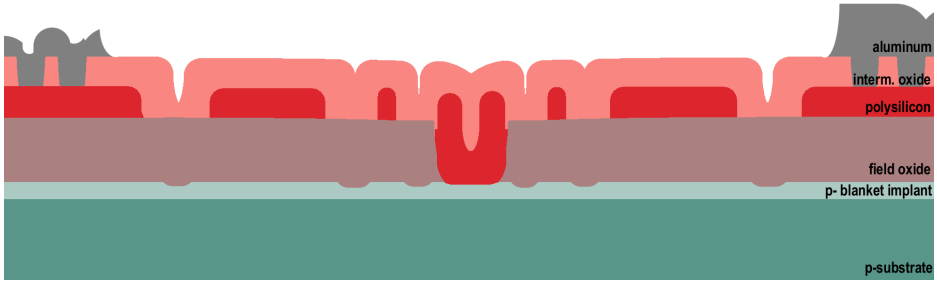

Figure 26: W10: METL Photolithography + Etch

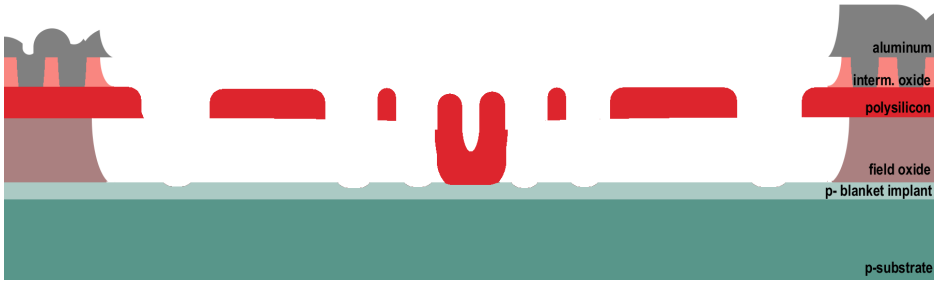

Figure 27: W11: MEMS Comb-drive Structure Release Photolithography + Etch

2 Process Procedures

2.1 Process Monitoring Measurements

Describe monitoring measurements that were done during processing:

Film color - Film color was used during etching processes. In order to determine wheather a layer had finished etching, we used visual queues by paying attention to the color change on the films. e.g. we know aluminum etch will have finished once the silver metalish color disappeared on the wafer.

Line Width - The width of 2 um lines were measured after photolithography and after etching and PR removal to determine the amount of overetch that occured for a given layer.

Thickness - The nanospec machine in the lab is used to measure film thicknesses. This can be done directly on our wafers or can be done on control wafers. We use control wafers in the process to measure certain film thicknesses as well as resistivities.

Resistivity - A four-point probe was used to measure the sheet resistance of the control wafer to monitor diffusion effects on doping concentration.

Vernier - Interlocking bars with slightly different spacing were produced by aligning the alignment keys of different mask layers. The offset of the bars allows the offset of the alignment between different layers to be determined very precisely.

Determine whether each layer was overetched or underetched? Did you purposely over/underetch? Why?

Field Oxide - Overetched. This was purposely overetched to ensure process latitude.
Polysilicon - Overetched. This was overetched in order to
Gate Oxide - Overetched. This was overetched in order to keep the source/drain clear.
Intermed Oxide - Overetched. This is because we want to make sure our contact holes are open before metalization. If the contact holes are blocked by oxide, our device will not function.
Aluminum - Overetched. This is done so contacts above the source/drain do not touch.

Describe how the verniers are used to measure misalignment. Using diagrams may help. Were any layers misaligned intentionally? For each pair of verniers (ACTVPOLY, ACTV-CONT, POLY-CONT, CONT-METL), describe how far the marks may be misaligned in terms of device function. (6 Points)

A vernier system usually looks like the figure below.

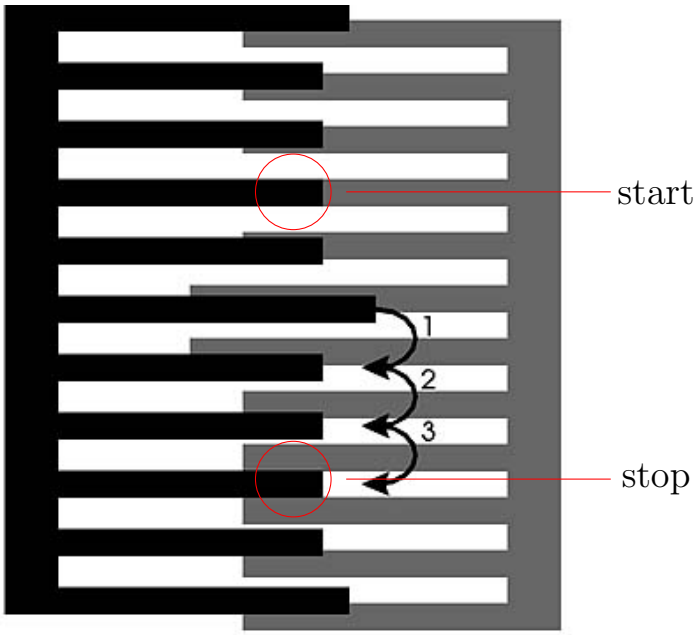

Figure 28: Typical vernier system.

The way vernier systems work is by aligning the square spacings in the middle. For our case, a spacing distance corresponds to 0.2 μm. Now more than likely the vernier spacing is not going to be perfect (like above), and as a result, you will have to calculate the misalignment by counting the spacings. To calculate the spacing, we start where the alignment between the verniers is perfect, this is circled in the above picture where it says 'start'. Now we count the number of spacings from the starting position until we hit alignment again, this is marked by 'stop' in the figure above. For the figure above, we count 5 spacings between alignment and since each spacing corresponds to 0.2 μm, this means we have a total misalignment of $0.2 * 5 = 1\,\mu$m. Now if you know exactly how much misalignment there was for a certain mask, you can repeat this same misalignment intentionally for the next mask in order to have the two masks aligned.

2.2 Batch Processing Steps

List and concisely describe the possible problems that could have occurred during the batch fabrication steps.
What were the sources of the problems, and how could you avoid them? How do you expect these deviations to affect the performance/function and cross-section of the device? List the types of monitoring measurements from Part A taken during each step (7 Points)

W2: Field Oxidation

- Thermal shock can occur when placing the wafer into the furnace. Also the time of oxidation could have been wrong and resulted in a different amount of oxide being grown.
- To fix the thermal shock problem we slowly placing the wafer into the furnace at a rate of 1 inch / 10 seconds. Using the nanospec we measured the oxide film thickness to make sure the right amount was grown.

W4: Gate Oxidation

- Depending on the cleaness of the clean room, particles and dust can get onto the gate oxide causing problems.
- Keeping the wafer inside a dark/clean box will help shield it from particles in the air.

W5: Poly Deposition

- Poly deposition takes a long time. This is because a LPCVD method is used by the nanolab to deposit the poly.

W7a: Source-Drain Prediffusion

- The dose rate is not well controlled and uniformity is not very good. Also since we are using diffusion, there is a max concentration rate because of the solid solubility limited reactions.

- One way to overcome the uniformity and dose rate problems is to use ion implantation instead of prediffusion. Also for dose rate, we use control wafers to measure resistivity.

W7b: Drive-In & Intermediate Oxidation

- The same problems that occur with prediffusion and oxide growth can occur here. The wrong amount of intermediate oxide can be grown which will cause problems later on when etching holes for the contacts.
- Using the nanoscope and control wafers to measure oxide growth will help prevent growing the wrong amount of an oxide film.

W9: Aluminum Evaporation

- Pressure not pumping below a certain amount (e.g. 1e-4 torr). No aluminum being evaporation onto a wafer.
- If there is not aluminum being evaporated then the tungsten coal might be contaminated and should be changed. If the pumping is not reaching certain pressures then there might be a leak somewhere. Make sure to clean the evaporator and check for any leaks.

W10: Sintering

- Having to high of a temperature can cause the silicon to diffuse into the aluminum contacts. As a result, spikes can form inside the source and drain. If these speaks go all the way through the heavily doped source/drain into the silicon substrate, the device is dead.
- One way to avoid this is to have 1% silicon already diffused in the aluminum before evaporation. This causes the aluminum to reach its solid solubility limit and won't allow more silicon to diffuse in creating spikes.

2.3 Individual Processing Steps

3 Calculations

a) Film Thickness

Layer	Theoretical calculation (nm)	Experimental (nm)	% Error	Linewidths (photoresist) (nm)	Linewidths (after PR Strip) (nm)	% Overetch
Field Oxide	505.8	477.2	5.65	2000	3000	50
Polysilicon	350	400	14	3628	4000	10
Gate Oxide	80.1	86.5	7.40	3628	4000	10
Intermed Oxide	386.3	320	17.2	2749	1869	47
Aluminum	800	N/A	N/A	2088	2520	21

Figure 29: film thicknesses and line widths for various thin films. N/A represents data that was not available.

b) Sheet Resistance

Layer	Sheet Resistance Ω/sqr	Surface Concentration (cm^{-3})
ACTV after Field Oxidation	530	6×10^{19}
Polysilicon	730	4×10^{19}
ACTV after Pre-Dep	5	5×10^{22}
ACTV after Drive-In	8	10^{21}
Metal	N/A	N/A

Figure 30: Surface concentrations calculated from sheet resistance using the irvin curves in jaeger (figure 4.16). The surface concentration used here is $N_B = 8 \times 10^{14}$ according to the silicon wafer resistivity. Junction depths for pre-diffusion and drive-in were calculated in Appendix 6.2. For field oxide, the junction depth used was the amount of silicon consumed when growing the field oxide ((0.46)(477 nm) = 219 nm). For poly and gate oxide, we calculated ((0.46)(86.5) = 39.8 nm) of silicon that got consumed during gate oxide growth. Therefore a junction depth of 219 + 39.8 = 258.8 nm. Refer to Appendix 6.1 for how to calculate oxide thickness.

c) Overetch

Layer	Measured Linewidth (nm)	% Overetch	Theoretical etch time (min)	Actual etch time (min)	% Overetch
Field Oxide	3000	50	4.8	6	25
Polysilicon	4000	10	1.6	~ 2.25	41
Gate Oxide	4000	10	0.87	0.83	4.6
Intermed Oxide	1869	47	3.2	4.5	41
Aluminum	2520	21	1.4	~ 5	360

Figure 31: Linewidth measurements and etch times used during lab. The theoretical etch times were calculated with etch rates and film thicknesses.

1) Theoretical and experimental thicknesses of field oxide, gate and intermediate oxides (Include orientation dependence of oxidation rate but not impurity dependence) (9 points)
For details on the theoretical oxide thickness calculations see Appendix 6.1.

Layer	Theoretical (nm)	Experimental (nm)	% Error
Field Oxide	505.8	477.2	5.65
Gate Oxide	80.1	86.5	7.40
Intermed Oxide	386.3	320	17.2

Figure 32: Theoretical values refers to the values found in the lab processing flow while experimental values are what was actually calculated based on etch rate and actual film thickness. See Appendix 6.1 for how to calculate oxide growth rates.

2) Junction depths after pre-diffusion and drive-in (theoretical, assume only phosphorous doping with surface concentration limited by solid solubility). You must consider the effect of the initial ion implantation. For pre-deposition you may use the box approximation, but for drive-in you must use the half-gaussian calculation. Why is this? (10 points)
For details on the junction depth calculations see Appendix 6.2. Also the reason we use a box approximation for the pre-diffusion is because we have a constant source profile. However, for drive-in we now have source-limited diffusion.

Step	Vertical junction Depth (nm)
Pre-diffusion	365
Drive-in	1000

Figure 33: pre diffusion and drive in junction depths for NMOS structure.

3) Final surface concentrations of dopants, as determined from Irvin's curves using sheet resistance measurements made in lab. (2 points)
Refer to Figure 30

4) Plot or sketch the change of dopant profile from the silicon surface through the source-drain after each thermal step. Quantitatively label significant points such as Peak concentration, Peak Width, Junction Depth. Show movement of the Silicon-Silicon Dioxide interface and qualitatively show non-ideal effects such as dopant redistribution during oxidation. (11 points)
The profiles were all created in Tsuprem-4 using the EE143 process flow and verified by hand calculations. The oxide growth and dopand concentrations were compared with the values calculated for other questions and are reasonably close enough to be accurate. Note that tsuprem4 takes into account a lot of other things that don't make it into the hand calculations. See Appendix 6.3 for the script file used to generate these plots.

- After initial silicon implant

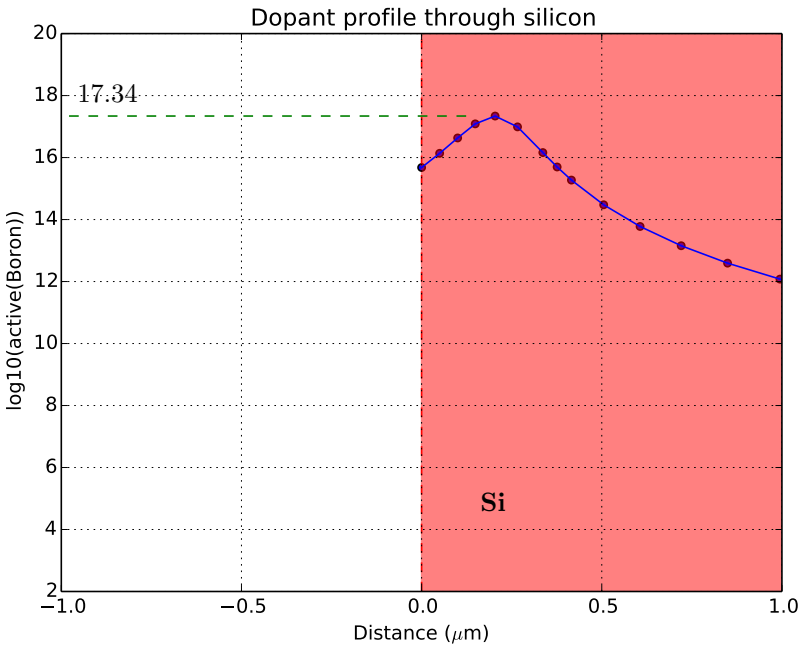

Figure 34: Doping profile of the bare silicon before any oxidation occurs, but after the original implant that occurs.

- After field Oxidation

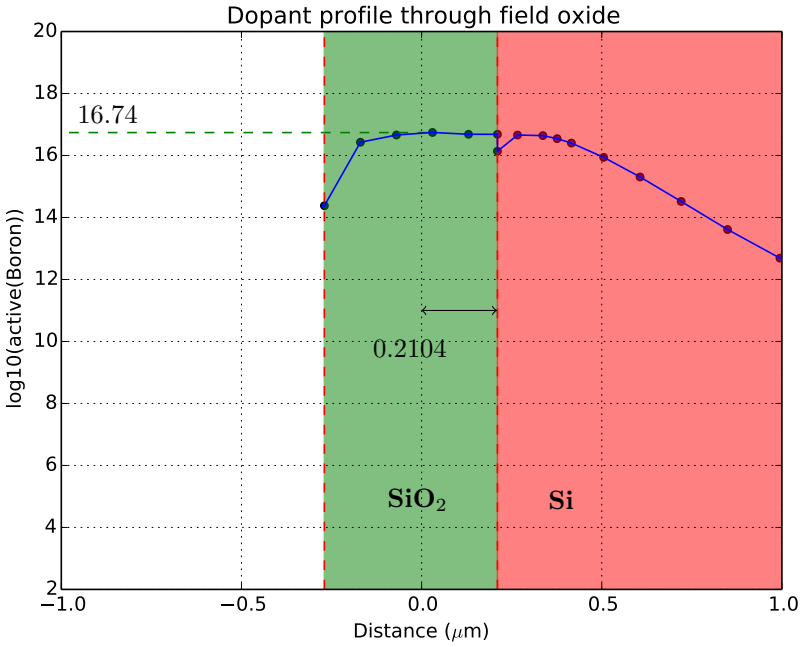

Figure 35: Dopant profile with only field oxide. The Si-SiO_2 interface occurs at 0.2104μm. There was about 500 nm of field oxide deposited here. The peak concentration is roughly $10^{16.74}$. Note the dopant redistribution effects evident from the original distribution in Figure 32.

- Gate Oxidation

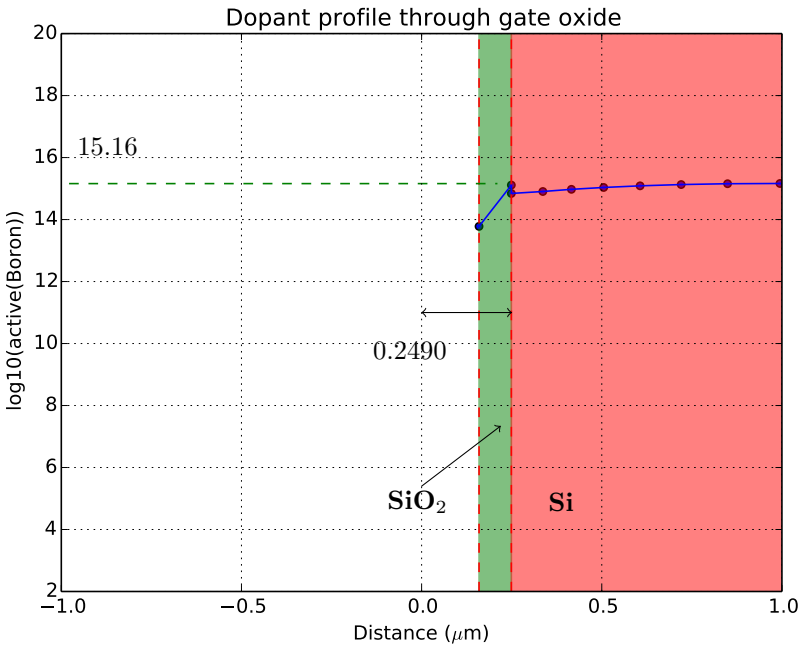

Figure 36: Dopant profile with after gate oxide. The Si-SiO_2 interface occurs at 0.2490μm. There was about 86 nm of gate oxide deposited here. The peak concentration is roughly $10^{15.16}$. Note the drastic dopant redistribution effects.

- Poly-Deposition

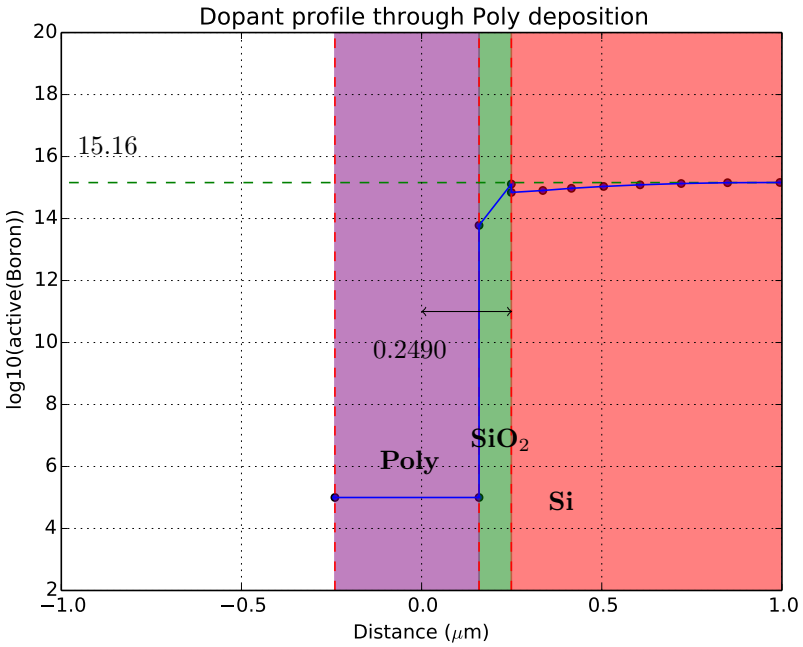

Figure 37: Dopant profile after Poly deposition. The Si-SiO_2 interface occurs at 0.2490μm. 400 nm of Poly was depositied. The peak concentration is roughly $10^{15.16}$. Note the drastic dopant redistribution effects.

- Pre-Deposition

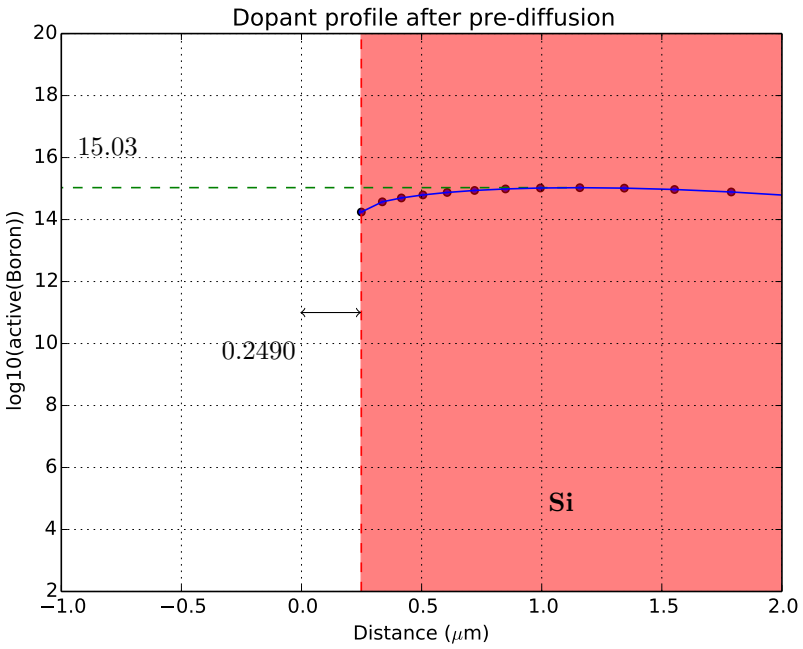

Figure 38: Dopant profile after Poly deposition. The Si-SiO_2 interface occurs at 0.2490μm. 400 nm of Poly was depositied. The peak concentration is roughly $10^{15.16}$. Note the drastic dopant redistribution effects.

- Drive-in & Intermediate oxide

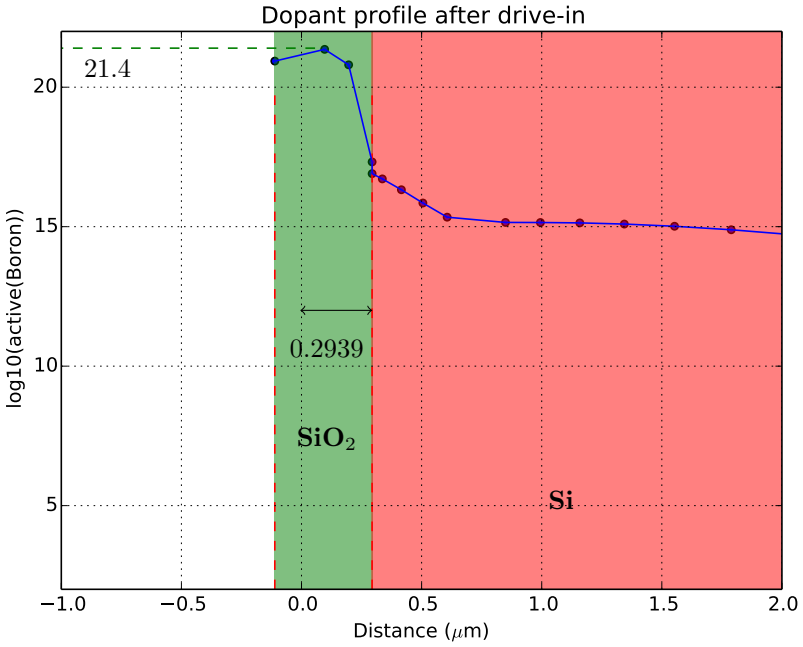

Figure 39: Dopant profile after drive-in. The Si-SiO_2 interface occurs at 0.2939μm. The peak concentration is roughly $10^{21.4}$..

5) Lateral diffusion under the MOSFET gates. You may estimate. Justify estimation. (Theoretical). (2 points)

Using the data calculated in Appendix 6.2, we see that for pre diffusion $N_0 = 10^{21}/\text{cm}^3$ and $N_B = 8 \times 10^{14}/\text{cm}^3$. Now we will use figure 4.10a [1] in the textbook and note that $N_B/N_0 \approx 10^{-7}$. Since our data goes off the graph in the figure, we will make an approximation that every multiple of 10 decrease in N_B/N_0 results in a vertical and lateral

junction depth increase of 0.5. Using this approximation we get a vertical junction depth of 4.3 and a lateral depth of 3.8. This gives us $3.8/4.3 = 0.88$. Now from our earlier junction depth calculations we see that pre diffustion resulted in a depth of 365 nm. Thus $(365)0.88 = 321$ nm lateral junction depth for pre diffusion. For drive-in we have the same values of N_B and N_0, but our junction depth here increased by 1000 nm. Thus $(1000)0.88 = 880$ nm.

Step	Lateral junction Depth (nm)
Pre-diffusion	321
Drive-in	880

6) List an estimate of the Young's modulus, Poisson ratio, and coefficient of thermalexpansion for SiO_2, poly-Si, and Al films as deposited. (You can find these in a table in many physics/ME textbooks, or in a web-based search.) (2 points)
See table below

Material	Young's modulus (GPa)	coeff. of thermal expansion (K^{-1})	Poisson's ratio (a.u.)
SiO_2 [3]	57(dry)-70(wet)	$5.6 \cdot 10^{-7}$	0.17
poly-Si [2]	169 ± 6.15	$4.6 \cdot 10^{-6}$	$0.22 \pm .011$
Aluminum [4]	70	$22.2 \cdot 10^{-6}$	0.33

Figure 40: Values were found from various journals/articles found online ([2],[3], and[4]) and many of these values are calculated for thin films of the material.

4 Questions

1) What type of photoresist (positive or negative? I-line or G-line?) do we use in the lab? What do I-line and G-line refer to? Briefly describe how the resist responds to the process steps like spinning, UV light exposure and development.
The lab uses positive photoresist. The lithography machine uses a light that has g line wavelength. The I and G lines refer to the wavelength of the light coming off the light bulb that reacts with the photoresist. G line is roughly 436nm wavelength and I line is 365nm wavelength. Photoresist is spun onto the wafer to spread it evenly over the wafer, but extreme topology and surface debris can cause excess PR in some areas and deficient PR in others. When exposed to UV light, the photo-sensitive part of the polymer activates changing it into an organic acid, whereas unexposed PR remains unchanged. When dipped into the PR developer, the organic acid form of the PR dissolves whereas the polymer form remains on the wafer, leaving a layer PR that masks certain areas of the wafer.

2) What is the purpose of baking the wafers at 120 °C before depositing HMDS? What is the purpose of the 90 °C bake after spinning on photoresist? What happens if the soft bake is too hot and too long (say 120 °C, 5 minutes)?
The purpose of baking the wafers at 120°C before depositing HMDS is to remove excess environmental moisture that has accumulated on the wafer. The purpose of the 90°C bake after spinning on photoresist is to evaporate the solvent and make it less sticky. If the soft bake is too long, the photoactive component of the PR may start to decompose and the PR may become less soluable in the developer.

3) What is the purpose of hard bake? What happens if we skip this step? What may happen if the bake is done at a temperature above 120 °C (say 200 °C)?
The purpose of the hard bake is to cross-polymerize the PR, making it less permeable to chemicals, more adhesive, and physically harder. If this step is skipped, subsequent etching and similar steps have a chance of penetrating the PR, making the mask meaningless. If the bake is done at a temperature above 120°C, the PR will start to become brittle, resulting in cracks that would also make the masking step meaningless.

4) We do lithography steps under yellow light only. What is the consequence if we expose the wafers to fluorescent light before development? What if we expose them to fluorescent light after development? Would red light damage your process?
If the fluorescent light happens to be near the wavelength of the g-line, it will react with the photoresist and make it soluble. Since there is no mask over the wafer at that time, it will make all the photoresist souble which will cause the developer to remove all the photoresist. If it were exposed after developement, it will still make the remaining

photoresist soluble, but since we have already done developement, there is no risk of the remaining photoresist coming off (unless we were to dip it in the developer again).

5) What are the differences between wet and dry oxidation that lead us to use one for the gate oxide and one for the field/intermediate oxide? What is the purpose of annealing in nitrogen after oxidation?
Wet oxidation has a higher growth rate but a tendency to create dangling bonds and a lower density oxide, making it more suitable for the thick field/intermediate oxide. Dry oxidation is much slower but creates a higher density oxide with fewer dangling bonds, making it more suitable for creating the thin gate oxide that is critical in device performance. The purpose of annealing in nitrogen is to allow the silicon atoms to diffuse and repair damage done by oxidization.

6) How do you determine etching time using theoretical etch rate in literature? List two ways to determine etch time empirically from lab measurements, when you etch the layers. (Hint: these methods include visual cues.). How close are the experimental and the theoretically calculated values?

7) Before n+ deposition (prior to SOG spinning), we clean in Piranha but not in HF. Before gate oxidation, we clean in both. Why the difference?
For n+ deposition, we are depositing PSG (a phosphorate-doped oxide) on top of the wafer for diffusion. The presence of a native oxide on the surface serves as a barrier material between the PSG and the silicon, preventing unwanted inter-diffusion effects. However, for growing a high-quality gate oxide, the poor-quality native oxide will adversely affect results, thus it must be removed with an HF dip.

8) Why is 5:1 BHF (5:1 NH_4F:HF) used for etching features in the oxide while 10:1 BHF is used for cleaning and spin-on-glass stripping? Why buffered HF?
We use buffered HF because normal HF etches way too quickly and tends to peel off photoresist as well. Using buffered HF allows for more controllable and constant etching which allows for good process control. According to the process flow, spin on glass etches at 470 nm/sec in 10:1 BHF while thermally grown oxide etches at 100nm/sec in 5:1 BHF. If we had used 5:1 BHF for the spin on glass, it would etch way to quickly and be difficult to control.

9) What would happen if we skipped the HF dip before metallization?
Skipping the HF dip before metallization would result in a thin layer of native oxide at the Al-Si interface, causing poor contact with the devices on the wafer.

10) What is etch selectivity?
Etch selectivity is the relative difference in etch rates for given materials on the wafer. Ideally, the etch should be highly selective towards the material to be etched and thus etch it the fastest whereas other material, like the PR, should etch much more slowly.

11) Why do we first use the roughing pump and then the diffusion pump when pumping down the aluminum deposition system? Why must the foreline pressure be kept below 100 mTorr?

12) What is the Al etchant composed of? What happens if you use it at room temperature? What is the purpose of sintering? What will result if sintering step is skipped? What happens if sintering temperature is too hot or too low?
Al etchant has a composition of 80% Phosphoric acid, 10% H2, 5% acetic acid, and 5% nitric acid. It etches much more slowly at room temperature then at 50 degC. Sintering allows the aluminum and silicon to interdiffuse, resulting in a good contact, as well as allowing hydrogen to diffuse into the oxide and tie up dangling bonds. If the sintering step is skipped, the contact may be poor. If the sintering temperature is too hot, the eutectic Al-Si system will melt. If the sintering temeperature is too low, the contact resistance between the aluminum and silicon will be too high.

13) Briefly explain the mechanism of XeF_2 etching. Is the etch isotropic or anisotropic? In an integrated CMOS/MEMS process, is there any consequence to using KOH instead of XeF_2 for etch?
XeF2 gas is absorbed by the silicon surface, where it breaks down into xenon and fluoride gas. The fluoride gas reacts with the silicon to form SiF2 gas, and both the xenon and SiF2 gas are released back into the air. XeF2 etching is isotropic. Using KOH as an etchant instead of XeF2 has two consequences. First, it is anisotropic and therefore less efficient at undercutting the beam. Secondly, it is a wet etch and liquid etchants can cause the freed structure to stick to the substrate.

14) . What would happen if a thick oxide film was left on the wafers as it went into the XeF_2 etching step?
Since XeF2 is highly selective against SiO2, the structure would not be freed as the etchant would not be able to etch through the oxide film to the silicon below.

15) Identify two of the 11 major processing steps that are unnecessary to fabricate a functional oxide cantilever beam. Why are they unnecessary?
Gate oxidation and S/D deposition are unnecessary to fabricating a functional oxide cantilever beam. The cantilever requires no gate so any gate oxide grown during this step must later be removed, and doping plays no part in the functioning of a cantilever device, so S/D deposition can also be skipped.

5 Bonus Questions (up to 10 Points)

1) Simulate the 143 process flow in Tsuprem4 (8 points) (updated on 11/20/14, you only need to simulate the NMOS LDD example available online (i.e., s4ex4a, -b, - c.inp))
I ran the files provided to us by Wei-chang on one of the eecs linux servers that had tusprem-4 installed. I only changed input/output directories in the script files to get them to work properly. Here is the resulting figure that is plotted after compiling and running the example NMOS.

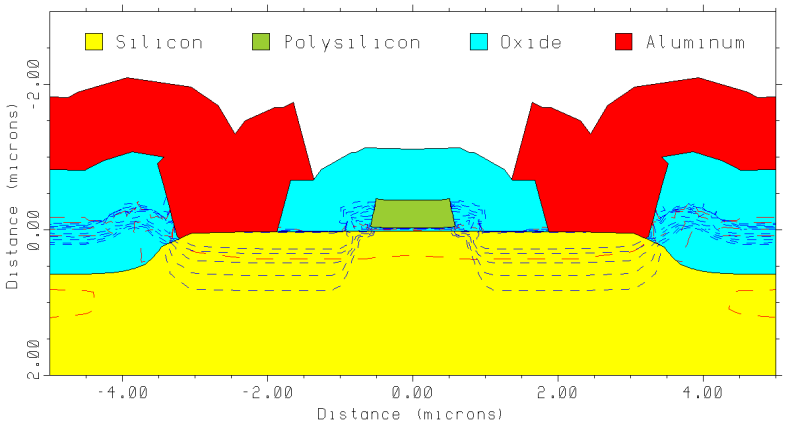

Figure 41: tsuprem4 generated NMOS example process

2) Describe an alternate method for doing one of the process steps (i.e. LOCOS instead of Field Oxide, Sputtering instead of Evaporation, etc) and the tradeoffs.

6 Appendix

6.1 Oxide Thickness calculations

Film thickness calculation for oxides:

$$X_{ox} = \frac{0.5B}{B/A}\left[\sqrt{1+\frac{4}{B}(\frac{B}{A})^2(t+\tau)}-1\right] \tag{1}$$

$$\tau = \frac{{X_i}^2}{B} + \frac{X_i}{B/A} \tag{2}$$

where

$B/A = D_o e^{\frac{-E_a}{kT}}$ (Use table 3.1 [1] to find $E_a$and D_o)
$B = D_o e^{\frac{-E_a}{kT}}$ (Use table 3.1 [1] to find $E_a$and D_o)
t = Time of oxide growth
τ = Time of initial oxide growth already present
X_i = length of initial oxide growth

Example: Calculated oxide thickness of Intermed Oxide:
Given: 5 min dry oxidation at 1050°C and 12 + 25 min wet oxidation annealing at 1050°C, calculate oxide growth.

First we consider the 5 min dry oxidation. Using table 3.1 [1] for a $< 100 >$ Silicon, and using dry oxidation, we see that for the linear rate constant (B/A), $E_A = 2.00$ eV and $D_o = 3.71 \times 10^6\,\mu$m/hr. For the parabolic rate constant (B), $E_A = 1.23$

eV and $D_o = 772\,\mu$m/hr.

Using an arrhenius equation where k = Boltzmann's constant, and T = temperature.

$$B/A = D_o e^{\frac{-E_A}{kT}} = 3.71 \times 10^6 e^{\frac{-2.00*1.602\times10^{-19}}{1.38\times10^{-23}(1050^\circ C+273)}} = 0.0887\mu\text{m/hr}$$
$$B = D_o e^{\frac{-E_A}{kT}} = 772 e^{\frac{-1.23*1.602\times10^{-19}}{1.38\times10^{-23}(1050^\circ C+273)}} = 0.0159\,\mu\text{m}^2/\text{hr}$$

Since there is no initial oxide here, $\tau = 0$,

$$X_{ox} = \frac{0.5B}{B/A}\Big[\sqrt{1+\frac{4}{B}(\frac{B}{A})^2(t+\tau)} - 1\Big] = \frac{0.5(0.0159)}{0.0887}\Big[\sqrt{1+\frac{4}{0.0159}(0.0887)^2(\frac{5\text{min}}{60\text{min/hr}}+0)} - 1\Big] \approx 7.11\,\text{nm}$$

Now after this dry oxidation, we have a 37 minute wet oxidation at 1050°C. Using table 3.1 [1] again, but this time using the constants that apply for wet oxidation,

$$B/A_{\text{wet}} = D_o e^{\frac{-E_A}{kT}} = 9.70 \times 10^7 e^{\frac{-2.05*1.602\times10^{-19}}{1.38\times10^{-23}(1050^\circ C+273)}} = 1.50\mu\text{m/hr}$$
$$B_{\text{wet}} = D_o e^{\frac{-E_A}{kT}} = 386 e^{\frac{-0.78*1.602\times10^{-19}}{1.38\times10^{-23}(1050^\circ C+273)}} = 0.411\,\mu\text{m}^2/\text{hr}$$

This time we do have an initial oxidation time τ because of the dry oxidation we did in the previous step. Here X_i is the oxide length we calculated for the dry oxidation growth,

$$\tau = \frac{{X_i}^2}{B_{\text{wet}}} + \frac{X_i}{B/A_{\text{wet}}} = \frac{0.00711^2}{0.411} + \frac{0.00711}{1.50} \approx 0.00488\text{hrs}$$

And finally our oxide growth is,

$$X_{ox} = \frac{0.5B}{B/A}\Big[\sqrt{1+\frac{4}{B}(\frac{B}{A})^2(t+\tau)} - 1\Big] = \frac{0.5(0.411)}{1.50}\Big[\sqrt{1+\frac{4}{0.411}(1.50)^2(\frac{(12+25)\text{min}}{60\text{min/hr}}+0.00488\text{hrs})} - 1\Big] \approx 386.3\,\text{nm}$$

6.2 Junction Depth Calculations

Junction depth calculation for box approximation (limited-source diffusion):

$$x_j = 2\sqrt{Dt\ln(N_o/N_B)} \tag{3}$$

and for a half gaussian (constant-source diffusion):

$$x_j = 2\sqrt{Dt}\,\text{erfc}^{-1}(N_B/N_o) \tag{4}$$

where,

$$D = D_o e\frac{-E_A}{kT}\ \text{(Diffusion coefficient)}$$
$$t = \text{time of diffusion}$$
$$N_B = \text{Background impurity concentration}$$
$$N_o = \text{Surface concentration limited by solid solubility}$$

Example: Calculate the junction depth after pre-diffusion and drive in.
According to the process flow [5], our silicon wafer has a resistivity of about 14-16 ohm-cm. From the same process flow we know that we had a phosphorus doped, solid solubility limited constant diffusion at 1050°C. Using figure 4.6 [1] we see that at a temperature of 1050°C our phosphorus surface concentration $N_o \approx 10^{21}/\text{cm}^3$. Now using the Resistivity of our wafer and figure 4.8 [1], we see that we have an impurity concentration $N_B \approx 8 \times 10^{14}/\text{cm}^3$.

Using table 4.1 [1], we can calculate our diffusion coefficient. Note that pre-diffusion was done at 1050°C for 5 minutes.

$$D = D_o e\frac{-E_A}{kT} = 10.5\,\text{cm}^2/\text{sec}\ \exp\left(\frac{-3.69*1.602\times10^{-19}}{1.38\times10^{-23}(1050+273)}\right) = 9.11\times10^{-14}\,\text{cm}^2/\text{sec}$$

Now we can plug everything into our solid solubility limited box approximation equation:

$$x_j = 2\sqrt{Dt}\,\text{erfc}^{-1}\left(N_B/N_o\right) = 2\sqrt{(9.11\times10^{-14})(300\text{sec})}\,\text{erfc}^{-1}\left(8\times10^{14}/10^{21}\right) \approx 365\,\text{nm}$$

Now for drive-in we kept the temperature the same, 1050°C, but kept the wafer inside the furnace for 37 minutes (2220 seconds). Also we can no longer assume a simple box approximation, we must use a half gaussian; this means that our surface concentration is going to change with drive-in.

We will use the following equation,

$$N_B = (Q/\sqrt{\pi D_2 t_2})\exp\left(-(\frac{x_j}{2\sqrt{D_2 t_2}})^2\right) \tag{5}$$

where Q is the does rate,

$$Q = 2N_o\sqrt{D_1 t_1/\pi} \tag{6}$$

Combining the two equations and noting that $D_1 = D_2$ because we are using the same temperature, 1050°C, for both pre-diffusion and drive-in (t_1 is the pre-diffusion time and t_2 is the drive in time),

$$N_B = (2N_o/\pi)\sqrt{\frac{t_1}{t_2}}\exp\left(-(\frac{x_j}{2\sqrt{D_2 t_2}})^2\right)$$

Solving this for x_j yields,

$$x_j = 2\sqrt{D_2 t_2 \ln\left((2N_o/\pi N_B)(\sqrt{t_1/t_2})\right)} = 2\sqrt{(9.11\times10^{-14})(2220)\ln\left((2(10^{21})/\pi(8\times10^{14}))(\sqrt{300/2220})\right)} \approx 1000\,nm$$

6.3 Dopant Profiles.

According to the EE143 process flow, There was an initial blanket implant of B11 3E12cm^{-3} on our $<100>$ wafer. Also our wafer had a resistivity of 14-16cm which corresponds to a background concentration of about 8E14cm^{-3}. Now for the field oxide, we used 5-80-5 minute dry,wet,dry oxidation to create about 500 nm of oxide. Putting all this information into Tsuprem-4 generates the plot in Figure 35.

Script file:

```
$ field oxide

$ Initialization
Initialize <100> material=silicon Phosphorus=8e14 width=1.5 dX=0.005

$ Blanket implant here
Implant B11 Energy=60 Dose=3e12

$ Plot here for initial dopant profile before any oxidation

$ 5-80-5 oxidation
Diffusion Time=5 Temperature=1000 DryO2
Diffusion Time=80 CONTINUE Temperature=1000 WetO2
Diffusion Time=5 CONTINUE Temperature=1000 DryO2

$ Plot here for dopant profile after field oxide

ETCH       OXIDE        TRAP

Diffusion Time= 35 Temperature= 1100 T.Rate=+5.714 Nitrogen
Diffusion Time=45 CONTINUE Temperature=1100 DryO2

$ Plot here for dopant profile after gate oxide

DEPOSIT   POLYSILICON  THICK=0.4

$ Plot here for dopant profile after poly deposition
```

```
ETCH POLY TRAP
ETCH  OXIDE TRAP

$PSG
Deposit Oxide Thickness = .320

Diffusion Time=5 CONTINUE Temperature=1050 Boron=5e22

$ Plot here for dopant profile after pre deposition

$ plotting
Select z=log10(active(boron))
Plot.1d
Print.1d
```

- Gate Oxide

7 References

1. Jaeger, Richard. *Introduction to microelectronic fabrication.* New Jersey: Prentice Hall, 2002. Print.

2. Sharpe, William N., Bin Yuan, and Ranji Vaidyanathan. Measurements of Young's Modulus, Poisson's ratio, and Tensile Strength of Polysilicon. Publication no. 1. Nagoya: IEEE, 1997. Web.

3. Kim, Min. "Influence of Substrates on the Elastic Reaction of Films for the Microindentation Tests." Thin Solid Films 283 (1996): 15. Web.

4. Chinmulgund, M. "Effect of Ar Gas Pressure on Growth, Structure, and Mechanical Properties of Sputtered Ti, Al, TiAl, and Ti3Al Films." Thin Solid Films 270.1-2 (1995): 260-63. Web.