Test Infor	mation			
Description	CSSE2010/7201 - Introduction to Computer Systems - Final Exam - Semester One 2020.  Materials permitted: anything on paper, any calculator without communication capability, access to course Blackboard site.  You may use the <b>last question</b> to specify any assumptions that you have made for those questions that don't allow free text entry.			
Instructions	Answer all questions. Questions are worth the number of marks indicated. There are 100 marks for the whole exam.  If you experience any technical difficulties during the exam, talk to your online invigilator via the webcam or chat functions. If the technical trouble cannot be resolved, you should ask for an email (or transcript of the chat) documenting any technical advice provided to support your request for a deferred exam.			
Timed Test	This test has a time limit of 2 hours and 30 minutes. This test will save and submit automatically when the time expires.  Warnings appear when <b>half the time</b> , <b>5 minutes</b> , <b>1 minute</b> , and <b>30 seconds</b> remain. [The timer does not appear when previewing this test]			
Multiple Attempts	Not allowed. This test can only be taken once.			
Force Completion	This test can be saved and resumed at any point until time has expired. The timer will continue to run if you leave the test.			

QUESTION 1	2 points	Save Answer
Consider the binary unsigned number 1011011011.		
What is the decimal value of this number?		
What is the octal representation of this number?		

	4 points	Save Answer
Consider the decimal number -115. Enter the binary representation of this number in the following formats. (Fand 1's only for these answers.)	Enter 0's	
9-bit two's complement:		
8-bit ones' complement:		
9-bit signed magnitude:		
8-bit excess-117:		
OHESTION 2		
QUESTION 3	4 points	Save Answer
format follows the same principles as IEEE floating point r (a) Enter the 16-bit binary pattern corresponding to the sr positive (non-zero) normalised number:  (b) Enter the 16-bit binary pattern corresponding to the la positive normalised number:  Consider the floating point number -17.625.  (c) Enter the 8-bit binary pattern that would represent the in the bfloat16 representation of this number:	nallest rgest	
(d) What is the bfloat16 representation of -17.625? Enter y in hexadecimal:	our answer	
OHESTION 4	4 mainte	
QUESTION 4	1 points	Save Answer
	estion also.]	

1 points

Save Answer

Consider the 8-bit two's complement binary numbers 10111011 and 11000110. (Same numbers as the previous question.)

What would be the values (0 or 1) of the V (overflow), C (carry), N (negative) and Z (zero) flags after the addition of these two numbers?

V:

C:

N:

Z:

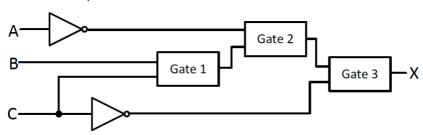
# **QUESTION 6**

1 points

Save Answer

Consider the equation  $X = (\overline{A} + B.C) \oplus \overline{C}$ .

What gates must Gate 1, Gate 2 and Gate 3 be in the following figure in order to implement this function?



Enter one of AND, OR, XOR, NAND, NOR, XNOR for each of the following:

Gate 1:

Gate 2:

Gate 3:

For the equation  $X = (\overline{A} + B.C) \oplus \overline{C}$  (same as in the previous

question), determine the truth table. Each entry in the truth table must be either 0 or 1.

		С	X
0	0	0	
Ш	0	Ш	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

**QUESTION 8** 

1 points

Save Answer

Consider the equation  $X = (\overline{A} + B.C) \oplus \overline{C}$  (same as the previous

question). Which of the following is NOT an equivalent expression for X?

$$\bigcirc$$
 a.  $\overline{A}$ .  $\overline{C}$  +  $A$ .  $\overline{B}$ .  $C$ 

$$\bigcirc$$
 b.  $(A \oplus C) + AB$ 

$$\bigcirc$$
 c.  $(A \oplus C) + BC$ 

$$\bigcirc$$
 d.  $\overline{A}$ .  $C + B$ .  $C + A$ .  $B$ 

$$\bigcirc$$
 e.  $\triangle B \cdot \overline{B} \cdot \overline{C} + (\triangle \oplus C) + B \cdot C$ 

Consider the equation  $X = (\overline{A} + B \cdot C) \oplus \overline{C}$  (same as the previous

question). Which of the following is an equivalent sum of products expression for X?

$$\bigcirc$$
 a.  $\overline{A}$ .  $C + B$ .  $C + A$ .  $B$ 

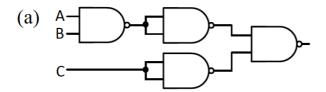
$$\bigcirc$$
 b.  $\overline{A}$ .  $\overline{B}$ .  $C + \overline{A}$ .  $B$ .  $C + A$ .  $B$ .  $\overline{C} + A$ .  $B$ .  $C$ 

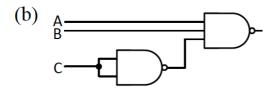
$$\bigcirc$$
 c.  $A.\overline{B.C}.\overline{C}+\overline{A}.C+B.C$ 

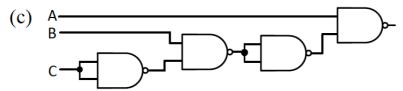
$$\bigcirc$$
 d.  $A.\overline{C} + \overline{A}.C + B.C$ 

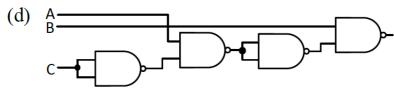
$$\bigcirc$$
 e.  $(A \oplus C) + A.B.C$ 

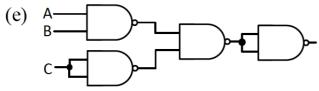
Which of the <u>following</u> circuits is NOT a NAND only implementation of the equation  $\overrightarrow{AB} + C$ ?





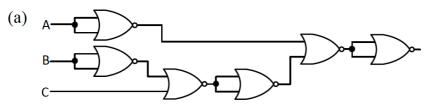


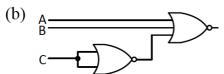


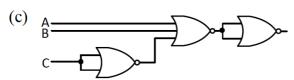


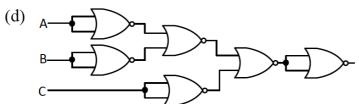
- O a. Circuit (a)
- Ob. Circuit (b)
- Oc. Circuit (c)
- Od. Circuit (d)
- O e. Circuit (e)

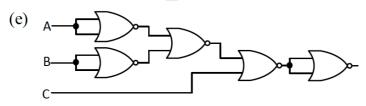
<u>Whi</u>ch of the following circuits is a NOR only representation of  $\overline{AB} + C$ ?











- O a. Circuit (a)
- O b. Circuit (b)
- O c. Circuit (c)
- Od. Circuit (d)
- O e. Circuit (e)

Consider a 3-bit synchronous counter that counts through the sequence

 $Q_2Q_1Q_0$ : 000 -> 001 -> 011 -> 010 -> 110 -> 111 -> 101 -> 100 -> 000 ...

(i) Copy the following truth table template to the answer area and fill it in. (2 marks)

(ii) Write equations for D2, D1 and D0. (You can use the equation editor OR write plain text using operations +, ., NOT, XOR etc. You can write the variables without subscripts, e.g. use Q2,Q1,Q0,D2,D1,D0 rather than  $Q_2,Q_1,Q_0,D_2,D_1,D_0$ .) (3 marks)

#### Answer template:

Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

D2 =

D1 =

D0 =

# **QUESTION 13**

5 points

Save Answer

Consider a sequence detector that has one input (A) and two outputs (X and Y).

The output X is 1 if and only if A = 1 for one clock cycle.

The output Y is 1 if and only if A = 0 for two clock cycles in a row.

Use the text area below to create a state table (either 1D or 2D) that represents this state machine. You may use one of the following two templates if you wish - copy and paste the table into the answer area. Add additional rows as required by right clicking on the table.

# 1D state table

Current State	 Next State	Output X	Output Y

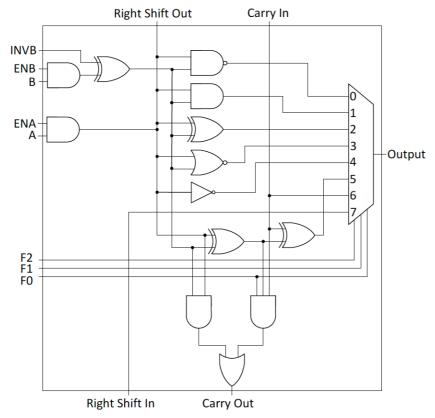
#### 2D state table

Current	Next State	Next State	Output	Output
State	if A=0	if A = 1	X	Y

Save Answer

Consider the ALU bit slice shown below. Assume 8 of these ALU bit slices put together to form an 8-bit ALU (i.e. with 8-bit data inputs A and B).

(The "carry in" control input applies only to the least significant bit, the "carry in" input of other bit slices comes from the "carry out" output of its neighbouring bit slice. The "right shift in" control input applies only to the most significant bit; the "right shift in" input of other bit slices comes from the "right shift out" output of its neighbouring bit slice. Note that for the output multiplexer on the right hand side, F2 is the most significant of the select bits, so for example, if F2,F1,F0 =0,0,1 then input 1 of the multiplexer will be selected.)



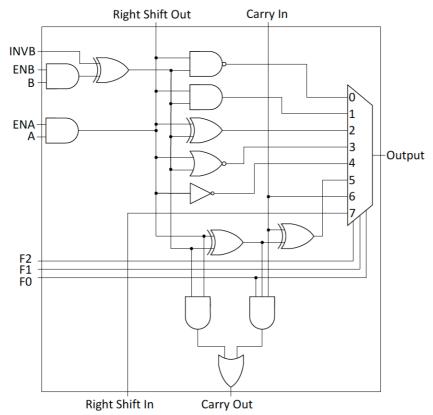
Determine the values of the control inputs for the ALU to perform the function listed below. Choose 0 or 1 or X (don't care) for ENA, ENB, INVB, Carry In and Right Shift In. Choose a number from 0 to 7 for the function input. If there is more than one way to generate the given function, just show one way.

Function: $\overline{A} \oplus \overline{B}$	
ENA (0, 1 or X):	
ENB (0, 1 or X):	
INVB (0, 1 or X):	
Carry In (0, 1 or X):	
Right Shift In (0, 1 or X):	
FUNCTION (0 to 7):	

Save Answer

Consider the ALU bit slice shown below - **the same as in previous question**. Assume 8 of these ALU bit slices put together to form an 8-bit ALU (i.e. with 8-bit data inputs A and B).

(The "carry in" control input applies only to the least significant bit, the "carry in" input of other bit slices comes from the "carry out" output of its neighbouring bit slice. The "right shift in" control input applies only to the most significant bit; the "right shift in" input of other bit slices comes from the "right shift out" output of its neighbouring bit slice. Note that for the output multiplexer on the right hand side, F2 is the most significant of the select bits, so for example, if F2,F1,F0 =0,0,1 then input 1 of the multiplexer will be selected.)



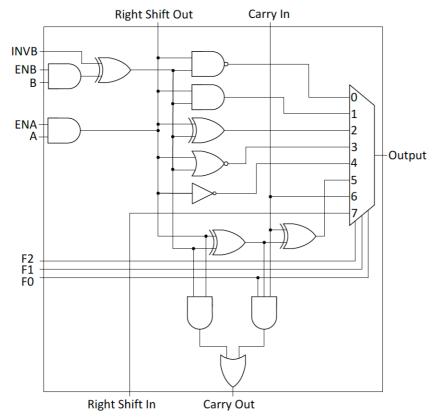
Determine the values of the control inputs for the ALU to perform the function listed below. Choose 0 or 1 or X (don't care) for ENA, ENB, INVB, Carry In and Right Shift In. Choose a number from 0 to 7 for the function input. If there is more than one way to generate the given function, just show one way.

Function: $\overline{A}$ . $B$	
ENA (0, 1 or X):	
ENB (0, 1 or X):	
INVB (0, 1 or X):	
Carry ln (0, 1 or X):	
Right Shift In (0, 1 or X):	
FUNCTION (0 to 7):	

Save Answer

Consider the ALU bit slice shown below - **the same as in previous question**. Assume 8 of these ALU bit slices put together to form an 8-bit ALU (i.e. with 8-bit data inputs A and B).

(The "carry in" control input applies only to the least significant bit, the "carry in" input of other bit slices comes from the "carry out" output of its neighbouring bit slice. The "right shift in" control input applies only to the most significant bit; the "right shift in" input of other bit slices comes from the "right shift out" output of its neighbouring bit slice. Note that for the output multiplexer on the right hand side, F2 is the most significant of the select bits, so for example, if F2,F1,F0 =0,0,1 then input 1 of the multiplexer will be selected.)

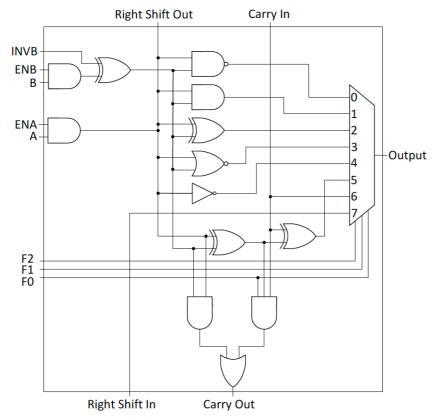


Determine the values of the control inputs for the ALU to perform the function listed below. Choose 0 or 1 or X (don't care) for ENA, ENB, INVB, Carry In and Right Shift In. Choose a number from 0 to 7 for the function input. If there is more than one way to generate the given function, just show one way.

Function: Logical Shift Left of A
ENA (0, 1 or X):
ENB (0, 1 or X):
INVB (0, 1 or X):
Carry In (0, 1 or X):
Right Shift In (0, 1 or X):
FUNCTION (0 to 7):

Consider the ALU bit slice shown below - **the same as in previous question**. Assume 8 of these ALU bit slices put together to form an 8-bit ALU (i.e. with 8-bit data inputs A and B).

(The "carry in" control input applies only to the least significant bit, the "carry in" input of other bit slices comes from the "carry out" output of its neighbouring bit slice. The "right shift in" control input applies only to the most significant bit; the "right shift in" input of other bit slices comes from the "right shift out" output of its neighbouring bit slice. Note that for the output multiplexer on the right hand side, F2 is the most significant of the select bits, so for example, if F2,F1,F0 =0,0,1 then input 1 of the multiplexer will be selected.)



For each of the following <u>outputs</u>, how many of the 8 functions could be used to generate that output? Enter a number between 0 and 8 inclusive for each answer.

Α:	
В:	
Ā:	
B:	

2 points

Save Answer

Consider a 16-bit two's complement binary number stored in AVR registers r7:r8. (r7 holds the most significant byte, r8 holds the least significant.) Write down a sequence of AVR assembly language instructions that subtracts 8 from that number, with the result ending up in r7:r8. Other registers can be used freely if required.

# **QUESTION 19**

2.5 points

Save Answer

Consider a 16-bit two's complement binary number stored in AVR registers r7:r8. (r7 holds the most significant byte, r8 holds the least significant.) Write down a sequence of AVR assembly language instructions that divide that number by 4, with the result ending up in r7:r8. Other registers can be used freely if required.

### **QUESTION 20**

3 points

Save Answer

Consider a 24-bit two's complement binary number stored in AVR registers r6:r7:r8. (r6 holds the most significant byte, r8 holds the least significant.) Write down a sequence of AVR assembly language instructions that multiplies that number by 512, with the result ending up in r6:r7:r8. Other registers can be used freely if required.

10 points

Save Answer

This question applies to the AVR ATmega324A microcontroller. What will be the binary value in register r28 after the execution of the nominated instructions (i) to (x) in the sequence of instructions below. Note that the instructions are not independent – registers and RAM maintain their values from one instruction to the next. You may assume that the stack pointer has been appropriately initialised. **Each answer must be given as an 8-bit binary number**. Answers that are not 8-bit binary numbers will be marked as incorrect. Each answer will be marked correct only if all 8-bits are correct.

	clr r28 push r28		
(i)	ldi r28, 0x3B	r28:	
	push r28		
(ii)	com r28	r28:	
(iii)	ldi r28, 037	r28:	
(iv)	ldi r28, -3	r28:	
	push r28		
(v)	neg r28	r28:	
	ldi YL, 0x35		
(vi)	ldi YH, 0x02	r28:	
(vii)	adiw YH:YL,3	r28:	
(viii)	lsl r28	r28:	
	pop r27		
(ix)	st Y+,r0	r28:	
	ldi r28, 0x45		
(x)	eor r28,r27	r28:	

**QUESTION 22** 

1 points

Save Answer

For the following C statement(s) for the Atmel AVR ATmega324A, write down the assembly language equivalent. (You may assume that definitions in the m324Adef.inc file are available. Several instructions may be required.)

OCR2B = 50;

1 points

Save Answer

For the following C statement(s) for the Atmel AVR ATmega324A, write down the assembly language equivalent. (You may assume that definitions in the m324Adef.inc file are available. Several instructions may be required.)

PORTD = TCNT2;

### **QUESTION 24**

2 points

Save Answer

For the following C statement(s) for the Atmel AVR ATmega324A, write down the assembly language equivalent. (You may assume that definitions in the m324Adef.inc file are available. Several instructions may be required.)

OCR1A = 9999;

# **QUESTION 25**

2 points

Save Answer

For the following C statement(s) for the Atmel AVR ATmega324A, write down the assembly language equivalent. (You may assume that definitions in the m324Adef.inc file are available. Several instructions may be required.)

TCCR1B = (0b010) | (1 << WGM13);

### **QUESTION 26**

2 points

Save Answer

For the following C statement(s) for the Atmel AVR ATmega324A, write down the assembly language equivalent. (You may assume that definitions in the m324Adef.inc file are available. Several instructions may be required.)

UBRR1 = UBRR0 / 2;

#### **QUESTION 27**

2 points

Save Answer

For the following C statement(s) for the Atmel AVR ATmega324A, write down the assembly language equivalent. (You may assume that definitions in the m324Adef.inc file are available. Several instructions may be required.)

```
DDRB |= 0b00100111;

PORTB = UDR0 & 0b00100111;

PORTC = PINB & 0b11011000;
```

2 points

Save Answer

For the following C statement(s) for the Atmel AVR ATmega324A, write down the assembly language equivalent. (You may assume that definitions in the m324Adef.inc file are available. Several instructions may be required.)

```
while(!(UCSR1A & (1<<UDRE1))) {
   ;
}
UDR1 = ADCL & 0x7F;</pre>
```

# **QUESTION 29**

5 points

Save Answer

Consult the AVR Atmega324A datasheet and for an ATmega324A clocked at 8MHz, determine what values (in binary) need to go in the following IO registers to configure timer/counter 1 to be clocked at 1MHz and cause port D pin 5 to toggle every 2 milliseconds and generate an interrupt at that time also. No other actions should be configured.

Enter each result as an 8-bit binary number with only 0's and 1's and no spaces. If a bit value can be 0 or 1 then enter either. An answer should be entered for all registers.

TCCR1A:	
TCCR1B:	
TCCR1C:	
OCR1AH:	
OCR1AL:	
OCR1BH:	
OCR1BL:	
TIMSK1:	

6 points

Save Answer

Write an AVR assembly language interrupt handler for the ATmega324A that will be called when an output compare match happens for timer/counter 2. If at that time the timer/counter value for timer/counter 0 is less then 100 then the interrupt handler should output 65 (the ASCII code for 'A') to the port C pins, otherwise it should output 66 (the ASCII code for 'B'). The timer/counter 0 value must then be reset to 0.

You can assume that the port C pins have been previously configured as output and that both timer/counter 0 and timer/counter 2 have been appropriately configured.

Your interrupt handler must preserve the values of all generalpurpose registers and the status register (i.e. these register values must be restored to their original values if they are changed by the handler).

#### **QUESTION 31**

4 points

Save Answer

For the Atmel ATmega324A, write a C function that reads a 4-bit unsigned number from the lower 4-bits of the port D pins, and sets the output compare register B for timer/counter 1 to 20 times this value. The function returns the value that was in this IO register prior to this new value being set.

QUESTION 32 8 points

Save Answer

Consider the following AVR ATmega324A assembly language module and answer the questions below.

```
.include "m324Adef.inc"
.equ INT32SIZE = 4
.dseg
clockTicks: .BYTE INT32SIZE
.cseq
init timer0:
   clr r1
   sts clockTicks, r1
   sts clockTicks + 1, r1
   sts clockTicks + 2, r1
   sts clockTicks + 3, r1
   out TCNT0, r1
   ldi r24, 0x7C
   out OCROA, r24
   ldi r24, 0x02
   out TCCR0A, r24
   ldi r24, 0x03
   out TCCR0B, r24
   ldi r30, TIMSKO
   ldi r31, 0
   ld r24, Z
   ori r24, 0x02
   st Z, r24
   sbi TIFRO, OCFOA
   ret
get current time:
   in r18, SREG
   cli
   lds r22, clockTicks
   lds r23, clockTicks+1
   lds r24, clockTicks+2
   lds r24, clockTicks+3
   tst r18
  brge done
   sei
done:
   ret
What is the overall size (in instruction words) of the code segment for
this module?
```

What is the overall size (in bytes) of the data segment for this

The module shown above (which we will now call module B) is linked with two other modules (A and C) with code and data segment sizes as shown in this table:

Module	Code segment size	Data segment size
Α	49	24
С	113	9

module?

If the modules are linked in order A, B, C starting from code segment address 0x3E (62 decimal) and data segment address 0x100 (256

1 points

Save Answer

[The following specification was introduced in the previous question.] The Seagate Exos X16 ST16000NM001G hard drive has the following specifications:

• Nominal Capacity: 16TB (1TB =  $10^{12}$  bytes)

• Sector size: 4096 bytes

• Rotational speed: 7200 RPM

Max Sustained transfer rate: 261MB/s (1MB = 10<sup>6</sup> bytes)

• Edge to edge seek time (approximate): 27.5ms

The hard drive is formatted with a file system that has a block size of 32kB (32,768 bytes) and currently contains 2,500,000 files of various sizes which occupy 150,000,000 data blocks.

What is the average seek time for this hard drive (in milliseconds)?

### **QUESTION 35**

1 points

Save Answer

[The following specification is the same as in the previous 2 questions.]

The Seagate Exos X16 ST16000NM001G hard drive has the following specifications:

- Nominal Capacity: 16TB (1TB =  $10^{12}$  bytes)
- Sector size: 4096 bytes
- Rotational speed: 7200 RPM
- Max Sustained transfer rate: 261MB/s (1MB = 10<sup>6</sup> bytes)
- Edge to edge seek time (approximate): 27.5ms

The hard drive is formatted with a file system that has a block size of 32kB (32,768 bytes) and currently contains 2,500,000 files of various sizes which occupy 150,000,000 data blocks.

How much space within the allocated 150,000,000 blocks is likely to be wasted (i.e. not used for storing data)? Express your answer in MB, where  $1MB = 10^6$  bytes.

1 points

Save Answer

[The following specification was used in the previous questions.] The Seagate Exos X16 ST16000NM001G hard drive has the following specifications:

- Nominal Capacity: 16TB (1TB =  $10^{12}$  bytes)
- Sector size: 4096 bytes
- Rotational speed: 7200 RPM
- Max Sustained transfer rate: 261MB/s (1MB = 10<sup>6</sup> bytes)
- Edge to edge seek time (approximate): 27.5ms

The hard drive is formatted with a file system that has a block size of 32kB (32,768 bytes) and currently contains 2,500,000 files of various sizes which occupy 150,000,000 data blocks.

If the block size were reduced to 16kB, how many data blocks are likely to be used to store the 2,500,000 files?

<b>QUESTION 37</b>
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1 points

Save Answer

[The following specification was used in the previous questions.] The Seagate Exos X16 ST16000NM001G hard drive has the following specifications:

- Nominal Capacity: 16TB (1TB =  $10^{12}$  bytes)
- Sector size: 4096 bytes
- Rotational speed: 7200 RPM
- Max Sustained transfer rate: 261MB/s (1MB = 10<sup>6</sup> bytes)
- Edge to edge seek time (approximate): 27.5ms

The hard drive is formatted with a file system that has a block size of 32kB (32,768 bytes) and currently contains 2,500,000 files of various sizes which occupy 150,000,000 data blocks.

If the file system overhead is 5% of the total disk capacity, how many free blocks are there?

1 points

Save Answer

[The following specification was used in the previous questions.] The Seagate Exos X16 ST16000NM001G hard drive has the following specifications:

- Nominal Capacity: 16TB (1TB =  $10^{12}$  bytes)
- Sector size: 4096 bytes
- Rotational speed: 7200 RPM
- Max Sustained transfer rate: 261MB/s (1MB = 10<sup>6</sup> bytes)
- Edge to edge seek time (approximate): 27.5ms

The hard drive is formatted with a file system that has a block size of 32kB (32,768 bytes) and currently contains 2,500,000 files of various sizes which occupy 150,000,000 data blocks.

The hard disk is connected to a computer via a USB 3.1 interface. If the USB interface is able to operate at <u>up to</u> 50% of the maximum, approximately how long will it take to copy all the files from the disk? (Enter your answer in <u>seconds</u>)

$\sim$ 11	EST		20
w		IC DIM	-59

2 points

Save Answer

Consider a little-endian computer with a memory that has an addressable cell size of one byte that requires natural alignment. The values in memory cells 400 to 408 are shown below:

Address (decimal)	Value (hexadecimal)
400	0x1F
400	UXIF
401	0x2E
402	0x01
403	0x00
404	0x05
405	0x3A
406	0xC5
407	0x5E
408	0x21

What 16-bit <u>decimal</u> value is	stored at address 404, if the	e number is
considered to be unsigned?		

If the decimal value 266 is stored as a 16-bit unsigned integer to address 402, what value (in <a href="https://example.com/hexadecimal">hexadecimal</a>) will be found in address

402?

QUESTION 40	2 points	Save Answer
Consider a CPU clocked at 8MHz (125ns clock period) with a two pipeline with each stage taking one clock cycle to execute. Assurthat one instruction can enter the pipeline on every clock cycle a always passes through the complete pipeline.	ne	
What is the latency of the pipeline? Enter your answer in		
nanoseconds.		
What is the throughput of the pipeline? Enter your answer in MI	PS	
(millions of instructions per second).		
QUESTION 41	0 points	Save Answer