CS3375: Computer Architecture
Spring 2020

Takehome Quiz #4 Solution

- Name only: _____
- Release date: Mar 11th, 2020 (Wednesday)
- Due date: ~~**Mar 23rd, 2020 (Monday) at the beginning of class**~~ → **Extended to Mar 30th, 2020 (Monday) before midnight**
- It should be done INDIVIDUALLY; Show ALL your work; ~~Handwritten~~ → Please type your solution in a word (or pdf) file and submit it through the blackboard.
- Write (i) your FULL name only and (ii) STAPLE if you turn-in multiple papers.
- Total: 10 pts

1. Problem in this exercise assume that logic blocks needed to implement a processor's datapath have the following latencies:

I-Men	Add	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-Left-2
200 ps	70 ps	20 ps	90 ps	90 ps	250 ps	15 ps	10 ps

a. If the only thing we need to do in a processor is fetch consecutive instructions (Figure 4.6, pp. 253), what would the cycle time be?

[2 pts]

- Mem takes longer than the Add unit, so the clock cycle time is equal to the latency of the I-Mem:
- 200 ps

b. Consider a datapath similar to the one in Figure 4.11 (pp. 258), but for a processor that only has one type of instruction: unconditional PC-relative branch. What would the cycle time be for this datapath?

[3 pts]

- The critical path for this instruction is through the instruction memory, Sign-extend and Shift-left-2 to get the off set, Add unit to compute the new PC, and Mux to select that value instead of PC+4. Note that the path through the other Add unit is shorter, because the latency of I-Mem is longer that the latency of the Add unit. We have:
- 200 ps + 15 ps + 10 ps + 70 ps + 20 ps = 315 ps

c. Repeat b, but this time we need to support only conditional PC-relative branches.

[3 pts]

- Conditional branches have the same long-latency path that computes the branch address as unconditional branches do. Additionally, they have a long latency path that goes through Registers, Mux, and ALU to compute the PCSrc condition. The critical path is the longer of the two, and the path through PCSrc is longer for these latencies:
- 200 ps + 90 ps + 20 ps + 90 ps + 20 ps = 420 ps

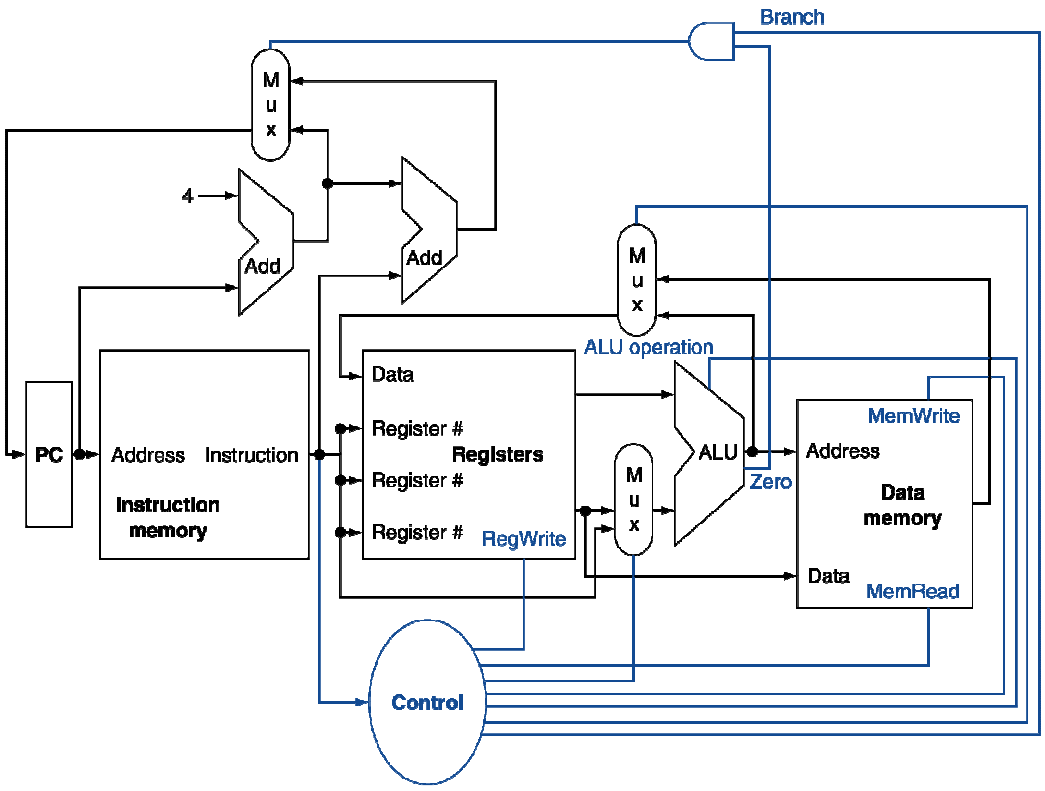
2. The basic single-cycle MIPS implementation in the following figure can only implement some instructions. New instructions can be added to an existing Instruction set Architecture (ISA), but the decision whether or not to do that depends, among other things, on the cost and complexity the proposed addition introduces into the processor datapath and control.

Instruction: `LWI Rt, Rd(Rs)`

Interpretation: `Reg[Rt] = Mem[Reg[Rd] + Reg[Rs]]`

Which existing blocks (if any) can be used for this instruction?

[2 pts]



- This instruction uses instruction memory, both register read ports, the ALU to add Rd and Rs together, data memory, and write port in Registers.