Name ONLY: _____

CS3375: Computer Architecture

Spring 2020

2nd Midterm Exam Solution

(12 problems & 15 total pts)

Apr 6th (Monday), 2020

Show ALL your work,
Open books and notes, and
NO calculator

1. The performance of a machine is determined by instruction count (IC), clock cycles per instruction (CPI), and clock cycle time. Here, [?] is determined by compiler and the instruction set architecture.

[0.5 pts]

- Instruction count (IC)

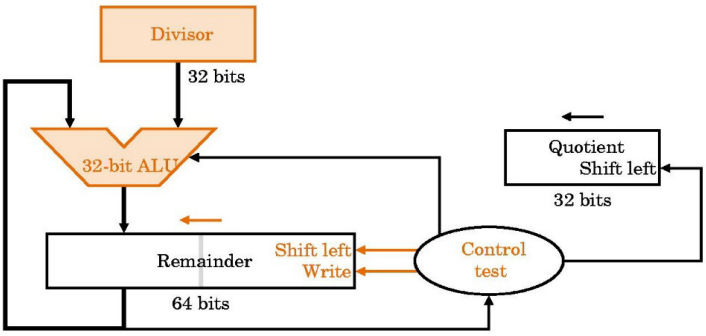
2. In a single cycle data path, every instruction begins on one clock edge and completes execution on the next clock edge. Thus, the CPI is [?].

[0.5 pts]

- CPI = 1

3. Based on the given steps in hardware for division implementation, fill out the blank.

[1 pt]



- Shift the dividend left one position
- Subtract the divisor from the left half of the dividend
- if (result positive)
  - Shift left a 1 into the quotient
- else
  - Shift left a 0 into the quotient
- Once the result is positive,
  - Repeat the process for the partial remainder
- Once the result is negative,
  - [ ]
- Do n iterations, where n is the size of the divisor

- Restore the partial remainder

4. Why do we use a bias for exponent number in the IEEE 754?

[1 pt]

- Avoid using 2's complement that requires an additional hardware

5. The MIPS need exactly five bits to specify the destination register in an R-type instruction? Why?

[1 pt]

- There are 32 registers, 2^5 = 32. Thus, 5 bits are needed to distinguish between 32 registers.

6. The single-cycle datapath must have separate instruction and data memories, because [c]

[1 pt]

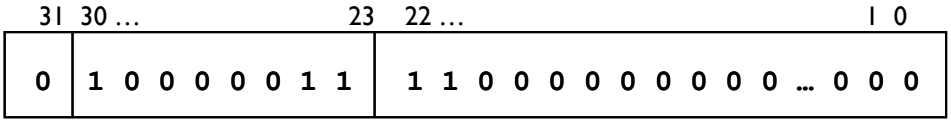
a. the formats of data and instructions are different in MIPS, and hence different memories are needed
b. having separate memories is less expensive
c. the processor operates in one cycle and cannot use a single-ported memory for two different accesses within that cycle

7. Answer the following questions. For your reference, the IEEE 754 uses the following format and the bias for this single precision is 127.

$$(-1)^S \times (1 + \text{Fraction}) \times 2^{(\text{Exponent} - \text{Bias})}$$

What decimal number is represented by the following single precision float form? Show ALL your work.

[2 pts]

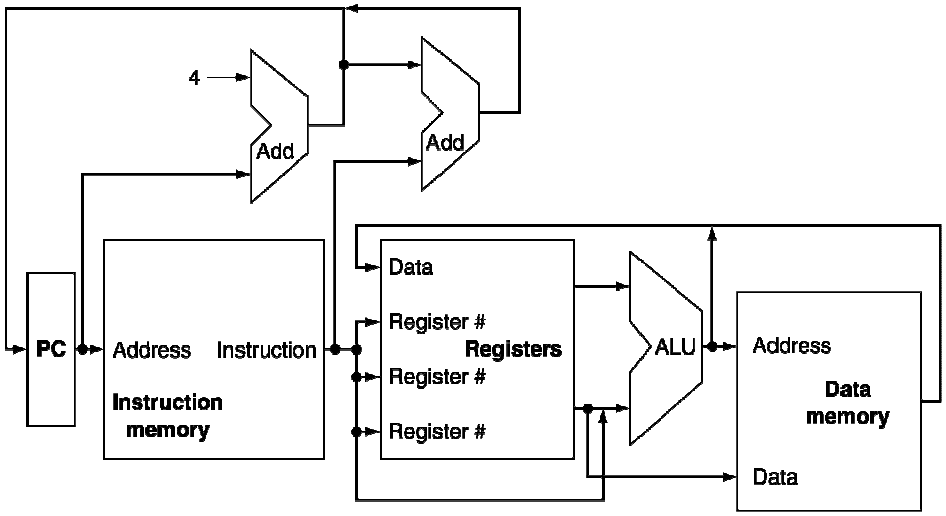


Sign = 0
Exponent = 131
Fraction = $1 \times 2^{-1} + 1 \times 2^{-2} = 0.5 + 0.25 = 0.75$

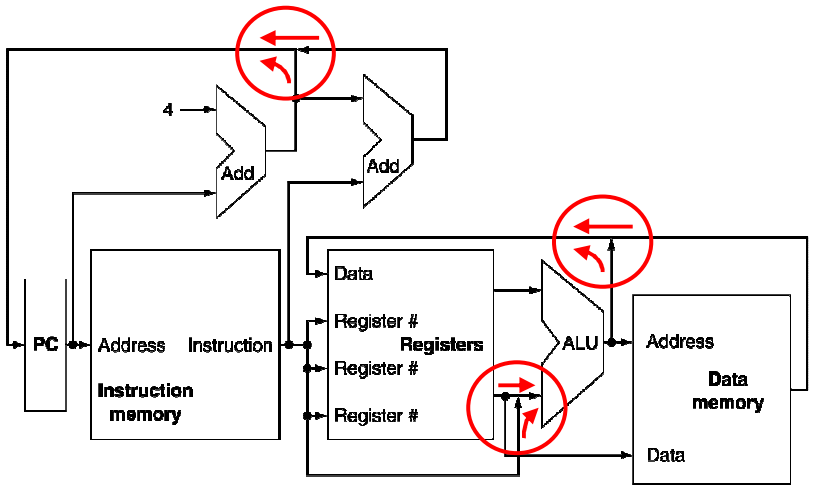
$(-1)^s \times (1 + \text{Fraction}) \times 2^{(\text{exponent} - \text{bias})}$
$= (-1)^0 \times (1. + 0.75) \times 2^{(131 - 127)}$
$= 1.75 \times 2^4 = 28.0$

8. [True/False]: In the following datapath, it needs <u>three</u> 2x1 multiplexors to avoid any conflict.

[1 pt]

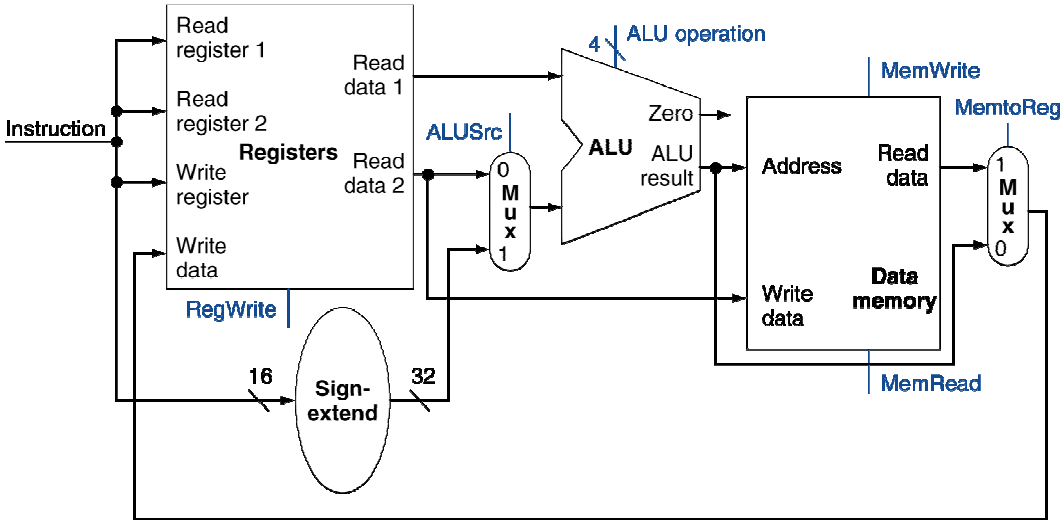


- True



9. Based on the figure below, which of the following is correct for a load instruction? [a]

[1 pt]



a. MemtoReg should be set to cause the data from memory to be sent to the register file.
b. MemtoReg should be set to cause the correct register destination to be sent to the register file
c. We do not care about the setting of MemtoReg for loads

10. Assume that individual stages of the datapath have the following latencies:

[2 pts]

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

a. What is the clock cycle time in a single-cycle processor?

- 1250 ps (= 250 ps + 350 ps + 150 ps + 300 ps + 200 ps)

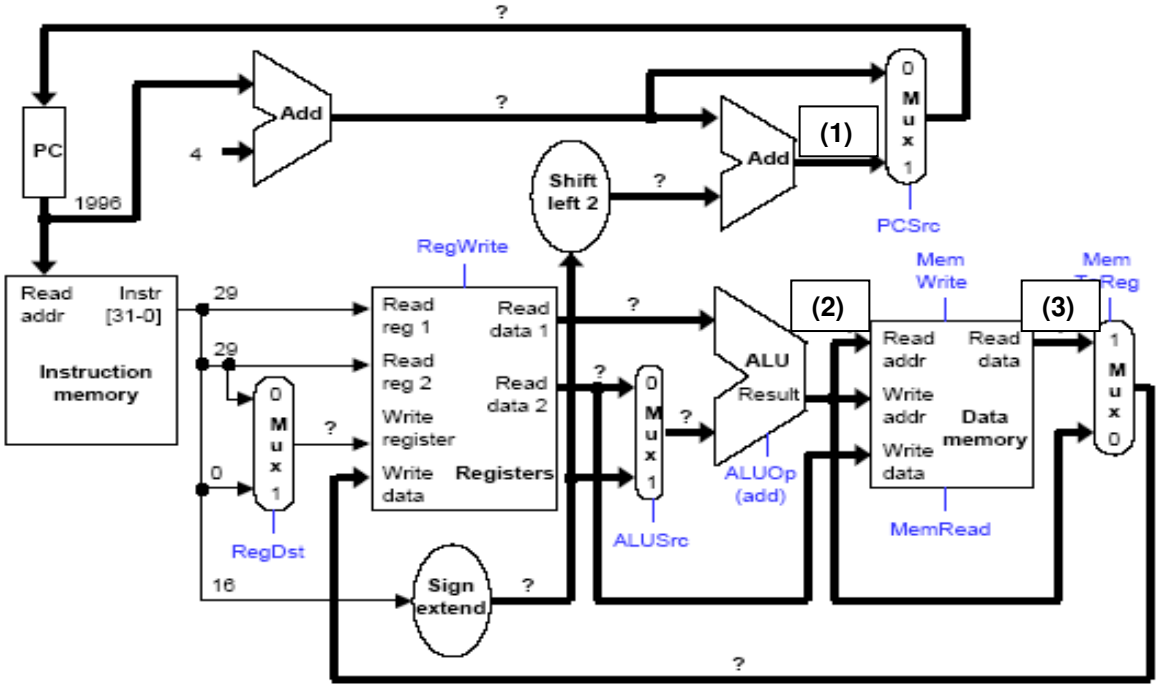
b. What is the total latency of an LW instruction in a single-cycle processor?

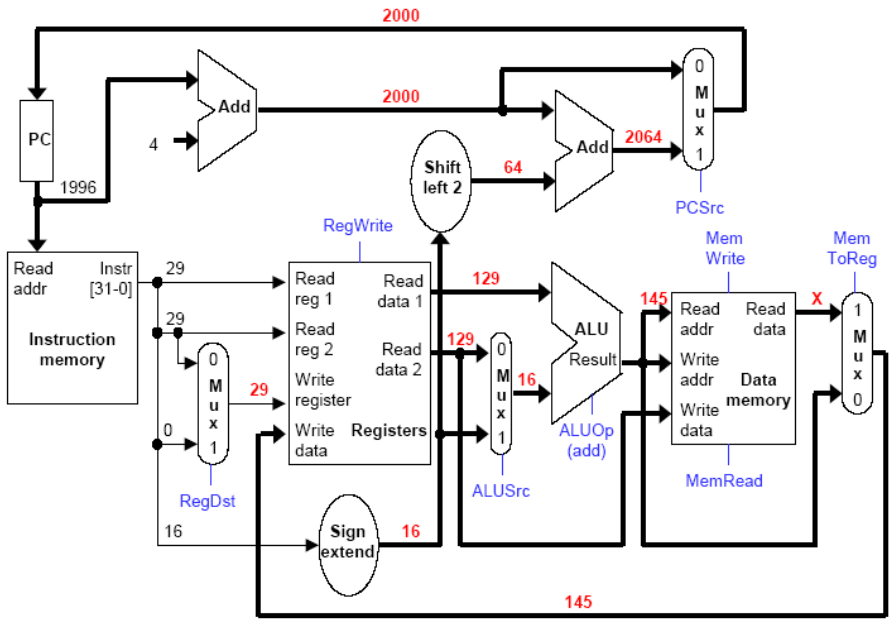
- 1250ps (= 250 ps + 350 ps + 150 ps + 300 ps + 200 ps)

11. Based on the following instruction, what are the values (in decimal) marked as "?" in the single cycle datapath? Suppose $29 initially contains the number 129. If a value cannot be determined, mark it as "x" (don't care).

```
addi $29, $29, 16
```

[2 pts]



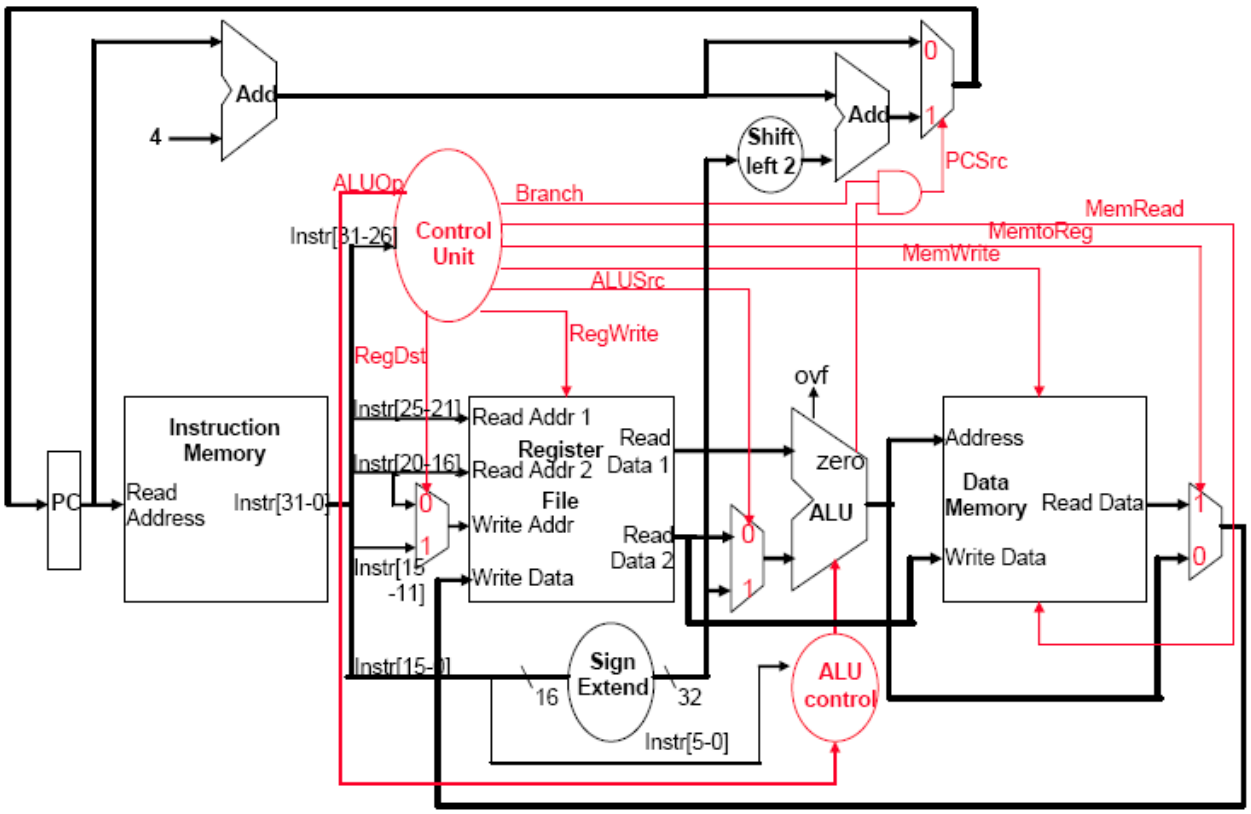


- (1) 2064, (2) 145, and (3) x

12. Based on the following instruction, fill out the control signal table. If a control signal value cannot be determined, mark it as "x" (don't care).

```
beq $t1, $t2, offset
```

[2 pts]



ALUOp1	ALUOp0	MemWrite	Branch	RegWrite	MemRead	RegDst	MemtoReg	ALUSrc
0	1	0	1	0	0	X	X	0