CS3375: Computer Architecture
Spring 2020

Review #7 Solution

- Full name only: _____
- Release date: Apr 10th, 2020 (Friday)
- Due date: **Apr 10th, 2020 (Friday) before midnight**
- Total 5 points

1. Assume that individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

Also, assume that instructions executed by the processor are broken down as follows:

alu	beq	lw	sw
45%	20%	20%	15%

[5 pts]

a. What is the clock cycle time in a pipelined and non-pipelined (single-cycle) processor?

- Pipelined: 350ps
- Non-pipelined: 1250ps

b. What is the total latency of an LW instruction in a pipelined and non-pipelined (single-cycle) processor?

- Pipelined: 1750ps
- Non-pipelined: 1250ps

c. If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?

- ID and 300ps

d. Assuming there are no stalls or hazards, what is the utilization of the data memory?

- 35%

e. Assuming there are no stalls or hazards, what is the utilization of the write-register port of the "Registers" unit?

- 65%