CS3375: Computer Architecture
Spring 2020

Review #9 Solution

- Full name only: _____
- Release date: Apr 29th, 2020 (Wednesday)
- Total 5 points

1. To take advantage of [spatial or temporal] locality, a cache must have a block size larger than one word. The use of a larger block [increases or decreases] the miss rate and improves the efficiency of the cache by reducing the amount of tag storage relative to the amount of data storage in the cache.

[1 pt]

- spatial; decreases

2. A larger block size can [increase or decrease] the miss penalty. If the miss penalty increases linearly with the block size, larger block could easily lead to [higher or lower] performance.

[1 pt]

- increase
- lower

3. To avoid performance loss, the bandwidth of main memory is increased to transfer cache blocks more efficiently. Common methods for increasing bandwidth external to the DRAM are making the memory (i) [ ] and (ii) [ ].

[2 pts]

- wider; interleaving

4. The speed of the memory system affects the designer's decision on the size of the cache block. Which of the following cache designer guidelines are generally valid? [ ]

[1 pt]

a. The shorter the memory latency, the smaller the cache block.

b. The shorter the memory latency, the larger the cache block.

c. The higher the memory bandwidth, the smaller the cache block.

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