Modern Digital System Design

ECE 2372

Final Exam

Texas Tech University

ECE Department

Dr. Tooraj Nikoubin

Fall 12/13/2017

First Name: ……

Last Name: …….

R#: ……

Section # 2

« 1 » A sequential detector circuit has one input (X) and one output (Z) for detection of both **000 & 111** sequences.

a. Draw the state diagram for the circuit
b. Draw the state table for the circuit
c. Find the minimum number of states
d. Design the circuit with JK-FF (Draw the circuit)
e. Design the circuit with T-FF

« 2 » Design a Count-up Counter in Aiken code with following flip flops:

a) D-FF (Active edge is high to low)
b) SR-FF (Active edge is high to low)
c) Use of output of circuit in part (b) and minimum number of logic gates for getting the Count-down counter in Aiken code

« 3 » Design a **closed loop** Counter for following sequence with JK-FFs.

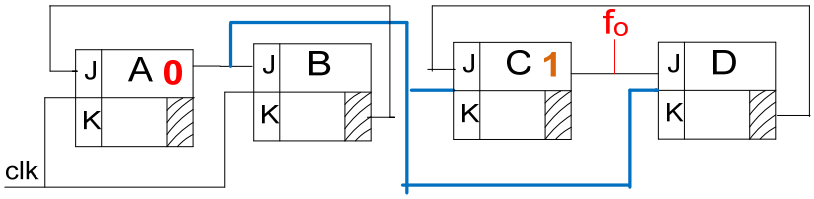
(0 →1→1→2→2→3→3→4→4→5→5→6→6→7→7→0)

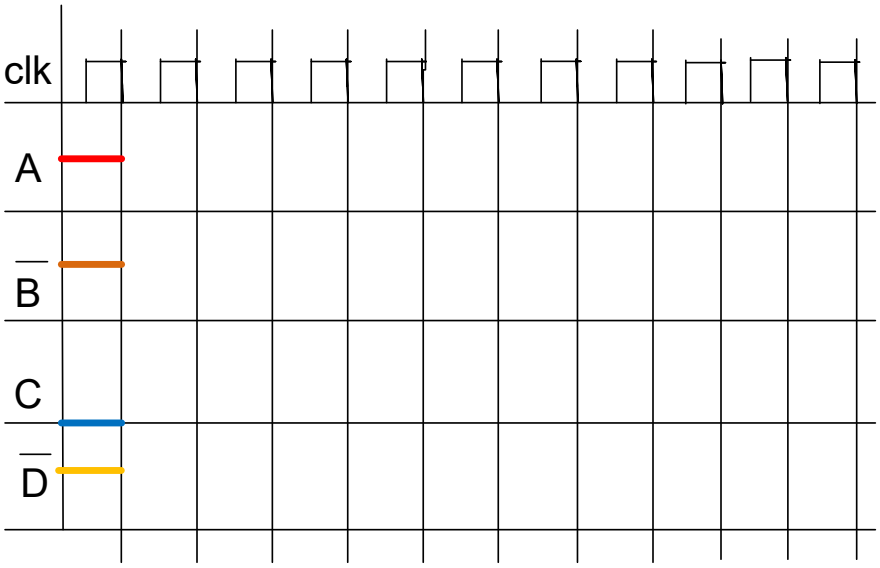
« 4 »

a. Complete the following timing diagram for the following circuit. The circuit works with falling edge. All of flip flops are JK-MS-FF.

b. What is the ratio of frequency divider?

c. By use of timing diagram specify the count routine of the circuit.
(Consider the main out-pout of each flip flop)





« **5** » For following circuit A and B are two binary numbers, (B= 1100b and A=0110b),

a. How many CLK pulse can pass to buffer when the input LOAD goes to be high for one period of CLK.

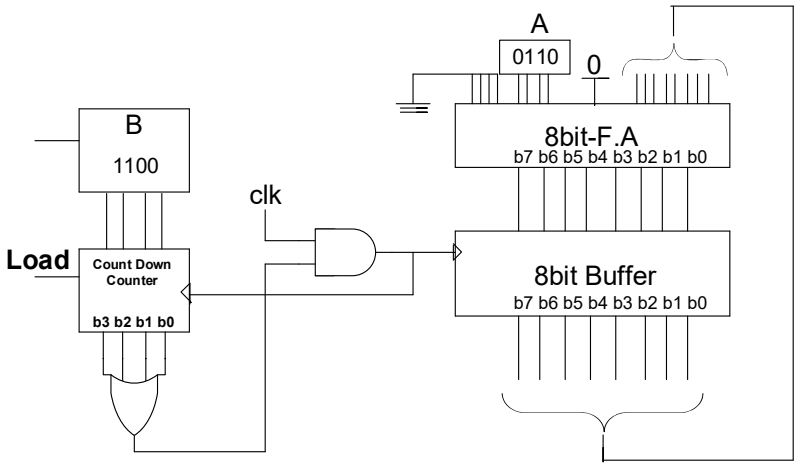
……

b. If the initial state of the 8-bit buffer is **<u>zero</u>**, specify the final value in the buffer, when the operation ended.

……

c. If the initial state of the 8-bit buffer is **<u>00001010b</u>**, specify the final value in the buffer, when the operation ended.

……



d. Complete the following table for above circuit If the initial state of the 8-bit buffer is zero

	Output of 8-bit Adder								Output of 8-bit Buffer								Output of counter			
	b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**	**b3**	**b2**	**b1**	**b0**
Initial Value	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0
After 1 CLK																				
After 2 CLK																				
After 3 CLK																				
After 4 CLK																				
After 5 CLK																				
After 6 CLK																				
After 7 CLK																				
After 8 CLK																				
After 9 CLK																				

e. Design a divider circuit for A÷B which both A & B are 4bit binary numbers.

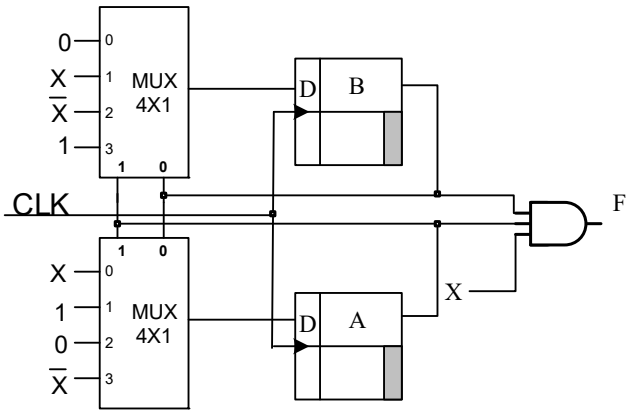
« 6 »

a) Are following tables Mealy or Moore machine?
b) Reduce the following table to a minimum number of states,
c) Draw the state graph of the machine after simplification
d) Design the machine with D-FF

	$X=0$	1	0	1
a	b	c	1	0
b	e	d	1	0
c	g	d	1	1
d	e	b	1	0
e	f	g	1	0
f	h	b	1	1
g	h	i	0	1
h	g	i	0	1
i	a	a	0	1

« 7 » Consider following sequential Circuit as machine state, (A is MSB & B is LSB)

a) Is this machine Mealy or Moore?
b) Draw the state table for this machine state
c) Draw the state diagram of this machine state



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Modern Digital System Design

ECE 2372

Final Exam

Texas Tech University

ECE Department

Dr. Tooraj Nikoubin

Fall 12/08/2017

First Name: ……

Last Name: …….

R#: ……

Section # 3

« 1 » A sequential detector circuit has one input (X) and one output (Z) for detection of both **110 & 011** sequences.

a. Draw the state diagram for the circuit
b. Draw the state table for the circuit
c. Find the minimum number of states
d. Design the circuit with RS-FF (Draw the circuit)
e. Design the circuit with T-FF

« 2 » Design a Count-up Counter in Aiken code with following flip flops:

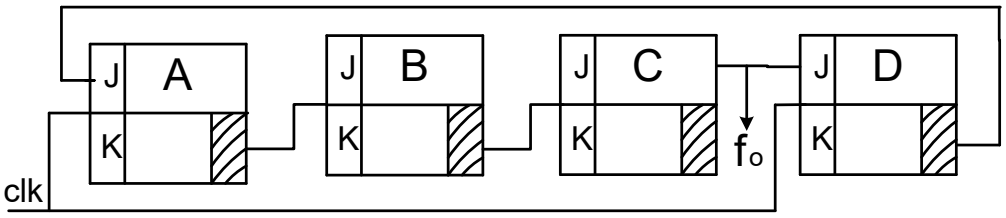
a) SR-FF (Active edge is high to low)
b) D-FF (Active edge is high to low)
c) Use circuit outputs in part (b) and minimum number of logic gates for getting the Count-down counter in Aiken code

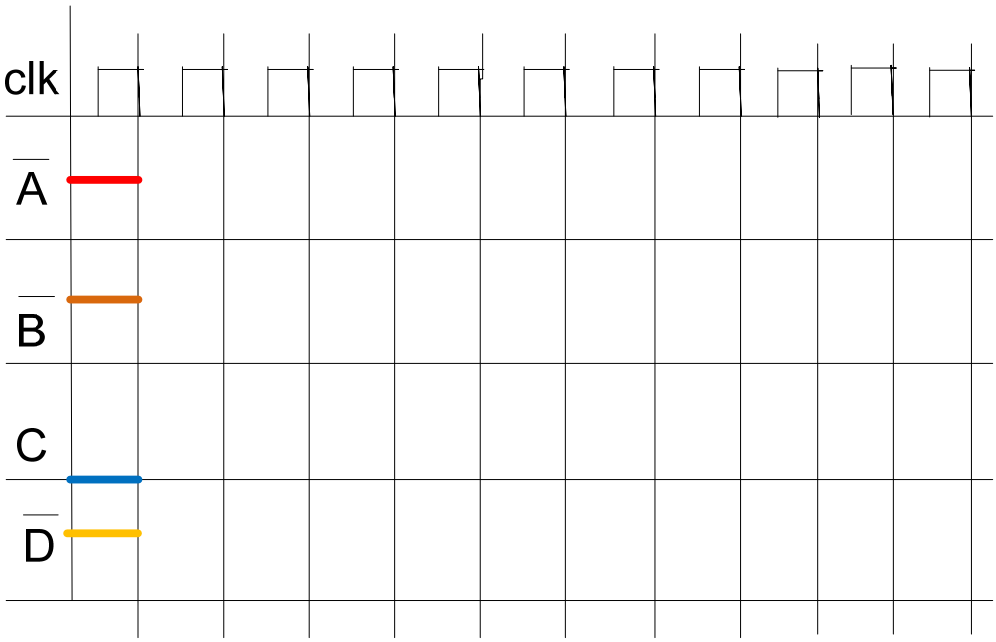
« 3 » Design a **closed loop** binary Counter for following sequence with D-FFs.
(0 →1→2→3→4→5→6→7→6→5→4→3→2→1→0)

« 4 »

a. Complete the timing diagram for the following circuit. The circuit works with falling edge. All of flip flops are JK-MS-FF and all J & K opens are 1.

b. Use timing diagram and specify the count routine of the circuit.
(Consider the main out-pout of each flip flop)





« **5** » For following circuit A and B are two binary numbers, (B= 0110b and A=0110b),

a. How many CLK pulse can pass to the buffer when the input LOAD goes to high for one period of CLK.

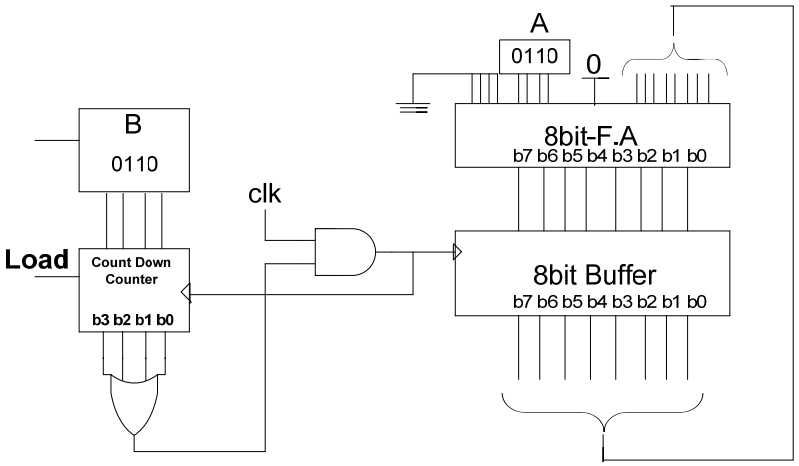
……

b. If the initial state of the 8-bit buffer is **zero**, specify the final value in the buffer, when the operation ended.

……

c. If the initial state of the 8-bit buffer is **00001010b**, specify the final value in the buffer, when the operation ended.

……...



d. Complete the following table for above circuit If the initial state of the 8-bit buffer is zero

	Output of 8-bit Adder								Output of 8-bit Buffer								Output of counter			
	b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**	**b3**	**b2**	**b1**	**b0**
Initial Value	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0
After 1 CLK																				
After 2 CLK																				
After 3 CLK																				
After 4 CLK																				
After 5 CLK																				
After 6 CLK																				
After 7 CLK																				
After 8 CLK																				
After 9 CLK																				

e. Design a divider circuit for A÷B which both A & B are 4bit binary numbers.

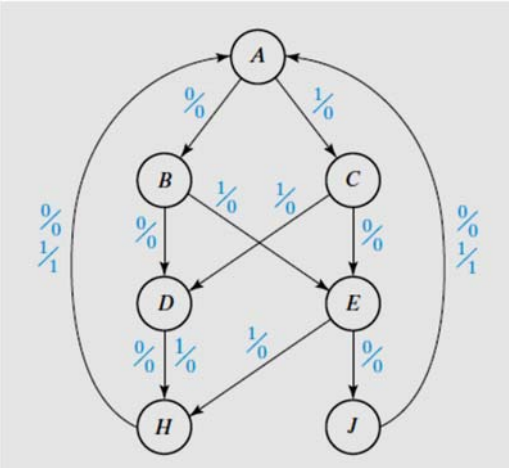
« 6 » a) Is following graph a Mealy or Moore machine?

b) Determine the state table of the following state graph.

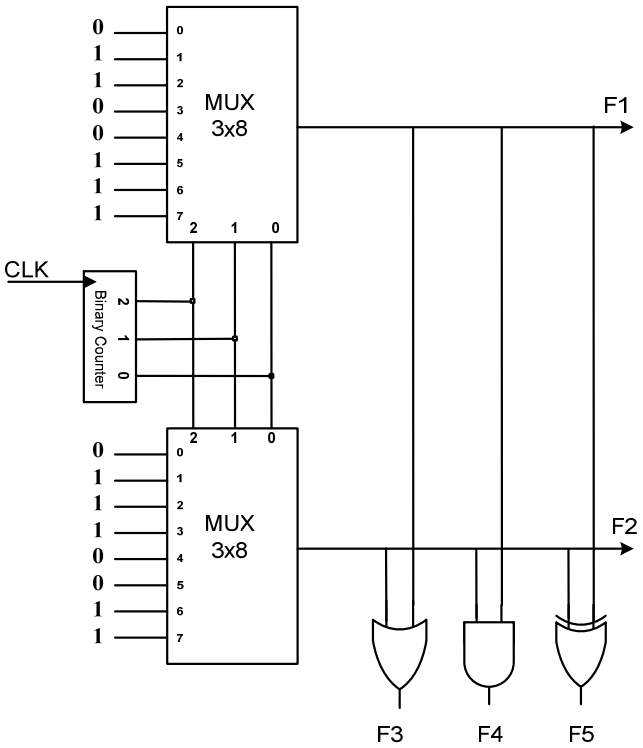
c) Reduce the number of states to minimum if it is possible.

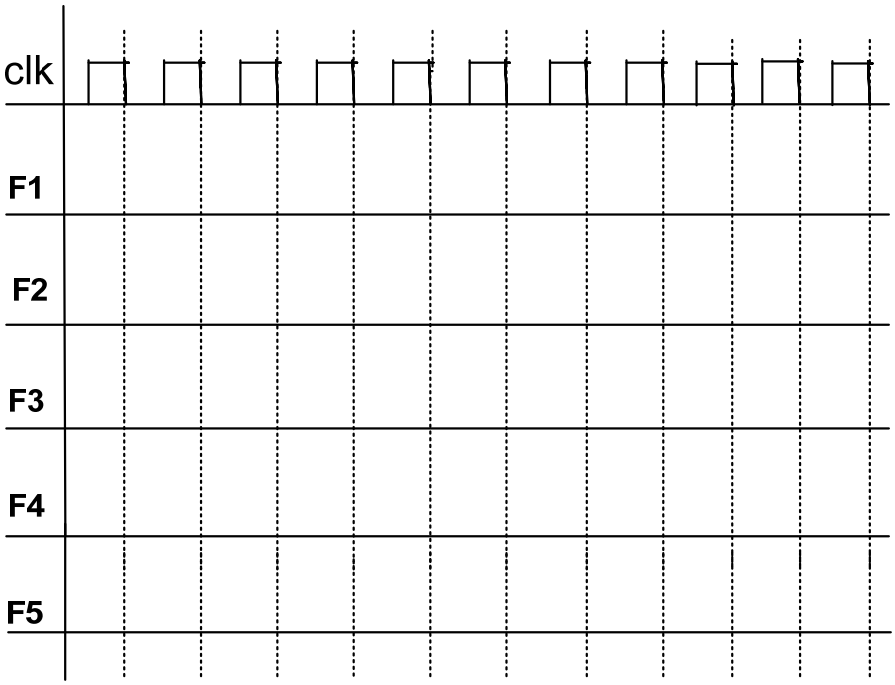
d) Design the circuit with D-FF

On the graph, X is independent input and Z is output. ($^{X}/_{Z}$).



« 7 » Consider following pattern generator circuit, and draw the output wave forms in the following timing diagram. (Initial state for the three bit count-up binary counter is 000)





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ECE Department

Dr. Tooraj Nikoubin

Fall 12/13/2017

First Name: ……

Last Name: …….

R#: ……

Section # 4

« 1 » A sequential detector circuit has one input (X) and one output (Z) for detection of **100 and/or 010** sequences.

a. Draw the state diagram for the circuit
b. Draw the state table for the circuit
c. Find the minimum number of states
d. Design the circuit with JK-FF (Draw the circuit)
e. Design the circuit with D-FF

« 2 » Design a Count-up Counter in Excess-3 code with following Flip Flops:

a) SR-FF (Active edge is high to low)
b) T-FF (Active edge is high to low)
c) Use of output of circuit in part (b) and minimum number of logic gates for getting the Count-down counter in Aiken code

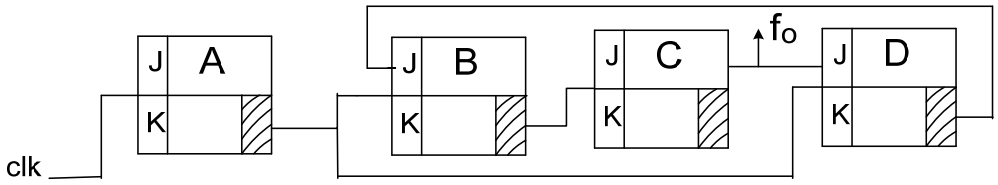
« 3 » Design a **closed loop** Counter for following sequence with SR-FFs.

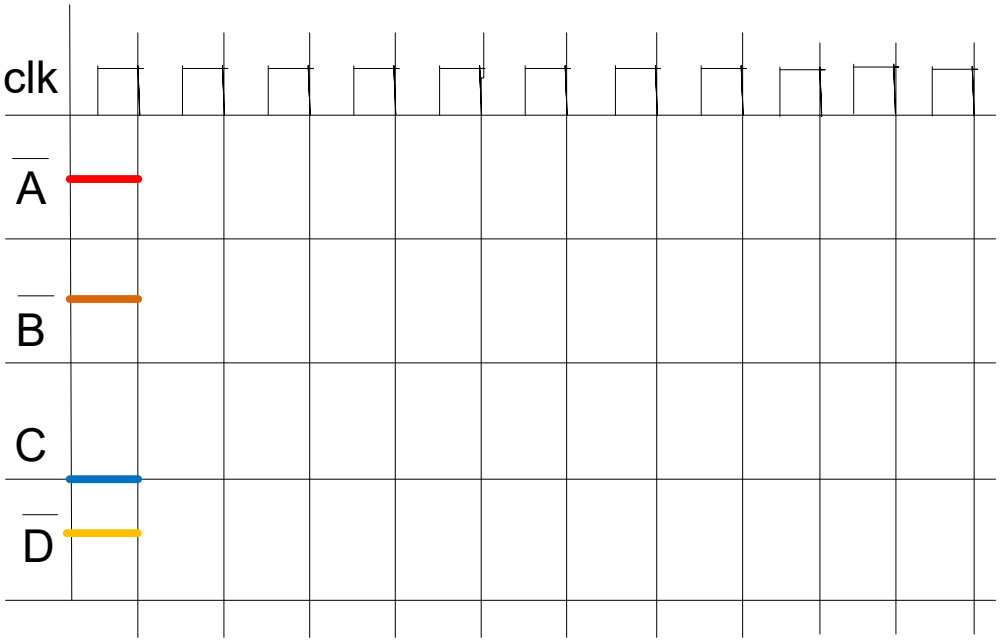
(7 →7→6→6→5→5→4→4→3→3→2→2→1→1→7)

« 4 »

a. Complete the following timing diagram for the following circuit. The circuit works with falling edge. All Flip Flops are JK-MS-FF and all J & K open inputs are 1.

b. By use of timing diagram specify the count routine of the circuit.
(Consider the main out-pout of each flip flop)





« **5** » For following circuit A and B are two binary numbers, (B= 0100b and A=1111b),

a. How many CLK pulse can pass to the buffer when the start signal goes to be high for one period of CLK.

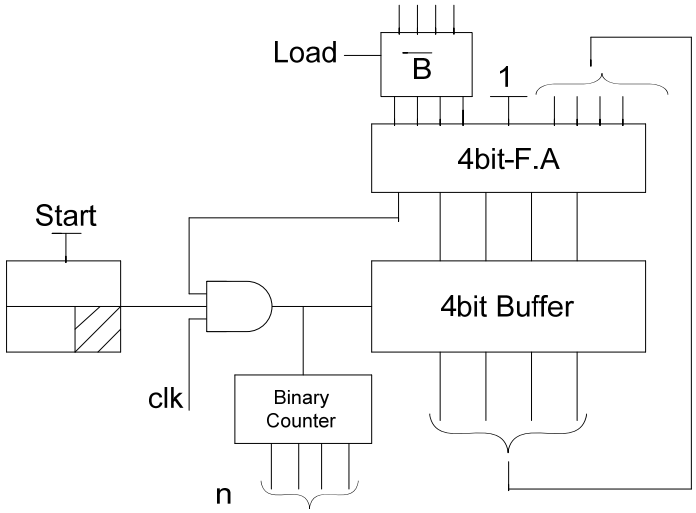
……

b. If the initial state of the 4-bit buffer is **A**, specify the final value in the buffer, when the operation ended.

……

c. If the initial state of the counter is **0111b**, specify the final value of the counter, when the operation ended.

…….



d. Complete the following table for above circuit If the initial state of the 4-bit buffer is A

	Output of 4-bit Adder **Co b3 b2 b1 b0**	Output of 4-bit Buffer **b3 b2 b1 b0**	Output of counter **b3 b2 b1 b0**
Initial Value	1 1 0 1 1	1 1 1 1	0 0 0 0
After 1 CLK			
After 2 CLK			
After 3 CLK			
After 4 CLK			
After 5 CLK			
After 6 CLK			
After 7 CLK			
After 8 CLK			
After 9 CLK			

e. Design a multiplier circuit for A x B which both A & B are 4bit binary numbers.

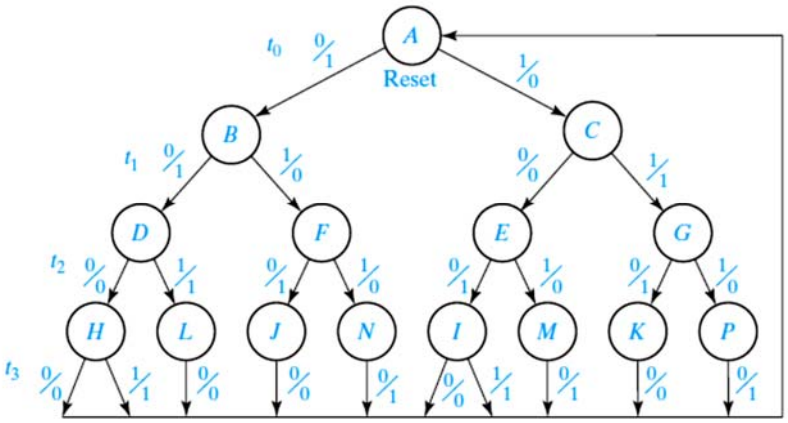
« 6 » a) Is following graph a Mealy or Moore machine?

b) Determine the state table of following state graph.

c) Reduce the number of states to minimum.

d) How many Flip Flop is needed for implementation of this circuit. ……

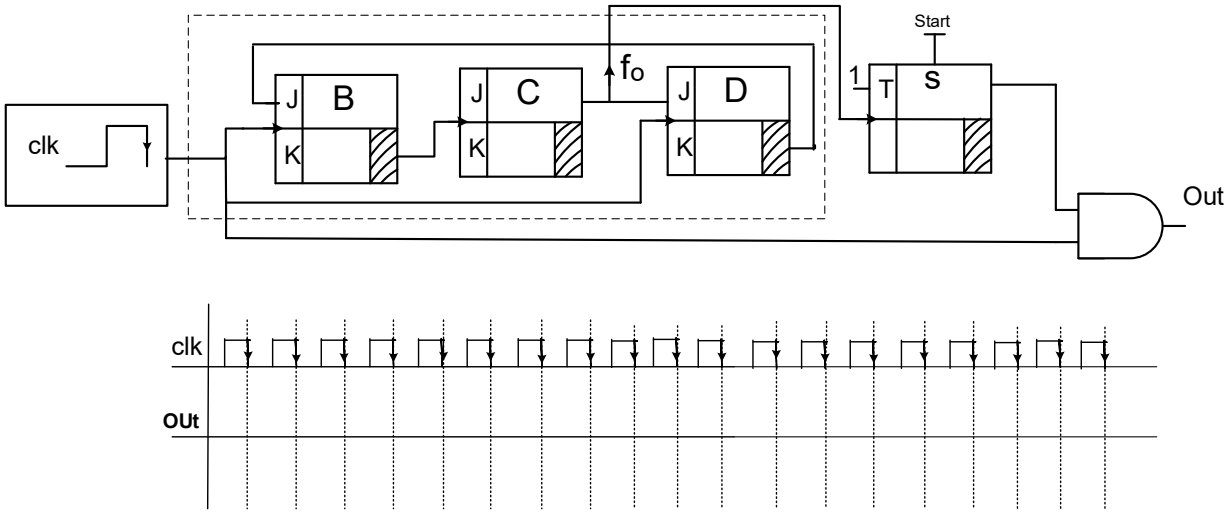
On the graph, X is independent input and Z is output. ($^{X}/_{Z}$).



« 7 » Consider following circuit which contains: frequency divider, T-FF, Oscillator and AND gate, Start signal can SET the T-FF.

a) Draw the wave form of the output on the following timing graph.

b) What is the value of the output (0 or 1) after 157 clock pulse .....



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Modern Digital System Design

ECE 2372

Final Exam

Texas Tech University

ECE Department

Dr. Tooraj Nikoubin

Fall 12/12/2016

First Name: ……

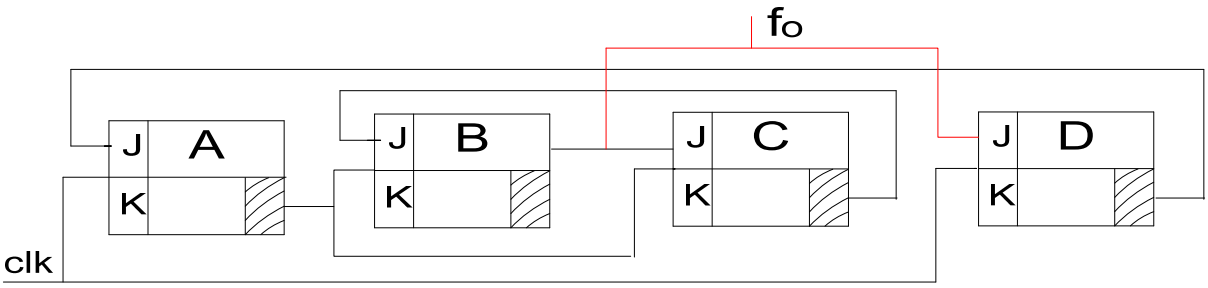
Last Name: …….

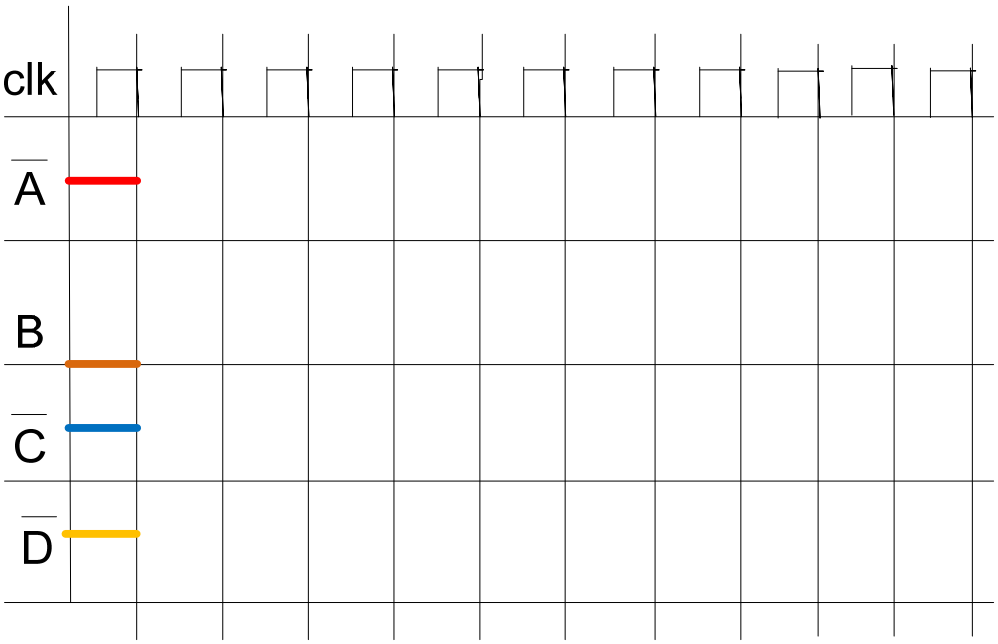
R#: ……

« 1 »

a. Complete the following timing diagram for the following circuit. The circuit works with falling edge. All of flip flops are JK-MS-FF.

b. By use of timing diagram specify the count routine of the circuit.
(Consider the main out-pout of each flip flop)



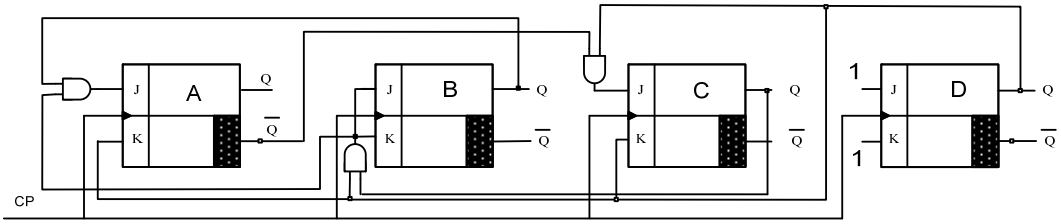


« 2 » Design a **Count-up** Counter in Excess-3 code with following flip flops:

a) SR-FF (Active edge is high to low)
b) D-FF (Active edge is high to low)
c) Use of output of circuit in part (b) and minimum number of logic gates for getting the **Count-down** counter in Excess-3 code

« 3 » Consider following sequential Circuit,

a) Specify the input functions of each flip flop (Ji & Ki) on the following table
b) Specify the input values of each flip flop (with 0 and/or 1) based on their function and previous state values
c) Specify the output of the flip flops for each state (with 0 and/or 1) and complete the diagram
d) With consideration of main outputs specify the routine of the count if A is MSB and D is LSB (Initial state for the counter is 000)



Function																
clk																
J_A																
K_A																
J_B																
K_B																
J_C																
K_C																
J_D																
K_D																
A	0															
B	0															
C	0															
D	0															

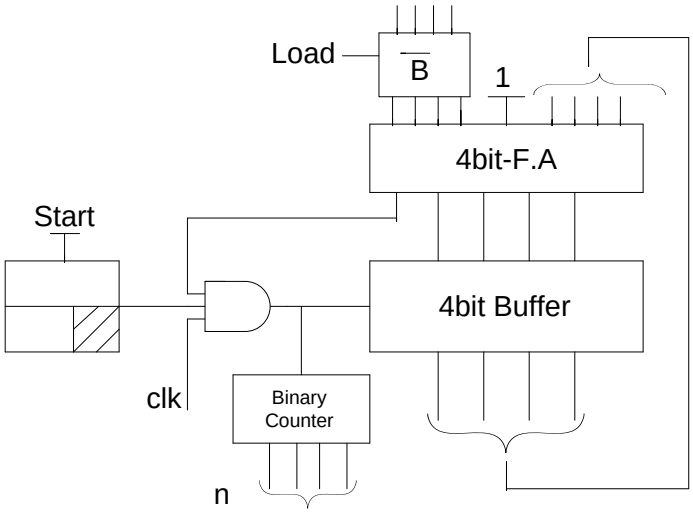
« 4 » Design a **closed loop** Counter for following sequence with D-FFs.
(7 →6→5→4→3→2→1→2→3→4→5→6→7)

« 5 » For following circuit A and B are two binary numbers, (B= 0011b and A=1110b),

a. How many CLK pulse can pass to the buffer when the start signal goes to be high for one period of CLK.

b. If the initial state of the 4-bit buffer is **A**, specify the final value in the buffer, when the operation ended.

c. If the initial state of the counter is **0110b**, specify the final in the counter, when the operation ended.



d. Complete the following table for above circuit If the initial state of the 4-bit buffer is A

	Output of 4-bit Adder **Co b3 b2 b1 b0**	Output of 4-bit Buffer **b3 b2 b1 b0**	Output of counter **b3 b2 b1 b0**
Initial Value	1 1 0 1 1	1 1 1 0	0 0 0 0
After 1 CLK			
After 2 CLK			
After 3 CLK			
After 4 CLK			
After 5 CLK			
After 6 CLK			
After 7 CLK			
After 8 CLK			
After 9 CLK			

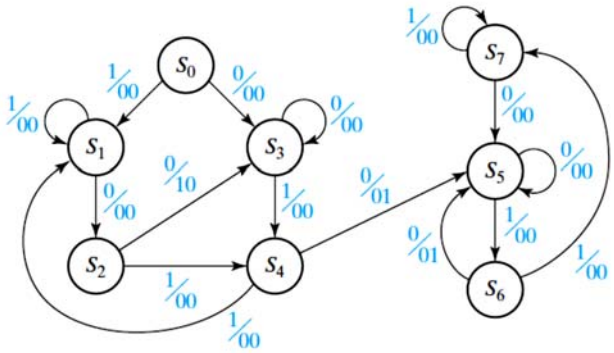
« 6 » A sequential detector circuit has one input (X) and one output (Z) for detection of **111 and/or 000** sequences.

a. Draw the state diagram for the circuit
b. Draw the state table for the circuit
c. Find the minimum number of states
d. Design the circuit with D-FF (Draw the circuit)
e. Design the circuit with T-FF

« 7 » a) Is following graph a Mealy or Moore machine?

b) Determine the state table of following state graph.

c) Reduce the number of states to minimum. On the graph, X is independent input and Z is output. ($^{X}/_{Z}$).



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Modern Digital System Design

ECE 2372

Final Exam

Texas Tech University

ECE Department

Dr. Tooraj Nikoubin

Spring 05/07/2015

First Name: …… **Last Name**: ……

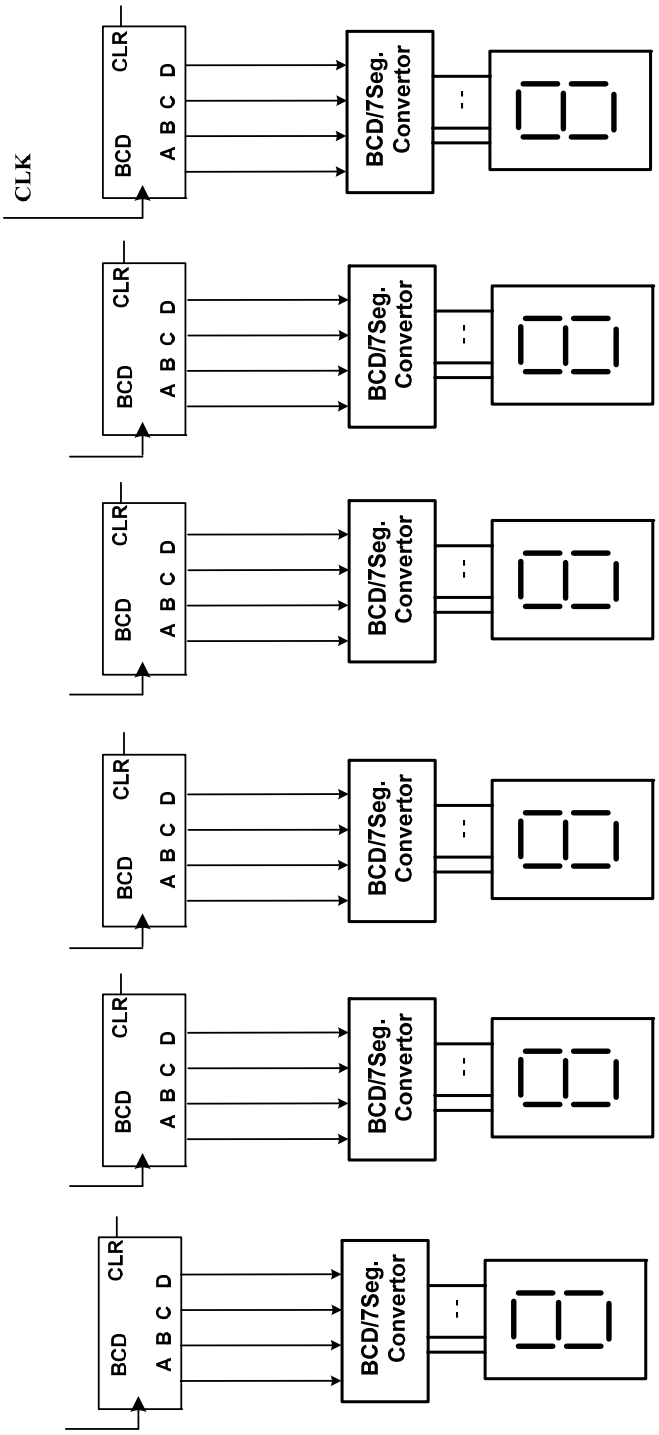
R#: ……

« 1 » Design a Count-up Counter in Excess-3 code with following flip flops.

a. JK-MS FF
b. D-FF

« 2 » Design a **closed loop** Counter for following sequence with SR-FF's.
(0 →1→1→2→2→3→4→5→5→6→7→0)

« 3 » Complete the following circuit with connections and logic gates for design of digital watch. The CLR input signals are synchronous and the counters can act with falling edges. Digital watch has three parts, second part (0-59), minute part (0-59) and hour part (0-23).



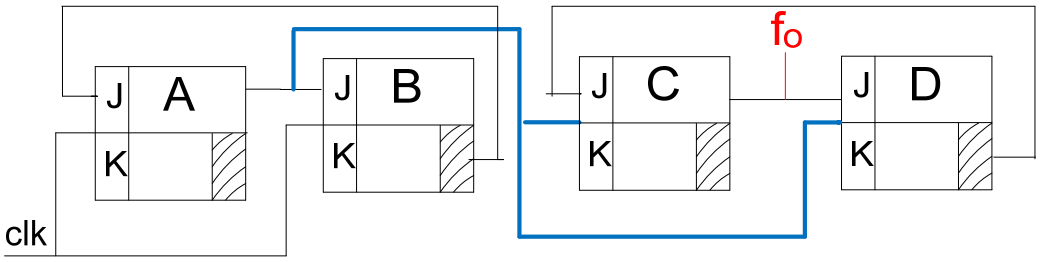
« 4 » A sequential circuit has one input (X) and one output (Z). The output occurs every time the input sequence 101 is completed.

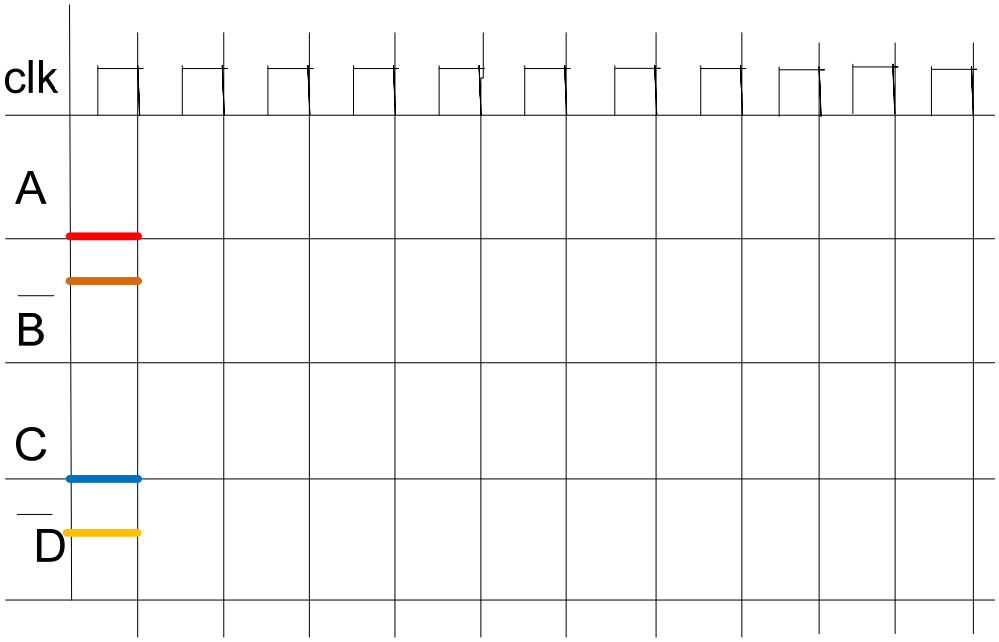
a. Draw the state diagram for the circuit
b. Draw the state table for the circuit
c. Find the minimum number of states
d. Design the circuit with JK-MS-FF
e. Design the circuit with D-FF

« 5 »

a. Complete the following timing diagram for the following circuit. The circuit works with falling edge. All of flip flops are JK-MS-FF.

b. By use of timing diagram specify the count routine of the circuit.
(Consider the main out-pout of each flip flop)



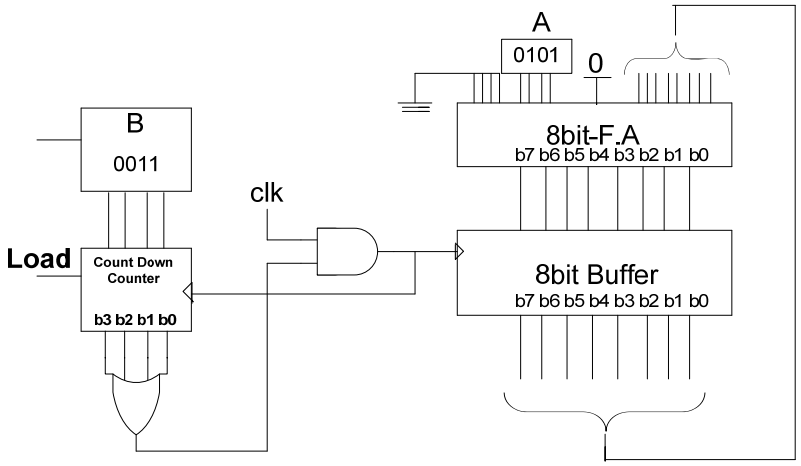


« 6 » For following circuit A and B are two binary numbers, (B= 0011b and A=0101b),

a. How many CLK pulse can pass to buffer when the input LOAD goes to be high for one period of CLK.

b. If the initial state of the 8-bit buffer is **<u>zero</u>**, specify the final value in the buffer, when the operation ended.

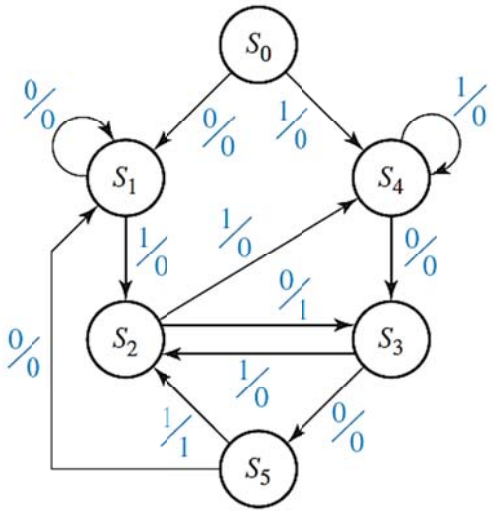
c. If the initial state of the 8-bit buffer is **<u>00000101b</u>**, specify the final value in the buffer, when the operation ended.



d. Complete the following table for above circuit If the initial state of the 8-bit buffer is zero

	Output of 8-bit Adder **b7 b6 b5 b4 b3 b2 b1 b0**	Output of 8-bit Buffer **b7 b6 b5 b4 b3 b2 b1 b0**	Output of counter **b3 b2 b1 b0**
After 1 CLK			
After 2 CLK			
After 3 CLK			
After 4 CLK			
After 5 CLK			
After 6 CLK			
After 7 CLK			
After 8 CLK			
After 9 CLK			

« 7 » Determine the state table of following state graph. Is this a Mealy or Moore machine? On the graph, X is independent input and Z is output. ($^{X}/_{Z}$)



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Modern Digital System Design

ECE 2372

Sample Problems # 1

Texas Tech University

ECE Department

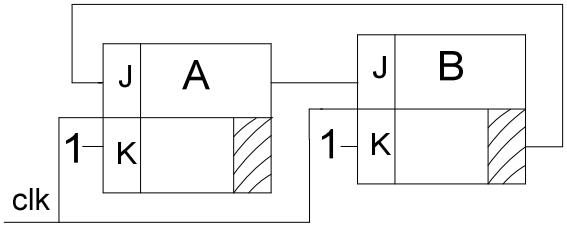
Dr. Tooraj Nikoubin

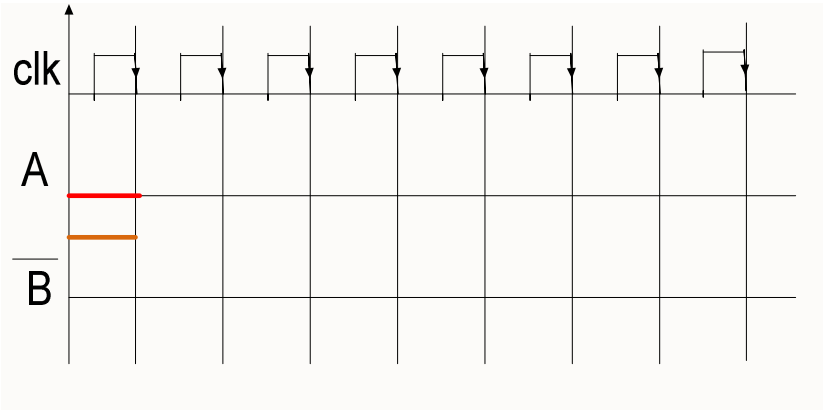
Fall --/--/2014

First Name: …… **Last Name**: ……

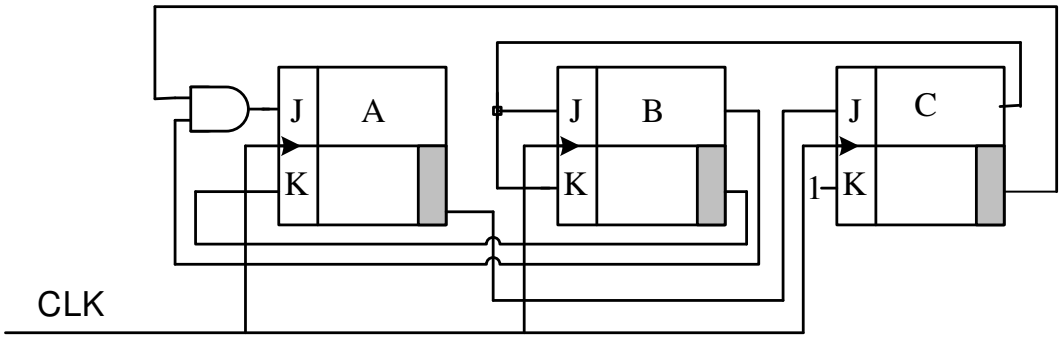
R#: …… Time: 100 min

« 1 » Complete the following timing diagram for the following circuit.
The circuit works with falling edge. Both of two FF's are JK-MS-FF.





« 2 » Determine the sequence of counting for following counter. (A is MSB and C is LSB)



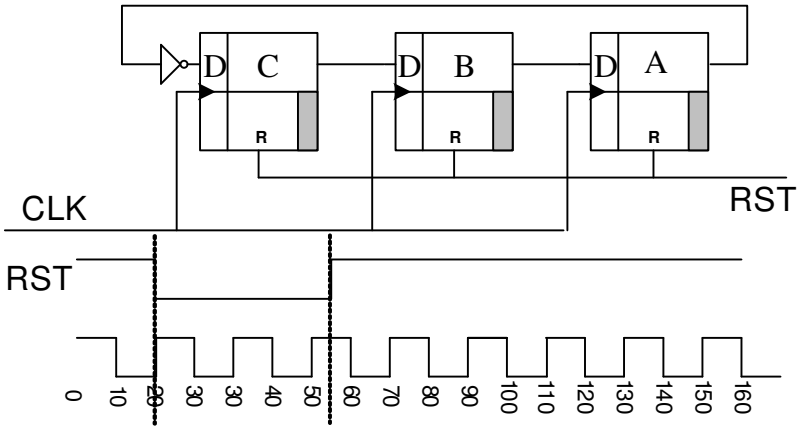
A) 0 → 2 → 3 → 5

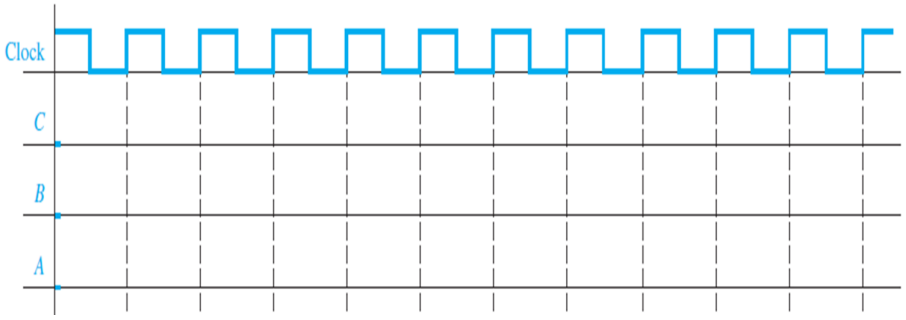
B) 0 → 1 → 2 → 7 → 4

C) 0 → 4 → 6 → 7

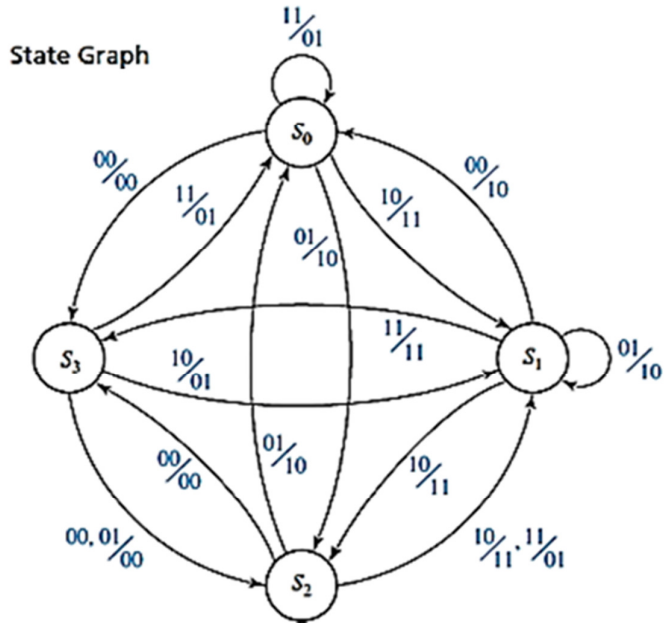
D) 0 → 2 → 4 → 7

« 3 » Complete the following timing diagram for the following circuit.
The circuit works with falling edge. RST is independent input signal.



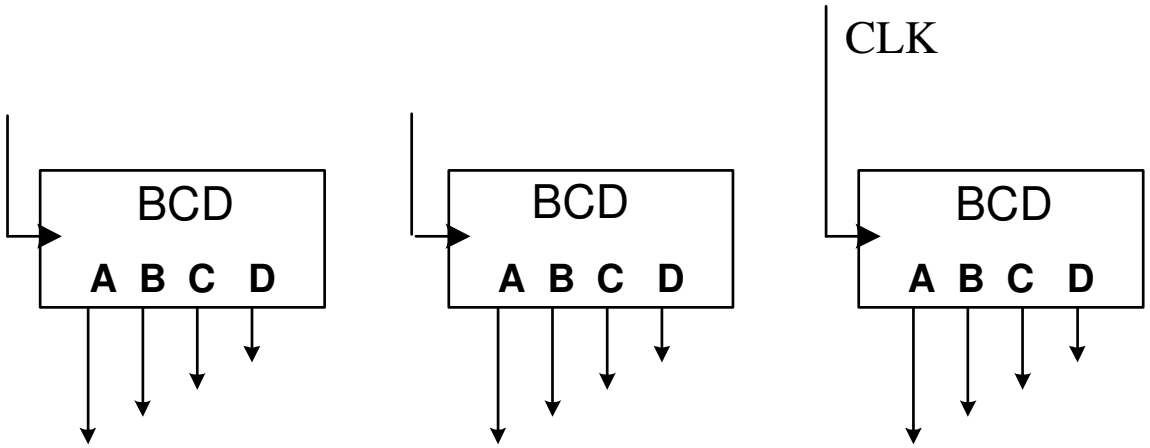


« 4 » Determine the state table of following state graph. Is this a Mealy or Moore machine?
On the graph, X1 and X2 are independent input signals and Z1 and Z2 are outputs.
($^{X2X1}/_{Z2Z1}$)



« 5 » Design a Count-down Counter in Excess-3 code with D-FF.

« 6 » Design a 3-digit count-up counter (0-999) with BCD count-up (0-9) counters. Use least possible logic gates in your design. The counters increment on falling edge. (A is MSB and D is LSB)



GOOD LUCK

Modern Digital System Design

ECE 2372

Sample Problems # 2

Texas Tech University

ECE Department

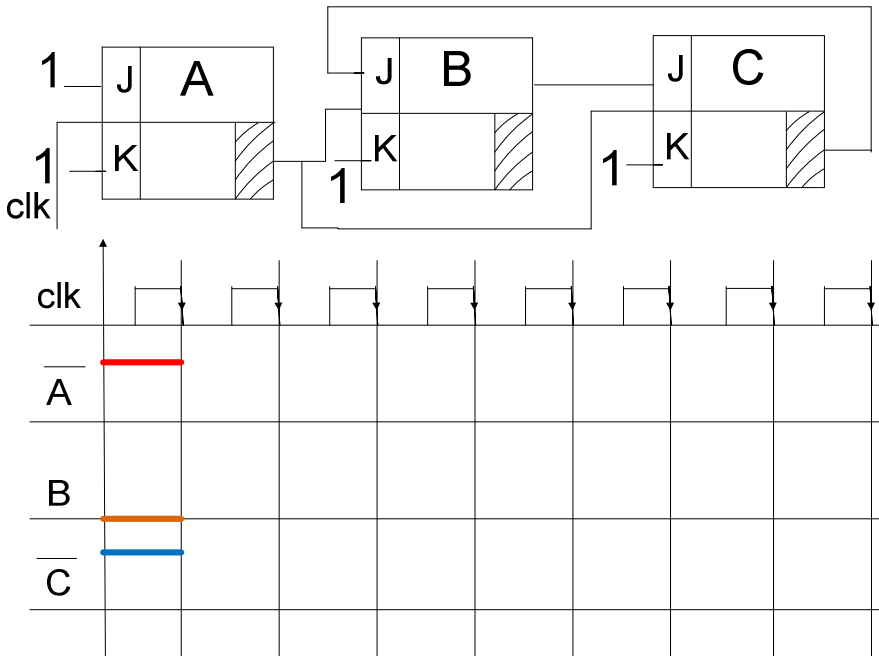
Dr. Tooraj Nikoubin

Fall --/--/2014

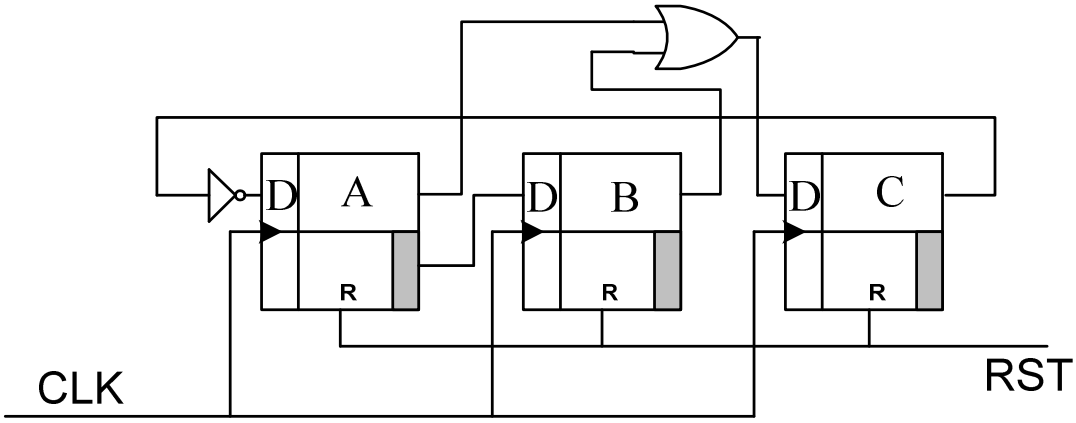
First Name: …… **Last Name**: ……

R#: …… Time: 120 min

« 1 » Complete the following timing diagram for the following circuit.
The circuit works with falling edge.



« 2 » Determine the sequence of counting for following counter.(A is MSB and C is LSB)



A) 0 → 2 → 3 → 5

B) 0 → 6 → 5 → 1 → 2 → 7

C) 0 → 4 → 6 → 7

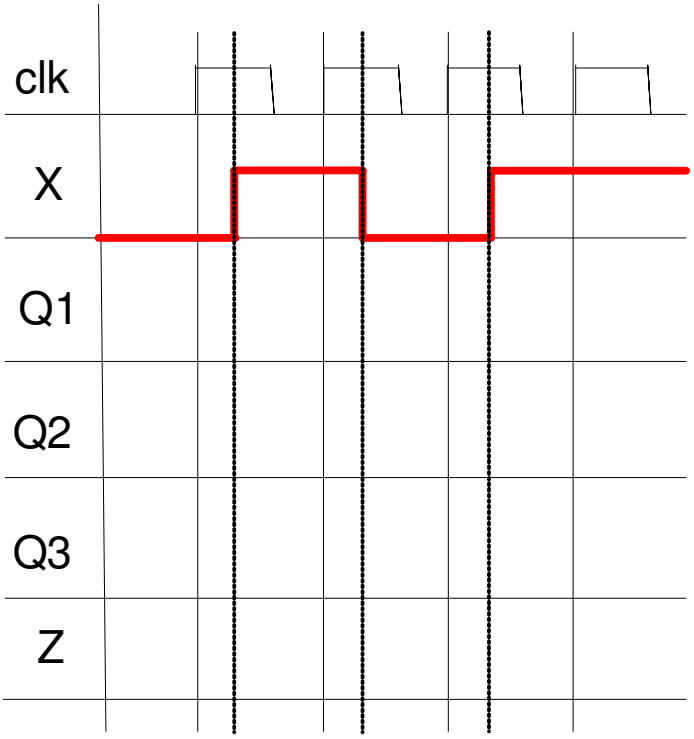
D) 0 → 2 → 4 → 7

« 3 » A sequential circuit has one input X, one output Z, and three flip-flops Q1, Q2, and Q3. The transition and output tables for the circuit follow:

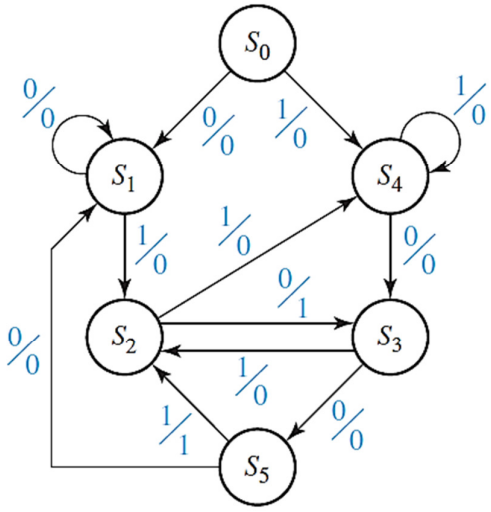
Present State	Next State $X=0$	Next State $X=1$	Output (Z) $X=0$	Output (Z) $X=1$
000	100	101	1	0
001	100	101	0	1
010	000	000	1	0
011	000	000	0	1
100	111	110	1	0
101	110	110	0	1
110	011	010	1	0
111	011	011	0	1

a) **Construct a timing chart for the input sequence X=0101 and initial state Q1Q2Q3=000. (Assume that the flip-flops are rising-edge triggered and that the input changes midway between the rising and falling edges of the clock.)**

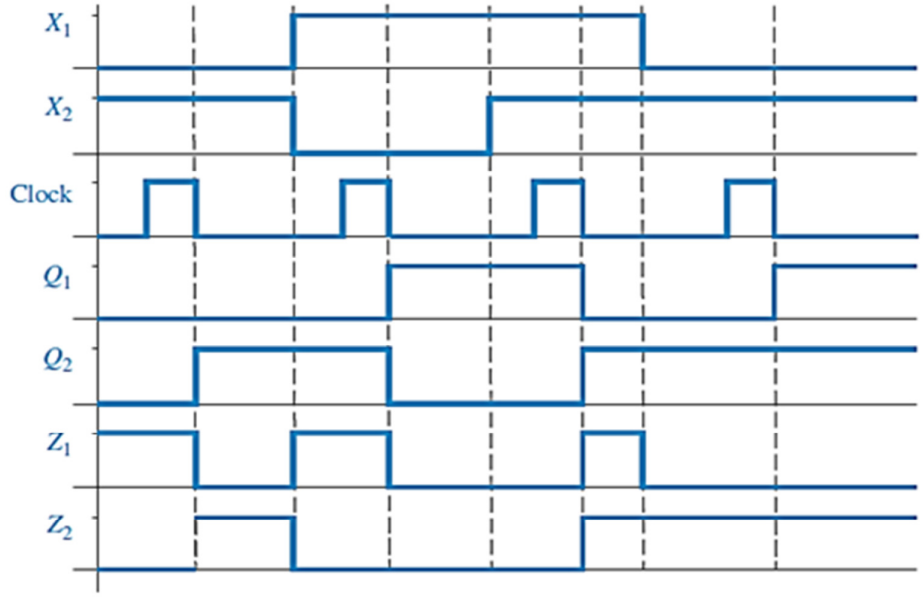
b) **List the output values produced by the input sequence.**



« 4 » Determine the state table of following state graph. Is this a Mealy or Moore machine? On the graph, X is independent input and Z is output. ($^{X}/_{Z}$)

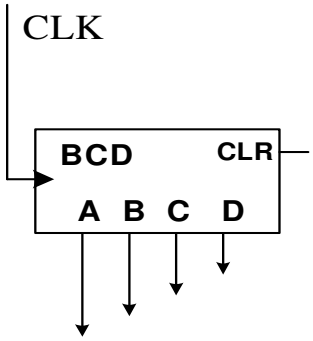


« 5 » Given the following timing chart for sequential circuit, construct as much of the state table as possible. Is this a Mealy or Moore machine? In the chart X1 and X2 are independent input signals and Z1 and Z2 are output signals. (X2X1/Z2Z1)



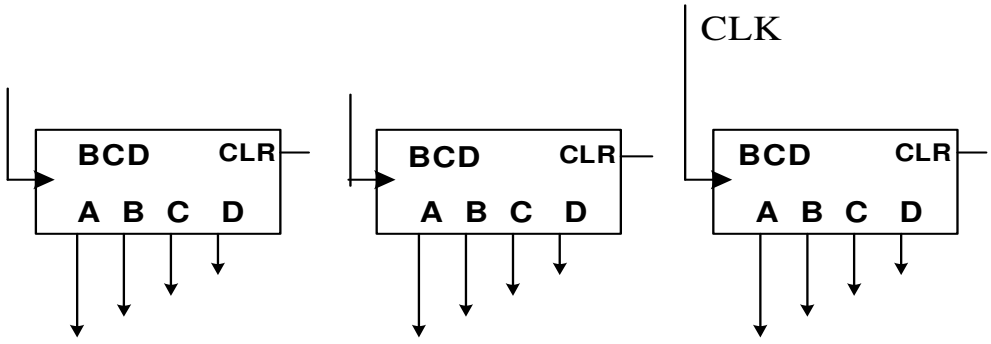
« 6 » Design a Count-up Counter for sequence of (0 --> 1 --> 2 --> 3 --> 4 --> 5 --> 6 --> 7) with BCD count-up counter block. The circuit works with falling edge (A is MSB and D is LSB)

a. **Use synchronous CLR input**
b. **Use Asynchronous CLR input**



« 7 » Design a 3-digit count-up counter (000-577) with BCD count-up (0-9) counter blocks. (Counter must go from 577 to 000) Use least possible logic gates in your design. The circuit works with falling edge (A is MSB and D is LSB)

a. **Use synchronous CLR inputs**
b. **Use Asynchronous CLR inputs**



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