CS3375: Computer Architecture
Spring 2020

Homework #6 Solution

- Name only: _____
- Release date: Apr 27th, 2020 (Monday)
- Due date: **May 4th, 2020 (Monday) before the class begins (1:00 PM)**
- It should be done INDIVIDUALLY; Show ALL your work
- Write your FULL name only
- Total: 10 pts

1. Caches are important to providing a high-performance memory hierarchy to processors. Below is a list of 32-bit memory address references, given as word addresses:

```
3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, 253
```

[6 pts]

a. For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty. Show all your work.

Word Address	Binary Address	Tag	Index	Hit/Miss
3	0000 0011	0	3	M
180	1011 0100	11	4	M
43	0010 1011	2	11	M
2	0000 0010	0	2	M
191	1011 1111	11	15	M
88	0101 1000	5	8	M
190	1011 1110	11	14	M
14	0000 1110	0	14	M
181	1011 0101	11	5	M
44	0010 1100	2	12	M
186	1011 1010	11	10	M
253	1111 1101	15	13	M

b. For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with two-word blocks and a total size of 8 blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty. Show all your work.

Word Address	Binary Address	Tag	Index	Hit/Miss

3	0000 0011	0	1	M
180	1011 0100	11	2	M
43	0010 1011	2	5	M
2	0000 0010	0	1	H
191	1011 1111	11	7	M
88	0101 1000	5	4	M
190	1011 1110	11	7	H
14	0000 1110	0	7	M
181	1011 0101	11	2	H
44	0010 1100	2	6	M
186	1011 1010	11	5	M
253	1111 1101	15	6	M

2. Assume a 2-way set associative cache with 4 blocks. To solve the problems in this exercise, you may find it helpful to draw a table like the one below, as demonstrated for the address sequence "0, 1, 2, 3, 4".

Address of Memory Block Accessed	Hit or Miss	Evicted Block	Contents of Cache Blocks After Reference			
			Set 0	Set 0	Set 1	Set 1
0	Miss		Mem[0]			
1	Miss		Mem[0]		Mem[1]	
2	Miss		Mem[0]	Mem[2]	Mem[1]	
3	Miss		Mem[0]	Mem[2]	Mem[1]	Mem[3]
4	Miss	0	Mem[4]	Mem[2]	Mem[1]	Mem[3]
...						

Consider the following address sequence: `0, 2, 4, 8, 10, 12, 14, 16, 0`

[4 pts]

a. Assuming a least recently used (LRU) replacement policy, how many hits does this address sequence exhibit? Show all your work.

- 0 hit

Address of Memory Block Accessed	Hit or Miss	Evicted Block	Contents of Cache Blocks After Reference			
			Set 0	Set 0	Set 1	Set 1
0	M		0			
2	M		0	2		
4	M	0	4	2		
8	M	2	4	8		
10	M	4	10	8		
12	M	8	10	12		
14	M	10	14	12		
16	M	12	14	16		
0	M	14	0	16		

b. Assuming a most recently used (MRU) replacement policy, how many hits does this address sequence exhibit? Show all your work.

- 1 hit

Address of Memory Block Accessed	Hit or Miss	Evicted Block	Contents of Cache Blocks After Reference			
			Set 0	Set 0	Set 1	Set 1
0	M		0			
2	M		0	2		
4	M	2	0	4		
8	M	4	0	8		
10	M	8	0	10		
12	M	10	0	12		
14	M	12	0	14		
16	M	14	0	16		
0	H		0	16		