Modern Digital System Design

ECE 2372
SECOND TEST

Texas Tech University
ECE Department
Dr. Tooraj Nikoubin

Spring 04/11/2016

First Name: ……

Last Name: …….

R#: …….

« 1 » a) Use a 8 to 1 multiplexer and a minimum number of external gates to realize the following function.

b) Use a 4 to 1 multiplexer and a minimum number of external gates to realize the following function.

Q= F(w, x, y, z) = $\sum_{m}(0, 3, 4, 5, 7, 8, 10, 14)$ **+** $\sum_{d}(2, 6, 11)$

« 2 » a) Implement a full adder using one 3 to 8 decoder active high outputs and minimum logic gates. **b)** Implement a full adder using one 3 to 8 decoder with active low outputs and minimum logic gates.

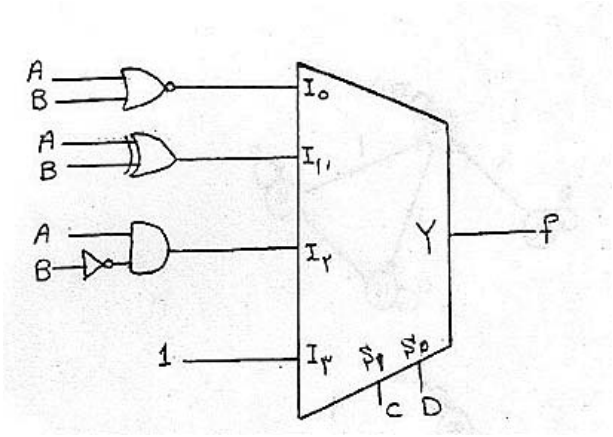
« 3 » **a)** Implement a 8 to1 multiplexer with 4 to 1 multiplexers.

b) Implement a 4 to 16 decoder with 2 to 4 decoders with enable input.

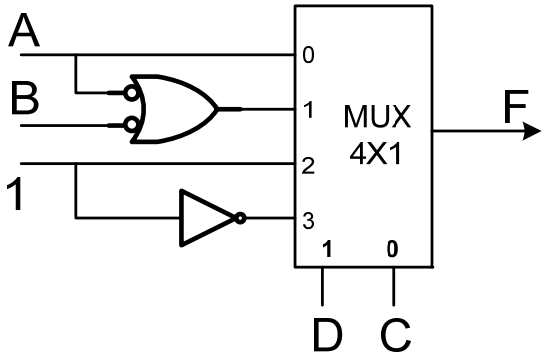
« 4 » a) Implement a 12bit binary adder with 4-bit binary adder blocks.

b) Implement a comparator for two 2-bit binary numbers with 4-bit Adder block.

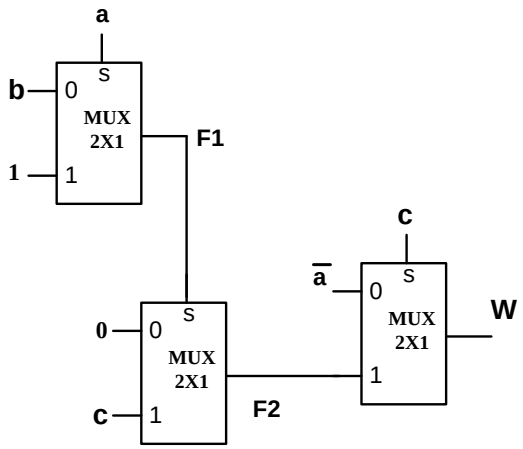
« 5 » Find the Mintrem numbers and output function of following circuit.

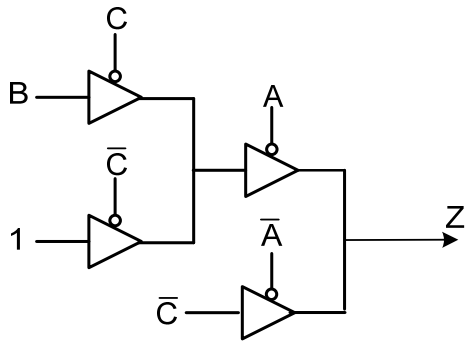


B) Find the Maxterm numbers and the output function for following circuit.



« 6 » Find the output Functions for Following circuits:





« 7 » a) Design one digit BCD adder, with 4-bit binary adder blocks and logic gates.

b) Implement one bit full adder with suitable PLA.

GOOD LUCK

Modern Digital System Design

ECE 2372
SECOND TEST

Texas Tech University
ECE Department
Dr. Tooraj Nikoubin

Fall 10/24/2016

First Name: ……

Last Name: …….

R#: …….

« 1 » a) Use a 4 to 1 multiplexer and a minimum number of external gates to realize the following function.

b) Use a 8 to 1 multiplexer and a minimum number of external gates to realize the following function.

Q = F (w, x, y, z) = $\sum_{m}(0, 1, 5, 7, 8, 9, 11, 12, 14)$ **+** $\sum_{d}(2, 6)$

« 2 » a) Implement following functions (Q1, Q2 & Q3) using one 3 to 8 decoder active high outputs and minimum logic gates. **b)** Implement following functions (Q1, Q2 & Q3) using one 3 to 8 decoder with active low outputs and minimum logic gates.

Q1 = F (x, y, z) = $\sum_{m}(\mathbf{0}, \mathbf{1}, \mathbf{3}, \mathbf{7},)$

Q2 = F (x, y, z) = $\sum_{m}(\mathbf{0}, \mathbf{2}, \mathbf{5}, \mathbf{6},)$

Q3 = F (x, y, z) = $\sum_{m}(\mathbf{1}, \mathbf{4}, \mathbf{5}, \mathbf{7},)$

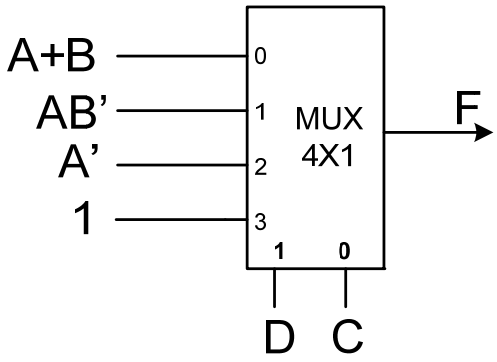
« 3 » **a)** Implement a 16 to1 multiplexer with 4 to 1 multiplexers.

b) Implement a 5 to 32 decoder with 3 to 8 decoders with enable input.

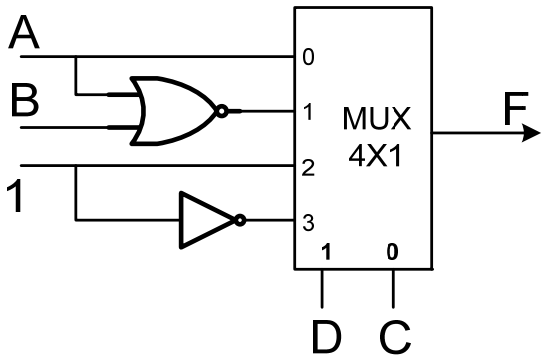
« 4 » a) Implement a 10bit binary adder with 4-bit binary adder blocks.

b) Use circuit (a) to implement a comparator for two 2-bit binary numbers with 6-bit Adder block. (Redraw the circuit for this part)

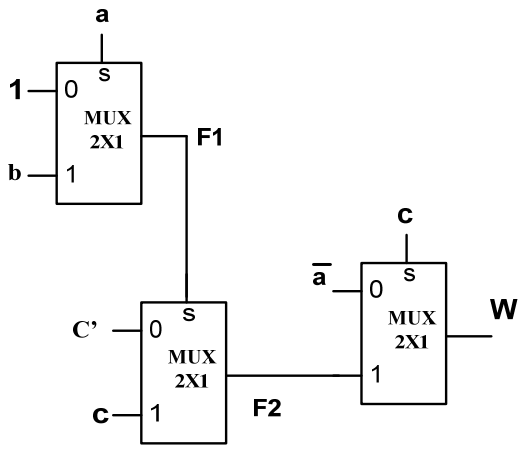
« 5 » Find the Mintrem numbers and output function of following circuit.



B) Find the Maxterm numbers and the output function for following circuit.



« 6 » a) Find the output Functions for Following circuits:



b) Implement the following function using only 2-to-1 MUXes:

$R = ab'h' + bch' + eg'h + fgh.$

c) Repeat part (b) using only tri-state buffers.

« 7 » a) Design one digit BCD adder, with 4-bit binary adder blocks and logic gates.

b) Implement 2-bit full binary adder with suitable PLA. (A=a1a0 & B=b1b0)

GOOD LUCK