Homework 3- Solution

Total Mark - 100

1. Design a combinational circuit that accepts a 4-bit number and generates a 3 –bit binary number output that approximates the square root of the number. If the square root is 3.5 or larger, give a result of 4. If less than <3.5 and >2.5, give the result of 3.

A	B	C	D	S2	S1	S0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	1	0
0	1	1	1	0	1	1
1	0	0	0	0	1	1
1	0	0	1	0	1	1
1	0	1	0	0	1	1
1	0	1	1	0	1	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0

$S0 = \bar{B}\bar{C}D + \bar{B}C\bar{D} + A\bar{B} + A\bar{C}\bar{D} + \bar{A}BCD$

$S1 = \bar{A}B + A\bar{B} + \bar{A}CD + B\bar{C}\bar{D}$

$S2 = ABC + ABD$

2. Design a circuit with a 4-bit BCD input A,B,C,D that produces an output W,X,Y,Z that is equal to the input +6 in binary. For example 9(1001)+6(0110)=15(1111). The output for invalid BCD codes are don't cares.

A	B	C	D	W	X	Y	Z
0	0	0	0	0	1	1	0
0	0	0	1	0	1	1	1
0	0	1	0	1	0	0	0
0	0	1	1	1	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	1	0	1	1
0	1	1	0	1	1	0	0
0	1	1	1	1	1	0	1
1	0	0	0	1	1	1	0
1	0	0	1	1	1	1	1
1	0	1	0	x	x	x	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	x	X	x	X

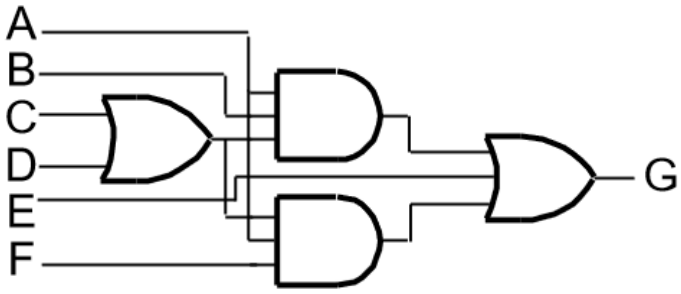
$$W = A + B + C$$

$$X = \bar{B}\bar{C} + BC$$

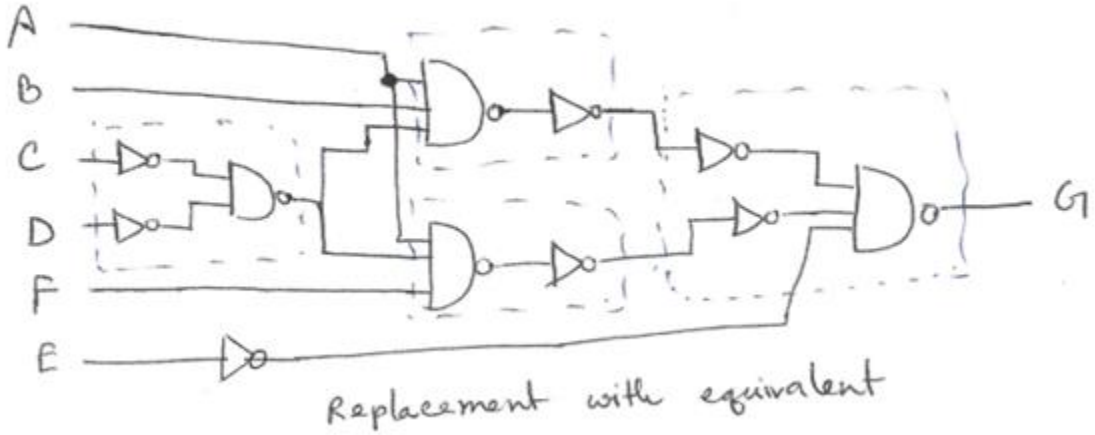
$$Y = \bar{C}$$

$$Z = D$$

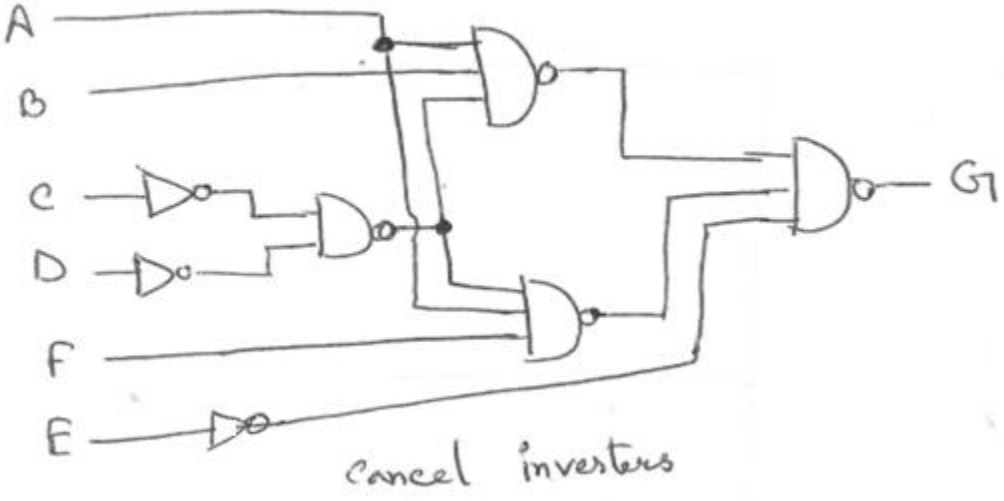
3. Perform technology mapping to (a) NAND and (b) NOR gates for the following circuit



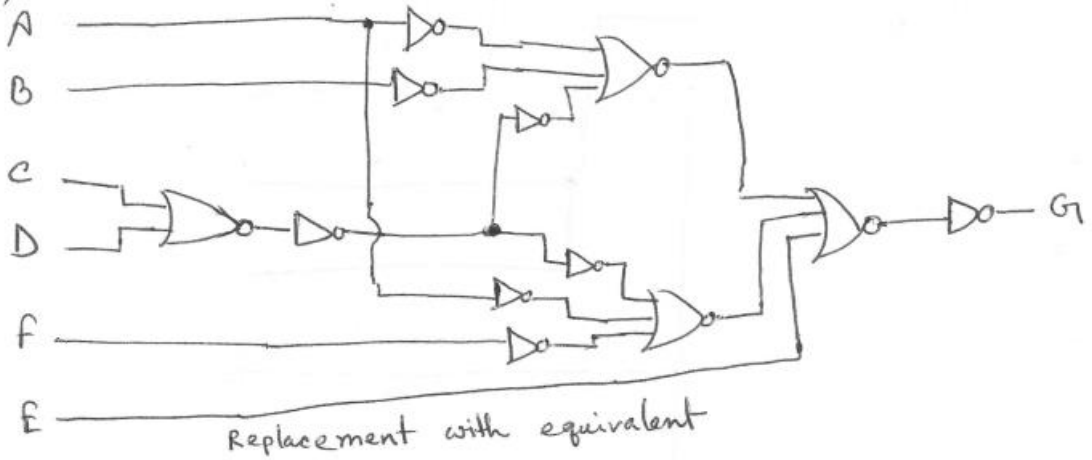
3(a)



3(a)

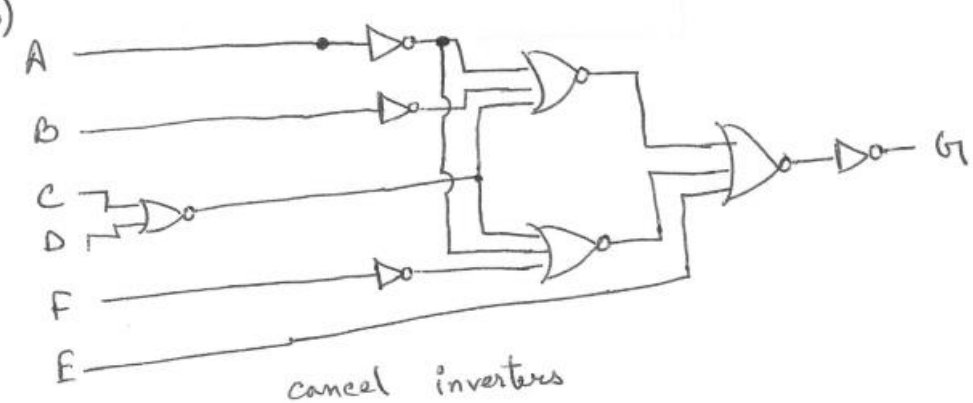


3(b)



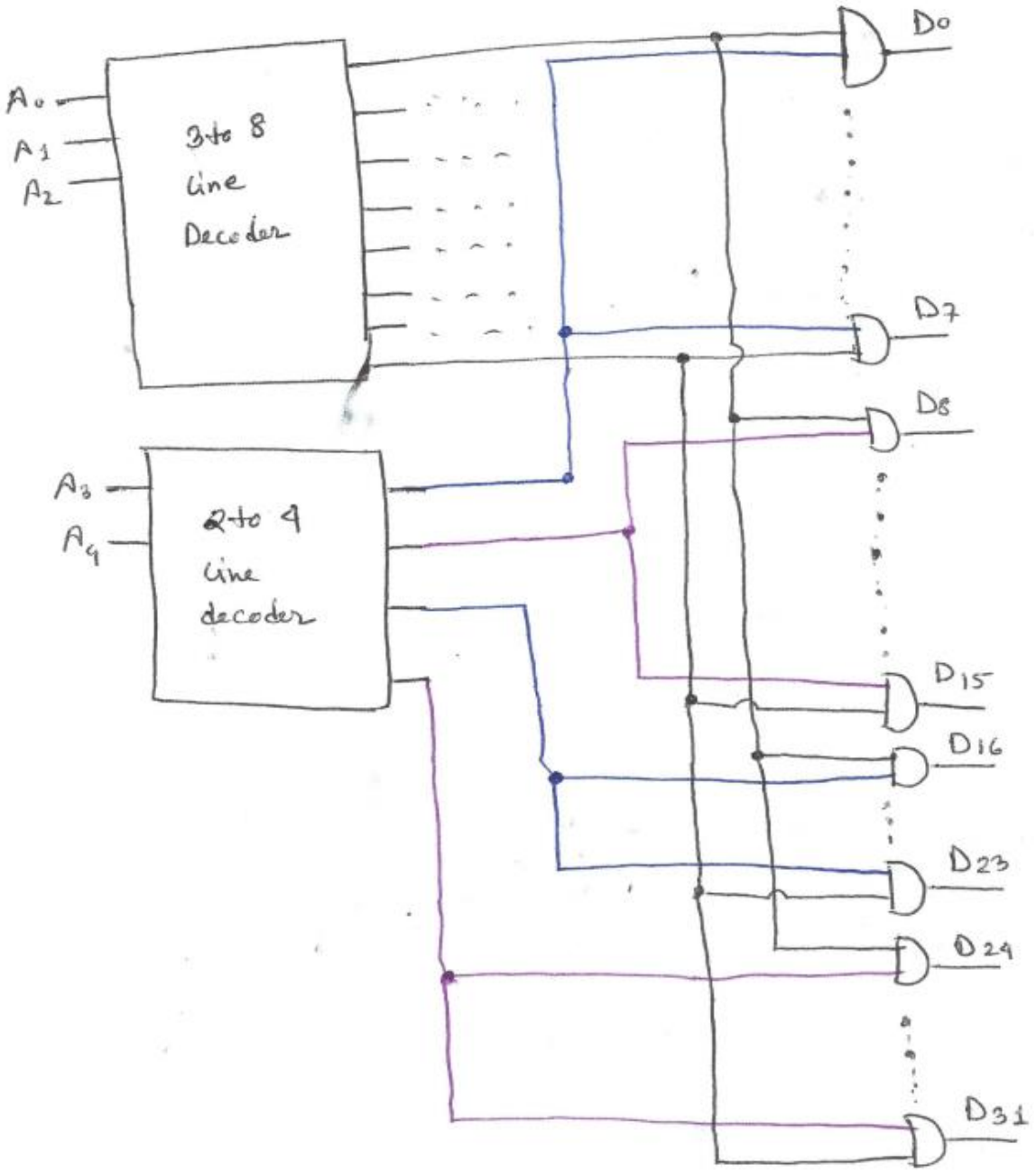
Replacement with equivalent

3(b)



cancel inverters

4. Design a 5 to 32 line decoder using a 3 to 8 line decoder ,a 2 to 4 line decoder and 32 2 input AND gates.



5. Design a 4-input priority encoder with four inputs and three outputs including the valid bit but with the truth table representing the case in which input D_0 has the highest priority and input D_3 has the lowest priority.

D_3	D_2	D_1	D_0	A_1	A_0	V
0	0	0	0	X	X	0
X	X	X	1	0	0	1
X	X	1	0	0	1	1
X	1	0	0	1	0	1
1	0	0	0	1	1	1

6. A combinational circuit is defined by the two Boolean functions

$$F_1 = \overline{X + Z} + XYZ$$

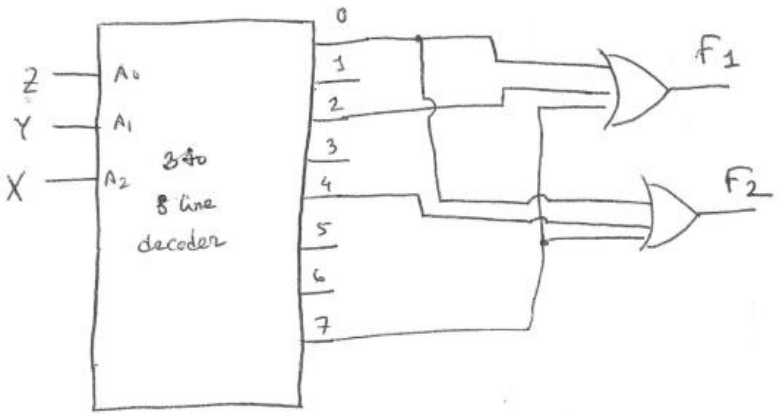
$$F_2 = \overline{Y + Z} + XYZ$$

Design the circuit with a decoder and external OR gate.

X	y	Z	XYZ	(X+Z)'	(Y+Z)'	F1	F2
0	0	0	0	1	1	1	1
0	0	1	0	0	0	0	0
0	1	0	0	1	0	1	0
0	1	1	0	0	0	0	0
1	0	0	0	0	1	0	1
1	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0
1	1	1	1	0	0	1	1

6 ⇒ $F_1 = \Sigma m(0, 2, 7)$

$F_2 = \Sigma m(0, 4, 7)$

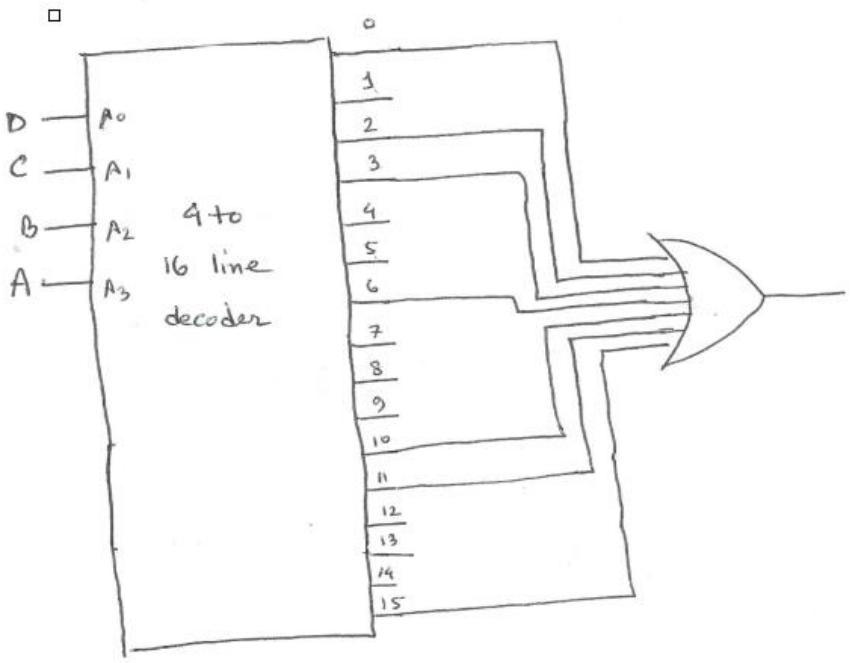


7. A combinational circuit is defined by the following Boolean functions

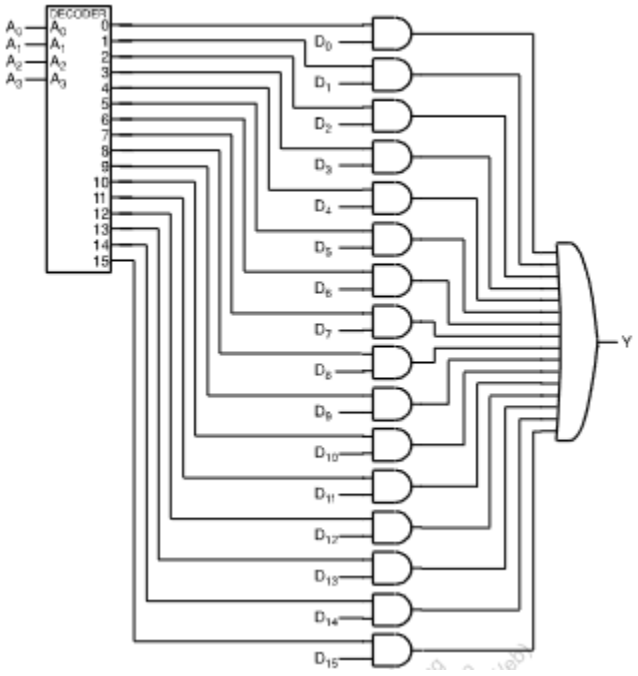
$$F(A,B,C,D) = \sum m(0,2,3,6,10,11,15)$$

Design the circuit with a decoder and external OR gate.

7. $F(A,B,C,D) = \sum m(0,2,3,6,10,11,15)$



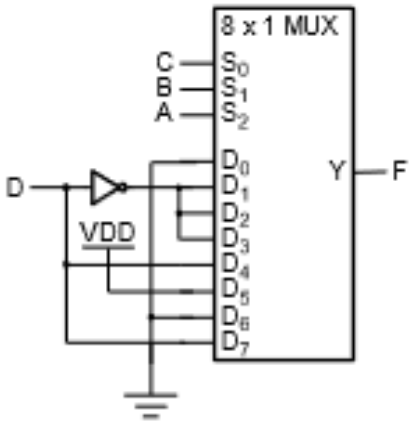
8. Design a 16 to 1 line multiplexer using a 4 to 16 line decoder and a 16 × 2 AND OR.



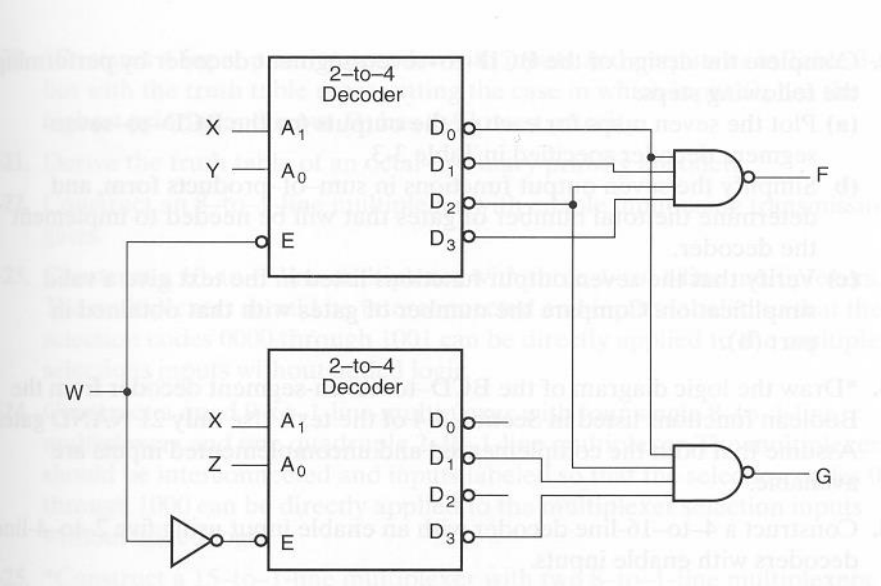
9. Implement the following Boolean function with an 8 to 1 line multiplexer and a single inverter with variable D as its input.

$$F(A,B,C,D) = \sum m(2,4,6,9,10,11,15)$$

A	B	C	D	F	
0	0	0	0	0	F = 0
0	0	0	1	0	
0	0	1	0	1	F = $\bar{D}$
0	0	1	1	0	
0	1	0	0	1	F = $\bar{D}$
0	1	0	1	0	
0	1	1	0	1	F = $\bar{D}$
0	1	1	1	0	
1	0	0	0	0	F = D
1	0	0	1	1	
1	0	1	0	1	F = 1
1	0	1	1	1	
1	1	0	0	0	F = 0
1	1	0	1	0	
1	1	1	0	0	F = D
1	1	1	1	1	



10. Find the truth table for the outputs F and G of the hierarchical circuit shown below.



W	X	Y	Z	F	G
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	1	1
0	1	0	1	1	1
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	1	0	1
1	0	1	0	0	0
1	0	1	1	0	1
1	1	0	0	0	0
1	1	0	1	0	1
1	1	1	0	0	0
1	1	1	1	0	1