

CS3375: Computer Architecture

Spring 2020

Homework #6

- Name only: Chen Zhang
- Release date: Apr 27th, 2020 (Monday)
- Due date: **May 4th, 2020 (Monday) before the class begins (1:00 PM)**
- It should be done INDIVIDUALLY; Show ALL your work
- Write your FULL name only
- Total: 10 pts

I. Caches are important to providing a high-performance memory hierarchy to processors. Below is a list of 32-bit memory address references, given as word addresses:

3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, 253

[6 pts]

- a. For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty. Show all your work.

Word Address	Binary Address	Tag	Index	Hit/Miss
3	00000011	0000	3	Miss
180	10110100	1011	4	Miss
43	00101011	0010	11	Miss
2	00000010	0000	2	Miss
191	10111111	1011	15	Miss
88	01011000	0101	8	Miss
190	10111110	1011	14	Miss
14	00001110	0000	14	Miss
181	10110101	1011	5	Miss
44	00101100	0010	12	Miss
186	10111010	1011	10	Miss
253	11111101	1111	13	Miss

- b. For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with two-word blocks and a total size of 8 blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty. Show all your work.

Word Address	Binary Address	Tag	Index	Hit/Miss
3	00000011 0000	1	1	Miss
180	10110100 1011	2	0	Miss
43	00101011 0010	5	1	Miss
2	00000010 0000	1	0	Hit
191	10111111 1011	7	1	Miss
88	01011000 0101	4	0	Miss
190	10111110 1011	7	0	Hit
14	00001110 0000	7	0	Miss
181	10110101 1011	2	1	Hit
44	00101100 0010	6	0	Miss
186	10111010 1011	5	0	Miss
253	11111101 1111	6	1	Miss

2. Assume a 2-way set associative cache with 4 blocks. To solve the problems in this exercise, you may find it helpful to draw a table like the one below, as demonstrated for the address sequence “0, 1, 2, 3, 4”.

Address of Memory Block Accessed	Hit or Miss	Evicted Block	Contents of Cache Blocks After Reference			
			Set 0	Set 0	Set 1	Set 1
0	Miss		Mem[0]			
1	Miss		Mem[0]		Mem[1]	
2	Miss		Mem[0]	Mem[2]	Mem[1]	
3	Miss		Mem[0]	Mem[2]	Mem[1]	Mem[3]
4	Miss	0	Mem[4]	Mem[2]	Mem[1]	Mem[3]
...						

Consider the following address sequence: 0, 2, 4, 8, 10, 12, 14, 16, 0

[4 pts]

- a. Assuming a least recently used (LRU) replacement policy, how many hits does this address sequence exhibit? Show all your work.

Address of Memory Block Accessed	Hit or Miss	Evicted Block	Contents of Cache Blocks After Reference			
			Set 0	Set 0	Set 1	Set 1
0	Miss		Memo[0]			
2	Miss		Memo[0]	Memo[2]		
4	Miss		Memo[4]	Memo[2]		
8	Miss		Memo[4]	Memo[8]		
10	Miss		Memo[4]	Memo[8]	Memo[10]	
12	Miss		Memo[12]	Memo[8]	Memo[10]	
14	Miss		Memo[12]	Memo[8]	Memo[14]	
16	Miss		Memo[12]	Memo[16]	Memo[14]	
0	Miss	0	Memo[0]	Memo[16]	Memo[14]	

- b. Assuming a most recently used (MRU) replacement policy, how many hits does this address sequence exhibit? Show all your work.

Address of Memory Block Accessed	Hit or Miss	Evicted Block	Contents of Cache Blocks After Reference			
			Set 0	Set 0	Set 1	Set 1
0	Miss		Memo[0]			
2	Miss		Memo[0]	Memo[2]		
4	Miss		Memo[4]	Memo[2]		
8	Miss		Memo[4]	Memo[8]		
10	Miss		Memo[4]	Memo[8]	Memo[10]	
12	Miss		Memo[12]	Memo[8]	Memo[10]	
14	Miss		Memo[12]	Memo[8]	Memo[14]	
16	Miss		Memo[16]	Memo[8]	Memo[14]	
0	Hit	1	Memo[0]	Memo[8]	Memo[14]	