

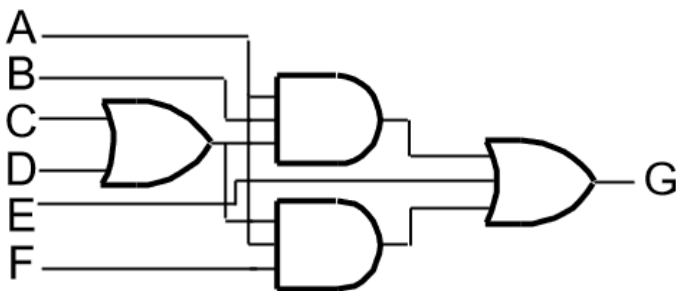
Homework 3

Due Date:3/8/2019

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Total Mark - 100

1. Design a combinational circuit that accepts a 4-bit number and generates a 3 –bit binary number output that approximates the square root of the number. If the square root is 3.5 or larger, give a result of 4. If less than <3.5 and >2.5, give the result of 3.
2. Design a circuit with a 4-bit BCD input A,B,C,D that produces an output W,X,Y,Z that is equal to the input +6 in binary. For example 9(1001)+6(0110)=15(1111). The output for invalid BCD codes are don't cares.
3. Perform technology mapping to (a) NAND and (b) NOR gates for the following circuit



4. Design a 5 to 32 line decoder using a 3 to 8 line decoder ,a 2 to 4 line decoder and 32 2 input AND gates.
5. Design a 4-input priority encoder with four inputs and three outputs including the valid bit but with the truth table representing the case in which input D₀ has the highest priority and input D₃ has the lowest priority.
6. A combinational circuit is defined by the two Boolean functions

$$F_1 = \overline{X + Z} + XYZ$$

$$F_2 = \overline{Y + Z} + XYZ$$

Design the circuit with a decoder and external OR gate.

7. A combinational circuit is defined by the following Boolean functions

$$F(A, B, C, D) = \sum m(0, 2, 3, 6, 10, 11, 15)$$

Design the circuit with a decoder and external OR gate.

8. Design a 16 to 1 line multiplexer using a 4 to 16 line decoder and a 16×2 AND OR.

9. Implement the following Boolean function with an 8 to 1 line multiplexer and a single inverter with variable D as its input.

$$F(A, B, C, D) = \sum m(2, 4, 6, 9, 10, 11, 15)$$

10. Find the truth table for the outputs F and G of the hierarchical circuit shown below.

