Homework 4_Solution

Total Mark - 100 (10+20+10+20+15+25)

1. Obtain the 1's and 2's complement of the following unsigned binary numbers: 10011100,10011101,10101000,10000000,10100010

Unsigned	10011100	10011101	10101000	10000000	10100010
1's	01100011	01100010	01010111	01111111	01011101
2's	01100100	01100011	01011000	10000000	01011110

2. Perform the following subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend:

(a) 11010 – 10001
(b) 11110 – 1110
(c) 1111110 – 1111110
(d) 101001 – 101

Unsigned	10001	01110	1111110	000101
1s	01110	10001	0000001	111010
2s	01111	10010	0000010	111011

a) 11010 + 01111 = 01001

b) 11110 + 10010 = 10000

c) 1111110 + 0000010 = 0000000

d) 101001 + 111011 = 100100

3. Perform the arithmetic operation in binary using signed 2's complement representation for negative numbers.

(a) (+36)+(-24)
(b) (-35)-(-24)

+36	=	0100100	36		0100100
- 24	=	1101000	+(–24)	+	1101000
- 35	=	1011101			10001100
			= 12	=	0001100
			–35		1011101
			- (–24)	+	0011000
			= –11	=	1110101

4. The following binary numbers have a sign in the leftmost position and if negative are in 2's complement form. Perform the indicated arithmetic and verify the answers.

(a) 100111+111001
(b) 001011+100110
(c) 110001 – 010010
(d) 101110 – 110111

Indicate whether overflow occurs for each computation.

a)

	100111	-25
+	111001	-7
	100000	-32

b)

	0010011	11
+	100110	-26
	110001	-15

Signed number	010010	110111
1s	101101	001000
2s	101110	110001

C) ` D)

110001	-15		101110	-18
101110	-18	+	001001	9
011111	-33		110111	-9
Overflow				

5. Design a combinational circuit whose input is a 4-bit number and whose output is the 2's complement of the input number.

A	B	C	D	E	F	G	H
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

$$H = D,$$
$$G = C \oplus D,$$
$$F = B'C + B'D + BC'D',$$
$$E = A'B + AB'C'D' + A'C + A'D$$

6. The adder and subtractor circuit of figure 1 has the following values for input select S and data input A and B

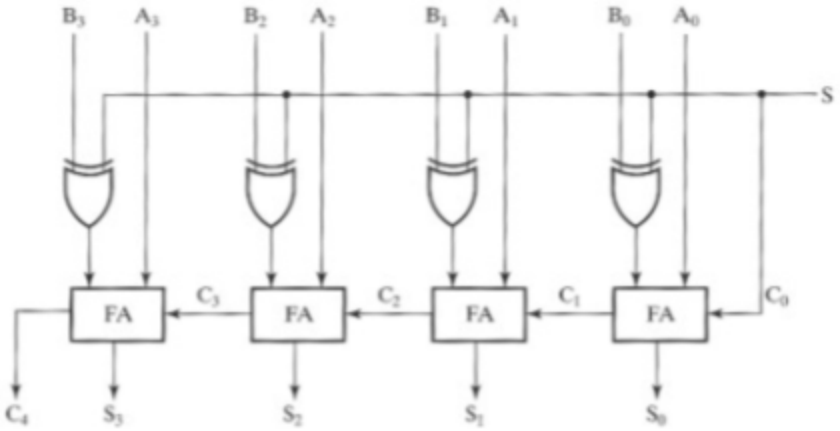

Figure 1: Adder subtractor circuit

S	A	B
a) 0	0111	0111
b) 1	0100	0111
c) 1	1101	1010
d) 0	0111	1010
e) 1	0001	1000

Determine, in each case, the values of the outputs S3, S2. S1, S0 and C4

S	A	B	C4	S3	S2	S1	S0
a)0	0111	0111	0	1	1	1	0
b)1	0100	0111	0	1	1	0	1
c)1	1101	1010	1	0	0	1	1
d)0	0111	1010	1	0	0	0	1
e)1	0001	1000	0	1	1	0	1