1. Design a combinational circuit that accepts a 3 bit number and generates a 6 bit binary output equal to the square of the input number

A	B	C	S5	S4	S3	S2	S1	S0	
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49

$$S0 = C,$$

$$S1 = 0,$$

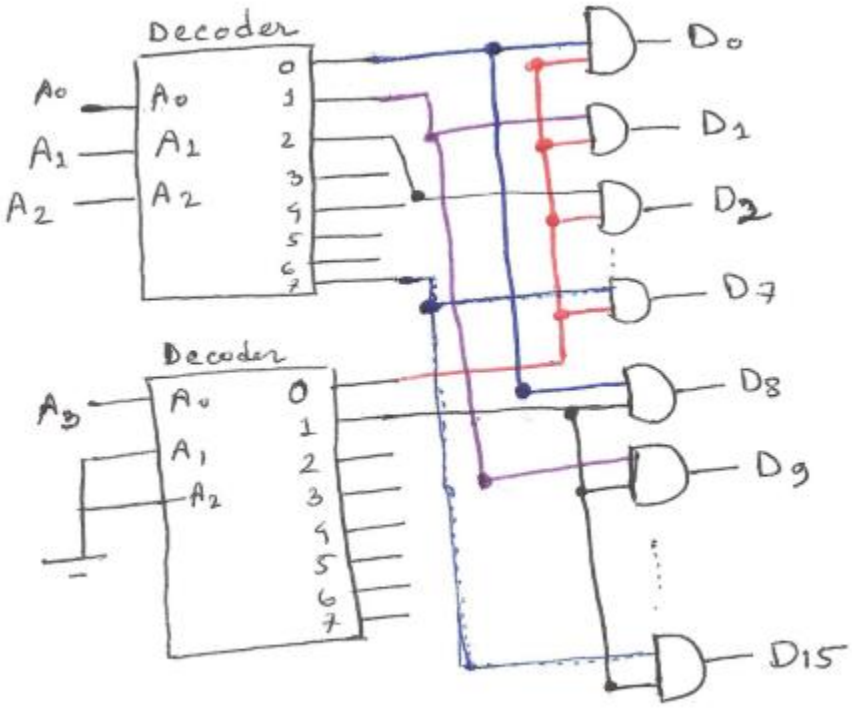
$$S2 = A'BC' + ABC' = BC',$$

$$S3 = A'BC + AB'C,$$

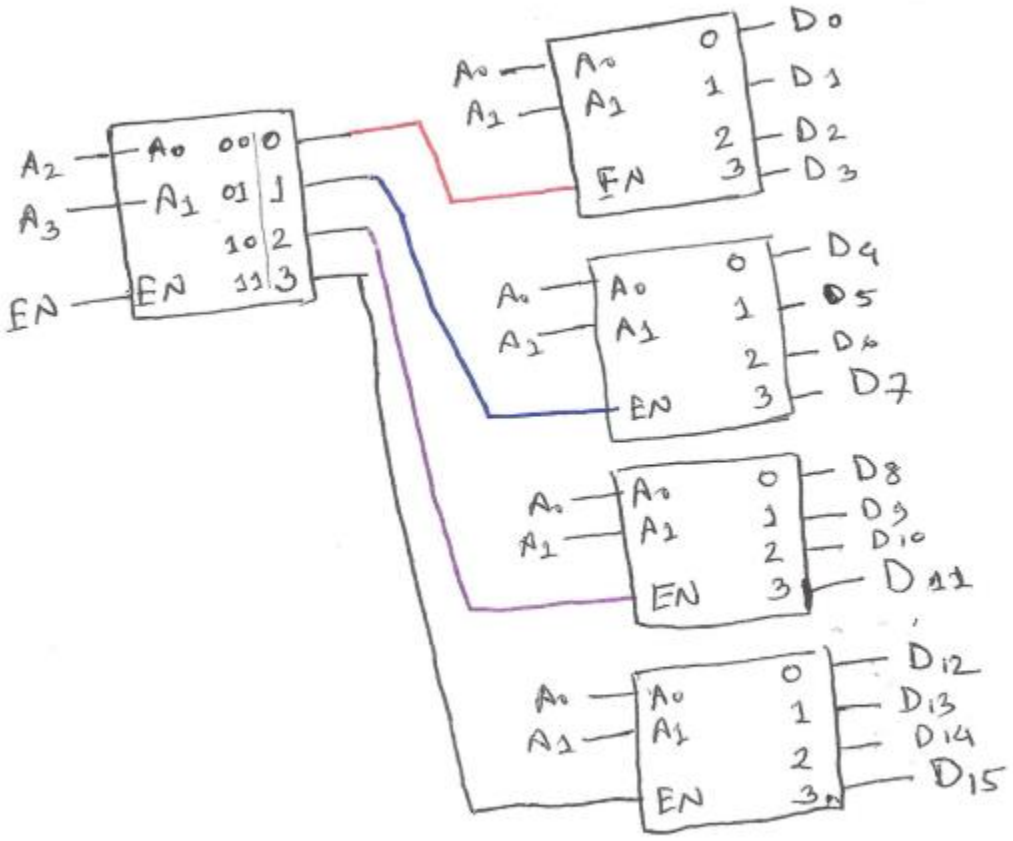
$$S4 = AB' + AC,$$

$$S5 = AB$$

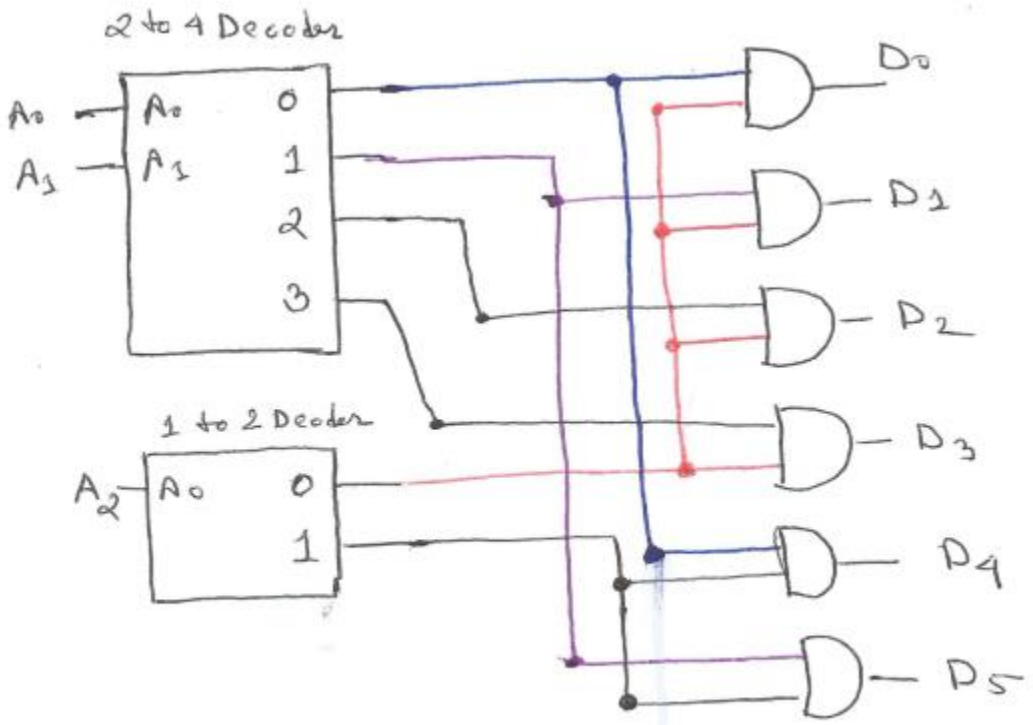
2. Design a 4 to 16 line decoder using two 3 to 8 line decoders and 16 2 input AND gates.



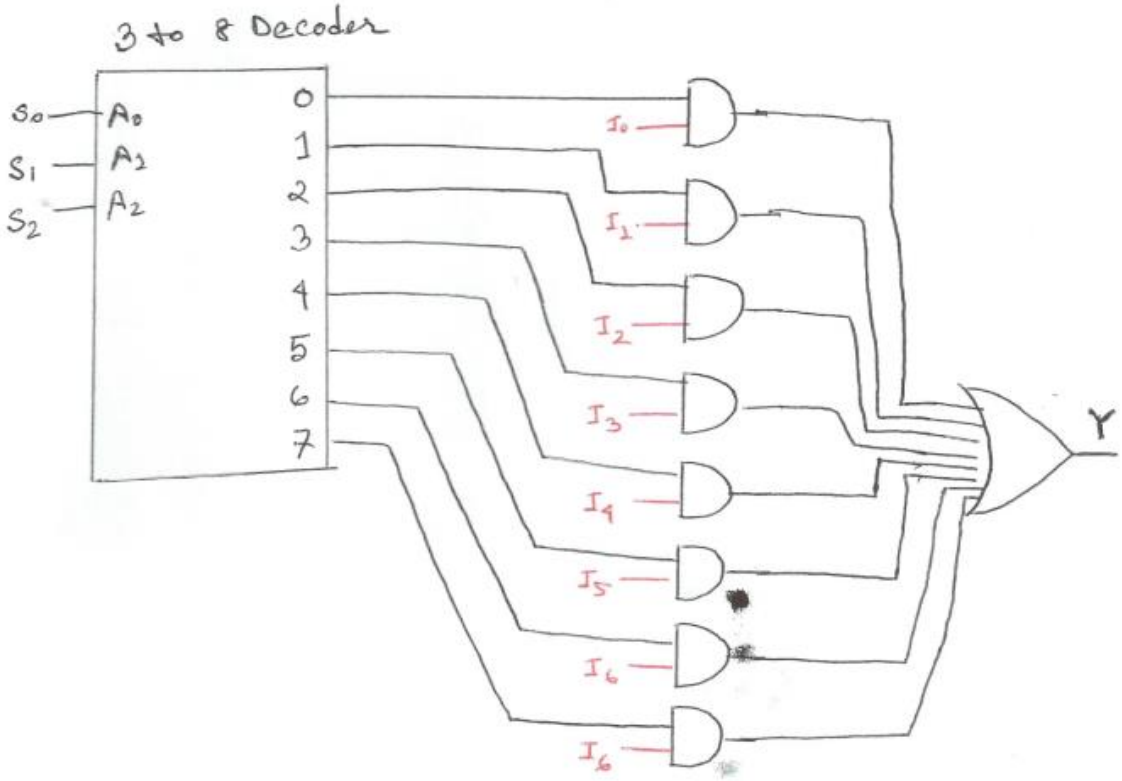
3. Design a 4 to 16 line decoder with enable using five 2 to 4 line decoders.



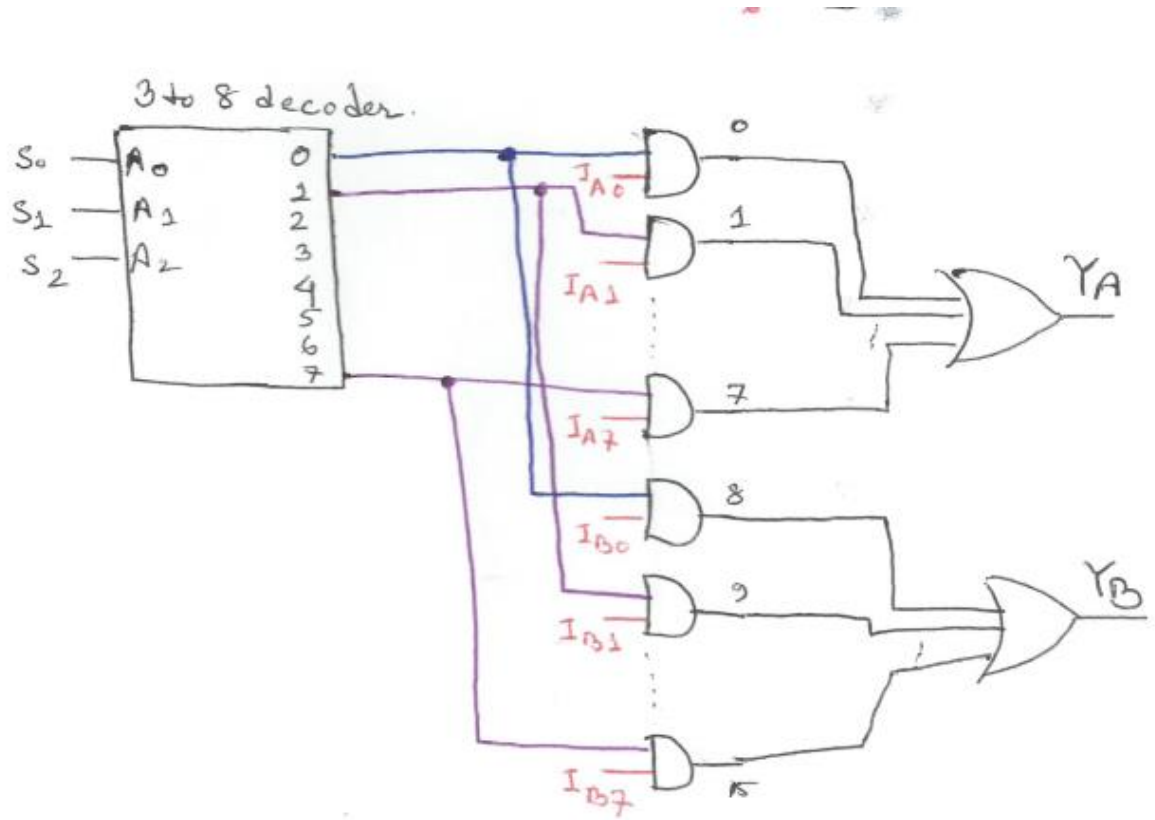
4. Design a 4 to 6 line decoder using a 2 to 4 line decoder and 1 to 2 line decoder



5. Design a (a)8 to 1 line multiplexer using a 3 to 8 line decoder and a 8 * 2 AND -OR.



6. Design a dual 8 to 1 line decoder using a 3 to 8 line decoder and a 16*2 AND-OR

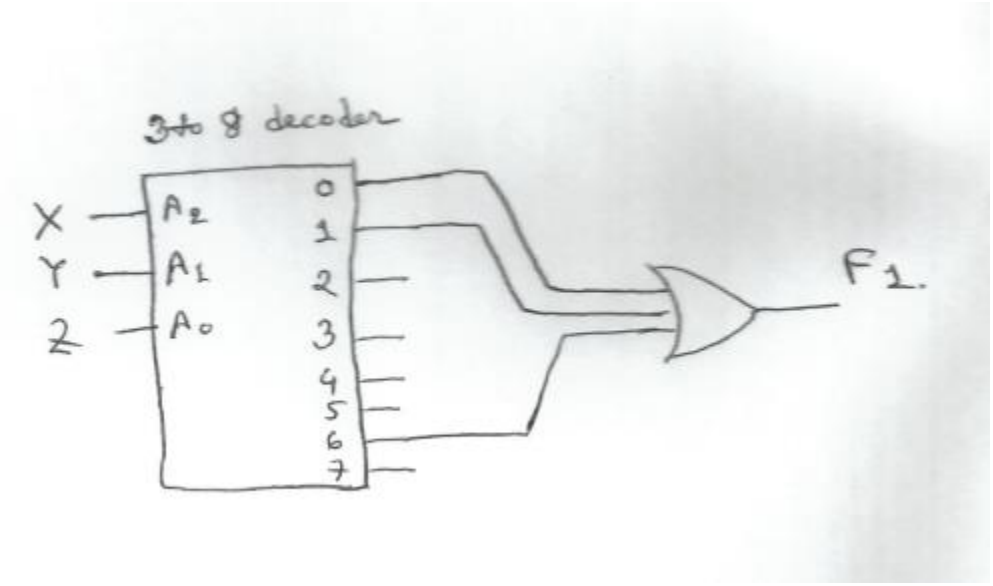


7. A Combinational circuit is defined by the following Boolean functions:

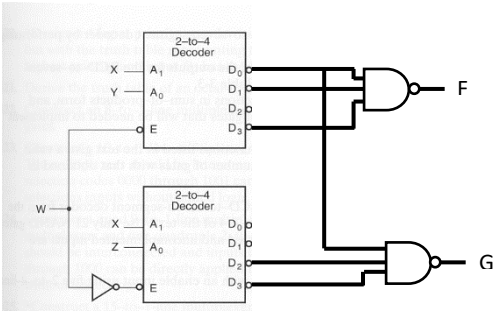
- F1(X, Y, Z) = X`Y` + XYZ`
- (i) Design the circuit with a 3x8 decoder, 2 2-input OR gates,

X	Y	Z	F1= X`Y` + XYZ`
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(i) $F_1 = \Sigma m(0,1,6)$



8. Find the truth table for the outputs F and G of the hierarchical circuit shown below



W	x	y	Z	F	G
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	0	1
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	0	1