FinFET NF parameter
&
MOS Parallel Reduction

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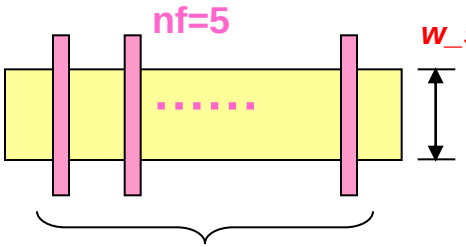
PDKD/TSMC

NF Handling in Model

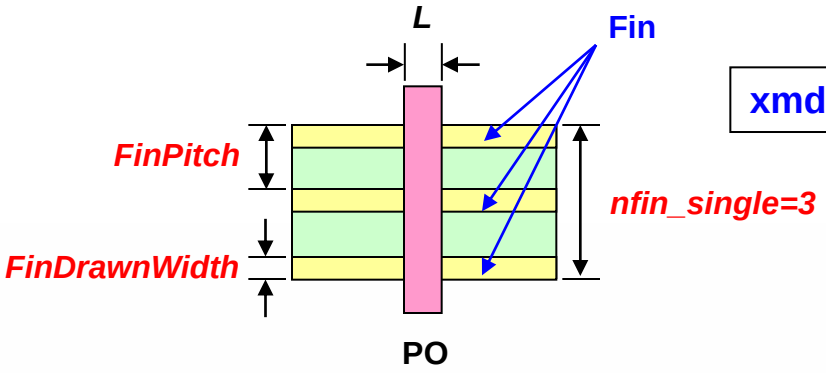
- **BSIM4 Planar Model (N20 and Before)**
  - The input instance ***w = w_total = nf * w_single***



xmdut d g s b nch_mac w=0.53u l=0.02u nf=5

w_total = nf * w_single = 5 * 0.106 = 0.53u

- **BSIMCMG FinFET Model (N10FF and N16FF)**
  - **The input instance is nfin.**
  - ***nfin = nfin_single*.**



xmdut d g s b nch_mac nfin=3 l=0.02u nf=5

FinFET NF Handling in LVS

- **nf can still be used in schematic under following constraints:**
  - **LVS will translate "nf" into equivalent "m" in schematic side.**
  - **LVS does not compare "nf" parameter.**

- **The equation of "nf-to-m" translation**

m' = m * nf

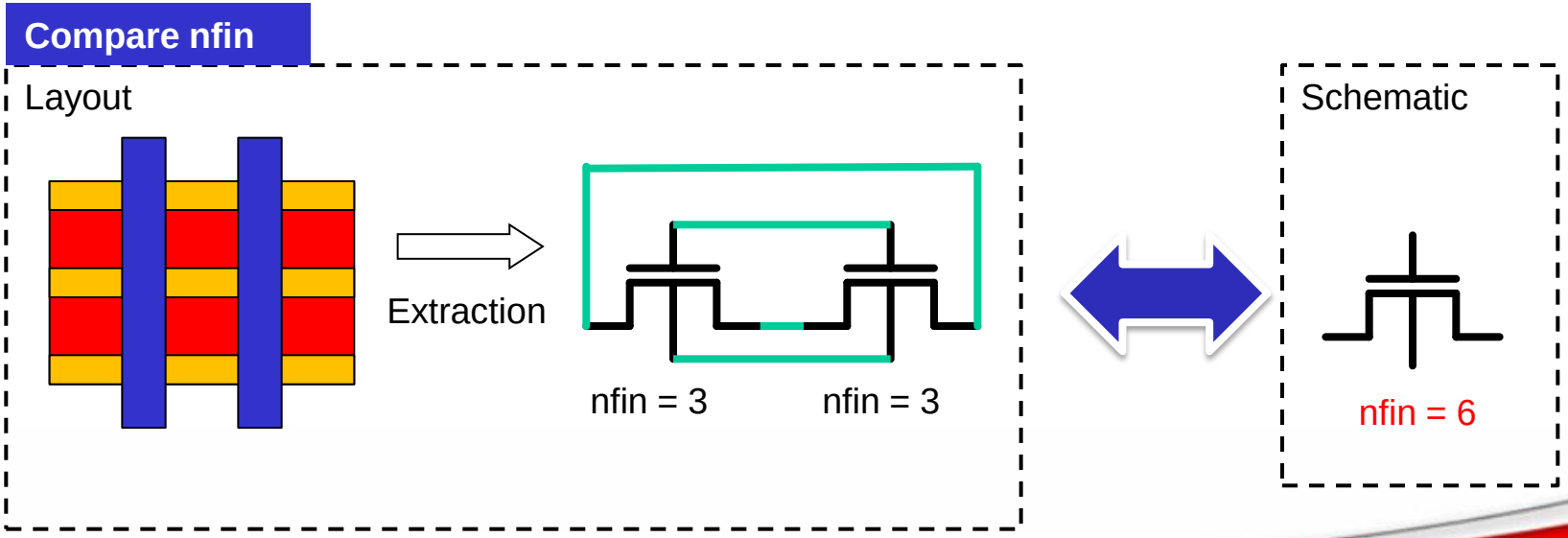
- **Example of nf-to-m:**

Original schematic:
M1 D G S B nch_svt_mac nfin=3 l=0.02e-6 nf=2 m=3

Translate nf to nfin during LVS execution:
M1 D G S B nch_svt_mac nfin=3 l=0.02e-6 m=6

FinFET MOS Parallel Reduction

- Redefine the behavior of parallel reduction for FinFET process.
- Redefined reduction function in the example below,
  - In layout side:
    - Two MOS with nfin=3 are extracted.
    - Sum up nfin = 6
  - In schematic side:
    - only one MOS with nfin=6.
  - LVS clean.



FinFET MOS Parallel Reduction (cont'd)

- Turn on the switch "LVS_REDUCE_PARALLEL_MOS" to enable MOS reduction function. Default is off.
- Only MOS with the same length could be reduced.
- Parallel reduction equation:

```
nfin  = sum( nfin )
l     = min(l)
```