# Unrecognized Device Checking

**LVSRCE/TSMC**

Sep/4, 2020

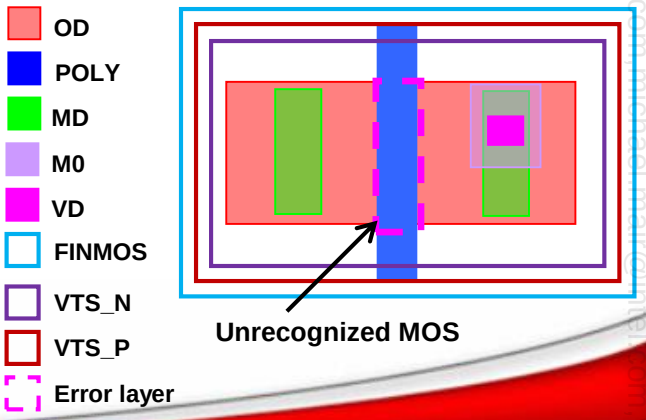
# Unrecognized MOS Methodology

- **Unrecognized device check is controlled by switch and default setting is off**
- **Recognized MOS**
  - **Follow truth table in DRM**

| Device | SPICE Name | Design Levels | | | | | | | | | | | | | | | | | | | | | | | | Special Layer | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | DNW | FinFET_Boundary_1 | OD | NW | NT_N | OD_12 | POLY | VTEL_N | VTEL_P | VTUL_N | VTUL_P | VTL_N | VTL_P | VTS_N | VTS_P | VTELN_LL | VTELP_LL | VTULN_LL | VTULP_LL | VTLN_LL | VTLP_LL | VTSN_LL | VTSP_LL | N+ | P+ | RH_TN | RHDMY_ALL | RHDMYn | NWDMY | VAR | IBJTDMY | DIODMY | SR_ESD | SDI | GATED | HIA_DUMMY | SDI_2 | MOMDMY |
| Std. Vt NMOS (0.75V) | nch_svt_mac | * | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | * | * | * | 0 | 0 | 0 | 0 | 0 | * | 0 | 0 | 0 | * |
| Std. Vt PMOS (0.75V) | pch_svt_mac | * | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | * | * | 0 | 0 | 0 | 0 | 0 | * | 0 | 0 | 0 | * |

- **Unrecognized MOS**
  - **realpo on diff(Valid OD) except following condition**
    - **All MOS gates (follow truth table) ➔ recognized MOS**
    - **SRAM region**
    - **NOD/NW or POD/PSUB ➔ pick-up**
    - **Passive devices(Diode/BJT)**
  - **Example**
    - **MOS with both VTS_N and VTS_P layers (Figure 1-1)**

**Figure 1-1**



# Unrecognized Passive Device Methodology(I)

- **Recognized Passive Device**
  - Passive devices include diode/BJT/Hi-R resistor/NW resistor
  - Follow truth table in DRM

| Device | SPICE Name | Design Levels | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Special Layer | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | DNW | FinFET_Boundary_1 | OD | NW | NT_N | OD_12 | POLY | VTEL_N | VTEL_P | VTUL_N | VTUL_P | VTL_N | VTL_P | VTS_N | VTS_P | VTELN_LL | VTELP_LL | VTULN_LL | VTULP_LL | VTLN_LL | VTLP_LL | VTSN_LL | VTSP_LL | N+ | P+ | RH_TN | RHDMY_ALL | RHDMYn | NWDMY | VAR | IBJTDMY | DIODMY | SR_ESD | SDI | GATED | HIA_DUMMY | SDI_2 | MOMDMY |
| iBJT PNP | pnp_i1_mac | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | * | * | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | * |
| (P+/NW/Psub) | pnp_i2_mac | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | * | * | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | * |

- **Unrecognized Diode Device**
  - Diff(valid OD) except following condition
    - recognized MOS gate
    - recognized diode
    - NOD/NW or POD/PSUB ➔ pick-up
    - SRAM region
    - SR-DOD
    - BJTDMY
  - Example
    - NOD with VTL_P layer (Figure 2-1)
- **Unrecognized BJT Device**
  - BJTDMY except following condition
    - recognized BJT ➔ BJTDMY with BJT body(emitter)
  - Example
    - BJTDMY with VTL_N layer (Figure 2-2)

Figure 2-1

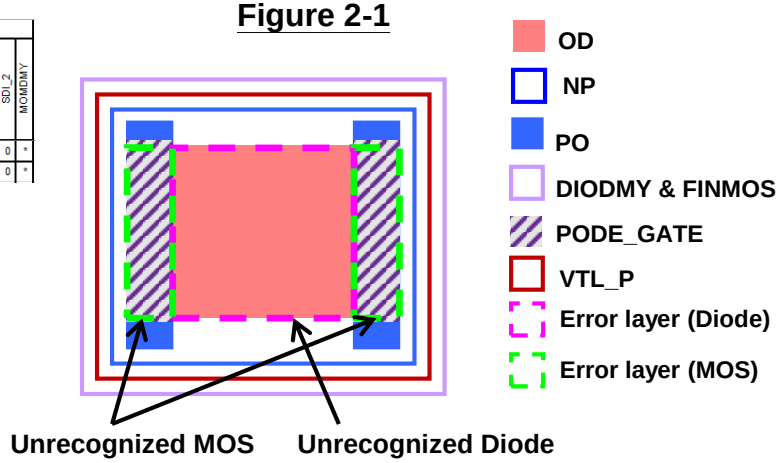
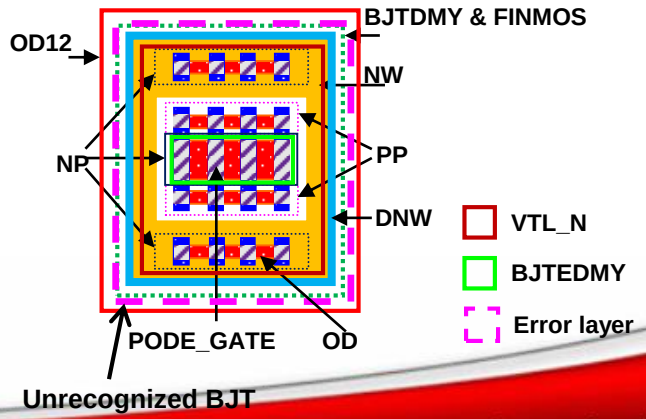



Figure 2-2



# Unrecognized Passive Device Methodology(II)

- **Unrecognized Hi-R Resistor Device**
  - **RHDMY except following condition**
    - **recognized 2T Hi-R resistor ➔ RHDMY with 2T Hi-R resistor body**
  - **Hi-R resistor body with VIA**
  - **Example**
    - **RHDMY with VIA layer (Figure 3)**

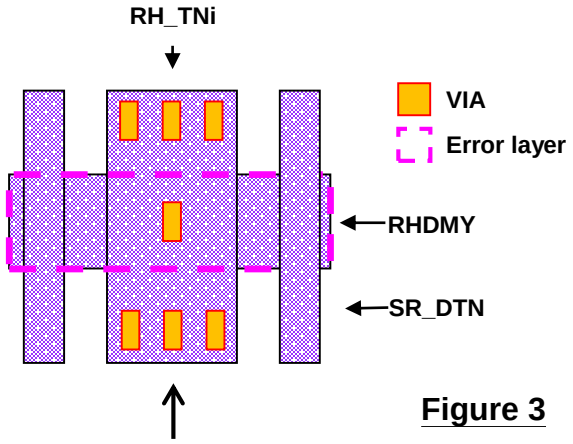



Figure 3