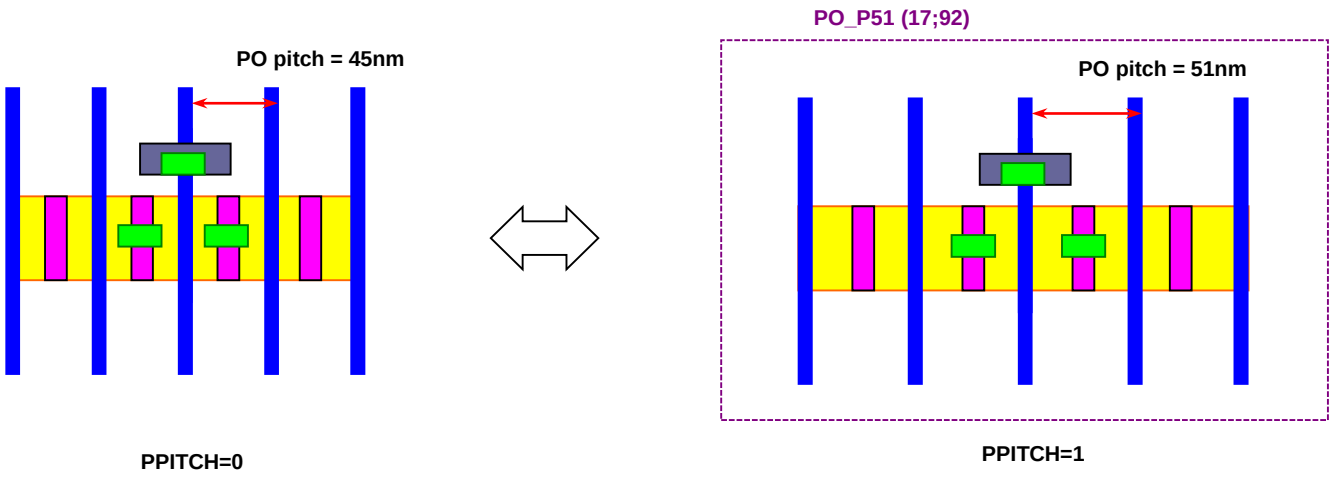
N3 Set “ppitch” As Trace Property

LVSRCE/TSMC

September 4, 2020

ppitch

- "ppitch" instance parameter extraction is based on PO_P51(17;92)
- Set "ppitch" as trace property
- All core MOS devices in source netlist have to have "ppitch" parameter for LVS comparision.



Switches Settings

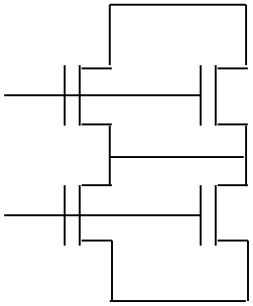
- **LVS_REDUCE_PARALLEL_MOS switch**
  - Turn on this switch to enable MOS parallel reduction function.
  - For core MOS, “PPITCH” , and “L” need to be the same to enable reduction.
  - For other MOS, “L” need to be the same to enable reduction.
  - This switch default is OFF
- **LVS_REDUCE_SPLIT_GATES switch**
  - Turn on this switch to enable MOS simple split gate reduction function.
  - This switch default is OFF.

MOS Parallel Reduction Cases

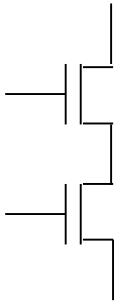
(Turn on LVS_REDUCE_PARALLEL_MOS)

- Core case1: Same ppitch value for reduction

nfin=2
l=3n
ppitch=0
for 4 devices



After reduction

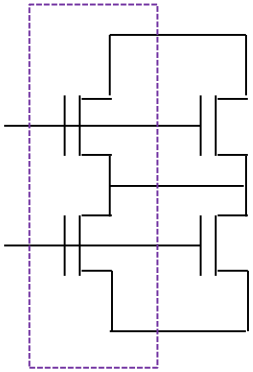


nfin=4
l=3n
ppitch=0
for both 2 devices

- Core case2: Different ppitch values will not reduce

nfin=2
l=3n
ppitch=1
for 2 devices

PO_P51



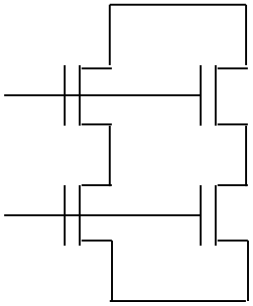
nfin=2
l=3n
ppitch=0
for 2 devices

Will NOT reduce

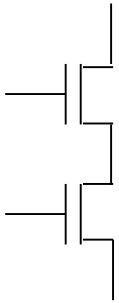
Split Gate Reduction Cases
(Turn on LVS_REDUCE_SPLIT_GATES)

- **Core case1: Same ppitch value for reduction**

nfin=2
l=3n
ppitch=0
for 4 devices



After reduction

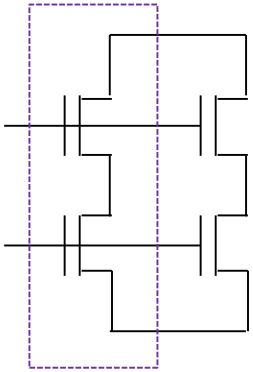


nfin=4
l=3n
ppitch=0
for both 2 devices

- **Core case2: Different ppitch values will not reduce**

PO_P51

nfin=2
l=3n
ppitch=1
for 2 devices



nfin=2
l=3n
ppitch=0
for 2 devices

Will NOT reduce