ERC Usage

LVSRCE/TSMC

2022/01/28

What is ERC (Electrical Rule Checking)

- ERC is a special option for designers. Some errors can be waived, but others may be fatal errors. So, designers must review every error or warning in LVS/ERC report.
- ERC rules included in TSMC official LVS command files are:
  - Soft connect checking
  - Path checking
  - ptap/ntap checking
  - MOS S/D power&ground checking
  - Gate directly connecting to power or ground checking
  - Floating well checking
- ERC report and database are “~.erc.sum” and “~.erc.db” separately.

ERC Report

Get ERC report at LVS stage

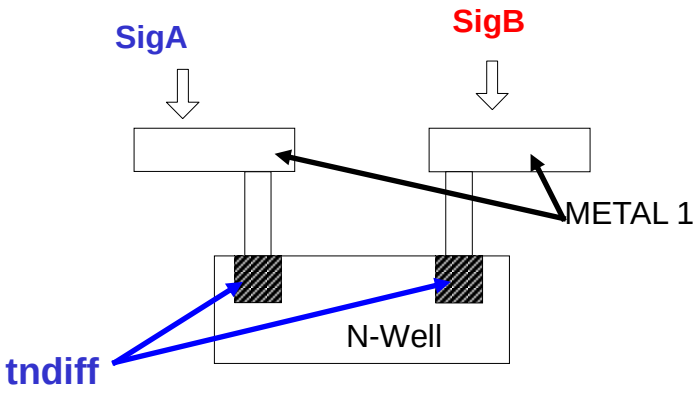
Calibre :

% calibre -lvs -hier -spi layout.net calibre_rule_deck

Check “calibre_erc.db” and “calibre_erc.sum” files

Soft connect and soft check

- **N-well and P-well are high resistor materials**



1. Treat as Short
   Sig A connect to Sig B
➔ If Sig A is a power line and Sig B connects to a IP power, the IP gets a high resistor power but IR drop is very serious.
➔ **ERROR**

2. Treat as open
   Sig A does not connect to Sig B
➔ If Sig A is a power signal and sig B is ground signal, power and ground shorts
➔ **ERROR**

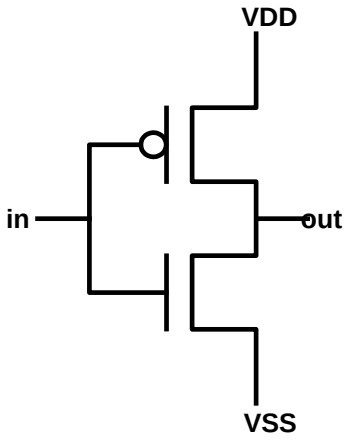
- **Use soft connect and soft check to highlight the case**

What is soft connect and soft checking ?

- **Sconnect definition**
  - **Pass established connectivity from the upper layer polygons onto specified lower layer polygons (unidirectional) < calibre manual>**
- **Softchk**
  - **Help designers to search which contact connects to Well**
- **ERC result**
  - **Please confirm each error and warning reported in lvs.rep and lvs.rep.ext.**
  - **Users can debug this error by using “calibre -rve” to open svdb/ file.**

Path Checking

- **Purpose**
  - Report nodes without a path to top-level power, ground, or pin.
- **Four Kinds of Path Checking**
  - Nodes with a path to power but not ground
  - Nodes with a path to ground but not power
  - Nodes without a path to both power and ground
  - Nodes without a path to pin

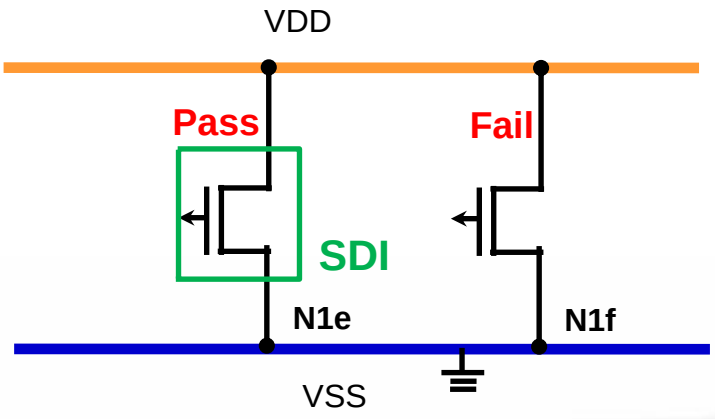


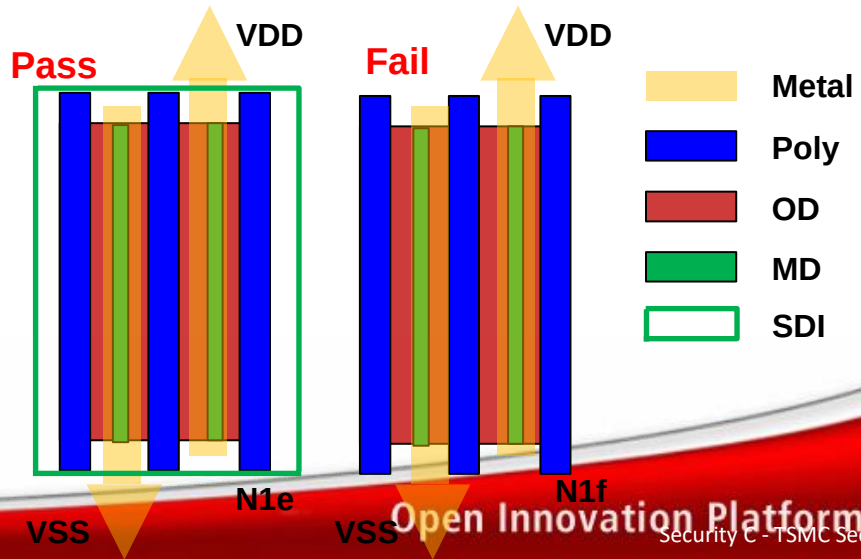
Well to power & ground checking

- **Purpose**
  - Check whether nwell connects to ground or psub connects to power.
- **Checking scope**
  - ERC “PPVDD49” for PTAP connected to power.
    - Except TCDDMY/ICOVL
  - ERC “NPVSS49” for NTAP connected to ground.
    - Except VAR/BJTDMY

MOS S/D power & ground checking

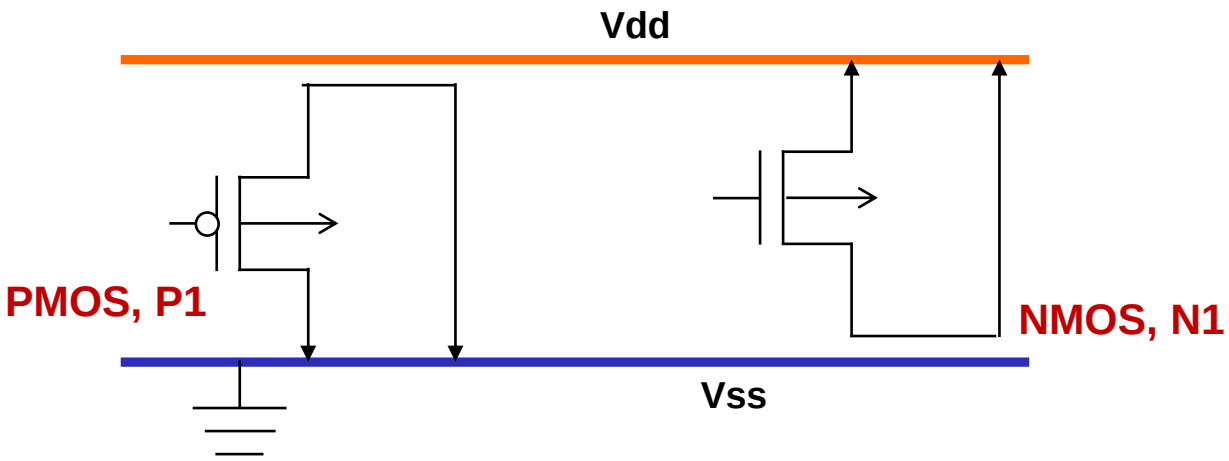
- For N/P MOS, one of source/drain connects to POWER and the other connects to ground
  - Check ERC error “mppg” for PMOS
  - Check ERC error “mnpg” for NMOS
- Exceptions: (only for mnpg/mppg)
  - If N/PMOS have SDI layer covered, they would be excluded from this checking since they are ESD power clamps
  - This exception isn’t applied to mnpg-ldd checking





Special MOS LUP Check (1/7)

- For NMOS, source and drain directly connect to Power
  - Check ERC violation “mnpp/mnpp_mpode”
- For PMOS, source and drain directly connect to Ground
  - Check ERC violation “mpgg/mpgg_mpode”

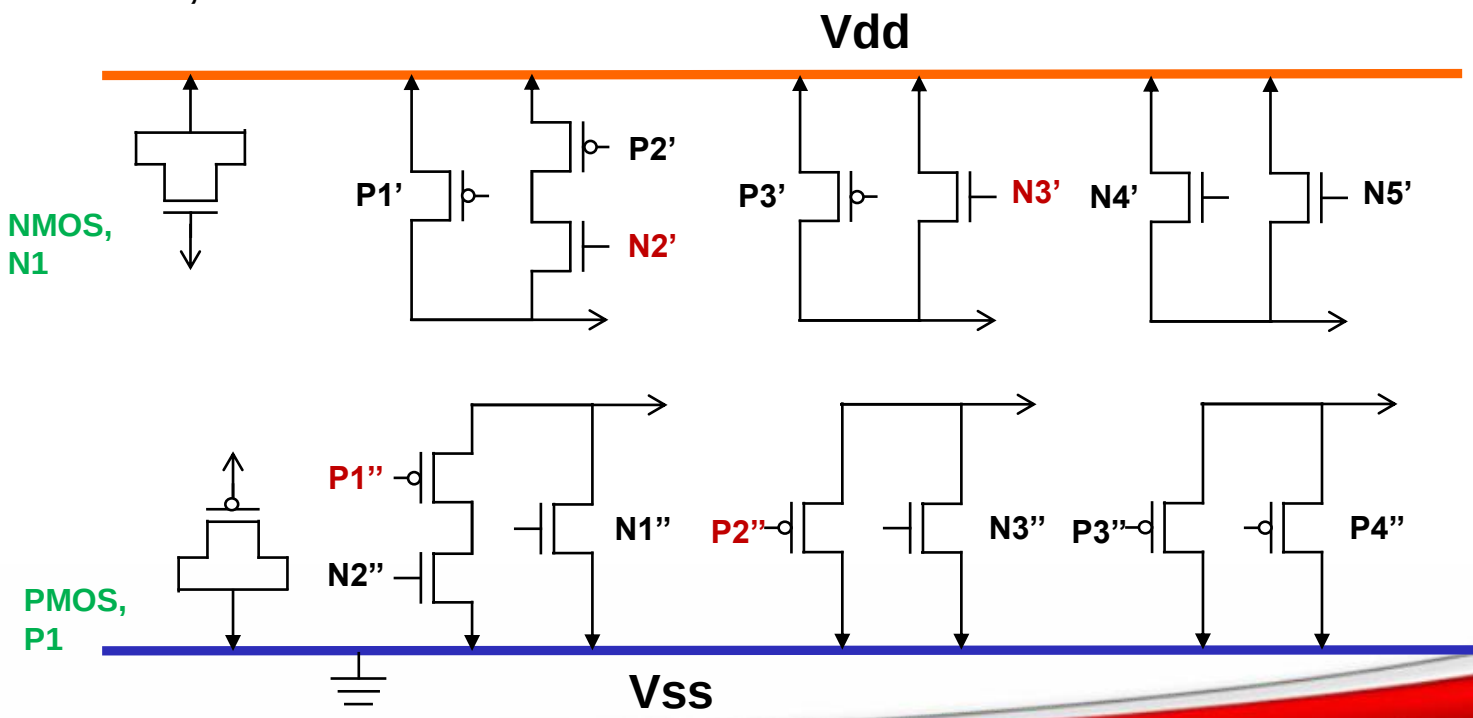


Special MOS LUP Check (2/7)

- **Definition of Virtual Power**
  - **Switch "MNPP_MPGG_VIRT_PWR_ENABLE" //Enable virtual power recognition for mnpp* and mpgg* ERC check**
    - **When switch ON, ERC flag on:**
      - **NMOS source and drain directly connect to power (mnpp*)**
      - **NMOS source and drain connect to virtual power (mnpp*)**
        - » Virtual power = internal nets with net information propagated from real power net through single stage PMOS s/d
      - **PMOS source and drain directly connect to ground (mpgg*)**
      - **PMOS source and drain connect to virtual ground (mpgg*)**
        - » Virtual ground = internal nets with net information propagated from real ground net through single stage NMOS s/d
      - **Notes: When virtual power/virtual ground propagated to same net as real ground/real power, the specific net is recognized as real ground/power.**
    - **When switch OFF, ERC flag on:**
      - **NMOS source and drain directly connect to power (mnpp*)**
      - **PMOS source and drain directly connect to ground (mpgg*)**
    - **Gate connection: don't care**
    - **Bulk connection: don't care**

Special MOS LUP Check (3/7)

- Below scheme flag by ERC
  - When “MNPP_MPGG_VIRT_PWR_ENABLE” switch ON, ERC flag on:
    - N1, N2’, N3’, P1, P1”, P2”
  - When “MNPP_MPGG_VIRT_PWR_ENABLE” switch OFF, ERC flag on:
    - N1, P1



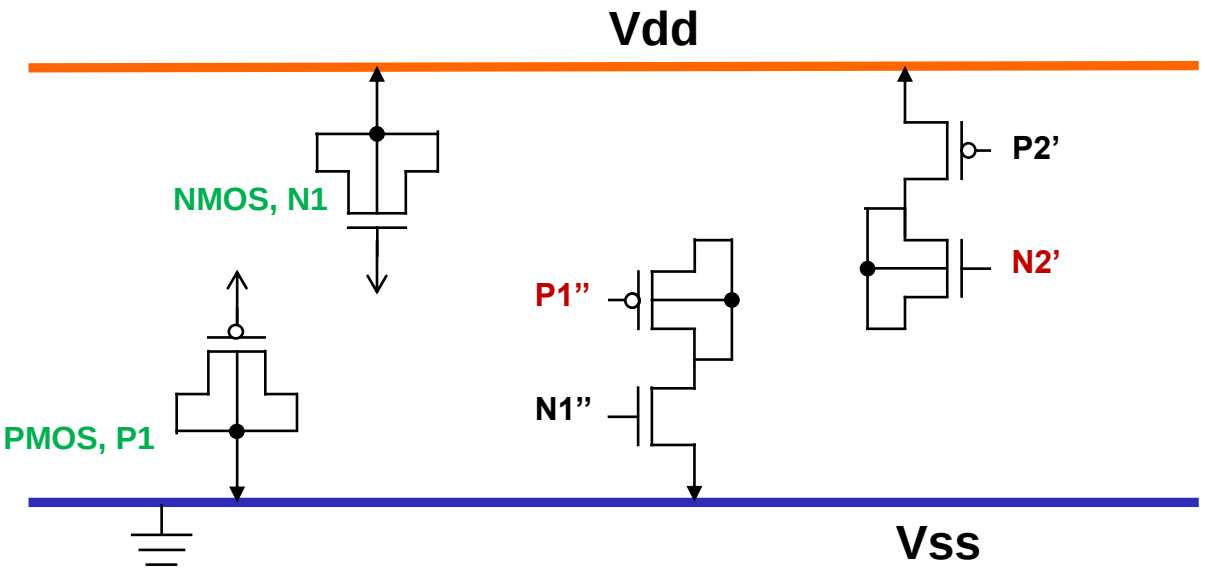
Special MOS LUP Check (4/7)

- LVS ERC rules switch

Switch	Virtual power switch (MNPP_MPGG_VIRT_PWR_ENABLE)	mnpp, mpgg,	mnpp_mpode, mpgg_mpode,
Regular MOS OFF (REGMOS_MNPP_MPGG_CHECK)	ON or OFF (does not matter)	Do NOT check	
MPODE OFF (MPODE_MNPP_MPGG_CHECK)			
Regular MOS ON (REGMOS_MNPP_MPGG_CHECK)	OFF	Check if connected to real power	n/a
MPODE ON (MPODE_MNPP_MPGG_CHECK)		n/a	Check if connected to real power
Regular MOS ON (REGMOS_MNPP_MPGG_CHECK)	ON	Check if connected to real or virtual power	n/a
MPODE ON (MPODE_MNPP_MPGG_CHECK)		n/a	Check if connected to real or virtual power

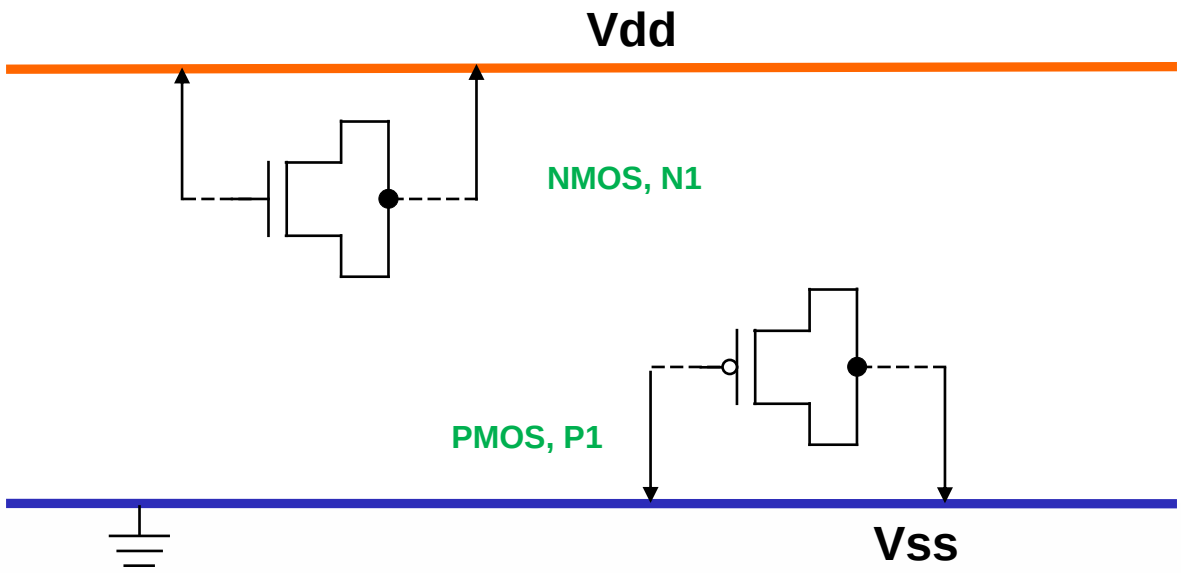
Special MOS LUP Check (5/7)

- **Additional Exceptions 1:**
  - **S/D/B tied together at same net (don't care for gate connection)**
    - **N1, N2', P1, P1" are exempted.**



Special MOS LUP Check (6/7)

- **Additional Exceptions 2:**
  - **IO N/PMOS [covered by OD2] is excluded from rule check**
- **Additional Exceptions 3:**
  - **S/D/G tied together at same net (don't care for bulk connection)**
    - **N1, P1 are exempted.**



Special MOS LUP Check (7/7)

- **Recommended ERC Switch Settings**

ERC switch	Switch Description	Default setting	Recommended setting
MNPP_MPGG_VIRT_PWR_ENABLE	Turn on to enable virtual power recognition for mnpp and mpgg related check	Disable	Disable
REGMOS_MNPP_MPGG_CHECK	Perform mnpp and mpgg related check for all MOS devices	Enable	Enable
MPODE_MNPP_MPGG_CHECK	Perform mnpp and mpgg related check for MPODE device which is covered by PODE_GATE(206;28) layer	Enable	Enable

Gate directly connects to power/ground

- **Flagged conditions:**
  - **The core voltage MOS gate (OD only; not OD_12) directly connects to Power and either source or drain directly connects to Ground.**
  - **The core voltage MOS gate (OD only; not OD_12) directly connects to Ground and either source or drain directly connects to Power.**
- **Exceptions:**
  - **Decoupling capacitor: source/drain/bulk directly connects to Power (GND) and gate directly connects to GND (Power).**
  - **GGNMOS/GDPMOS across power-ground:**
    - **GGNMOS case: Gate, bulk, and either drain or source directly connect to ground while the leftover drain or source directly connects to power.**
    - **GDPMOS case: Gate, bulk, and either drain or source directly connect to power while the leftover drain or source directly connects to ground.**

Floating Well Check

- No power connecting to NWELL
  - Highlight nwell which has no path to power
  - Check ERC error “floating.nxwell” for NWELL
- No ground connecting to PSUB
  - Highlight psub which has no path to ground
  - Check ERC error “floating.psub” for PSUB
- No POWER or GROUND signal in the layout might abort this check.
  - For example, the following messages means no POWER nets present in the layout and ERC “floating.nxwell_float” doesn’t function at all.

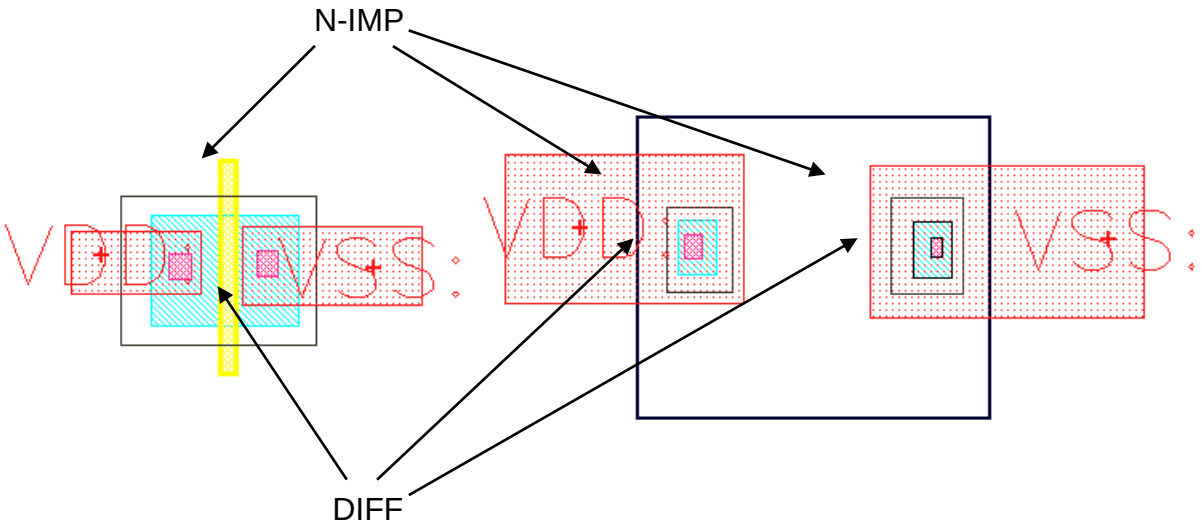
lvs.rep.ext

```
WARNING: Invalid PATHCHK request "! POWER": no POWER nets present, operation aborted.
```

erc.sum

```
RULECHECK floating.nxwell_float ... TOTAL Result Count = 0 (0) FAILED PATHCHK IN LAYER DERIVATION
```

Layout Example



~.sum

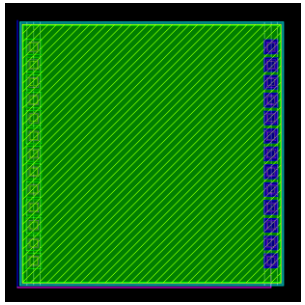
```
------------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK mppg .... TOTAL Result Count = 1
RULECHECK mnpg .... TOTAL Result Count = 0
RULECHECK ppvdd49 ... TOTAL Result Count = 0
RULECHECK npvss49 ... TOTAL Result Count = 1
------------------------------------------------------------------------
```

~.ext

WARNING: Stamping conflict in SCONNECT - Multiple source nets stamp one target net.
Use LVS REPORT OPTION S or LVS SOFTCHK statement to obtain detailed information.

ERC : Unexpected SHDMIM device

- **ERC : UnexpectedDev.SHDMIM**
  - **Purpose : To highlight SHDMIM device in the layout**
  - **Switch : unexpected_device_checking_SHDMIM (default is ON)**
- **Usage for LVS**
  - **Suggest to turn on this switch when there is no shdmimcap in RC techfile**
- **Example :**
  - **A SHDMIM device in the layout**

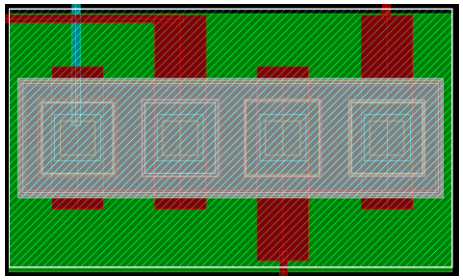


  - **ERC report**

```
RULECHECK UnexpectedDev.SHDMIM .... TOTAL Result Count = 1 (1)
```

ERC : Unexpected SHPMIM client device

- **ERC : UnexpectedDev.SHPMIM_client**
  - **Purpose : To highlight SHPMIM client device in the layout**
  - **Switch : unexpected_device_checking_SHPMIM_client (default is ON)**
- **Usage for LVS**
  - **Suggest to turn on this switch when there is no shpmimcap client in RC techfile**
- **Example :**
  - **A SHPMIM client device in the layout**

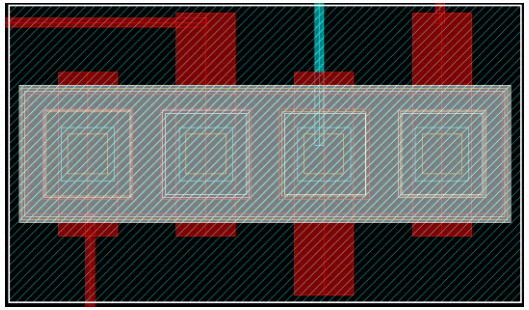


  - **ERC report**

```
RULECHECK UnexpectedDev.SHPMIM_client ... TOTAL Result Count = 1   (1)
```

ERC : Unexpected SHPMIM server device

- **ERC : UnexpectedDev.SHPMIM_server**
  - **Purpose : To highlight SHPMIM server device in the layout**
  - **Switch : unexpected_device_checking_SHPMIM_server (default is ON)**
- **Usage for LVS**
  - **Suggest to turn on this switch when there is no shpmimcap server in RC techfile**
- **Example :**
  - **A SHPMIM server device in the layout**



  - **ERC report**

```
RULECHECK UnexpectedDev.SHPMIM_server ... TOTAL Result Count = 1   (1)
```

Summary for ERC Checker

- Please confirm every error or warning of these three files: “~.rep”, “~.rep.ext” and “svdb/~.rep” for Calibre
- Every soft connect error must be fixed
- Other ERC errors/warnings need to be reviewed by circuit designers