# N3 Calibre LVS/LPE Deck Usage

## LVSRCE/TSMC

Jan. 28, 2022

# Contents

- Switches and Variables Setting
- Runset Options
- Calibre LVS/xACT Flow
- Calibre/StarRCXT LVS/CCI Flow

# Switches and Variables Setting

# Calibre Switches(I)



- **#define RC_DFM_RULE – Calibre Flow**
  - Turn on this switch for Calibre XACT extraction with DFM effect.
  - For MOS devices, the DFM effect parameters will be extracted.
- **#define CCI_DFM_RULE – CCI Flow**
  - Turn on this switch for Calibre+StarRCXT extraction with DFM effect in CCI deck.
  - For MOS devices, the DFM effect parameters will be extracted.
- **#define LVS_DECK – CCI Flow**
  - Turn on this switch for Calibre LVS check in CCI deck.

# Calibre Switches(II)

- **#define FILTER_DGS_TIED_MOS (Recommend to turn off)**
  - Turn on this switch to filter drain, gate and source tied MOS devices.
  - Turn off it to filter all pins tied MOS devices.
- **#define NW_RING**
  - Turn on this switch to enable NW ring to separate the node from BULK.
  - Not recommend to turn on because from process's point of view BULK cannot be fully separated by NW ring
- **#define WELL_TEXT**
  - Turn on this switch to enable NW/PSUB text to be well pins.
  - **DO NOT turn on this switch for full-chip checking.**
- **#define FILTER_PODE**
  - Turn off to compare PODE device, default will filter both layout and source PODE device at LVS comparison stage
- **#define FILTER_MPODE**
  - Turn off to compare MPODE device, default will filter both layout and source MPODE device at LVS comparison stage
- **#define LVS_REDUCE_PARALLEL_MOS**
  - Turn on this switch to enable MOS reduction function.
- **#define LVS_REDUCE_PARALLEL_MIMCAP**
  - Turn on this switch to enable SHDMIMCAP reduction function.

# Calibre Switches(III)



- **#define extract_dnwpsub**
  - Turn on to extract parasitic dnw/pub diode
- **#define extract_pwdnw**
  - Turn on to extract parasitic rw/dnw diode
- **#define extract_pnwdio**
  - Turn on this switch to extract parasitic NW-PSUB diodes, and this device will not be compared

# Calibre Switches(IV)

- **#define LVS_REDUCE_SPLIT_GATES**
  - Turn on this switch to enable MOS split gate reduction .
  - This switch default is OFF.
- **#define MATCHFLAG**
  - Turn on to extract matchingflag and edgeflag for high sensitivity mismatching design
- **#define FLICKER_CORNER_EXTRACTION**
  - Turn on to enable flicker corner extraction
- **/#define SELF_HEATING_EFFECT_EXTRACTION**
  - Turn on to enable self heating effect extraction.
- **#define SKIP_ODSE**
  - Turn on this switch to skip OD space effect.
- **#define SKIP_XVTMBE**
  - Turn on this switch to skip Mixed VT MBE effect
- **#define SKIP_LPCCN**
  - Turn on this line to skip LOD/PXE/CPO/CPODE/NPB effect
- **#define PARAMETERIZED_CPODE**
  - Turn on this switch to enable parameterized_cpode extraction

# Calibre Switches(V)

- **About ERC rule switches at LVS stage:**
  Following are the switches for important ERC checking rules, and we have suggestion for default on or off.
  - **#define WELL_TO_PG_CHECK**
    - Default is on. Turn on to highlight if nwell connects to ground or psub connects to power.
  - **#define GATE_TO_PG_CHECK**
    - Default is off. Turn on to highlight if a mos gate directly connects to power or ground.
  - **#define PATH_CHECK**
    - Default is off. Set on to highlight if
      - nodes have a path to power but no path to ground
      - nodes have a path to ground but no path to power
      - nodes have no path to power or ground
      - nodes have no path to any label net
  - **#define DS_TO_PG_CHECK**
    - Default is on. Turn on to highlight if drain connects to power and source connects to ground.
  - **#define FLOATING_WELL_CHECK**
    - Default is off. Turn on to highlight if well does not connect to power or ground.
    - Exclude the nwell of moscap, nwell-resistor terminals and nwell regions covered by TCDDMY(165;1) / ICOVL(165;320) layers.

# Calibre Switches(VI)

- **About ERC rule switches at LVS sate:**
  Following are the switches for important ERC checking rules, and we have suggestion for default on or off.
  - **#define PICKUP_CHECK**
    - Default is on. Turn on to highlight if dummy pickup of separate WELL are connected in LVS stage.
    - Please refer to “N3_ERC_PICKUP_CHECK.pdf”
  - **#define PSUB2_ERC_CHECK**
    - Default is on. Turn off to disable SR_DOD cut PSUB2 checking
  - **#define MNPP_MPGG_VIRT_PWR_ENABLE**
    - Default is off. Turn on to enable virtual power recognition for mnpp and mpgg related check
  - **#define MNPP_MPGG_LAYER_WAIVER_ENABLE**
    - Default is off. Turn on to  enable LUPVTWDMY cad
  - **#define REGMOS_MNPP_MPGG_CHECK**
    - Default is on. Perform mnpp and mpgg related check for all MOS devices
  - **#define MPODE_MNPP_MPGG_CHECK**
    - Default is on. Perform mnpp and mpgg related check for MPODE device which is covered by PODE_GATE(206;28) layer
  - **#define METAL_MAIN_CHECK**
    - Default is on. Turn on to highlight if the layout has non-color main metal layer

# Calibre Switches(VII)

- **About ERC rule switches at LVS stage:**
  Following are the switches for important ERC checking rules, and we have suggestion for default on or off.
  - **#define unrecognized_device_checking**
    - Default is off
    - Turn on this line to do unrecognized device checking
  - **#define unexpected_device_checking_SHDMIM**
    - Turn off this line to disable unexpected SHDMIM device checking
  - **#define unexpected_device_checking_SHPMIM_server**
    - Turn off this line to disable unexpected server-type SHPMIM device checking
  - **#define unexpected_device_checking_SHPMIM_client**
    - Turn off this line to disable unexpected client-type SHPMIM device checking
  - **#define LVSDMY4_CHECK**
    - Default is on.
    - The LVSDMY4 layer is used in LVS deck to identify logic N-Type MOS within the DNW only. Not recommend that LVSDMY4 layer is used without DNW layer

# Calibre Switches Overview (I/III)



| SWITCH NAMES | Default | IP | FULL CHIP | COMMENT |
|---|---|---|---|---|
| LVS_DECK | YES | YES | YES | regard deck as a LVS command file |
| CCI_DFM_RULE | NO | NO | NO | regard deck as a DFM CCI command file |
| SKIP_ODSE | NO | NO | NO | skip ODSE extraction |
| FILTER_DGS_TIED_MOS | NO | NO | NO | filter MOS with D, G and S tied together |
| WELL_TO_PG_CHECK | YES | YES | YES | highlight nwell connecting to ground or psub connecting to power |
| GATE_TO_PG_CHECK | NO | NO | NO | highlight mos gate directly connecting to power or ground |
| PATH_CHECK | NO | NO | NO | (1) nodes have a path to power but no path to ground<br>(2) nodes have a path to ground but no path to power<br>(3) nodes have no path to power or ground<br>(4) nodes have no path to any label net |
| DS_TO_PG_CHECK | YES | YES | YES | highlight drain connecting to power and source connecting to ground |
| FLOATING_WELL_CHECK | YES | YES | YES | highlight well not connecting to power or ground |
| LVSDMY4_CHECK | YES | YES | YES | highlight LVSDMY4 not in DNW region but interacting NMOS |
| NW_RING | NO | NO | NO | enable NW isolation ring |
| unrecognized_device_checking | NO | NO | NO | unrecognized device check |

# Calibre Switches Overview (II/III)



| SWITCH NAMES | Default | IP | FULL CHIP | COMMENT |
|---|---|---|---|---|
| PICKUP_CHECK | YES | YES | YES | dummy pickup check |
| MNPP_MPGG_VIRT_PWR_ENABLE | NO | NO | NO | enable virtual power recognition for mnpp and mpgg |
| MNPP_MPGG_LAYER_WAIVER_ENABLE | NO | NO | NO | enable LUPVTWDMY cad layer waiver for mnpp and mpgg |
| REGMOS_MNPP_MPGG_CHECK | YES | YES | YES | mnpp and mpgg check for all MOS devices |
| MPODE_MNPP_MPGG_CHECK | YES | YES | YES | mnpp and mpgg check for MPODE devices |
| WELL_TEXT | NO | NO | NO | enable well pin |
| SKIP_XVTMBE | NO | NO | NO | skip XVTMBE |
| SKIP_LPCCN | NO | NO | NO | skip LOD/PXE/CPO/CPODE/NPB |
| FILTER_PODE | YES | YES | YES | fitler pode devices |
| FILTER_MPODE | YES | YES | YES | fitler mpode devices |
| extract_dnwpsub | NO | NO | NO | extract parasitic dnw/pub diode |
| extract_pnwdio | NO | NO | NO | extract parasitic rw/dnw diode |

# Calibre Switches Overview (III/III)



| SWITCH NAMES | Default | IP | FULL CHIP | COMMENT |
|---|---|---|---|---|
| extract_pwdnw | NO | NO | NO | extract parasitic NW-PSUB diodes |
| LVS_REDUCE_PARALLEL_MOS | NO | NO | NO | enable MOS parallel reduction |
| LVS_REDUCE_SPLIT_GATES | NO | NO | NO | enable MOS SPLIT GATE reduction |
| LVS_REDUCE_PARALLEL_MIMCAP | NO | NO | NO | enable MIMCAP parallel reduction |
| METAL_MAIN_CHECK | YES | YES | YES | highlight non-color main metal layer |
| MATCHFLAG | YES | YES | YES | extract matchingflag and edgeflag |
| FLICKER_CORNER_EXTRACTION | NO | NO | NO | flicker corner extraction |
| SELF_HEATING_EFFECT_EXTRACTION | NO | NO | NO | self heating effect extraction |
| PARAMETERIZED_CPODE | NO | NO | NO | enable parameterized cpode feature |
| unexpected_device_checking_SHDMIM | YES | YES | YES | unexpected SHDMIM device check |
| unexpected_device_checking_SHPMIM_server | YES | YES | YES | unexpected SHPMIM server device check |
| unexpected_device_checking_SHPMIM_client | YES | YES | YES | unexpected SHPMIM client device check |
| PSUB2_ERC_CHECK | YES | YES | YES | SR_DOD cut PSUB2 checking |

# Calibre Variables(I)

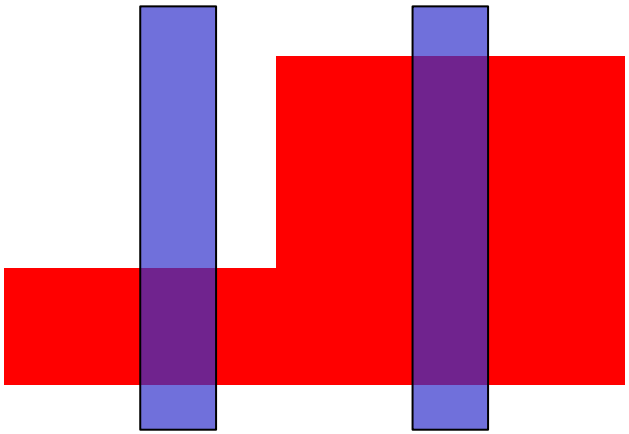
- **VARIABLE POWER_NAME**
  - Power name string setting.
- **VARIABLE GROUND_NAME**
  - Ground name string setting.
- **VARIABLE PRESCALE**
  - Scale factor for WPE and DFM effect.
  - For N3 process, PRESCALE=1.0.
  - Please do not change the default value.

# Calibre Variables(II)

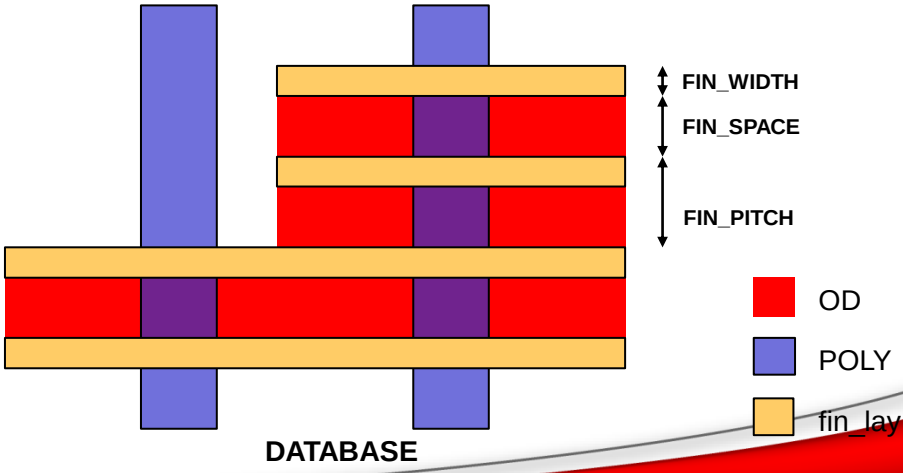
- **The following variables are to control the LVS error tolerance. For example, MOS_Lerr is the error tolerance of length of all MOS devices.**
  - VARIABLE MOS_NFINerr 0
  - VARIABLE MOS_Lerr 0

# Calibre Variables(III)

- In N3 process, LVS needs to generate “fin_lay” to let RC tools know the fin shape in the silicon and calculate the correct RC parasitics. The following variables are to specify the fin structure.
  - `VARIABLE FIN_WIDTH 0.006`
  - `VARIABLE FIN_SPACE 0.020`
  - `VARIABLE FIN_PITCH 0.026`
  - `VARIABLE FIN_WIDTH_IO 0.006`
  - `VARIABLE FIN_SPACE_IO 0.022`
  - `VARIABLE FIN_PITCH_IO 0.028`



LAYOUT




DATABASE

# Calibre Variables(IV)



- **VARIABLE L_SHAPE_OD_GATE_LEN 0.221**
  - When two standard cells abut, LVS deck generates a small gate automatically at abutted PODE. This variable is the maximum allowed PODE Lg to form small gate.

# Runset Options

# Runset Options

- **Virtual Connection Setting**
  - By default, VIRTUAL CONNECT COLON is set yes.
    Please set to "**NO**" in LVS command file as doing full-chip checking.
    - VIRTUAL CONNECT COLON YES ➔ VIRTUAL CONNECT COLON NO

# Calibre LVS/xACT Flow

# Calibre LVS Flow

- **Run LVS deck(default):**
  - Include “source.added” file in your source netlist for subcircuits.
    - .include source.added
  - Comment the following line for LVS check.
    - //#define RC_DFM_RULE
  - Fill in the gds file name and top_cell name in the rule deck.
    - LAYOUT PRIMARY “top_cell”
    - LAYOUT PATH “top_cell.gds”
  - Fill in the source netlist name and top_cell name in the rule deck.
    - SOURCE PRIMARY “top_cell”
    - SOURCE PATH “top_cell.cdl”
  - Run Calibre
    - **% calibre -lvs -hier -spi layout.net calibre_rule_deck**
    - Files lvs.rep and lvs.rep.ext are LVS result and path check report.
  - It’s recommend to flatten dummy patterns for performance.
    - FLATTEN CELL top_cell_DM top_cell_DODDPO

# Calibre xACT Extraction Flow(1)

- **Prepare xACT technology file :**
  - Download the xACT RC technology file corresponding to the process you used from TSMC online.
    - For example, you need to download the xACT technology file corresponding to N3 process.
  - Unzip the zip file and extract the capacitance and resistor rule statement file(rules).
  - Make sure “BA_mapping” and “xact_mapping_*m” files are under the run directory. (Can specify the path in the LVS rule deck)
    - Please make sure to use the one inside “**MAIN_DECK/CALIBRE_FLOW**” folder generated by deck installation and **do not** use the one inside “profile/CALIBRE_FLOW” folder.
  - Finally, run RCX on your design. Make sure the "rules" file is located in the working directory.

# Calibre xACT Extraction Flow(2)

- **Run RC deck:**
  - Uncomment the following line for RC extraction flow.
    - #define RC_DFM_RULE
  - Fill in the gds file name and top_cell name in the rule deck.
    - LAYOUT PRIMARY “top_cell”
    - LAYOUT PATH “top_cell.gds”
  - Fill in the source netlist name and top_cell name in the rule deck.
    - SOURCE PRIMARY “top_cell”
    - SOURCE PATH “top_cell.cdl”
  - **Run Calibre xACT with cross reference.**
    - File “xcell” is used for RC cell blocking in RF devices.
    - **% calibre -lvs -xcell xcell -hier calibre_rule_deck**
    - **% calibre -xact -xcell xcell -rcc calibre_rule_deck**
  - **Run Calibre xACT without cross reference.**
    - File “xcell” is used for RC cell blocking in RF devices.
    - **% calibre -xact -xcell xcell -rcc calibre_rule_deck**
  - Files net.dist , net.dist.pex, and net.dist.pxi are created.

# Calibre/StarRCXT LVS/CCI Flow

# Calibre LVS/CCI Flow

- **Run LVS deck:**
  - Include “source.added” file in your source netlist for subcircuits.
    - .include source.added
  - Comment the following line for LVS check.
    - //#define CCI_DFM_RULE
  - Uncomment the following line for LVS check.
    - #define LVS_DECK
  - Fill in the gds file name and top_cell name in the rule deck.
    - LAYOUT PRIMARY “top_cell”
    - LAYOUT PATH “top_cell.gds”
  - Fill in the source netlist name and top_cell name in the rule deck.
    - SOURCE PRIMARY “top_cell”
    - SOURCE PATH “top_cell.cdl”
  - Run Calibre
    - **% calibre -lvs -hier -spi layout.net calibre_rule_deck**
    - Files lvs.rep and lvs.rep.ext are LVS result and path check report.
  - It’s recommend to flatten dummy patterns for performance.
    - FLATTEN CELL top_cell_DM top_cell_DODDPO

# Calibre/StarRCXT CCI FLOW



- **Run CCI deck(default) :**
  - Include “source.added” file in your source netlist for subcircuits.
    - .include source.added
  - Comment the following line for CCI StarRCXT flow.
    - //#define LVS_DECK
  - Uncomment the following line for CCI StarRCXT flow.
    - #define CCI_DFM_RULE
  - Run Calibre
    - **% calibre -lvs -xcell xcell -hier -spi layout.net calibre_rule_deck**
    - **% calibre -query svdb < query_cmd | tee query.log**
  - Download StarRCXT tech file( *.nxtgrd file ) from TSMC online.
  - Fill in the top cell name, calibre runset file, TCAD file, mapping file and pin file in star_cmd
    - BLOCK: top_cell
    - CALIBRE_RUNSET: calibre_rule_deck
    - MAPPING_FILE: starrcxt_mapping
      - Please make sure to use the one inside **“MAIN_DECK/CCI_FLOW”** folder generated by deck installation and **do not** use the one inside “profile/ CCI_FLOW” folder.
    - TCAD_GRD_FILE: *.nxtgrd
    - CALIBRE_OPTIONAL_DEVICE_PIN_FILE: pin_file.txt
  - Run StarRC
    - **% StarXtract -clean star_cmd**
    - top_cell.spf is the RC+LPE layout netlist.

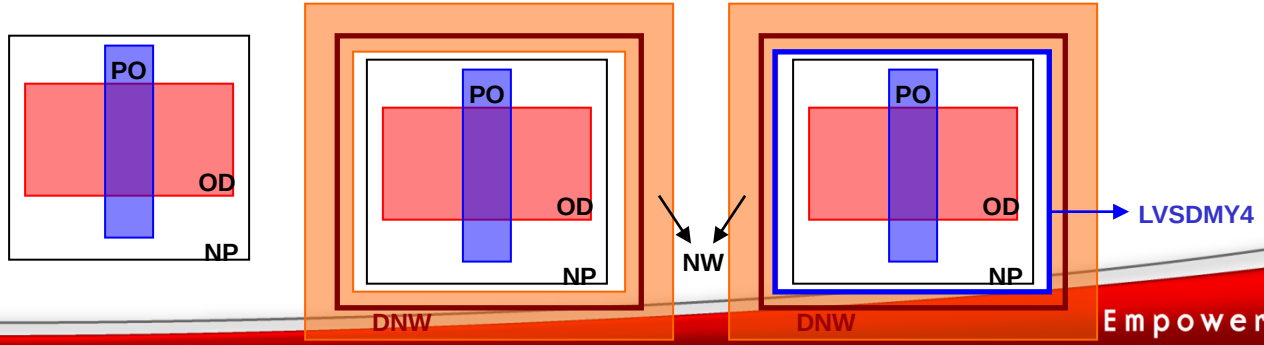
# Appendix

## NMOS in DNW Region

# NMOS in DNW Region

- For all Core/IO NMOS, LVS will separate ‘NMOS inside DNW region’ as new type of LVS naming (model naming is not changed)
- Marker layer LVSDMY4(208;4) is required to change device LVS naming as ‘nch*_dnw_mac’
- Support “LVSDMY4_check” to make sure LVSDMY4 will not be existed alone
- Exception:
  - All native NMOS which inside NT_N ex: nch_na_mac
- Example:

| Device Type | Model Naming | Device LVS Naming | | | Device LPE Naming |
|---|---|---|---|---|---|
| | | w/o DNW | w/i DNW , no LVSDMY4 | w/i DNW, add LVSDMY4 | |
| Core | nch_svt_mac | nch_svt_mac | nch_svt_mac | nch_svt_dnw_mac | nch_svt_mac |
| I/O | nch_12_mac | nch_12_mac | nch_12_mac | nch_12_dnw_mac | nch_12_mac |



# Appendix

## Back-notation for Model flags

# Back Annotation Parameters

- **LPE_PARAM: param_name mode1 value1 [mode2 value2…] [PINEXCEPT pinIds] [PINOPERATION {AND}|OR]**
  - **Description**
    - **To back-annotate the LPE parameters after RC extraction. The parameter value is determined by the mode. The mode is basically determined by the execution type, for example, R, C or RC extraction. However, the mode will become NORC when one or multiple terminal of a device does not extract R or C. So the mode may be different between devices. One mode is followed by a value. RC tool will attach parameter value according to the mode of each device.**
  - **PINEXCEPT**
    - **When considering mode of a device, some pins should be excluded because those pins have nothing to do with this parameter. This command is used to specify what pins should be excluded.**
  - **PINOPERATION**
    - **After some pins are excluded, the rest of the pins are relative to the parameter. This command is to determine the relation is “AND” operation or “OR” operation. If the operation is “AND”, it means if any one of the pins does not extract RC, the mode goes to NORC. If the operation is “OR”, it means when all the pins does not extract RC, the mode goes to NORC.**
- **Example**
  - **LPE_PARAM: ccodflag NORC 1 C 0 R 1 RC 0 PINEXCEPT 2 3 PINOPERATION OR**

# Back Annotation Mapping(I)



- The values are determined by "EXTARCTION: R/C/RC" command

```
*** RC Extraction options
TCAD_GRD_FILE: ./clnxxg+_1p0xm+alrdl_typical.nxtgrd
MAPPING_FILE:  ./starrcxt_mapping
EXTRACTION: RC
MODE: 400
```

- Table of flags results vs. extraction mode:

| | R-only | C-only | RC Mode | NoRC Mode |
|---|---|---|---|---|
| Flags | ccodflag = 1 | ccodflag = 0 | ccodflag = 0 | ccodflag = 1 |
| Result | ccosflag = 1 | ccosflag = 0 | ccosflag = 0 | ccosflag = 1 |
| | rcodflag = 0 | rcodflag = 1 | rcodflag = 0 | rcodflag = 1 |
| | rcosflag = 0 | rcosdflag = 1 | rcosflag = 0 | rcosflag = 1 |
| | rgflag = 0 | rgflag = 1 | rgflag = 0 | rgflag = 1 |

- All MOS devices supports these 5 flags are listed in "LPE_DEVICES"

# Back Annotation Mapping(II)

- The values are determined by "EXTARCTION: R/C/RC" command

```
*** RC Extraction options
TCAD_GRD_FILE: ./clnxxg+_1p0xm+alrdl_typical.nxtgrd
MAPPING_FILE:  ./starrcxt_mapping
EXTRACTION: RC
MODE: 400
```

- Table of flags results vs. extraction mode:

| | R-only | C-only | RC Mode | NoRC Mode |
|---|---|---|---|---|
| Flags | ccopflag = 1 | ccopflag = 0 | ccopflag = 0 | ccopflag = 1 |
| Result | rcopflag = 0 | rcopflag = 1 | rcopflag = 0 | rcopflag = 1 |
| | rgpflag = 0 | rgpflag = 1 | rgpflag = 0 | rgpflag = 1 |

- All PODE devices supports these 3 flags are listed in "LPE_DEVICES"

# Back Annotation Mapping(III)



- The values are determined by "EXTARCTION: R/C/RC" command

```
*** RC Extraction options
TCAD_GRD_FILE: ./clnxxg+_1p0xm+alrdl_typical.nxtgrd
MAPPING_FILE:  ./starrcxt_mapping
EXTRACTION: RC
MODE: 400
```

- Table of flags results vs. extraction mode:

| | R-only | C-only | RC Mode | NoRC Mode |
|---|---|---|---|---|
| Flags | capflag = 1 | capflag = 0 | capflag = 0 | capflag = 1 |
| Result | ccoflag = 1 | ccoflag = 0 | ccoflag = 0 | ccoflag = 1 |
| | rgateflag = 0 | rgateflag = 1 | rgateflag = 0 | rgateflag = 1 |
| | rcoflag = 0 | rcoflag = 1 | rcoflag = 0 | rcoflag = 1 |

- Passive devices supports flag are listed in "LPE_DEVICES"

# LPE PARAM - ccodflag / ccosflag

| | D | G | S | Flag => 0/1 |
|---|---|---|---|---|
| ccodflag | X | X | | 1 |
| | X | V | | 0 |
| | V | X | | 0 |
| | V | V | | 0 |
| ccosflag | | X | X | 1 |
| | | V | X | 0 |
| | | X | V | 0 |
| | | V | V | 0 |

X: There is no RC extracted

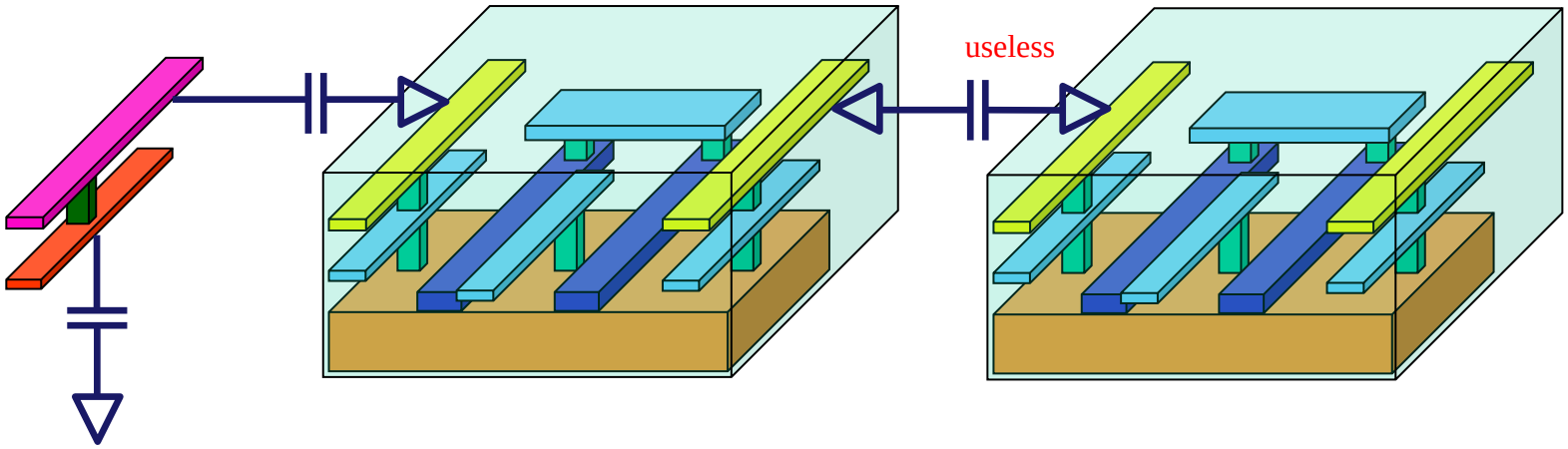
V: There is RC extracted

# Appendix

## Pin-to-Pin PCELL Extraction

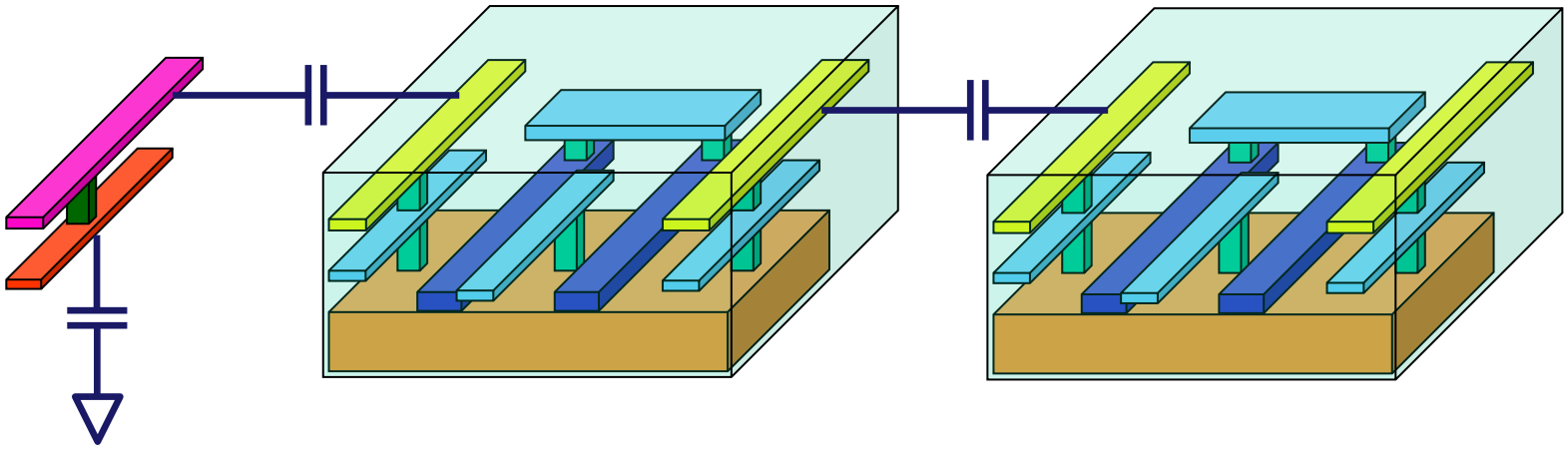
# Cell Blocking without Pin-to-Pin Function

- Interconnect to pcell capacitance is netlisted as interconnect to ground
- Cell to cell cap can't be extracted.



# Cell Blocking with Pin-to-Pin Function Enablement (Default)

- Interconnect to pcell capacitance is netlisted as interconnect to pcell pin.
- Cell to cell cap is netlisted as pin-to-pin capacitance.



ground node

# Enable Pin-to-Pin Extraction in StarRC

- **Add this command in star_cmd file**

  **COUPLE_TO_PCELL_PINS: YES AUTOMATIC_CG_HANDLING**

# Appendix
## Pin text layer of N3

# Pin Text of N3 (PORT)

- N3 has different pin text definition from other process:
  - Pin text layers (PORT also) are using layer number (202; XX).
  - Add pin text layers for MD/MP conductors.

| | Layer Number | Text Name | Purpose |
|---|---|---|---|
| FEOL | (202; 17) | Text for poly (poly_text) | Pin text attached for “n_poly/p_poly” conductor |
| MEOL | (202; 82) | Text for MD (MD_text) | Pin text attached for “MD_OD/MD_STI” conductor |
| BEOL | (202; 30) | Text for M0 (M0_text) | Pin text attached for “M0_A/M0_B” conductor |
| | (202; 31~48) | Text for M1~M18 (M#_text) | Pin text attached for “M#_A/M#_B/M#” conductor |
| | (202 ; 74) | Text for ALRDL(AP_text) | Pin text attached for “AP” conductor |
| WELL TEXT | (202; 2) | Text for PSUB (psub_text) | Pin text attached for psub region<br>Need to turn on switch “WELL_TEXT” |
| | (202; 3) | Text for NW (nxwell_text) | Pin text attached for nxwell region<br>Need to turn on switch “WELL_TEXT” |

# NET Text of N3

- **N3 NET text layers:**
  - **Using layer number (127; XX).**

| | Layer Number | Text Name | Purpose |
|---|---|---|---|
| FEOL | (127;17) | Text for poly (Tpoly_text) | NET text attached for “n_poly/p_poly” conductor |
| MEOL | (127;82) | Text for MD (TMD_text) | NET text attached for “MD_OD/MD_STI” conductor |
| BEOL | (127;30) | Text for M0 (TM0_text) | NET text attached for “M0_A/M0_B” conductor |
| | (127;31~48) | Text for M1~M18 (TM#_text) | NET text attached for “M#_A/M#_B/M#” conductor |
| | (127;74) | Text for ALRDL(TAP_text) | NET text attached for “AP” conductor |