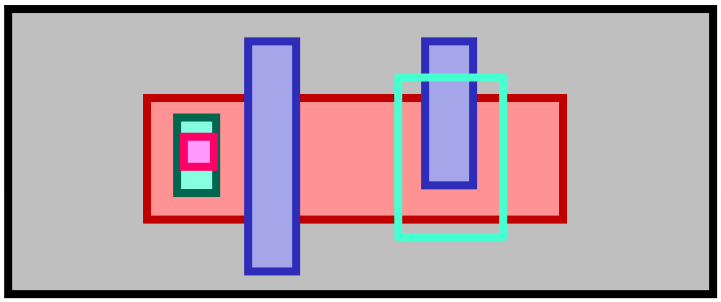
LVS Filter Introduction

LVSRCE/TSMC

September 4, 2020

RODMY & SRAM Layers

- **Definition**
  - RODMY is a LVS dummy layer for SRAM process to exclude OD area
- **LVS Usage**
  - This layer is to remove OD layer in SRAM area only
  - No gate when OD & PO covered by RODMY in SRAM block
- **Logic Operation**
  - diff = OD NOT (RODMY AND SRM)
- **Example**

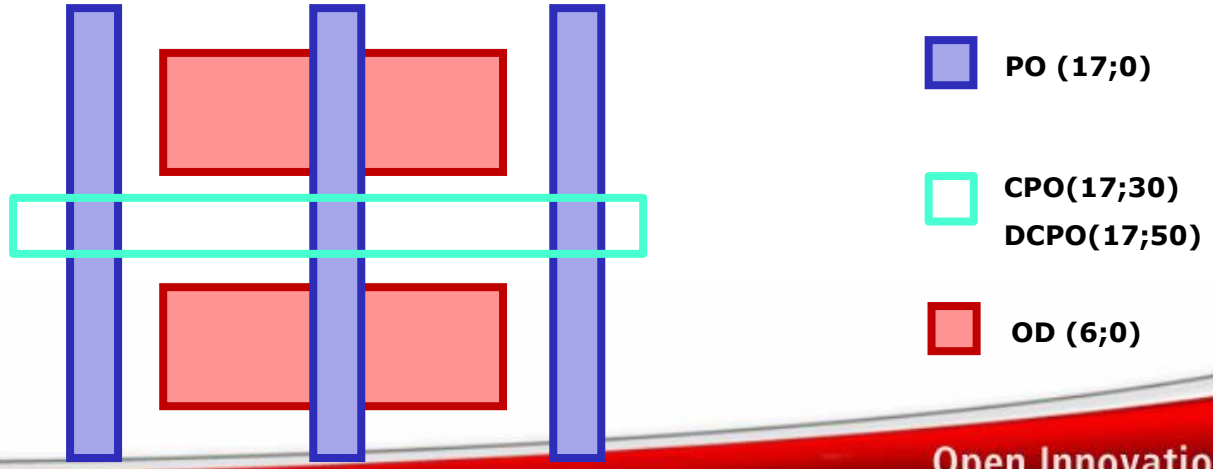


Only 1 (left) device extracted

PO (17;0)
RODMY (20;100)
OD (6;0)
MD (82;150)
VD (179;150)
SRM (20;0)

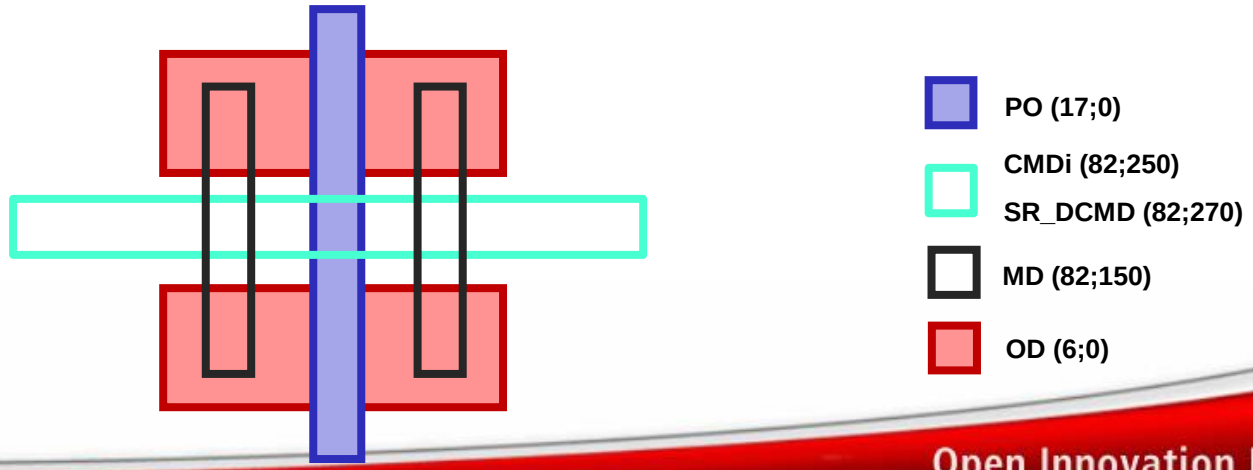
CPO Layers

- Definition
  - Layers used to cut poly
- LVS Usage
  - CPO/DCPO layers will remove POLY layer
- Logic Operation
  - poly_cut = CPO OR DCPO
  - POx = POx1 NOT poly_cut
- Example



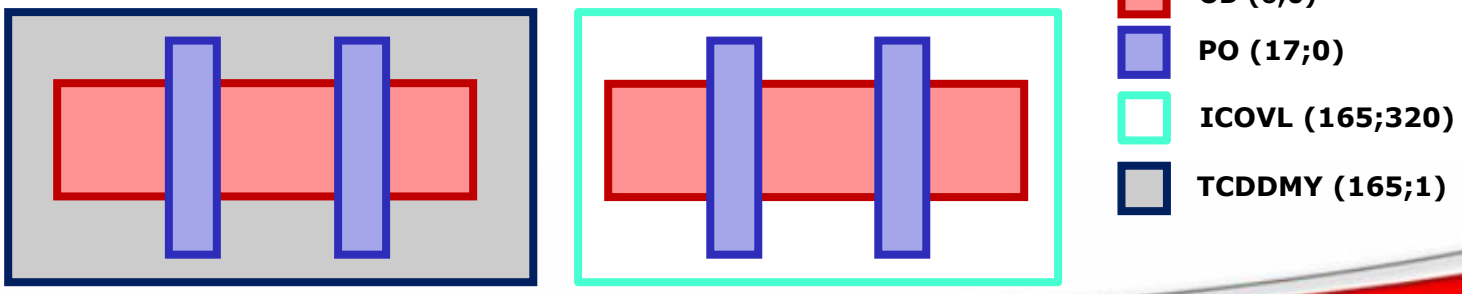
CMD Layers

- Definition
  - Layers used to cut MD
- LVS Usage
  - CMD/SR_DCMD layers will remove MD layer
- Logic Operation
  - MD_cut = CMDi OR SR_DCMD
  - MD = MDi NOT MD_cut
- Example



TCDDMY & ICOVL Layers

- **Definition**
  - DRC dummy layers for TCD & ICOVL dummy patterns
- **LVS Usage**
  - OD/PO would be removed under these layers, so no devices would be formed
- **Logic Operation**
  - OD = ODi NOT (TCDDMY OR ICOVL)
  - PO = POi NOT (TCDDMY OR ICOVL)
- **Example**



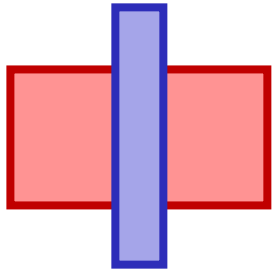
LVS Dummy Layers

- **The followings are dummy layers for LVS to identify particular devices**

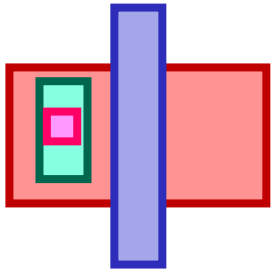
Layer Name in LVS	Layer Usage Description
BJTDMY, BJTHPDMY, IBJTDMY	dummy layer to form BJT
DIODMY	dummy layer to form diode
RMDMY	dummy layer to form ALRDL/METAL resistor
RPDMY	dummy layer to form MG/TiN resistor
NWDMY	dummy layer to form N-Well resistor
MOMDMY	dummy layer to recognize MOM region
INDDMY	dummy layer to recognize IND(SPIRAL) region
MFUSE/VFUSE	dummy layer to recognize Metal Fuse /Via Fuse resistor.
LVSDMY4	dummy layer to recognize DNW-type NMOS (with DNW)
HIA_DUMMY	dummy layer to recognize HIA diode devices.
PODE_GATE	dummy layer to recognize 3T PODE devices
PODE_TrGATE	dummy layer to recognize 4T PODE devices.

MOS Recognition

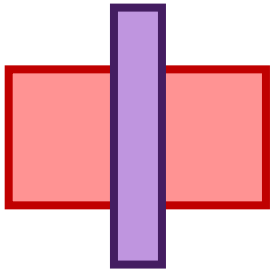
- Illustration for MOS identification



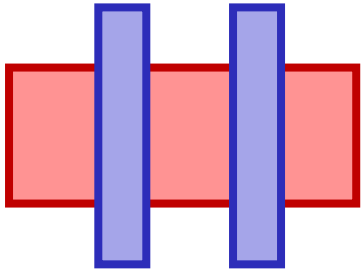
1. nothing extracted



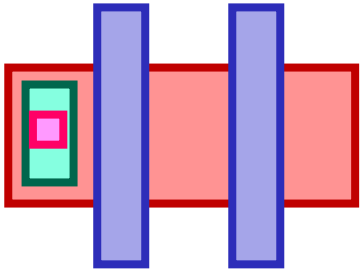
2. one mos extracted



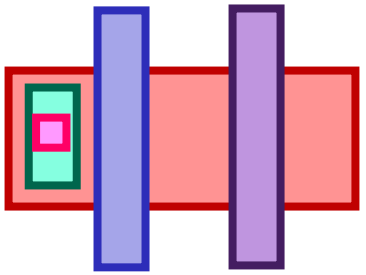
3. nothing extracted



4. nothing extracted



5. two mos extracted



6. one mos extracted (right mos is filtered)

OD (6;0)

PO (17;0)

MD (82;150)

SR_DPO (17;7)

VD (179;150)

MOS Recognition (Cont.)

- **Rule for MOS recognition**
  - MOS gate can only be formed when PO on OD are both drawing layers and satisfy valid_PO or valid_OD conditions. (see “N3_STDCELL_FILTER.pdf")
  - MOS gate is not formed when
    a). OD is not drawing layers
    b). OD and PO are not valid conditions (see “N3_STDCELL_FILTER.pdf")
  - MOS gate is not formed by SR_DPO

Poly Covered by PODE_GATE (206;28)

Region	Marker Layer	Form device	ERC Check
MOS	X	3T PODE	X
Varactor	143;0	X	X
Diode	119;0	X	X
BJT	110;0	X	X
Hia diode	168;0	X	X
Strap	NOD on NW POD on PW	X	X