TSMC ESD/LUP PERC Checking Methodology

(T-N03-CL-DR-007, V1.0_3)

EETD/DTP

May 6th, 2022

Contents

PERC Methodology

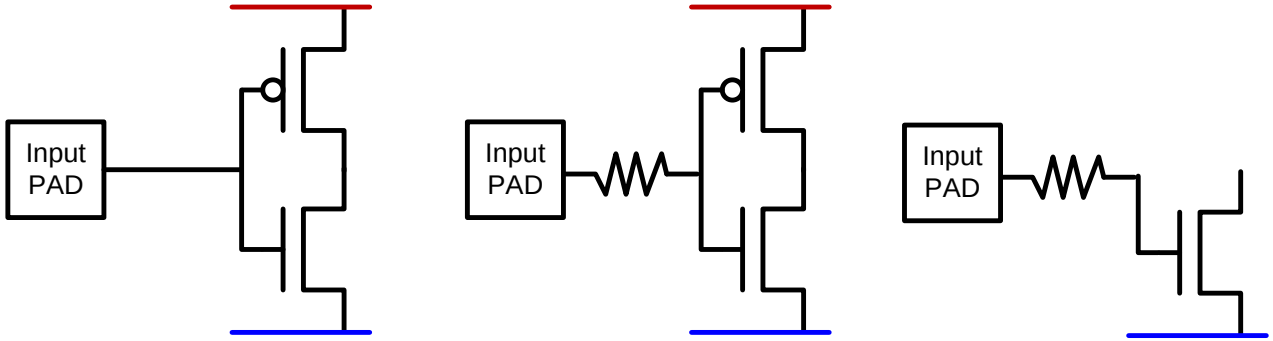
(General N3 PERC Introduction)

PAD Definition

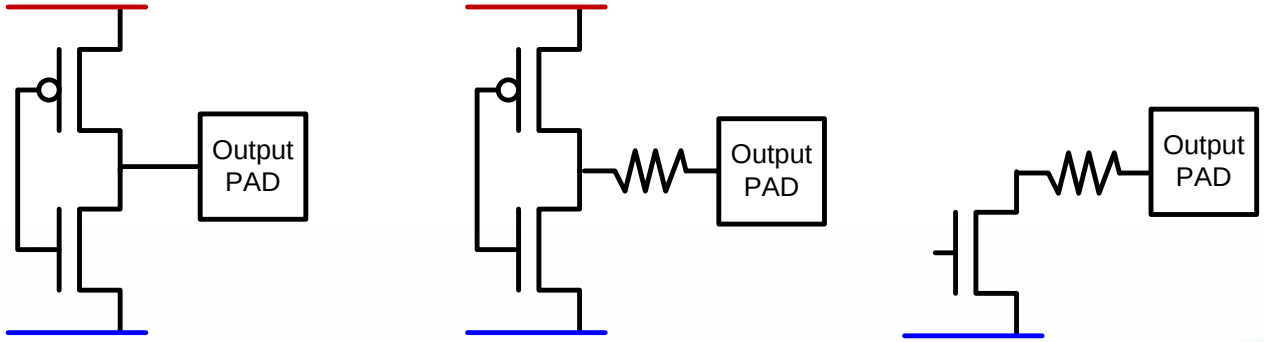
- **Auto-detect wire-bond(WB) / flip-chip(FC) pad as below:**
  - **Wire-Bond (Cu RDL)** Cu_RDL(73;0) AND CB2_WB(86;20)
  - **Flip-Chip (Cu RDL)** Cu_RDL(73;0) AND { Cu_CB2_FC(86;300) OR Cu_CB2_FCU(86;325) }
  - **InFO (Cu RDL)** Cu_RDL(73;0) AND CB2_IN(86;30)

Input/Output Net Definition

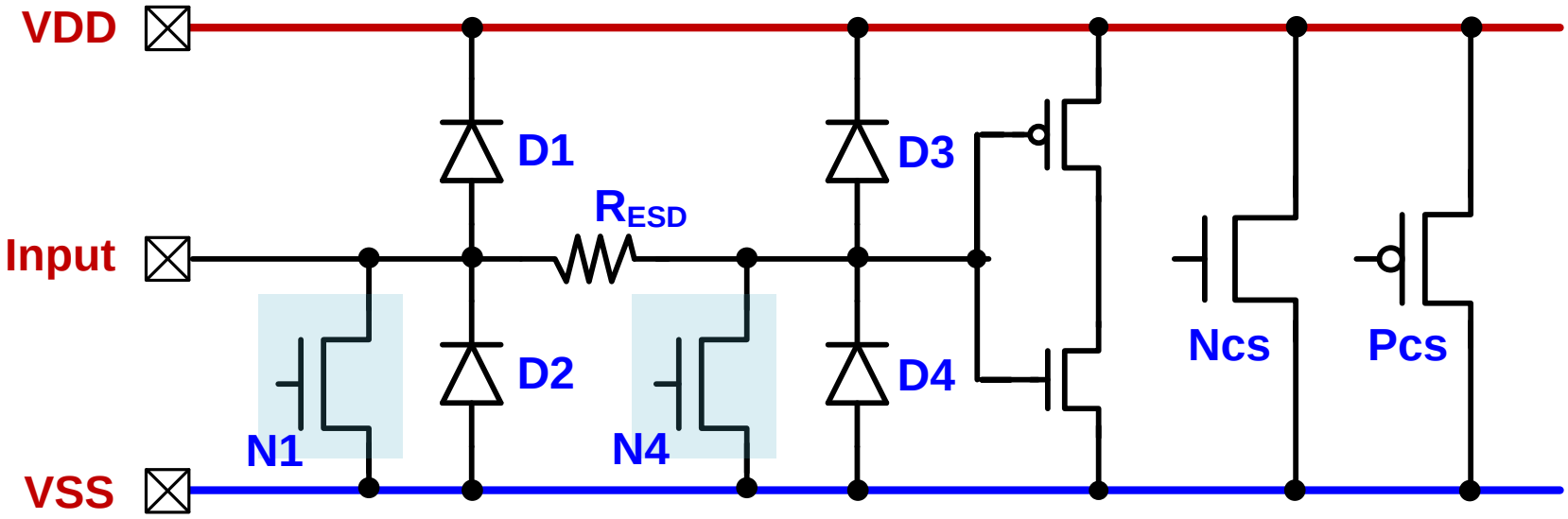
- **Input Net: Net connected between MOS gate and IO Pad (through or not-through) resistor**



- **Output Net : Net connected between MOS drain and IO Pad (through or not-through) resistor**



ESD Structure on IO Pad Defined by N3 PERC



N1: Primary ESD protection (snapback based approach, including single and two stage)

N4: Secondary ESD protection (snapback based approach, including single and two stage)

D1/D2: Primary ESD protection (diode based approach ➔ pull-up/pull-down diode)

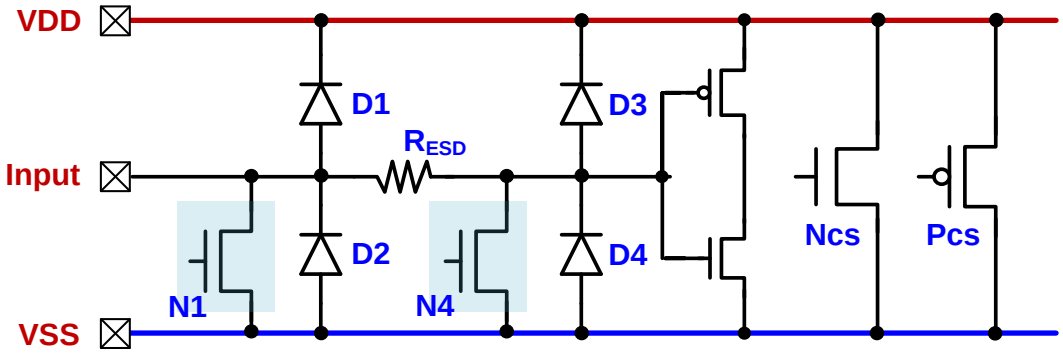
D3/D4: Secondary ESD protection (diode based approach ➔ pull-up/pull-down diode)

Pcs/Ncs: Single stage power clamp (PMOS and NMOS type) or cascoded power clamp (NMOS type)

R_{ESD}: ESD resistor

For Output PAD, resistor and secondary ESD protection is neither required and nor checked by PERC

General Concept of N3 ESD Rules



1. All input and output IO Net should have rule-complied primary ESD protection (either N1 or D1+D2) (DRC checking/PERC CDL checking)
    1. Either rule-complied snapback based protection or rule-complied diode based protection is required (ESD.NET.1g, ESD.NET.1.1g)
    2. Rule-complied diode based protection = rule-complied pull-up diode (D1) AND rule-complied pull-down diode (D2)
2. All input IO Net should have rule-complied secondary ESD protection (either N4 or D3+D4)

    (PERC checking, ESD.9.0g~9.3g)
    1. Either rule-complied snapback based protection or rule-complied diode based protection is required
    2. Rule-complied diode based protection = rule-complied pull-up diode (D3) AND rule-complied pull-down diode (D4)
3. All Power Net should have rule-complied power clamp (Ncs/Pcs) (PERC checking, ESD.40g~ESD.43g)
4. There should be rule-complied ESD resistor (R_{ESD}) between input IO net and MOS gate (PERC checking, ESD.8g, ESD.8.1g)

General ESD Device Definition

ESD device on IO net:

1. **Defined in the ESD device table**
2. **Have specific connection conditions**
   - **Snapback device(N1) :**
     - **Single stage : drain tied to PAD, source and bulk tied to ground, gate connection does not matter.**
     - **Two stage is allowed as well.**
   - **Snapback device(N4) : drain tied to net after ESD resistor, source and bulk tied to ground (single stage and two stage are allowed).**
   - **Dual diode (D1 + D2) : must exist in the same IO PAD**
   - **Dual diode (D3 + D4) : must exist in the same net after ESD resistor**
   - **For device structures not defined in the PERC ESD network scheme and device table, it is not recognized by PERC and would not be checked.**
3. **Primary ESD device should be covered with specific dummy layers**

   (a) Snapback NMOS: SDI, SDI_2, SDI_3 and SR_ESD (for DRC checking)

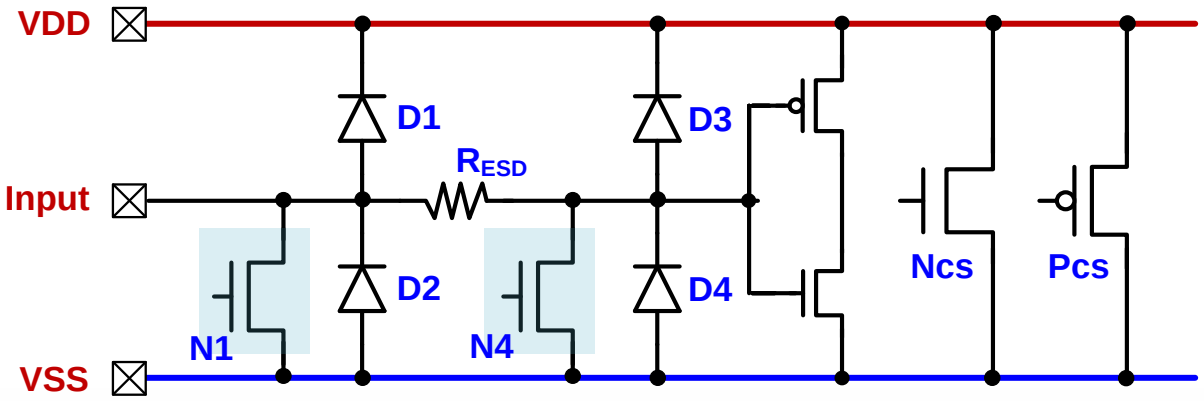
   (b) Dual Diode: HIA Dummy (for DRC checking)

Power clamp:

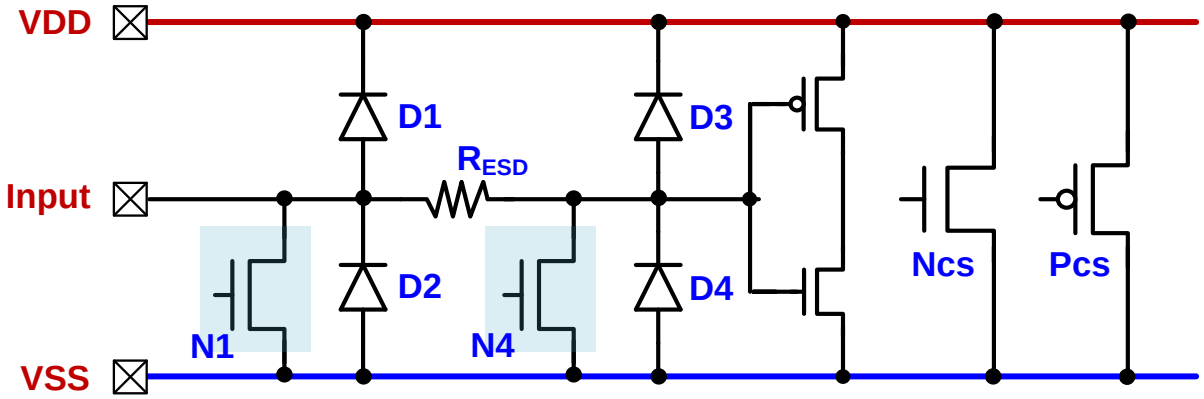
1. **Defined in the ESD device table**
2. **Have specific connection**
3. **Both single stage and cascoded power clamp should cover with SDI.**

ESD Device Definition

- **Main categories:**
  1. **NMOS for primary NMOS (N1) and secondary NMOS (N4)**
  2. **Diode for primary ESD diode (D1, D2)**
  3. **Diode for secondary ESD diode (D3, D4)**
  4. **Diode for back-to-back (B2B) diode**
  5. **ESD resistor (R_{ESD})**
  6. **NMOS for power clamp (Ncs) or PMOS for power clamp (Pcs)**

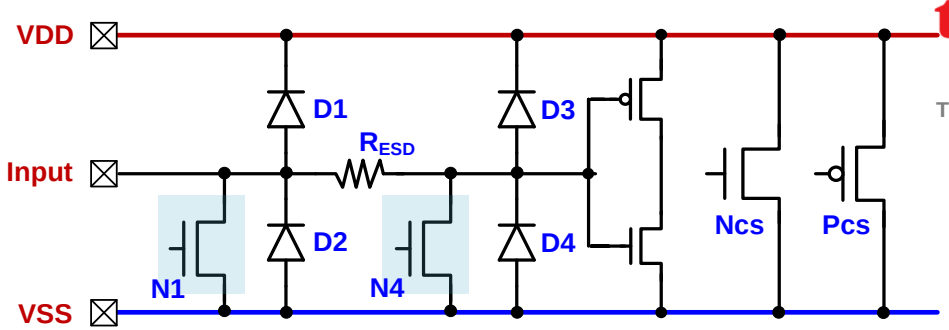


ESD Device Definition



- **Special summary**
  1. **Core NMOS cannot be primary ESD MOS (N1) nor 2nd ESD MOS (N4).**
  2. **PMOS is not used as either primary nor secondary ESD device. If pull-up PMOS is required in the circuit, only cascoded PMOS design is allowed.**
  3. **Only HIA-diode can be primary or secondary ESD diode protection device. (D1, D2, D3, D4)**
  4. **Only HIA-diode can be B2B diode device.**
  5. **Cascoded NMOS is enabled for primary ESD protection and secondary ESD protection in HV tolerant application.**

Device Table (N3)



CORE NMOS (Ncs)	CORE PMOS (Pcs)	I/O NMOS (N1, N4)	I/O NMOS (Ncs)	I/O PMOS (Pcs)	Primary, Secondary Diode (D1,D2, D3,D4)	Resistor (R_{ESD})	Diode (B2B diode)
nch_svt_mac	pch_svt_mac	nch_hia12_mac	nch_12_mac	pch_12_mac	ndio_hia12_mac	rhim	ndio_hia12_mac
nch_ulvt_mac	pch_ulvt_mac		nch_12od15_mac	pch_12od15_mac	ndio_hia12_ntn_mac		ndio_hia12_ntn_mac
nch_ulvtll_mac	pch_ulvtll_mac		nch_12_dnw_mac		pdio_hia12_mac		pdio_hia12_mac
nch_lvt_mac	pch_lvt_mac		nch_12od15_dnw_mac				
nch_lvtll_mac	pch_lvtll_mac						
nch_elvt_mac	pch_elvt_mac						
nch_eflvt_mac	pch_eflvt_mac						
nch_efsvt_mac	pch_efsvt_mac						
nch_svt_dnw_mac		Cascoded NMOS (N1b, N4b)	3.3V NMOS (Ncs1, Ncs2, Ncs3)	3.3V PMOS (Pcs1, Pcs2, Pcs3)			
nch_ulvt_dnw_mac							
nch_ulvtll_dnw_mac		nch_12_mac	nch_12_mac	pch_12_mac			
nch_lvt_dnw_mac		nch_12od15_mac	nch_12od15_mac	pch_12od15_mac			
nch_lvtll_dnw_mac			nch_12_dnw_mac				
nch_elvt_dnw_mac			nch_12od15_dnw_mac				
nch_eflvt_dnw_mac							
nch_efsvt_dnw_mac							

- **Only resistor listed above will be identified as ESD resistor. Metal resistor will be regarded as short, and other resistor's resistance will be set to 0 ohm.**
- **Device/scheme not covered by defined ESD network would not be recognized.**
- **For N1 & N4, gate connection in PERC definition is 'don't care.' In DRC, it should be turn-off (checked by ESD.39g)**
- **For Ncs & Pcs, gate connection in PERC definition is 'cannot directly tie to ground or power.'**

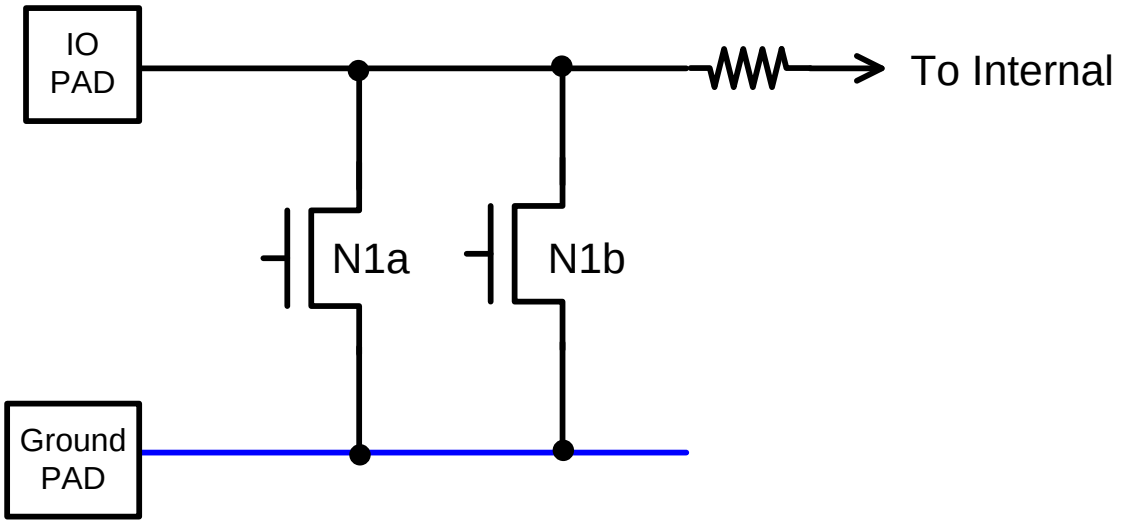
PERC Methodology

(N3 DRM/LC Rules for Topology Checker)

[Topology / CDL]

Primary-Res: ESD.8gU, ESD.8.1gU
Primary-ESD: ESD.NET.1gU, ESD.NET.1.1gU, ESD.NET.1.2gU, ESD.18g, ESD.20g, ESD.27g, ESD.29g, ESD.31g, HIA.1g, HIA.3g, HIA.3.1g
Secondary-ESD: ESD.9.0gU, ESD.9.0.1gU, ESD.9.0.2gU, ESD.9.0.3gU, ESD.9.1gU, ESD.9.1.1gU, ESD.9.1.2gU ESD.9.1.3gU, ESD.9.3gU
Power-Clamp: ESD.40g, ESD.40.1g, ESD.40.2gU, ESD.40.3.1gU, ESD.40.4gU, ESD.42g, ESD.42.1gU, ESD.42.2g, ESD.43gU
Cross-domain: ESD.45.0gU, ESD.45.0.1gU, ESD.45.0.2gU, ESD.45.1gU, ESD.47gU
MOS Protection: ESD.1.1gU, ESD.WARN.3gU, ESD.WARN.3.1gU, ESD.WARN.4.1gU, ESD.WARN.4.2gU, LUP.WARN.4U
Back-to-Back Diode: ESD.15gU
LC Primary-ESD: ESD.LC.3g, ESD.LC.3.1g
LC Power-Clamp: ESD.LC.5gU, ESD.LC.5.1gU
HiCDM Victim: ESD.CDM.1gU, ESD.CDM.1.1gU, ESD.CDM.1.3gU, ESD.CDM.2gU, ESD.CDM.2.1gU
HiCDM Power-Clamp: ESD.CDM.4gU, ESD.CDM.6g, ESD.CDM.6.1g
HiCDM B2B Diode: ESD.CDM.B.1gU, ESD.CDM.B.2gU
HiCDM Cross-domain: ESD.XDM.VIC.3gU, ESD.XDM.VIC.4gU

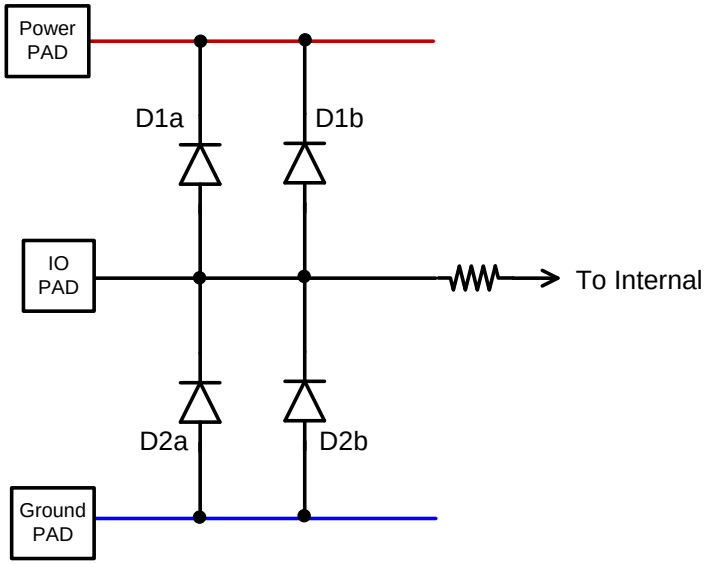
Primary ESD Definition (N1)



What will be regarded as a primary ESD snapback protection:

1. **Defined in the ESD device table**
2. **Have specific connection**
    1. **Drain directly connected to IO PAD (not through resistor)**
    2. **Source/bulk is grounded**
    3. **Gate: No specific connection condition is required**
3. **If many MOSs (N1a + N1b) are on the same IO net, their width should be summed-up for total width check.**

Primary ESD Definition (D1+D2)



What will be regarded as a primary ESD diode based protection:

1. **Defined in the ESD device table (HIA diode only)**
2. **If many Diodes (D1a + D1b or D2a + D2b) are on the same IO net, their size should be summed-up for total perimeter check.**
3. **PERC outputs perc.sum report under the RUN-directory to summarize the IO pad protection scheme.**

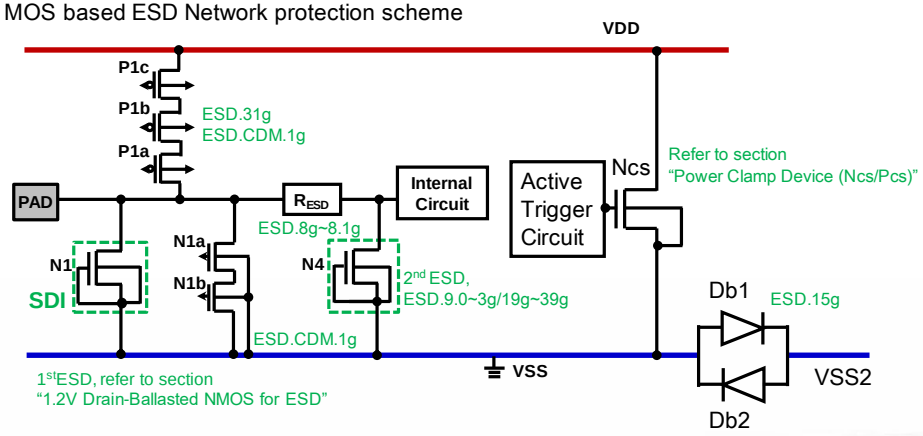
Primary ESD Device Rule

- **Existence Check: The primary ESD device size is also checked in the existence check of ESD.NET.1g & ESD.NET.1.1g.**

Rule No.	Description	Label	Op.	Rule
ESD.NET.1g^{U}	For I/O pin ESD protection scheme, the primary ESD protection (1st ESD) devices are required and it can be one of following listed devices. 1. Single stage Drain-ballasted NMOS (refer to ESD.18g~39g) 2. 2-stage cascoded Drain-ballasted NMOS (refer to ESD.18g~39g) 3. HIA diode (single stage or 2-stacked) (refer to HIA.1~18g)			
ESD.NET.1.1g^{U}	For 1.8V I/O pin ESD protection scheme, the primary ESD protection (1st ESD) devices are required and it can be one of following listed devices. Single stage Drain-ballasted NMOS is not allowed. 1. 2-stage cascoded Drain-ballasted NMOS 2. HIA diode (single stage or 2-stacked)			

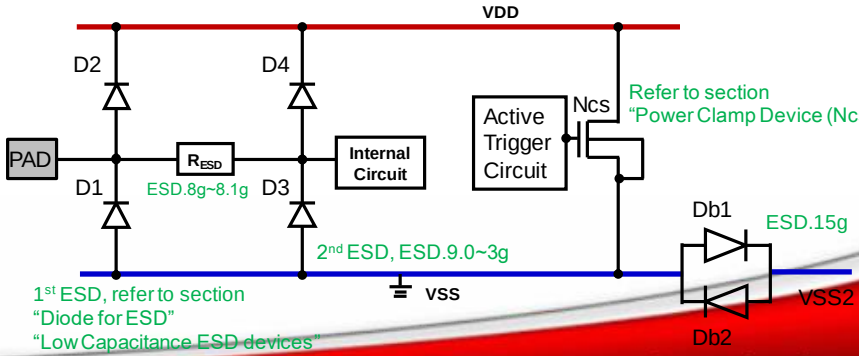
- **Snapback-based solution I/O: Drain-ballasted IO NMOS (nch_hia12) + RDR cascoded IO PMOS (pch_12)**

MOS based ESD Network protection scheme



- **Diode-based solution I/O: N-diode (ndio_hia12) + P-diode (pdio_hia12)**

Diode based ESD Network protection scheme

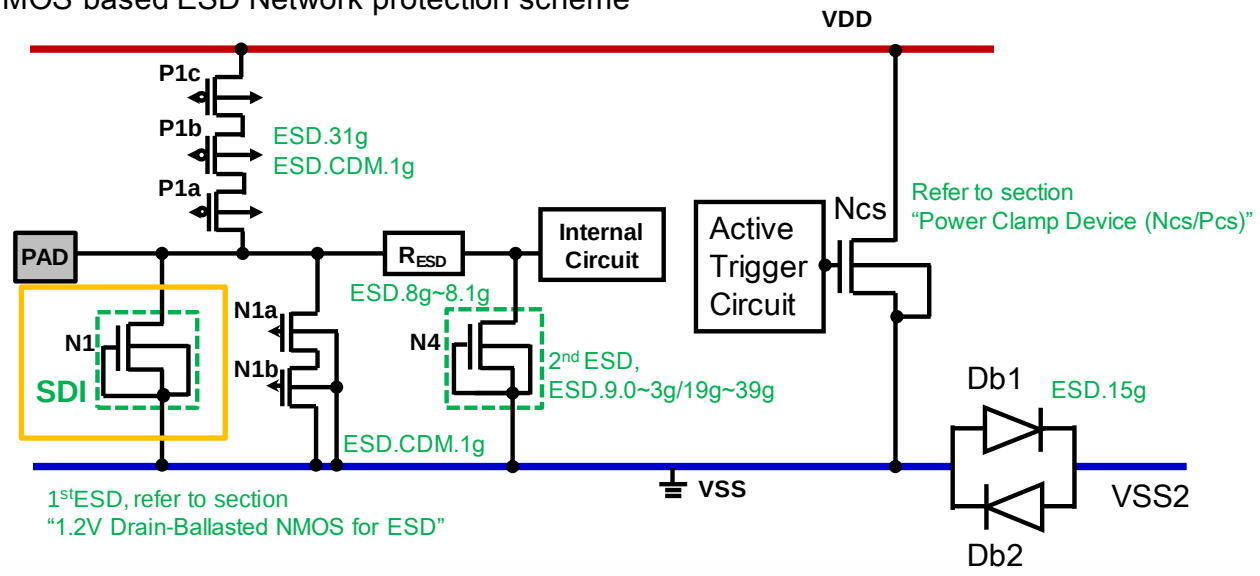


Primary ESD Device Rule

- **1.2V Drain-Ballasted NMOS for ESD**

Rule No.	Description	Label	Op.	Rule
ESD.18g	Total finger width of NMOS in same connection of IO PAD		≥	490
ESD.20g	Channel length: 1.2V drain-ballasted NMOS (in OD_12)	L	=	0.135

MOS based ESD Network protection scheme

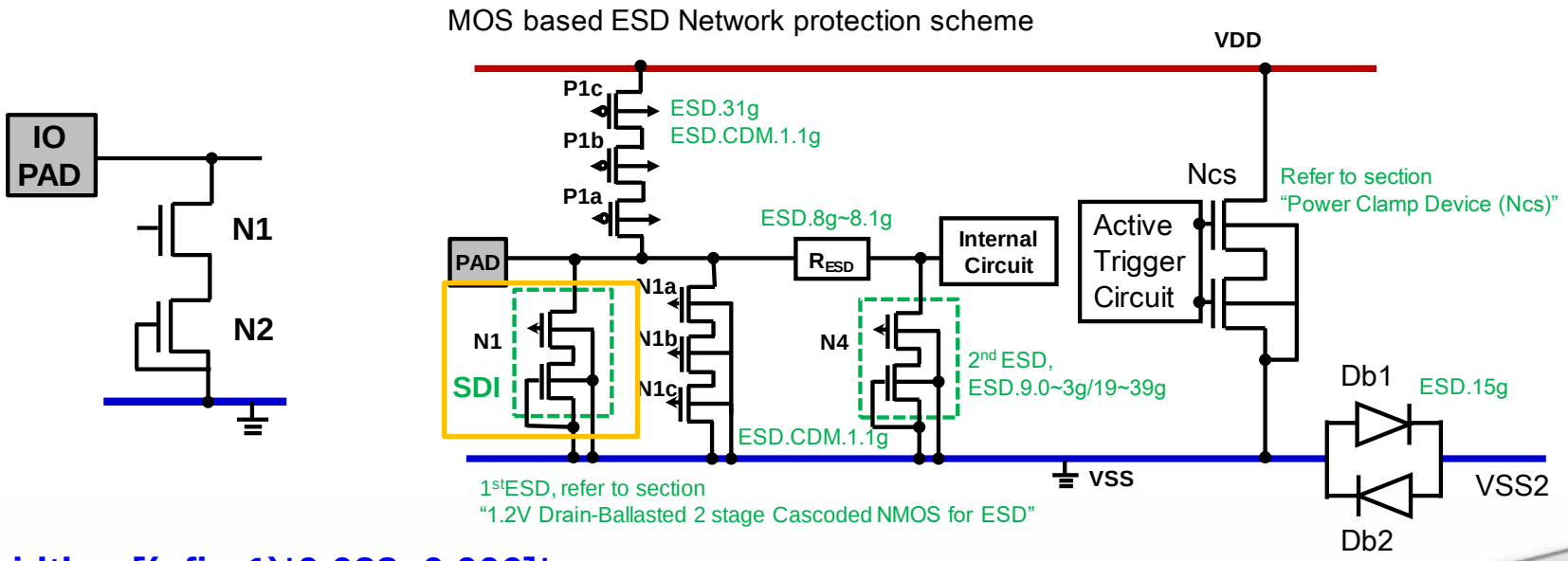


Total width = [(nfin-1)*0.028+0.006]*m

Primary ESD Device Rule

- **1.2V Drain-Ballasted Cascoded NMOS for ESD**

Rule No.	Description	Label	Op.	Rule
ESD.27g	Total finger width of 2-stage cascoded NMOS in same connection of drain connected to IO PAD		≥	540
ESD.29g	Channel length: 1.2V drain-ballasted 2-stage cascoded NMOS (1.8V tolerant I/O).	L	=	0.135



Total width = [(nfin-1)*0.028+0.006]*m

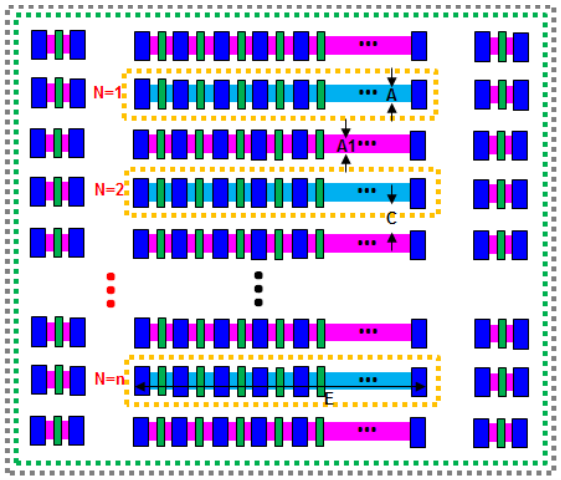
(Cascoded NMOS in the same connection of drain needs to be same OD structure: ESD.35g^{U})

Primary ESD Device Rule

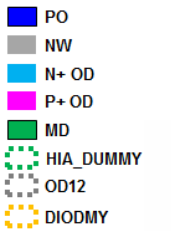
- **HIA Diode**

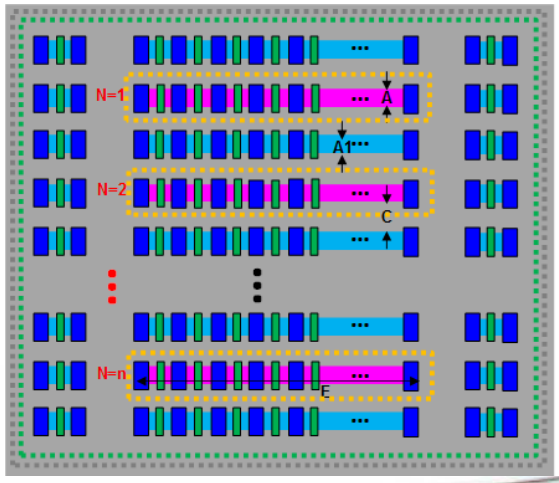
Rule No.	Description	Label	Op.	Rule
HIA.1g	Width of NACT (N-HIA diode's cathode) and PACT (P-HIA diode's anode) inside HIA_DUMMY and connect to IO PAD. (Figure 9.2.28.1~ 9.2.30.6)	A	=	0.202~0.314
HIA.3g	Total perimeter of NACT or PACT inside HIA_DUMMY in same connection of IO PAD DRC checks the drawn anode junction perimeter inside HIA_DUMMY, i.e. (A+E)*2*N (Except LC_DMY)		≥	240

Total perimeter = {[(nfin-1)*0.028+0.006]+L}*2*NF

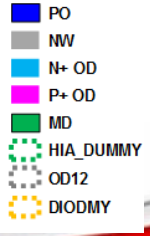


N-HIA diode





P-HIA diode

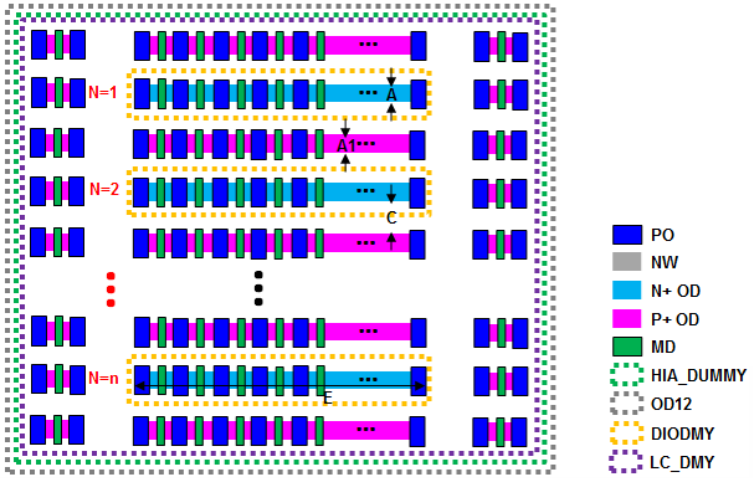


Primary ESD Device Rule

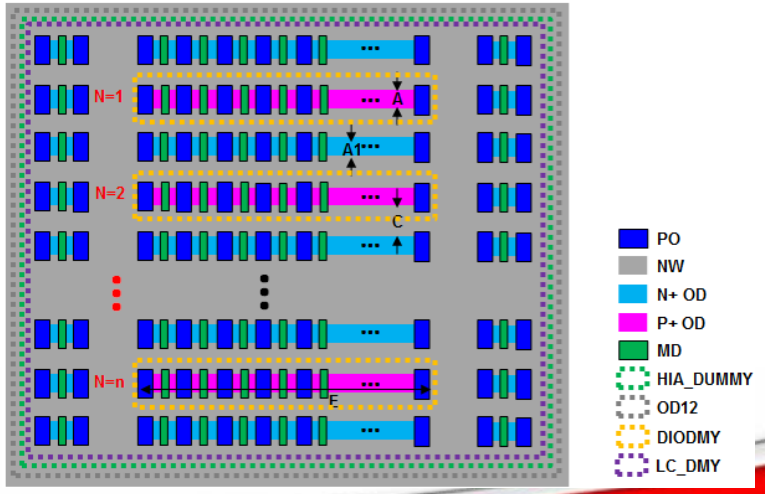
- **HIA Diode (Low-Cap)**

Rule No.	Description	Label	Op.	Rule
HIA.1g (LC diode follow same rule)	Width of NACT (N-HIA diode's cathode) and PACT (P-HIA diode's anode) inside HIA_DUMMY and connect to IO PAD. (Figure 9.2.28.1~ 9.2.30.6)	A	=	0.202~0.314
ESD.LC.3g	Total perimeter of NACT or PACT [INSIDE LC_DMY, in same connection of IO PAD] (Figure 9.2.29.1, 9.2.29.2, 9.2.30.4, 9.2.30.5 and 9.2.30.6). DRC checks the drawn anode junction perimeter inside HIA_DUMMY, i.e. (A+E)*2*N.		≥	130

Total perimeter = {[(nfin-1)*0.028+0.006]+L}*2*NF



N-HIA diode

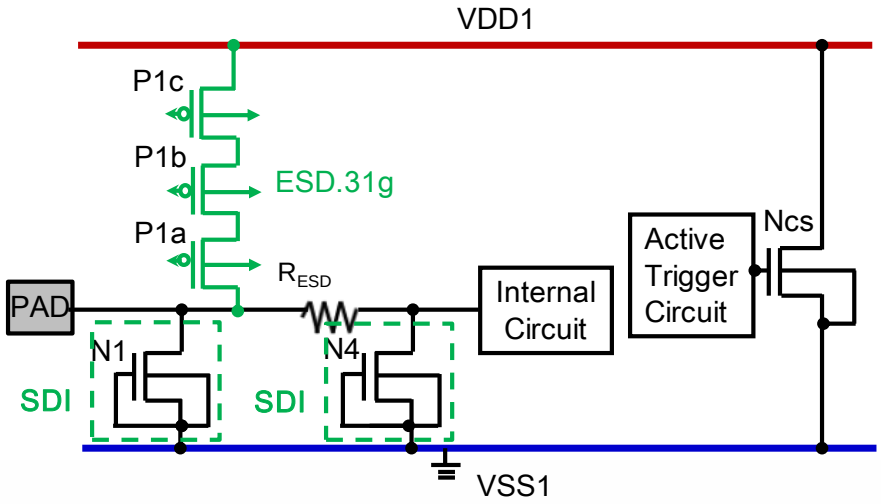


P-HIA diode

Restricted Rule for PMOS

- **PMOS must be “cascoded” as it is connected to IO PAD directly.**

Rule No.	Description
ESD.31g	As PMOS is connected between IO PAD and VDD/VSS PAD, the PMOS must be cascoded structure. (Figure 9.2.24) The PMOS after resistor will not be flagged by ESD.31g DRC checking. For CDM 5A application with snapback as primary ESD, 3-stage separated NW is must (refer to ESD.CDM.1gU and ESD.CDM.1.1gU). As for primary ESD protection with dual diode, 3-stage /2-stage separated OD is required for core/IO driver, respectively (refer to ESD.CDM.2gU).



ESD Resistor: resistance calculation

Resistance calculation

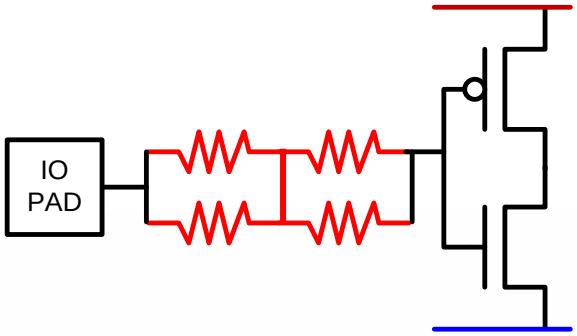
1. **Use SPICE model (TT corner, 25C, V=0.01V) to calculate resistance**

$$Ro = r_{sh}\frac{(L_{um} - dl)}{(W_{um} - dw)} \times \frac{1}{multi}$$

$$W_{um} = width\ in\ um\ ;\ L_{um} = length\ in\ um$$

2. **Variations are not considered in ESD.8g**

Rule No.	Description	Label	Op.	Rule
ESD.8gU	Value of resistor RESD (ohm) between internal circuits with gate oxide ESD path and IO pad. For snapback based ESD protection scheme, secondary ESD protection device total channel width multiplies with RESD resistor value should be ≥ 3200um*ohm. Also, primary ESD device and secondary ESD device should be on the common ground. This is checked by ESD.CDM.1gU, ESD.CDM.1.1gU and ESD.CDM.1.3gU.If the design is verified by ESD network calculator, it can be exempted.		≥	200



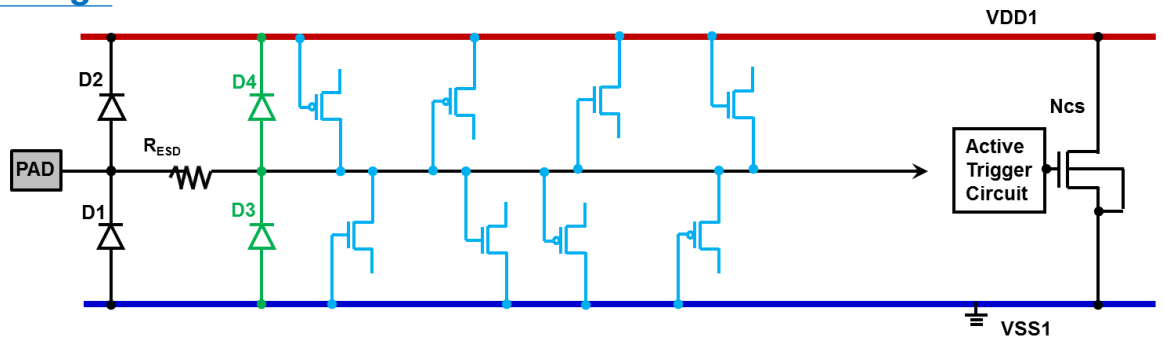
What will be regarded as input resistor:

1. **On the ESD device table**
2. **All input resistor on the same PAD to GATE path should be calculated together (parallel/serial) for ESD.8g checking**
3. **RES200 would not waive ESD.8g, if R<200ohm.**

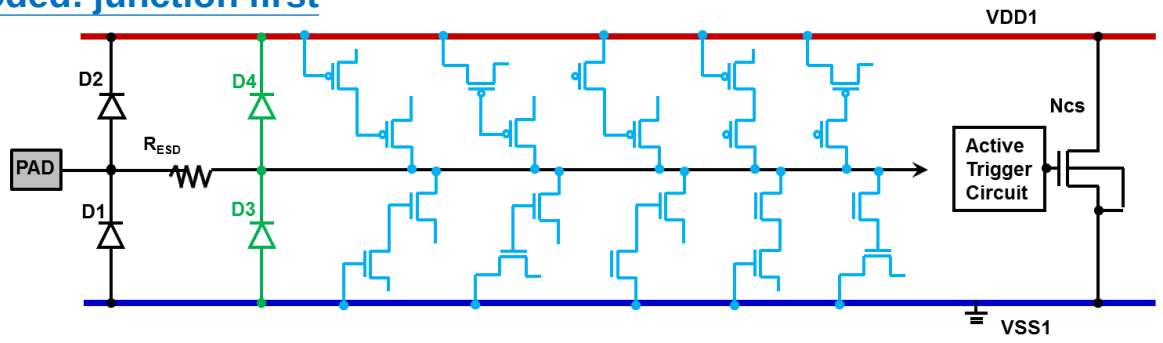
Secondary ESD Device Rule

Rule No.	Description
ESD.9.0g^{U}	Either MOS based or diode based secondary ESD protection (2nd ESD) with ESD resistor is required for internal circuits with gate oxide ESD path between IOPAD and power/ground PAD. This rule checks on internal circuits with single stage, 2-stage or >2-stage gate oxide ESD path to VDD/VSS. (Figure 9.2.16.1/9.2.16.2/9.2.16.3) For N/PMOS mixed scenario, it's checked as well. For 2nd ESD, HIANMOS (single stage and 2-stage cascoded) and HIA diodes can be used and needs to be put between resistor and the internal circuit. (N4 in Figure 9.2.17.1 and D3/D4 in Figure 9.2.17.2) This rule checks on MOS/MPODE gate. Exception: 1. Dummy device (D/G/S shorted) is exempted from this rule check. 2. Single stage or cascoded (2-stage) snapback NMOS as primary or secondary ESD protection. 3. Cascoded gate oxide ESD path [through one or more I/O GOX] with source or drain tied to IOPAD directly or through resistor and 2nd-stage tied to VDD or VSS. 4. Cascoded (> 2 stack) gate oxide ESD path with source or drain tied to IOPAD. ESD immunity highly depends on circuit design and real layout implantation, please ensure the MOS channel are turned off during ESD event and design is Si-proven before mass production.
ESD.9.0.1g^{U}	For 1.8V application, the secondary ESD protection device with ESD resistor is required for input path and it can be one of following listed devices. Single stage Drain-ballasted NMOS is not allowed. 1. 2-stage cascoded Drain-ballasted NMOS 2. HIA diode (single stage)
ESD.9.0.3g^{U}	Either MOS based or diode based secondary ESD protection (2nd ESD) with ESD resistor is required for internal circuits with gate oxide connected to IOPAD through single stage N/PMOS (pass gate/ transmission gate). For 2nd ESD, HIANMOS (single stage and 2-stage cascoded) and HIA diodes can be used and needs to be put between resistor and the internal circuit. (N4 in Figure 9.2.17.1 and D3/D4 in Figure 9.2.17.2) This rule checks on MOS/MPODE gate.
ESD.9.5g^{U}	Gate oxide connected to IOPAD directly or through resistor should be surrounded by a P+ guard ring. N/PMOS can share the same ring. This rule is checked in PERC LDL.

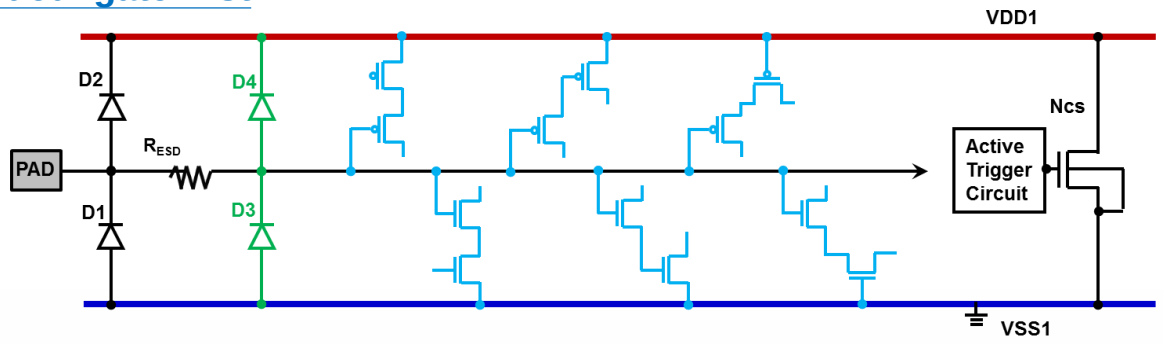
Single stage



Cascoded: junction first



Cascoded: gate first



Secondary ESD Device Rule

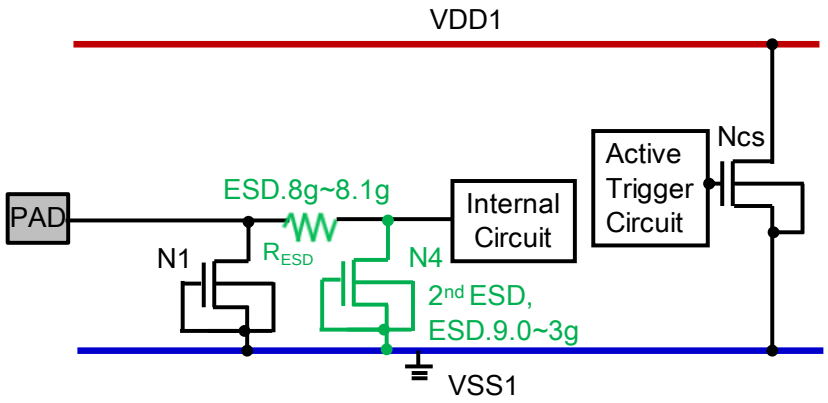
- **Methodology for ESD.9.0gU group/ESD.9.0.1gU/ESD.9.0.3gU:**

Single stage or cascoded	IO/ Core	1st stage scheme Gate first or junction first	2nd stage scheme Gate first or junction first	PERC ESD.9.0gU group (ESD.1.1gU, ESD.8gU, ESD.8.1gU & 2nd ESD CD/P2P)	Exception
Dummy device (D/G/S shorted)	IO/ Core	--	--	Exempted	--
Single stage	Pure IO	Gate first	--	Check	--
		Junction first	--	Check	1. nch_hia12* [drain tied to IOPAD directly; source/gate tied to same VSS directly]
	Pure Core	Don't care	--	Check	--
Cascoded (2-stage)	Pure Core, Pure IO or Mixed	Gate first	Don't care	Check	1. nch_hia12* [drain tied to IOPAD directly or through Resd]
		Junction first (s/d -> s/d)	Gate first	Check	--
			Junction first (s/d -> gate)	Check	1. Through one or more I/O GOX (s/d -> gate or gate -> s/d) directly or through resistor
		Junction first (s/d -> gate)	Don't care	Check	1. Through one or more I/O GOX (s/d -> gate or gate -> s/d) directly or through resistor
Cascoded (>2-stage)	Pure Core, Pure IO or Mixed	Gate first	Don't care	Check	--
		Junction first (s/d -> s/d)	Gate first	Check	--
			Junction first (s/d -> s/d or s/d -> gate)	Exempted	--
		Junction first (s/d -> gate)	Don't care	Exempted	--

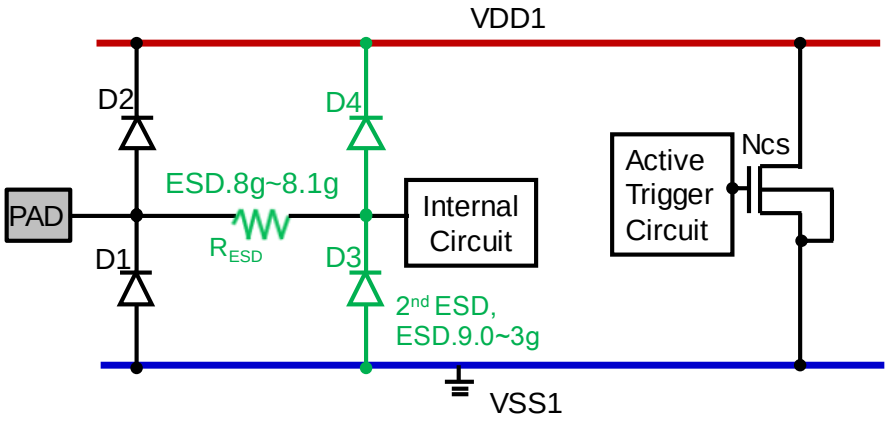
- **Consider N/PMOS mixed & Core/IO mixed.**
- **MPODE is checked as well.**

Secondary ESD Device Rule

Snapback MOS based 2nd ESD
(suggested for snapback MOS based primary protection)

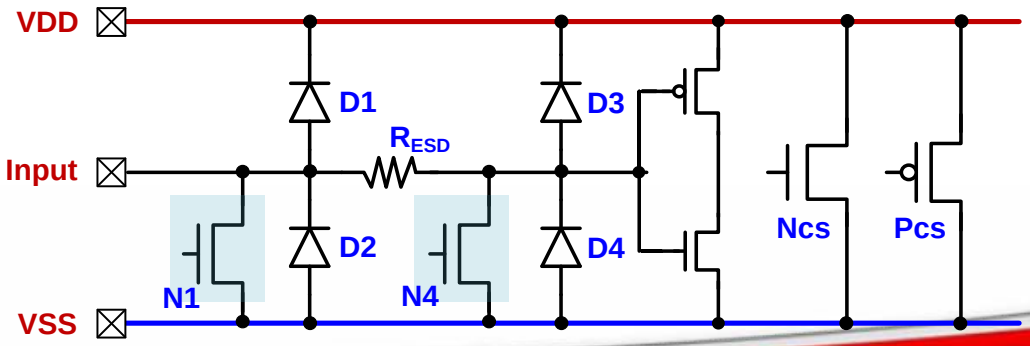


Diode based 2nd ESD
(suggested for diode based primary protection)



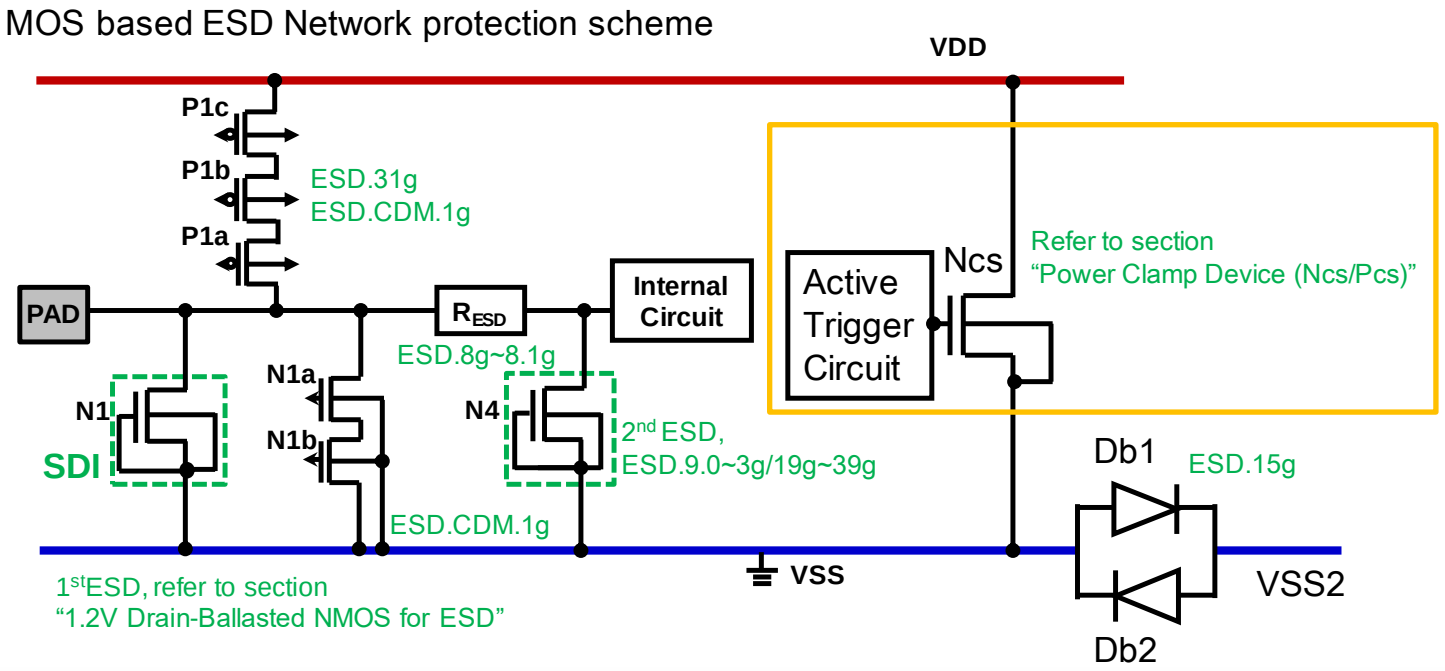
Secondary ESD Device Rule

Rule No.	Description	Label	Op.	Rule
ESD.9.1g^{U}	Channel length for single stage drain-ballasted NMOS (N4) and 2-stage cascoded drain-ballasted NMOS of MOS based ESD secondary protection (2nd ESD) in Figure 9.2.17.1. The drain-ballasted NMOS for 2nd ESD purpose needs to follow ESD.20g~ESD.26.1 and ESD.29g~ESD.39g in chap.9.2.6.3 and chap.9.2.6.4		=	0.1350
ESD.9.1.1g^{U}	Channel width for single stage drain-ballasted NMOS (N4) and 2-stage cascoded drain-ballasted NMOS of MOS based ESD secondary protection (2nd ESD) in Figure 9.2.17.1. The drain-ballasted NMOS for 2nd ESD purpose needs to follow ESD.20g~ESD.26.1 and ESD.29g~ESD.39g in chap.9.2.6.3 and chap.9.2.6.4. For snapback based ESD protection scheme, secondary ESD protection device total channel width multiplies R_{ESD} resistor value should be ≥ 3200um*ohm. Also, primary ESD device and secondary ESD device should be on the common ground. This is checked by ESD.CDM.1gU, ESD.CDM.1.1gU and ESD.CDM.1.3gU.		≥	4
ESD.9.1.2g^{U}	Unit OD width of single stage drain-ballasted NMOS (N4) and 2-stage cascoded drain-ballasted NMOS of MOS based ESD secondary protection (2nd ESD) in Figure 9.2.17.1. The drain-ballasted NMOS for 2nd ESD purpose needs to follow ESD.20g~ESD.26.1 and ESD.29g~ESD.39g in chap.9.2.6.3 and chap.9.2.6.4.		=	0.0900
ESD.9.1.3g^{U}	2-stage cascoded drain-ballasted NMOS of MOS based ESD secondary protection (2nd ESD) needs to be common OD structure			
ESD.9.3g^{U}	Total perimeter of HIA diode (D3/D4) of diode based ESD secondary protection (2nd ESD) in Figure 9.2.17.2, the perimeter calculation align with HIA diode.		≥	4



Power Clamp Rule

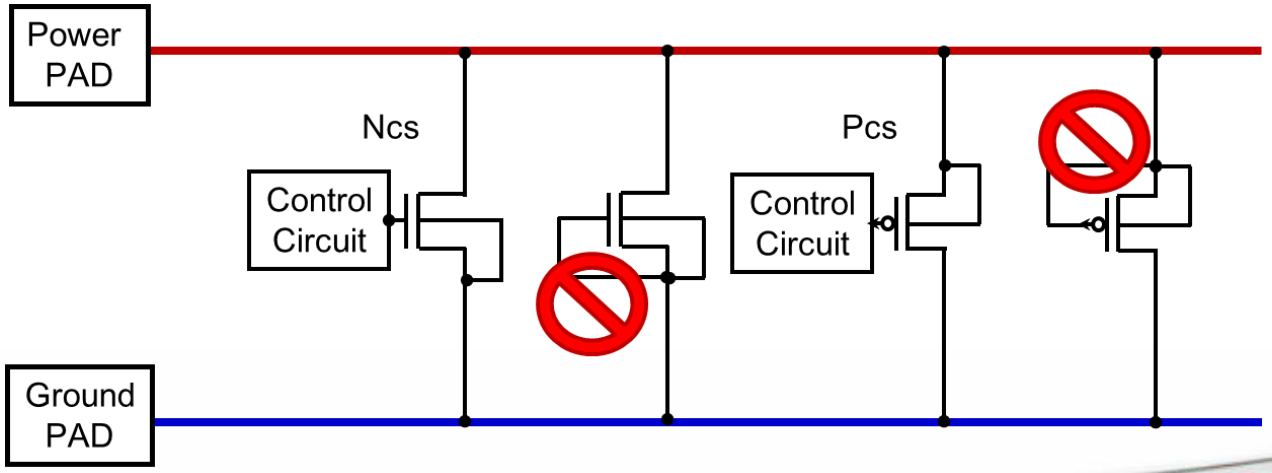
- **The Active Power Clamp is required to put between Power and Ground buses. The Active Power Clamp consists of trigger circuit components and clamp device components (Ncs/Pcs).**



Power Clamp Rule

- **Single Stage Power Clamp**

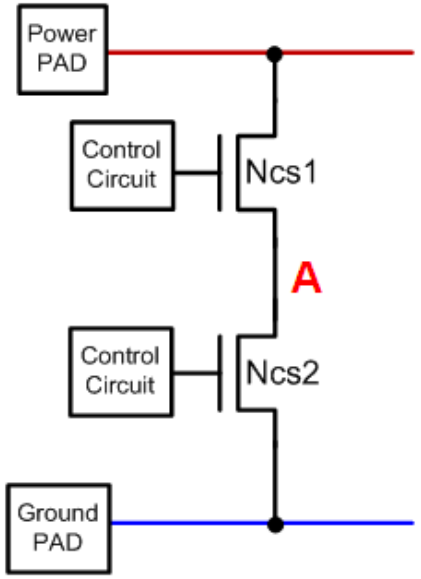
1. **On the ESD device table**
2. **Have specific connection**
    1. **PMOS (Pcs) Source and Bulk connected to same Power Net**
    2. **PMOS (Pcs) Drain connected to Ground Net**
    3. **NMOS (Ncs) Source and Bulk connected to same Ground Net**
    4. **NMOS (Ncs) Drain connected to Power Net**
    5. **Gate is NOT directly connected to Ground/Power Net**



Power Clamp Rule

- 2-stage NMOS Power Clamp
- For 1.8V application power pad, cascoded power clamp is needed and is checked by PERC.

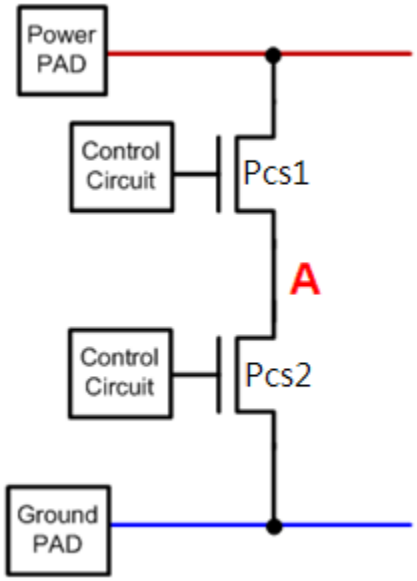
1. 1.2V NMOS defined in the ESD device table
2. Have specific connection
    1. 2-stage NMOS with one NMOS's (Ncs1) drain side connecting to power net and the other NMOS's (Ncs2) source side connecting to ground net.
    2. Gate is NOT directly connected to Power/Ground/Signal Net.
    3. For Node A, it can be a true power net or an internal net which does not connect to neither NMOS gate nor PMOS gate.
    4. If Node A is a true power net, bulk of Ncs1 can be connected to net A or ground net as Ncs2's source. If Node A is a internal net, bulk of Ncs1 need to connect to ground net as Ncs2's source. For bulk of Ncs2, it needs to connected to ground net as Ncs2's source.
3. Cascoded core NMOS power clamp is NOT recognized by PERC.
4. If one power net exists rule-complied single stage power clamp, no checking of cascoded power clamp rules.



Power Clamp Rule

- 2-stage PMOS Power Clamp
- For 1.8V application power pad, cascoded power clamp is needed and is checked by PERC.

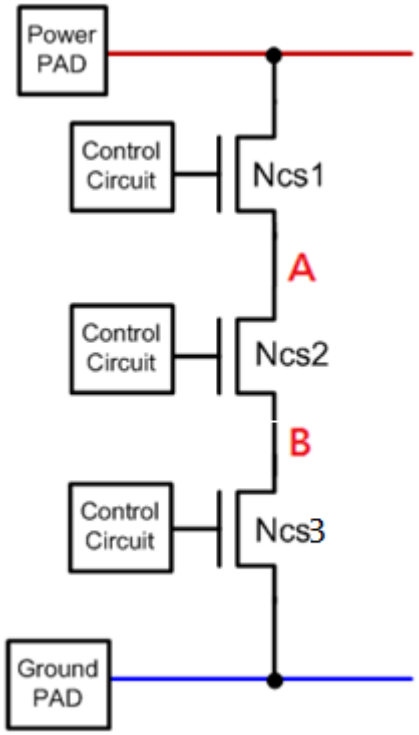
1. 1.2V PMOS defined in the ESD device table
2. Have specific connection
    1. 2-stage PMOS with one PMOS's (Pcs1) source side connecting to power net and the other PMOS's (Pcs2) drain side connecting to ground net.
    2. Gate is NOT directly connected to Power/Ground/Signal Net.
    3. For Node A, it can be a true power net or an internal net which does not connect to neither NMOS gate nor PMOS gate.
    4. If Node A is a true power net, bulk of Pcs2 can be connected to net A or power net as Pcs1's source. If Node A is a internal net, bulk of Pcs2 need to connect to power net as Pcs1's source. For bulk of Pcs1, it needs to connected to power net as Pcs1's source.
3. Cascoded core PMOS power clamp is NOT recognized by PERC.
4. If one power net exists rule-complied single stage power clamp, no checking of cascoded power clamp rules.



Power Clamp Rule

- 3-stage NMOS Power Clamp
- For 3.3V application power pad, 3-stage power clamp is needed and is checked by PERC.

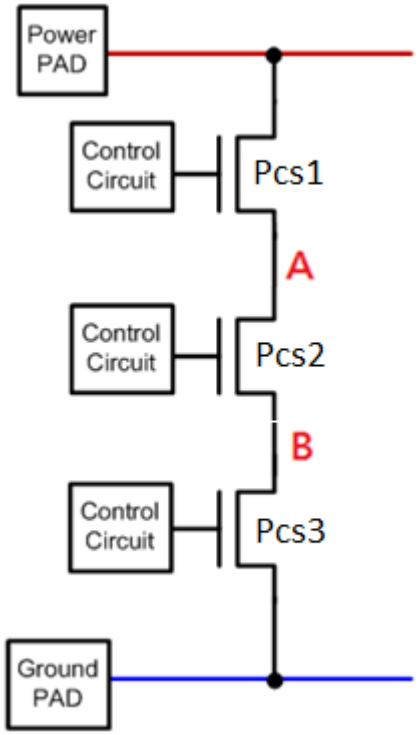
1. 1.2V/1.5V NMOS defined in the ESD device table
2. Have specific connection
    1. 3-stage NMOS with one NMOS's (Ncs1) drain side connecting to power net and the other NMOS's (Ncs3) source side connecting to ground net.
    2. Gate is NOT directly connected to Power/Ground/Signal Net.
    3. For Node A/B, it should be an internal net which does not connect to neither NMOS gate nor PMOS gate.
    4. Ncs1/Ncs2/Ncs3 should be in Deep-Nwell. Besides, bulk of Ncs1 needs to connect to node A, and bulk of Ncs2 needs to connected to node B. For bulk of Ncs3, it needs to connected to ground net as Ncs3's source.
3. Cascoded core NMOS power clamp is NOT recognized by PERC.
4. If one power net exists rule-complied single stage power clamp, no checking of cascoded power clamp rules.



Power Clamp Rule

- 3-stage PMOS Power Clamp
- For 3.3V application power pad, 3-stage power clamp is needed and is checked by PERC.

1. 1.2V/1.5V PMOS defined in the ESD device table
2. Have specific connection
    1. 3-stage PMOS with one PMOS's (Pcs1) source side connecting to power net and the other PMOS's (Pcs3) drain side connecting to ground net.
    2. Gate is NOT directly connected to Power/Ground/Signal Net.
    3. For Node A/B, it should be an internal net which does not connect to neither NMOS gate nor PMOS gate.
    4. Bulk of Pcs2 need to connect to power net as Pcs1's source. For bulk of Pcs1, it needs to connected to power net as Pcs1's source. PERC will not check the connection of Pcs3's bulk. *If the Pcs3's bulk connect to power net as Pcs1's source, the reliability of the Pcs3's gate oxide can sustain ≤3V application but not 3.3V application.* Please run simulation to make sure the design can pass reliability.
3. Cascoded core PMOS power clamp is NOT recognized by PERC.
4. If one power net exists rule-complied single stage power clamp, no checking of cascoded power clamp rules.



Exclude power clamp recognition by cell names

- **Users can exclude power clamp recognition by defining cell names in perc_n03_xxx.top file :**

//VARIABLE EXCLUDE_PC_CELL “”

// define cell names to be excluded for power clamp recognition (e.g. "CELL_A" "CELL_B")

// the used cell names should be defined in hcell to preserve hierarchy

Power Clamp Rule

Rule No.	Description	Label	Op.	Rule
ESD.40g	Total **fin number** of I/O Power Clamp (in OD2) in same connection of Power PAD. (Except PODE_GATE (206;28)) (Ncs/Pcs in Figure 9.2.25, 9.2.26) This rule checks on power PAD only.		≥	76400
ESD.40.1g	Total **fin number** of core Power Clamp in same connection of Power PAD. (Except PODE_GATE (206;28)) (Ncs/Pcs in Figure 9.2.25, 9.2.26) This rule checks on power PAD only.		≥	84000
ESD.40.2g^{U}	Total **fin number** of 1.8V Power Clamp in same connection of Power PAD. The suggested 1.8V Power Clamps can be formed by 2-stack cascoded 1.2V NMOS. (Ncs in Figure 9.2.25)		≥	84000
ESD.40.3.1g^{U}	Total **fin number** of the unit cell power clamp (unit cell: group of devices close to each other)		≥	15200
ESD.42g	Channel length: I/O Power Clamp (in OD2)	L	=	0.055~0.135
ESD.42.1g^{U}	Channel length: 1.8V Power Clamp (cascoded 1.2V NMOS in OD2)	L	=	0.055~0.135
ESD.42.2g	Channel length: core Power Clamp (not in OD2)	L	=	0.055~0.100
ESD.43g^{U}	Each set of VDD and VSS must have its own power clamp cells and active Power Clamp is required (Figure 9.2.25)			

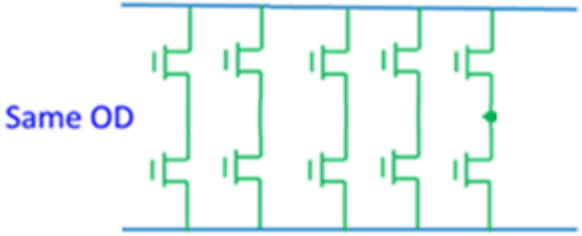
ESD guidelines for 3.3V application

Rule No.	Description	Label	Op.	Rule
ESD.NET.1.2g^{U}	For 3.3V I/O pin ESD protection scheme, the primary ESD protection (1st ESD) devices are required and it should be realized by P-HIA and NT_N-HIA diode. Drain-ballasted NMOS (single-stage and cascaded) and N-HIA (NOT NT_N) diode are not allowed.			
ESD.9.0.2g^{U}	For 3.3V application, the secondary ESD protection device with ESD resistor is required for input path and it should be realized by P-HIA diode and NT_N N-HIA diode. Drain-ballasted NMOS (single-stage and cascaded) and N-HIA (NOT NT_N) diode are not allowed.			
ESD.40.4g^{U}	Total fin number of 3.3V Power Clamp in same connection of Power PAD. 3.3V Power Clamps can be formed by 3-stack cascoded 1.2V PMOS or 3-stack cascoded 1.2V NMOS, these 1.2V NMOS of 3-stacked should be in Deep-Newll.		≥	143000

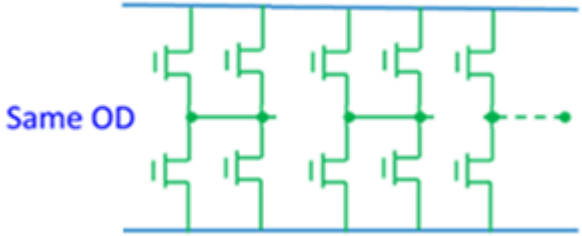
2-stack ESD devices with same-OD layout style

- Due to the current N3 layout constraints, some number of MOS must share the same middle net for 2-stack MOS with same-OD layout style.
  - 2-stack same-OD **HIANMOS (1st/2nd ESD)**
  - 2-stack same-OD **Power Clamp**
- There is a variable to constrain ***the finger number of the middle-net shorted MOS*** for 2-stack ESD devices. And the default value is **≤ 2** and defined in **perc_n03_constant.tcl**.
- This variable varies from same-OD layout styles; users could modify this variable as long as the process rules are clean for their same-OD layout styles.

The finger number of the middle-net shorted MOS = 1



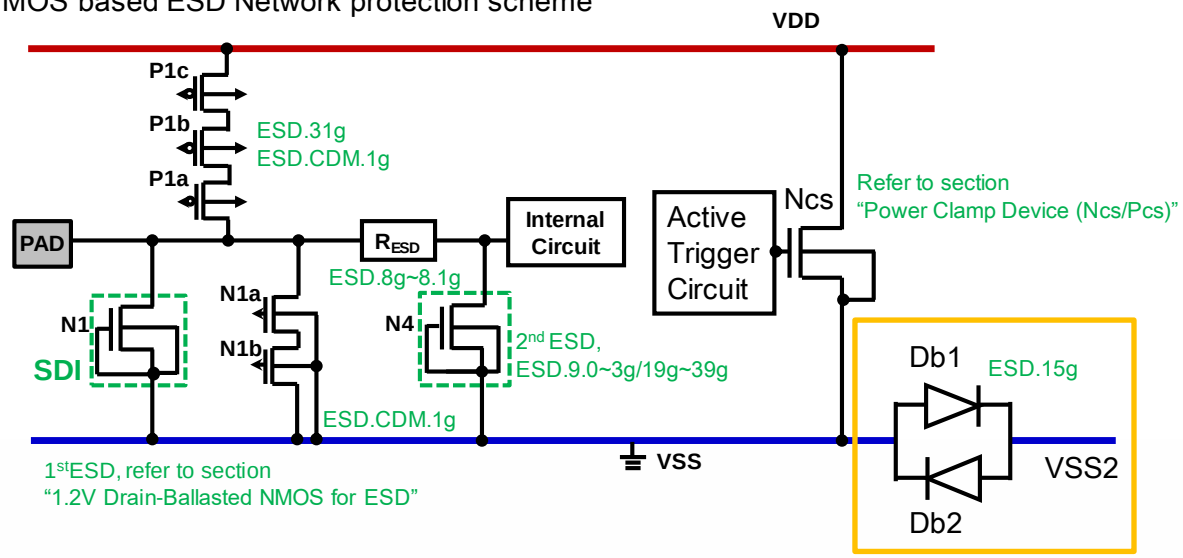
The finger number of the middle-net shorted MOS = 2

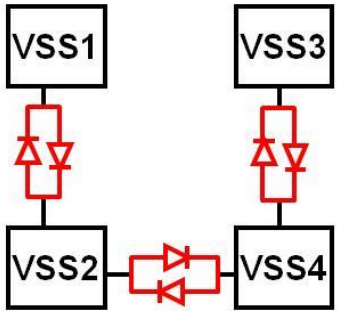


Back to Back Diode

Rule No.	Description	Label	Op.	Rule
ESD.15g[U]	Bypass discharge cells should be inserted between each separate VSS to avoid ESD damage to internal circuits. The suggested bypass discharge cell is back to back diode (Figure.9.2.21) and it can be HIA diode. The perimeter of back to back diodes (Db1/Db2) needs to meet HIA.3g The connections are illustrated in Figure 9.2.20. (For more details, please see the “Tips for the Power Protection” section in this chapter.)			

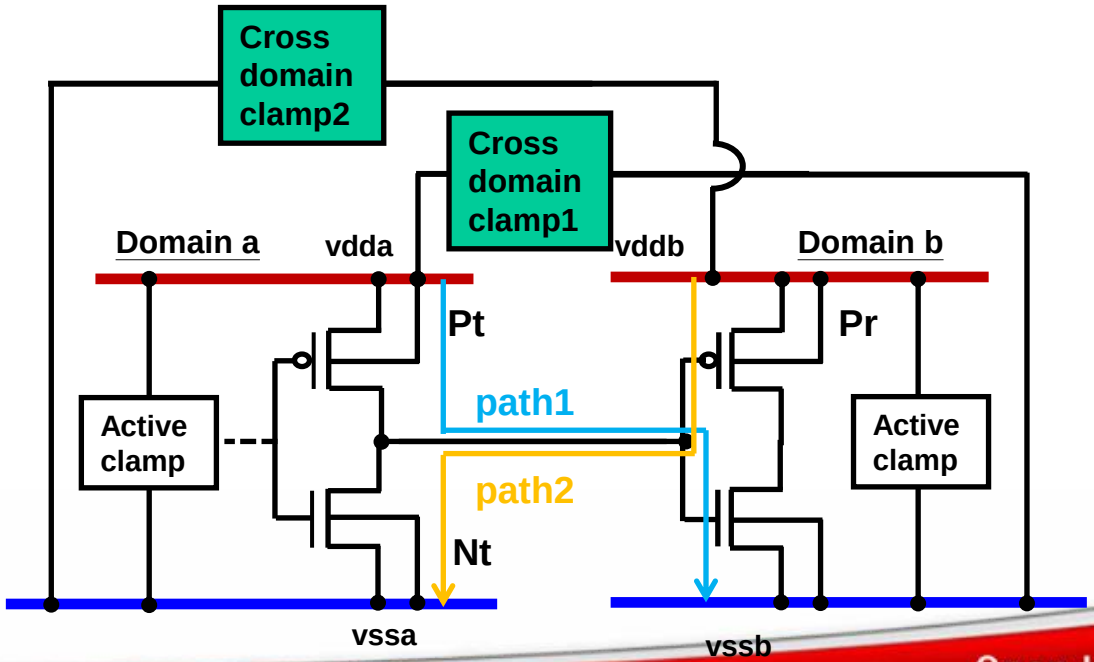
MOS based ESD Network protection scheme





Cross Domain Detection

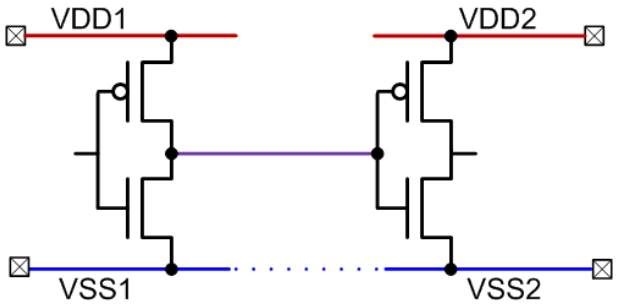
- PERC detects power /ground information from source/drain of MOS and mark it as the path 1 & path 2.
- If no cross domain power clamp exist in path 1 or path2, it will be marked as the cross domain.
- PERC flags if checking path only has one PMOS and NMOS without cross domain ESD protection device.



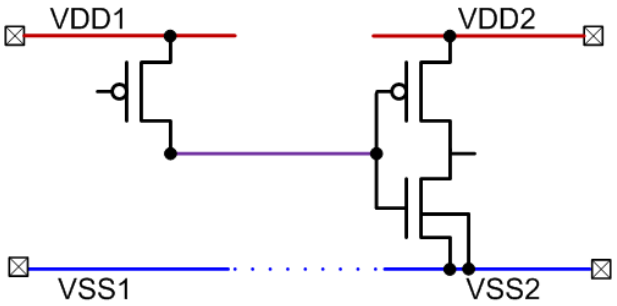
Cross Domain Definition

- If transceiver and receiver side are single NMOS, single PMOS, or both of them, then cross domain protection device is needed.

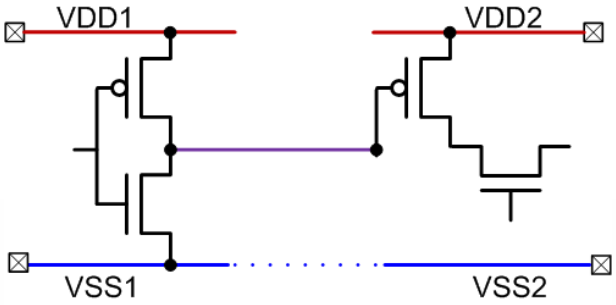
Transceiver: single NMOS and PMOS
Receiver: single NMOS and PMOS



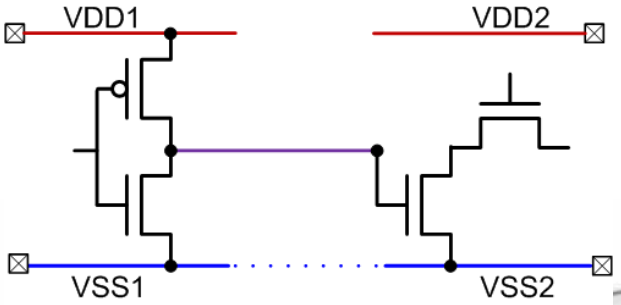
Transceiver: single PMOS
Receiver: single NMOS and PMOS



Transceiver: single NMOS and PMOS
Receiver: single PMOS

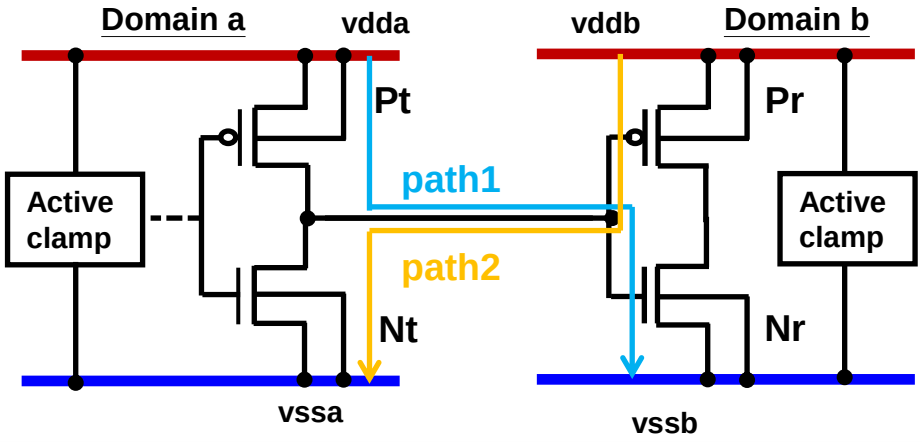


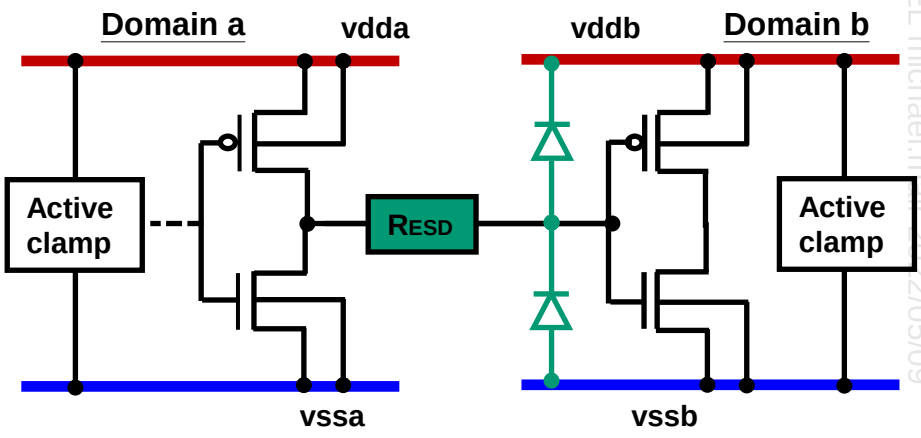
Transceiver: single NMOS and PMOS
Receiver: single NMOS



Cross Domain Check Methodology

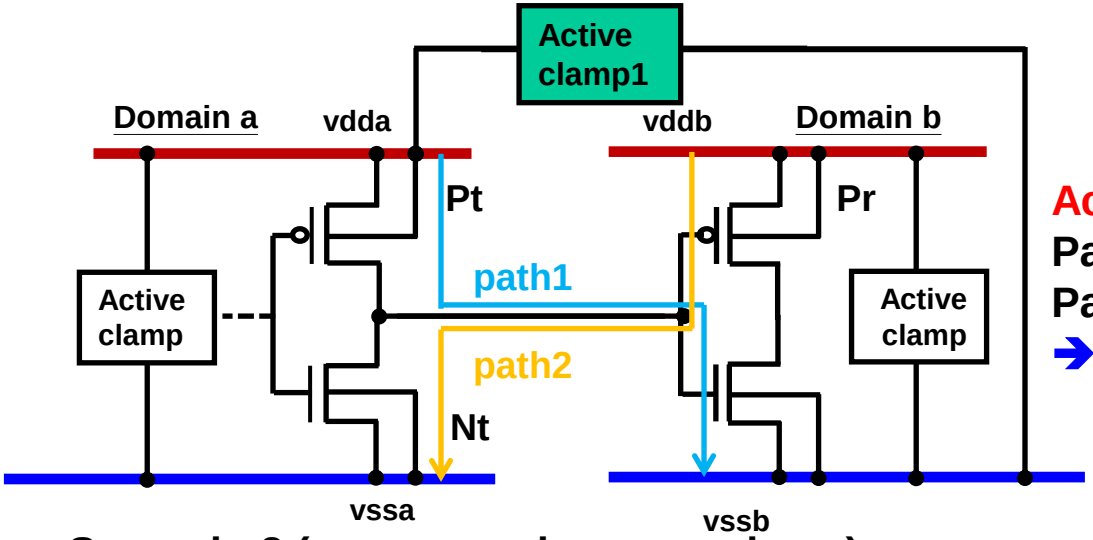
- Highlight violation path (path 1 or path 2) in RVE.
- The cross domain protection device for:
  - Path 1: R_{ESD} and dual diode are must
  - Path 2: R_{ESD} and dual diode are must





Cross Domain Check Methodology

Scenario 1 (cross couple power clamp)



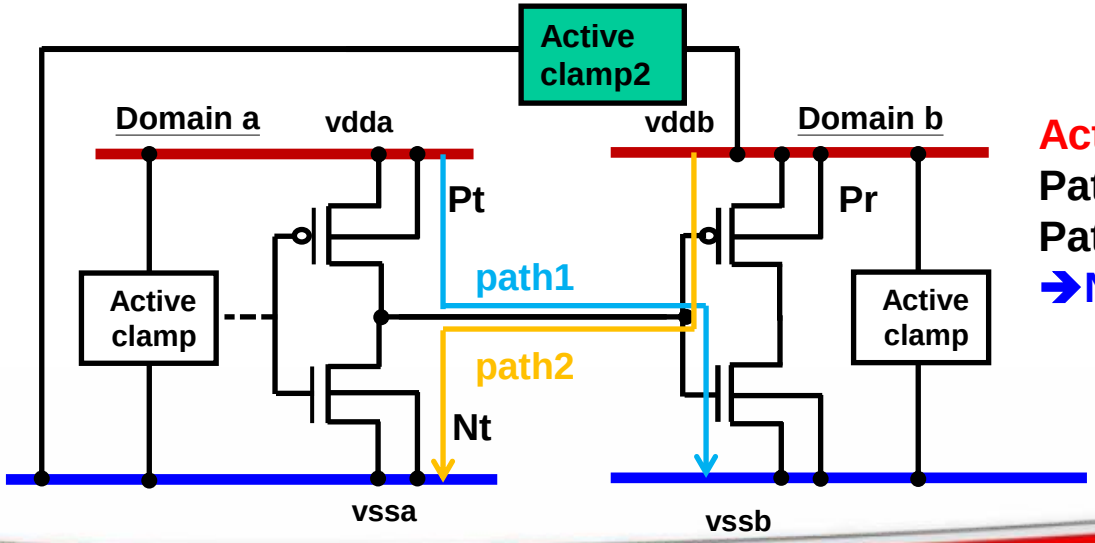
Active clamp1 meets ESD total width rule

Path 1: R_{ESD} and 2nd ESD are no needed

Path 2: R_{ESD} and 2nd ESD are needed

➔Need to put R_{ESD} and 2nd ESD

Scenario 2 (cross couple power clamp)



Active clamp2 meets ESD total width rule

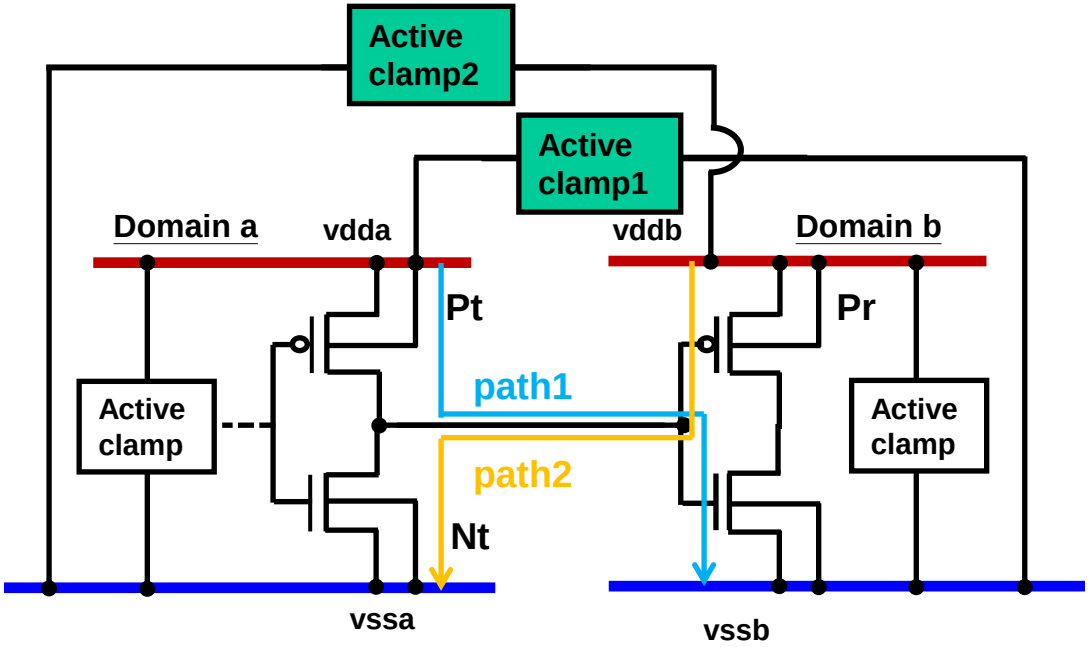
Path 1: R_{ESD} and 2nd ESD are needed

Path 2: R_{ESD} and 2nd ESD are no needed

➔Need to put R_{ESD} and 2nd ESD

Cross Domain Check Methodology

Scenario 3 (cross couple power clamp)



Active clamp1&2 meet ESD total width rule

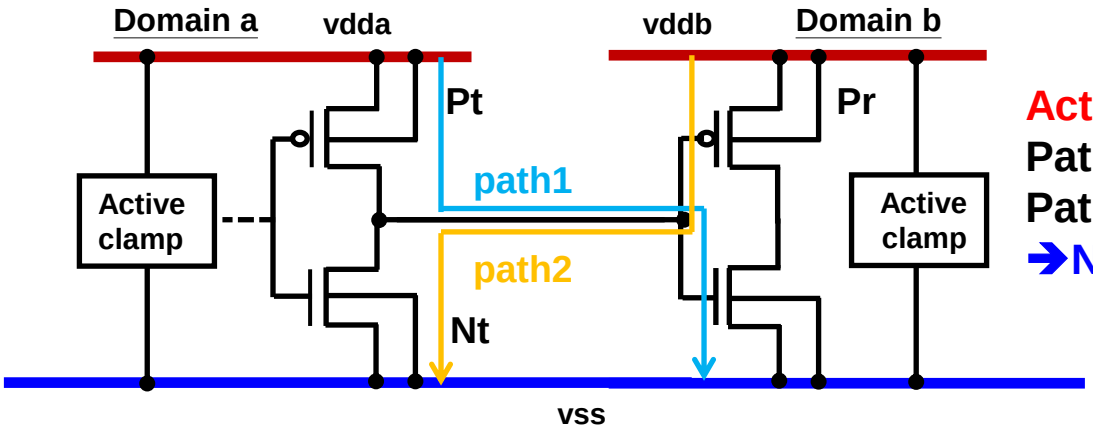
Path 1: R_{ESD} and 2nd ESD are no needed

Path 2: R_{ESD} and 2nd ESD are no needed

➔No need to put R_{ESD} and 2nd ESD.

Cross Domain Check Methodology

Scenario 4 (common ground)



Active clamp meet ESD total width rule

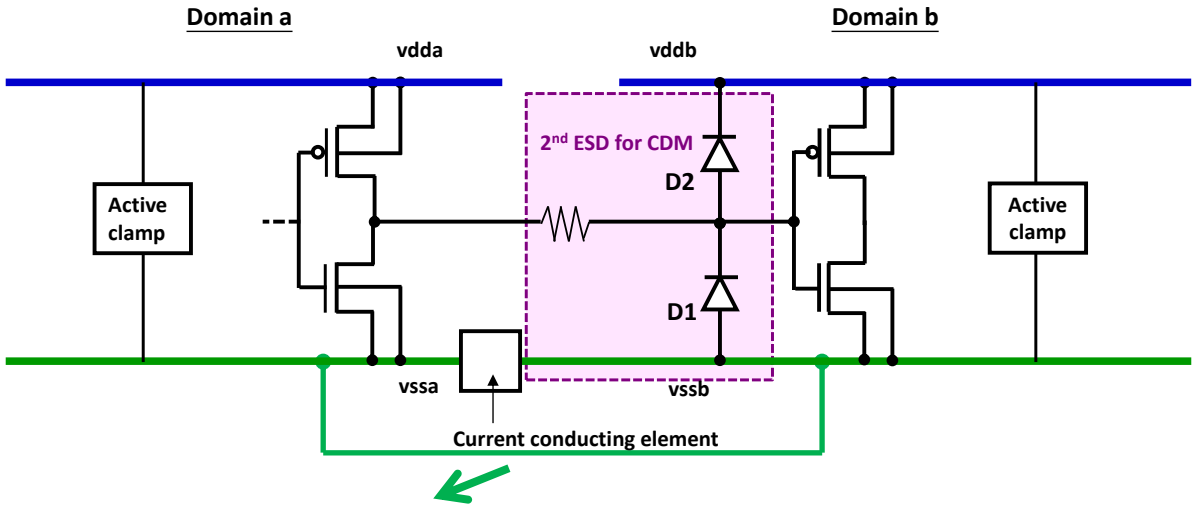
Path 1: R_{ESD} and 2nd ESD are no needed

Path 2: R_{ESD} and 2nd ESD are no needed

➔No need to put R_{ESD} and 2nd ESD.

Cross Domain CDM ESD Rules

Rule No.	Description	Label	Op.	Rule
ESD.45.0g[U]	1. For cross domain with separated grounds (Fig. 9.2.33.2), diode based secondary protection with interface resistor is required at interface. (D1/D2 in Figure 9.2.33.2). 2. If the receiver is I/O device, the secondary protection is not required. 3. As the cross domain with on-rule power clamp added between vdda and vssb, the secondary protection is not required. For COMMON_GROUND protection scheme, this rule can be disable. Checker will skip this rule.			



If vssa is direct short to vssb, the 2nd ESD is not required.
If vssa is not direct short to vssb, the back to back diode, R_{ESD} and 2nd ESD are required.

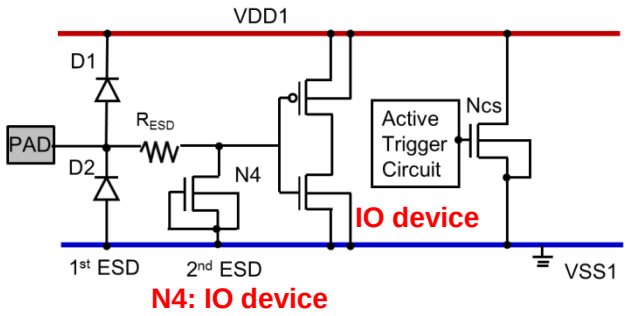
Cross Domain CDM ESD Rules

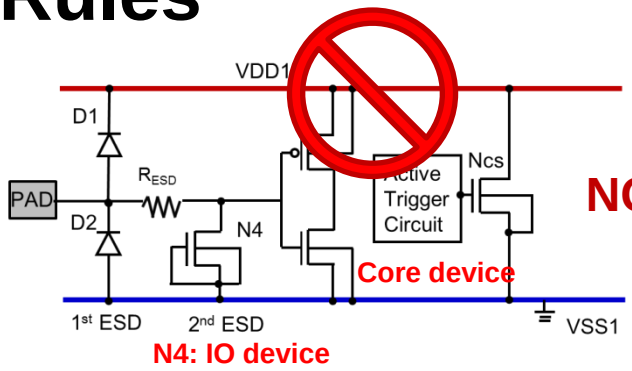
Rule No.	Description	Label	Op.	Rule
ESD.45.0g^{U}	1. For cross domain with separated grounds (Fig. 9.2.33.2), diode based secondary protection with interface resistor is required at interface. (D1/D2 in Figure 9.2.33.2). 2. If the receiver is I/O device, the secondary protection is not required. 3. As the cross domain with on-rule power clamp added between vdda and vssb, the secondary protection is not required. For COMMON_GROUND protection scheme, this rule can be disable. Checker will skip this rule.			
ESD.45.0.1g^{U}	Single stage N/PMOS in series under cross domain scenario is not allowed. As cross domain with on-rule power clamp, this rule can be waived. (Fig. 9.2.33.4) For COMMON_GROUND protection scheme, this rule can be disable. Checker will skip this rule.			
ESD.45.0.2g^{U}	Cascoded (2-stage) N/PMOS under cross domain scenario is not allowed. As cross domain with on-rule power clamp, this rule can be waived. (Fig. 9.2.33.5) For COMMON_GROUND protection scheme, this rule can be disable. Checker will skip this rule.			
ESD.45.1g^{U}	Total perimeter of cross-domain diode based secondary protection. (D1/D2 in Figure 9.2.33.2) For COMMON_GROUND protection scheme, this rule can be disable. Checker will skip this rule.		≥	4
ESD.47g^{U}	Recommended interface voltage clamping resistor resistance for cross-domain with separated ground (resistor in Figure 9.2.33.1~2) For COMMON_GROUND protection scheme, this rule can be disable. Checker will skip this rule.		≥	200

ESD MOS Protection Rules

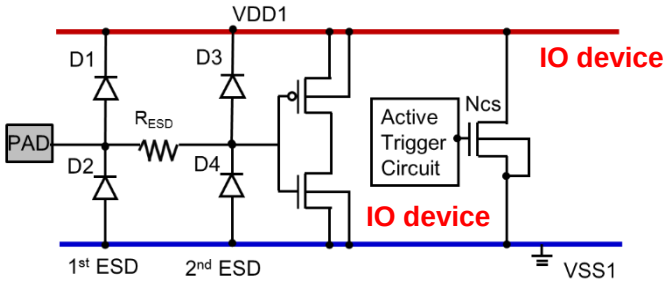
Rule No.	Description	Label	Op.	Rule
ESD.1.1g^{U}	Use thick oxide transistor for thick oxide secondary ESD protection (2nd ESD, N4). (Figure 9.2.14) For diode based 2nd ESD protection, use thin oxide transistor (Mp/Mn) for thin oxide power clamp (Ncs); use thick oxide transistor (Mp/Mn) for thick oxide power clamp (Ncs) (Fig 9.2.14.1) Thick oxide ESD protection or power clamp connect to thin oxide transistor is not allowed. Both input pin and cross domain 2nd ESD are required to comply with this rule.			

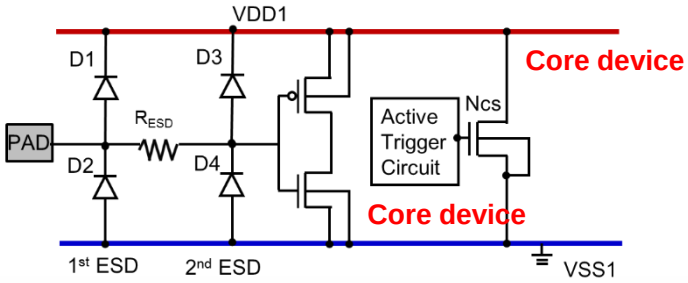
ESD MOS Protection Rules

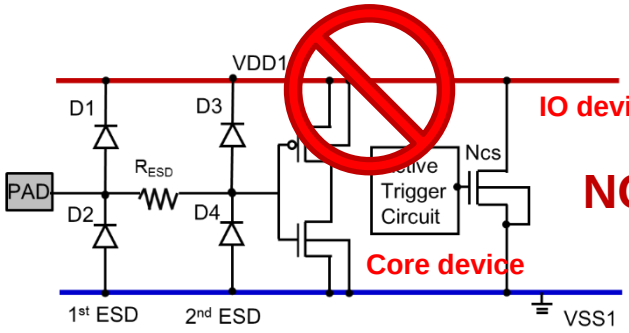




NOT ALLOWED!







NOT ALLOWED!

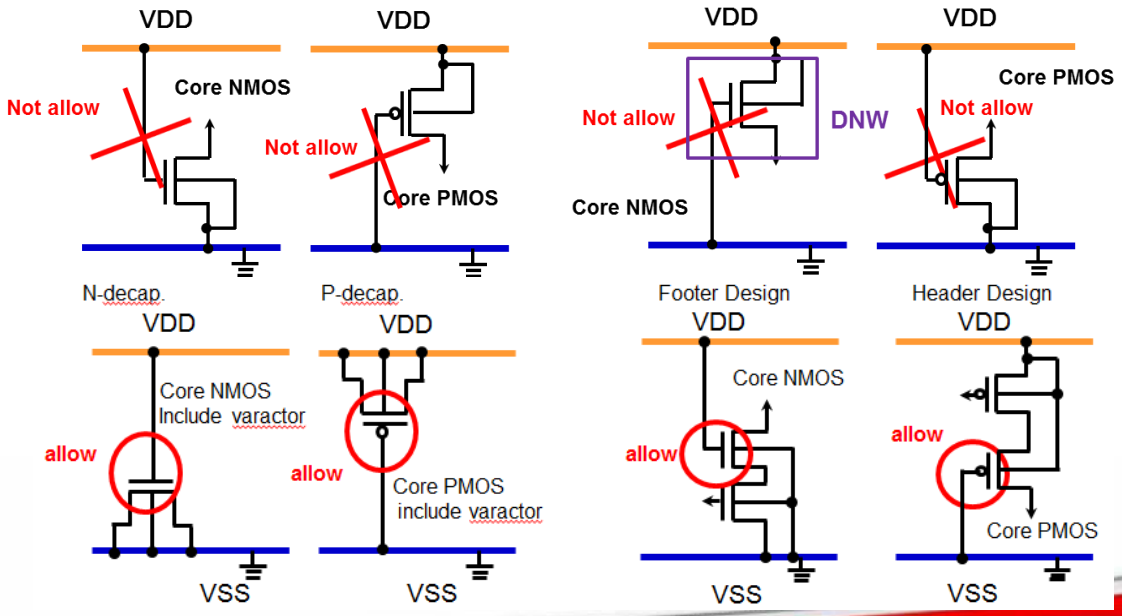
◆ Core MOS protecting IO MOS is allowed in PERC, however, please take care about the reliability issue.

ESD MOS Protection Rules

- **PERC use following methodology to judge the type of GOX ESD path.**
  - For single stage, core or I/O GOX ESD path is judged by the device type directly.
  - For 2-stage cascode, it is judged by the crossed GOX type
    - For I/O, core mixed type, treat it as I/O GOX ESD path
    - For pure core type, treat it as core GOX ESD path
    - For pure I/O type, treat it as I/O GOX ESD path
  - For > 2-stage cascode, it is judged by the device connected to PAD directly
- **For core GOX ESD path,**
  - I/O GGNMOS 2nd ESD is not allowed.
  - With dual diode 2nd ESD, power clamp should be core type.
- **For I/O GOX ESD path,**
  - I/O GGNMOS is okay.
  - With dual diode 2nd ESD, power clamp can be core or I/O type.

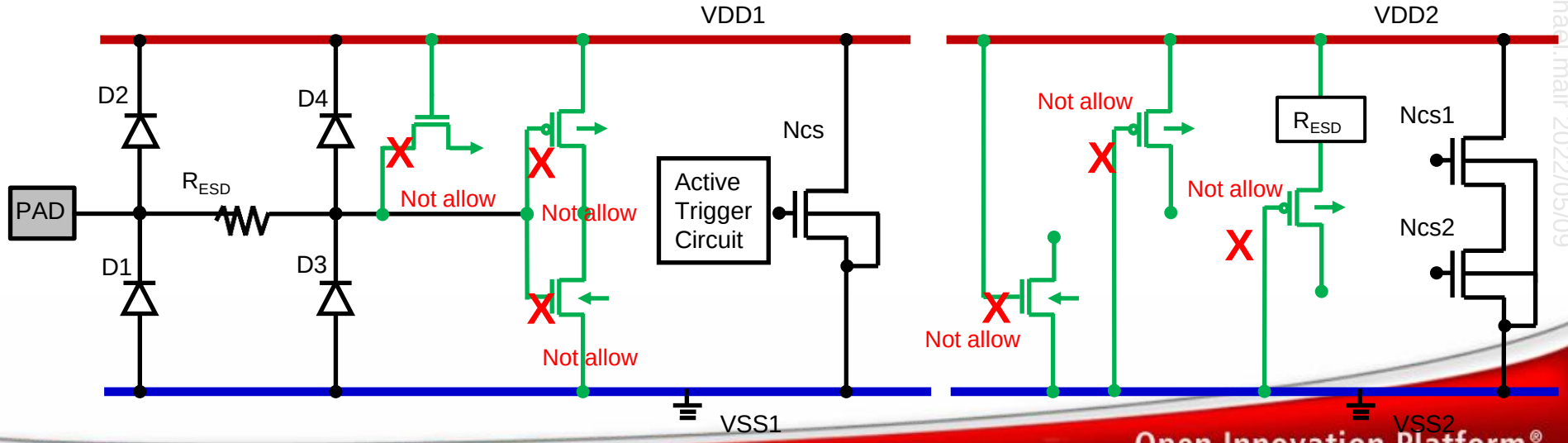
ESD MOS Protection Rules

Rule No.	Description	Label	Op.	Rule
ESD.WARN.3g^{U}	If the circuits have core gate directly tie to VDD(VSS) and source/drain tie to VSS(VDD), rules below must be followed to get the ESD design scheme robust. (Figure 9.2.11) 1. ESD.14.4g, ESD.40.1g and ESD.43g for HBM 2. ESD.CDM.P.3gU, ESD.CDM.P.7.1.1gU, ESD.CDM.P.7.1.2gU, ESD.40.1g, ESD.43gU, ESD.CDM.C.2gU and ESD.CDM.C.3.1gU for CDM This rule checks on MOS/MPODE gate. Dummy device (D/G/S shorted) is exempted from this rule check. As for Decap and footer/header design, they can be exempted.			



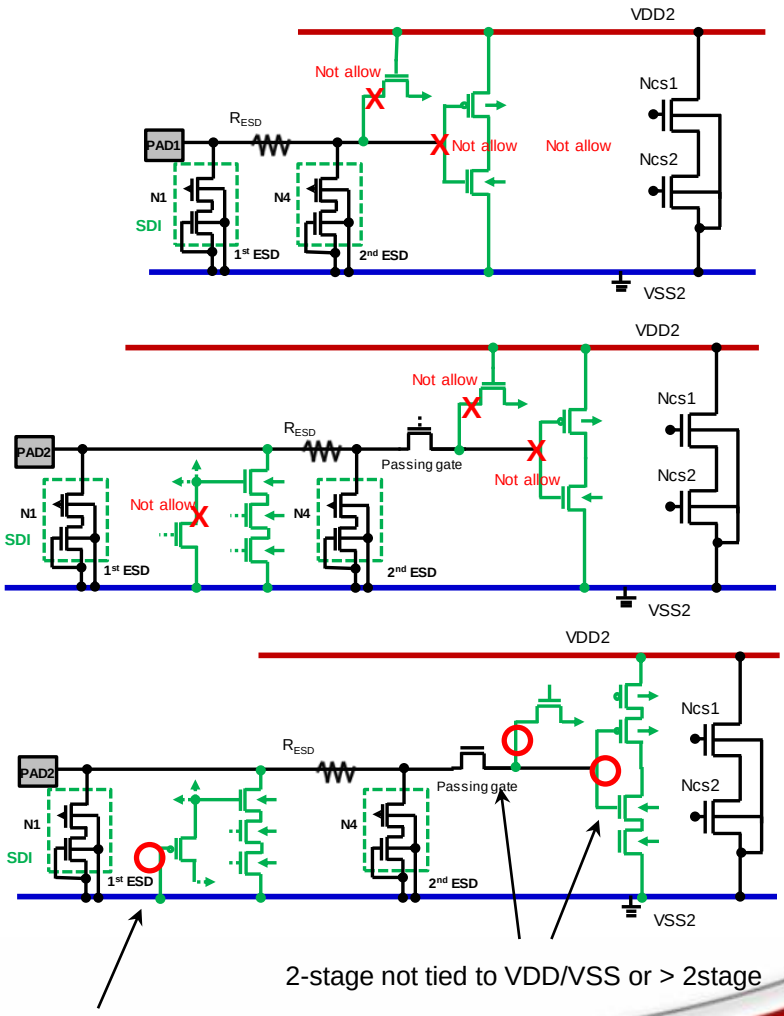
ESD MOS Protection Rules

Rule No.	Description
ESD.WARN.3.1g^{U}	As core gate connects to IOPAD directly or through resistor, the source/drain cannot connect to any power/ground directly or through resistor. As source/drain connects to IOPAD directly or through resistor, the core gate cannot connect to any power/ground directly or through resistor. (Figure 9.2.12.1) This rule checks on MOS/MPODE gate. Dummy device (D/G/S shorted) is exempted from this rule check. ESD immunity highly depends on circuit design and real layout implantation, please ensure the MOS channel are turned off during ESD event and design is Si-proven before mass production.
ESD.WARN.4.2g^{U}	For cascoded power clamp protected power domain, As I/O gate connects to power directly, the source/drain cannot connect to ground directly. As source/drain connects to power directly or through resistor, the I/O gate cannot connect to ground directly. (Figure 9.2.13.2). This rule checks on MOS/MPODE gate. Exception: 1. Dummy device (Drain/Gate/Source shorted) is exempted from this rule check. 2. 1.8V PMOS Capacitor (I/O PMOS with Drain/Source/Bulk shorted) is exempted from this rule check.



ESD MOS Protection Rules

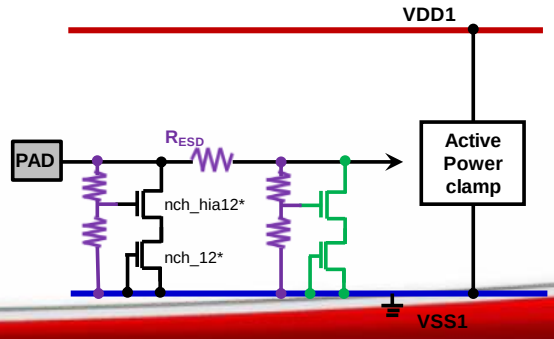
Rule No.	Description
ESD. WARN.4.1g^{U}	For cascoded (2-stage) snapback based primary protection, all gate oxide ESD path should be ≥ 3 stage between IOPAD and power/ground. Pure core GOX path is not allowed. For >3stage design, this rule only checks on first three stages. Resistor between IOPAD and the first stage of gate oxide ESD path is ignored. (Figure 9.2.13.1) Exception: 1. Dummy device (D/G/S shorted) is exempted from this rule check. 2. Cascoded (2-stage) snapback NMOS as primary or secondary ESD protection is exempted. 3. Gate oxide ESD path through two or more I/O gate oxide. This rule checks on MOS/MPODE gate. ESD immunity highly depends on circuit design and real layout implantation, please ensure the MOS channel are turned off during ESD event and design is Si-proven before mass production.



ESD.WARN.4.1g Methodology

- **Consider N/PMOS mixed & Core/IO mixed.**
- **MPODE is checked as well.**

Single stage or cascoded	IO/ Core	1st stage scheme Gate first or junction first	2nd stage scheme Gate first or junction first	PERC ESD.WARN.4.1g	Exception
Dummy device (D/G/S shorted)	IO/ Core	--	--	Exempted	--
Single stage	Pure IO	Don't care	--	Check	1. Cascoded snapback NMOS for primary or 2nd ESD protection
	Pure Core	Don't care	--	Check	--
Cascoded (2-stage)	Pure Core, Pure IO or Mixed	Gate first	Don't care	Check	1. Cascoded snapback NMOS for primary or 2nd ESD protection 2. Both 1st/2nd stage are through IO GOX (s/d -> gate or gate -> s/d)
		Junction first (s/d -> s/d)	Gate first	Check	--
			Junction first (s/d -> gate)	Check	1. Cascoded snapback NMOS for primary or 2nd ESD protection
		Junction first (s/d -> gate)	Don't care	Check	1. Both 1st/2nd stage are through IO GOX (s/d -> gate or gate -> s/d)
Cascoded (>=3-stage)	Pure Core, Pure IO or Mixed	Don't care	Don't care	Flag on ESD path with pure core GOX	--



- Conventional scheme for cascoded snapback NMOS for primary or 2nd ESD protection.

Low Capacitance Pin ESD guidelines

- This guidelines is set for Low Capacitance (LC) solution with Hi-CDM 5A (FWHM<1ns) target.
- The suggested diode for LC application is HIA diode.
- For LC ESD design scheme tighten rules, please refer to ESD.LC.2g~4.1g & ESD.LC.10g (DRC checked) and ESD.LC.5g (PERC checked).
- For LC Rx-like victim (gate oxide) and Tx-like victim (junction of driver) design guidelines, please refer to ESD calculator. Similar victim checker is implemented in ESD.9g group and ESD.CDM.2g.

Rule No.	Description	Label	Op.	Rule
ESD.LC.5g^{U}	Cascoded power clamp is not allowed as the primary protection is dual diode inside LC_DMY			
ESD.LC.5.1g^{U}	For LC diode based primary protection scheme, power clamp total width should be two times larger than ESD.40g, ESD.40.1g defined.			

PERC Methodology

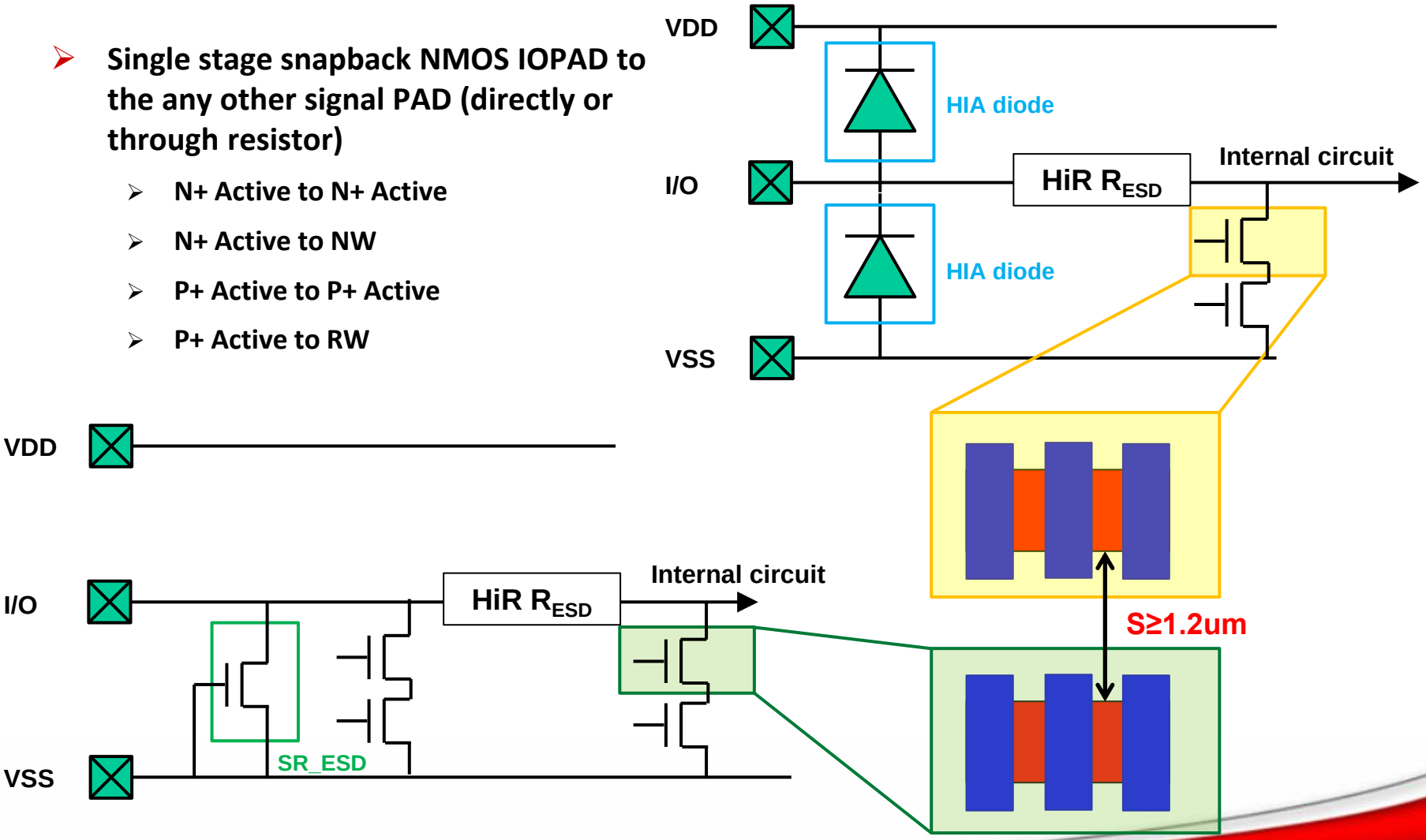
(N3 DRM Rules for Layout(LDL) Checker)

[LDL-DRC]

Primary-ESD: ESD.35gU
Power-Clamp: ESD.43.1gU
Gate Victim: ESD.9.5gU
HiCDM Victim: ESD.CDM.1gU, ESD.CDM.1.1gU, ESD.CDM.2gU
HiCDM Internal: ESD.CDM.C.2gU, ESD.CDM.C.3.1gU, ESD.CDM.C.3.2gU
Other: SR_ESD.R.7U, ESD.7gU, ESD.7.0.1gU, ESD.7.0.1.1gU, ESD.7.0.2gU, ESD.7.0.2.1gU, ESD.7.0.3gU, ESD.7.0.4gU, ESD.7.1gU, ESD.7.1.1gU, ESD.7.1.2gU, ESD.7.1.3gU, ESD.7.1.4gU
Latch-Up: LUP.WARN.3U, LUP.WARN.3.1U, LUP.1.0.1U, LUP.2.0.1U, LUP.2.1U, LUP.4.2U, LUP.14.0.1U LUP.IHIA.1.0.1U, LUP.IHIA.14.0.1U

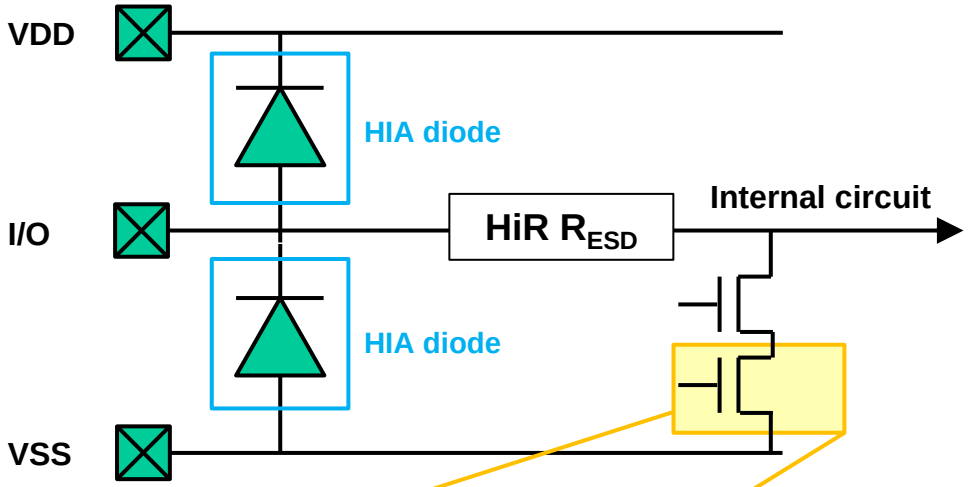
Parasitic NPN/PNP ESD spacing rules ESD.7g (ESD.7.0.1g~ESD.7.0.4g)

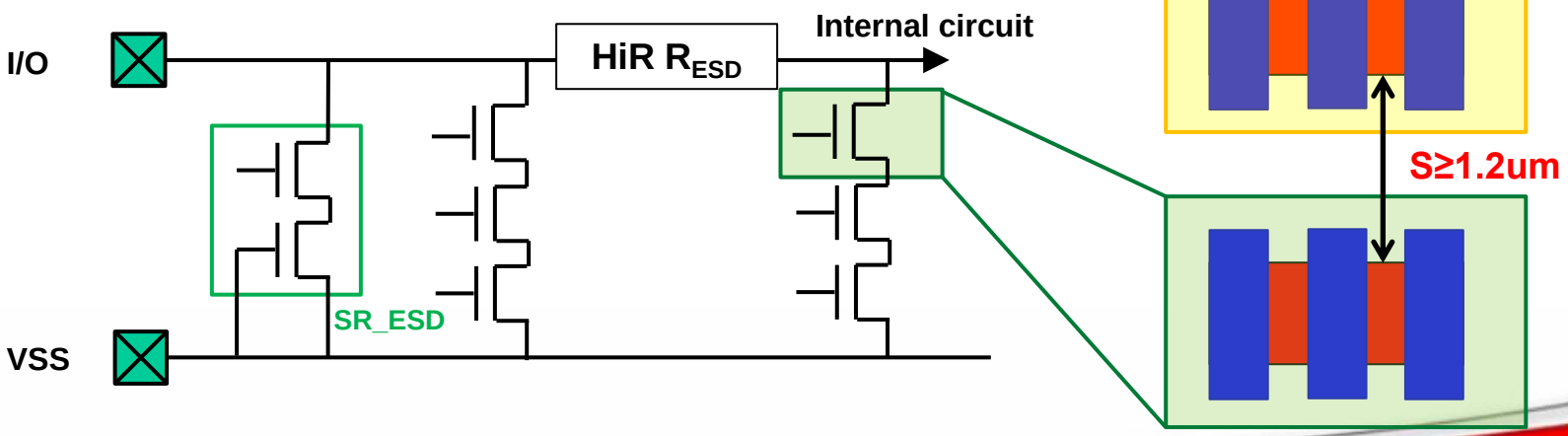
- Single stage snapback NMOS IOPAD to the any other signal PAD (directly or through resistor)
  - N+ Active to N+ Active
  - N+ Active to NW
  - P+ Active to P+ Active
  - P+ Active to RW



Parasitic NPN/PNP ESD spacing rules ESD.7.1g (ESD.7.1.1g~ESD.7.1.4g)

- Cascoded snapback NMOS IOPAD to any other power/ground/signal PAD (directly or through resistor)
  - N+ Active to N+ Active
  - N+ Active to NW
  - P+ Active to P+ Active
  - P+ Active to RW



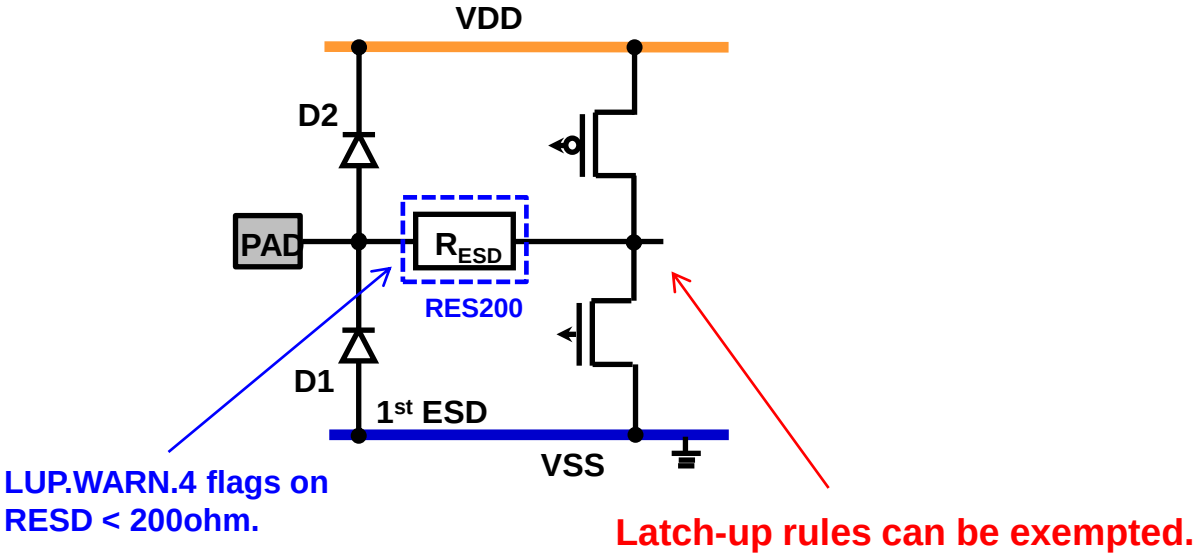


ESD Parasitic Bipolar Rules

Rule No.	Description	Label	Op.	Rule
ESD.7g^{U}	For single stage snapback NMOS protected I/O pad, specific spacing rules should be followed to avoid low triggering voltage induced issues on parasitic NPN/PNP (ESD.7.0.1g^{U}~ESD.7.0.4g^{U}) Connections would be broken by resistors [connected to power or ground pad directly].			
ESD.7.0.1g^{U}	Space between “((N+ Active NOT PO) NOT SDI_3)” and “((N+ Active NOT PO) NOT SDI_3)” if one of them connect to I/O pad stated above (directly or through resistor) and the other one connect to any different I/O pad (directly or through resistor).		≥	1.2
ESD.7.0.1.1g^{U}	Space between “((NACT NOT ALL_PO) NOT SDI)” connect to I/O pad stated above (directly or should be through resistor with resistance < 200 ohm) and “(NACT in DIODMY)” connect to different I/O pad directly.		≥	30
ESD.7.0.2g^{U}	Space between “((N+ Active NOT PO) NOT SDI_3)” and “NW” if one of them connect to I/O pad stated above (directly or through resistor) and the other one connect to any different I/O pad (directly or through resistor).		≥	1.2
ESD.7.0.2.1g^{U}	Space between “((NACT NOT ALL_PO) NOT SDI)” connect to I/O pad stated above (directly or should be through resistor with resistance < 200 ohm) to any LUP NWSTRAP tie to power.		≥	10
ESD.7.0.3g^{U}	Space between “(P+ Active NOT PO)” and “(P+ Active NOT PO)” if one of them connect to I/O pad stated above (directly or through resistor) and the other one connect to any different I/O pad (directly or through resistor).		≥	1.2
ESD.7.0.4g^{U}	Space between “(P+ Active NOT PO)” and “RW” if one of them connect to I/O pad stated above (directly or through resistor) and the other one connect to any different I/O pad (directly or through resistor).		≥	1.2
ESD.7.1g^{U}	For cascoded snapback NMOS protected I/O pad, specific spacing rules should be followed to avoid low triggering voltage induced issues on parasitic NPN/PNP (ESD.7.1.1g^{U}~ESD.7.1.4g^{U}) Connections would be broken by resistors [connected to power or ground pad directly].			
ESD.7.1.1g^{U}	Space between “((N+ Active NOT PO) NOT SDI_3)” and “((N+ Active NOT PO) NOT SDI_3)” if one of them connect to I/O pad stated above (directly or through resistor) and the other one connect to any different I/O (directly or through resistor) or power/ground pad (directly).		≥	1.2
ESD.7.1.2g^{U}	Space between “((N+ Active NOT PO) NOT SDI_3)” and “NW” if one of them connect to I/O pad stated above (directly or through resistor) and the other one connect to any different I/O (directly or through resistor) or power/ground pad (directly).		≥	1.2
ESD.7.1.3g^{U}	Space between “(P+ Active NOT PO)” and “(P+ Active NOT PO)” if one of them connect to I/O pad stated above (directly or through resistor) and the other one connect to any different I/O (directly or through resistor) or power/ground pad (directly).		≥	1.2
ESD.7.1.4g^{U}	Space between “(P+ Active NOT PO)” and “RW” if one of them connect to I/O pad stated above (directly or through resistor) and the other one connect to any different I/O (directly or through resistor) or power/ground pad (directly).		≥	1.2

Latch-up rules waive condition in PERC

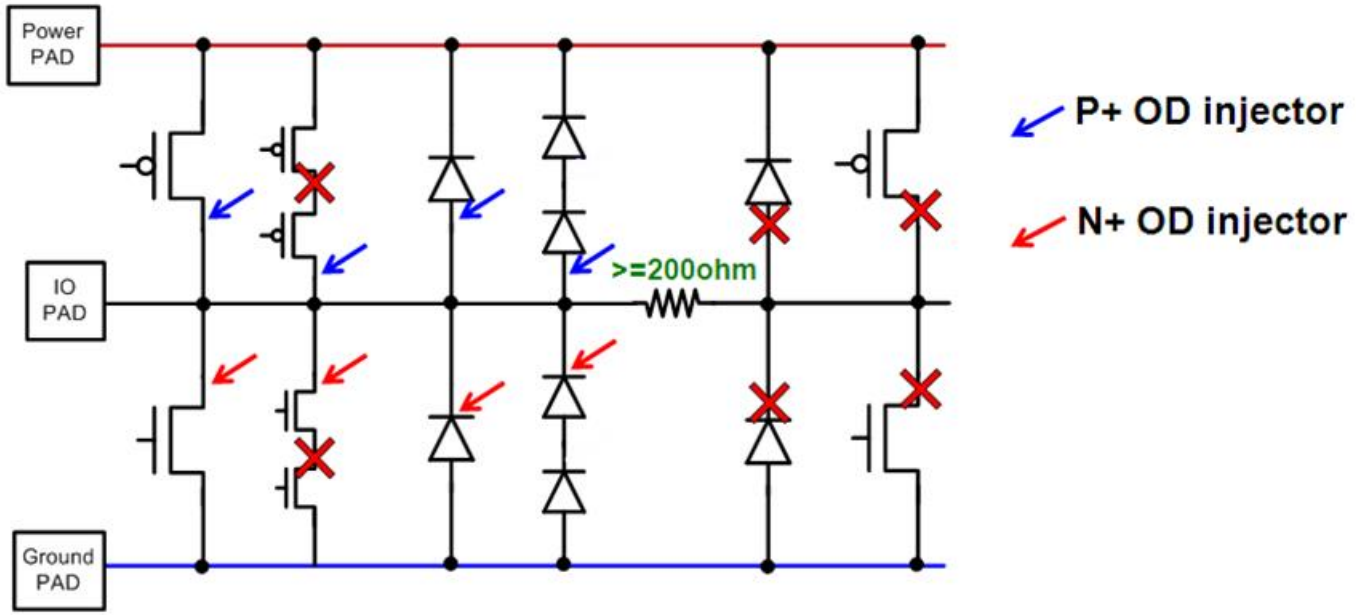
- If RESD is covered by RES200 dummy, the OD injector behind RESD would not be taken as latch-up current trigger source.
- If the resistance of RESD is < 200ohm and covered by RES200, it will be flagged by LUP.WARN.4^{U}. (Checked in PERC Topology Checker)



Rule No.	Description
LUP.WARN.4^{U}	For LUP OD injector blocking purpose, the resistor between internal device and IOPAD should be high resistance (R ≥ 200ohm) with RES200. The internal device includes all devices except gate of MOS and high-R resistor (rhim).

OD injector

Noun	Definition
OD injector	Any Active OD (Ex. MOS, STI diode, diode string (DRC unchecked), and well resistor) or NWSTRAP/RWSTRAP (Ex. Well diode and so on) directly connected to I/O PAD. N+ OD or NWSTRAP directly connected to I/O pad is N+ OD injector. P+ OD or RWSTRAP directly connected to I/O pad is P+ OD injector.



NOTE:

- **All OD injectors would be recognized as Area-IO OD injector in N3 PERC.**

Signal I/O PAD category

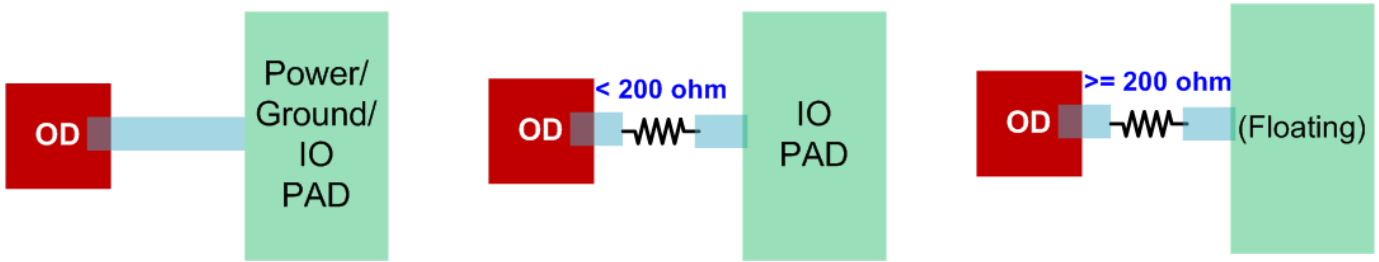
- **SIGNAL Pins: defined in SIGNAL_NAME**
  - **Subset of signal pins (all signal I/O pin must be defined in SIGNAL_NAME of n03_perc*.top)**

	Usage	Purpose
LC pin	Defined in LC_PAD_NAME or Recognized by LC_DMY on primary ESD	Low-Cap ESD guidelines check
PoP signal pins	Defined in PoP_PAD_NAME	LUP rule relax for die-to-die IOPAD through PoP interconnect
Ultra-low noise pins	Defined in ULTRA_LOW_NOISE_PAD_NAME	LUP rule relax for signal I/O pin with ultra-low overshoot/undershoot swing (i.e. ≤ +/-0.3V)

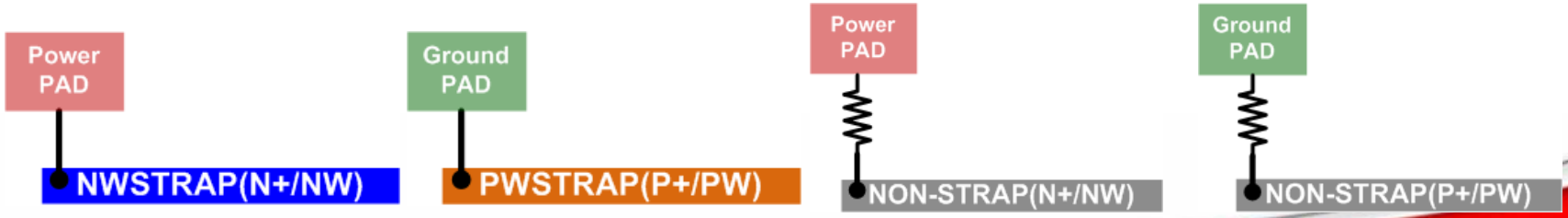
```
//VARIABLE LC_PAD_NAME "" // define low capacitance PAD names

//VARIABLE PoP_PAD_NAME "" // define die-to-die IO PAD names through PoP interconnect

//VARIABLE ULTRA_LOW_NOISE_PAD_NAME "" // define ultra-low noise IO PAD names

VARIABLE VIRTUAL_POWER_NAME "NW1" "NW2" "NW3" // define virtual power names for LDL checks (e.g. "VVDD1" "VVDD2@CELL2")
                              // the used cell names should be defined in hcell to preserve hierarchy

//VARIABLE D2D_INTERFACE_NAME ""    // define LHDI die-to-die interface names

VARIABLE SIGNAL_NAME "?" // define signal names, "?" matches all top port names (except power/ground names)

VARIABLE POWER_NAME "VDD?" "?vdd?" "?PWR?" "?pwr?" "NW_L" // define power names

VARIABLE GROUND_NAME "?VSS?" "?vss?" "?GND?" "?gnd?" "ESD_GLOBAL" // define ground names
```

Guard-Ring/Strap and LUP PAD Definition

- **LUP PAD Definition**
  - Power / Ground PAD : PAD directly not through resistor tie to OD.
  - IO PAD : PAD directly or through resistor < 200ohm (not covered by RES200) tie to OD



- **Guard-Ring / STRAP Definition**
  - NWSTRAP: N+/NW directly tie to power pad
  - PWSTRAP: P+/PW directly tie to ground pad



Virtual Power for LUP Guard-Ring/STRAP

- In latch-up suppression point of view, Guard-Rings and STRAPs are required and should be biased to power/ground net.
- For designs with Guard-Rings/STRAPs biased to **virtual powers**, a special pin group in **"*.top file"** is enabled to have complete LUP Guard-Ring/STRAP connection check.

```
//VARIABLE GLOBAL_ESD_BUS ""          // define global ESD bus

//VARIABLE LC_PAD_NAME ""             // define low capacitance PAD names

//VARIABLE ULTRA_LOW_NOISE_PAD_NAME ""  // define ultra-low noise IO PAD names

//VARIABLE VIRTUAL_POWER_NAME ""      // define virtual power names for LDL checks (e.g. "VVDD1" "VVDD2@CELL2")
                                      // the used cell names should be defined in hcell to preserve hierarchy

VARIABLE SIGNAL_NAME "?"    // define signal names, "?" matches all top port names (except power/ground names)

VARIABLE POWER_NAME  "?VDD?" "?vdd?" "?PWR?" "?pwr?"    // define power names

VARIABLE GROUND_NAME "?VSS?" "?vss?" "?GND?" "?gnd?"    // define ground names
```

- Virtual power pin group would not be taken to ESD related rule check.
- Device connected to virtual power is exempted from LUP rule checks.

Virtual Power for LUP Guard-Ring/STRAP

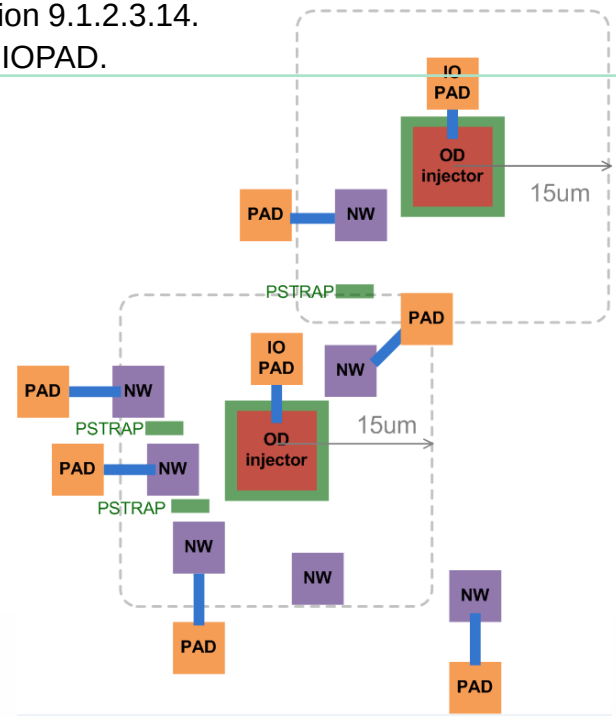
- There are two methods to define virtual power
  1) **VARIABLE VIRTUAL_POWER_NAME "VVDD1"**
     - Defined by pin text at top hierarchy of **top level** layout database
     - Only LVS recognized port is allowed
  2) **VARIABLE VIRTUAL_POWER_NAME "VVDD2@CELL2"**
     - Defined by pin text at top hierarchy of **subcells**
     - The used cell names should be defined in hcell to preserve hierarchy
     - Only LVS recognized port is allowed

  - For both top level and sub-block level, if there is no LVS recognized port in the design database, user can use following lines to define the port name and location of top cell or sub-blocks w.r.t specific metal lines.

```
LAYOUT TEXT "P1" 2.915 26.4325 M0_text CELL1
LAYOUT TEXT "P2" 2.915 26.4325 M0_text CELL2
```

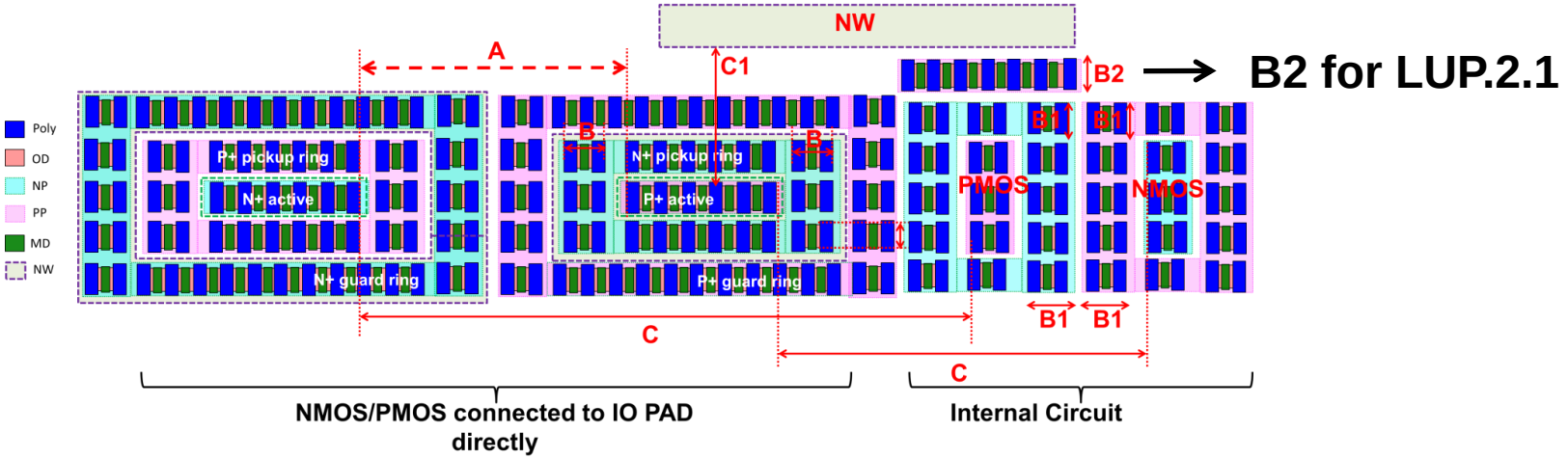
LUP.2.1

Rule No.	Description
LUP.2.1[U]	Within 15 μm (≤ 15 μm) space from the OD injector, an P+ACTIVE in proximity to another NW and with the relative higher potential to another NW, a PWSTRAP is required to be inserted between P+ ACTIVE to another NW. (Figure 9.1.13) Exception: a. ACTIVE OD does not connect to VD, VDR, or VG. b. If all of the OD injectors connected to specific signal pin are with ultra-low noise, LUP.2.1 can be excluded. For the detail of ultra-low noise OD injector recognition methodology, please refer to Section 9.1.2.3.14. c. OD injectors connected to PoP IOPAD.



LUP.4.2

- **PERC find LUP.2.1 related device and their corresponding strap, and check the width.**

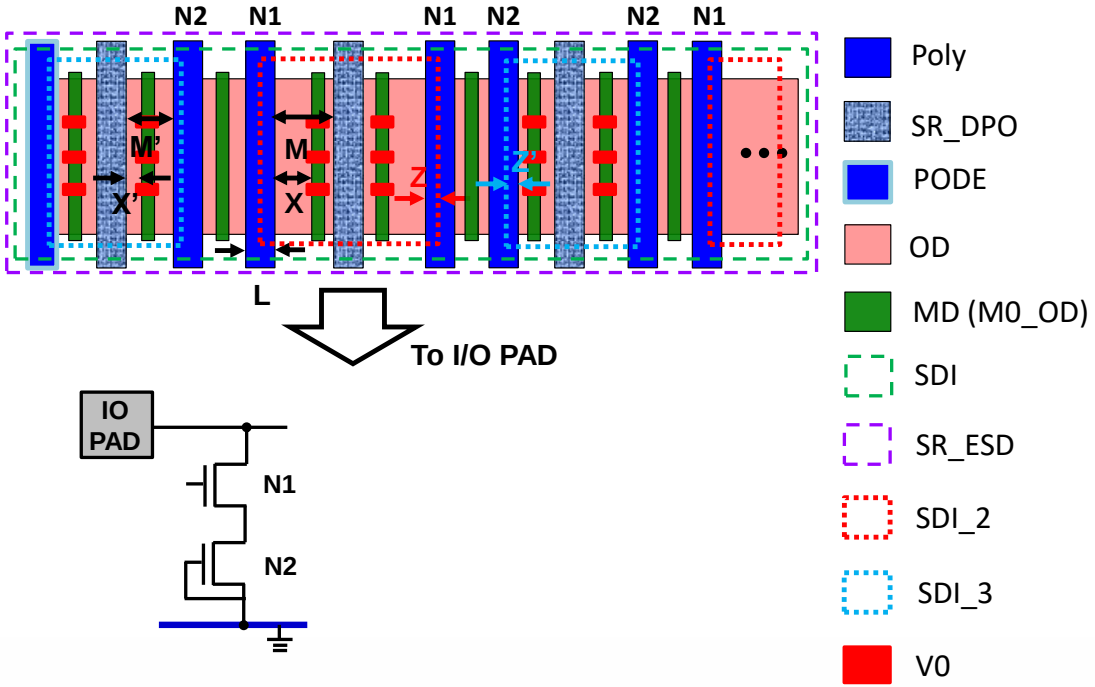


Rule No.	Description	Op.	Value
LUP.4.2^{U}	OD width of the PWSTRAP for LUP.2.1U. (Figure 9.1.11) Exception: a. ACTIVE OD does not connect to VD, VDR, or VG. b. If all of the OD injectors connected to specific signal pin are with ultra-low noise, LUP.4.2 can be excluded. For the detail of ultra-low noise OD injector recognition methodology, please refer to Section 9.1.2.3.14. c. OD injectors connected to PoP IOPAD.	≧	0.09

ESD.35g

Rule No.	Description	Op.	Value
ESD.35g^{U}	2-stage cascoded NMOS need to be same OD structure		

2-stage cascaded drain-ballasted NMOS



CD/P2P Discharging Path Existence Pre-check

- In general, complete CD/P2P check is really time-consuming. To have a preliminary quality check in early stage, two options in **"*.top file"** is enabled.
- By turning on "DEFINE CD_PRE_CHECK" and "DEFINE P2P_PRE_CHECK" options, user can check the existence of discharge path before performing complete CD/P2P check.
- Note: There is one difference between discharging path pre-check & those checks in CD/P2P flow. In complete CD/P2P checking flow, it takes "physically connected" discharging path. In the pre-check flow, it takes both "physically connected" and "virtual connected" ones into consideration. For ESD network design, it is suggested to use physically connected discharging path.

```
#DEFINE TOPO     // Turn on to enable Topology checks
#DEFINE LDL      // Turn on to enable LDL(Logic-Driven-Layout) DRC checks
//#DEFINE CD     // Turn on to enable CD(Current Density) checks
//#DEFINE P2P    // Turn on to enable P2P(Point-to-Point) checks

// ** Note: CD & P2P cannot be enabled at the same time **

#DEFINE CD_PRE_CHECK          // Turn on to check the existence of CD path only

#DEFINE P2P_PRE_CHECK         // Turn on to check the existence of P2P path only
```

PERC Methodology

(N3 DRM Rules for Current Density Checker)

[CD]
Primary-ESD: ESD.CD.1gU , ESD.CD.1.1gU
Secondary-ESD: ESD.CD.2gU
SCR-Path: ESD.CD.3.1gU , ESD.CD.3.2gU, ESD.CD.3.3gU, ESD.CD.3.4gU

Current Density Methodology

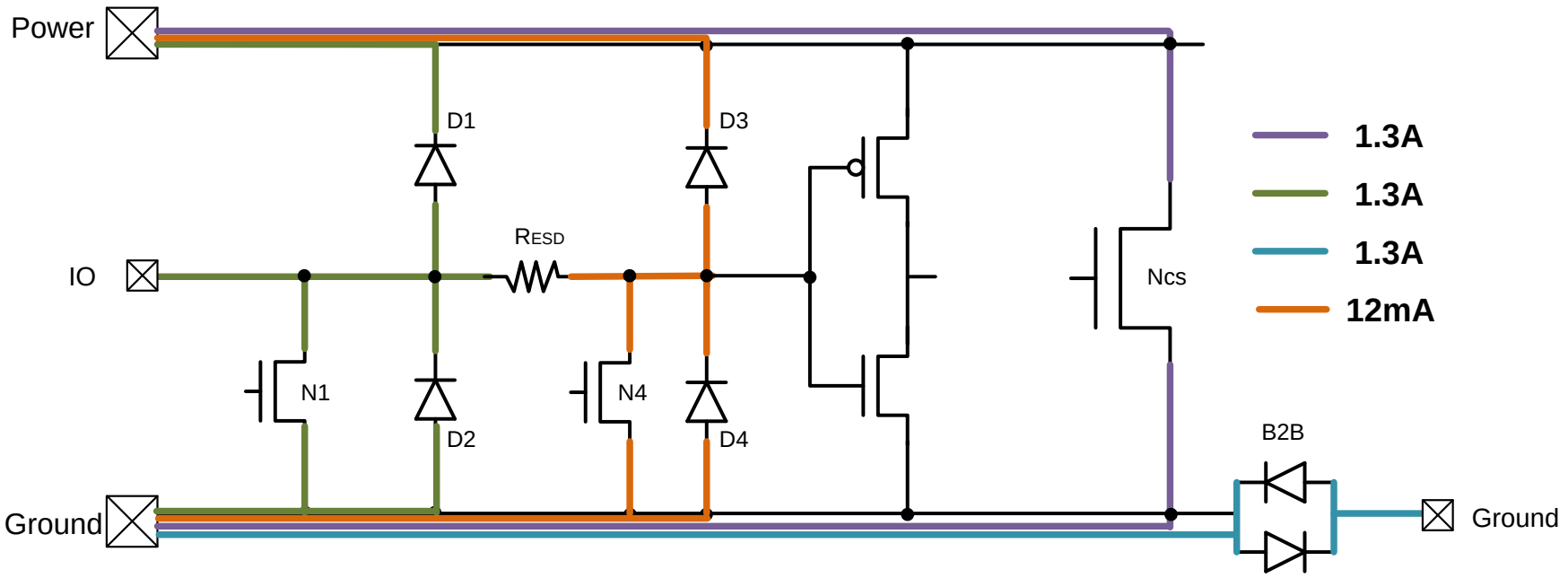
- **Primary Path**
  - **Total current injecting from source side is 1.3A**
  - **Checking backend layer connected between IO pad and primary ESD device**
  - **Checking path stopped before ESD resistor**
- **Secondary Path**
  - **Total current injecting from source side is 12mA**
  - **Checking current density from ESD resistor (R_{ESD}) to secondary ESD device**
  - **Includes ESD resistor and back-end layer**

Rule No.	Description	Label	Op.	Rule
ESD.CD.1g^{u}	Suggested minimum ESD current (unit: A, IESD) for the primary ESD discharge path. Primary ESD devices include dual-diode, drain-ballasted NMOS, drain-ballasted cascoded NMOS, power clamp and back to back (b2b) diode Primary ESD discharge current path includes: 1. Metal line width connecting the “bond pad” and the primary ESD device. 2. The Via number in the primary ESD device.	I	≧	1.3
ESD.CD.2g^{u}	Suggested minimum ESD current (Unit: A, IESD) for the secondary ESD discharge path. Secondary ESD devices include ESD resistor, diode based and MOS based secondary protection. Secondary ESD discharge current path includes: 1, Metal line width connecting the “bond pad” and the secondary ESD device. 2. The Via number in the secondary ESD device	I	≧	0.012

Current Density Methodology

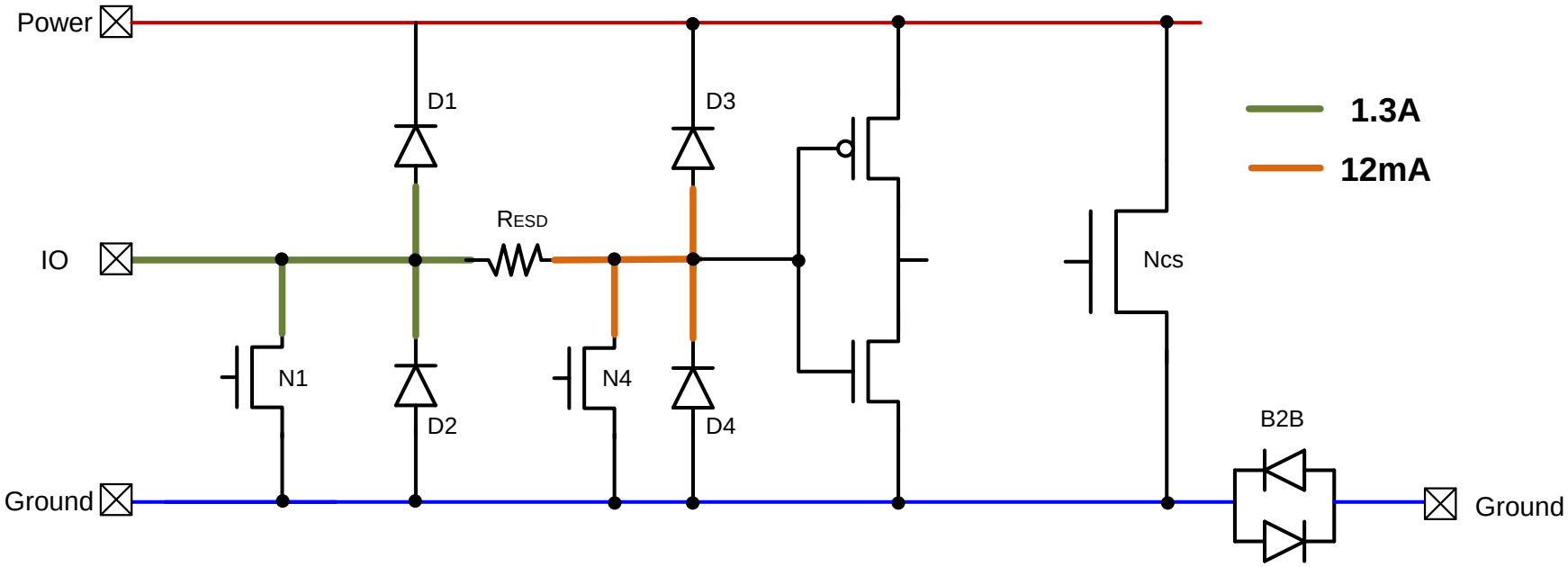
- User can choose Full Path CD checks (Default) or Basic Path CD checks
  - Full Path CD checks (Default):
    1. I/O Pad to Power/Ground Pad through primary ESD device
    2. R_{ESD} to Power/Ground Pad through secondary ESD device
    3. Power Pad to Ground Pad through Power clamp
    4. Two Ground Pads through B2B diode connection
  - Basic Path CD checks: (by disable CHECK_FULL_PATH_CD)
    1. I/O Pad to primary ESD device
    2. R_{ESD} to secondary ESD device
- Non TSMC defined ESD network scheme is not checked by PERC CD, and there will be error reported in Topology check
- Full Path CD checks can be used for Cell/IP or small size chip. However for big size chip it might encounter severe runtime issue.

CD Methodology: Full Path (Default)



1. Check backend layer connected between PADs through ESD protection device.
2. Non TSMC defined ESD network scheme is not checked by PERC CD
3. Full Path CD check can be used for Cell/IP or small size chip. However for big size chip it might encounter severe runtime issue. Basic Path CD checks are recommended only when Full Path CD cannot be done for whole chip with big size to avoid severe runtime issue.

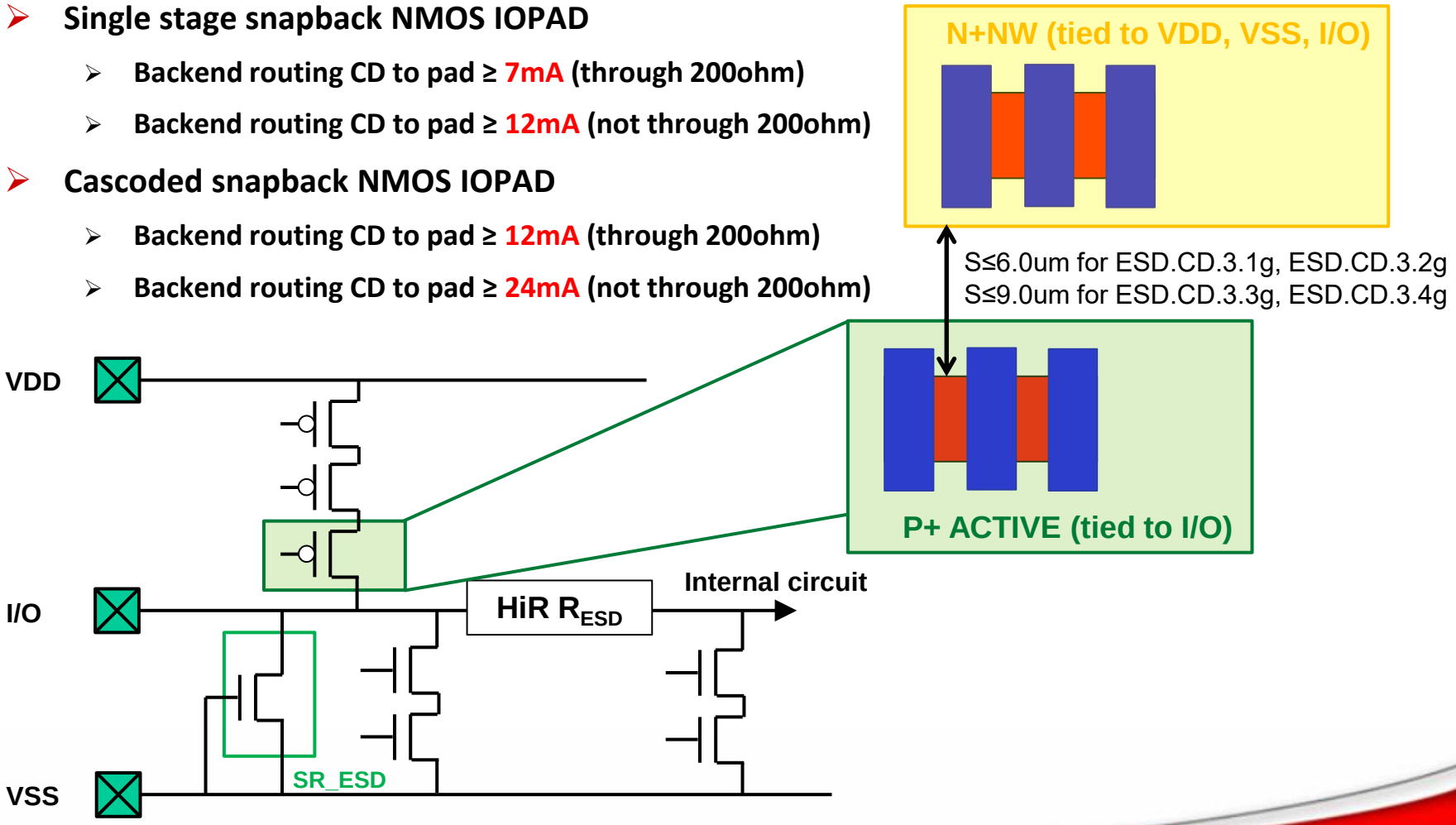
CD Methodology: Basic Path (CHIP Level)



1. Check backend layer connected between IO pad and Primary/Secondary ESD device
2. Non TSMC defined ESD network scheme is not checked by PERC CD
3. Basic Path CD checks are recommended only when Full Path CD cannot be done for whole chip with big size to avoid severe runtime issue.

Parasitic SCR (P+ Active to NW) ESD CD rules ESD.CD.3.1g~ESD.CD.3.4g

- Single stage snapback NMOS IOPAD
  - Backend routing CD to pad ≥ 7mA (through 200ohm)
  - Backend routing CD to pad ≥ 12mA (not through 200ohm)
- Cascoded snapback NMOS IOPAD
  - Backend routing CD to pad ≥ 12mA (through 200ohm)
  - Backend routing CD to pad ≥ 24mA (not through 200ohm)



ESD Parasitic Bipolar Rules

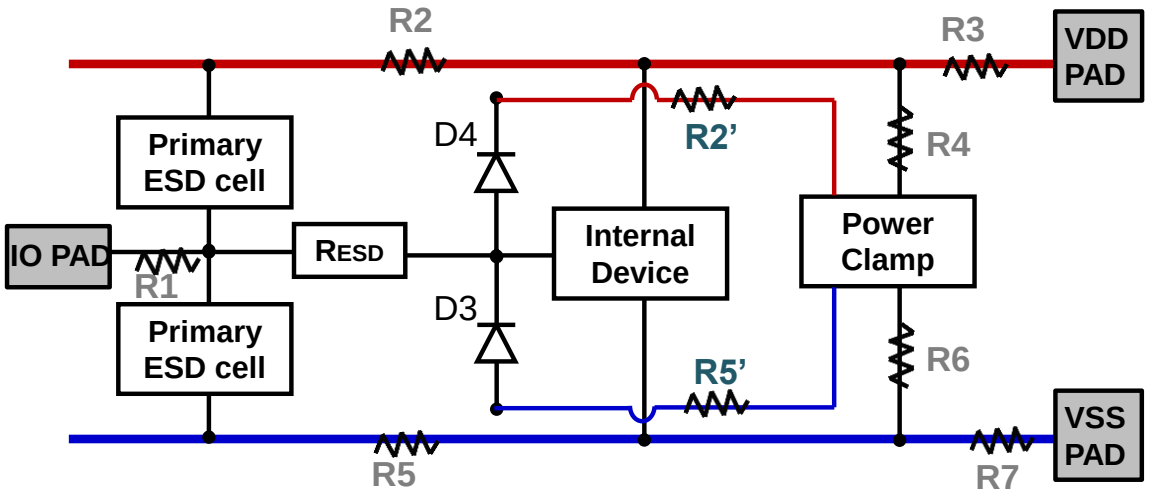
Rule No.	Description	Label	Op.	Rule
ESD.CD.3.1g^{U}	For single stage snapback NMOS protected IOPAD, minimum ESD current (Unit: A, IESD) for parasitic SCR discharging path through 200ohm ESD resistor. Parasitic SCR path forms by followings, 1. ESD_SCR_ANODE = PACT [connected to IOPAD (state above) through 200ohm resistor] 2. ESD_SCR_CATHODE = {NW AND OD} [space to ESD_SCR_ANODE (state above) ≤ 6μm] [connected to any different I/O (directly or through any resistor) or power/ground pad (directly)]		≥	0.0070
ESD.CD.3.2g^{U}	For single stage snapback NMOS protected IOPAD, minimum ESD current (Unit: A, IESD) for parasitic SCR discharging path not through 200ohm ESD resistor. Parasitic SCR path forms by followings, 1. ESD_SCR_ANODE = PACT [connected to IOPAD (state above) directly or through < 200ohm resistor] 2. ESD_SCR_CATHODE = {NW AND OD} [space to ESD_SCR_ANODE (state above) ≤ 6μm] [connected to any different I/O (directly or through any resistor) or power/ground pad (directly)]		≥	0.0120
ESD.CD.3.3g^{U}	For cascoded snapback NMOS protected IOPAD, minimum ESD current (Unit: A, IESD) for parasitic SCR discharging path through 200ohm ESD resistor. Parasitic SCR path forms by followings, 1. ESD_SCR_ANODE = PACT [connected to IOPAD (state above) through 200ohm resistor] 2. ESD_SCR_CATHODE = {NW AND OD} [space to ESD_SCR_ANODE (state above) ≤ 9μm] [connected to any different I/O (directly or through any resistor) or power/ground pad (directly)]		≥	0.0120
ESD.CD.3.4g^{U}	For cascoded snapback NMOS protected IOPAD, minimum ESD current (Unit: A, IESD) for parasitic SCR discharging path not through 200ohm ESD resistor. Parasitic SCR path forms by followings, 1. ESD_SCR_ANODE = PACT [connected to IOPAD (state above) directly or through < 200ohm resistor] 2. ESD_SCR_CATHODE = {NW AND OD} [space to ESD_SCR_ANODE (state above) ≤ 9μm] [connected to any different I/O (directly or through any resistor) or power/ground pad (directly)]		≥	0.0240

PERC Methodology

(N3 DRM/LC Rules for P2P Checker)

[P2P]
Primary-ESD: ESD.14.3gU
Power-Clamp: ESD.14.4gU
Secondary-ESD: ESD.14.5gU
Pick-up to PAD: ESD.14.6gU, ESD.14.7gU, ESD.14.8gU
LC Primary-ESD: ESD.LCP2P.1gU, ESD.LCP2P.2gU
HiCDM Primary-ESD: ESD.CDM.P.1gU, ESD.CDM.P.1.0gU, ESD.CDM.P.1.1gU, ESD.CDM.P.1.2gU, ESD.CDM.P.2gU , ESD.CDM.P.2.1gU
HiCDM Power-Clamp: ESD.CDM.P.3gU, ESD.CDM.P.4gU, ESD.CDM.P.5gU , ESD.CDM.P.5.1gU, ESD.CDM.P.7gU, ESD.CDM.P.7.1.1gU, ESD.CDM.P.7.1.2gU, ESD.CDM.P.7.2gU, ESD.CDM.P.7.3gU, ESD.CDM.P.7.4gU, ESD.CDM.P.7.5gU, ESD.DISTP2P.1gU, ESD.DISTP2P.1.0gU, ESD.DISTP2P.1.1gU, ESD.DISTP2P.1.1.0gU, ESD.DISTP2P.1.2gU, ESD.DISTP2P.1.2.0gU, ESD.DISTP2P.1.3gU, ESD.DISTP2P.1.3.0gU
HiCDM B2B Diode: ESD.CDM.P.8gU, ESD.CDM.P.9gU
HiCDM Victim: ESD.CDM.P.10gU

DRM P2P Checking (14.3g~14.5g)



Rule No.	Description	Op.	Rule
ESD.14.3gU	1. Resistance of the Power bus line from IO pad to the closest Power clamp. (R1+R2+R4 in Figure 9.2.19.2) (Ω) 2. Resistance of the ground bus line from IO pad to the closest Power clamp. (R1+R5+R6 in Figure 9.2.19.2) (Ω) If the IO PAD connects to ESD cell first, the R1 can be ignored.	≤	1
ESD.14.4gU	Resistance of the bus line from Power pad to the closest GND pad.(R3+R4+R6+R7 in Figure 9.2.19.1~3) (Ω) If the Power/Ground PAD connects to power clamp first, this rule can be waived.	≤	1
ESD.14.5gU	Resistance of the bus line from 2nd ESD Diode to the closest Power Clamp. 1. Resistance of the power bus line from 2nd ESD diode to the closest Power clamp. (R2' in Figure 9.2.19.4) (Ω) 2. Resistance of the ground bus line from 2nd ESD diode to the closest Power clamp. (R5' in Figure 9.2.19.4) (Ω)	≤	10

For ESD.14.3g, as snapback NMOS as primary protection, power clamp p2p check take IO power clamp only.

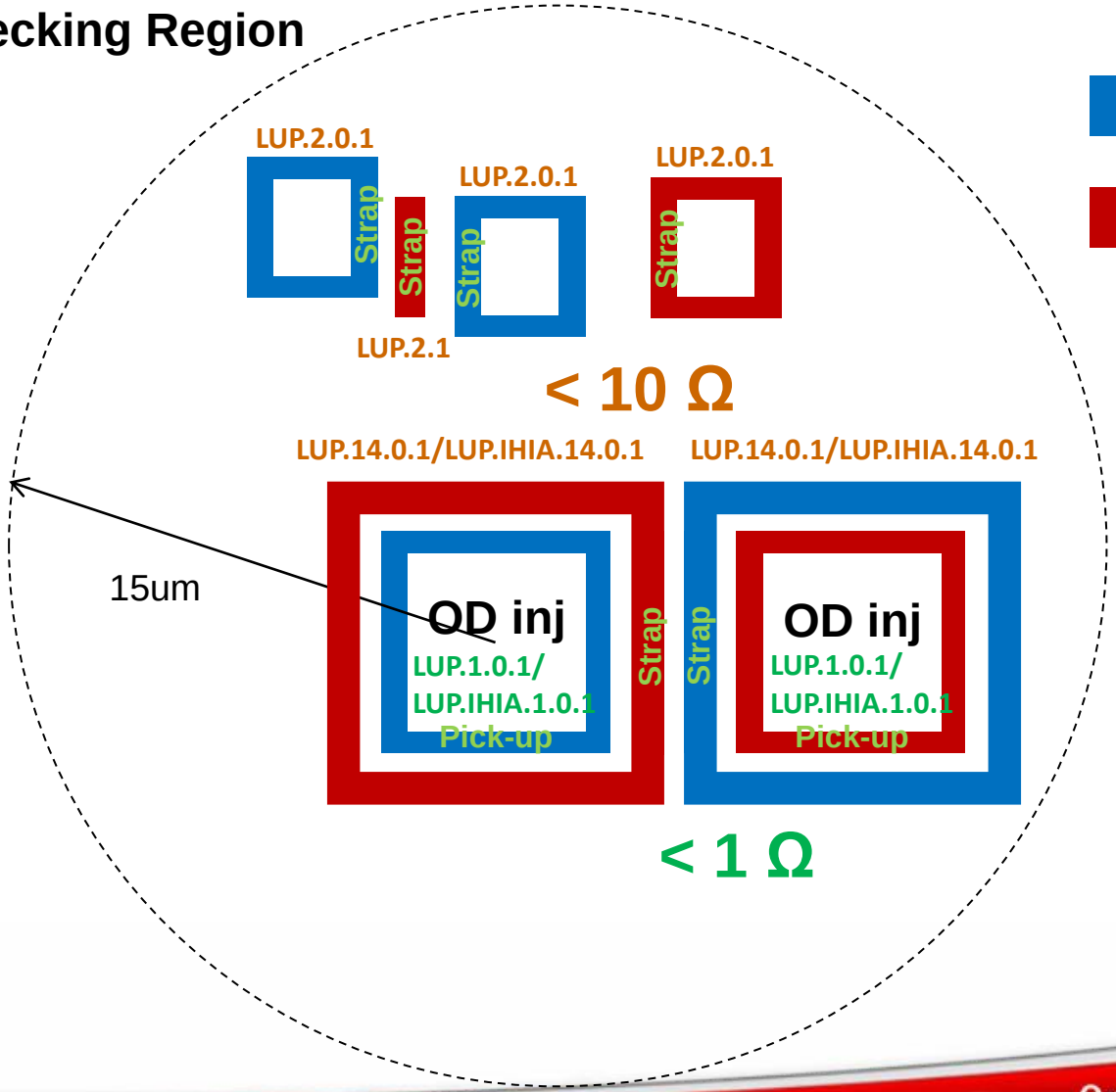
DRM P2P Checking (14.6g~14.8g)

- ESD.14.6g~ESD.14.8g check the resistance of Bond pad to guard-rings/straps of LUP.1.0.1^{U}, LUP.IHIA.1.0.1^{U}, LUP.2.0.1^{U}, LUP.2.1^{U}, LUP.14.0.1^{U}, and LUP.IHIA.14.0.1^{U}.
- ESD.14.6g~ESD.14.8g do NOT check the connection of guard-rings/straps. Floating guard-rings/straps will not be checked and there will be no warning message reported.
- PERC LDL Latch-Up rules: LUP.1.0.1^{U}, LUP.IHIA.1.0.1^{U}, LUP.2.0.1^{U}, LUP.2.1^{U}, LUP.14.0.1^{U}, and LUP.IHIA.14.0.1^{U} will check NW STRAP tied to power and PW STRAP tied to ground. Please make sure Latch-Up rules passed in LDL check to get these rules checked properly.
- To check these rules, user need to:
  1. Run LDL check first to get Marker GDS: TSMC.ESD.MARK.gds
  2. Enable CHECK_PICK_UP_P2P switch in top file

Rule No.	Description	Op.	Rule
ESD.14.6g^{U}	Resistance of bus line from the pick-up ring of LUP.1.0.1^{U} and LUP.IHIA.1.0.1^{U} to the closest Power / Ground Pad (Ω)	≤	1
ESD.14.7g^{U}	Resistance of bus line from the pick-up ring/ guard-ring/ strap of LUP.2.0.1^{U} and LUP.2.1^{U} to the closest Power / Ground Pad (Ω)	≤	10
ESD.14.8g^{U}	Resistance of bus line from the guard-ring of LUP.14.0.1^{U} and LUP.IHIA.14.0.1^{U} to the closest Power / Ground Pad (Ω)	≤	10

DRM P2P Checking (14.6g~14.8g)

- **Checking Region**



NW

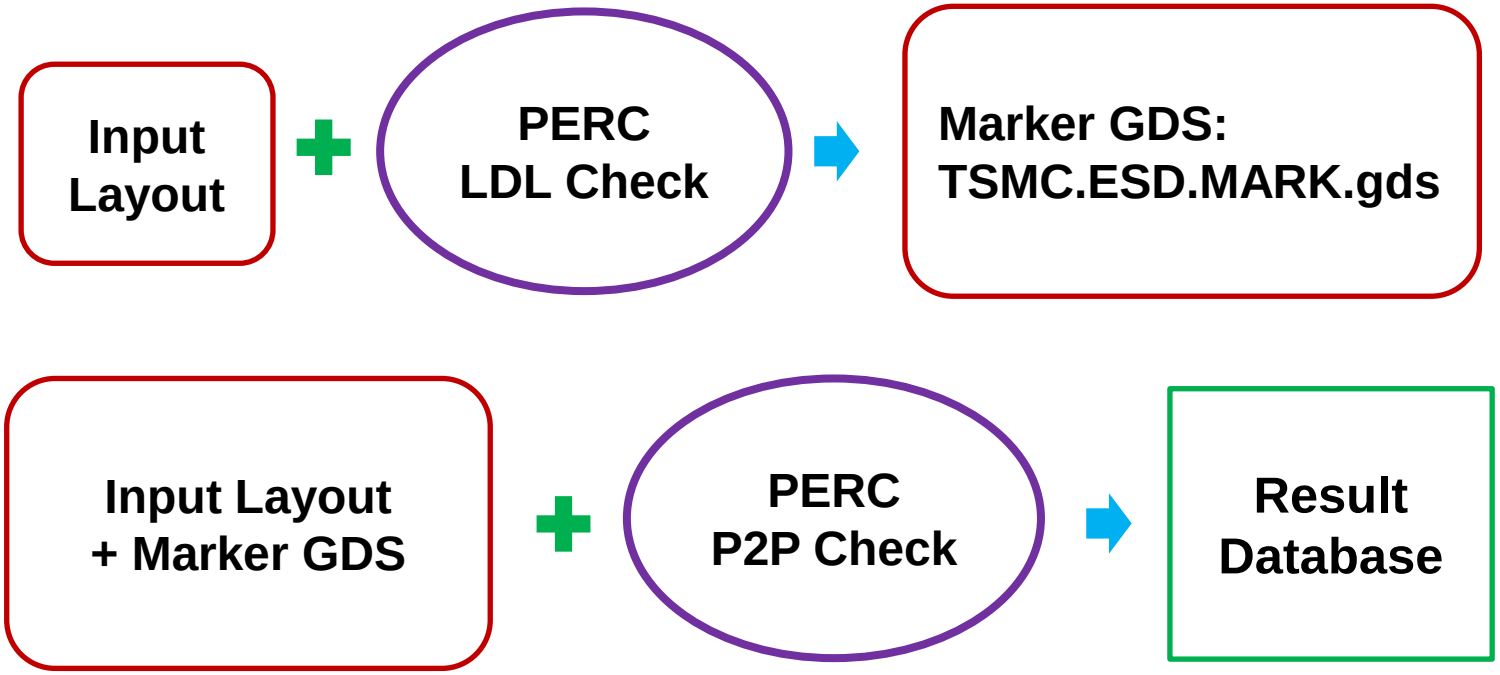
PW

Pick-up ring/Strap of

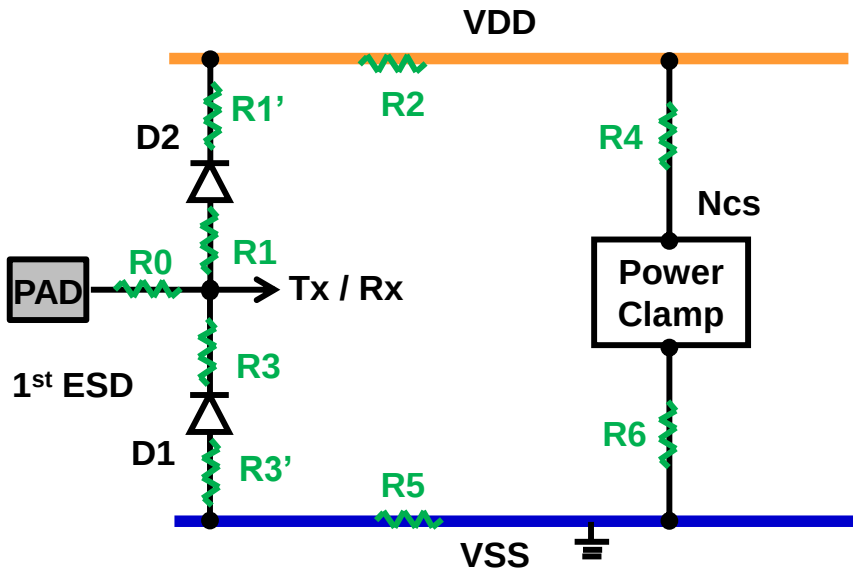
- LUP.1.0.1
- LUP.IHIA.1.0.1
- LUP.2.0.1
- LUP.2.1
- LUP.14.0.1
- LUP.IHIA.14.0.1

DRM P2P Checking (14.6g~14.8g)

- Checking Flow



LC P2P Checking



Rule No.	Description	Op.	Rule
ESD.LCP2P.1g^{U}	Metal Bus resistance of IOPAD to ESD dual diode inside LC_DMY R1 & R3 ≤ 0.1 ohm. (Fig.9.2.32.2) No needed to take "R0" into account.	≤	0.1
ESD.LCP2P.2g^{U}	Metal Bus resistance of ESD dual diode inside LC_DMY to power clamp R1'+R2+R4 ≤ 0.1 ohm, R3'+R5+R6 ≤ 0.1 ohm. (Fig.9.2.32.2)	≤	0.1

PERC Methodology

(N3 DRM Rules for CDM Checker)

-For CDM peak current 5A (FWHM<1ns)

Snapback Base (1/12)

Rule No.	Category	N3 CDM peak current 5A purpose
ESD.CDM.1g^{U}	Snapback Base Primary Protection Scheme (For 1.2V)	For single stage snapback NMOS based primary protection, Output driving NMOS should be ≥ 2 stack I/O device (Lg ≥ 86nm) with separated OD structure; Output driving PMOS should be ≥ 3 stack I/O device (Lg ≥ 86nm) with separated OD structure and two separated NW. (Figure 9.2.35~9.2.37.1) Core device or core-I/O device in cascoded scheme is not allowed. For I/O NMOS cascoded with I/O PMOS scheme, it is not allowed. Exception: 1. Single stage I/O NMOS, whose source side does not connect to VDD/VSS. 2. Single stage I/O PMOS, whose source side does not connect to VDD/VSS, with NW does not tie to VDD. 3. 2-stage cascoded I/O N/PMOS (including N/PMOS mixed scenario), whose source side of 2nd-stage MOS does not connect to VDD/VSS, with NW of PMOS does not tie VDD. 4. Devices without ESD path (S/D shorted) is exempted from this rule check. 5. Single stage snapback NMOS as secondary ESD protection with Rout (RESD) in series. Total channel width multiplies with Rout (RESD) value should be ≥ 3200um*ohm. Definition of separated OD: 1. 1st stage NMOS are surrounded by P+ guard ring. All device inside the guard ring are the 1st stage ones only. 2. 2nd stage NMOS are surrounded by P+ guard ring. 3. The guard rings are tied to ground accordingly. 4. For > 3 stack design scheme, the checker only check first three stage only. Definition of two separated NW: 1. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to VDD. 2. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to its active OD. 3. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to active OD of the other PMOS. 4. The NW of first-stage and third stage PMOS (P1a/P1c) of 3 stack PMOS cannot tie to each other. 5. 1st stage PMOS are surrounded by N+ guard ring. All device inside the guard ring are the 1st stage ones only. 6. 2nd stage PMOS are surrounded by N+ guard ring. All device inside the guard ring are the 2nd stage ones only. 7. 3rd stage PMOS are surrounded by N+ guard ring. 8. For > 3 stack design scheme, the checker only check first three stage PMOS only. This rule is based on limited test structure. For single stage MOS, it is based on gate-grounded design. For cascoded scheme, the test structure is with top-gate floating and bottom-gate grounded. ESD immunity highly depends on circuit design and real layout implantation, please ensure the MOS channel are turned off during ESD event and design is Si-proven before mass production.

Snapback Base (2/12)

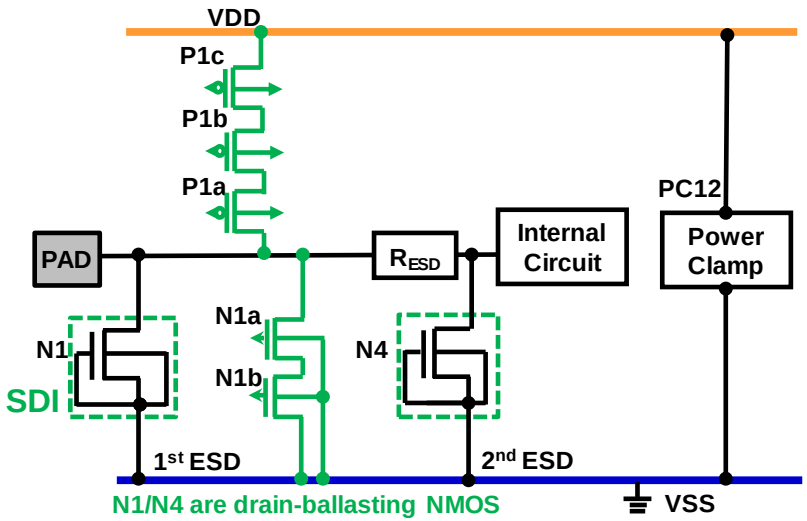


Fig.1.1
Snapback base primary protection scheme

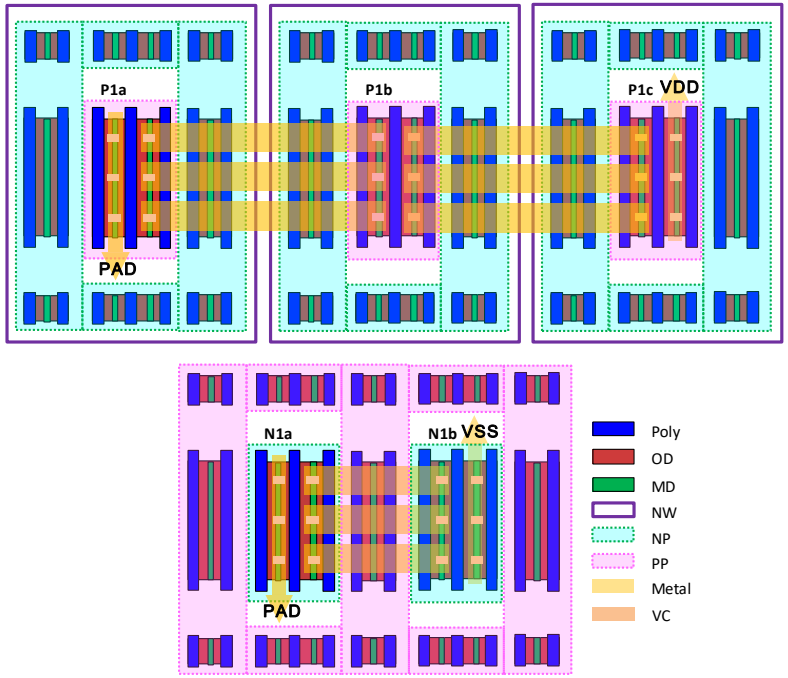


Fig.1.2
Layout view of 2-stack separated OD NMOS and 3-stack separated NW PMOS

Snapback Base (3/12)

1. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to VDD.
2. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to its active OD.
3. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to active OD of the other PMOS.
4. The NW of first-stage and third stage PMOS (P1a/P1c) of 3 stack PMOS cannot tie to each other.
5. 1st stage PMOS are surrounded by N+ guard ring. All device inside the guard ring are the 1st stage ones only.
6. 2nd stage PMOS are surrounded by N+ guard ring. All device inside the guard ring are the 2nd stage ones only.
7. 3rd stage PMOS are surrounded by N+ guard ring.
8. For > 3 stack design scheme, the checker only check first three stage PMOS only.

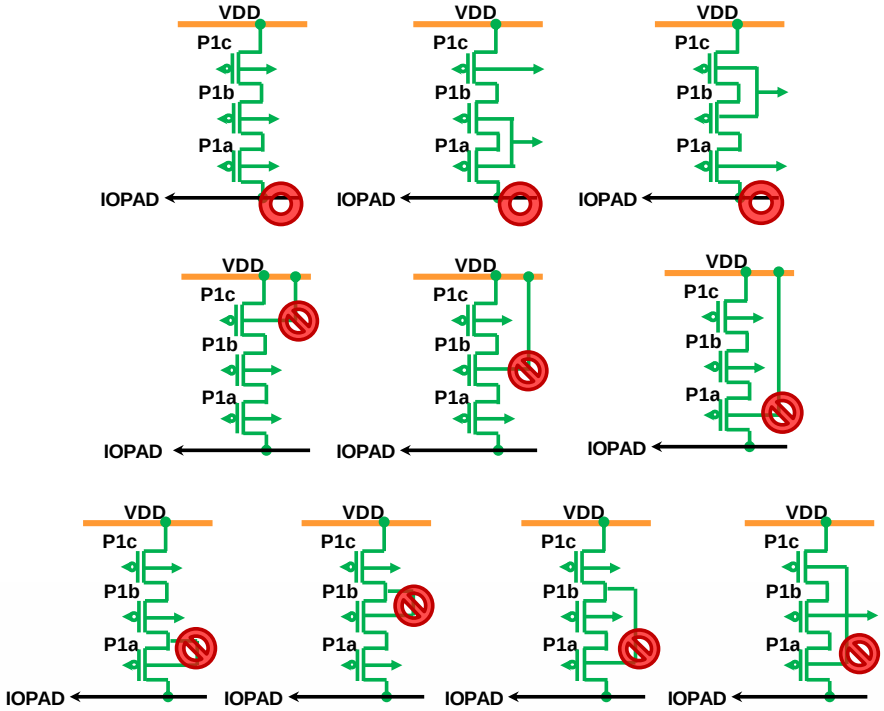


Fig.1.3 Schematic view of 3-stack PMOS with 2 separated NWs

Above devices are non-ESD current path, so the metal CD (EM) is not needed to meet ESD metal current density rule.

Snapback Base (4/12)

Rule No.	Category	N3 CDM peak current 5A purpose
ESD.CDM.1.1g^{U}	Cascoded Snapback Base Primary Protection Scheme (For 1.8V)	For 2-stage cascoded snapback NMOS based primary protection, Output driving N/PMOS should be ≥ 3 stack I/O device (Lg ≥ 86nm) with separated OD structure on NMOS and three separated NWs on PMOS. (Figure 9.2.37.2, 9.2.38 and 9.2.39) Core device or core-I/O device in cascoded scheme is not allowed. For I/O NMOS cascoded with I/O PMOS scheme, it is not allowed. Exception: 1. Single stage I/O NMOS, whose source side does not connect to VDD/VSS. 2. Single stage I/O PMOS, whose source side does not connect to VDD/VSS, with NW does not tie to VDD. 3. 2-stage cascoded I/O N/PMOS (including N/PMOS mixed scenario), whose source side of 2nd-stage MOS does not connect to VDD/VSS, with NW of PMOS does not tie VDD. 4. Devices without ESD path (S/D shorted) is exempted from this rule check. 5. 2-stage cascoded snapback NMOS as secondary ESD protection (common OD) with Rout (RESD) in series. Total channel width multiplies with Rout (RESD) value should be ≥ 3200um*ohm. Definition of separated OD: 1. 1st stage NMOS are surrounded by P+ guard ring. All device inside the guard ring are the 1st stage ones only. 2. 2nd stage NMOS are surrounded by P+ guard ring. All device inside the guard ring are the 2nd stage ones only. 3. 3rd stage NMOS are surrounded by P+ guard ring. 4. The guard rings are tied to ground accordingly. 5. For > 3 stack design scheme, the checker only check first three stage only. Definition of three separated NWs: 1. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to VDD. 2. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to its active OD. 3. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to active OD of the other PMOS. 4. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to each other. 5. 1st stage PMOS are surrounded by N+ guard ring. All device inside the guard ring are the 1st stage ones only. 6. 2nd stage PMOS are surrounded by N+ guard ring. All device inside the guard ring are the 2nd stage ones only. 7. 3rd stage PMOS are surrounded by N+ guard ring. 8. For > 3 stack design scheme, the checker only check first three stage PMOS only. This rule is based on limited test structure. For single stage MOS, it is based on gate-grounded design. For cascoded scheme, the test structure is with top-gate floating and bottom-gate grounded. ESD immunity highly depends on circuit design and real layout implantation, please ensure the MOS channel are turned off during ESD event and design is Si-proven before mass production.

Snapback Base (5/12)

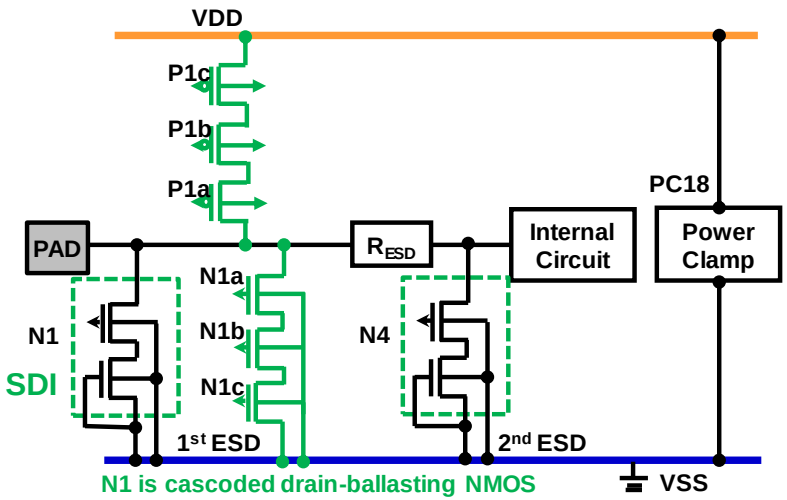


Fig.1.4
Cascoded snapback base primary protection scheme

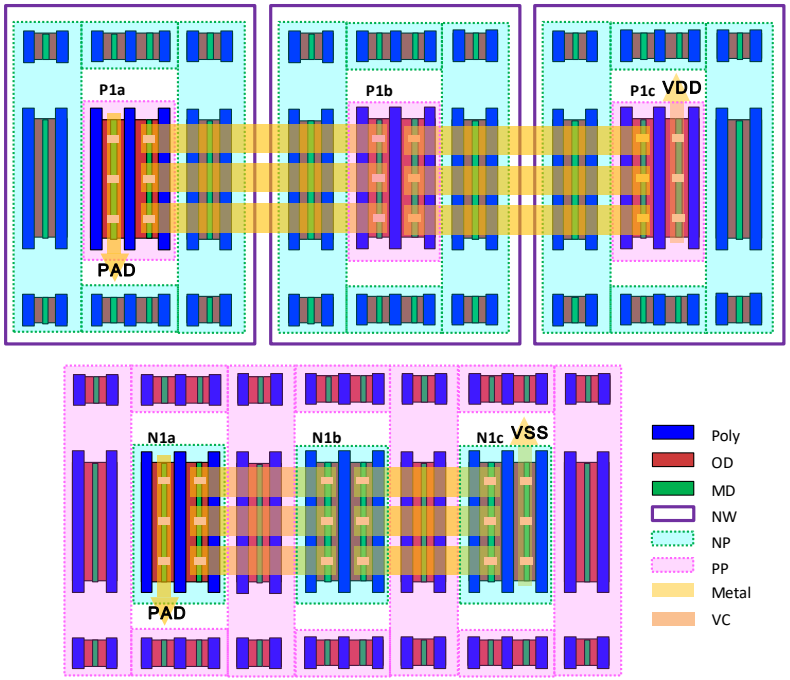


Fig.1.5
Layout view of 3-stack separated OD NMOS and 3-stack separated NW PMOS

Snapback Base (6/12)

1. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to VDD.
2. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to its active OD.
3. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to active OD of the other PMOS.
4. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to each other.
5. 1st stage PMOS are surrounded by N+ guard ring. All device inside the guard ring are the 1st stage ones only.
6. 2nd stage PMOS are surrounded by N+ guard ring. All device inside the guard ring are the 2nd stage ones only.
7. 3rd stage PMOS are surrounded by N+ guard ring.
8. For > 3 stack design scheme, the checker only check first three stage PMOS only.

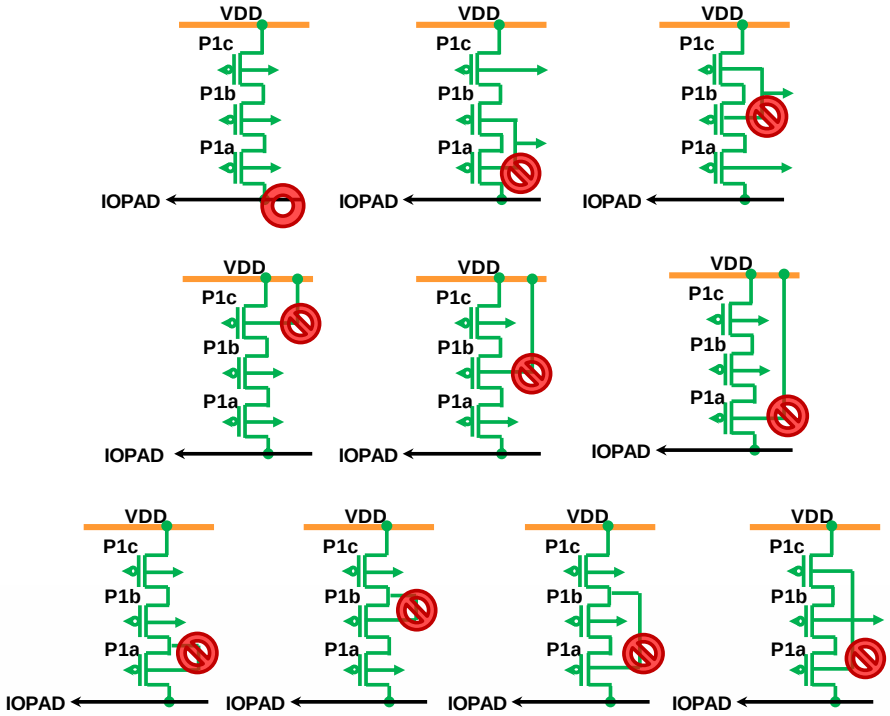


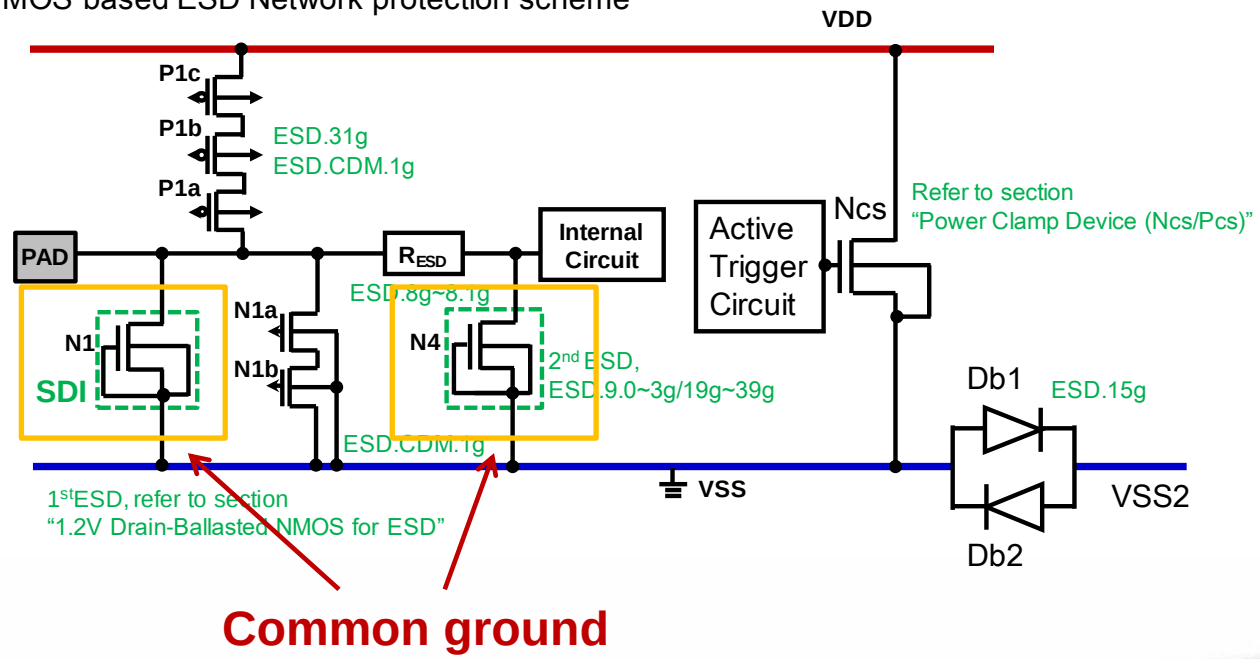
Fig.1.3 Schematic view of 3-stack PMOS with 3 separated NWs

Above devices are non-ESD current path, so the metal CD (EM) is not needed to meet ESD metal current density rule.

Snapback Base (7/12)

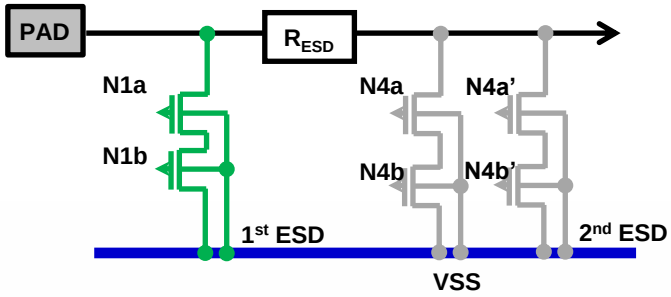
Rule No.	Category	N3 CDM peak current 5A purpose
ESD.CDM.1.3g^{U}	**All Snapback Base Primary Protection Scheme (For 1.2V/1.8V)**	**For snapback NMOS protected IOPAD, its primary ESD protection and secondary ESD protection should be on the common ground.**

MOS based ESD Network protection scheme

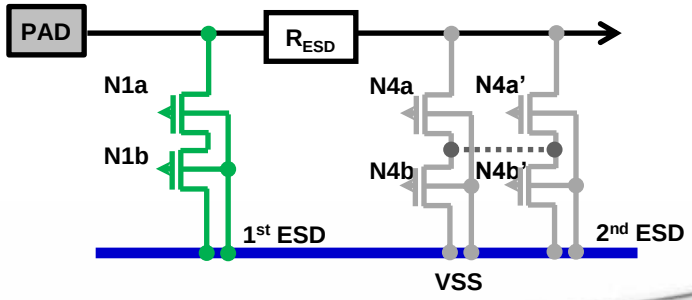


Snapback Base (8/12) -- Checking Methodology

- For ESD.CDM.1g and ESD.CDM.1.1g, most of cases should follow separate OD/separate NW criteria.
- There is one and only R*W exception for secondary ESD protection.
  - For single stage snapback MOS protected I/O pad, single stage 2nd ESD NMOS (R*W ≥ 3200um*ohm, Lg ≥ 135nm, common OD, connected to ground net directly) is allowed.
  - For 2-stage snapback MOS protected I/O pad, 2-stage 2nd ESD NMOS (R*W ≥ 3200um*ohm, Lg ≥ 135nm, common OD , connected to ground net directly) is allowed.
  - For these two rules, common OD check for cascoded 2nd ESD NMOS is performed in a "topology way".
    - When it is lack of "cross link" between first-stage HIANMOS and second-stage regular NMOS, it is recognized as a common OD structure.
    - For single stage or cascoded HIANMOS not in secondary-like connections (i.e. with cross link or not tied to ground net directly), they need to follow same guidelines as general NMOS.



w/o cross link between 1st stage and 2nd stage



w/i cross link between 1st stage and 2nd stage

Snapback Base (9/12) --

Victim MOS Type/Scheme			Victim Condition	Victim Lg	Single stage snapback protection (ESD.CDM.1g)		2/3-stage snapback protection (ESD.CDM.1.1g)	
					Condition 1 (R*W, same for VDD/VSS)	Condition 2 (sep-OD/sep-NW)	Condition 1 (R*W, same for VDD/VSS)	Condition 2 (sep-OD/sep-NW)
Single stage with the other ends tied to P/G directly or through resistor	IO	NMOS	Regular I/O NMOS or non-qualified HIANMOS	--	flag	N/A	flag	N/A
			HIANMOS 2nd ESD	>=135nm	R*W>3200ohm*um	N/A	flag	N/A
				<135nm	flag	N/A	flag	N/A
		PMOS	--	--	flag	N/A	flag	N/A
	Core	NMOS	--	--	flag	N/A	flag	N/A
		PMOS	--	--	flag	N/A	flag	N/A
Single stage with the other ends not tied to P/G directly nor through resistor	IO	NMOS	--	--	Exempted	N/A	Exempted	N/A
		PMOS	--	--	Exempted	N/A	Exempted	N/A
			NW tied to VDD		flag	N/A	flag	N/A
	Core	NMOS			flag	N/A	flag	N/A
		PMOS			flag	N/A	flag	N/A

- HIANMOS 2nd ESD is categorized by following condition. For others, they should follow guidelines for regular NMOS.
  - By nch_hia12 (single stage) or nch_hia12+regular I/O NMOS (2-stage)
  - Common OD layout structure
  - Connected to ground net directly

Snapback Base (10/12) --

Victim MOS Type/Scheme			Victim Condition	Victim Lg	Single stage snapback protection (ESD.CDM.1g)		2/3-stage snapback protection (ESD.CDM.1.1g)	
					Condition 1 (R*W, same for VDD/VSS)	Condition 2 (sep-OD/ sep-NW)	Condition 1 (R*W, same for VDD/VSS)	Condition 2 (sep-OD/ sep-NW)
2 stage Cascoded with the other ends tied to P/G directly or through resistor	IO	NMOS	Regular I/O NMOS or non-qualified HIANMOS	>=86nm	don't care	2 separated OD	flag	N/A
				<86nm	flag	N/A	flag	N/A
			HIANMOS 2nd ESD	>=135nm	flag	N/A	R*W>3200ohm*um	Common OD
				<135nm	flag	N/A	flag	N/A
		PMOS		>=86nm	flag	N/A	flag	N/A
				<86nm	flag	N/A	flag	N/A
		N/PMOS Mixed		>=86nm	flag	N/A	flag	N/A
				<86nm	flag	N/A	flag	N/A
	Core	NMOS			flag	N/A	flag	N/A
		PMOS			flag	N/A	flag	N/A
		N/PMOS Mixed			flag	N/A	flag	N/A
	IO/Core Mixed	NMOS			flag	N/A	flag	N/A
		PMOS			flag	N/A	flag	N/A
		N/PMOS Mixed			flag	N/A	flag	N/A

Snapback Base (11/12) --

Victim MOS Type/Scheme			Victim Condition	Victim Lg	Single stage snapback protection (ESD.CDM.1g)		2/3-stage snapback protection (ESD.CDM.1.1g)	
					Condition 1 (R*W, same for VDD/VSS)	Condition 2 (sep-OD/ sep-NW)	Condition 1 (R*W, same for VDD/VSS)	Condition 2 (sep-OD/ sep-NW)
2 stage Cascoded with the other ends not tied to P/G directly nor through resistor	IO	NMOS	Regular I/O NMOS or non-qualified HIANMOS	>=86nm	Exempted	N/A	Exempted	N/A
				<86nm	Exempted	N/A	Exempted	N/A
		PMOS		>=86nm	Exempted	N/A	Exempted	N/A
				<86nm	Exempted	N/A	Exempted	N/A
			NW tied to VDD	>=86nm	flag	N/A	flag	N/A
				<86nm	flag	N/A	flag	N/A
		N/PMOS Mixed		>=86nm	Exempted	N/A	Exempted	N/A
				<86nm	Exempted	N/A	Exempted	N/A
			NW tied to VDD	>=86nm	flag	N/A	flag	N/A
				<86nm	flag	N/A	flag	N/A
	Core	NMOS			flag	N/A	flag	N/A
		PMOS			flag	N/A	flag	N/A
		N/PMOS Mixed			flag	N/A	flag	N/A
	IO/Core Mixed	NMOS			flag	N/A	flag	N/A
		PMOS			flag	N/A	flag	N/A
		N/PMOS Mixed			flag	N/A	flag	N/A

Snapback Base (12/12) --

Victim MOS Type/Scheme			Victim Condition	Victim Lg	Single stage snapback protection (ESD.CDM.1g)		2/3-stage snapback protection (ESD.CDM.1.1g)	
					Condition 1 (R*W, same for VDD/VSS)	Condition 2 (sep-OD/ sep-NW)	Condition 1 (R*W, same for VDD/VSS)	Condition 2 (sep-OD/ sep-NW)
3 stage Cascoded with the other ends tied to P/G directly or through resistor Or 3 stage Cascoded with the other ends not tied to P/G directly nor through resistor Or >= 4 stage Cascoded	IO	NMOS	Regular I/O NMOS or non-qualified HIANMOS	>=86nm	don't care	2 separated OD or 3 separated OD	don't care	3 separated OD
				<86nm	flag	N/A	flag	N/A
		PMOS		>=86nm	don't care	2 separated NW && 3separated OD	don't care	3 separated NW
				<86nm	flag	N/A	flag	N/A
		N/PMOS Mixed		>=86nm	flag	N/A	flag	N/A
				<86nm	flag	N/A	flag	N/A
	Core	NMOS			flag	N/A	flag	N/A
		PMOS			flag	N/A	flag	N/A
		N/PMOS Mixed			flag	N/A	flag	N/A
	IO/Core Mixed	NMOS			flag	N/A	flag	N/A
		PMOS			flag	N/A	flag	N/A
		N/PMOS Mixed			flag	N/A	flag	N/A

Diode Base (1/11)

Rule No.	Category	N3 CDM peak current 5A purpose
ESD.CDM.2g^{U}	Diode Base Primary Protection scheme (For 0.75V/1.2V/1.5V/1.8V)	For diode based primary protection, Output driving N/PMOS need ≥ 2 stack for pure I/O device scheme and ≥ 3 stack for pure core device scheme (Figure 9.2.40). All of them need to follow separated OD structure (Figure 9.2.42 and 9.2.43). For NMOS cascoded with PMOS scheme, additional Rout in series is required. For core device cascoded with I/O device, additional Rout in series is required. Definition of separated OD 1. 1st stage NMOS (PMOS) are surrounded by P+ guard ring (N+ guard ring). All device inside the guard ring are the 1st stage ones only. 2. 2nd stage NMOS (PMOS) are surrounded by P+ guard ring (N+ guard ring). All device inside the guard ring are the 2nd stage ones only. For ≥ 2 stack pure I/O cascoded scheme, the 2nd stage NMOS (PMOS) can share guard ring with the other internal device except the 1st stage ones. 3. 3rd stage NMOS (PMOS) are surrounded by P+ guard ring (N+ guard ring) 4. The guard rings are tied to power/ground accordingly. 5. For > 2 stack design scheme, the checker only check first three stage only. Exception: 1. Single stage N/PMOS connected VDD/VSS with Rout in series (Fig.9.2.41). The Rout value depends on the total width of N/PMOS, please refer to network calculator. 2. Cascoded N/PMOS with Rout in series. The Rout value depends on the total width of cas-N/PMOS, please refer to network calculator. 3. Devices without ESD path (S/D shorted) is exempted from this rule check. This rule is based on limited test structure. For single stage MOS, it is based on gate-grounded design. For cascoded scheme, the test structure is with top-gate floating and bottom-gate grounded. ESD immunity highly depends on circuit design and real layout implantation, please ensure the MOS channel are turned off during ESD event and design is Si-proven before mass production.

Diode Base (2/11)

Rule No.	Category	N3 CDM peak current 5A purpose
ESD.CDM.2.1g^{U}	Diode Base Primary Protection scheme (For 0.75V/1.2V/1.5V/1.8V)	For diode based primary protection, snapback NMOS cannot connect to IOPAD directly or through resistor. The checked devices includes all snapback NMOS for ESD-purpose or function-purpose.

Diode Base (3/11)

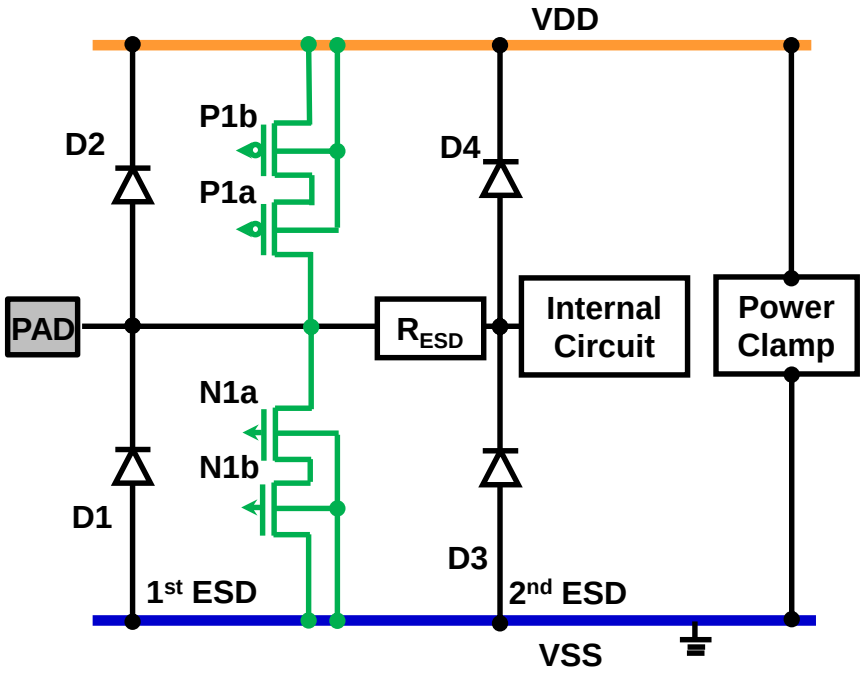


Fig.2.1
Diode Base Primary Protection scheme without serial Resistor Rout on output driving N/PMOS

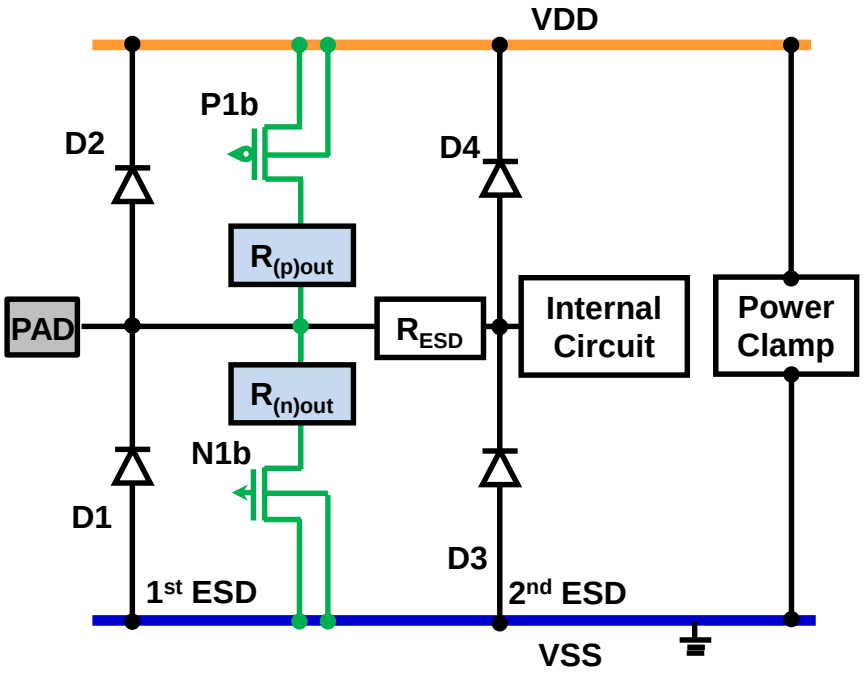


Fig.2.2
Diode Base Primary Protection scheme with serial Resistor Rout on output driving N/PMOS

Diode Base (4/11)

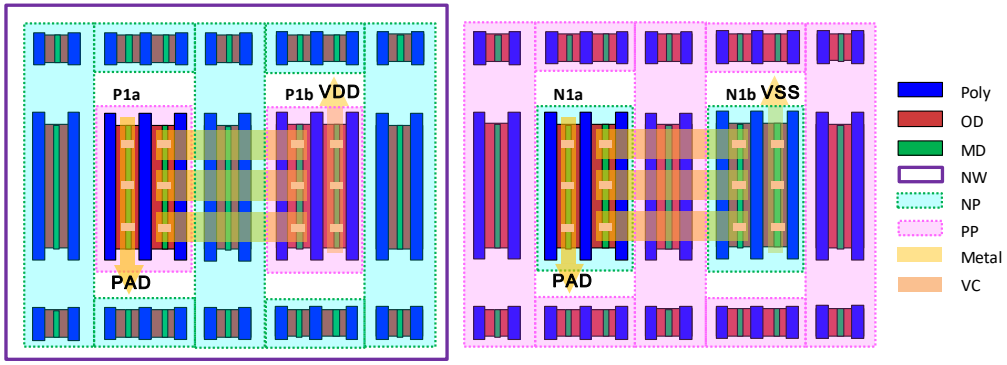


Fig.2.3
2-stack and separated OD P/NMOS

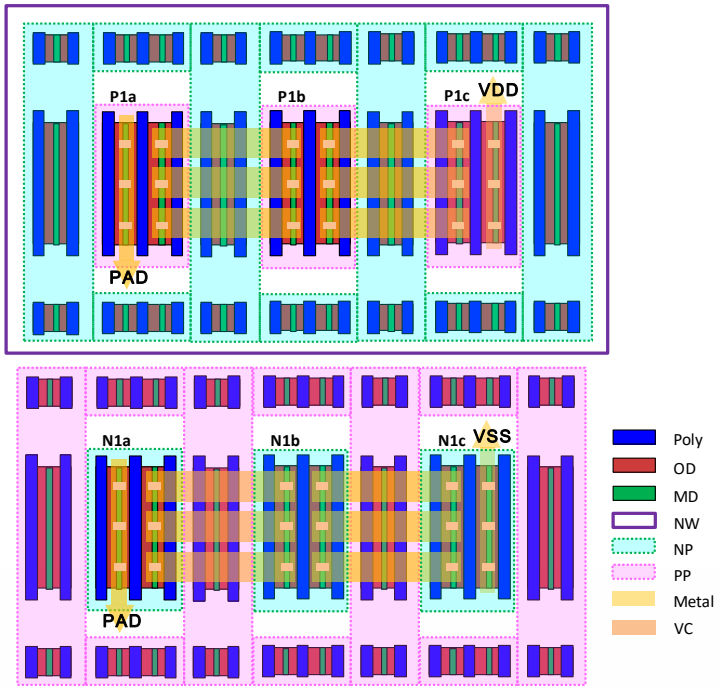
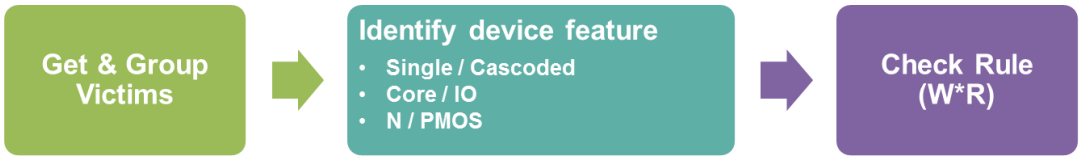
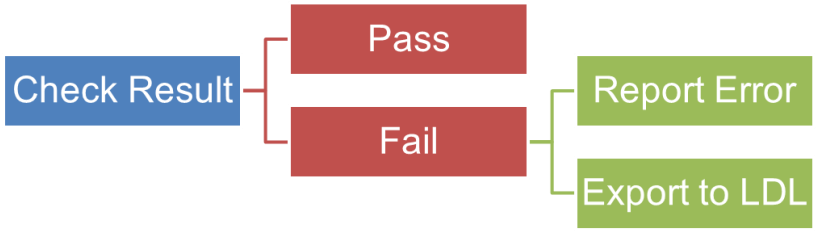


Fig.2.4
3-stack and separated OD P/NMOS

Above devices are non-ESD current path, so the metal CD (EM) is not needed to met ESD metal current density rule.

Diode Base (5/11) -- Checking Methodology





- For ESD.CDM.2g, most of cases should follow R*W criteria.
- The exception criteria for **IO device** is valid for **>= 2 stage** cascoded **pure IO NMOS** and **pure IO PMOS** scheme under **separated OD layout style**.
- The exception criteria for **core device** is valid for **>= 3 stage** cascoded **pure core NMOS** and **pure core PMOS** scheme under **separated OD layout style**.

Diode Base (6/11) -- [ESD resistor resistance] x [Device width]

Victim MOS Type/Scheme			Victim Lg	Diode based primary protection (ESD.CDM.2g)		
				Victim tied to VSS	Victim tied to VDD	LDL check for separate OD
Single stage and the other end tied to P/G directly or through resistor	IO	HIANMOS		flag	flag	N/A
		NMOS	>=135nm	23569	12242	N/A
			<135nm; >=86nm	26684	15088	N/A
			<86nm	26820	15088	N/A
		PMOS	>=135nm	13456	6618	N/A
			<135nm; >=86nm	30304	13726	N/A
			<86nm	57058	29130	N/A
	Core	NMOS	>=55nm	7251	4704	N/A
			<55nm	24177	16384	N/A
		PMOS	>=55nm	11550	7296	N/A
			<55nm	31620	22015	N/A

Victim MOS Type/Scheme			Victim Lg	Diode based primary protection (ESD.CDM.2g)		
				Victim tied to VSS	Victim tied to VDD	LDL check for separate OD
Single stage and the other end not tied to P/G directly nor through resistor	IO	HIANMOS		Exempted	Exempted	N/A
		NMOS	>=135nm	Exempted	Exempted	N/A
			<135nm; >=86nm	Exempted	Exempted	N/A
			<86nm	Exempted	Exempted	N/A
		PMOS	>=135nm	Exempted	Exempted	N/A
			<135nm; >=86nm	Exempted	Exempted	N/A
			<86nm	Exempted	Exempted	N/A
	Core	NMOS	>=55nm	Exempted	Exempted	N/A
			<55nm	Exempted	Exempted	N/A
		PMOS	>=55nm	Exempted	Exempted	N/A
			<55nm	Exempted	Exempted	N/A

- HIANMOS 2nd ESD is categorized by following condition. For others, they should follow guidelines for regular NMOS.
  - By nch_hia12 (single stage) or nch_hia12+regular I/O NMOS (2-stage). 3-stage or more is not available.
  - Common OD layout structure; Connected to ground net directly.

Diode Base (7/11) -- [ESD resistor resistance] x [Device width]

Victim MOS Type/Scheme			Victim Lg	Diode based primary protection (ESD.CDM.2g)		
				Victim tied to VSS	Victim tied to VDD	Separated OD exemption for small R*W scheme (LDL check)
2 stage Cascoded and the other end tied to P/G directly or through resistor	IO	HIANMOS		flag	flag	N/A
		NMOS	>=135nm	8486	2198	YES
			<135nm; >=86nm	10122	3045	YES
			<86nm	11315	3905	YES
		PMOS	>=135nm	12966	138	YES
			<135nm; >=86nm	20817	1837	YES
			<86nm	20817	1837	YES
		N/PMOS Mixed	>=135nm	23569	12242	N/A
			<135nm; >=86nm	30304	15088	N/A
			<86nm	57058	29130	N/A
	Core	NMOS	>=55nm	2322	243	N/A
			<55nm	10882	5059	N/A
		PMOS	>=55nm	1515	0	N/A
			<55nm	18937	10231	N/A
		N/PMOS Mixed	>=55nm	11550	7296	N/A
			<55nm	31620	22015	N/A
	Mix	NMOS	>=55nm	2322	243	N/A
			<55nm	10882	5059	N/A
		PMOS	>=55nm	1515	0	N/A
			<55nm	18937	10231	N/A
		N/PMOS Mixed	>=55nm	11550	7296	N/A
			<55nm	31620	22015	N/A

- For cascoded victim scheme, PERC use following method to calculate Rout*Width value.
  - Take the first-stage MOS device width as “Width”
  - Take the Hi-R resistance value from IOPAD to first-stage MOS device as “Rout”
  - Consider all MOS device with source/drain connected in series from IOPAD (tied to IOPAD directly or through resistor) to VDD/VSS (tied to VDD/VSS directly or through resistor)
  - For > 3 stage design scheme, PERC checks first three stages MOS and R*W criteria follows the same as “tied to VSS” groups.
- HIANMOS 2nd ESD is categorized by following condition. For others, they should follow guidelines for regular NMOS.
  - By nch_hia12 (single stage) or nch_hia12+regular I/O NMOS (2-stage). 3-stage or more is not available.
  - Common OD layout structure; Connected to ground net directly.

Diode Base (8/11) -- [ESD resistor resistance] x [Device width]

Victim MOS Type/Scheme			Victim Lg	Diode based primary protection (ESD.CDM.2g)		
				Victim tied to VSS	Victim tied to VDD	Separated OD exemption for small R*W scheme (LDL check)
2 stage Cascoded and the other end not tied to P/G directly nor through resistor	IO	HIANMOS		Exempted	Exempted	N/A
		NMOS	>=135nm	Exempted	Exempted	N/A
			<135nm; >=86nm	Exempted	Exempted	N/A
			<86nm	Exempted	Exempted	N/A
		PMOS	>=135nm	Exempted	Exempted	N/A
			<135nm; >=86nm	Exempted	Exempted	N/A
			<86nm	Exempted	Exempted	N/A
		N/PMOS Mixed	>=135nm	Exempted	Exempted	N/A
			<135nm; >=86nm	Exempted	Exempted	N/A
			<86nm	Exempted	Exempted	N/A
	Core	NMOS	>=55nm	Exempted	Exempted	N/A
			<55nm	Exempted	Exempted	N/A
		PMOS	>=55nm	Exempted	Exempted	N/A
			<55nm	Exempted	Exempted	N/A
		N/PMOS Mixed	>=55nm	Exempted	Exempted	N/A
			<55nm	Exempted	Exempted	N/A
	Mix	NMOS	>=55nm	Exempted	Exempted	N/A
			<55nm	Exempted	Exempted	N/A
		PMOS	>=55nm	Exempted	Exempted	N/A
			<55nm	Exempted	Exempted	N/A
		N/PMOS Mixed	>=55nm	Exempted	Exempted	N/A
			<55nm	Exempted	Exempted	N/A

- For cascoded victim scheme, PERC use following method to calculate Rout*Width value.
  - Take the first-stage MOS device width as “Width”
  - Take the Hi-R resistance value from IOPAD to first-stage MOS device as “Rout”
  - Consider all MOS device with source/drain connected in series from IOPAD (tied to IOPAD directly or through resistor) to VDD/VSS (tied to VDD/VSS directly or through resistor)
  - For > 3 stage design scheme, PERC checks first three stages MOS and R*W criteria follows the same as “tied to VSS” groups.
- HIANMOS 2nd ESD is categorized by following condition. For others, they should follow guidelines for regular NMOS.
  - By nch_hia12 (single stage) or nch_hia12+regular I/O NMOS (2-stage). 3-stage or more is not available.
  - Common OD layout structure; Connected to ground net directly.

Diode Base (9/11) -- [ESD resistor resistance] x [Device width]

Victim MOS Type/Scheme			Victim Lg	Diode based primary protection (ESD.CDM.2g)		
				Victim tied to VSS	Victim tied to VDD	Separated OD exemption for small R*W scheme (LDL check)
3 stage Cascoded and the other end tied to P/G directly or through resistor	IO	HIANMOS		flag	flag	N/A
		NMOS	>=135nm	4810	0	YES
			<135nm; >=86nm	5278	170	YES
			<86nm	5433	0	YES
		PMOS	>=135nm	2588	0	YES
			<135nm; >=86nm	2596	0	YES
			<86nm	3996	0	YES
		N/PMOS Mixed	>=135nm	23569	12242	N/A
			<135nm; >=86nm	30304	15088	N/A
			<86nm	57058	29130	N/A
	Core	NMOS	>=55nm	1368	0	YES (3 Separated OD)
			<55nm	2000	208	YES (3 Separated OD)
		PMOS	>=55nm	363	0	YES (3 Separated OD)
			<55nm	7579	163	YES (3 Separated OD)
		N/PMOS Mixed	>=55nm	11550	7296	N/A
			<55nm	31620	22015	N/A
	Mix	NMOS	>=55nm	1368	0	YES (3 Separated OD)
			<55nm	2000	208	YES (3 Separated OD)
		PMOS	>=55nm	363	0	YES (3 Separated OD)
			<55nm	7579	163	YES (3 Separated OD)
		N/PMOS Mixed	>=55nm	11550	7296	N/A
			<55nm	31620	22015	N/A

- For cascoded victim scheme, PERC use following method to calculate Rout*Width value.
  - Take the first-stage MOS device width as “Width”
  - Take the Hi-R resistance value from IOPAD to first-stage MOS device as “Rout”
  - Consider all MOS device with source/drain connected in series from IOPAD (tied to IOPAD directly or through resistor) to VDD/VSS (tied to VDD/VSS directly or through resistor)
  - For > 3 stage design scheme, PERC checks first three stages MOS and R*W criteria follows the same as “tied to VSS” groups.
- HIANMOS 2nd ESD is categorized by following condition. For others, they should follow guidelines for regular NMOS.
  - By nch_hia12 (single stage) or nch_hia12+regular I/O NMOS (2-stage). 3-stage or more is not available.
  - Common OD layout structure; Connected to ground net directly.

Diode Base (10/11) -- [ESD resistor resistance] x [Device width]

Victim MOS Type/Scheme			Victim Lg	Diode based primary protection (ESD.CDM.2g)		
				Victim tied to VSS	Victim tied to VDD	Separated OD exemption for small R*W scheme (LDL check)
3 stage Cascoded and the other end not tied to P/G directly nor through resistor or 4 stage Cascoded	IO	HIANMOS		flag	flag	N/A
		NMOS	>=135nm	4810	4810	YES
			<135nm; >=86nm	5278	5278	YES
			<86nm	5433	5433	YES
		PMOS	>=135nm	2588	2588	YES
			<135nm; >=86nm	2596	2596	YES
			<86nm	3996	3996	YES
		N/PMOS Mixed	>=135nm	23569	23569	N/A
			<135nm; >=86nm	30304	30304	N/A
			<86nm	57058	57058	N/A
	Core	NMOS	>=55nm	1368	1368	YES (3 Separated OD)
			<55nm	2000	2000	YES (3 Separated OD)
		PMOS	>=55nm	363	363	YES (3 Separated OD)
			<55nm	7579	7579	YES (3 Separated OD)
		N/PMOS Mixed	>=55nm	11550	11550	N/A
			<55nm	31620	31620	N/A
	Mix	NMOS	>=55nm	1368	1368	YES (3 Separated OD)
			<55nm	2000	2000	YES (3 Separated OD)
		PMOS	>=55nm	363	363	YES (3 Separated OD)
			<55nm	7579	7579	YES (3 Separated OD)
		N/PMOS Mixed	>=55nm	11550	11550	N/A
			<55nm	31620	31620	N/A

- For cascoded victim scheme, PERC use following method to calculate Rout*Width value.
  - Take the first-stage MOS device width as “Width”
  - Take the Hi-R resistance value from IOPAD to first-stage MOS device as “Rout”
  - Consider all MOS device with source/drain connected in series from IOPAD (tied to IOPAD directly or through resistor) to VDD/VSS (tied to VDD/VSS directly or through resistor)
  - For > 3 stage design scheme, PERC checks first three stages MOS and R*W criteria follows the same as “tied to VSS” groups.
- HIANMOS 2nd ESD is categorized by following condition. For others, they should follow guidelines for regular NMOS.
  - By nch_hia12 (single stage) or nch_hia12+regular I/O NMOS (2-stage). 3-stage or more is not available.
  - Common OD layout structure; Connected to ground net directly.

Diode Base (11/11) -- [ESD resistor resistance] x [Device width]

- For ESD.CDM.2g, the constant of [ESD resistor resistance] times [device width] plays an important role in identifying ESD risky scheme.
- This constant varies from device type and scheme. The default value is defined in **perc_n03_constant.tcl**.

```
set ::g_hc_dd_vic(default)              [list ESD.CDM.2gU >= {0 0}]
set ::g_hc_dd_vic(mn_io_hia_gnd_wxr)    [list ESD.CDM.2gU >= {0 3200}                    ]
set ::g_hc_dd_vic(mn_io_hia_pwr_wxr)    [list ESD.CDM.2gU >= {0 3200}                    ]
set ::g_hc_dd_vic(mn_io_gnd_wxr)        [list ESD.CDM.2gU >= {0.135 2419 0 5063}         ]
set ::g_hc_dd_vic(mn_io_pwr_wxr)        [list ESD.CDM.2gU >= {0.135 1005 0 2261}         ]
set ::g_hc_dd_vic(mp_io_gnd_wxr)        [list ESD.CDM.2gU >= {0.135 43169 0 65868}       ]
set ::g_hc_dd_vic(mp_io_pwr_wxr)        [list ESD.CDM.2gU >= {0.135 14425 0 25910}       ]
set ::g_hc_dd_vic(mn_core_gnd_wxr)      [list ESD.CDM.2gU >= {0.084 1087 0.02 1690 0 4633}  ]
set ::g_hc_dd_vic(mn_core_pwr_wxr)      [list ESD.CDM.2gU >= {0.084 553 0.02 913 0 2668}    ]
set ::g_hc_dd_vic(mp_core_gnd_wxr)      [list ESD.CDM.2gU >= {0.084 9847 0.02 41820 0 59679}]
set ::g_hc_dd_vic(mp_core_pwr_wxr)      [list ESD.CDM.2gU >= {0.084 4971 0.02 25243 0 56505}]
set ::g_hc_dd_vic(cas_mn_io_hia_gnd_wxr) [list ESD.CDM.2gU >= {0 3200}                   ]
set ::g_hc_dd_vic(cas_mn_io_hia_pwr_wxr) [list ESD.CDM.2gU >= {0 3200}                   ]
set ::g_hc_dd_vic(cas_mn_io_gnd_wxr)    [list ESD.CDM.2gU >= {0.135 2556 0 2725}         ]
set ::g_hc_dd_vic(cas_mn_io_pwr_wxr)    [list ESD.CDM.2gU >= {0.135 1255 0 1255}         ]
set ::g_hc_dd_vic(cas_mp_io_gnd_wxr)    [list ESD.CDM.2gU >= {0.135 22351 0 29941}       ]
set ::g_hc_dd_vic(cas_mp_io_pwr_wxr)    [list ESD.CDM.2gU >= {0.135 0 0 1406}            ]
set ::g_hc_dd_vic(cas_mm_io_gnd_wxr)    [list ESD.CDM.2gU >= {0.135 43169 0 65868}       ]
set ::g_hc_dd_vic(cas_mm_io_pwr_wxr)    [list ESD.CDM.2gU >= {0.135 14425 0 25910}       ]
set ::g_hc_dd_vic(cas_mn_core_gnd_wxr)  [list ESD.CDM.2gU >= {0.084 842 0.02 929 0 4204}    ]
set ::g_hc_dd_vic(cas_mn_core_pwr_wxr)  [list ESD.CDM.2gU >= {0.084 257 0.02 257 0 1190}    ]
set ::g_hc_dd_vic(cas_mp_core_gnd_wxr)  [list ESD.CDM.2gU >= {0.084 8786 0.02 34103 0 51135}]
set ::g_hc_dd_vic(cas_mp_core_pwr_wxr)  [list ESD.CDM.2gU >= {0.084 0 0.02 2018 0 20757}    ]
set ::g_hc_dd_vic(cas_mm_core_gnd_wxr)  [list ESD.CDM.2gU >= {0.084 9847 0.02 41820 0 59679}]
set ::g_hc_dd_vic(cas_mm_core_pwr_wxr)  [list ESD.CDM.2gU >= {0.084 4971 0.02 25243 0 56505}]
set ::g_hc_dd_vic(cas_mn_io_hia_wxr)    [list ESD.CDM.2gU >= {0 3200}                    ]
set ::g_hc_dd_vic(cas_mn_io_wxr)        [list ESD.CDM.2gU >= {0.135 2556 0 2725}         ]
set ::g_hc_dd_vic(cas_mp_io_wxr)        [list ESD.CDM.2gU >= {0.135 22351 0 29941}       ]
set ::g_hc_dd_vic(cas_mm_io_wxr)        [list ESD.CDM.2gU >= {0.135 43169 0 65868}       ]
set ::g_hc_dd_vic(cas_mn_core_wxr)      [list ESD.CDM.2gU >= {0.084 842 0.02 929 0 4204}    ]
set ::g_hc_dd_vic(cas_mp_core_wxr)      [list ESD.CDM.2gU >= {0.084 8786 0.02 34103 0 51135}]
set ::g_hc_dd_vic(cas_mm_core_wxr)      [list ESD.CDM.2gU >= {0.084 9847 0.02 41820 0 59679}]
set ::g_hc_dd_vic(ldl_conditions)       [list [list {stack 2} {vol io}   {mos mn}] [list {stack 2} {vol io}   {mos mp}] \
                                              [list {stack n} {vol io}   {mos mn}] [list {stack n} {vol io}   {mos mp}] \
                                              [list {stack n} {vol core} {mos mn}] [list {stack n} {vol core} {mos mp}] ]
```

Warnings in Pure Topology check

- For ESD.CDM.2g, there are two ways to pass rule check. One of them is to meet R*W criteria; the other one is adopting separate OD layout style. Designer can based on their design requirement to determine the final implementation.
- To get early R*W alarm in pure topology check stage, user can find and refer to violations named as “ESD.CDM.2gu_topo.” All these flags are dedicate for those victims which do not meet R*W criteria and may pass rule by separate OD layout style. Note that these warnings are for pure topology check only.
- As for the other sets of violations named without *_topo, they are violations cannot fix by separate OD layout style. Please take care them by changing design scheme.

Check / Cell	Results	P	R	W
Check ESD.WARN.3gu	772	772	0	0
Check ESD.NET.1gu	61	61	0	0
Check ESD.CDM.6g	13	13	0	0
Check ESD.CDM.2gu_topo	5	5	0	0
Check ESD.CDM.2gu	1	1	0	0
Check ESD.CDM.1gu	50	50	0	0
Check ESD.9gu	9	9	0	0

Internal Power for ESD.CDM.1/1.1/2gU

- For ESD.CDM.1/1.1/2gU, the net connected to more than 10000 devices will be set to internal power, and victim path will be checked as tied to ground.
- The default devices number is defined by set ::g_int_pwr_limit 10000 in **perc_n03_constant.tcl**.

```
## ================================================================================
##         User Defined Variables
## ================================================================================
set tcl_precision        12 ; # tcl precision
set ::g_unit              1 ; # unit of net list (default is 1 meter, set 1e-6 for um)
set ::g_dio_lw_ratio     10 ; # diode length/width ratio, used to calculate diode perimeter from area
set ::g_trace_limit      10 ; # maximum distance to trace a path type to source net (must be > 0)
set ::g_result_limit   5000 ; # maximum number of reported devices in some rule checks (set 0 to show all)
set ::g_int_pwr_limit 10000 ; # net with more than this number of devices connected will be recognized as internal power
```

Back to Back diode

Rule	N3 CDM peak current 5A purpose
ESD.CDM.B.1g^{U}	On-chip global ESD bus (user defined) is required, each Ground bus need connecting the global bus with back-to-back (B2B) diode or metal in short scheme. The back to back (B2B) diode can be HIA diode. (Fig. 9.2.44) The perimeter of HIA diode as back to back diode need to meet HIA.3g.

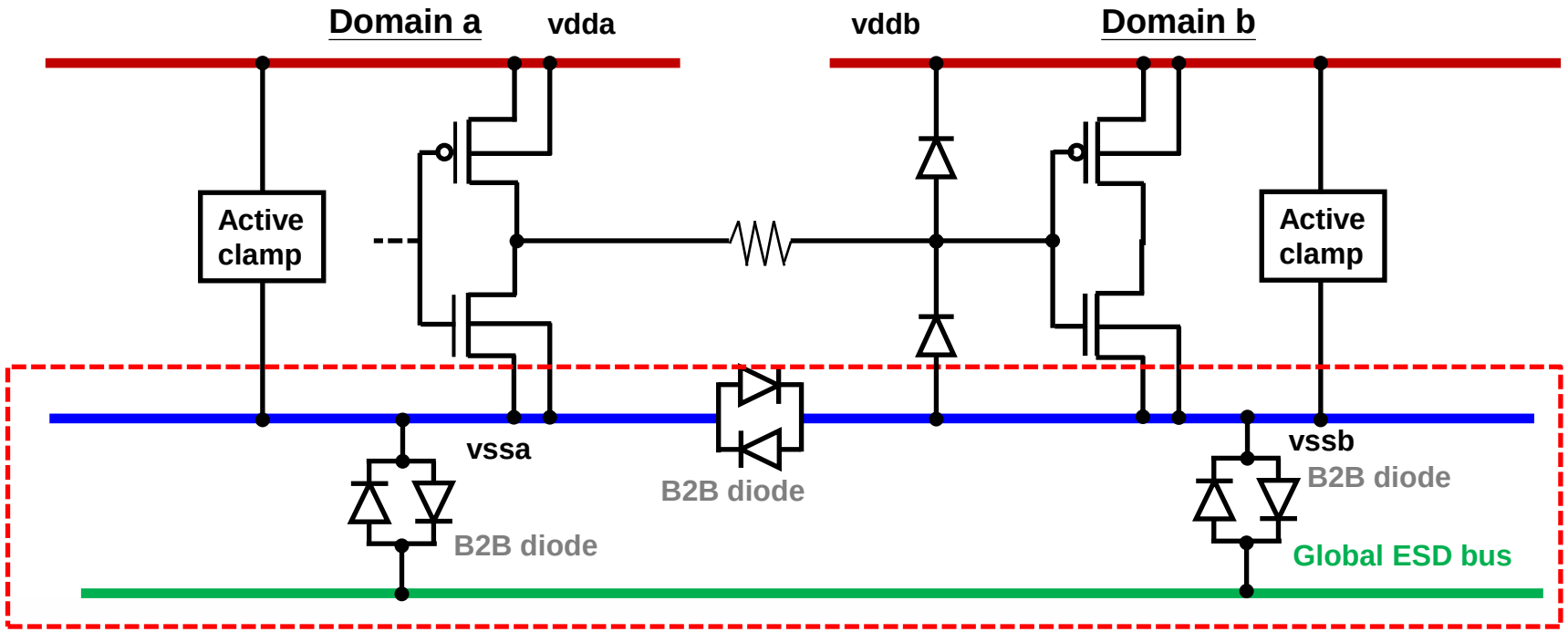


Fig.B.1 Back to Back diode for global ESD bus

Back to Back diode

Rule	N3 CDM peak current 5A purpose
ESD.CDM.B.2g^{U}	Cross domain back to back (B2B) diode is needed. (Fig. 9.2.45) The back to back diode can be HIA diode. The perimeter of HIA diode as back to back diode need to meet HIA.3g For COMMON_GROUND protection scheme, this rule can be disable. Checker will skip this rule.

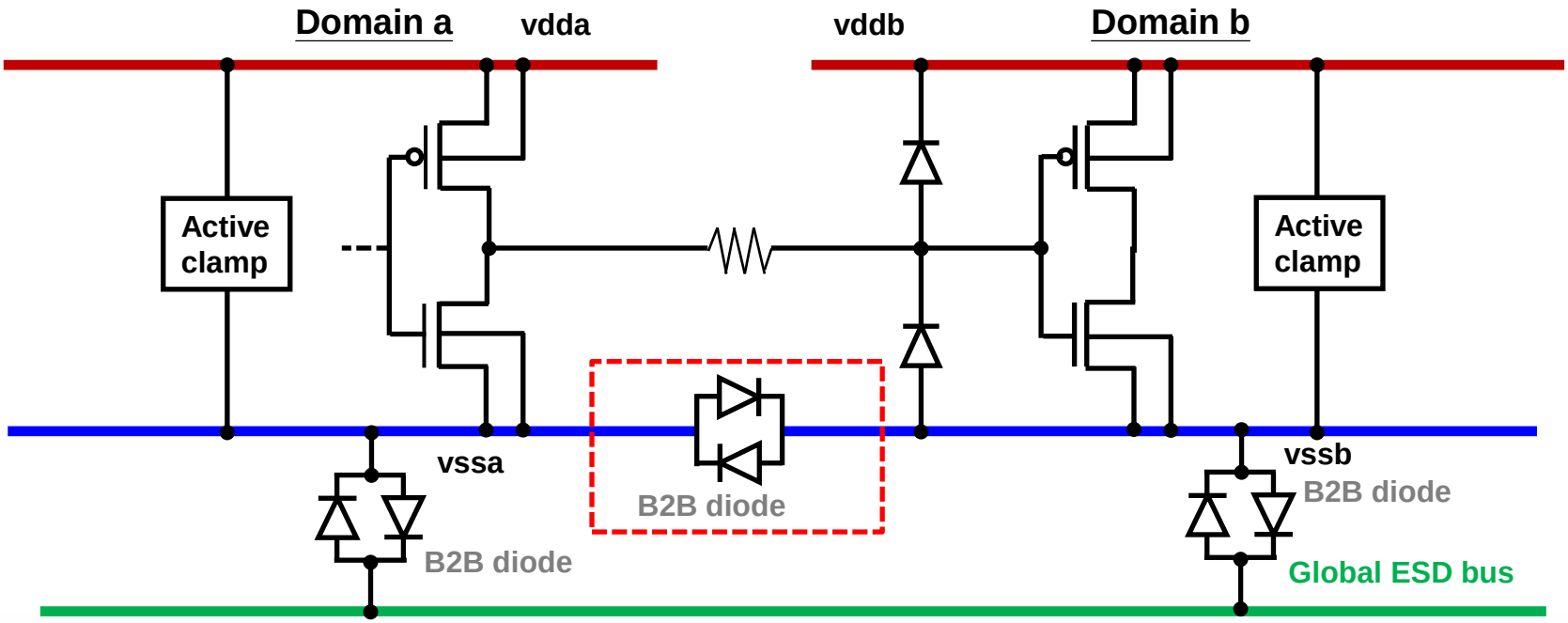


Fig.B.1 Back to Back diode for global ESD bus

1.8V Power Clamp

Rule No.	Category	N3 CDM peak current 5A purpose
ESD.CDM.4g^{U}	1.8V power clamp	For cascoded (1.8V) power clamp protected power domain, additional reverse HIA diode (in parallel with cascoded power clamp) is needed. The area of HIA diode needs to meet HIA.3.1g. (Fig. 9.2.46)

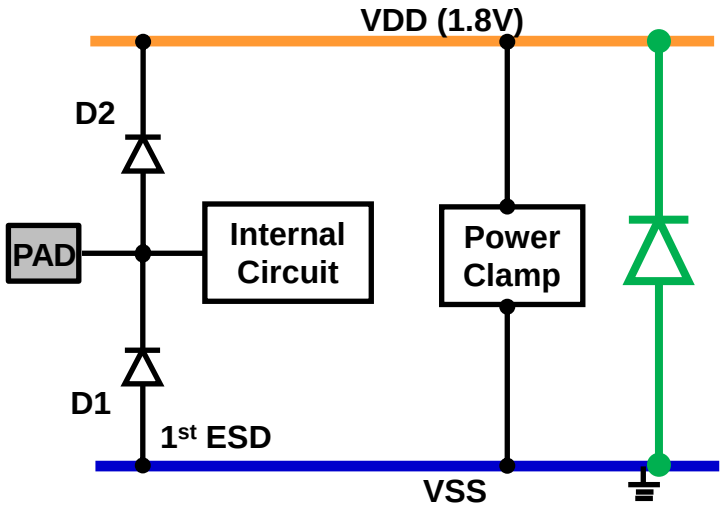


Fig.4 Reverse diode for 1.8V power clamp

Power clamp Fool Proof

Rule No.	Category	N3 CDM peak current 5A purpose
ESD.CDM.6.0g	Power Clamp	Core ESD power clamp (not in OD2) can not be used for > 0.96V application. (This rule doesn't support DV_SYNC function)
ESD.CDM.6.1g		Single stage I/O ESD power clamp can not be used for > 1.65V application. Single stage means all ACTIVE OD SEGMENT on single ACTIVE OD are connected to power or ground net. (This rule doesn't support DV_SYNC function)

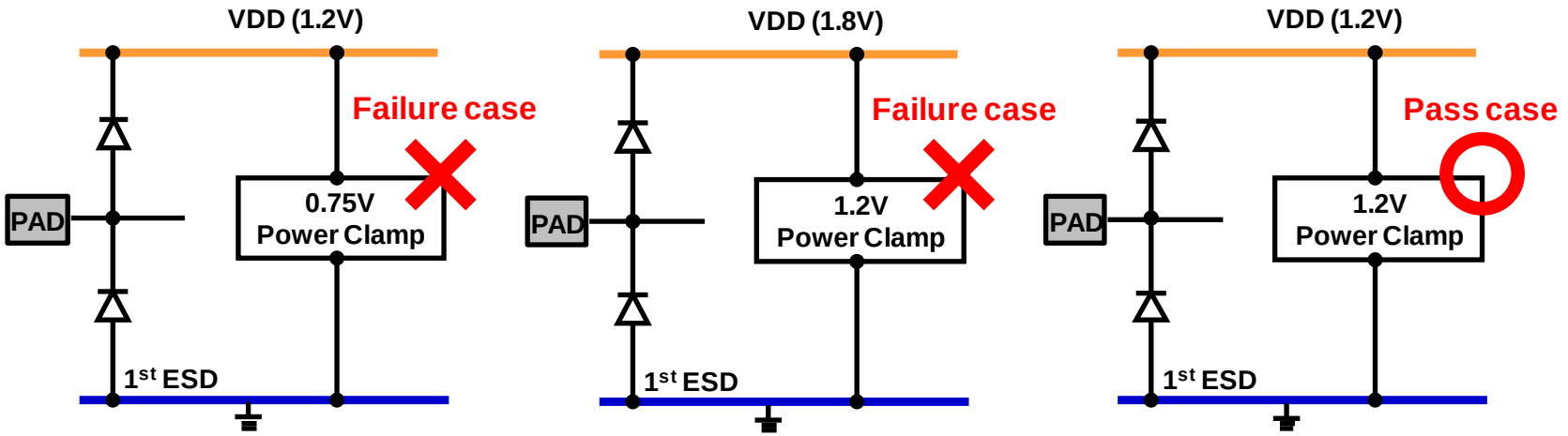


Fig.6 Power clamp implementation rule

DISTP2P, ESD Metal Bus

HIA Diode conduction resistance (Rpdio, Rndio) is calculated by total fin count:

- HIA Diode Ron = 88 / Pj (Pj in um)

Power clamp conduction resistance (Rpc1, Rpc2) is calculated by total fin count:

- Core Power Clamp Ron = 27435 / fin#
- I/O Power Clamp Ron = 32870 / fin#

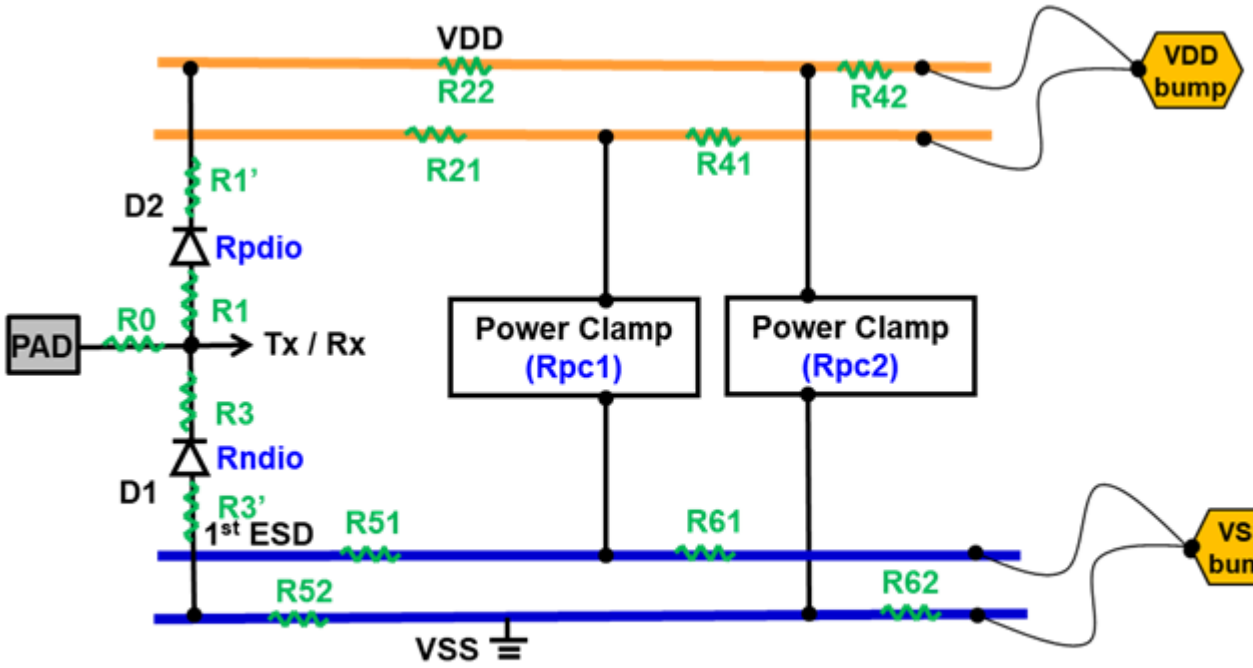


Figure 9.2.61 ESD discharging path resistance of ESD diode to power/ground bump through power clamp

Power clamp placement

Rule	N3 CDM peak current 5A purpose
ESD.CDM.C.2g^{U}	For any MOS connected to Power or Ground, there should be a power clamp with spacing ≤ 1500 µm or Rbus ≤ 0.5 ohm for core (0.75V) domain and ≤ 2 ohm for I/O (1.2V) domain. (Fig.9.2.48)

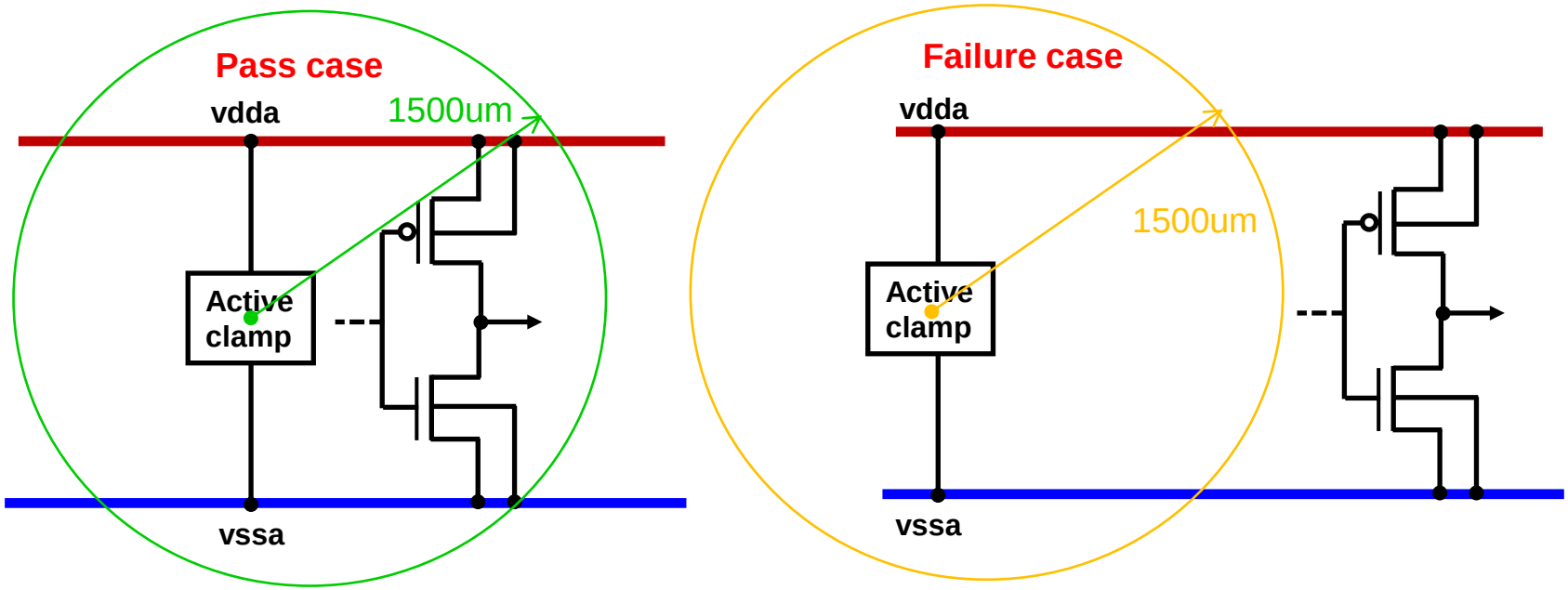


Fig.C.2 Power clamp placement uniformity for cross domain interface design

Gate direct tie to P/G

Rule	N3 CDM peak current 5A purpose
ESD.CDM.C.3.1g^{U}	For any core MOS with gate and source/drain connected between power or ground, there should be a single stage core power clamp with spacing ≤ 1500μm or Rbus ≤ 0.5 ohm. (Fig.9.2.48.1) The power clamp and the protected core MOS must be at the same P/G pair. Lack of direct clamping ESD device is not allowed. Decap is excluded from this rule.
ESD.CDM.C.3.2g^{U}	For any I/O MOS with gate and source/drain connected between power or ground, there should be a single stage I/O or core power clamp with spacing ≤ 1500 μm or Rbus ≤ 2 ohm. (Fig.9.2.48.1) The power clamp and the protected I/O MOS must be at the same P/G pair. Lack of direct clamping ESD device is not allowed. Decap is excluded from this rule.

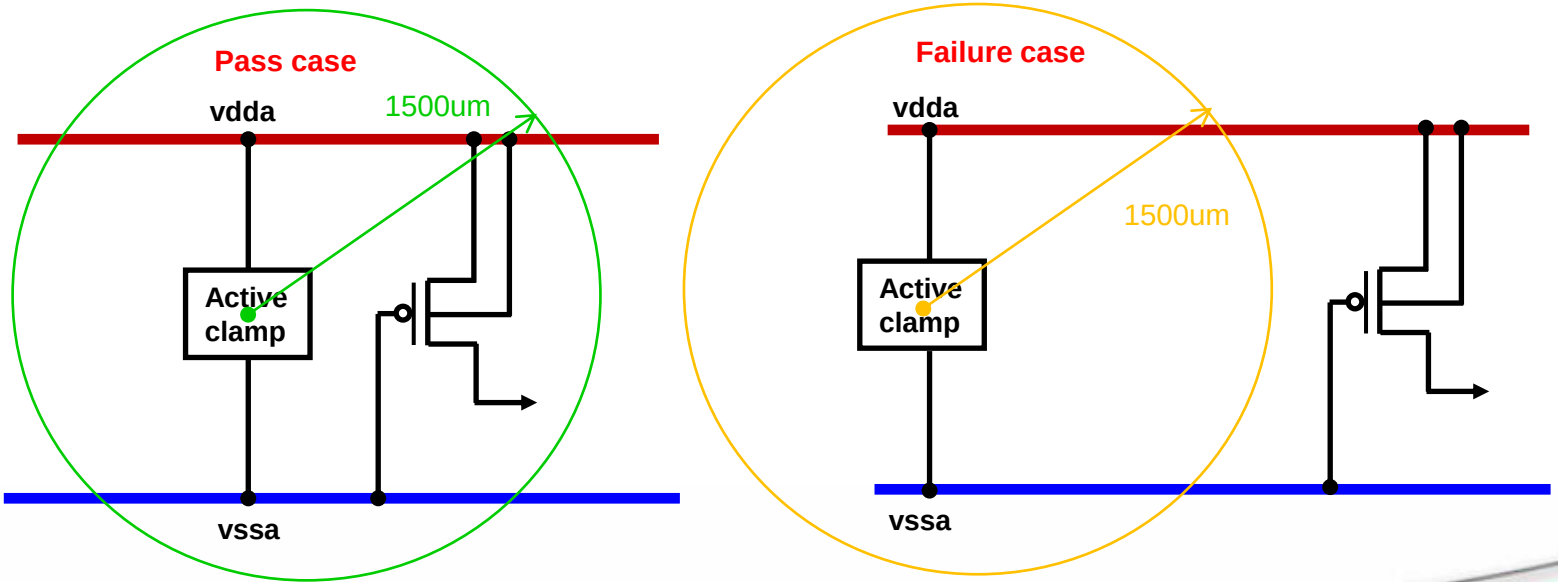


Fig.C.3 Power clamp placement uniformity for gate direct tie to P/G design.

Switch to show the number of stack for ESD.XDM.VIC.3/4gU

- **Users can turn on the switch of SHOW_XPWR_STACK in perc_n03_xxx.top file to show the number of transistors and resistors across power domain nets for ESD.XDM.VIC.3/4gU :**

```
//#DEFINE SHOW_XPWR_STAC
    // Turn on to show the number of transistors and resistors across power domain nets
    // By default, only "single" or "cascoded" stack information will be shown in the result
    // When this switch is enabled, there could be runtime performance issue in chip level design
    // The affected rules: ESD.XDM.VIC.3gU, ESD.XDM.VIC.4gU
```

PERC Methodology

(N3 DRM Rules for CDM Checker)

-CDM 6A/7A/9A ESD guidelines

CDM 6A/7A/9A ESD guidelines

- Controlled by switch “CDM6A” / “CDM7A” / “CDM9A” (turn off by default)

		CDM 5A (FWHM < 1ns)	CDM 6A (FWHM < 1ns)	CDM 7A (FWHM < 1ns)	CDM 9A (FWHM < 1ns)
Primary ESD & B2B diode	Primary ESD availability (ESD.NET.1g^{U}/ ESD.NET.1.1g^{U}/ ESD.CDM6A/7A/9A.NET.1g^{U})	• Drain-ballasted NMOS • HIA diode	• HIA diode	• HIA diode	• HIA diode
	Single stage Drain-ballasted NMOS (ESD.18g)	490um	N/A	N/A	N/A
	2-stage cascoded Drain-ballasted NMOS (ESD.27g)	540um	N/A	N/A	N/A
	HIA Diode (HIA.3g/ HIA.3.1g)	240um/36um^2	240um/36um^2	400um/60um^2	480um/72um^2
	LC HIA Diode (ESD.LC.3g/ ESD.LC.3.1g)	130um/18um^2	130um/18um^2	260um/30um^2	300um/36um^2
	B2B diode (ESD.15g)	240um	240um	400um	480um
Secondary ESD	ESD Resistor width (ESD.8.1g^{U}/ ESD.CDM7A/9A.8.1g^{U})	2.06um	2.06um	3.30um	5.15um
	Secondary ESD availability (ESD.9.0g^{U}/ ESD.CDM6A/7A/9A.9.0g^{U})	• Drain-ballasted NMOS • HIA diode	• HIA diode	• HIA diode	• HIA diode
	Secondary ESD NMOS device total width (ESD.9.1.1g^{U})	4um	N/A	N/A	N/A
Power clamp	IO power clamp total fin count (ESD.40g)	76400fins	76400fins	122300fins	145200fins
	Core power clamp total fin count (ESD.40.1g)	84000fins	84000fins	134400fins	160500fins
	2-stack cascoded IO power clamp total fin count (ESD.40.2g^{U})	84000fins	84000fins	134400fins	160500fins
	Total fin count for unit cell (DRC ESD.40.3g/ ESD.40.3.1g^{U})	15200fins	15200fins	38000fins	45800fins
	3.3V 3-stack cascoded IO power clamp total fin count (ESD.40.4g^{U})	143000fins	143000fins	222000fins	272000fins

CDM 6A/7A/9A ESD guidelines

- **Controlled by switch "CDM6A" / "CDM7A" / "CDM9A" (turn off by default)**

		CDM 5A (FWHM < 1ns)	CDM 6A (FWHM < 1ns)	CDM 7A (FWHM < 1ns)	CDM 9A (FWHM < 1ns)
HiCDM Rule	Back-to-Back diode to global ESD bus (ESD.CDM.B.1g^{U})	• HIA diode (240um)	• HIA diode (240um)	• HIA diode (400um)	• HIA diode (480um)
	Back-to-Back diode for cross domain (ESD.CDM.B.2g^{U})				
	Power/Ground reverse diode for cascoded power clamp protected domain (ESD.CDM.4g^{U})	36um^2	36um^2	60um^2	72um^2
	Power clamp Placement for all MOS (ESD.CDM.C.2g^{U})	1500um (0.5ohm/2ohm)	1500um (0.5ohm/2ohm)	1350um (0.4ohm/1.5ohm)	1250um (0.35ohm/1.1ohm)
	Power clamp Placement for core MOS gate (ESD.CDM.C.3.1g^{U})	1500um (0.5ohm)	1500um (0.5ohm)	1350um (0.4ohm)	1250um (0.35ohm)
	Power clamp Placement for IO MOS gate (ESD.CDM.C.3.2g^{U})	1500um (2ohm)	1500um (2ohm)	1350um (1.5ohm)	1250um (1.1ohm)
	Power clamp Placement for IO/core cross domain (ESD.CDM.C.4g^{U})	--	--	500um (0.1ohm/0.5ohm)	410um (0.08ohm/0.4ohm)
	B2B diode Placement for IO/core cross domain (ESD.CDM.C.4.1g^{U})	--	--	500um (0.1ohm/0.5ohm)	410um (0.08ohm/0.4ohm)
	Power clamp Placement for small power domain (ESD.CDM.C.5g^{U})	--	--	500um (0.1ohm/0.5ohm)	410um (0.08ohm/0.4ohm)
	Cross domain power clamp/2nd ESD requirement (ESD.CDM.X.1g^{U})	Nice to have (not checked)	Nice to have (not checked)	Needed	Needed

CDM 6A/7A/9A ESD guidelines

- Controlled by switch “CDM6A” / “CDM7A” / “CDM9A” (turn off by default)

		CDM 5A (FWHM < 1ns)	CDM 6A (FWHM < 1ns)	CDM 7A (FWHM < 1ns)	CDM 9A (FWHM < 1ns)
HiCDM P2P Rule	Rbus between IOPAD and primary ESD (ESD.CDM.P.1g^{U})	0.1ohm	0.05ohm	0.07ohm	0.05ohm
	R0 in ESD.CDM.P.1gU (ESD.CDM.P.1.0g^{U})	3ohm	2.5ohm	2.1ohm	1.6ohm
	Rbus between P/G bump and primary ESD (ESD.CDM.P.1.1g^{U})	1ohm	1ohm	0.7ohm	0.5ohm
	Rbus at the middle net of stacked primary ESD diode (ESD.CDM.P.1.2g^{U})	0.1ohm	0.1ohm	0.07ohm	0.05ohm
	Rbus between primary ESD and power clamp (ESD.CDM.P.2^{U})	0.3ohm	0.15ohm	0.2ohm	0.17ohm
	Rbus between primary ESD and reverse diode (ESD.CDM.P.2.1^{U})	0.3ohm	0.15ohm	0.2ohm	0.17ohm
	Rbus between P/G bump and core power clamp (ESD.CDM.P.3g^{U})	0.1ohm	0.1ohm	0.07ohm	0.05ohm
	Rbus between P/G bump and IO power clamp (ESD.CDM.P.4g^{U})	0.2ohm	0.2ohm	0.14ohm	0.1ohm
	Rbus between P/G bump and cascoded IO power clamp (ESD.CDM.P.5g^{U})	0.2ohm	0.2ohm	0.14ohm	0.1ohm
	Rbus between P/G bump and reverse diode (ESD.CDM.P.5.1g^{U})	0.2ohm	0.2ohm	0.14ohm	0.1ohm
	Rbus between IO power clamp and IO power clamp (ESD.CDM.P.7g^{U})	2ohm	2ohm	1.4ohm	1ohm
	Rbus between core power clamp and core power clamp on **VDD net** (ESD.CDM.P.7.1.1g^{U})	1ohm	1ohm	1ohm	1ohm
	Rbus between core power clamp and core power clamp on **VSS net** (ESD.CDM.P.7.1.2g^{U})	1ohm	1ohm	0.7ohm	0.5ohm

CDM 6A/7A/9A ESD guidelines

- Controlled by switch “CDM6A” / “CDM7A” / “CDM9A” (turn off by default)

		CDM 5A (FWHM < 1ns)	CDM 6A (FWHM < 1ns)	CDM 7A (FWHM < 1ns)	CDM 9A (FWHM < 1ns)
HiCDM P2P Rule	Rbus between cascoded IO power clamp and cascoded IO power clamp (ESD.CDM.P.7.2g^{U})	2ohm	2ohm	1.4ohm	1ohm
	Rbus between IO power clamp and cascoded IO power clamp (ESD.CDM.P.7.3g^{U})	2ohm	2ohm	1.4ohm	1ohm
	Rbus between IO power clamp and core power clamp (ESD.CDM.P.7.4g^{U})	1ohm	1ohm	0.7ohm	0.5ohm
	Rbus between core power clamp and cascoded IO power clamp (ESD.CDM.P.7.5g^{U})	1ohm	1ohm	0.7ohm	0.5ohm
	Rbus between B2B diode and ground bumps (ESD.CDM.P.8g^{U})	0.3ohm	0.3ohm	0.2ohm	0.17ohm
	Rbus between B2B diode and power clamp (ESD.CDM.P.9g^{U})	0.3ohm	0.3ohm	0.2ohm	0.17ohm
	Rbus of guard rings for internal circuits ESD isolation purpose (ESD.CDM.P.10g^{U})	10ohm	10ohm	10ohm	10ohm
XDM P2P Rule	Rbus between B2B diode and local power clamp of cross domain interface on both ground nets (ESD.XDM.P.1g^{U})	--	--	0.17ohm	0.12ohm
LC P2P Rule	Rbus between IOPAD and primary ESD on LC pin (ESD.LCP2P.P.1g^{U})	0.1ohm	0.05ohm	0.07ohm	0.05ohm
	Rbus between power clamp and primary ESD on LC pin (ESD.LCP2P.P.2g^{U})	0.1ohm	0.05ohm	0.07ohm	0.05ohm

CDM 6A/7A/9A ESD guidelines

- Controlled by switch “CDM6A” / “CDM7A” / “CDM9A” (turn off by default)

		CDM 5A (FWHM < 1ns)	CDM 6A (FWHM < 1ns)	CDM 7A (FWHM < 1ns)	CDM 9A (FWHM < 1ns)
Full Path P2P Rules	Full path resistance from power (ground) bus of ESD dual diode, through core power clamp to ground (power) bump (ESD.DISTP2P.1g^{U})	1.20ohm	0.95ohm	0.78ohm	0.63ohm
	R0 in ESD.DISTP2P.1gU (ESD.DISTP2P.1.0g^{U})	3ohm	2.5ohm	2.1ohm	1.6ohm
	Full path resistance from power (ground) bus of ESD dual diode, through I/O power clamp to ground (power) bump (ESD.DISTP2P.1.1g^{U})	1.40ohm	1.15ohm	0.94ohm	0.74ohm
	R0 in ESD.DISTP2P.1.1gU (ESD.DISTP2P.1.1.0g^{U})	3ohm	2.5ohm	2.1ohm	1.6ohm
	Full path resistance from power (ground) bus of LC ESD dual diode, through core power clamp to ground (power) bump (ESD.DISTP2P.1.2g^{U})	1.00ohm	0.74ohm	0.65ohm	0.56ohm
	R0 in ESD.DISTP2P.1.2gU (ESD.DISTP2P.1.2.0g^{U})	3ohm	2.5ohm	2.1ohm	1.6ohm
	Full path resistance from power (ground) bus of LC ESD dual diode, through I/O power clamp to ground (power) bump (ESD.DISTP2P.1.3g^{U})	1.20ohm	0.95ohm	0.81ohm	0.67ohm
	R0 in ESD.DISTP2P.1.3gU (ESD.DISTP2P.1.3.0g^{U})	3ohm	2.5ohm	2.1ohm	1.6ohm

		CDM 5A (FWHM < 1ns)	CDM 6A (FWHM < 1ns)	CDM 7A (FWHM < 1ns)	CDM 9A (FWHM < 1ns)
Backend Current Density	ESD CD for primary ESD discharge path (ESD.CD.1g^{U})	1.3A	1.6A	1.8A	2.4A
	ESD CD for secondary ESD discharge path (ESD.CD.2g^{U})	0.012A	0.016A	0.022A	0.030A