Unleash Innovation

N03 ESD/LUP PERC Userguide

DRC, DMKD, DTP

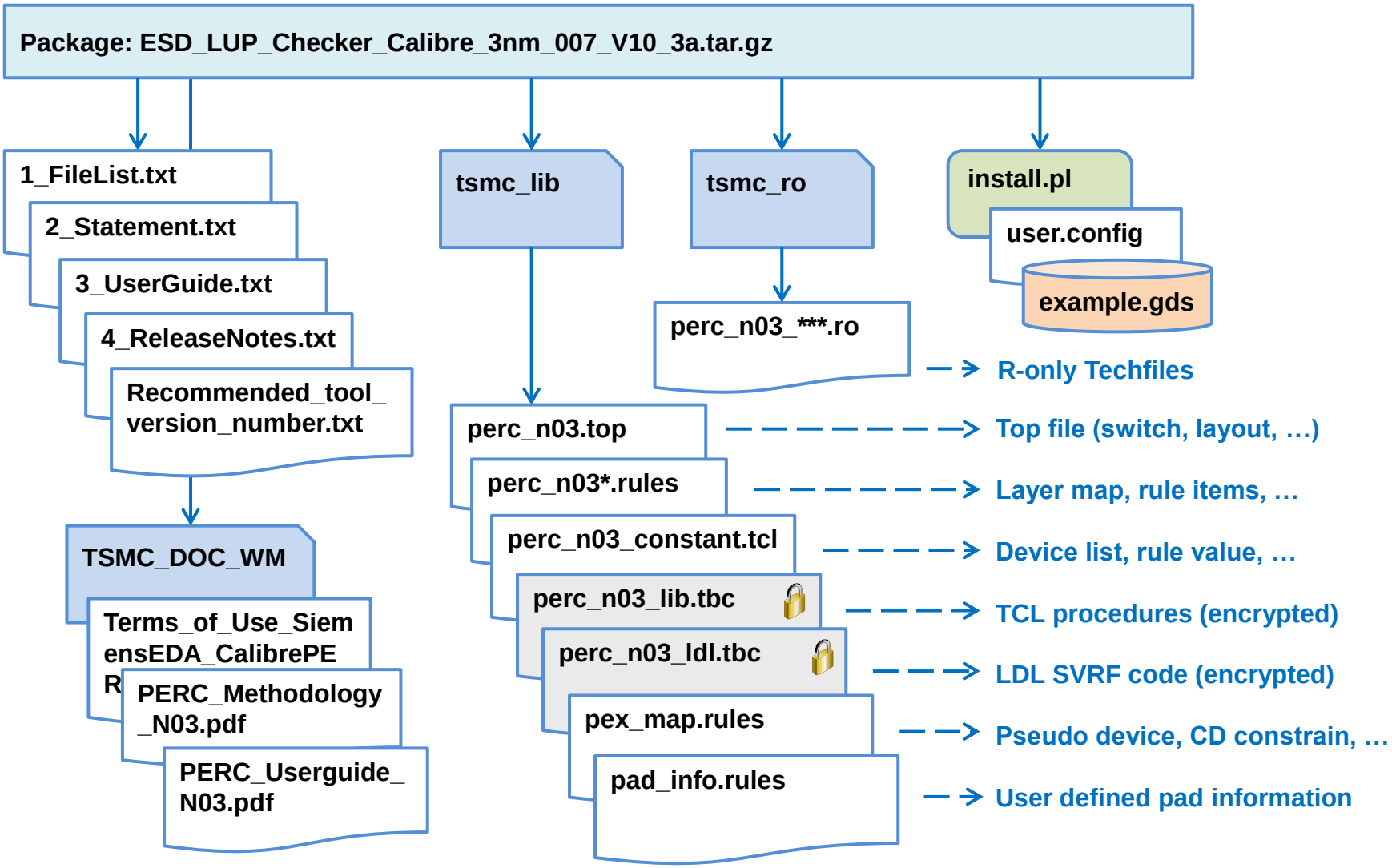
PERC Userguide Outline

- PERC Introduction
- PERC Package Structure
- PERC Installation
- PERC Execution
  - Set Top File
  - Variables for PAD Recognition
  - Set PAD Voltage & PAD Text
  - Switch / Variable Usage
  - Select Check Rules
- PERC Result Review

PERC Introduction

- **PERC is mainly used to check ESD and Latch-up rules, and constructed of following four categories:**
  - **Topology (Circuit Connection and Device Size)**
    - **Check ESD protection scheme: ESD.NET.1g^{U}~ESD.47 g^{U}, ...**
  - **LDL (Logic-Driven-Layout DRC)**
    - **Check Latch-up rules: LUP.2.1U~LUP.9U, ...**
  - **CD (Current Density)**
    - **Check primary ESD discharge path: ESD.CD.1gU, ...**
    - **Check secondary ESD discharge path: ESD.CD.2gU, ...**
  - **P2P (Point-to-Point Resistance)**
    - **Check I/O to power-clamp path: ESD.14.3gU, ...**
    - **Check power to ground path: ESD.14.4gU, ...**

PERC Package Structure



PERC Installation

- 1. Download LVS deck from TSMC on-line
- 2. Edit User Configuration File: ”user.config”

```
# absolute path to install PERC deck
INSTALLATION_PATH = /home/user/perc_n03_deck

# path of TSMC formal released LVS package or file without modification (either one is ok)
# note: please use the same LVS version as '4_ReleaseNotes.txt' to prevent from unexpected result
LVS_PACKAGE_DIRECTORY = T-N03-CL-SP-005-C1/1.0b
#LVS_FILE = DFM_LVS_RC_CALIBRE_N3_1p18M_1X1Xb1Xc1Xd1Ya1Yb5Y2Yy2Yx1R1U_CURDL.1.0b
#MAP_FILE = xact_mapping_1p18M_1X1Xb1Xc1Xd1Ya1Yb5Y2Yy2Yx1R1U

# metal Scheme
METAL_SCHEME = 1P18M_1X1Xb1Xc1Xd1Ya1Yb5Y2Yy2Yx1R1U_SHPMIM1_UT-CURDL
```

- 3. Execute: %> perl install.pl user.config

PERC Execution

- 1. Copy top file “perc_n03_<metal_scheme>.top” from installation path to work directory.
- 2. Refer to below pages to edit the top file
- 3. Run PERC
  - For Pure Topology (only TOPO switch is on):
    - %> calibre -perc -hier -turbo -hyper perc_n03_<metal_scheme>.top
    - Result database is svdb
  - For LDL / CD / P2P (any of LDL / CD / P2P switch is on):
    - %> calibre -perc -ldl -hier -turbo -hyper -ys_hyper perc_n03_<metal_scheme>.top
    - Result database is dfmdb

Set Top File

- **1. Set switches**

perc_n03.top

```
#DEFINE TOPO     // Turn on to enable Topology checks
#DEFINE LDL      // Turn on to enable LDL(Logic-Driven-Layout) PERC checks
//#DEFINE CD     // Turn on to enable CD(Current Density) checks
//#DEFINE P2P    // Turn on to enable P2P(Point-to-Point) checks

// ** Note: CD & P2P cannot be enabled at the same time **

//#DEFINE CD_PRE_CHECK          // Turn on to check the existence of CD path

//#DEFINE P2P_PRE_CHECK         // Turn on to check the existence of P2P path

#DEFINE Hi_CDM                  // Turn on to check Hi-CDM rules for Hi-CDM design

#DEFINE IN_DIE_MODE             // Turn off to disable In-Die Mode during R extraction to improve runtime
                                // Please note: accuracy will be impacted when this switch is disabled

#DEFINE GROUP_PWR_CLAMP         // Turn off to short all Power-clamp for ESD.CD.1gU:pc, ESD.14.4gU, and ESD.
                                // Turn on to check each Power-clamp group separately

//#DEFINE SET_PWR_CLAMP_RON     // Turn on to set Power-clamp Ron for Full Path CD/P2P check, to improve acc

//#DEFINE CHECK_FULL_PATH_CD    // Turn off for Default CD checks: (recommended for big size chip)
                                //   1. I/O Pad to primary ESD device
                                //   2. R-ESD to secondary ESD device
```

Define Check Flow (refer to "PERC Introduction" section)

Set Switches (refer to "Switch Usage" section)

Set Top File (Cont.)

- **2. Set input information**

perc_n03.top

```
LAYOUT SYSTEM GDSII     // set SPICE for CDL(netlist) check
LAYOUT PATH "GDSFILENAME"
LAYOUT PRIMARY "TOPCELLNAME"

PERC NETLIST LAYOUT

#IFDEF CHECK_PICK_UP_P2P
LAYOUT SYSTEM2 GDSII
LAYOUT PATH2 "RUN_LDL/TSMC.ESD.MARK.gds"  // ESD Marker GDS generated in LDL run
LAYOUT PRIMARY2 "TOPCELLNAME"
LAYOUT BUMP2 1000
TEXT DEPTH 1    // set target TEXT DEPTH + 1
PORT DEPTH 1    // set target PORT DEPTH + 1
#ELSE
TEXT DEPTH 0
PORT DEPTH 0
#ENDIF

VIRTUAL CONNECT NAME "?"
//VARIABLE GLOBAL_ESD_BUS ""    // define global ESD bus
//VARIABLE LC_PAD_NAME ""   // define LC PAD names
//VARIABLE VIRTUAL_POWER_NAME ""    // define virtual power names for LDL checks
VARIABLE SIGNAL_NAME "?"    // define signal names, "?" matches all top port names
VARIABLE POWER_NAME  "?VDD?" "?vdd?" "?PWR?" "?pwr?"    // define power names
VARIABLE GROUND_NAME "?VSS?" "?vss?" "?GND?" "?gnd?"    // define ground names

INCLUDE "<INSTALLATION_PATH>/<METAL_SCHEME>/pad_info.rules"  // define pad voltage & pad text
```

Set Input Layout/Netlist

Set ESD Marker (optional)

Set Text Depth

Set Signal/Power/Ground Names

Set PAD Voltage & Text

(refer to next page)

Set PAD Voltage & PAD Text

- **PAD Voltage** is required for **Topology/LDL** checks
- **PAD Text** is required when **no pin-text** on input layout

pad_info.rules

```
// ====================================
// =  Defined PAD Voltage Here        =
// ====================================
// Syntax:
//   VARIABLE "VOL_<pad-text-name>" <pad-voltage>      // first priority
//   VARIABLE "<pad-text-name>" <pad-voltage>          // second priority
//
// Example:
//   VARIABLE "VDD"      2.5    // set VDD net as 2.5v
//   VARIABLE "VSS"      0.0    // set VSS net as 0.0v
//   VARIABLE "INPUT1"   1.8    // set INPUT1 net as 1.8v
//   VARIABLE "INPUT2"   1.0    // set INPUT2 net as 1.0v
//   VARIABLE "VOL_CLK"  2.0    // set CLK net as 2.0v when VARIABLE "CLK" is used for other purpose

// ====================================
// =  Defined PAD Text Here           =
// ====================================
// Syntax:
//   LAYOUT TEXT "<pad-text-name>" <x-coordinate> <y-coordinate> <pin-text-layer>
//
// Example:
//   LAYOUT TEXT "VDD"    50  100 AP_text  // create AP pin-text named VDD at (50,100)
//   LAYOUT TEXT "VSS"    50  0   AP_text  // create AP pin-text named VSS at (50,0)
//   LAYOUT TEXT "INPUT1" 100 100 M7_text  // create M7 pin-text named INPUT1 at (100,100)
//   LAYOUT TEXT "INPUT2" 100 0   M7_text  // create M7 pin-text named INPUT2 at (100,0)
```

Set Variable for Net Type Definition

Net Type	Variable Names	Definition
Power	POWER_NAME	power names
	- D2D_INT_CDM05V0D040A_POWER_NAME - D2D_INT_CDM35V0D220A_POWER_NAME	die-to-die interface power names (D2D_VDD)
Ground	GROUND_NAME	ground names
	- GLOBAL_ESD_BUS	global ESD bus
Signal	SIGNAL_NAME	signal names
	- LC_PAD_NAME	low capacitance PAD names
	- PoP_PAD_NAME	package-on-package IO PAD names
	- ULTRA_LOW_NOISE_PAD_NAME	ultra-low noise IO PAD names
Virtual Power	VIRTUAL_POWER_NAME	virtual power names for LDL checks
D2D Interface	D2D_INT_CDM05V0D040A_NAME D2D_INT_CDM35V0D220A_NAME	die-to-die CDM customized interface names

1. **The variable with preceding "-" is a subtype of previous variable. (e.g. LC_PAD_NAME is subtype of SIGNAL_NAME)**
2. **A net assigned in subtype needs to be assigned in the main Net Type as well. (e.g. a net assigned in LC_PAD_NAME needs to be assigned in SIGNAL_NAME also)**
3. **A net cannot be assigned to different Net Type at the same time. (e.g. a net cannot be assigned in both SIGNAL_NAME and D2D_INT_CDM35V0D220A_NAME). If there is conflict, only one Net Type will be kept; the priority is: Power → Ground → Virtual Power → D2D Interface → Signal**

Switch Usage

- **CD_PRE_CHECK**
  - In CD check, it will check the existence of ESD path first and then export the ESD path for CD simulation.
  - By turn on this switch, the existence of ESD path can be checked in advance with Topology checks.

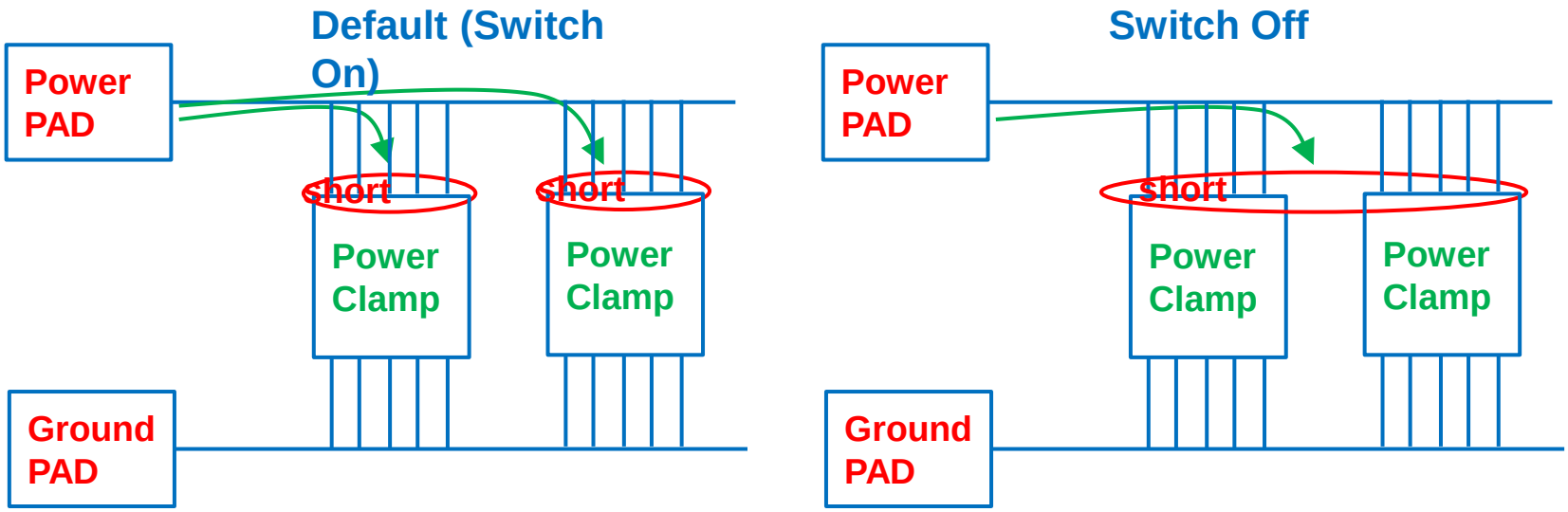
- **P2P_PRE_CHECK**
  - In P2P check, it will check the existence of ESD path first and then export the ESD path for P2P simulation.
  - By turn on this switch, the existence of ESD path can be checked in advance with Topology checks.

Switch Usage (Cont.)

- **CDM_6A/7A/9A**
  - **These switches are to enable CDM-6A/7A/9A relative rule checks.**
- **Hi_CDM**
  - **This switch is to enable Hi-CDM relative rule checks.**
- **IN_DIE_MODE**
  - **By default, this switch is enabled to take indie variation (widths, thicknesses, etc) into consideration during R extraction**
  - **If user suffer long runtime issue in IP level design, turning off this switch may help to improve the runtime, however the accuracy will degrade.**

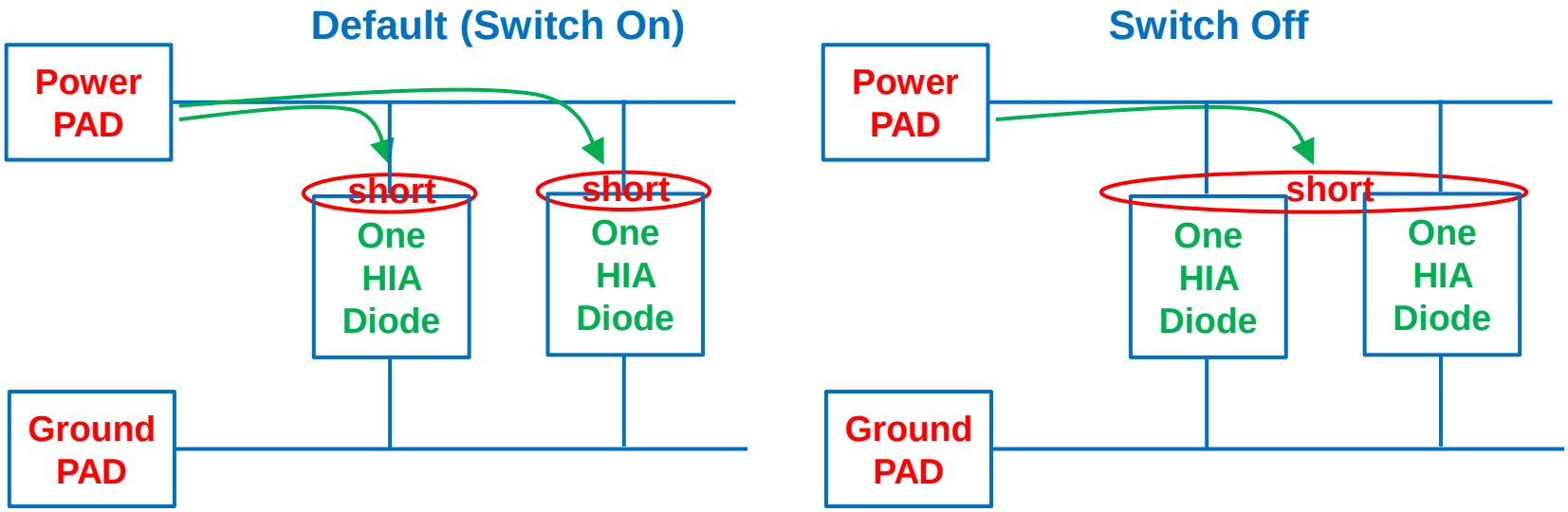
Switch Usage (Cont.)

- **GROUP_PWR_CLAMP**
  - **This switch is to control following rule checks:**
    - **ESD.CD.1gU:pc, ESD.14.4gU, and ESD.CDM.P.3~5gU**
  - **By default, Power-Clamps will be grouped by location and checked separately.**
  - **By turn off this switch, all Power-Clamps will be shorted.**



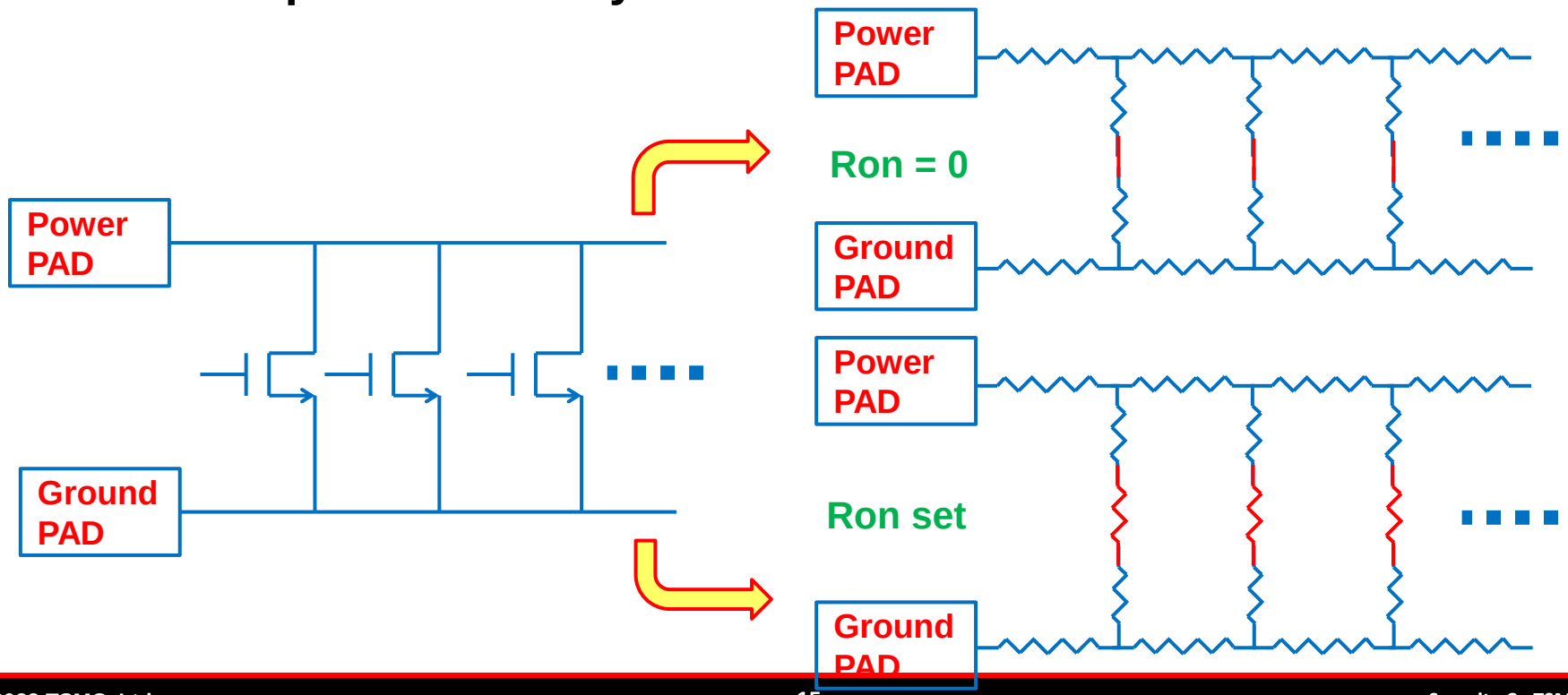
Switch Usage (Cont.)

- **GROUP_HIA_DIODE**
  - This switch is to control following rule checks:
    - ESD.CD.1.1gU, and ESD.CDM.P.5.1gU
  - By default, one reverse HIA diode between POWER and GROUND will be grouped by LVS device formation and checked separately.
  - By turn off this switch, all reverse HIA diodes between POWER and GROUND will be shorted.



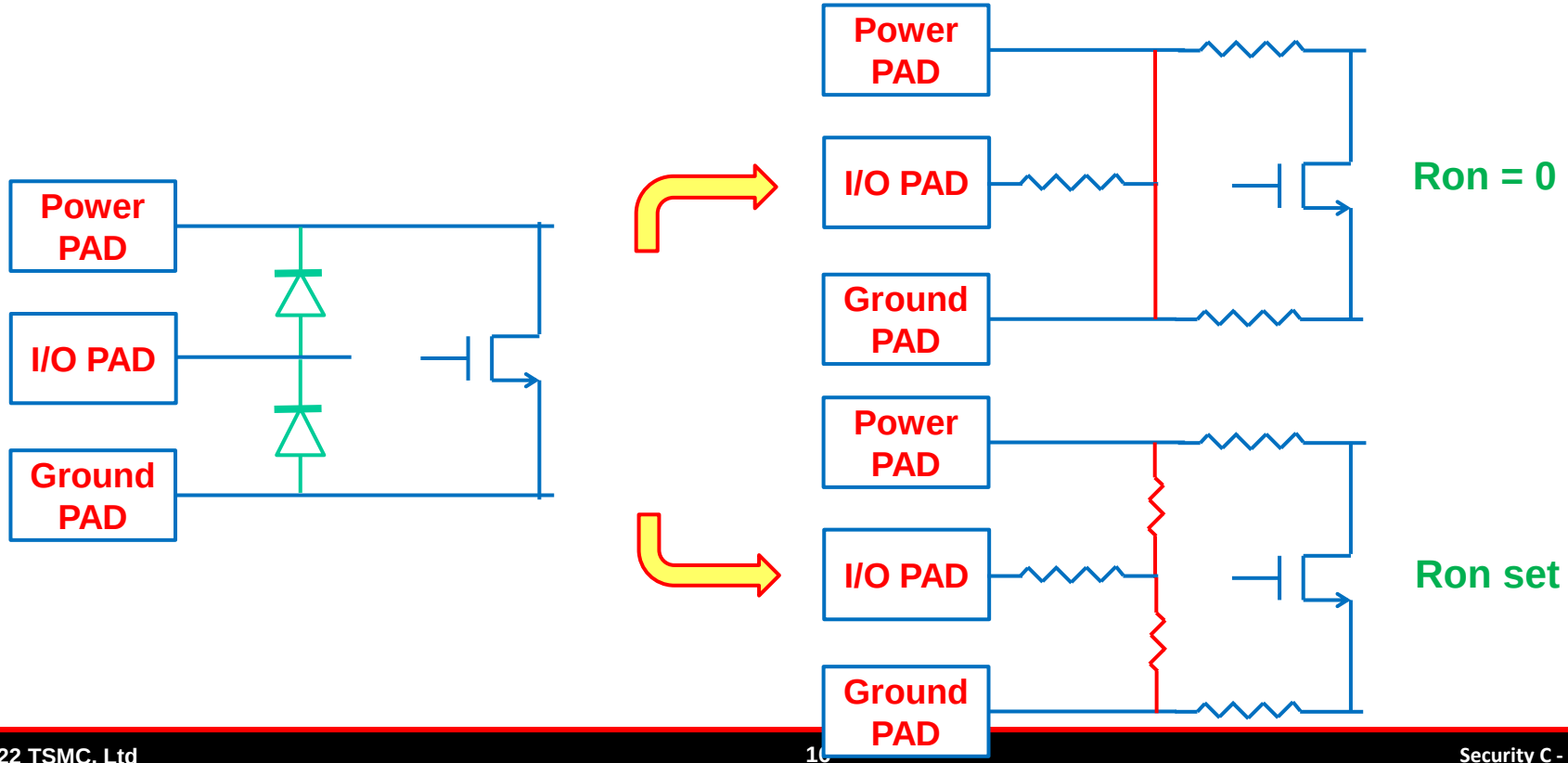
Switch Usage (Cont.)

- **SET_PWR_CLAMP_RON**
  - **By default, Power-Clamp Ron is set to 0 for Full Path CD/P2P checks.**
  - **By turn on this switch, Power-Clamp Ron will be set to improve accuracy.**



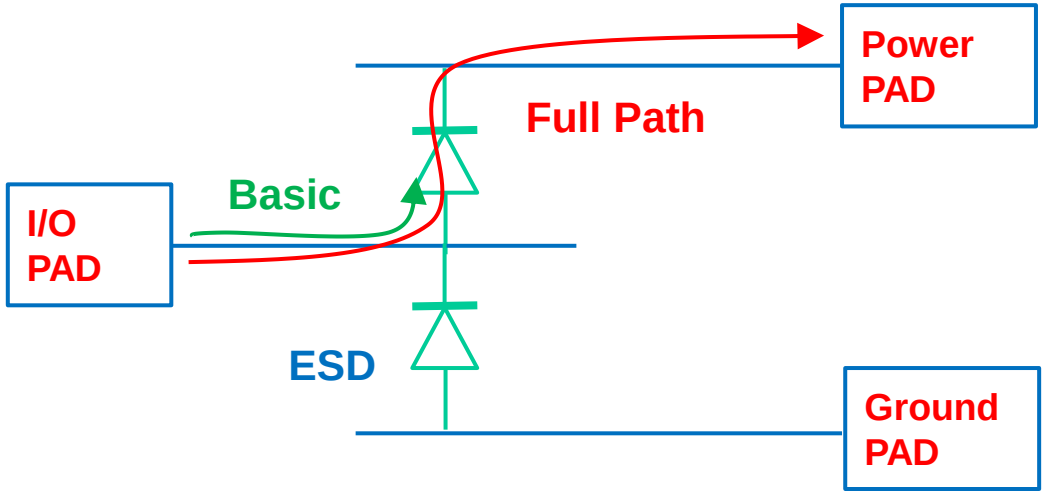
Switch Usage (Cont.)

- **SET_DIODE_RON**
  - **By default, primary ESD diode Ron will be calculated to improve accuracy for Full Path CD/P2P checks.**
  - **By turn off this switch, diode Ron is set to 0.**



Switch Usage (Cont.)

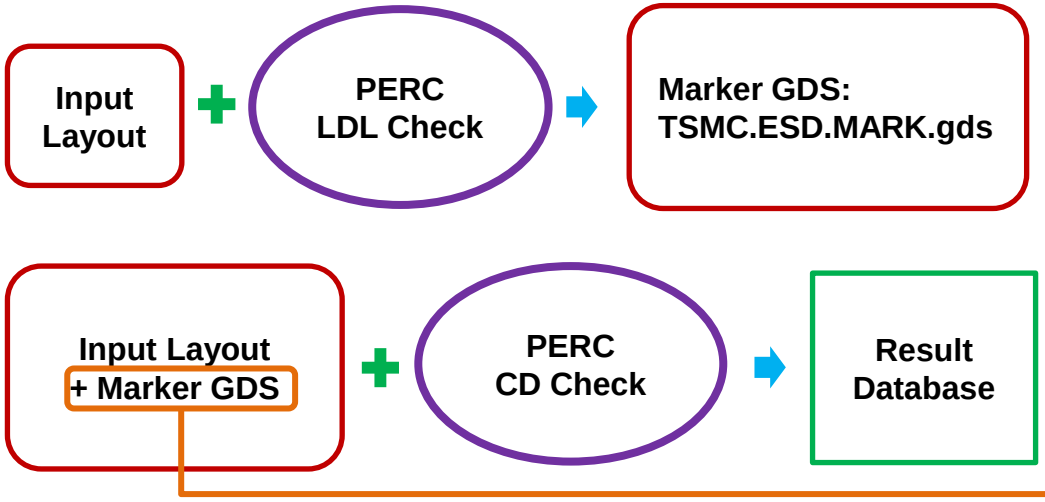
- **CHECK_FULL_PATH_CD**
  - **This switch is to control Current Density (CD) check path.**
  - **By default, it is enabled to check full path CD from I/O PAD to Power/Ground PAD**
  - **When full path CD cannot be done in chip level design, this switch can be disabled to check basic CD from I/O PAD to ESD device only.**



Switch Usage (Cont.)

- **CHECK_SCR_PATH_CD**
  - This switch is to control ESD.CD.3.1~4gU checks.
  - Before turn on this switch, please:
    1. Run LDL check to get ESD Marker GDS: TSMC.ESD.MARK.gds
    2. Complete relative settings, i.e. Marker GDS Path, top-cell name, text depth, …

  Note: These checks may have long runtime issue.




```
#IFDEF INCLUDE_LDL_MARKER
LAYOUT SYSTEM2 GDSII
LAYOUT PATH2 "RUN_LDL/TSMC.ESD.MARK.gds"
LAYOUT PRIMARY2 "TOPCELLNAME"
LAYOUT BUMP2 1000
TEXT DEPTH 1    // set target TEXT DEPTH + 1
PORT DEPTH 1    // set target PORT DEPTH + 1
#ELSE
TEXT DEPTH 0
PORT DEPTH 0
#ENDIF
```

Switch Usage (Cont.)

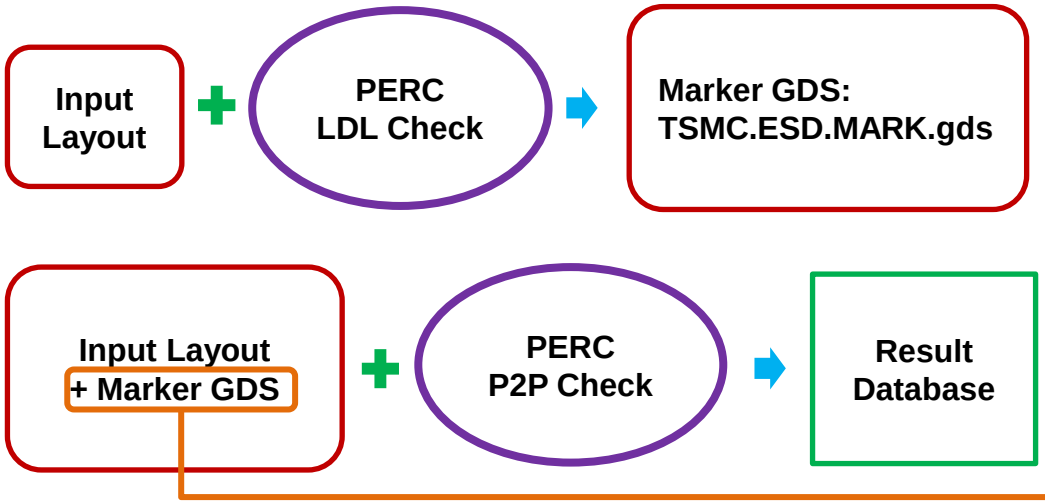
- **CHECK_FULL_PATH_P2P**
  - **This switch is to control following checks:**
    - **ESD.DISTP2P.1gU, ESD.DISTP2P.1.1gU, ESD.DISTP2P.1.2gU, ESD.DISTP2P.1.3gU.**
    - **These checks involve both power and ground nets**
  - **This switch is recommended for Cell/IP level design**

Note: runtime may increase dramatically when this switch is enabled in chip level.

Switch Usage (Cont.)

- **CHECK_PICK_UP_P2P**
  - This switch is to control PAD to Pick-Up Ring/Strap checks.
  - Before turn on this switch, please:
    1. Run LDL check to get ESD Marker GDS: TSMC.ESD.MARK.gds
    2. Complete relative settings, i.e. Marker GDS Path, top-cell name, text depth, …

  Note: These checks may have long runtime issue.




```
#IFDEF INCLUDE_LDL_MARKER
LAYOUT SYSTEM2 GDSII
LAYOUT PATH2 "RUN_LDL/TSMC.ESD.MARK.gds"
LAYOUT PRIMARY2 "TOPCELLNAME"
LAYOUT BUMP2 1000
TEXT DEPTH 1    // set target TEXT DEPTH + 1
PORT DEPTH 1    // set target PORT DEPTH + 1
#ELSE
TEXT DEPTH 0
PORT DEPTH 0
#ENDIF
```

Switch Usage (Cont.)

- **CREATE_PAD_BY_TEXT**
  - For CD/P2P checks, PAD is required to define the current source or sink.
  - When there is not real PAD, the LVS recognized ports will be used instead.
  - If user want to constrain the port on certain layers only, please enable the "CREATE_PAD_BY_TEXT" switch, set following two variables in "user.config", and run install again.
  - In this example, only top hierarchy level pin text on AP and M7 will be used to form pseudo PAD.

user.config

```
PORT_LAYER = AP M7     # port layers with pin-text used to form pseudo pad
TOP_PORT_ONLY = y      # y: use top hierarchy level pin-text only,
                       # n: use all hierarchy level pin-text
```

Switch Usage (Cont.)

- **DISABLE_IODMY**
  - Turn on to disable IODMY recognition.
  - By default, PERC will use {IODMY AND M1} to recognize internal nets as signal in LDL check

- **EXPORT_ONE_VICTIM**
  - By default, all victim devices will be exported for LDL checks
  - By turn on this switch, only one of multiple parallel connected victim devices will be exported for LDL check to reduce runtime and memory usage, but the result may has false or missing error.

Switch Usage (Cont.)

- **COMMON_GROUND**
  - **By default, this switch is disabled for any kind of design.**
  - **For common ground design, user can turn on this switch to disable the rule checks below to improve runtime.**
    - TOPO: ESD.45gu, ESD.45.0.1gu, ESD.CDM.B.2gu, ESD.CDM.X.1gu, and cascoded case in ESD.XDM.VIC.3gu, ESD.XDM.VIC.4gu
    - LDL: ESD.CDM.C.4gu, ESD.CDM.C.4.1gu
    - P2P: ESD.CDM.P.8gu, ESD.CDM.P.9gu, ESD.XDM.P.1gu

Switch Usage (Cont.)

- **CD_GROUP1~4**
  - By default, all switches are enabled to check all CD rules.
  - If user suffers long runtime issue, these switches can be used to split the rules into multiple runs to reduce runtime.

- **P2P_GROUP1~6**
  - By default, all switches are enabled to check all P2P rules.
  - If user suffers long runtime issue, these switches can be used to split the rules into multiple runs to reduce runtime.

Recommended setup for PERC running

- For IP, please run PERC by using “IP level” setup
- For full chip, please run PERC by using “Chip level” setup.

N3 PERC running setup	Topology/LDL check (IP level)	Topology/LDL check (Chip level)	CD check (IP level)	CD check (Chip level)	P2P check (IP level)	P2P check (Chip level)
#DEFINE TOPO	On	On	Off	Off	Off	Off
#DEFINE LDL	On	On	Off	Off	Off	Off
#DEFINE CD	Off	Off	On	On	Off	Off
#DEFINE P2P	Off	Off	Off	Off	On	On
#DEFINE CD_PRE_CHECK	On	On	Off	Off	Off	Off
#DEFINE P2P_PRE_CHECK	On	On	Off	Off	Off	Of
#DEFINE CDM_6A/7A/9A	*(1)	*(1)	*(1)	*(1)	*(1)	*(1)
#DEFINE Hi_CDM	On	On	On	On	On	On
#DEFINE IN_DIE_MODE	---	---	On	On*(2)	On	On*(2)
#DEFINE GROUP_PWR_CLAMP	---	---	On	On	On	On
#DEFINE GROUP_HIA_DIODE	---	---	On	On	On	On
#DEFINE SET_PWR_CLAMP_RON	---	---	On	Off	On	Off
#DEFINE SET_DIODE_RON	---	---	On	On	On	On
#DEFINE CHECK_FULL_PATH_CD	---	---	On	On*(3)	---	---
#DEFINE CHECK_SCR_PATH_CD	---	---	On[a]	Off	---	---
#DEFINE CHECK_FULL_PATH_P2P	---	---	---	---	On	Off
#DEFINE CHECK_PICK_UP_P2P	Off	Off	Off	Off	On[a]	Off
#DEFINE CREATE_PAD_BY_TEXT	Off	Off	Off	Off	Off	Off

*(1): Turn it on to check CDM-6A/7A/9A ESD guidelines.
*(2): If user suffers runtime or hardware issues in Chip level, call for vendor’s help or turn it off to improve runtime w/ taking risk of losing accuracy of R extraction.
*(3): If user suffers runtime or hardware issues in Chip level, call for vendor’s help or turn it off to improve runtime w/ taking risk of potential escapes. In order to minimize the risk of escapes as turning off the switch, please confirm IP level results with all used metal scheme checked by full path CD and P2P.
[a] : Need GDS input (TSMC.ESD.MARK.gds) from LDL results.
--- : Don’t care

Recommended setup for PERC running

Unleash Innovation

- For IP, please run PERC by using “IP level” setup
- For full chip, please run PERC by using “Chip level” setup.

N3 PERC running setup	Topology/LDL check (IP level)	Topology/LDL check (Chip level)	CD check (IP level)	CD check (Chip level)	P2P check (IP level)	P2P check (Chip level)
#DEFINE TOPO	On	On	Off	Off	Off	Off
#DEFINE LDL	On	On	Off	Off	Off	Off
#DEFINE CD	Off	Off	On	On	Off	Off
#DEFINE P2P	Off	Off	Off	Off	On	On
#DEFINE DISABLE_IODMY	*(4)	*(4)	*(4)	*(4)	*(4)	*(4)
#DEFINE EXPORT_ONE_VICTIM	Off	Off*(5)	---	---	---	---
#DEFINE SHOW_XPWR_STACK	On	Off	---	---	---	---
#DEFINE COMMON_GROUND	Off*(6)	Off*(6)	Off*(6)	Off*(6)	Off*(6)	Off*(6)
#DEFINE CD_GROUP1~4	---	---	On*(7)	On*(7)	---	---
#DEFINE P2P_GROUP1~6	---	---	---	---	On*(7)	On*(7)
#DEFINE USE_SUB_PROPERTY	On*(8)	Off	---	---	---	---
#DEFINE ENABLE_R0_CHECK	---	---	---	---	On*(8)	On*(8)

*(4): Turn it on to disable IODMY functionality. (Available only when GDS/OASIS input)

*(5): If user suffers runtime or hardware issues in Chip level, call for vendor’s help or turn it on w/ taking risk of potential false alarms or escapes in LDL check.

*(6): Turn it on for common ground design, which will disable some cross-domain checks (e.g. ESD.45.0gu) and reduce runtime.

*(7): If user suffer long runtime issue, these switches can be used to split the rules into multiple runs to reduce runtime

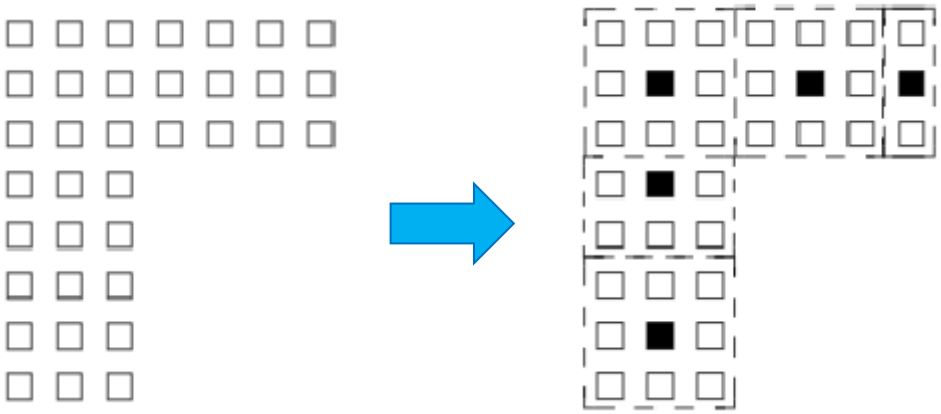
*(8): Suggest to enable it. If user suffers runtime or hardware or license issues, then please turn it off.

a : Need GDS input (TSMC.ESD.MARK.gds) from LDL results.

--- : Don’t care

Variable Usage

- **VIA_REDUCE_STEP [number]**
  - **For Full Chip P2P check, it may take a long time to extra R-network, or even can not finish in a certain period.**
  - **To reduce R-network, tool will replace 3x3 via array by an equivalent single via as shown below.**
  - **To improve runtime, user can try to use a larger number, however the accuracy will be degraded.**



Select Check Rules

- **User can control rule check group by turn on/off following switches defined in "perc_n03.top"**
  - **Note: CD and P2P can not be enabled at the same time**

```
//#DEFINE TOPO  // Turn on to enable Topology checks.
//#DEFINE LDL   // Turn on to enable LDL(Logic-Driven-Layout) DRC checks.
//#DEFINE CD    // Turn on to enable CD(Current Density) checks.
//#DEFINE P2P   // Turn on to enable P2P(Point-to-Point) checks.
```

- **To disable certain rule checks, user can comment out the rules defined in "perc_n03.rules"**

```
PERC LOAD perc_lib INIT input_pad_init SELECT
    ESD.NET.1gu
    ESD.WARN.3gu
    // ESD.8gu
    // ESD.9gu
    ESD.15gu
    ESD.LC.8gu
    ESD.LC.9gu
```

Add "//" to disable ESD.8gu & ESD.9gu

PERC Result Review

- **Open dfmdb or svdb with Calibre RVE:**
  - **%> calibre -rve -perc dfmdb**