GA-970A-D3

Revision : 1.01

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Title: COVER SHEET

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Model Name:GA-970A-D3

Component value change history

Version: 1.01

P-Code: U98094-0

Date	Change Item		Reason
2011.03.10	0.1 9M970AD3-00-01		
2011.03.11	0.1 9M970AD3-00-01A		
2011.05.09	9M970AD3-00-10A	PCB Ver 1.0	
2011.05.10	9M970AD3-00-10B	PCB Ver 1.01	

Circuit or PCB layout change for next version

Date	Change Item	Reason
	0.1	
2011.02.22	Modify from GA-990XA-UD3	
	移除 PCIEx8, 1394, Front USB3	
	增加PCIEx1_3	
	Vcore change 4+1 power pake 6329+6609	
2011.03.11	修改CPU Vcore OCP與RC 電阻值	
	修改超電壓由每格10mV改爲5mV	
2011.03.14	6329 PIN GVOT.PVCC add P-H VCC	
	USB3.0 Fuse 3.0A change 3.5A	
	OPTICAL add 0.1uF(靠近OPTICAL)	
	LAN:8111E LA_VD33 add 0.1uF+4.7uF	
2011.05.09	change M2CPU料號12KRC-04K812-31R_12KRC-04K812-32R]	
	820uF change 560uF	
2011.05.10	cheang ddr dimm文字面順序1.2.3.4->4.2.3.1	

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Title: BOM & PCB HISTORY

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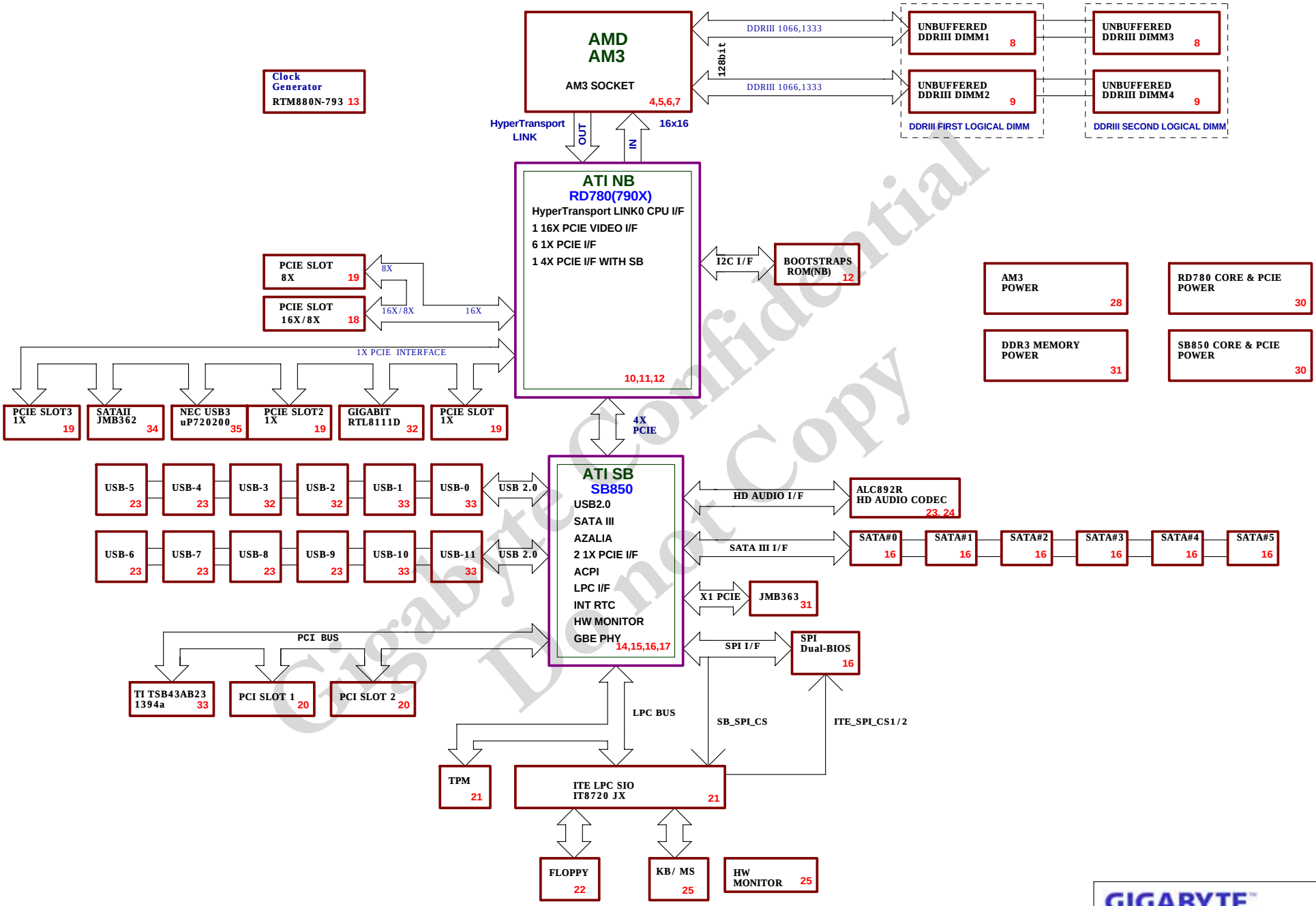

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Title: BLOCK DIAGRAM

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L0_CADIN_L[0..15]
L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15]
L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15]
L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15]
L0_CADOUT_H[0..15] 10

M2CPUA

HYPERTRANSPORT

10 L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 10
10 L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 10
10 L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 10
10 L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 10
10 L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 10
10 L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 10
10 L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 10
10 L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 10
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AE5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AE4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AE1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/942AM3b/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

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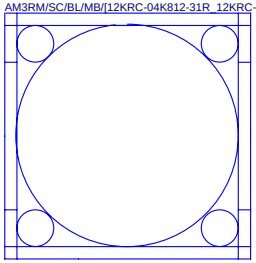
M2CPU
AM3RM/SC/BL/MB/[12KRC-04K812-31R_12KRC-04K812-32R]



COUPON1 COUPON1 1 2 COUPON/X VCC
COUPON2 COUPON2 1 2 COUPON/X

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Title	CPU HYPER TRANSPORT	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
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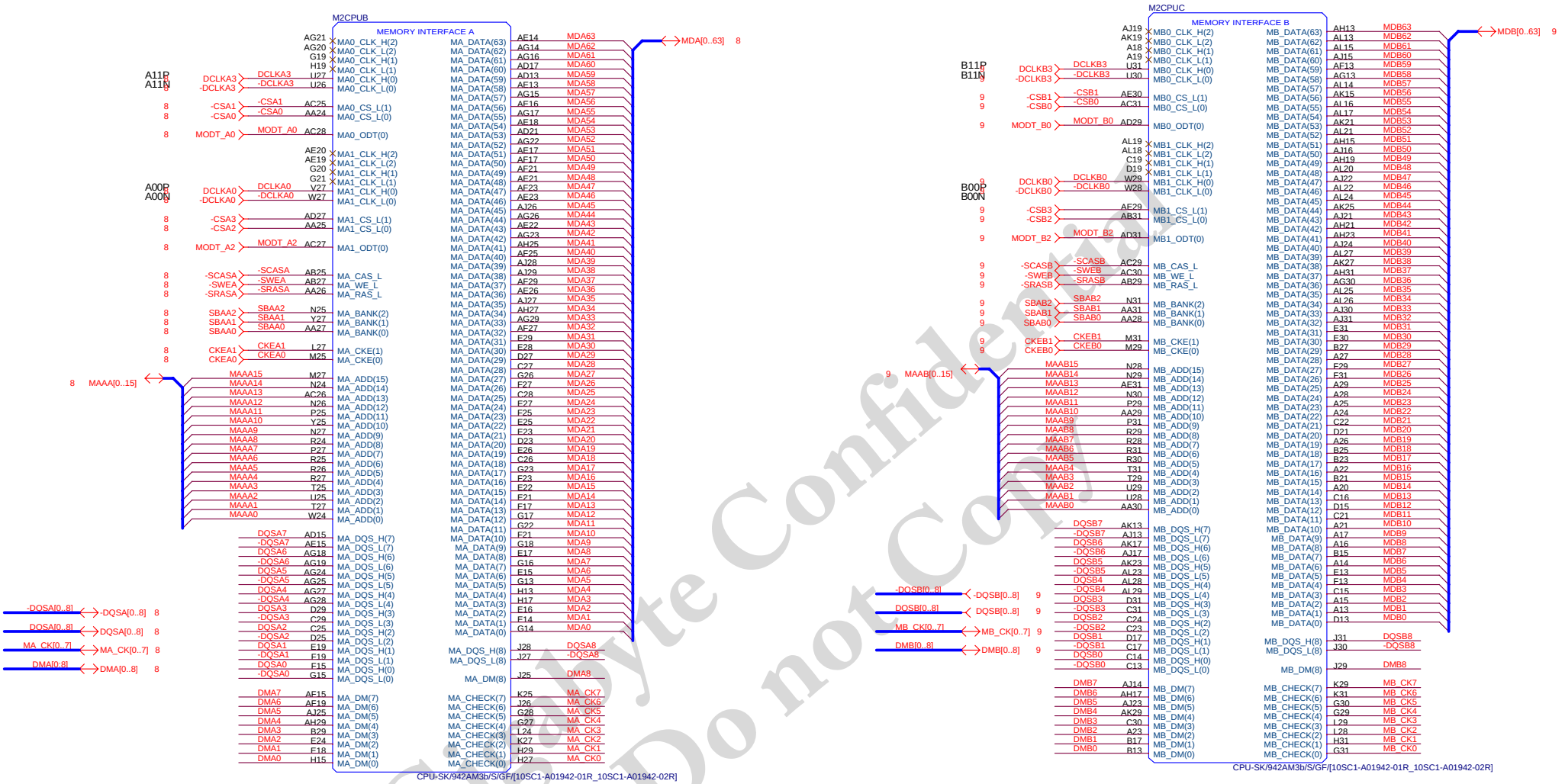

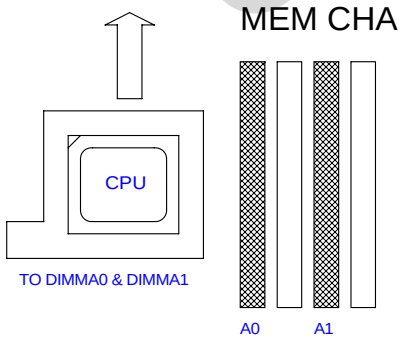

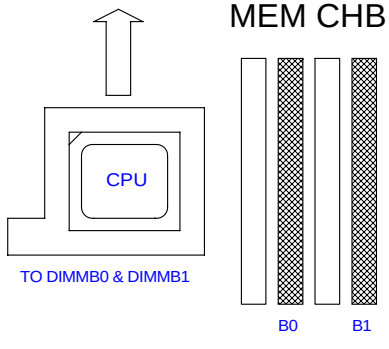

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Title	CPU DDRIII MEMORY	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
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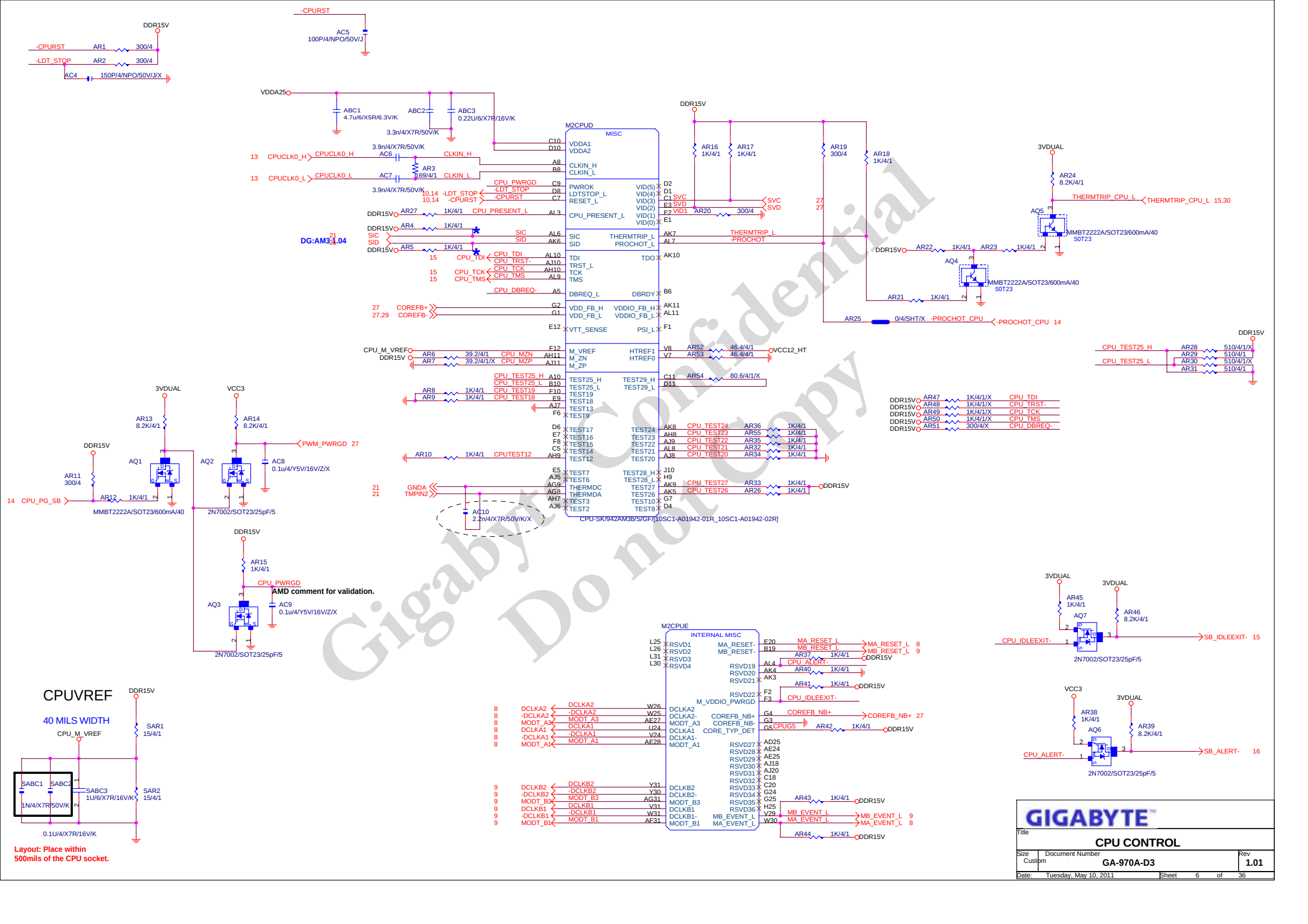

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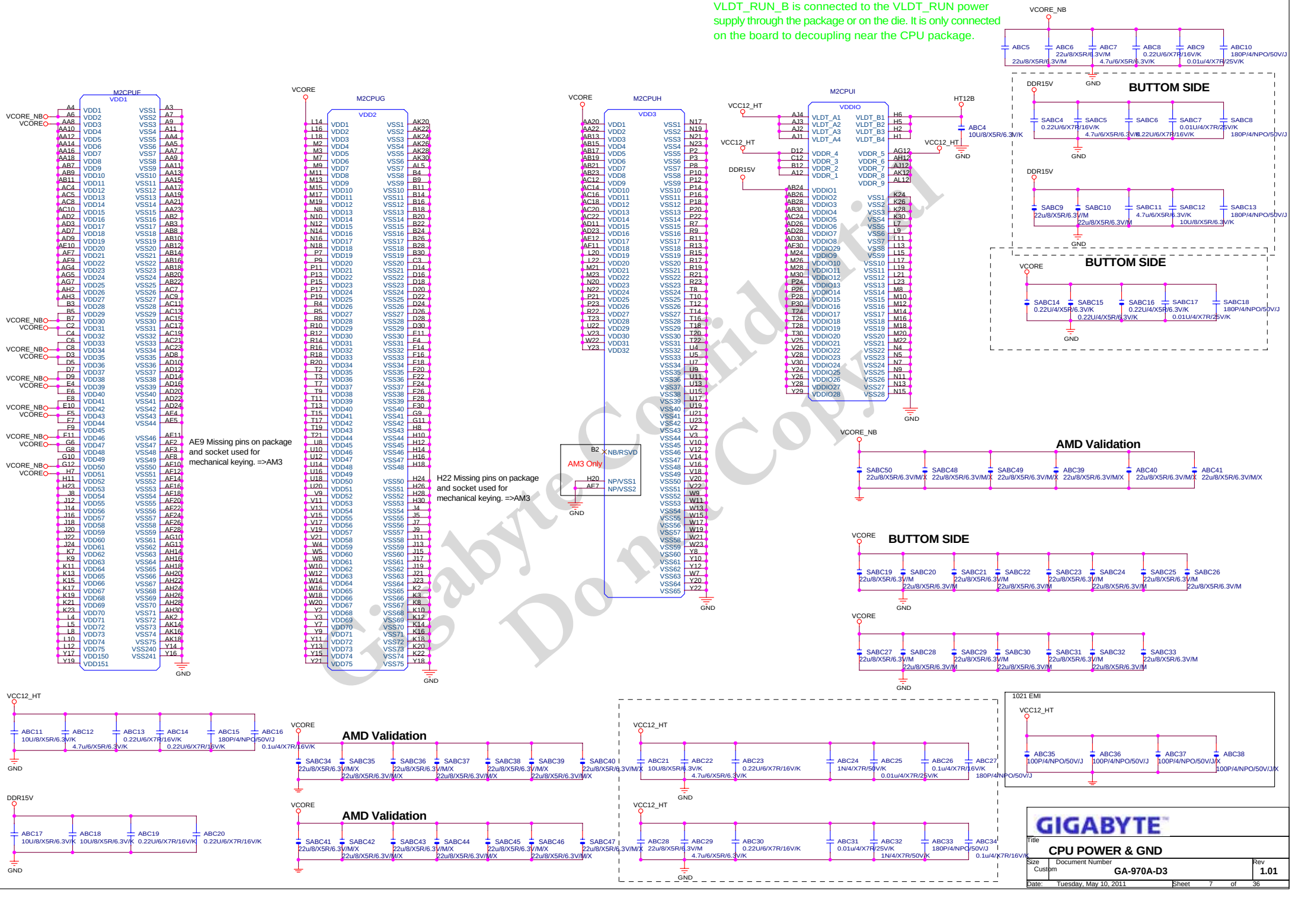
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



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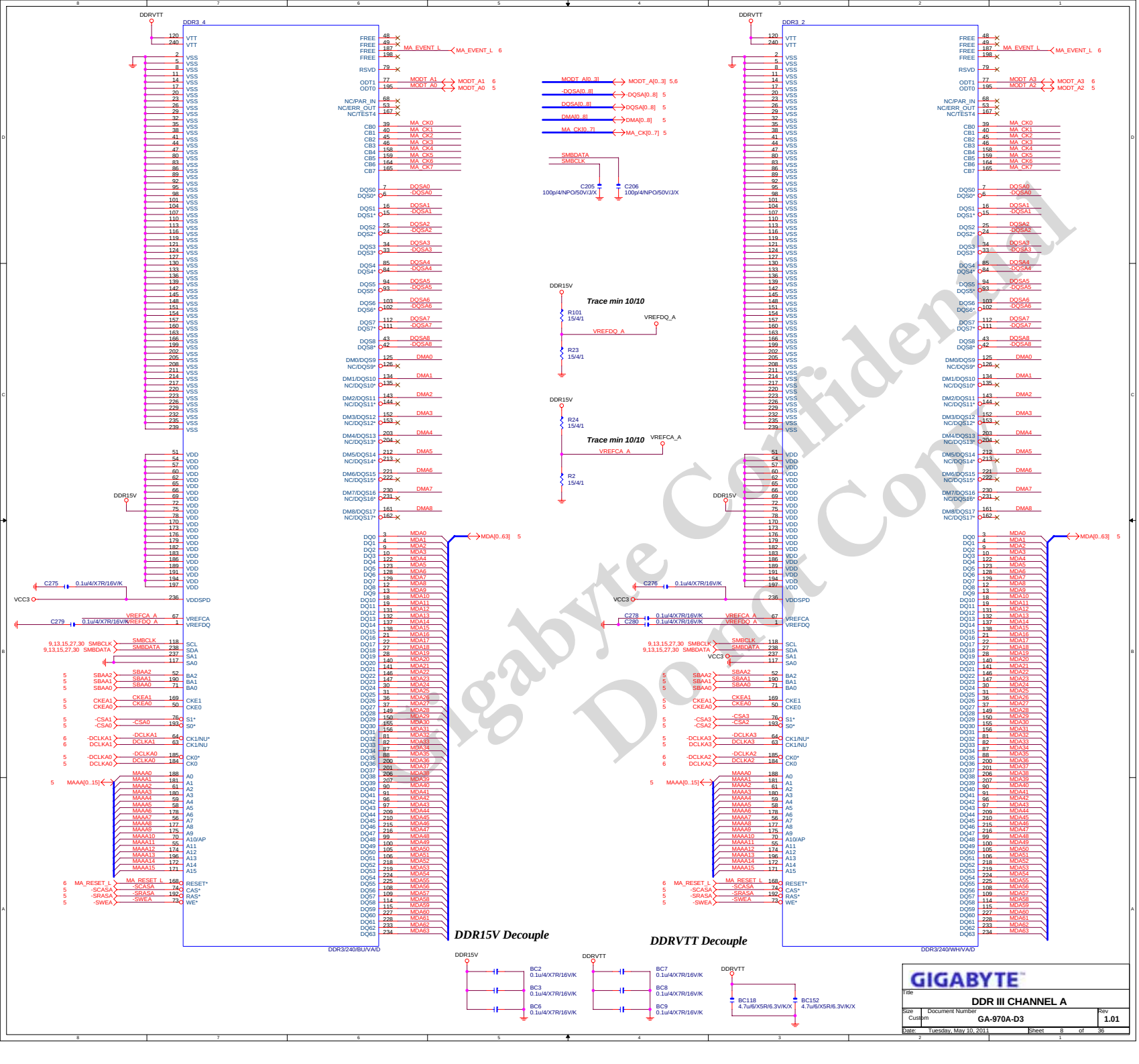

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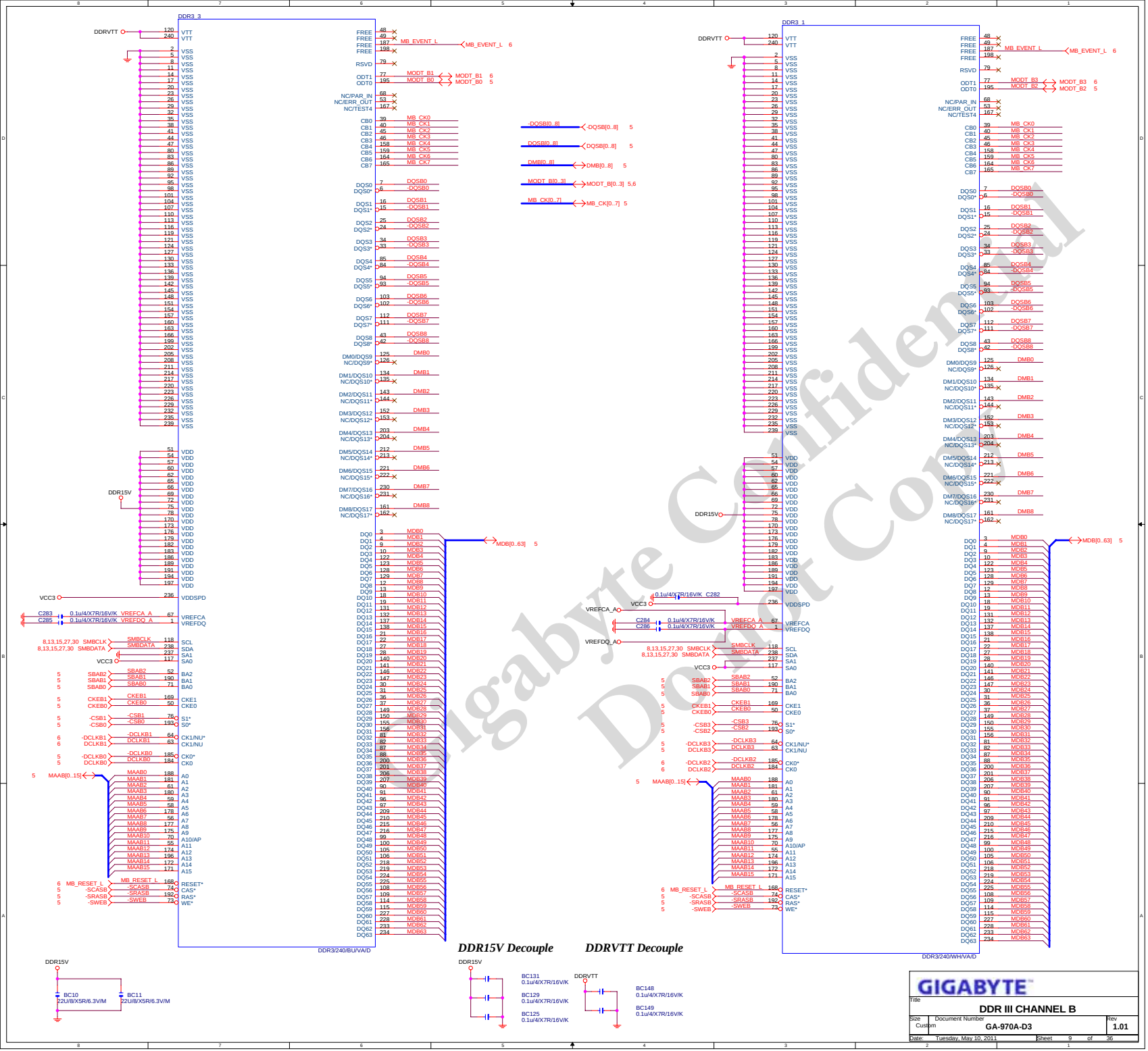
Title	DDR III CHANNEL A	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 8 of 36	



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Title: DDR III CHANNEL B

Size	Document Number	Rev
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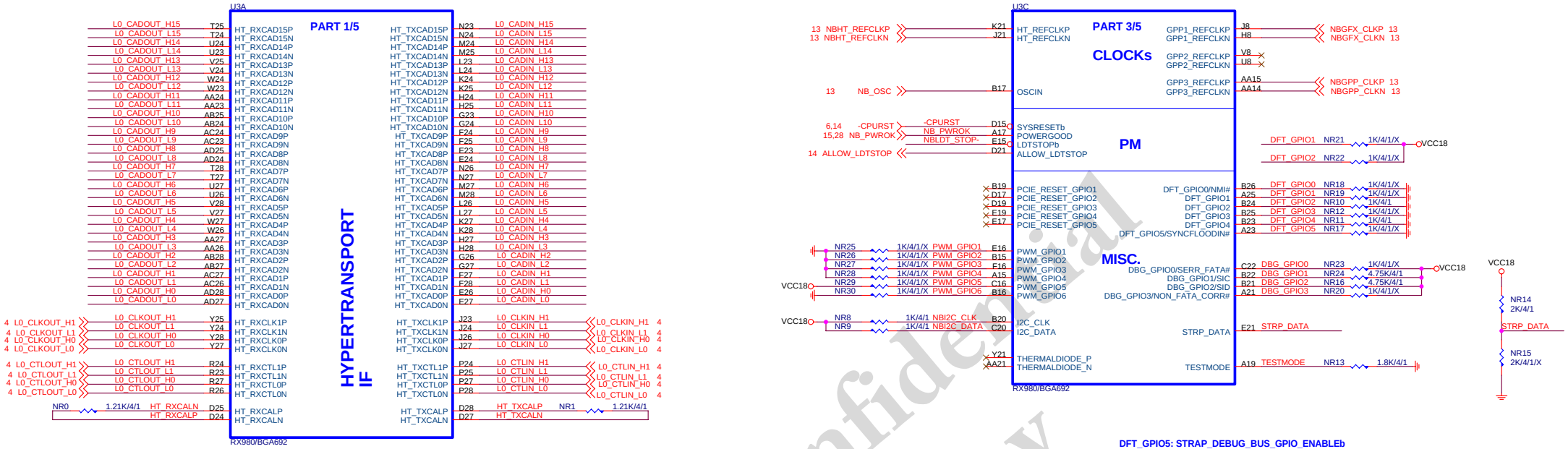

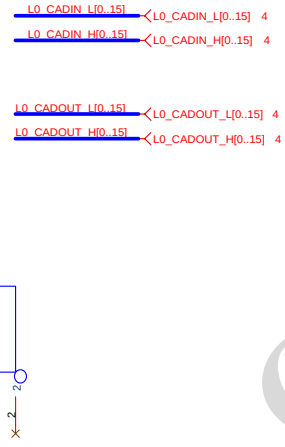

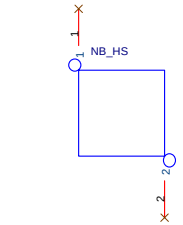

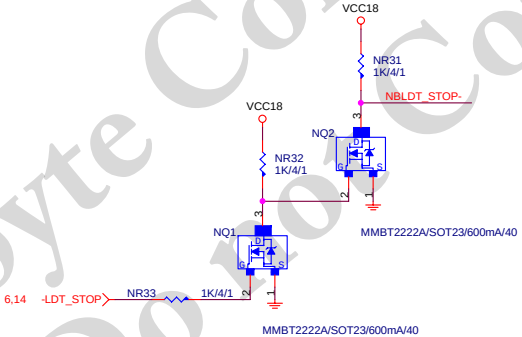

DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101: 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

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Title: RS780 HT-LINK I/F

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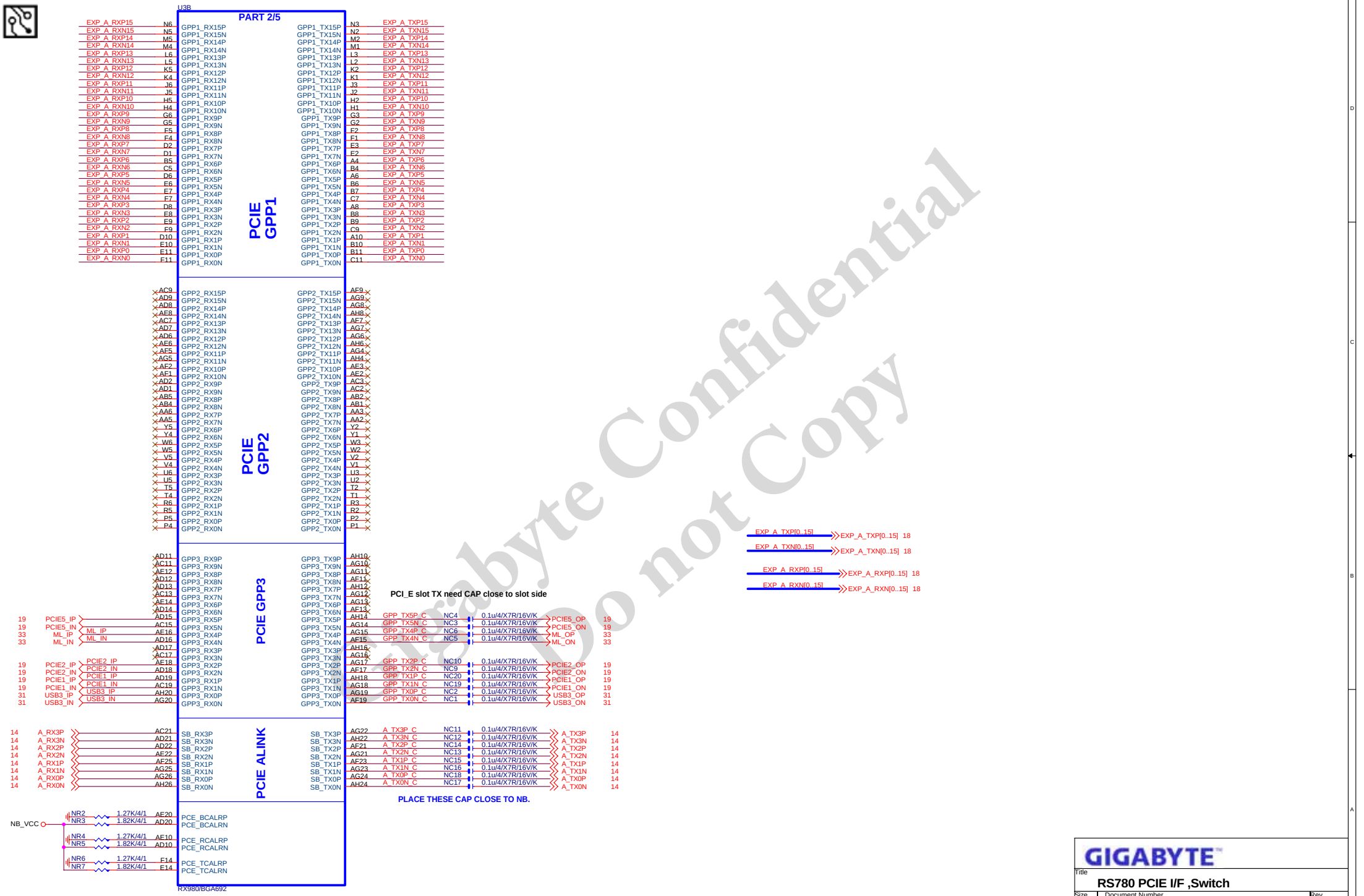

Title	RS780 PCIE I/F ,Switch
Size	Custom
Document Number	GA-970A-D3
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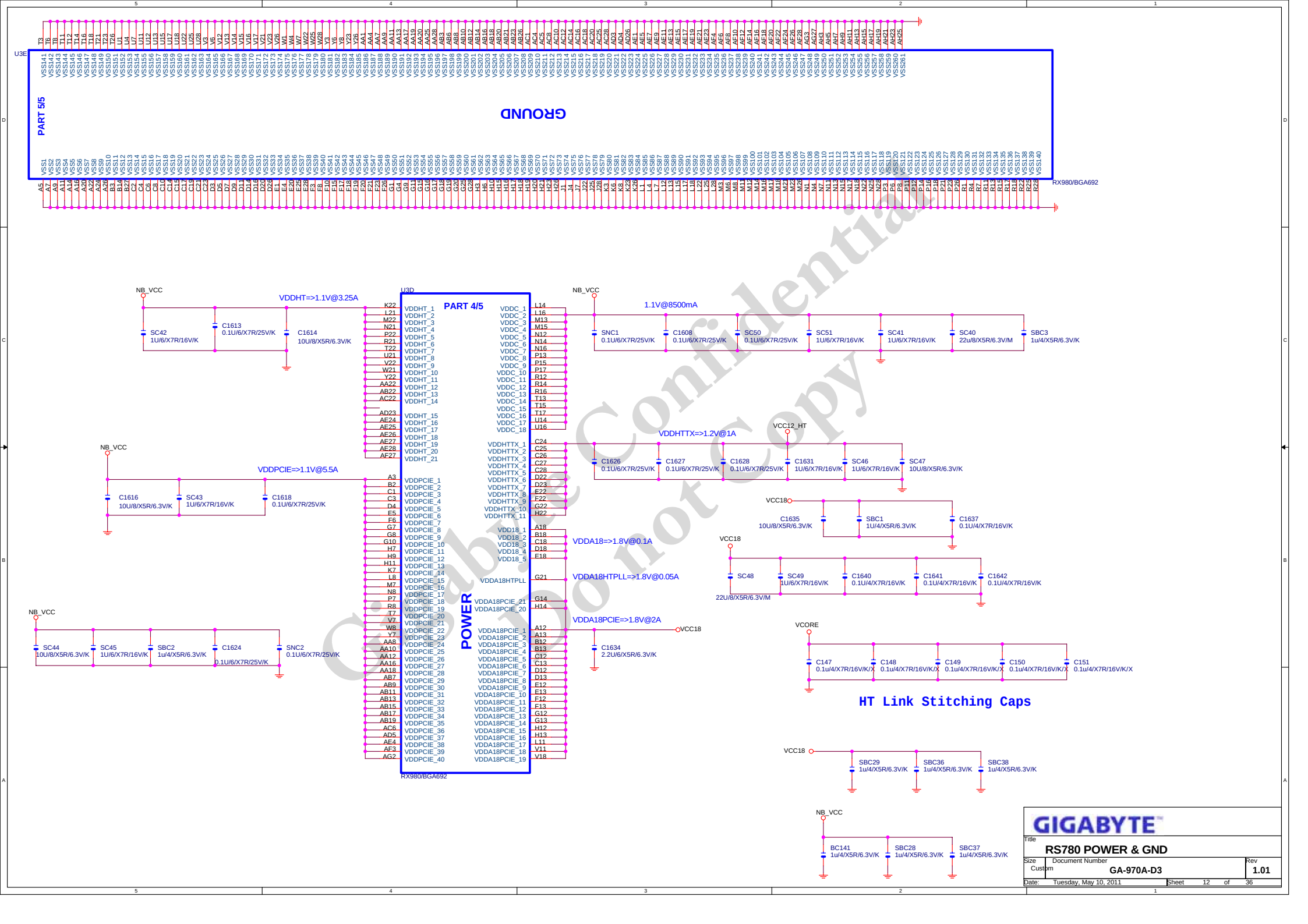
U3E
PART 5/5
GROUND
RX980/BGA692
U3D
PART 4/5
POWER
RX980/BGA692
NB_VCC
VDDHT=>1.1V@3.25A
SC42 1U/6/X7R/16V/K
C1613 0.1U/6/X7R/25V/K
C1614 10U/8/X5R/6.3V/K
VDDPCIE=>1.1V@5.5A
C1616 10U/8/X5R/6.3V/K
SC43 1U/6/X7R/16V/K
C1618 0.1U/6/X7R/25V/K
SC44 10U/8/X5R/6.3V/K
SC45 1U/6/X7R/16V/K
SBC2 1u/4/X5R/6.3V/K
C1624 0.1U/6/X7R/25V/K
SNC2 0.1U/6/X7R/25V/K
1.1V@8500mA
SNC1 0.1U/6/X7R/25V/K
C1608 0.1U/6/X7R/25V/K
SC50 0.1U/6/X7R/25V/K
SC51 1U/6/X7R/16V/K
SC41 1U/6/X7R/16V/K
SC40 22u/8/X5R/6.3V/M
SBC3 1u/4/X5R/6.3V/K
VDDHTTX=>1.2V@1A
VCC12_HT
C1626 0.1U/6/X7R/25V/K
C1627 0.1U/6/X7R/25V/K
C1628 0.1U/6/X7R/25V/K
C1631 0.1U/6/X7R/16V/K
SC46 1U/6/X7R/16V/K
SC47 10U/8/X5R/6.3V/K
VDDA18=>1.8V@0.1A
VDDA18HTPLL=>1.8V@0.05A
VDDA18PCIE=>1.8V@2A
C1634 2.2U/6/X5R/6.3V/K
VCC18
C1635 10U/8/X5R/6.3V/K
SBC1 1U/4/X5R/6.3V/K
C1637 0.1U/4/X7R/16V/K
SC48 22U/8/X5R/6.3V/M
SC49 1U/6/X7R/16V/K
C1640 0.1U/4/X7R/16V/K
C1641 0.1U/4/X7R/16V/K
C1642 0.1U/4/X7R/16V/K
VCORE
C147 0.1u/4/X7R/16V/K/X
C148 0.1u/4/X7R/16V/K/X
C149 0.1u/4/X7R/16V/K/X
C150 0.1u/4/X7R/16V/K/X
C151 0.1u/4/X7R/16V/K/X
HT Link Stitching Caps
SBC29 1u/4/X5R/6.3V/K
SBC36 1u/4/X5R/6.3V/K
SBC38 1u/4/X5R/6.3V/K
BC141 1u/4/X5R/6.3V/K
SBC28 1u/4/X5R/6.3V/K
SBC37 1u/4/X5R/6.3V/K
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Title
RS780 POWER & GND
Size Custom
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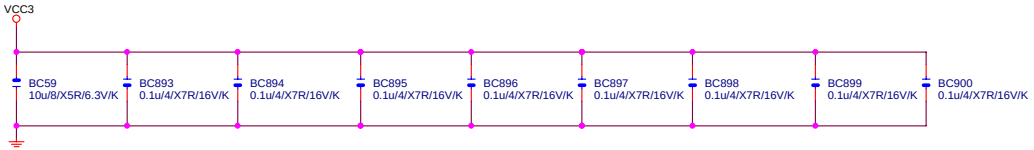


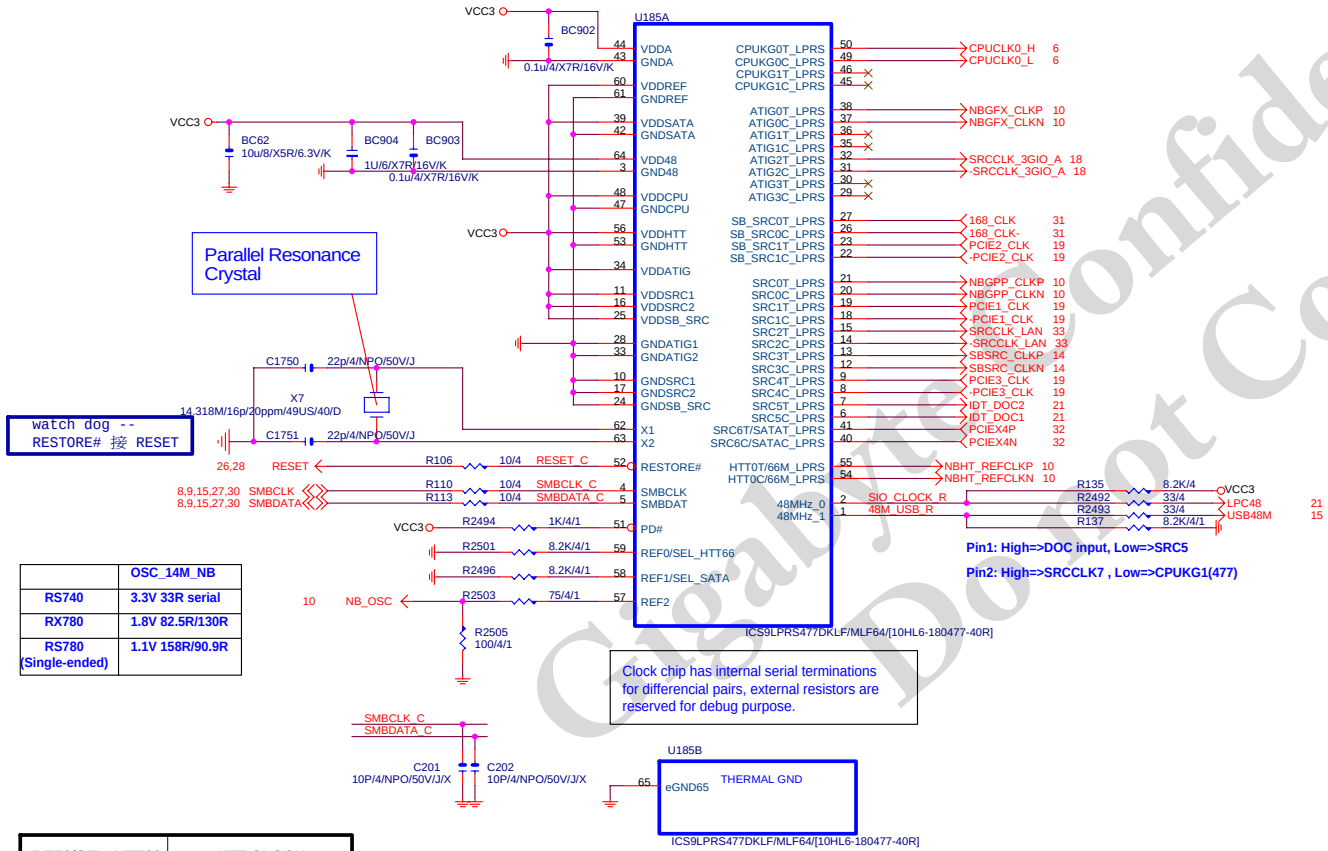
1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

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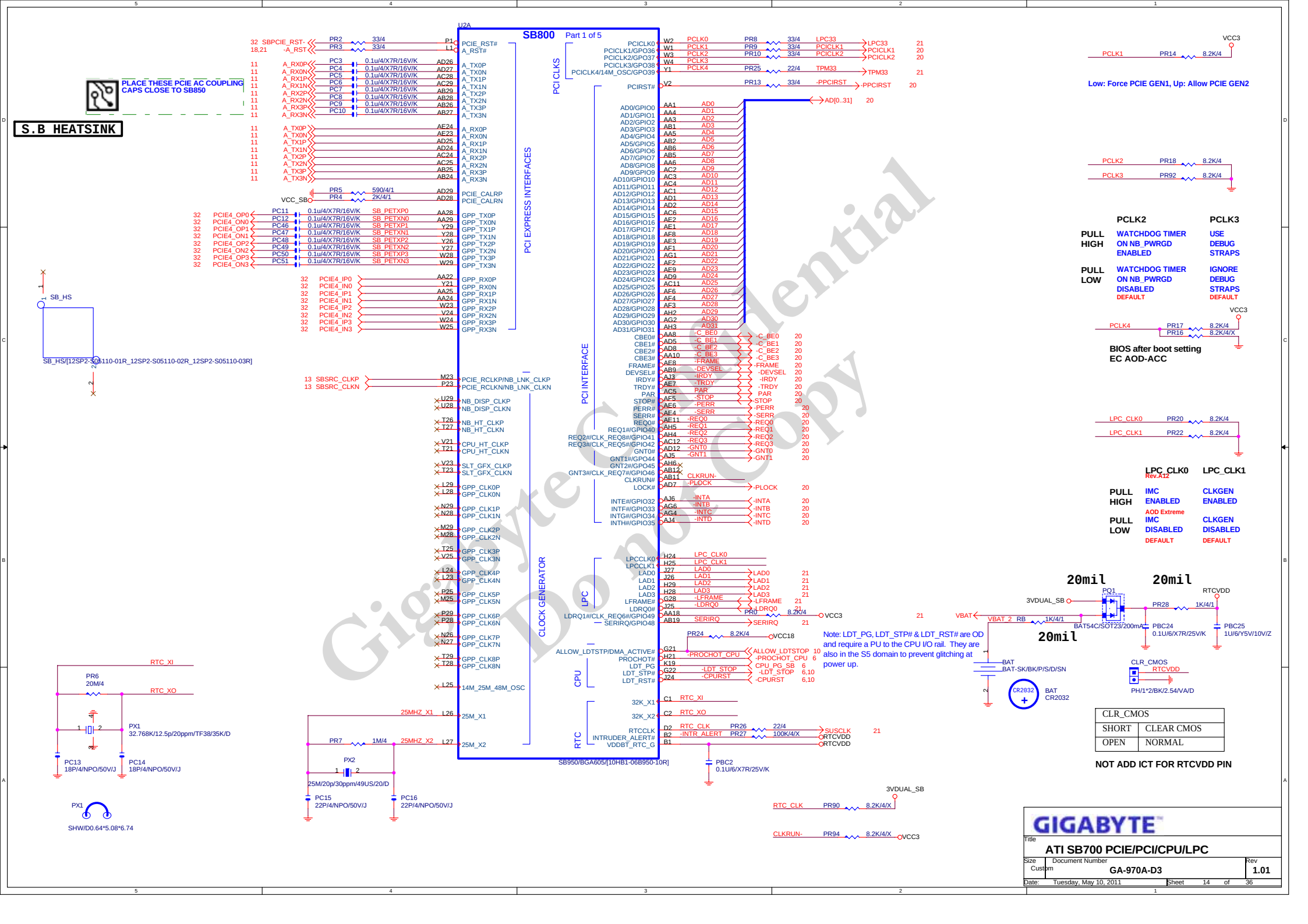
Title: RTM880N-793

Size: Custom | Document Number: GA-970A-D3 | Rev: 1.01

Date: Tuesday, May 10, 2011 | Sheet 13 of 36



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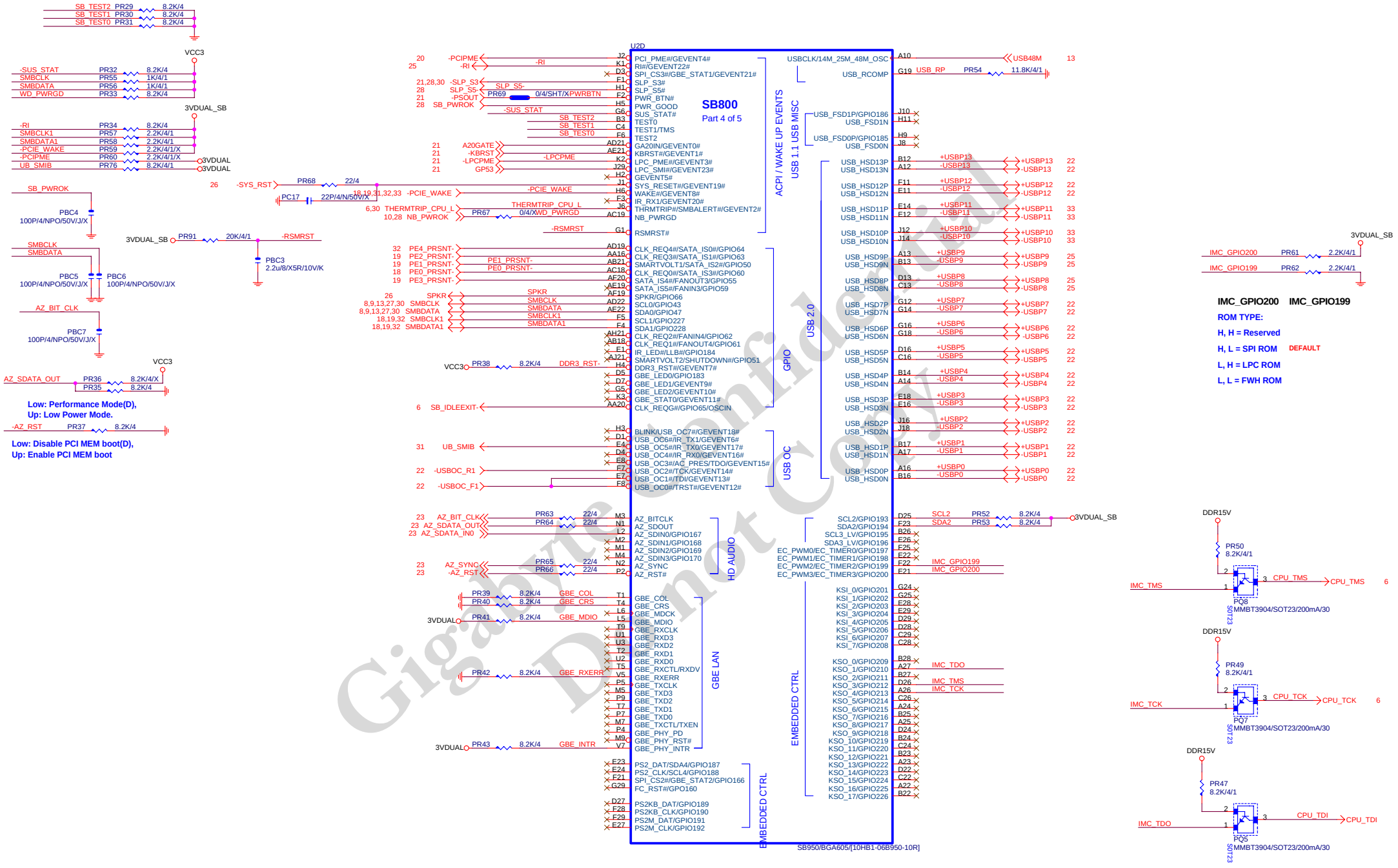

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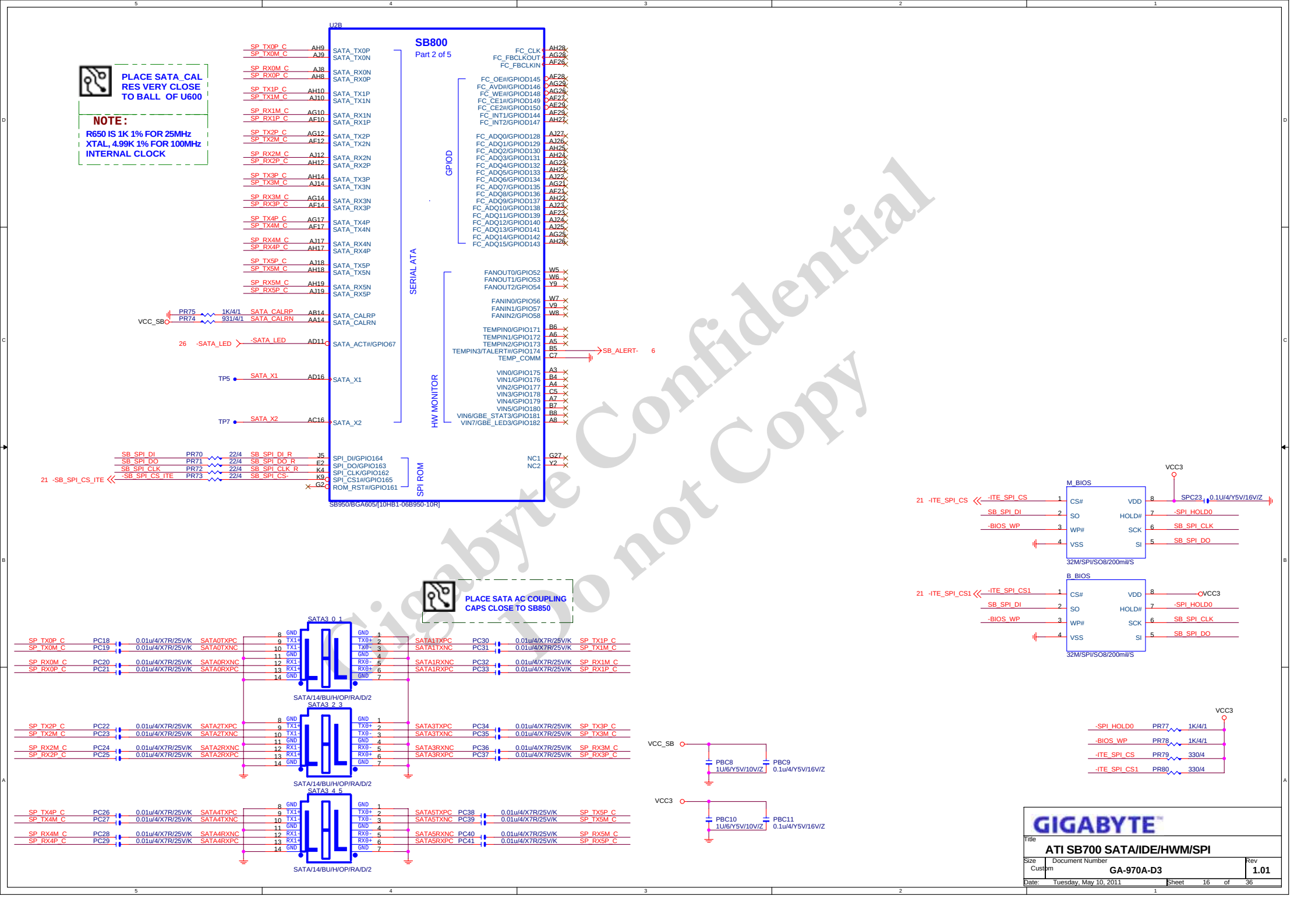
Title: ATI SB700 ACPI/USB/GPIO/AUDIO

Size	Document Number	Rev
Custom	GA-970A-D3	1.01

Date: Tuesday, May 10, 2011 Sheet 15 of 36


PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600
NOTE:
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK
U2B
SB800
Part 2 of 5
SERIAL ATA
GPIOD
HW MONITOR
SPI ROM
SB950/BGA605/[10HB1-06B950-10R]
PLACE SATA AC COUPLING CAPS CLOSE TO SB850
M_BIOS
B_BIOS
32M/SPI/SO8/200mil/S
SATA3_0_1
SATA3_2_3
SATA3_4_5
SATA/14/BU/H/OP/RA/D/2
GIGABYTE
ATI SB700 SATA/IDE/HWM/SPI
GA-970A-D3
1.01
Tuesday, May 10, 2011
Sheet 16 of 36
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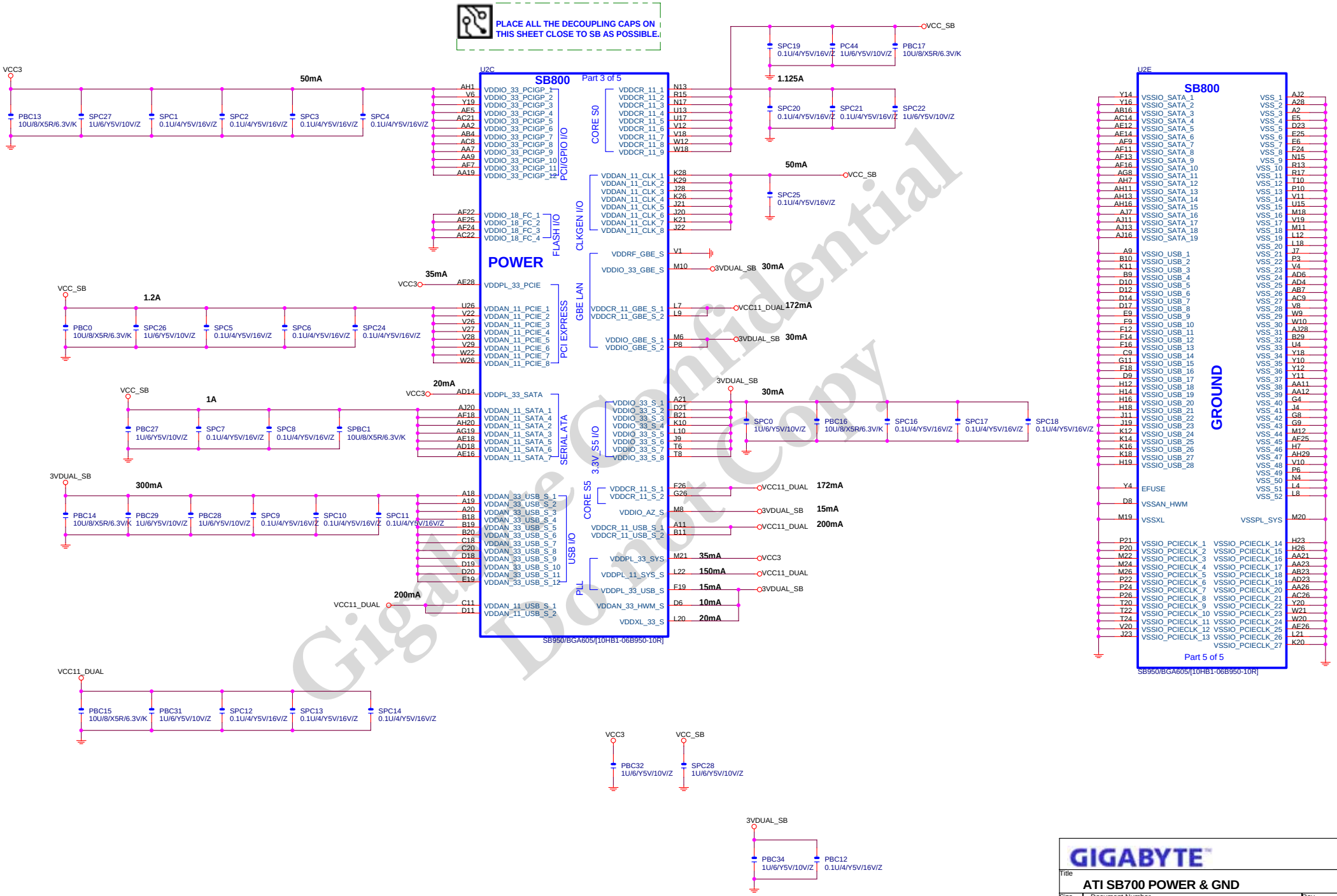
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
SB800
Part 3 of 5
POWER
PCI/GPIO I/O
FLASH I/O
CLKGEN I/O
GBE LAN
PCI EXPRESS
SERIAL ATA
3.3V_S5 I/O
CORE S0
CORE S5
USB I/O
PLL
SB950/BGA605/[10HB1-06B950-10R]
SB800
GROUND
Part 5 of 5
SB950/BGA605/[10HB1-06B950-10R]
50mA
1.125A
35mA
1.2A
20mA
1A
300mA
200mA
30mA
172mA
15mA
150mA
10mA
20mA
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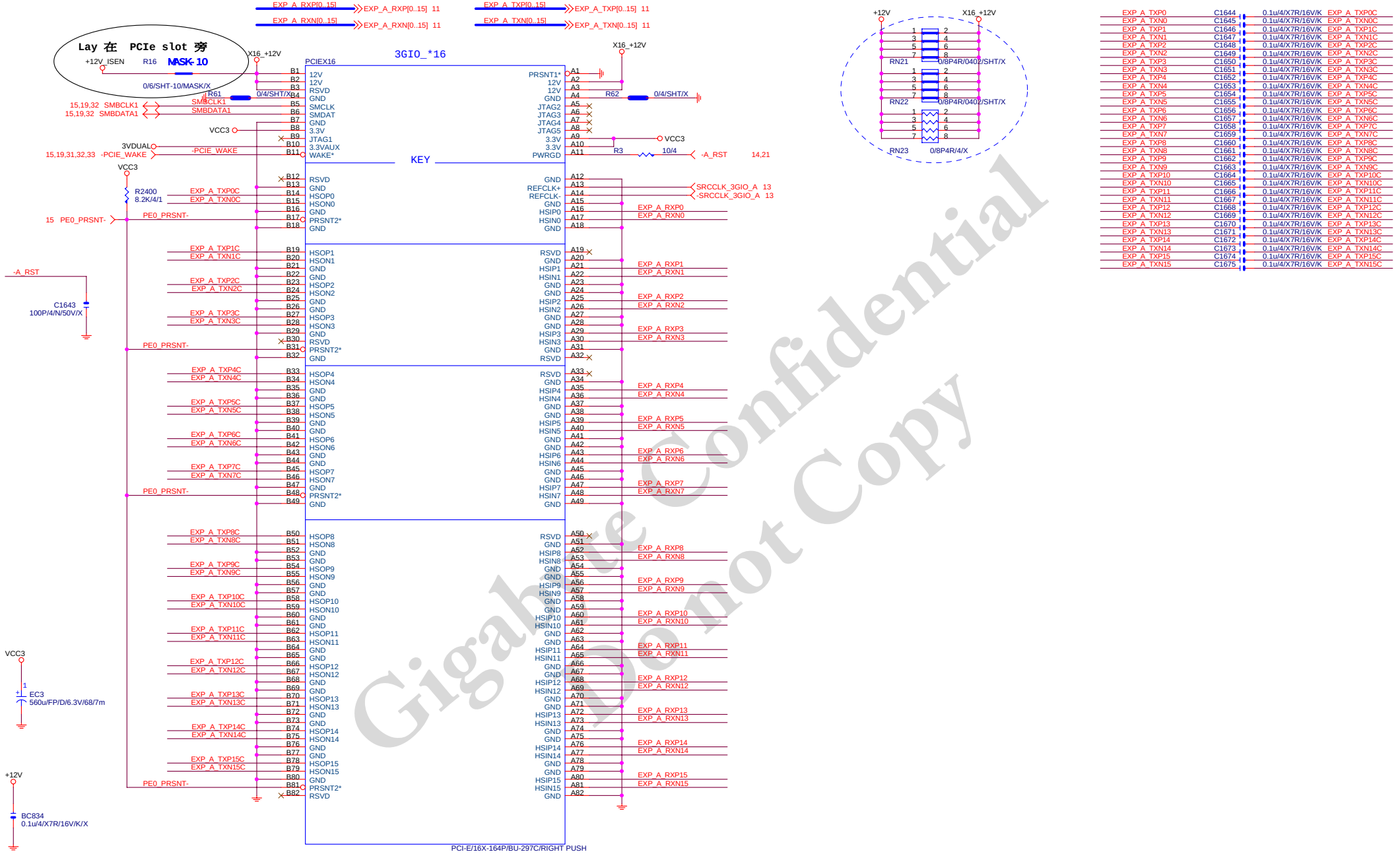
ATI SB700 POWER & GND
GA-970A-D3
1.01
Tuesday, May 10, 2011
17 of 36



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EXP_A_TXP0	C1644	0.1u/4/X7R/16V/K EXP_A_TXP0C
EXP_A_TXN0	C1645	0.1u/4/X7R/16V/K EXP_A_TXN0C
EXP_A_TXP1	C1646	0.1u/4/X7R/16V/K EXP_A_TXP1C
EXP_A_TXN1	C1647	0.1u/4/X7R/16V/K EXP_A_TXN1C
EXP_A_TXP2	C1648	0.1u/4/X7R/16V/K EXP_A_TXP2C
EXP_A_TXN2	C1649	0.1u/4/X7R/16V/K EXP_A_TXN2C
EXP_A_TXP3	C1650	0.1u/4/X7R/16V/K EXP_A_TXP3C
EXP_A_TXN3	C1651	0.1u/4/X7R/16V/K EXP_A_TXN3C
EXP_A_TXP4	C1652	0.1u/4/X7R/16V/K EXP_A_TXP4C
EXP_A_TXN4	C1653	0.1u/4/X7R/16V/K EXP_A_TXN4C
EXP_A_TXP5	C1654	0.1u/4/X7R/16V/K EXP_A_TXP5C
EXP_A_TXN5	C1655	0.1u/4/X7R/16V/K EXP_A_TXN5C
EXP_A_TXP6	C1656	0.1u/4/X7R/16V/K EXP_A_TXP6C
EXP_A_TXN6	C1657	0.1u/4/X7R/16V/K EXP_A_TXN6C
EXP_A_TXP7	C1658	0.1u/4/X7R/16V/K EXP_A_TXP7C
EXP_A_TXN7	C1659	0.1u/4/X7R/16V/K EXP_A_TXN7C
EXP_A_TXP8	C1660	0.1u/4/X7R/16V/K EXP_A_TXP8C
EXP_A_TXN8	C1661	0.1u/4/X7R/16V/K EXP_A_TXN8C
EXP_A_TXP9	C1662	0.1u/4/X7R/16V/K EXP_A_TXP9C
EXP_A_TXN9	C1663	0.1u/4/X7R/16V/K EXP_A_TXN9C
EXP_A_TXP10	C1664	0.1u/4/X7R/16V/K EXP_A_TXP10C
EXP_A_TXN10	C1665	0.1u/4/X7R/16V/K EXP_A_TXN10C
EXP_A_TXP11	C1666	0.1u/4/X7R/16V/K EXP_A_TXP11C
EXP_A_TXN11	C1667	0.1u/4/X7R/16V/K EXP_A_TXN11C
EXP_A_TXP12	C1668	0.1u/4/X7R/16V/K EXP_A_TXP12C
EXP_A_TXN12	C1669	0.1u/4/X7R/16V/K EXP_A_TXN12C
EXP_A_TXP13	C1670	0.1u/4/X7R/16V/K EXP_A_TXP13C
EXP_A_TXN13	C1671	0.1u/4/X7R/16V/K EXP_A_TXN13C
EXP_A_TXP14	C1672	0.1u/4/X7R/16V/K EXP_A_TXP14C
EXP_A_TXN14	C1673	0.1u/4/X7R/16V/K EXP_A_TXN14C
EXP_A_TXP15	C1674	0.1u/4/X7R/16V/K EXP_A_TXP15C
EXP_A_TXN15	C1675	0.1u/4/X7R/16V/K EXP_A_TXN15C

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Title: PCI EXPRESS X 16 ,X1

Size	Document Number	Rev
Custom	GA-970A-D3	1.01

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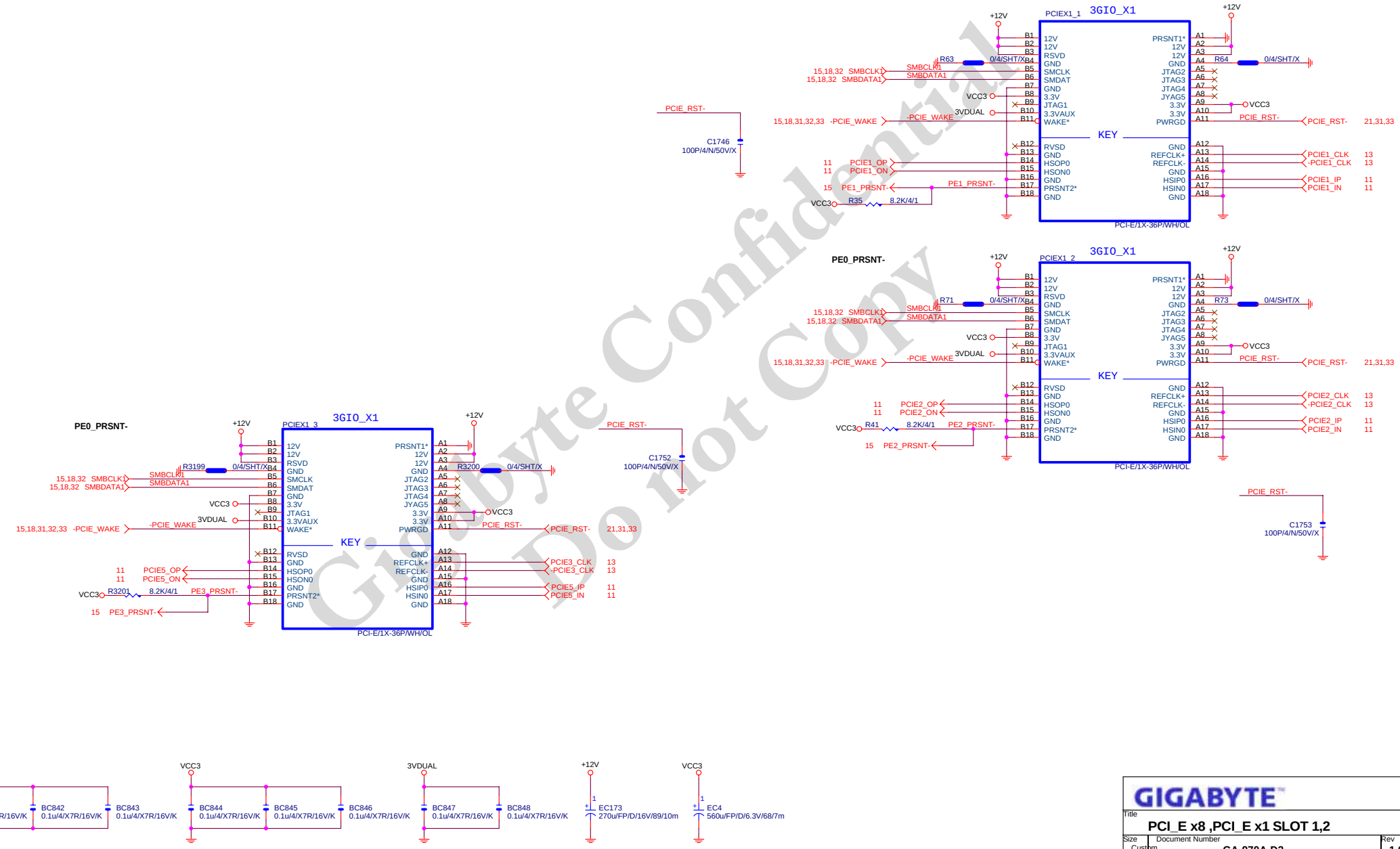

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Title: PCI_E x8 ,PCI_E x1 SLOT 1,2

Size	Document Number	Rev
Custom	GA-970A-D3	1.01

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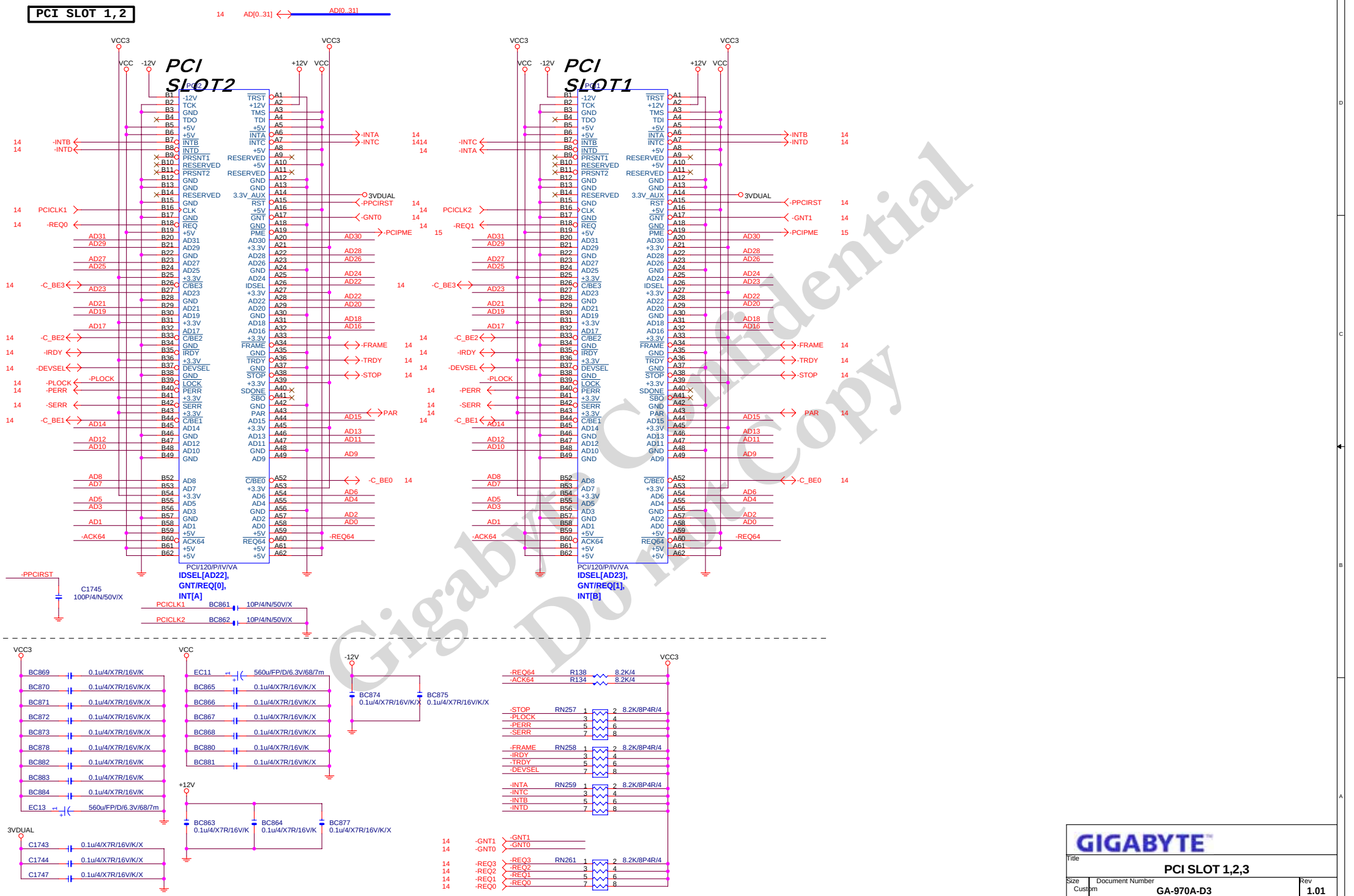
PCI SLOT 1,2



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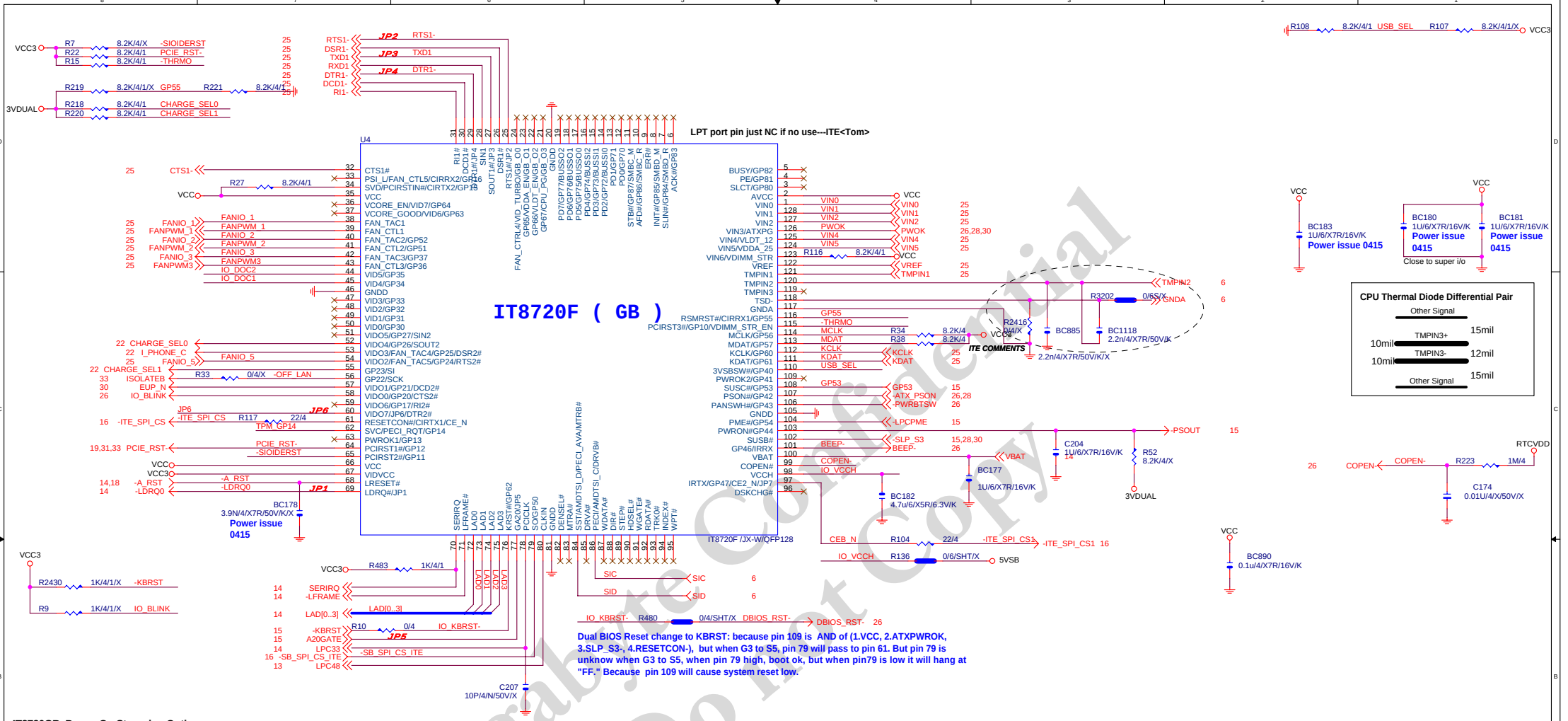
Title	PCI SLOT 1,2,3	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 20 of 36	



IT8720GB Power On Strapping Options

	Symbol	value	Description
JP1 Pin 69			
JP2 Pin 25	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 27	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 29	K8PWR_EN	1	K8 power sequence disabled
		0	K8 power sequence enabled
JP3 & JP5 Pin 27 & Pin 77	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5 Pin 77	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin 60	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function
JP7 Pin 97	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
		0	Disable Dual BIOS Function for GigaByte Only

Title	ITE 8720 JX LPC IO ,Dual-BIOS ,TPM	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
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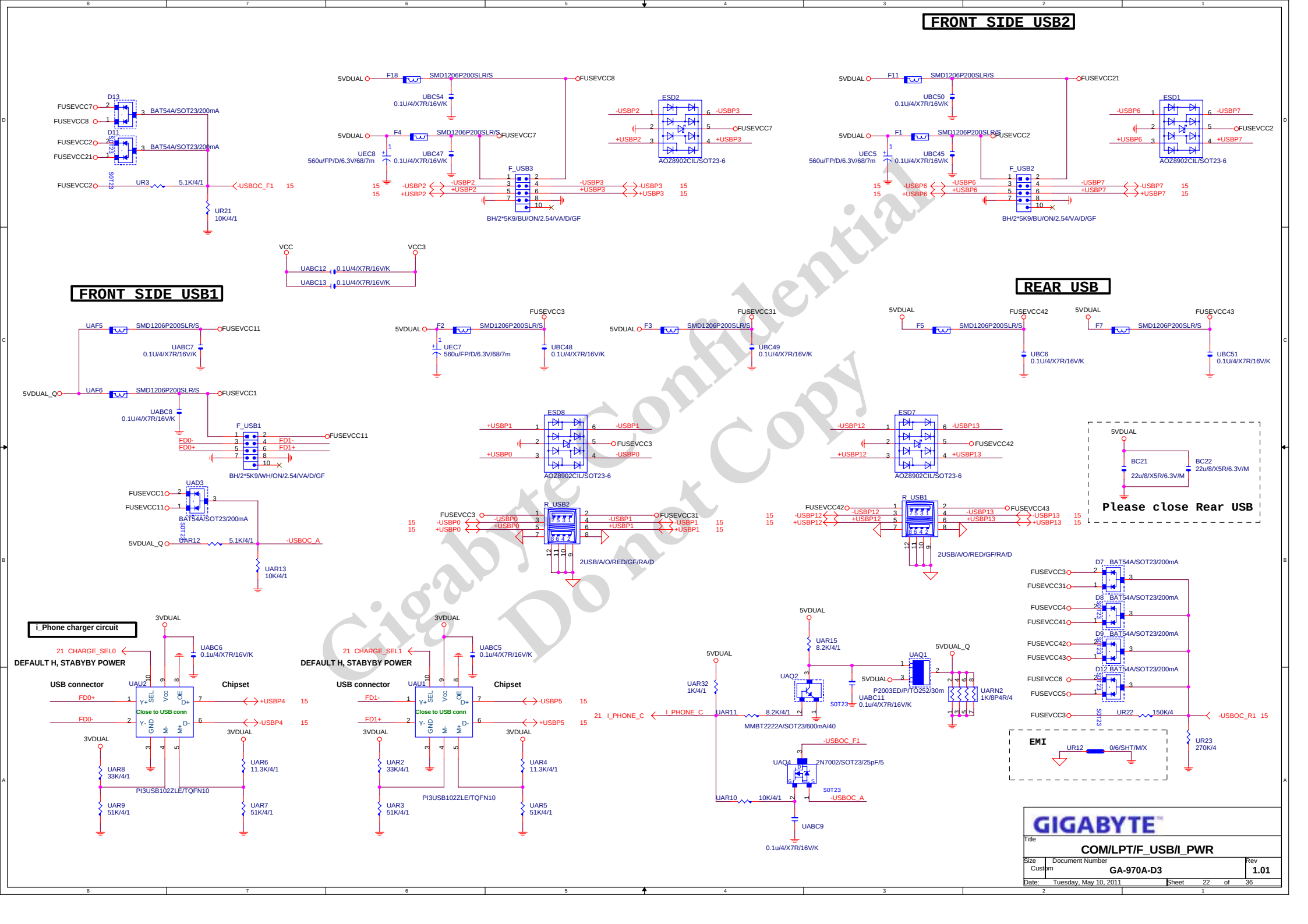
FRONT SIDE USB2
FRONT SIDE USB1
REAR USB
i_Phone charger circuit
DEFAULT H, STABYBY POWER
USB connector
Chipset
Close to USB conn
PI3USB102ZLE/TQFN10
2USB/A/O/RED/GF/RA/D
BH/2*5K9/BU/ON/2.54/VA/D/GF
BH/2*5K9/WH/ON/2.54/VA/D/GF
AOZ8902CIL/SOT23-6
MMBT2222A/SOT23/600mA/40
P2003ED/P/TO252/30m
2N7002/SOT23/25pF/5
Please close Rear USB
EMI
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COM/LPT/F_USB/I_PWR
GA-970A-D3
1.01
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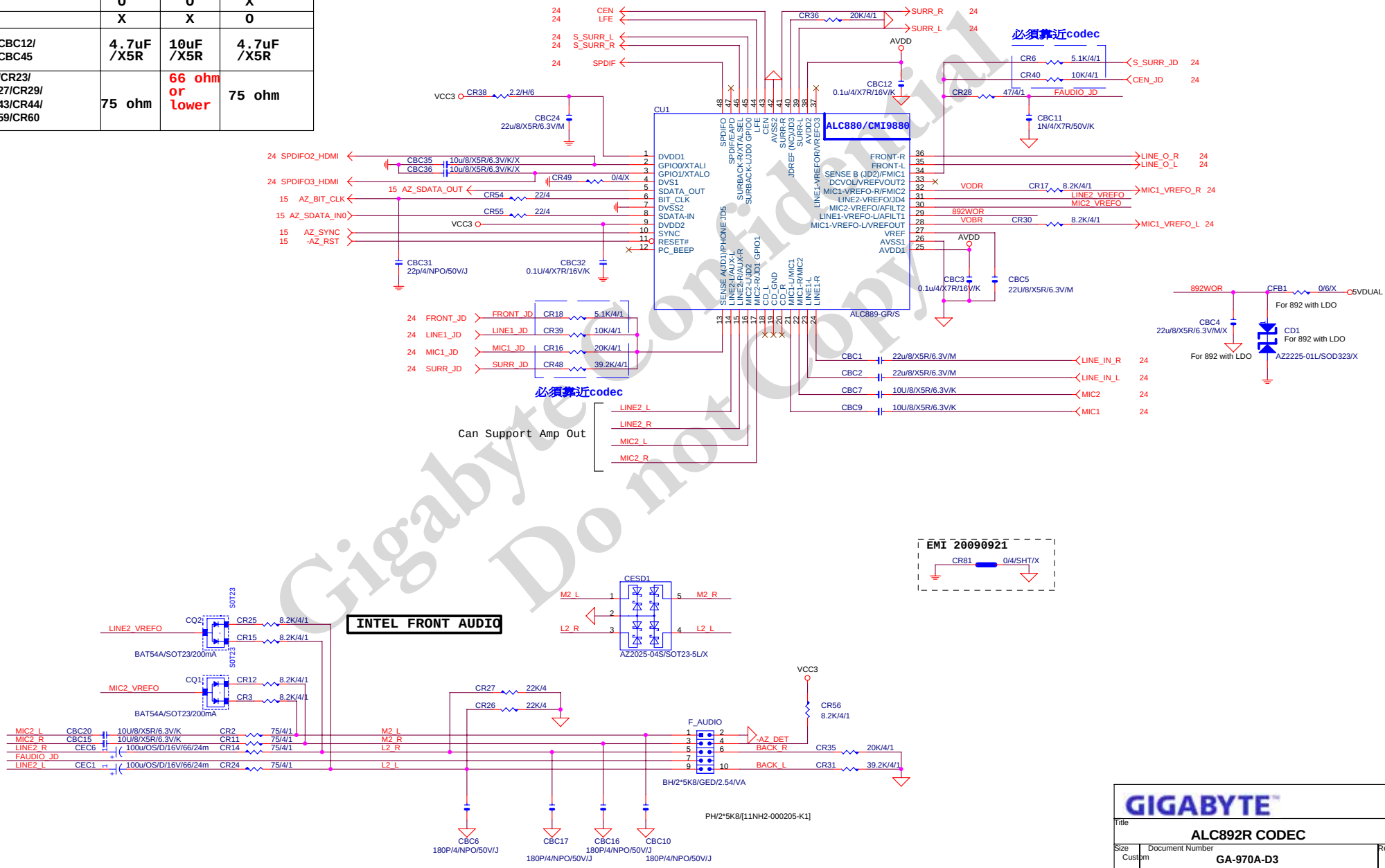
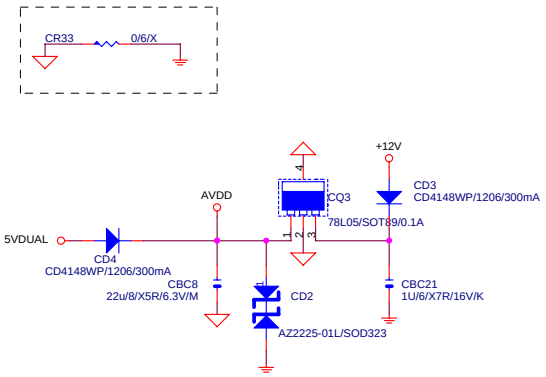
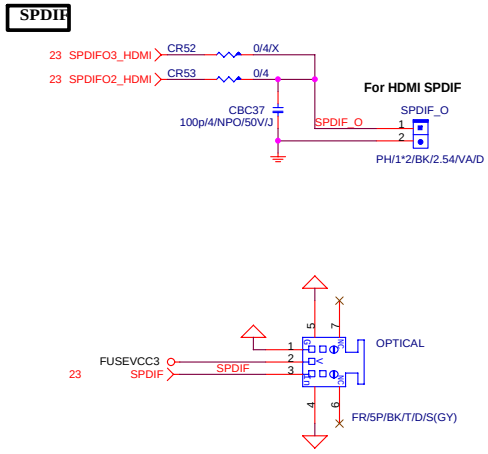
AZALIA CODEC *ALC892/ALC889/ Colay*

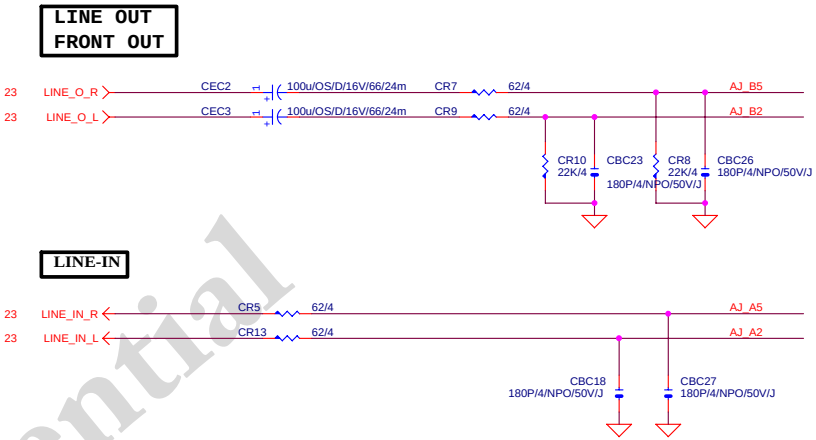
	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm

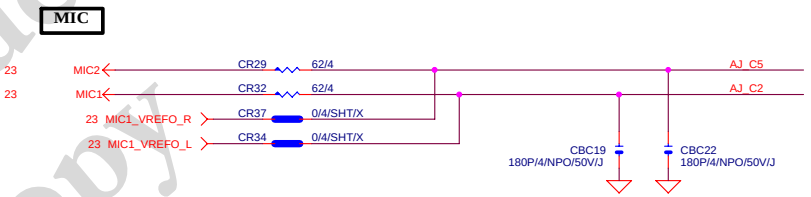


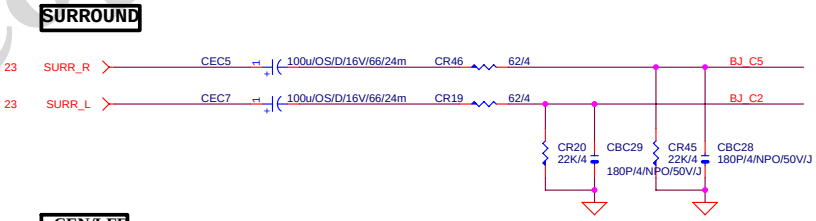
Title	ALC892R CODEC
Size	Custom
Document Number	GA-970A-D3
Rev	1.01
Date:	Tuesday, May 10, 2011
Sheet	23 of 36

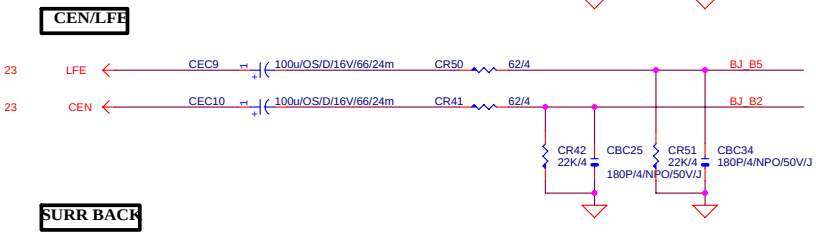


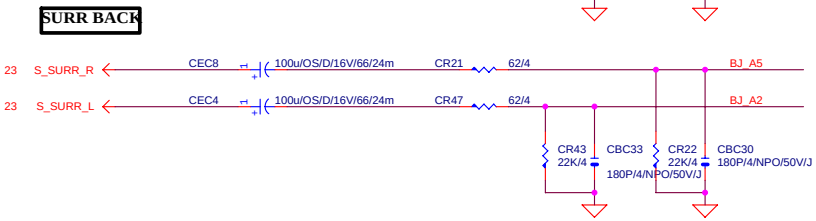


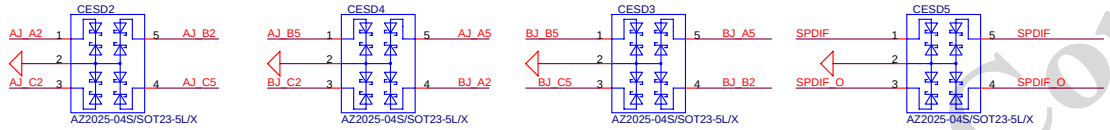


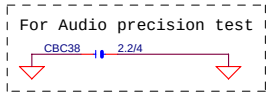


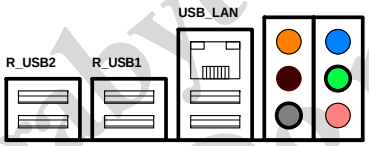


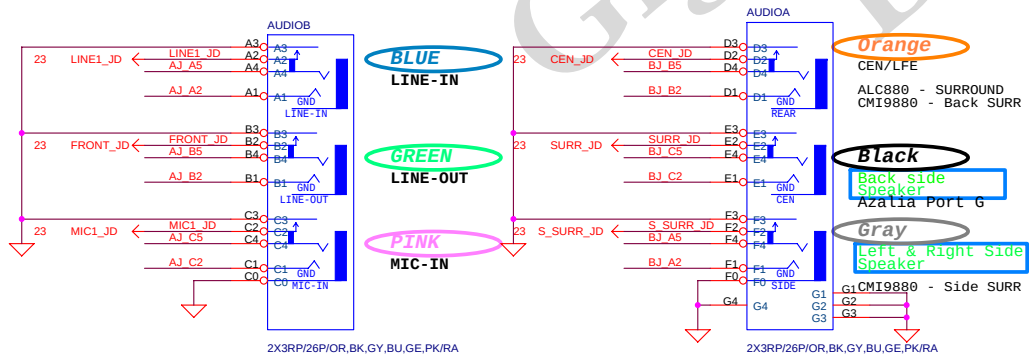












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Title: AUDIO JACK

Size	Document Number	Rev
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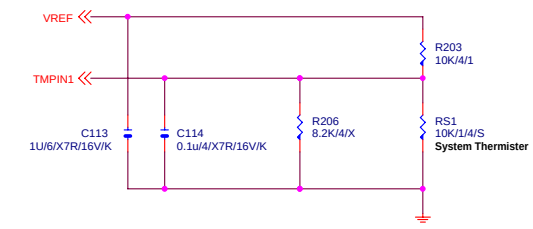
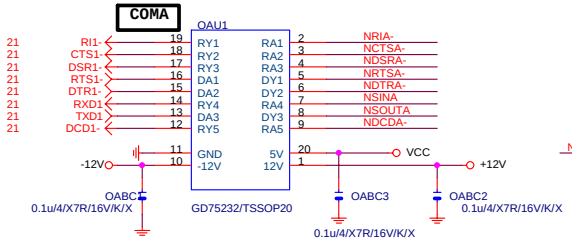
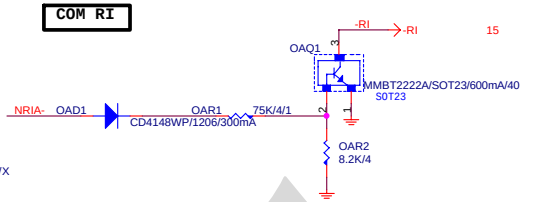
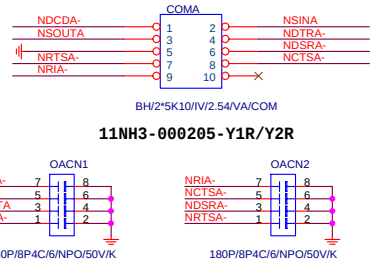
Hardware Monitor circuits

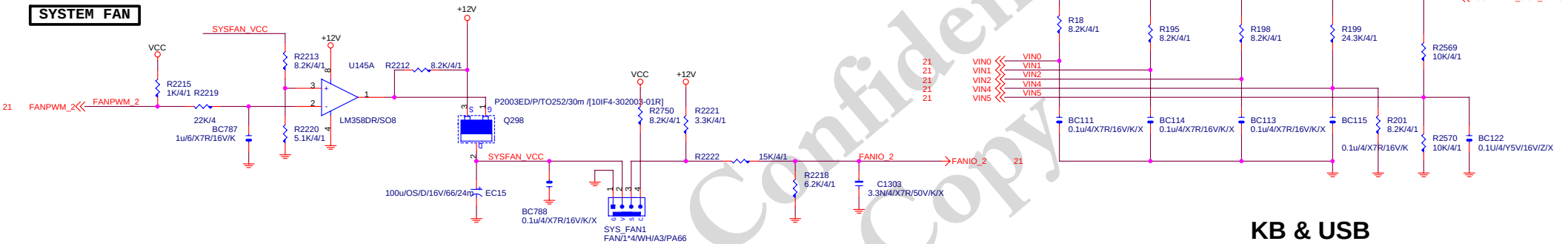




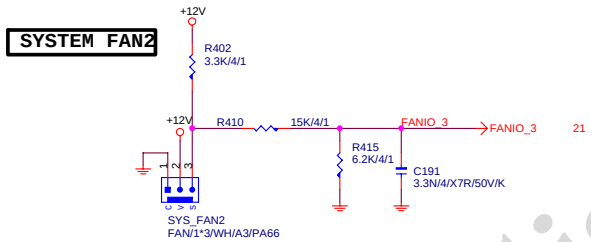




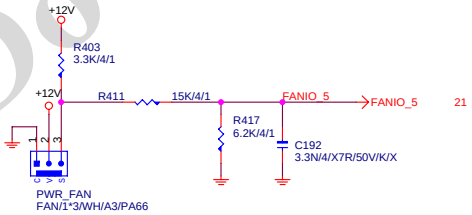
SYSTEM FAN



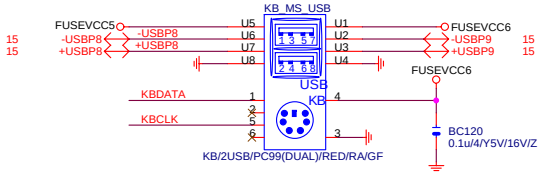
SYSTEM FAN2

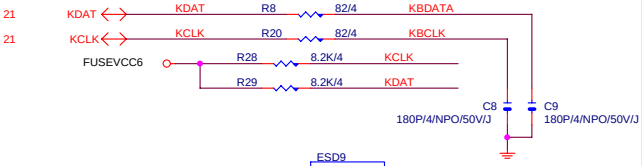


POWER FAN

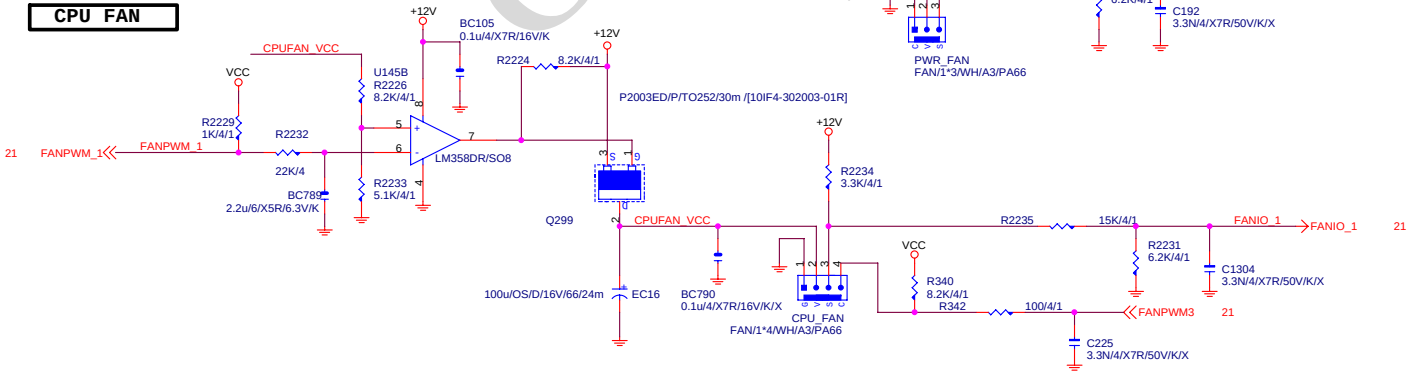


KB & USB





CPU FAN



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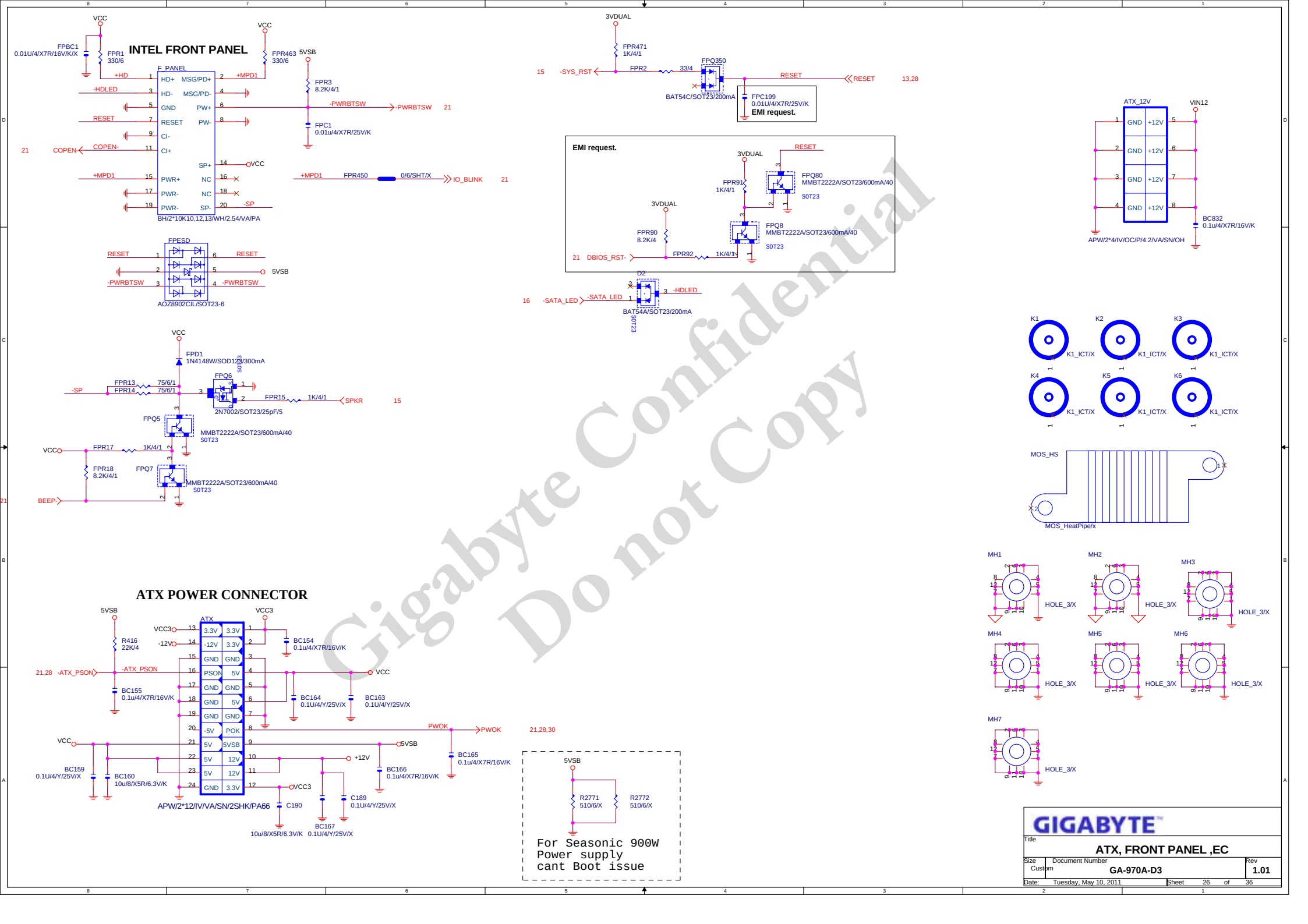
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 25 of 36	


INTEL FRONT PANEL
F_PANEL
BH/2*10K10,12,13/WH/2.54/VA/PA
AOZ8902CIL/SOT23-6
ATX POWER CONNECTOR
APW/2*12/IV/VA/SN/2SHK/PA66
For Seasonic 900W
Power supply
cant Boot issue
EMI request.
ATX_12V
APW/2*4/IV/OC/P/4.2/VA/SN/OH
MOS_HeatPipe/x
HOLE_3/X
GIGABYTE
ATX, FRONT PANEL ,EC
GA-970A-D3
1.01
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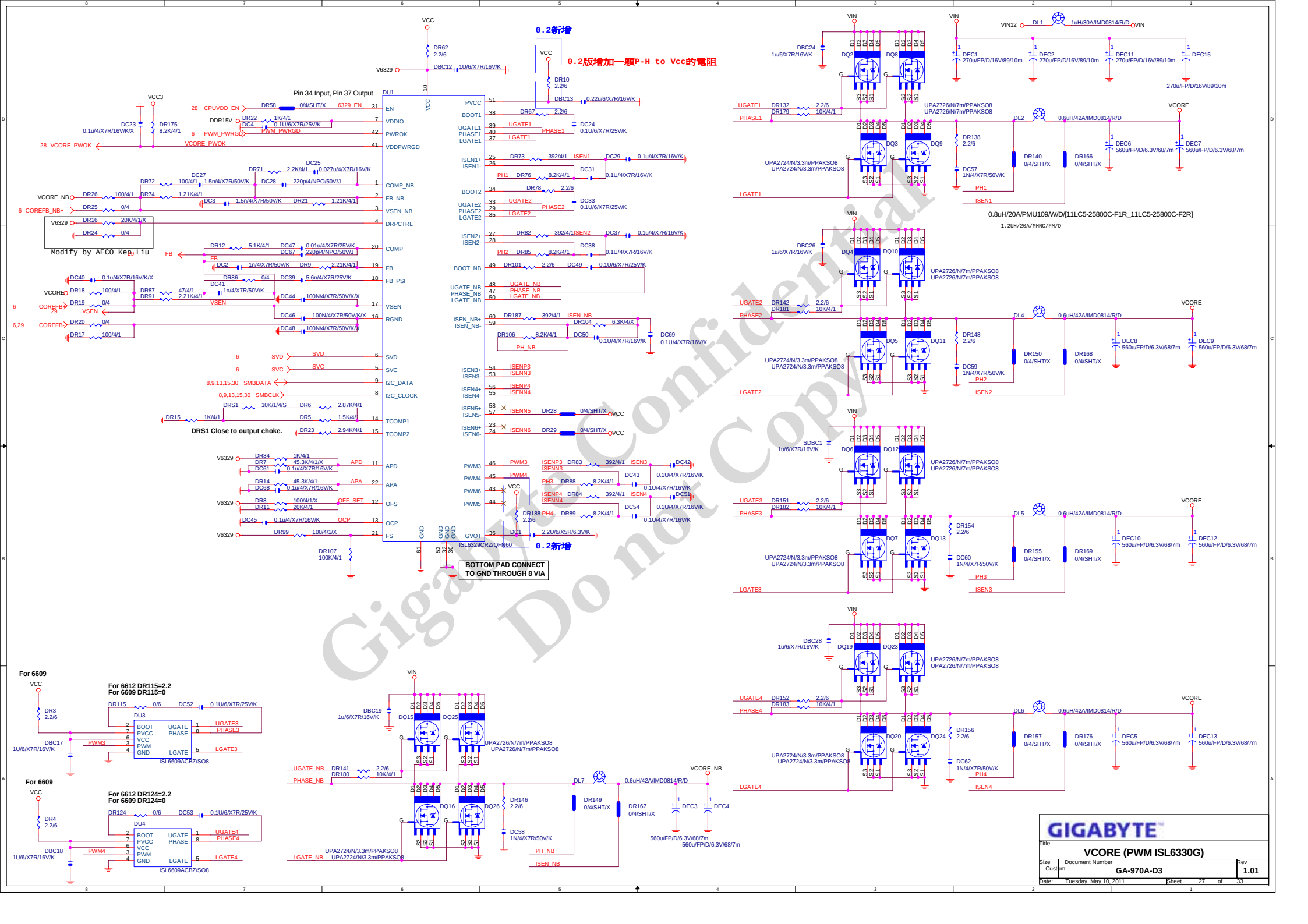
Pin 34 Input, Pin 37 Output
Modify by AECO Ken Liu
DRS1 Close to output choke.
BOTTOM PAD CONNECT TO GND THROUGH 8 VIA
0.2新增
0.2版增加一顆P-H to Vcc的電阻
0.8uH/20A/PMU109/W/D/[11LC5-25800C-F1R_11LC5-25800C-F2R]
1.2UH/20A/MHNC/FM/D
ISL6329CRZ/QFN60
ISL6609ACBZ/SO8
For 6609
For 6612 DR115=2.2
For 6609 DR115=0
For 6612 DR124=2.2
For 6609 DR124=0
GIGABYTE
VCORE (PWM ISL6330G)
GA-970A-D3
1.01
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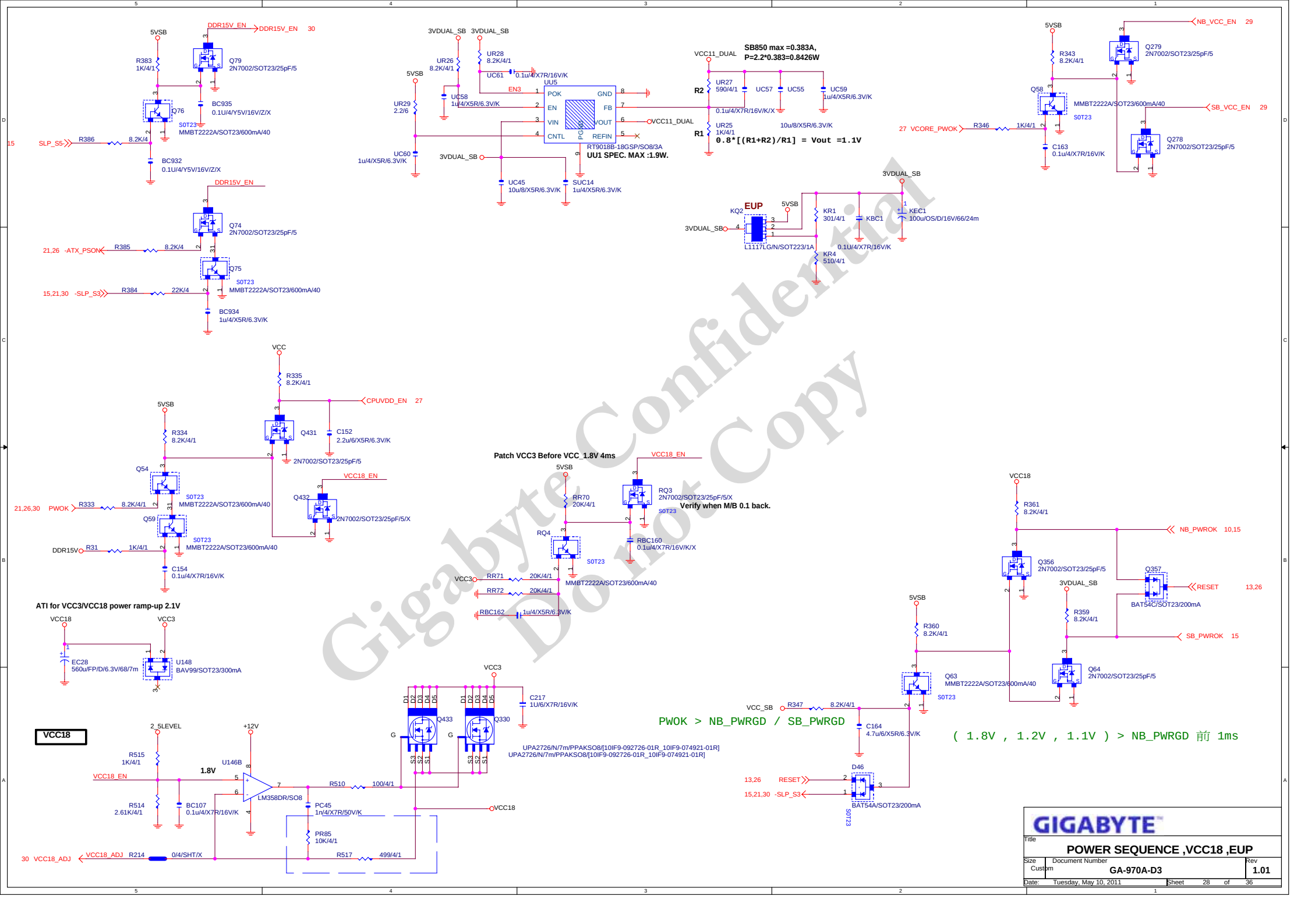

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Title	POWER SEQUENCE ,VCC18 ,EUP	
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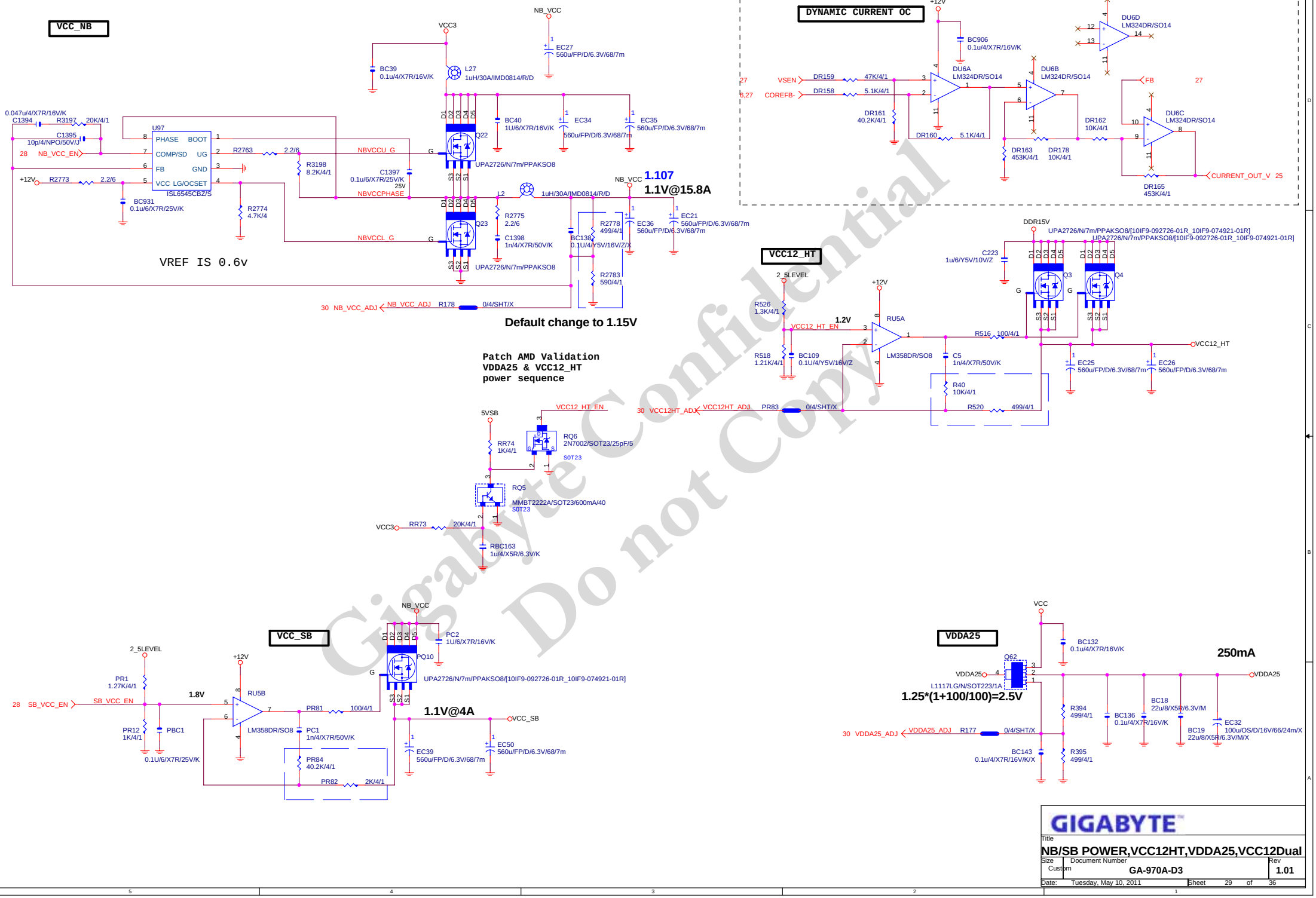

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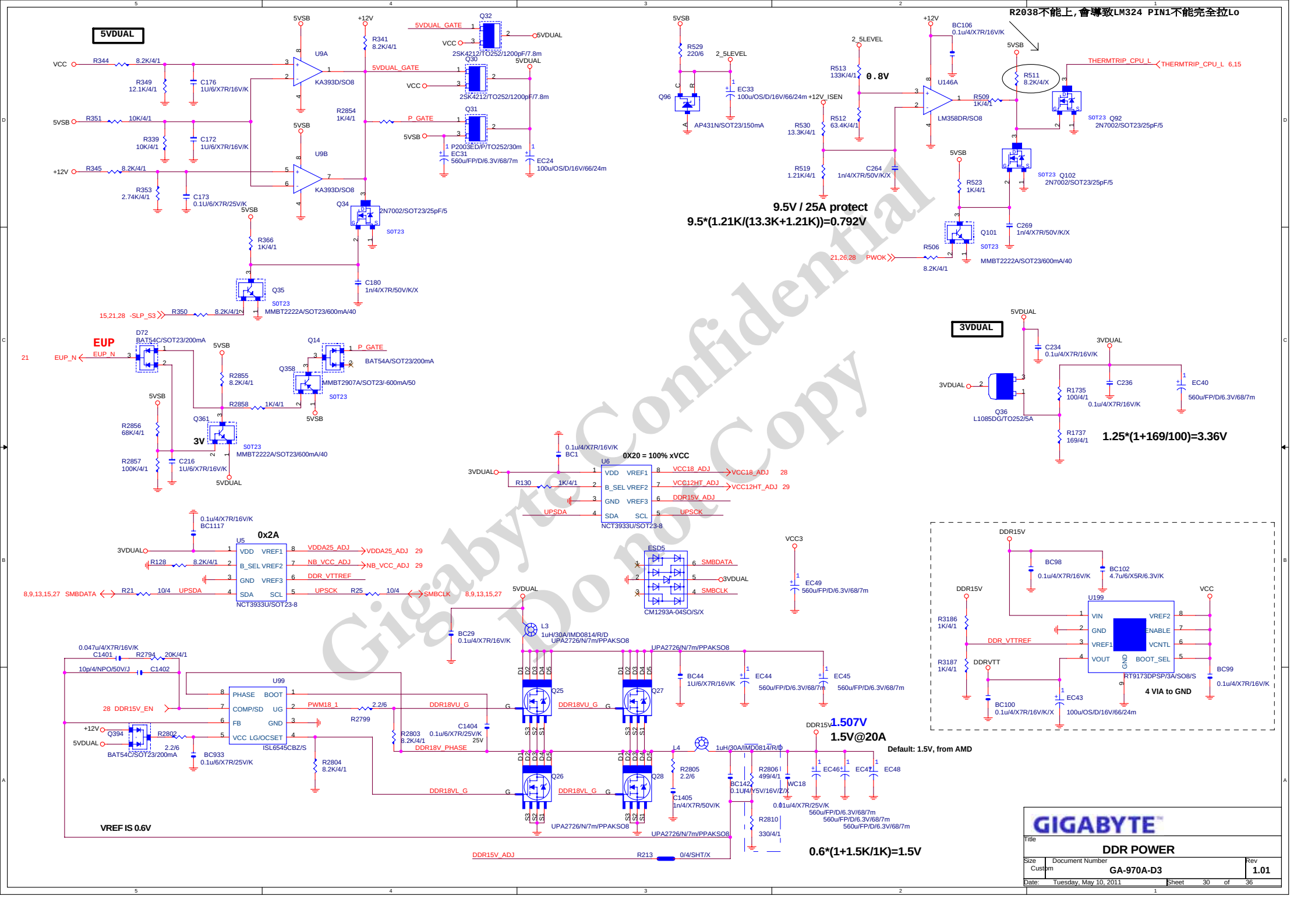
R2038不能上，會導致LM324 PIN1不能完全拉Lo
5VDUAL
EUP
3VDUAL
0x20 = 100% xVCC
0x2A
9.5V / 25A protect
9.5*(1.21K/(13.3K+1.21K))=0.792V
1.25*(1+169/100)=3.36V
3V
1.507V
1.5V@20A
Default: 1.5V, from AMD
0.6*(1+1.5K/1K)=1.5V
VREF IS 0.6V
4 VIA to GND
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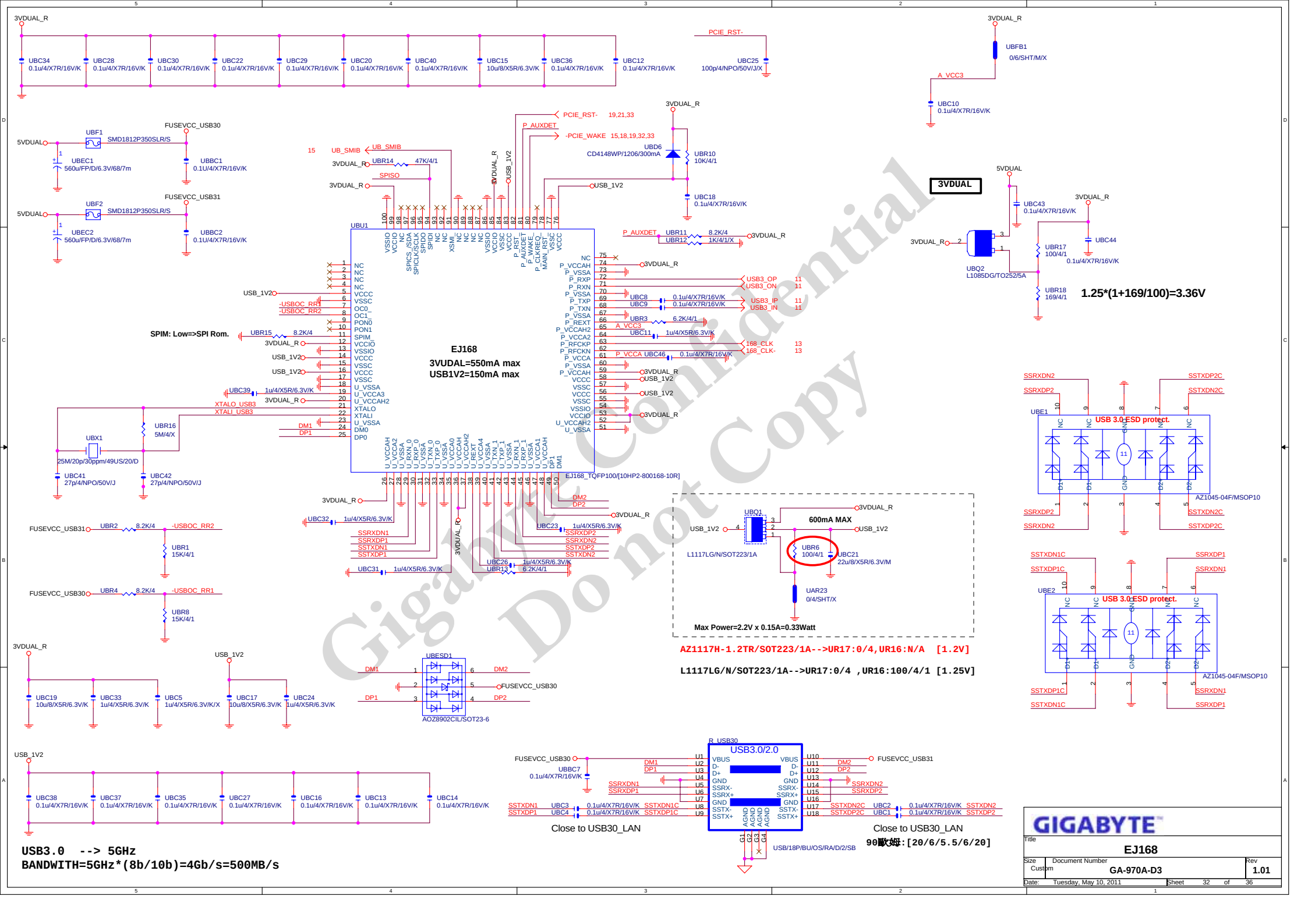
DDR POWER
GA-970A-D3
1.01
Tuesday, May 10, 2011


3VDUAL_R
UBC34 0.1u/4/X7R/16V/K
UBC28 0.1u/4/X7R/16V/K
UBC30 0.1u/4/X7R/16V/K
UBC22 0.1u/4/X7R/16V/K
UBC29 0.1u/4/X7R/16V/K
UBC20 0.1u/4/X7R/16V/K
UBC40 0.1u/4/X7R/16V/K
UBC15 10u/8/X5R/6.3V/K
UBC36 0.1u/4/X7R/16V/K
UBC12 0.1u/4/X7R/16V/K
PCIE_RST-
UBC25 100p/4/NPO/50V/J/X
UBFB1 0/6/SHT/M/X
A_VCC3
UBC10 0.1u/4/X7R/16V/K
5VDUAL
UBF1 SMD1812P350SLR/S
FUSEVCC_USB30
UBEC1 560u/FP/D/6.3V/68/7m
UBBC1 0.1U/4/X7R/16V/K
UBF2 SMD1812P350SLR/S
FUSEVCC_USB31
UBEC2 560u/FP/D/6.3V/68/7m
UBBC2 0.1U/4/X7R/16V/K
15 UB_SMIB
UBR14 47K/4/1
SPISO
PCIE_RST- 19,21,33
P_AUXDET
-PCIE_WAKE 15,18,19,32,33
UBD6 CD4148WP/1206/300mA
UBR10 10K/4/1
UBC18 0.1u/4/X7R/16V/K
USB_1V2
UBU1
EJ168
3VUDAL=550mA max
USB1V2=150mA max
SPIM: Low=>SPI Rom.
UBR15 8.2K/4
XTALO_USB3
XTALI_USB3
UBX1 25M/20p/30ppm/49US/20/D
UBR16 5M/4/X
UBC41 27p/4/NPO/50V/J
UBC42 27p/4/NPO/50V/J
UBC39 1u/4/X5R/6.3V/K
DM1
DP1
EJ168_TQFP100/[10HP2-800168-10R]
P_AUXDET
UBR11 8.2K/4
UBR12 1K/4/1/X
UBC8 0.1u/4/X7R/16V/K
UBC9 0.1u/4/X7R/16V/K
USB3_OP 11
USB3_ON 11
USB3_IP 11
USB3_IN 11
UBR3 6.2K/4/1
A_VCC3
UBC11 1u/4/X5R/6.3V/K
168_CLK 13
168_CLK- 13
P_VCCA UBC46 0.1u/4/X7R/16V/K
UBC32 1u/4/X5R/6.3V/K
UBC23 1u/4/X5R/6.3V/K
UBC31 1u/4/X5R/6.3V/K
UBC26 1u/4/X5R/6.3V/K
UBR13 6.2K/4/1
SSRXDN1
SSRXDP1
SSTXDN1
SSTXDP1
SSRXDP2
SSRXDN2
SSTXDP2
SSTXDN2
FUSEVCC_USB31
UBR2 8.2K/4
-USBOC_RR2
UBR1 15K/4/1
FUSEVCC_USB30
UBR4 8.2K/4
-USBOC_RR1
UBR8 15K/4/1
UBQ1
L1117LG/N/SOT223/1A
600mA MAX
UBR6 100/4/1
UBC21 22u/8/X5R/6.3V/M
UAR23 0/4/SHT/X
Max Power=2.2V x 0.15A=0.33Watt
AZ1117H-1.2TR/SOT223/1A-->UR17:0/4,UR16:N/A [1.2V]
L1117LG/N/SOT223/1A-->UR17:0/4 ,UR16:100/4/1 [1.25V]
3VDUAL
UBQ2 L1085DG/TO252/5A
UBC43 0.1u/4/X7R/16V/K
UBC44 0.1u/4/X7R/16V/K
UBR17 100/4/1
UBR18 169/4/1
1.25*(1+169/100)=3.36V
UBE1
UBE2
USB 3.0 ESD protect.
AZ1045-04F/MSOP10
UBESD1
AOZ8902CIL/SOT23-6
UBC19 10u/8/X5R/6.3V/K
UBC33 1u/4/X5R/6.3V/K
UBC5 1u/4/X5R/6.3V/K/X
UBC17 10u/8/X5R/6.3V/K
UBC24 1u/4/X5R/6.3V/K
UBC38 0.1u/4/X7R/16V/K
UBC37 0.1u/4/X7R/16V/K
UBC35 0.1u/4/X7R/16V/K
UBC27 0.1u/4/X7R/16V/K
UBC16 0.1u/4/X7R/16V/K
UBC13 0.1u/4/X7R/16V/K
UBC14 0.1u/4/X7R/16V/K
USB3.0 --> 5GHz
BANDWITH=5GHz*(8b/10b)=4Gb/s=500MB/s
R_USB30
USB3.0/2.0
UBBC7 0.1u/4/X7R/16V/K
UBC3 0.1u/4/X7R/16V/K
UBC4 0.1u/4/X7R/16V/K
SSTXDN1C
SSTXDP1C
UBC2 0.1u/4/X7R/16V/K
UBC1 0.1u/4/X7R/16V/K
SSTXDN2C
SSTXDP2C
Close to USB30_LAN
Close to USB30_LAN
90歐姆:[20/6/5.5/6/20]
USB/18P/BU/OS/RA/D/2/SB
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EJ168
Size Custom
Document Number GA-970A-D3
Rev 1.01
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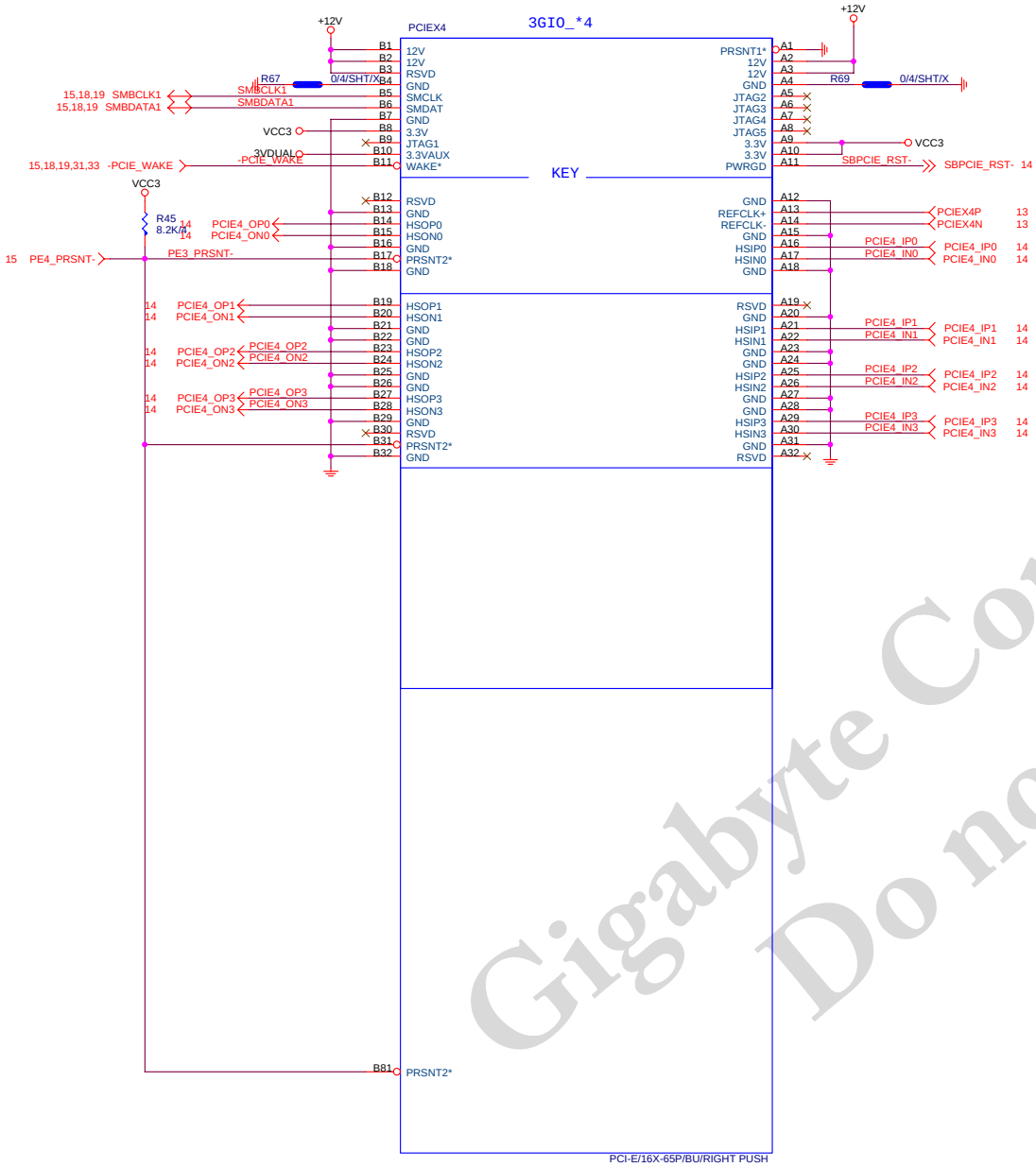

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PCIE-1G LAN

要用1% 的電阻,trace不能太長,建議在200 mil以內

Pin34/35(VDDREG) 接到3VDUAL的trace 建議寬度大於 40mil

Data trace(MDI0~3)的+/-線長需等長,誤差在5mils以內,Pair跟Pair之間線長,最長跟最短data trace請勿超過800 mil

0.2版要修改

RTL8111E-VL-CG/QFN48/S

CLOSE LAN CHIP 離IC近越好200mil以內

(CLOSE LU1)

USB_LAN CONNECTOR

P35-152-19W9

YELLOW ORANGE(+,-) GREEN(-,+)

建議使用X5R電容

USB_LAN

RTL8101E:LR38/LC5/LR43/LC6-->O

RTL8111C:LC6-->O

RTL8102E:LC5/LC6-->O

FOR EMI

USB+LAN/1G/GO,Y/OS/RA/D/1/RED

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)

1G :USB+LAN/1G/GO,Y/OS/RA/D/1

100M:USB+LAN/100/GO,Y/OS/RA/D/1

EMI

AOZ8902CIL/SOT23-6

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