IOP Publishing Superconductor Science and Technology
Supercond. Sci. Technol. 31 (2018) 115008 (9pp) https://doi.org/10.1088/1361-6668/aae0e7

Process for scalable fabrication of low AC loss HTS conductors

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Received 5 July 2018, revised 25 August 2018
Accepted for publication 12 September 2018
Published 12 October 2018

Abstract

A scalable process has been developed to fabricate low AC loss cable from second generation high-temperature superconducting (2G HTS) coated conductors with an emulated Rutherford twisted conductor topology. The process uses an indexed tape design to precisely align separate YBCO tapes to form a single tape structure making it compatible with a reel-to-reel production process and involves a combination of three methods: (1) the use of laser lithography to striate 2G HTS tapes into a pattern of isolated diagonal filaments, (2) the precise alignment and decal bonding of a pattern of solder preforms to the filament edge contact areas, and (3) the alignment and bonding of a top and bottom HTS tape with a thin intervening adhesive layer that provides mechanical adhesion and electrical isolation between adjacent bonds and the interior where filament transposition occurs. The observation of a resistive critical current transition in the fully fabricated transposed striated HTS conductor indicates that all bonds were well formed and the superconducting current path was restricted to the filaments.

Supplementary material for this article is available online

Keywords: AC loss, coated conductor, high temperature superconductor, commercial production, laser lithography, filament transposition, solder bonding

(Some figures may appear in colour only in the online journal)

1. Introduction

The reduction of AC loss in second generation high-temperature superconducting (2G HTS) coated conductors is crucial for broadening their commercial use beyond DC applications and current strategies for achieving this goal include striating the HTS layer into multiple electrically-isolated thin filaments [1, 2], the Roebel arrangement [3], cable on round conductor (CORC®) [4], and combinations thereof [5, 6]. However, the emulation of a Rutherford cable configuration has the potential to yield HTS cables with the most AC versatility since it combines the AC loss reduction benefits of a striated conductor with the high frequency operation enabled by a twisted conductor with short twist pitch [7–13, 14]. This approach requires that two striated HTS tapes with slanted filaments be bonded with the filament sides facing each other separated by an insulating layer. The filaments from the two tapes must electrically connect to each other only at the edges to prevent shorting as shown in the basic diagram of figure 1.

Despite the advantages of the Rutherford configuration, the fabrication process is rather complex, thus preventing the demonstration of a method that is scalable for mass production. A summary of previous work in connecting two composite electrical tapes in the face-to-face configuration is given in table 1. There are several technical challenges associated with these methods: (1) in all cases the integrity of the bond relies on the mechanical strength of the electrical connection for adhesion; (2) the time required for diffusion bonding prevents practical scale-up; (3) the insulating layer creates a gap between the tapes that complicates the electrical bonding process; (4) the insulating layers previously used do not provide adequate isolation of adjacent filaments during solder bonding; (5) the filament widths in striated HTS tapes are typically less than a few hundred microns and openings in the insulating layer must be aligned precisely between the upper and lower filaments.

In this report we describe a process that enables the precise alignment and placement of the HTS striated tape and insulating layers by incorporating indexing holes in each constituent tape.

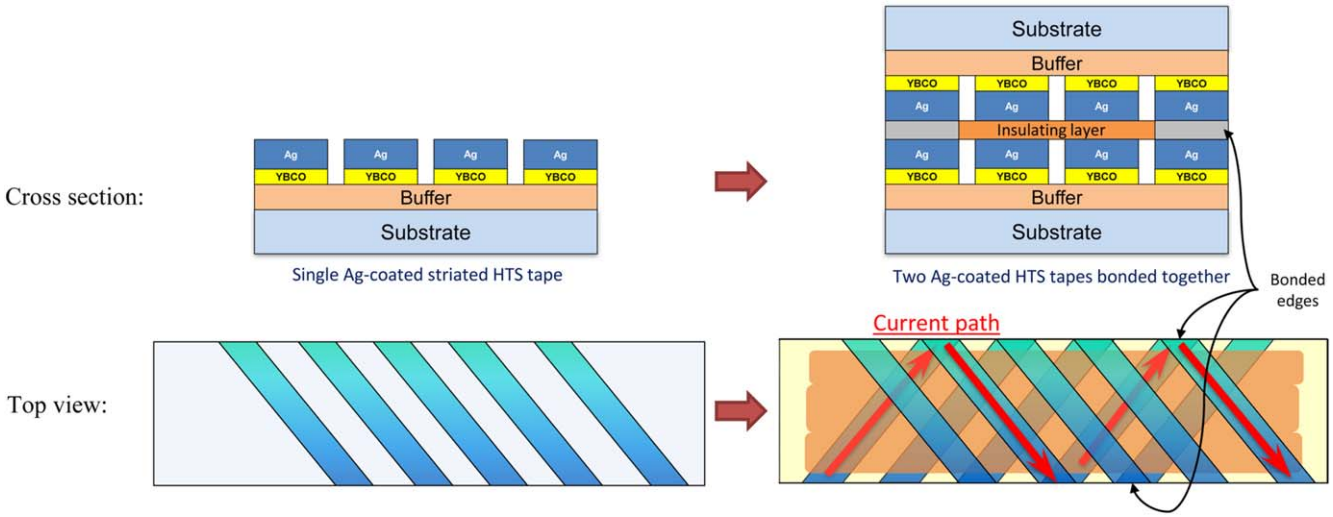

Figure 1. Diagram of the emulated Rutherford tape. The substrate is not shown in the top view for clarity.

Table 1. Summary of previous work bonding coated conductors face-to-face for low AC loss HTS cable.

	Electrical bond	Mechanical bond	Insulating layer	Bond area	R_c per bond @ 77 K
Reference [12]	Diffusion + crimping	Electrical bond	Mica thin film	0.04 cm^2	0.038 $\mu\Omega\,cm^2$
Reference [13]	Diffusion + etched mesa	Electrical bond	Photoresist	0.0025 cm^2	0.116 $\mu\Omega\,cm^2$
Reference [15]	Diffusion + hot press	Electrical bond	Kapton tape	0.375 cm^2	0.600 $\mu\Omega\,cm^2$
Reference [14]	Manual soldering (pure In)	Electrical bond	Fiber-glass epoxy tape	0.045 cm^2	0.060 $\mu\Omega\,cm^2$

It also enables reliable adhesion of the top and bottom tapes while providing containment of solder to the bond area without relying merely on electrical bonds for adhesion strength. This process is fully compatible with reel-to-reel production methods and is thus suitable for scale-up to enable the production of long lengths of emulated 2G Rutherford conductor.

2. Transposed HTS conductor fabrication

The basic components of a bonded striated tape with transposed filaments are shown in figure 2. They consist of two striated HTS tapes, an insulating double-sided adhesive (DSA) layer and solder preforms. For the laboratory demonstration an alignment jig (not shown) with index pins was used to align all of the components together. Figure 2 also displays a flow diagram giving the basic steps used to fabricate the low AC loss tape assembly. The processes shown at step level 1 are those that can be performed in parallel, independently of one another while those in step levels 2–4 are performed in sequence. The following sections discuss the fabrication of the individual components that give rise to the layers of figure 2 and give the precise details of the full assembly process. Pattern dimensions can be found in supplementary figure S1, available online at stacks.iop.org/SUST/31/115008/mmedia.

2.1. Striated HTS tape fabrication

The coated conductor tapes used in this study were taken from a 4.6 cm × 8 m long roll commercially available from AMSC's 2G HTS wire production facility. The sample architecture consisted of a 75 μm thick Ni(5at%)W RABiTS^{TM} substrate with 75 nm buffer layers of Y_2O_3, YSZ and CeO_2, deposited by reactive sputtering, and a 0.8 μm thick Dy_2O_3 doped YBCO HTS layer, deposited by a metal organic deposition process. A 3 μm thick Ag layer was deposited on both sides of the tape, which was then oxygen annealed. Samples measured by AMSC at each end of the 8 m length had I_c's (77 K, self-field) of $\sim$350 A cm^{-1} w^{-1}. These tapes were then laser cut into segments 5 and 6.7 cm in length by 1 cm in width and then patterned into multi-filament arrays using laser lithography and wet etching while the indexing holes were made by laser micromachining (see figure 3, the details of this process were previously reported in [1]).

The two striated HTS tapes and their pattern dimensions are shown in figure 2 and S1, respectively, and include several notable design features: (1) they each have 24 filaments slanted at 45° that are 190 ± 10 μm in width and which terminate in a larger pentagonal shaped area (1 mm wide, 0.477 mm^2 area) where edge bonding occurs; (2) a 1.6 mm wide border was etched free of Ag/YBCO between all patterned regions and laser machined edges to prevent possible shorting to the metallic Ni(5at%)W substrate and to remove potentially laser-damaged YBCO material; (3) the first and final few filaments terminate in large pads that allow the attachment of leads for electrical measurement across the transposed region; (4) the current lead pads of striated HTS tape #1 are solder-bonded to the extended pads on tape #2 to allow leads access to the pads on the same side. This last feature reduces shearing forces between tapes when clamping

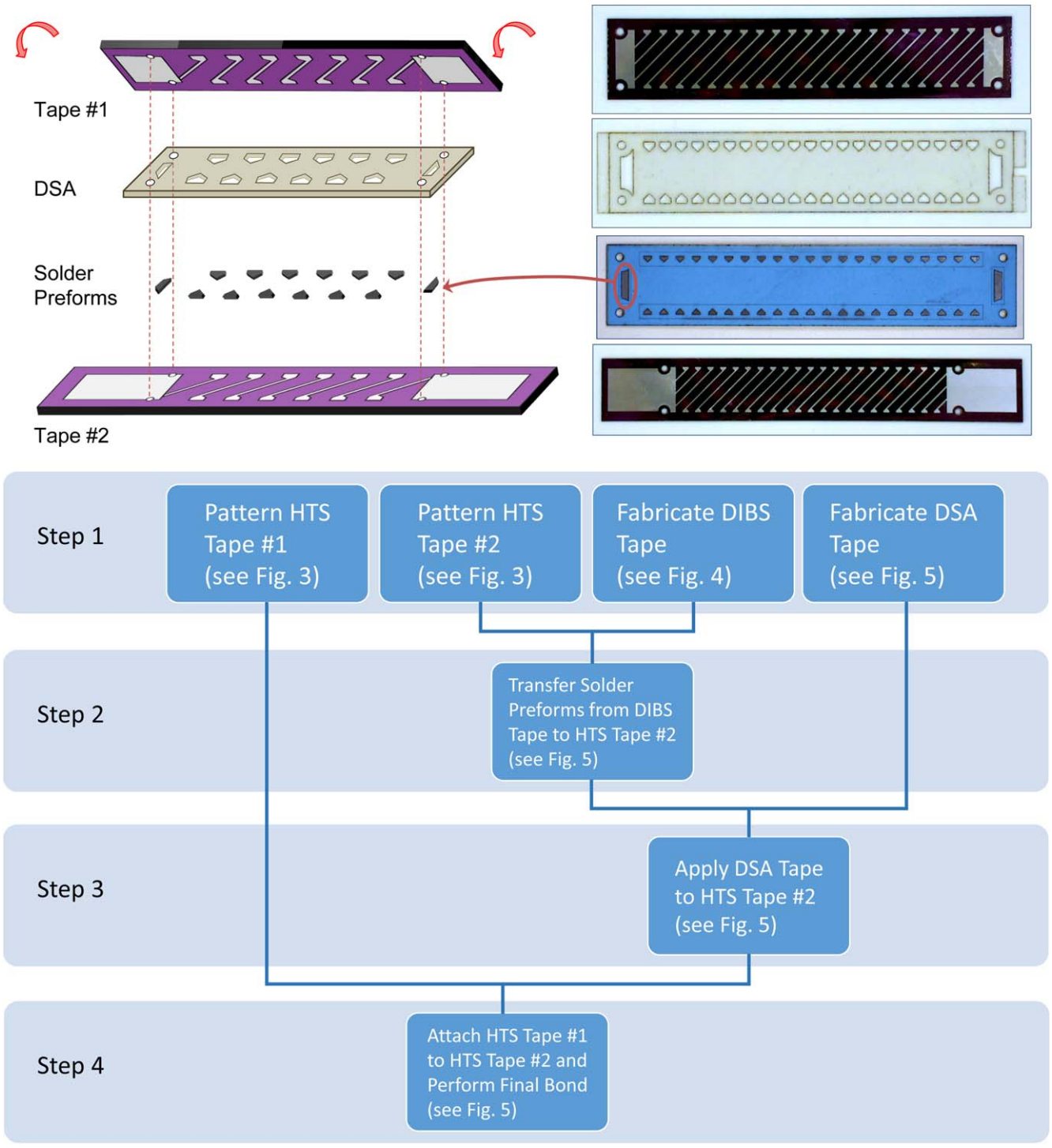

Figure 2. (Top left) Illustration of final components in assembled tape. (Top right) Actual components used to fabricate the low AC loss tape assembly. Note: double-sided adhesive (DSA) shown with backing layers present and solder preforms shown attached to blue 'low tack tape' for the decal imprinting and bonding of solder (DIBS) procedure. Note dimensions are not to scale. (Bottom) Flow diagram summarizing the basic steps to fabricating the low AC loss tape assembly.

the pads since only one side of the stacked tape structure is gripped. The filament width was chosen to be close to but not less than 150 μm since our previous work on the filament width dependence of the I_c showed that these particular tapes become sensitive to microscopic variation and drop from their nominal I_c value below $\sim$150 μm [1]. The pentagonal shape of the contacts is the result of maximizing the edge bond area (to reduce contact resistance) while maintaining a reasonable distance ($\sim$1 mm) between adjacent contact in case of solder spreading, an issue to be discussed further in 2.2 and 2.3. It is also important that the ratio of the edge contact area to the cross-sectional area of the YBCO filaments be greater than 3000 so as to not exceed the YBCO c-axis critical current [9]; the ratio of these areas in the present design is $\sim$3135.

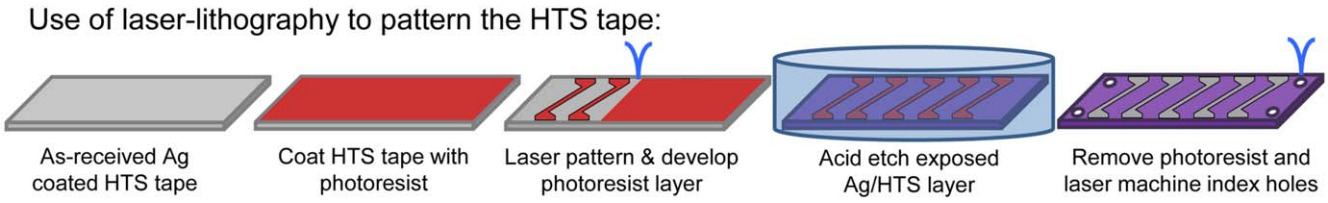

Figure 3. Simplified diagram for patterning a HTS tape by laser lithography. Full details are in [1].

While a liquid photoresist was spun on for this work, there are several techniques that are suitable for a reel-to-reel laser lithography system [16]. For example, liquid photoresists could be applied to the tape using spray or dip processes, or a solid film photoresist could be laminated to the tape. A solid film resist could be pre-patterned and pre-indexed before being applied to the tape and would simplify the setup and shorten processing time. Note that different shapes and quantities of indexing holes may be used to ensure alignment over long lengths. For example, rectangular index holes can be spaced regularly along both edges of the tape in a reel-to-reel system. The indexing holes can also be made in a separate (larger non-HTS) carrier to which the HTS tape is securely attached. This arrangement would conserve the HTS material while still taking advantage of the indexing feature.

2.2. Edge contact development

The critical factor in creating a striated tape structure is the precision bonding of narrow individual filaments from the two striated tapes to form a continuous circuit. As summarized in table 1, different methods have been used to electrically bond the filament edges from the two tapes. Three of these methods involve thermal annealing of the tapes to allow diffusion bonding across the interface of the two filament surfaces [12, 13, 15]. However, the long processing times (2–3 h), high pressures (several MPa), and in some cases the pure O_2 atmosphere [12, 15] required limit this method's practicality. In addition, to make up for the gap between the tapes caused by the inclusion of an insulating layer, the edge bonds formed by diffusion bonding require either crimping at the edges [12], etching a recessed area of the filament's silver coating in order to fill the interior region with photoresist as insulation and create a raised mesa contact area at the edge [13], or sputtering additional silver.

A more practical solution is to use a low melting temperature solder for bonding the 2G HTS coated conductors that prevents damaging or delaminating the layered structure. Several types of solder exist with different melting temperatures and resistivities at 77 K, (T_m, ρ_{77K}), such as $In_{52}Sn_{48}$ (118 °C, 12.5 $\mu\Omega$ cm), Wood's metal (70 °C, 19.3 $\mu\Omega$ cm), In_2Bi (72 °C, 39 $\mu\Omega$ cm), and $Bi_{57}In_{26}Sn_{17}$ (79 °C, 41 $\mu\Omega$ cm) [17]. We chose the In_2Bi solder because of the low melting temperature and its commercial availability in a flat ribbon form (discussed further in section 2.2.1). Measurements of single junction bonds of our HTS filaments using In_2Bi have shown that the contact resistance is 0.04 $\mu\Omega\,cm^2$, similar to that achieved with our tests using diffusion bonding (see supplementary figure S2) indicating that the minimum contact resistance is limited by the YBCO/silver interface, consistent with results reported by other groups using various solders [13, 17]. In addition, the thermal expansion of the solder between room temperature and the operating temperature is a factor that must be considered. For In_2Bi, the thermal expansion between 300 K and 77 K is approximately −0.65% while YBCO coated conductor is approximately −0.25% [18]. Despite this mismatch, we observe no delamination effects upon cooldown, which will be discussed further in section 2.3.

A simple soldering method for selectively bonding multiple isolated areas on a surface exploits the different solder wetting properties of the filament surfaces and the insulator layers (as in solder masking) so that the solder would only bond to the filament areas. This technique is traditionally used with solder pastes; however, the high temperatures needed to activate the solder flux are incompatible with 2G HTS tapes. Alternatively, either the edges of the entire tape structure can be dipped in a low melting temperature eutectic solder or a bead of solder applied to the tape edges. However, our tests have shown that the solder occasionally adheres to the insulator layer and solder bonds were inconsistent at the filaments. Even doctor blading the solder into well-defined windows over the striated tape did not produce sufficiently uniform bonds. Preventing the solder from bleeding out of the bond area and bridging to adjacent edge contacts becomes critical once their spacing reaches the order of the insulating layer thickness, since current sharing among adjacent filaments will negatively affect the transposed conduction path.

Solder preforms deliver a consistent and precise amount of solder in various shapes and sizes and are used routinely in 'pick-and-place' machines in electronics assembly lines. A reel of solder preforms of a prescribed shape and size could be used in a 'pick-and-place' machine to bond to the striated tape. However, since all the solder preforms on a reel are the same size and the preforms are individually placed onto the HTS tape, this is a serial process which may limit throughput. In addition, the 50 μm thickness of the solder preforms used on our HTS tapes is approaching the operating limits of typical 'pick-and-place' machines.

2.2.1. Decal imprinting and bonding of solder. By pre-placing solder preforms of any geometry at pre-determined locations on a release tape, the entire pattern of solder preforms can be transferred and bonded to the striated tape in a single step thereby increasing throughput. We have developed a new technique termed the decal imprinting and bonding of solder

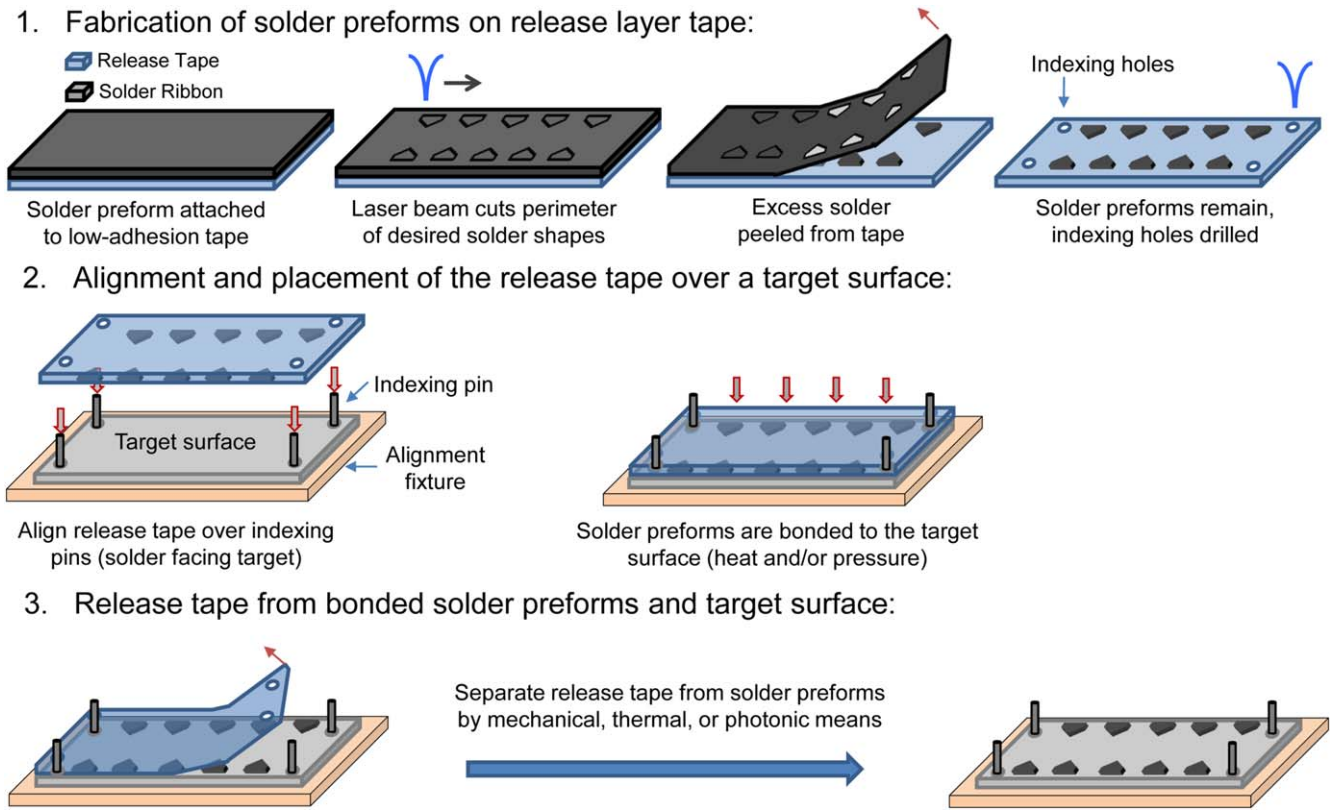

Figure 4. Step-by-step diagram of the general DIBS process.

(DIBS) process that allows any combination of size, shape and location of solder preforms to be pre-assembled on a release tape that can then be released and bonded collectively to a target surface. Note that this solder release tape can be easily adapted to a reel-to-reel system by using regularly spaced indexed holes to match the guide pins in a rotating reel.

The DIBS process consists of three primary steps as shown in figure 4—the fabrication of the solder preforms (shape and spacing) on the release tape, the alignment and placement of the release tape over a target surface, and release of the individual solder preforms from the release tape onto the target surface and their subsequent bonding to the target surface. The solder preforms can be detached from the release tape and bonded to the target surface by mechanical, thermal or photonic means.

To apply the DIBS process to the fabrication of the solder release tape for bonding the filaments in a stacked striated tape structure, a strip of semiconductor dicing tape ('low tack') was used as the support substrate for the solder preforms. Components attached to 'low tack' dicing tape can be removed mechanically. Other types of dicing tape can use heat (Nitto 'Revalpha') or UV light (DU-300) to lower its adhesion properties in order to release its attached components. A strip of dicing or release tape about the same size and shape as the target surface (striated HTS tape) was secured to a stable surface (e.g. vacuum chuck). Next, a ribbon of In_2Bi solder of fixed thickness was pressed onto the release tape. A UV ($\lambda = 355$ nm) laser beam was then focused onto the solder and perforated the perimeters of the desired solder preforms without damaging the underlying release tape. The use of a laser beam to fabricate solder preforms over a scanned area allows an arbitrary distribution and location of solder sizes and shapes on a carrier tape in contrast to the fixed tape/reel packages used in a 'pick-and-place' machine. To ensure precise alignment of the release tape (and the solder preforms) to the target surface, the same laser was used to drill indexing holes into the release tape outside the solder bonding area. The laser drilling of the index holes and the laser perforation of the solder preforms must be done in the same setup without physically disturbing the release tape. Afterwards, the solder ribbon can be carefully peeled off the release tape, leaving behind the pattern of the desired solder preforms. Figure 2 shows a finished blue 'low tack' release tape with a set of solder preforms ready for use.

This solder preform tape was then guided over the corresponding indexing pins of an alignment jig, which held the target surface, and the solder side placed over and pressed onto the target bonding surface as shown in step 1 of figure 5. Solder preforms such as In_2Bi, can be mechanically released from the dicing tape and then pressure and/or thermally treated to bond to a compatible surface in a single step. The release tape was then removed leaving behind a precisely spaced pattern of solder preforms on the pentagonal shaped contact area at the filament ends and the contact pads at the tape ends for transport measurements. Figure 6(a) shows the precision of the solder placement and the pattern dimensions, respectively. Note that additional layers or tapes with the

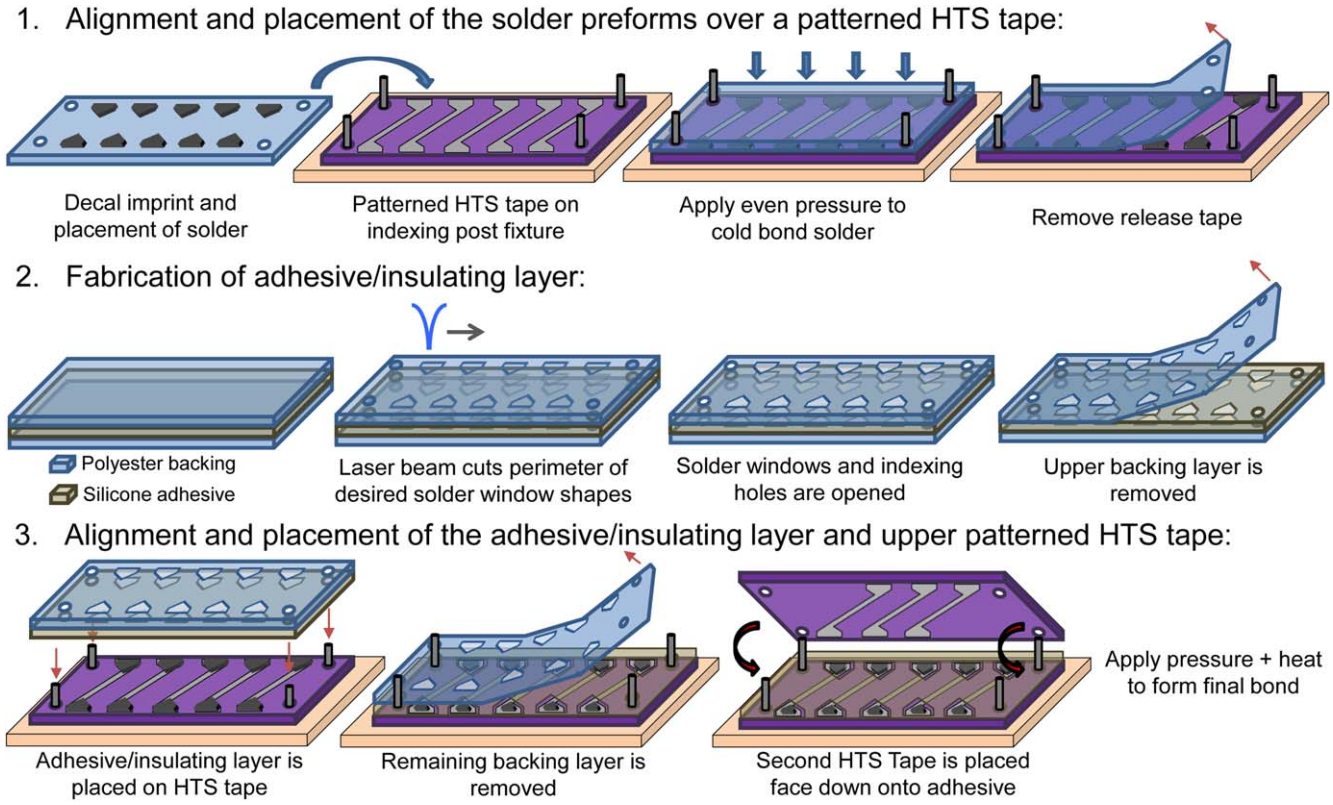

Figure 5. Step-by-step diagram of the low AC loss HTS cable fabrication process.

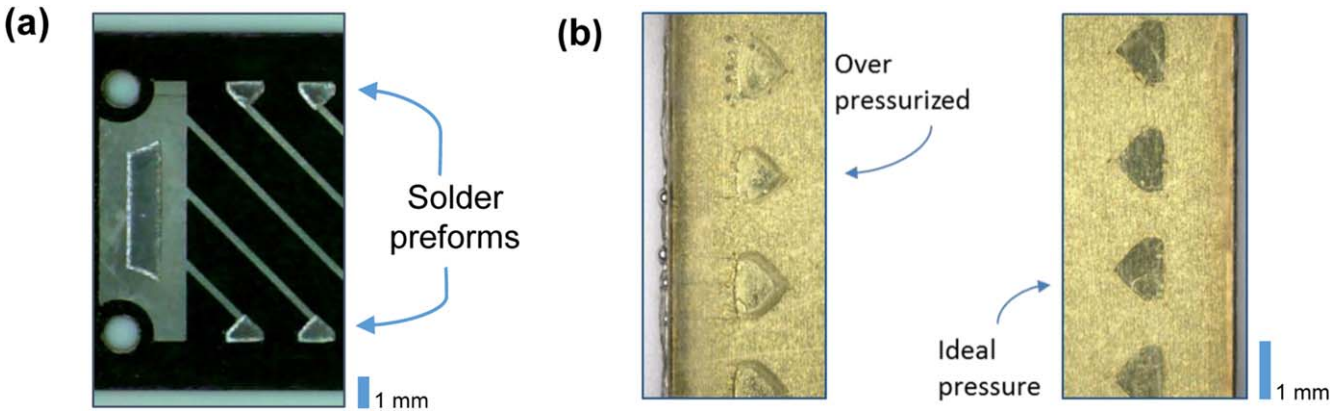

Figure 6. Photographs of (a) solder preforms bonded to a striated HTS tape before the insulator/adhesive layer application and (b) stainless steel tapes bonded to optically transparent Ultem pieces showing the effect of over-pressure versus ideal pressure on solder containment.

same pattern of indexing holes can be precisely aligned and placed over this first layer of solder preforms.

2.3. Insulating/adhesive layer

The DSA is 25 μm thick (silicone adhesive only) and initially protected by a liner on both sides. The DSA is rated for operation over a wide temperature range (−185 °C to 260 °C) but in-house testing of bonded stainless steel (SS) tapes and transport measurements of the fully fabricated HTS conductor (discussed in section 3) showed no signs of failure after numerous rapid immersions in liquid nitrogen (−195.8 °C).

Openings that coincide with the ends of the HTS filaments were laser machined through the adhesive to allow electrical connection between tapes and to restrict the flow of solder to the bonding area only. This adhesive (with one liner removed) was carefully aligned and placed over one of the HTS tapes using the alignment jig. Next, the remaining adhesive backing was removed and the top striated HTS tape was placed over the alignment jig with the filament side facing the adhesive. The liners included tabs extending beyond the adhesive layer to facilitate handling of the DSA (figure 2 (right)). For bonding the filaments in a stacked striated tape structure, the solder preforms were slightly higher than the adhesive (e.g. In_2Bi, 50 μm thick eutectic solder ribbon) and were previously placed (using DIBS) onto a bare striated HTS tape. The thickness of the adhesive and

the solder preforms were minimized to reduce electrical resistive losses. The ends of each filament could be widened to increase the solder bond area and hence lower its contact resistance.

2.4. Bonding of the stacked tape structure

The alignment jig was then placed in a press and then heat and/or pressure treated to melt the solder to provide electrical connection between the two sets of HTS filaments. During this final step the four-point resistance across the outer contacts of the longer HTS tape was monitored in real-time to determine the minimum pressure required to achieve electrical continuity. Typical heat, pressure, and time conditions were 95 °C at 50 PSI for <10 s as determined by saturation of the resistance value with time. We note that these parameters are also within the accessible range of hot-roll lamination equipment which can be readily incorporated into a reel-to-reel system.

The maximum values of the bonding parameters were deduced by bonding optically transparent Ultem pieces to surrogate SS tapes with the DSA layers and the DIBS process. Figure 6(b) shows that an over-pressure condition can result in solder squeezing out of the bond area containment windows of the DSA layer, leading to electrical shorting between filaments and/or the metal substrate. Further tests were performed by bonding SS/DSA/SS with no solder preforms to ensure no shorting between tapes occur at the edges or interior of the tapes through possible rupture points in the insulating layer.

3. Electrical transport

Although extensive testing was performed to optimize the bonding parameters, isolation of the electrical current path to the transposed filaments was difficult to verify once the HTS tapes were fully bonded and visual inspection was not possible. Since there are resistive solder bonds in series with the superconducting current path, this current could potentially be shared with other parallel paths (e.g. shorts through the buffer layer, incomplete filament isolation, solder spreading, etc) causing the critical current (I_c) value to be anomalously high. Therefore, we performed current–voltage (I–V) measurements of several fully fabricated tapes immersed in liquid nitrogen in order to observe the self-field critical current transition as a check of current path isolation. Shown in figure 7 is the I–V curve of a sample with 190 ± 10 μm wide filaments forming six parallel transposed current paths that total ~1.2 mm in width. The abrupt transition at ~36.2 A indicates a normalized I_c per-unit-width of ~302 A cm^{-1} w^{-1}, which agrees well with the expected value of 350 A cm^{-1} w^{-1} quoted by AMSC for the as-manufactured tape. Thus, the observation of this resistive critical current transition in the fully fabricated twisted striated HTS conductor indicates that all bonds are well formed and the superconducting current path is isolated to the filaments.

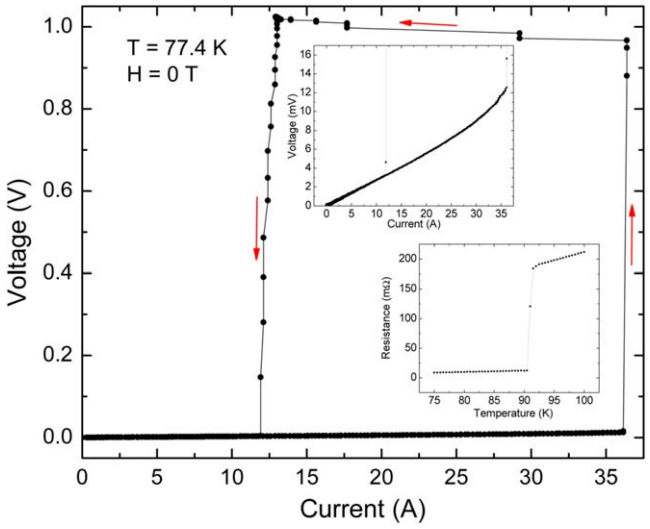

Figure 7. I–V curve in zero applied magnetic field for a fully fabricated low AC loss conductor. The hysteresis in the curve is due to Joule heating generated once the filaments enter the normal state. Upper inset: magnified view of the low voltage region of the critical current transition. Lower inset: resistance versus temperature at $H = 0$.

Upon removal from the liquid nitrogen the samples were allowed to warm to room temperature under ambient conditions (or by judicious use of a heat gun) while the resistance was monitored as a function of time, showing no discontinuities in the charted data that would indicate a broken bond due to thermal expansion (see supplementary figure S3). Three subsequent immersions and measurements of the I_c were performed which yielded repeatable results. As a final check that the sample did not incur damage from the critical current measurements, the resistance versus temperature was measured. The lower inset of figure 7 shows that a superconducting transition is still present and occurs at $T_c = 91.5$ K.

As expected, a background resistance is apparent at temperatures below T_c due to the non-persistent edge contacts. The slope of the I–V curve in figure 7 gives a total background resistance $R_T = 263.2$ $\mu\Omega$ at 77.4 K. A circuit analysis of the transposed tape stack can be modeled as six parallel paths each with eight resistive contacts in series. Assuming each contact has equal resistance, that gives a resistance per bond of $R_c = 3R_T/4 = 197.4$ $\mu\Omega$ and a contact resistance of 0.94 $\mu\Omega$ cm^2. Assuming a solder thickness equal to the insulating layer ($t = 0.002\,54$ cm) spread across the edge contact area ($A \sim 0.004\,77$ cm^2) and using the resistivity value for In_2Bi found in [19] of $\rho_s(77.4\text{ K}) = 39$ $\mu\Omega$ cm we expect a contribution of resistance from the solder of $R_s \sim 20.8$ $\mu\Omega$. The contribution from each silver contact ($t = 0.0003$ cm) using the resistivity value obtained from [18] of $\rho_{Ag}(77.4\text{ K}) \sim 0.2$ $\mu\Omega$ cm gives a combined contribution of $2R_s = 0.025$ $\mu\Omega$. Thus, after subtracting these contributions we obtain a Ag/YBCO interfacial resistance of $2R_i \sim 176.6$ $\mu\Omega$ and a contact resistance from each interface of ~0.42 $\mu\Omega$ cm^2. Although this interfacial contact resistance is higher than that found for our single filament junction

bond, it is still close to the value of 0.116 $\mu\Omega\,cm^2$ found in [13] using AMSC tapes.

Further optimization of the layer patterns and the tape bonding conditions beyond the present work are possible to reduce the edge bond resistances. For instance, the absolute contact resistance can be reduced several times by increasing the contact area ($R_c \propto 1/A$) and a small benefit could be gained by switching from In_2Bi solder to $In_{52}Sn_{48}$. The contact area can be increased in the dimension transverse to the tape's long axis but can only be increased along the length of the tape up to the spacing size between filaments. However, the most important factor is the quality and uniformity of the bond between the YBCO and its normal-metal stabilizing layer along the length and width of the coated conductor. It has been previously shown that noble metal/YBCO interfaces with contact resistances of the order of 10^{-4} $\mu\Omega\,cm^2$ are achievable through careful preparation [20]. Nevertheless, the interfacial resistance values vary considerably throughout the literature. For instance, Polák *et al* measured REBCO/Silver interfacial resistances that varied from 0.02 to 0.370 $\mu\Omega\,cm^2$ in 2G HTS tapes produced by a single manufacturer [21] while Bagrets *et al* have performed several studies that found interfacial resistances varying from 0.008 to 0.05 $\mu\Omega\,cm^2$ in tapes produced by various manufacturers [22]. Therefore, provided special care is taken during the silver coating step of the 2G HTS tape manufacturing process, an over three orders of magnitude reduction in contact resistance is still possible while using solder bonding and our fabrication technique.

4. Outlook

The scalability of the fabrication process demonstrated in this work is enabled by the compatibility and ease of adaptation of each step with a reel-to-reel process to produce the quasi-twisted, emulated Rutherford low AC loss HTS tape in a continuous manner. As previously mentioned, the components are all derived from flexible tapes that can be indexed to maintain alignment and synchronize roller rotation speed with a laser machining and patterning system. The low applied pressure, heat, and duration requirements allow component transfer, lamination, and bonding to be performed using hot-roll lamination equipment with silicone and Teflon coated rollers rather than heavy-duty rolling mill equipment that could damage the layered structure of the conductor during assembly.

To give an estimate on the throughput envisioned for such a production line, we reiterate that the fabrication and patterning of HTS tapes #1 and #2, the DSA tape, and the DIBS tape can be performed independently and at relatively high speeds for each component reel. With reels of the components pre-fabricated, the transfer of solder preforms from the DIBS tape, application of the DSA, and the attachment and final bonding of the HTS tape #1 to HTS tape #2, the total assembly process could be performed serially with each subsequent reel feeding its components into the low AC loss tape structure as it travels through the production line.

5. Summary

We have demonstrated a scalable process to fabricate a quasi-twisted, emulated Rutherford low AC loss HTS tape assembled from striated 2G HTS coated conductors. The conductor consists of two striated HTS tapes, an insulator (and adhesive) layer and solder preforms. The thin DSA minimizes the thickness of the insulating layer and therefore, the contact resistance between the upper and lower filaments and provides mechanical bonding and thermal shock resistance while the solder preforms provide electrical bonding. In combination with DIBS, our process enables the precise placement of a consistent volume of solder at the bond locations of each filament thus ensuring reliable electrical connection and eliminating interfilamentary shorting. Indexing holes and pins in the tapes also means the alignment can be maintained before and during the bonding process. Finally, the possibility of combining solder preform tape fabrication and HTS tape bonding in a single machine (reel-to-reel or roll-to-roll manufacturing) facilitates the commercialization of low AC loss HTS-based conductors. Future testing and experiments on these conductors such as mechanical shear strength, critical current versus radius of curvature, and AC loss measurements are forthcoming and will be reported in the near future.

Acknowledgments

This work was funded by the Office of Naval Research (ONR) through a direct grant and through the Naval Research Laboratory Basic Research Program. The authors would like to thank Marty Rupich of American Superconductor Corporation for supplying materials and useful suggestions to the work.

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