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A ternary memory cell using small Josephson junction arrays

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Abstract

In this paper we present a ternary cryogenic memory cell paradigm that is based on an array of inductively coupled Josephson junctions. We show how reading, writing and resetting are implemented using single flux quantum current pulse inputs to the circuit and reading voltage pulse outputs from the circuit. We further show how both destructive readout and non-destructive readout can be implemented.

Keywords: ternary memory, cryogenic memory, Josephson junction array

(Some figures may appear in colour only in the online journal)

Introduction

Superconducting digital logic circuits show promise in advancing high performance computing [1, 2]. However, design of superconducting random access memory (RAM) that can store and recall data as efficiently as logic operations take place is still a largely unsolved problem [3]. Proposed solutions to this problem include magnetic RAM designs involving using magnetic Josephson junctions [4–6], hybrid superconducting–CMOS designs [7, 8], and others [9]. The key challenges associated with developing a functional RAM are reducing power dissipation, increasing memory read/write speed, and reducing chip size [3, 9, 10].

Memory units of up to 4 kb have been demonstrated using single flux quantum (SFQ)-based designs [11–13]. However, it has been difficult to build units larger than this because of energy dissipation and memory access problems [13]. For instance, the memory cells used in the most successful cryogenic RAM designs [11, 13] are based on the vortex transition cell [14]. This cell is limited by the fact that it takes a bipolar control current (i.e. the current inputs need to have both positive and negative peaks), which requires some extra peripheral processing to interface with most unipolar cryogenic logic circuits. A RAM based on a modified unipolar vortex-transitional cell has since been proposed, however this has not been implemented [15]. Hybrid superconducting–CMOS designs interface between the SFQ circuitry and room-temperature CMOS circuitry [7, 8]. However, this approach introduces a significant amount of latency for memory access [8].

The largest source of power consumption in SFQ-based memory systems currently is known to not be simply the memory cell itself, but rather peripheral circuits that access memory [12, 13, 16, 17]. It therefore may be useful to consider designs that allow for less peripheral circuitry for memory cells. A memory cell that stores more than two states could be such a design, since it allows the same amount of peripheral circuitry to be connected to a unit however offers larger information capacity. Radix 3 number systems are theoretically the most efficient (of integer radix) for digital representation of numbers [18]. Assuming that a trit does not require more energy to operate than a bit of the same type, this means that the trit should be significantly more energy-efficient as a memory storage unit than a bit. A set of 100 bits based on three Josephson junctions can store information with a maximum Shannon entropy of $S = 100$. However, a set of 100 trits that operate with three Josephson junctions can store $S = \log_2(3^{100}) \approx 158$, which is more than 50% more information. Though it could require extra processing to use higher order memory cells, when the number of quickly accessible memory cells is the key limiting factor in design of scalable SFQ circuits [3], the ability to store more information in a single unit could be invaluable. In particular, if three (or

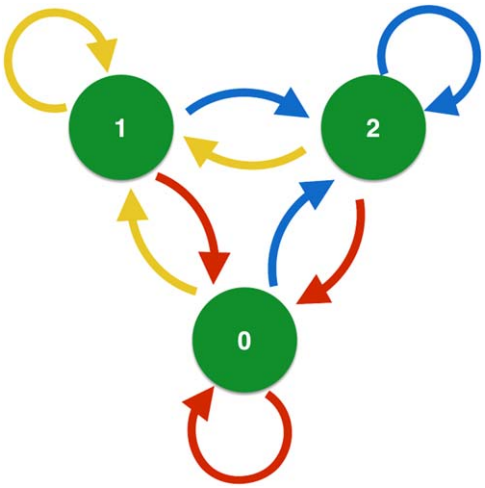

Figure 1. State transition diagram for a trit. Red arrows correspond to the 'write 0' command, golden arrows correspond to the 'write 1' command, and blue arrows correspond to the 'write 2' command. Each state is accessible from any other state and can overwrite itself.

more) states could be accessed with the same speed and delay at which two are normally accessed, incorporating higher order memory cells would also increase speed of memory access. Cryogenic ternary memory units [19, 20] and peripheral circuitry based on these units [21] have been proposed for Josephson junctions, however these are not currently being developed.

As it is becoming increasingly difficult [22] to shrink the size of the memory cell by developing more advanced fabrication techniques, it may be useful to consider an alternative approach to increasing memory density by encoding more than one bit of information on a single memory cell. Multi-valued memories have been proposed and studied [23] employing a variety of technologies such as resonant tunneling diodes [24–26], single-electron-based flexible multi-valued logic gates, such as single-electron transistors [27], memristor-based devices [28], and interconnected lasers [29]. Memory cells with as many as nine states have been demonstrated and studied (e.g. resonant tunneling diode memory was demonstrated in [26]).

In this paper, we present a ternary memory cell paradigm that is based on three coupled Josephson junctions. We show how a memory cell can be designed and present the dynamics of the cells using WRspice simulations [30]. This cell is very similar in design to recently published binary memory designs [31–33]. Reading and writing can be performed using SFQ pulses to change memory states and trigger voltage output from the cell for reading the state.

The cell we present operates such that it is possible to access any state from any other state with a single pulse. A diagram of the states and possible transitions between the states is shown in figure 1. The memory cell is such that in order to write a state into the cell, it is not necessary to know the previous state of the cell. Further, we will show that reading the state can be accomplished by writing '0.'

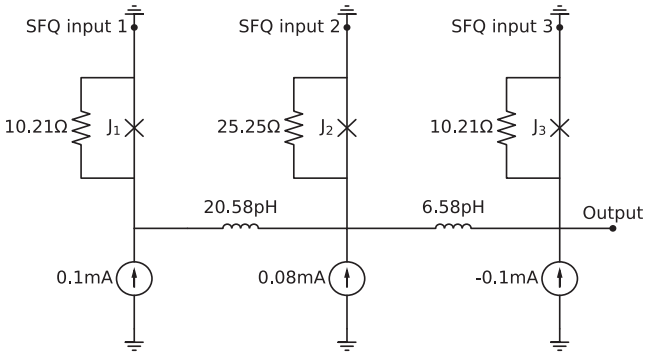

Figure 2. A ternary memory cell based on three inductively coupled Josephson junctions. The appropriate inputs for this circuit are SFQ pulses of 2 ps width. Note that the shunt resistances $R_{s,j}$ specify only the *added* parallel resistances to the junctions, which include default resistance and capacitances.

Memory cell operations

In figure 2 we present the schematic of the ternary memory cell. In this system, the component parameters are chosen in agreement with the SFQ5ee process [34]. The junction diameter is 1 μm^2 so that the critical current is $I_c = 0.1$ mA, the gap voltage is $\Delta V = 2.5$ mV, the sub-gap resistance is $R_{sg} = 144\ \Omega$, the junction resistance is $R_N = 16\ \Omega$, and the junction capacitance is $C_N = 0.07$ pF. This circuit is designed for SFQ pulses with 2 ps pulse-width as the inputs. State transitions between 0, 1, and 2 states are achieved by sending SFQ pulses into the input terminals.

The dynamics of voltage across a small Josephson junction of the type we consider in this paper follow the resistively shunted junction model:

$$C_N\frac{dV}{dt} + \frac{1}{R(V)}V + I_c\sin(\phi) = C_N\frac{\hbar}{2e}\ddot{\phi} + \frac{\hbar}{2eR(V)}\dot{\phi} + I_c\sin(\phi) = I_{\text{in}}, \tag{1.1}$$

where $R(V)$ is a piecewise linear resistance [35]:

$$R(V) = \begin{cases} \dfrac{R_sR_{sg}}{R_s + R_{sg}} & \text{if } V < \Delta V \\ \dfrac{R_sR_N}{R_s + R_N} & \text{if } V > \Delta V \end{cases}.$$

The inductive coupling shown in figure 2 is part of the I_{in} term in equation (1.1). The current from junction j into junction i is then

$$I_{ij} = \frac{1}{L_{ij}}\int (V_j - V_i)\mathrm{d}t = \frac{\hbar}{2eL_{ij}}\int(\dot{\phi}_j - \dot{\phi}_i)dt = \frac{\hbar}{2eL_{ij}}(\phi_j - \phi_i), \tag{1.2}$$

so that the junctions are coupled by their phase differences

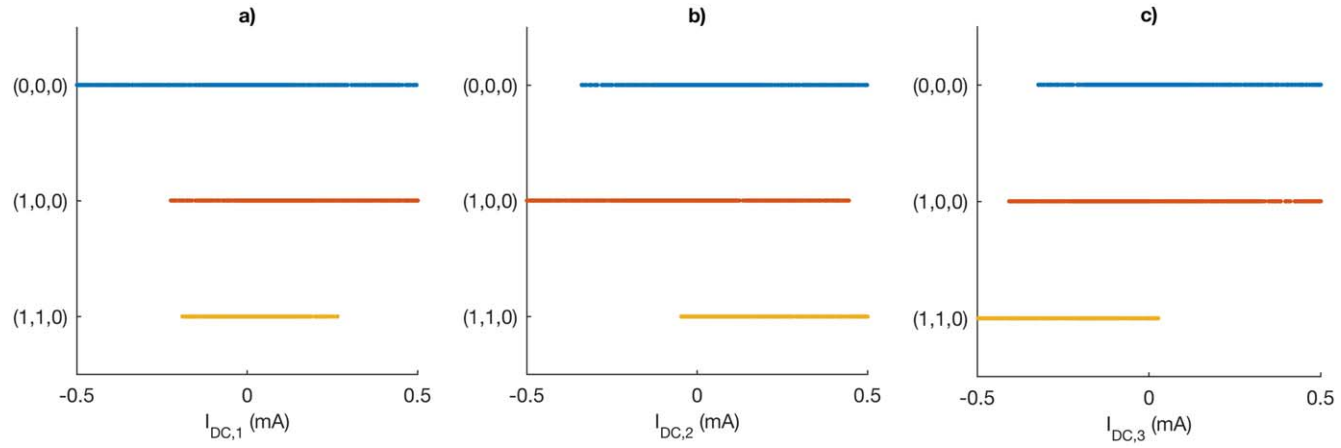

Figure 3. Regions of stability are plotted for three states as the DC bias current is varied (one at a time) for each junction. The parameters we have chosen ($I_{\mathrm{DC},1} = 0.1$ mA, $I_{\mathrm{DC},2} = 0.08$ mA, and $I_{\mathrm{DC},3} = -0.1$ mA) are such that small variances in DC (on the order of 0.05 mA) should not destabilize any state.

Table 1. Parameters of fixed-point states of the circuit.

State label	(n_1, n_2, n_3)	$\phi_1/2\pi$	$\phi_2/2\pi$	$\phi_3/2\pi$	Current across L_1	Current across L_2	Write command
0	(0, 0, 0)	0.1757	0.0691	−0.0858	10.71 μA	48.66 μA	2 ps SFQ pulse to input 3
1	(1, 0, 0)	1.0251	0.1857	−0.0446	84.32 μA	72.36 μA	2 ps SFQ pulse to input 1
2	(1, 1, 0)	1.1248	0.8321	0.2071	29.40 μA	196.38 μA	2 ps SFQ pulse to input 2

such that the full equations of motion are:

$$
\begin{aligned}
&C_{N,1}\frac{\hbar}{2e}\ddot{\phi}_1 + \frac{\hbar}{2eR_1(V)}\dot{\phi}_1 + I_c\sin(\phi_1) = I_{\mathrm{in},1} + I_{\mathrm{DC},1} \\
&+ \frac{\hbar}{2eL_{12}}(\phi_2 - \phi_1) \\
&C_{N,2}\frac{\hbar}{2e}\ddot{\phi}_2 + \frac{\hbar}{2eR_2(V)}\dot{\phi}_2 + I_c\sin(\phi_2) = I_{\mathrm{in},2} + I_{\mathrm{DC},2} \\
&+ \frac{\hbar}{2eL_{12}}(\phi_1 - \phi_2) + \frac{\hbar}{2eL_{23}}(\phi_3 - \phi_2) \\
&C_{N,3}\frac{\hbar}{2e}\ddot{\phi}_3 + \frac{\hbar}{2eR_3(V)}\dot{\phi}_3 + I_c\sin(\phi_3) = I_{\mathrm{in},3} \\
&+ I_{\mathrm{DC},3} + \frac{\hbar}{2eL_{23}}(\phi_2 - \phi_3),
\end{aligned}
\tag{1.3}
$$

where $I_{\mathrm{in},i}$ is the current from the SFQ input shown in figure 2 and $I_{\mathrm{DC},i}$ is the bias current. The memory states for this memory cell are fixed-point solutions of (1.3). Each state is a solution of junction phases (ϕ_1, ϕ_2, ϕ_3) such that the currents through the coupling inductors, as described in (1.2) is non-zero. The memories are therefore stored as states of the zero-voltage super-current circulating between the junctions.Since the fixed-point states are stable at zero-voltage (below the gap voltage), we can simply use the sub-gap resistance and shunt resistance values instead of the piecewise linear resistance function (which is still included in all simulations in this paper). We can therefore consider the simplified non-dimensionalized equations shown in equation (1.4). The non-dimensional equations of motion for this system are then:

$$
\begin{aligned}
&\ddot{\phi}_1 + \gamma_1\dot{\phi}_1 + \sin(\phi_1) = i_{\mathrm{DC},1} + i_{\mathrm{in},1} + \kappa_1(\phi_2 - \phi_1) \\
&\ddot{\phi}_2 + \gamma_2\dot{\phi}_2 + \sin(\phi_2) = i_{\mathrm{DC},2} + i_{\mathrm{in},2} + \kappa_1(\phi_1 - \phi_2) \\
&+ \kappa_2(\phi_3 - \phi_2) \\
&\ddot{\phi}_3 + \gamma_3\dot{\phi}_3 + \sin(\phi_3) = i_{\mathrm{DC},3} + i_{\mathrm{in},3} + \kappa_2(\phi_2 - \phi_3),
\end{aligned}
\tag{1.4}
$$

where the non-dimensionalized parameters are $\kappa_i = \frac{\hbar}{2eI_cL_i}$, $i_{\mathrm{DC},i} = I_{\mathrm{DC},i}/I_c$, $\gamma_i = \sqrt{\frac{\hbar}{2eI_cC_N}}(R_{sg}^{-1} + R_{s,i}^{-1})$. The time-derivatives are with respect to the non-dimensionalized time $\tau = \sqrt{\frac{2eI_c}{\hbar C_n}}t$. To find the fixed-points, we can set the derivatives and time-dependent terms to zero and solve for solutions (ϕ_1, ϕ_2, ϕ_3):

$$
\begin{aligned}
&\sin(\phi_1) = i_{\mathrm{DC},1} + \kappa_1(\phi_2 - \phi_1) \\
&\sin(\phi_2) = i_{\mathrm{DC},2} + \kappa_1(\phi_2 - \phi_1) + \kappa_2(\phi_3 - \phi_2) \\
&\sin(\phi_3) = i_{\mathrm{DC},3} + \kappa_2(\phi_2 - \phi_3).
\end{aligned}
\tag{1.5}
$$

The stable solutions of (1.5) are the memory states. For our parameters, there are three exponentially stable states. A state for this system can be defined by a vector of three integers, one for each junction,(n_1, n_2, n_3) where the phase of the ith junction is $\phi_i = 2\pi n_i + \theta_i$. Here, $|\theta_i| < \pi$ such that θ_i is the phase of the ith junction relative to its own sinusoidal potential well [16, 29]. In this paper, we will consider three stable states: (0, 0, 0), (1, 0, 0), and (1, 1, 0). We will denote the (0, 0, 0) state as '0,' the (1, 0, 0) as '1,' and the (1, 1, 0) state as '2.'

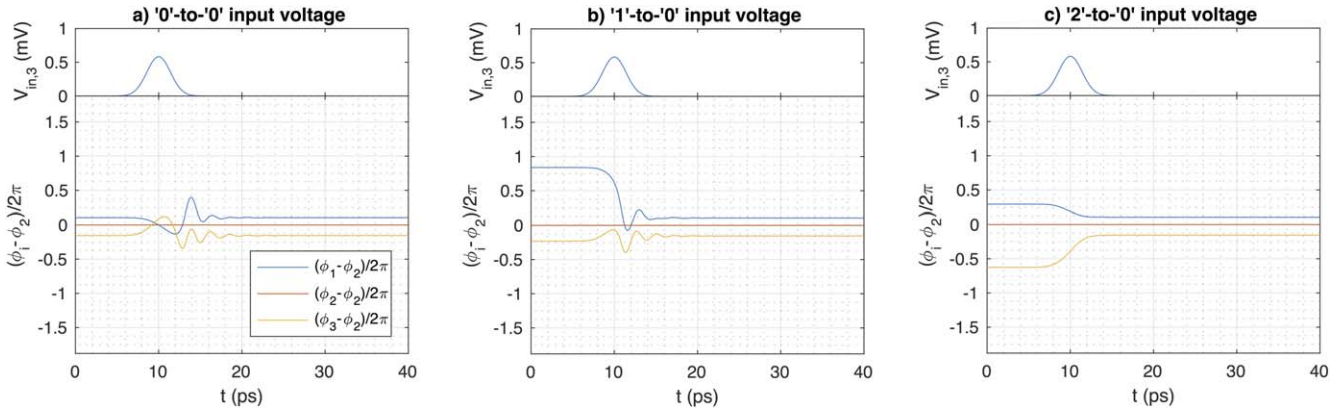

Figure 4. The input voltages are plotted above the phases relative to that of the second junction for the command to write '0.' Writing '0' is accomplished by sending an SFQ pulse into the third junction in the circuit. The time-series are generated from WRSpice simulations.

We present the details of these solutions in table 1 (calculated by numerically solving (1.5)). Determining stability of a solution is done by diagonalizing the Jacobian matrix of (1.4) evaluated at the solution and checking if the eigenvalues have negative real part. The solutions we describe all can be shown to be exponentially stable.

Each of the fixed-points in table 1 is robust to moderate variations in bias current. In order to be physically realizable the solutions must exist if there are small errors in current. However, when there is a spike in bias current (as in a read or write function) the solutions should destabilize so that the state can change. We show how the solutions become unstable with variations in bias currents in figure 3. The DC current parameters we have chosen for this system ensure that if the DC currents vary within 50% of their values, the three states should exist and be stable.

To write the '0' state, a 2 ps SFQ pulse is sent into the SFQ input 3 (i.e. the right-most junction). In figure 4, we show results from WRspice simulations of how the 2 ps SFQ pulse changes the phase relationships between the three junctions. We plot the phase differences with respect to that of the second (center) junction (scaled by 2π). In 4(a) the initial condition of the circuit is the '0' state, where there is 10.71 μA stored in L_1 and 48.66 μA stored in L_2 and all junctions are in the zero phase potential well, i.e. the state is (0, 0, 0). When a pulse is sent to the third junction, there is transient behavior in the circuit, but the state does not change. In 4(b), the initial condition of the circuit is the '1' state, where there is 84.32 μA in L_2 and 72.36 μA in L_2 and the first junction has a phase of approximately 2π with respect to the other two junctions, i.e. the state is (1, 0, 0). When a pulse is sent to the third junction, the transient behavior results in a change of state back to the '0,' which is (0, 0, 0). In 4(c), the initial condition of the circuit is in the '2' state, where there is 29.40 μA in L_2 and 196.38 μA in L_2 and the first two junctions have approximately 2π phase difference with respect to the third junction. When a pulse is sent to the third junction, the third junction's phase is shifted by approximately 2π resulting in a change of state to the (0, 0, 0) or '0' state.

To write the '1' state, a 2 ps SFQ pulse is sent into the SFQ input 1 (i.e. the left-most junction). In figure 5, we show how the 2 ps SFQ pulse changes the phase relationships between the three junctions. In 5(a) the initial condition of the circuit is the (0, 0, 0) or '0' state, where the phases are all close to zero. When a pulse is sent to the first junction, the phase in the first junction is shifted by approximately 2π and the state changes to the (1, 0, 0) or '1' state. In 5(b), the initial condition of the circuit is the '1' state. When a pulse is sent to the first junction, there is transient behavior, but it does not result in a change of state. In 5(c), the initial condition of the circuit is in the (1, 1, 0) or '2' state. When a pulse is sent to the first junction, the transient behavior results in a change of state to the (1, 0, 0) or '1' state.

To write the '2' state, a 2 ps SFQ pulse is sent into the SFQ input 2 (i.e. the middle junction). In figure 6, we show how the 2 ps SFQ pulse changes the phase relationships between the junctions in the circuit. In 6(a) the initial condition of the circuit is the '0' state. When a pulse is sent to the middle junction, the phase of the second junction is shifted by approximately 2π and the phase of the first junction follows, leading to the (1, 1, 0) or '2' state. In 6(b), the initial condition of the circuit is the '1' state. When a pulse is sent to the middle junction, the phase of the junction is shifted by approximately 2π placing the system into the (1, 1, 0) or '2' state. In 6(c), the initial condition of the circuit is already in the '2' state. When a pulse is sent to the middle junction, there is transient behavior, but it does not lead to a state change.

A destructive read function can be implemented by simply using one of the write functions. It is possible to use any of the three write functions as a read function, but it seems like using the write '0' command is optimal since it results in output pulses of the largest variety. We show the outputs (i.e. the voltage measured at the output node of the circuit) of WRspice simulations for reading using each of the write commands in figure 7.

In order for this system to be suitable for computing, the energy of switching should be sufficiently low. We can calculate the switching energy for a state transition using the following integral:

$$E_{\text{switch}} = \sum_{j=1}^{3} \int_{\text{state1}}^{\text{state2}} |V_j||I_j| \, dt.$$

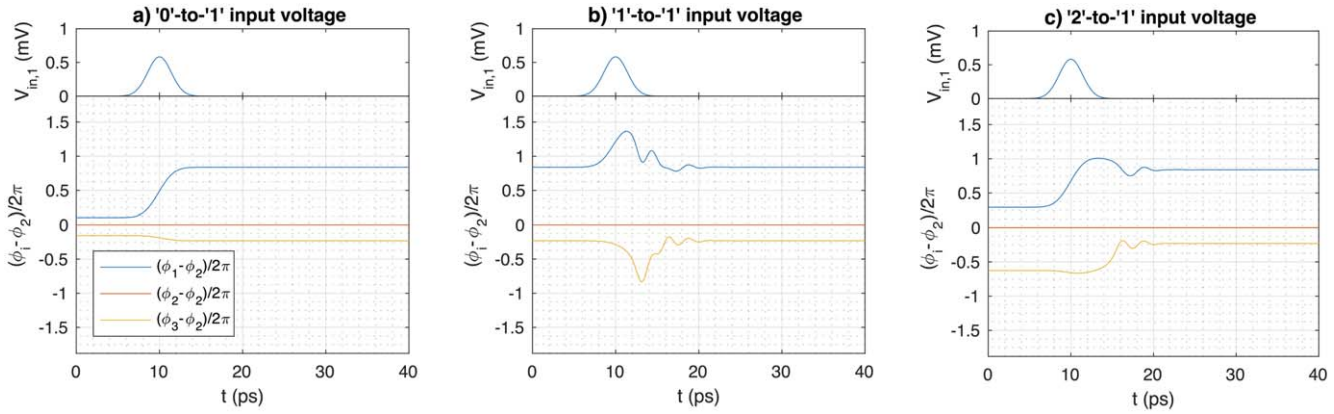

Figure 5. The input voltages are plotted above the phases relative to that of the second junction for the command to write '1.' Writing '1' is accomplished by sending an SFQ pulse into the first junction in the circuit. The time-series are generated from WRSpice simulations.

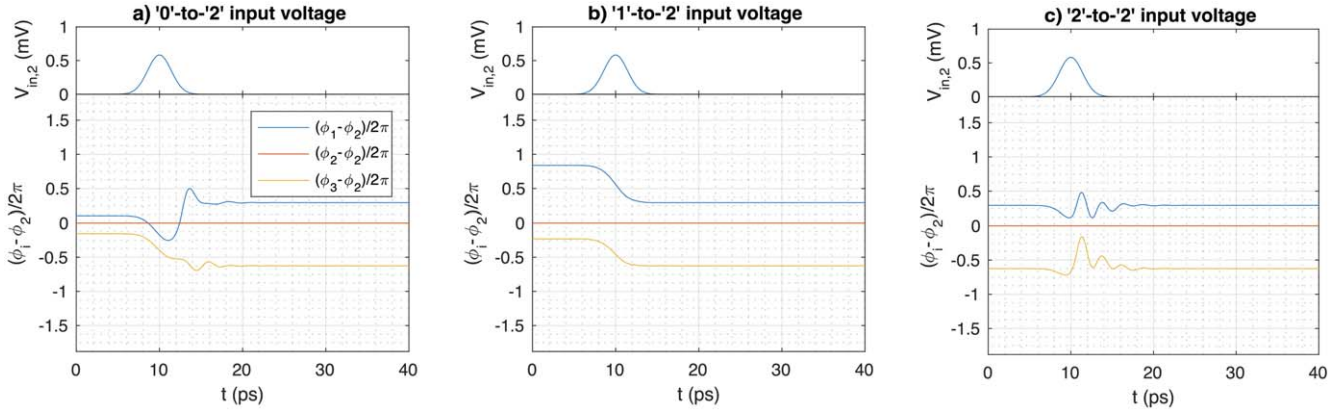

Figure 6. The input voltages are plotted above the phases relative to that of the second junction for the command to write '2.' Writing '2' is accomplished by sending an SFQ pulse into the middle junction in the circuit. The time-series are generated from WRSpice simulations.

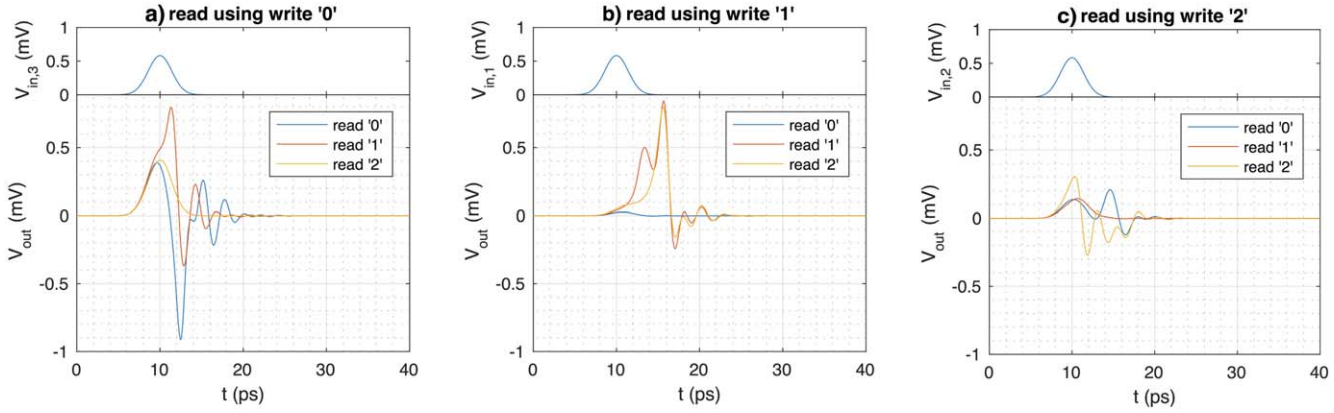

Figure 7. The input voltages are plotted above the resulting output voltages. In (a) a 2 ps SFQ pulse is sent into the third junction for the write '0' command and the output is plotted for simulations with initial condition in the '0,' '1,' and '2' states. In (b) a 2 ps SFQ pulse is sent into the first junction for the write '1' command and the output is plotted for simulations with initial condition in the '0,' '1,' and '2' states. In (c) a 2 ps SFQ pulse is sent into the second junction for the write '2' command and the output is plotted for simulations with initial condition in the '0,' '1,' and '2' states.

We numerically calculated the integral from WRSpice simulations. The energies are presented in the table 2. Note that these energy values are the measures of the energy dissipated during the switching process in the circuit.

We also numerically calculated the access times for switching between the states. This was done by measuring the time between the start of a pulse (taken to be 15 ps before the pulse center for a 2 ps pulse) and the end of transient behavior in the circuit. The end of transient behavior is numerically defined here to be when current values across the inductors have permanently reached within 0.1 μA of their steady-state values for the end state.

Table 2. Numerically calculated access energies for all possible state transitions of the circuit. These values were calculated from WRspice simulations.

	Write '0'	Write '1'	Write '2'
Start '0'	0.2128 aJ	0.1061 aJ	0.1215 aJ
Start '1'	0.2128 aJ	0.0407 aJ	0.0959 aJ
Start '2'	0.0819 aJ	0.0675 aJ	0.1872 aJ

Table 3. Numerically calculated access times for all possible state transitions of the circuit. These values were calculated from WRspice simulations.

	Write '0'	Write '1'	Write '2'
Start '0'	32.6 ps	20.3 ps	32.4 ps
Start '1'	30.2 ps	32.5 ps	22.2 ps
Start '2'	21.0 ps	32.6 ps	32.7 ps

We would like to note that the access time and access energy values presented in tables 2 and 3 are not optimized values, and perhaps lower access times and access energies can be achieved by optimizing the circuit parameters and developing control methodologies for transitions between the memory states [36].

Non-destructive readout (NDRO)

In this section we show the principles of how to implement a NDRO for a ternary memory cell. The NDRO principle is based on the premise that the output voltage amplitudes in response to the applied to the memory cell pulses will be different for each memory state, even if the pulse amplitude is too small to change the memory state. Consequently, these differences can be recorded and distinguished by a circuit that reads the output voltages. Dependent on the system parameters, the output voltage amplitude differences for different memory states could be small but distinguishable and parameter optimization is required to optimize the cell to its best optimal performance.

The memory cell circuit is shown in figure 8. This circuit is almost the same circuit as presented in figure 2, except it has a fourth input. The resistor between the input and the circuit leads to an attenuation of the input pulse such that the pulse is not strong enough to destabilize the state of the system. The non-destructive read is accomplished by sending an SFQ pulse of 2 ps width (the same as used for write functions) into the input labeled 'SFQ input 4.'

The NDRO works by disturbing the system with a voltage pulse. However the pulse is attenuated by the resistor R_{read} so that it is not large enough to cause any full phase rotations of the junction phases. The behavior of the circuit is plotted in figure 9. When the read pulse is sent, the state (i.e. the current stored in the inductors) does not change after a transient disturbance period.

To show that the NDRO works as an operational read function, we plot the output voltages measured from the 'Output' node in figure 10. From each state, the output voltage has unique amplitude. This ensures that it is possible to read each state without disturbing the state itself. This NDRO is perhaps simpler to implement than the destructive readout (DRO) for the ternary circuit since each output voltage function has unique amplitude.

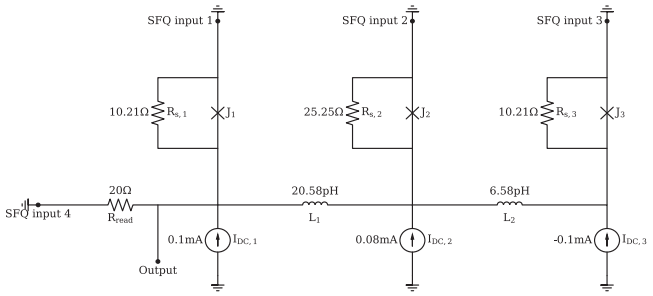

Figure 8. A ternary memory cell with NDRO is shown. Write functions and '0,' '1,' and '2,' states are the same as in the DRO circuit, however the read function and the output node is different. Reading is accomplished by sending an SFQ pulse (2 ps width) into the point labeled 'SFQ input 4.'

Conclusions

We have shown a simple energy-efficient design paradigm for a ternary Josephson junction-based memory cell, described how it operates, and presented the principles upon which it operates. Memory is stored via Josephson junction array phase state combinations (which physically means storing memory states via super-current in the inductors between the Josephson junctions). Writing a state is accomplished by sending an SFQ pulse into one of the inputs of the cell. Reading can be accomplished by measuring the output voltage when applying a pulse to any one of the three states. Implementation of the ternary memory cell peripheral circuits or variants of this type of circuit can be done within the framework of traditional SFQ-based cryogenic circuits. Since the inputs are simply SFQ pulses, one can use existing RSFQ circuit libraries [2] for the peripheral circuits. As we have further described a design paradigm for a NDRO for the ternary system, the next step towards implementation would be increasing the contrast between the states in the analog readout to allow for even larger fabrication irregularities. We believe, that this challenge can be solved by employing a parameter optimization technique on the entire circuit (including the peripherals), possibly similar to the techniques that we have implemented for a binary memory cell [31].

Using principles we have described in this paper, memory cells with larger numbers of states (i.e. *N*-array memory) can similarly be designed. For example, a 4 state memory cell using three junctions would double the memory density of a circuit that uses binary memory cells. Higher-state memory cells could be beneficial not only to minimize of interconnects and associated bias currents, but also to maximize memory density in a circuit with a limited number of Josephson junctions.

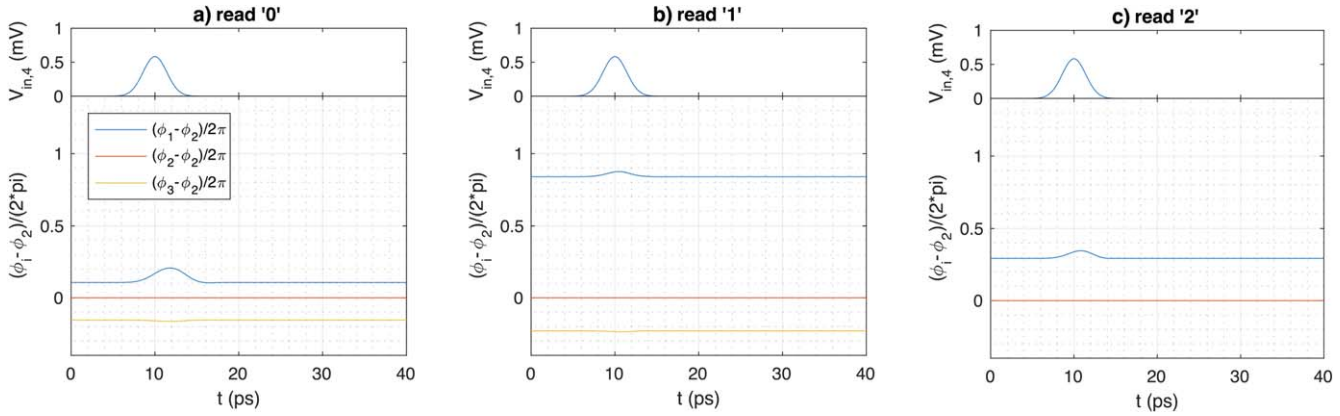

Figure 9. The input voltages are plotted above phases relative to that of the second junction. In each plot, an SFQ pulse is sent into the read input node. In (a) the cell is in the '0' state. In (b) the cell is in the '1' state. In (c) the cell is in the '2' state. Note that the states do not change when the pulse is sent. The read function is therefore non-destructive.

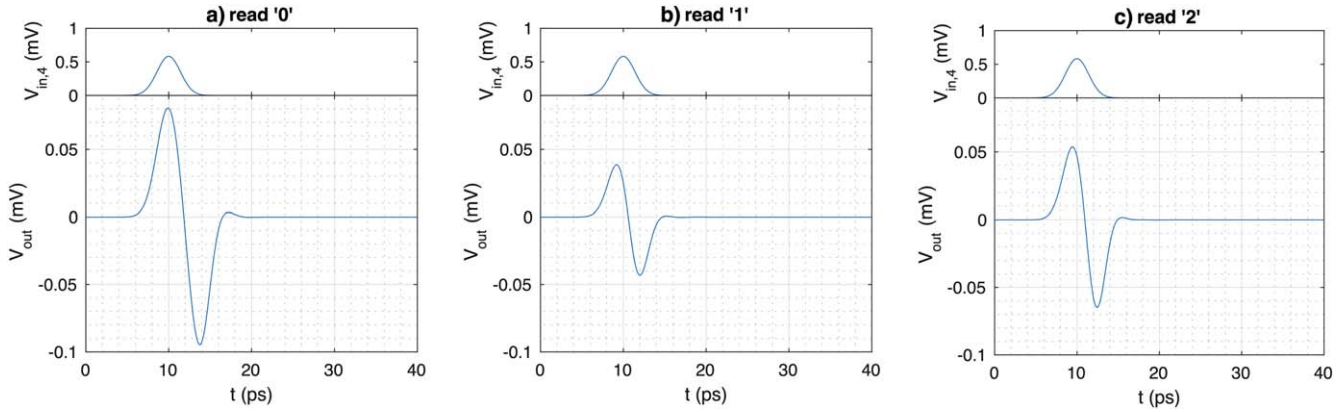

Figure 10. The input voltages are plotted above the resulting output voltages. In each plot, an SFQ pulse is sent into the read input node. In (a) the cell is in the '0' state. In (b) the cell is in the '1' state. In (c) the cell is in the '2' state. Note that the resulting output voltage amplitude is different for each state. This ensures that this read function works correctly.

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