OPEN ACCESS
IOP Publishing
Superconductor Science and Technology
Supercond. Sci. Technol. **31** (2018) 105003 (7pp)
https://doi.org/10.1088/1361-6668/aad78d

Design methodology of single-flux-quantum flip-flops composed of both 0- and π-shifted Josephson junctions

Yuki Yamanashi[1,2], Sotaro Nakaishi[1], Akira Sugiyama[1], Naoki Takeuchi[2,3] and Nobuyuki Yoshikawa[1,2]

[1] Department of Electrical and Computer Engineering, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan
[2] Institute of Advanced Sciences, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan
[3] PRESTO, Japan Science and Technology Agency, 4-1-8 Honcho, Kawaguchi, Saitama 332-0012, Japan

E-mail: yamanashi-yuki-kr@ynu.ac.jp

Received 1 June 2018, revised 24 July 2018
Accepted for publication 2 August 2018
Published 28 August 2018

Abstract

A methodology for designing single-flux-quantum (SFQ) flip-flops composed of both conventional (0-) and π-shifted Josephson junctions is investigated. We investigated the implementation of a storage loop, which can store flux quantum and is indispensable to express binary logic states in superconductor logic circuits. As all SFQ flip-flops have storage loops, the investigated design methodology can be applied to their design. We designed several SFQ flip-flops composed of 0- and π-shifted Josephson junctions using the investigated design methodology. The performances of the designed SFQ flip-flops were quantitatively evaluated by using an analog circuit simulator which we developed. We confirmed the correct operation of various SFQ flip-flops composed of 0- and π-shifted Josephson junctions with wide operating margins. Moreover, we observed that the investigated design methodology is suitable for SFQ flip-flops with complementary outputs because a storage loop composed of both 0- and π-shifted Josephson junctions has a symmetric structure and the complementary output function can be realized by using the storage loop. Our investigation indicates that the number of Josephson junctions and static power consumption of a non-destructive read-out flip-flop with complementary outputs (NDROC) can be reduced to less than half of those of the conventional NDROC, which has two storage loops composed of 0-Josephson junctions, to realize the complementary output function. The investigated design methodology is expected to be applied to not only SFQ circuits but also other superconducting logic circuits and novel reconfigurable logic devices using programmable 0-π Josephson junctions.

Keywords: SFQ circuit, flip-flop, π-shifted Josephson junction, circuit simulator, circuit design methodology

(Some figures may appear in colour only in the online journal)

1. Introduction

As the end of Moore's law approaches, beyond-CMOS (complementary metal–oxide–semiconductor) devices have been attracting attention [1, 2]. Such devices can overcome the physical limitations of semiconductor CMOS devices.

Superconducting logic devices are one of these candidates, owing to their high operation speed and extremely high energy efficiency [3–6].

A conventional Josephson junction (0-JJ herein) [7, 8], where the flowing superconducting current is related to the phase difference between two superconducting electrodes comprising the 0-JJ, is the most fundamental element of superconducting circuits such as a single-flux-quantum (SFQ) circuit [9, 10], quantum flux parametron [11, 12], and reciprocal quantum logic circuit [13]. To improve the performances of superconducting circuits, the introduction of π-shifted JJs (π-JJs) into superconducting circuits has been investigated [14, 15]. The current–phase relationship of a π-JJ is expressed as

$$I = I_C \sin(\theta + \pi) = -I_C \sin\theta, \quad (1)$$

where I is the current, I_C is the critical current of the π-JJ, and θ is the gauge-invariant superconducting phase difference between the two superconducting electrodes of the π-JJ.

Superconducting loops that contain 0-JJs are used to express the binary logic states of a superconducting circuit. In the case of conventional SFQ flip-flops, the existence and absence of flux quantum in the superconducting loop, called a storage loop, represents the internal logic states of the flip-flops. The bias current is asymmetrically injected into the storage loop to realize the bistable energy potential of the storage loop, which is indispensable to the implementation of SFQ flip-flops [16].

In contrast, bistable energy potential can be realized using a superconducting loop containing a π-JJ without applying bias current to the loop [16]. Consequently, the static power consumption of the SFQ circuit can be reduced by introducing π-JJs into the circuits [15–18]. Furthermore, we can implement dense superconducting circuits by using π-JJs because the large inductance required by the storage loop can be replaced with a π-JJ, which has an intrinsic π phase shift [17, 19]. A superconducting quantum interference device composed of π-JJs can also be utilized as a superconducting flux quantum bit that does not require magnetic flux bias [20–22].

Thus far, π-JJs with a superconductor–ferromagnet–superconductor (SFS) tunnel junction structure suitable for integrated circuit applications have been implemented [23–25]. The operation of small-scale SFQ circuits composed of 0-JJs and SFS π-JJs has been demonstrated [26]. The fabrication processes required for implementing SFS π-JJs with high uniformity have been investigated for large-scale integrated circuit applications [27, 28]. Programmable SFS Josephson junctions, where the 0- and π-states can be switched, have been experimentally demonstrated [29, 30].

Among various superconducting SFQ flip-flops, only a toggle flip-flop (TFF) has been investigated and implemented by using π-JJs so far [15, 16, 18]. This is because a TFF has a simple circuit structure and is suitable for circuit implementation and demonstration. However, the method of designing SFQ flip-flops using π-JJs and the question of whether the performance of flip-flops can be improved by introducing π-JJs are not clear.

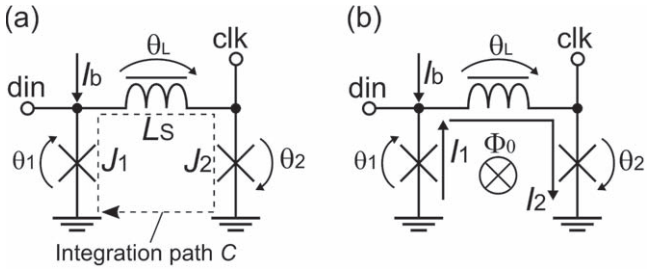

Figure 1. Simplified equivalent circuit of storage loop used in the conventional SFQ flip-flops. (a) '0' and (b) '1' states of the storage loop are shown. The critical current of J_1 and J_2 is I_C. Φ_0 denotes the flux quantum. 'din' and 'clk' mean data and clock inputs, respectively.

In this study, we investigated a circuit design methodology for designing SFQ flip-flops by considering the implementation method of a storage loop, which can store flux quantum and is indispensable for the implementation of SFQ flip-flops, by using π-JJs. We designed several SFQ flip-flops composed of 0- and π-JJs based on the investigated design methodology. To simulate and quantitatively evaluate the designed SFQ flop-flops, we developed an analog circuit simulator that can simulate the operation of superconducting circuits composed of both 0-JJs and π-JJs. The performances of the designed SFQ flip-flops composed of 0-JJs and π-JJs were quantitatively evaluated by using the developed analog circuit simulator. The circuit performances of the designed flip-flops were compared with those of the conventional SFQ flip-flops.

2. Analysis of storage loop containing π-JJs

We investigated the implementation method of a storage loop composed of 0-JJs and π-JJs to design SFQ flip-flops using π-JJs. Figure 1 shows the simplified equivalent circuits of a storage loop in the conventional SFQ flip-flop composed of two 0-JJs. To simplify the discussion, the critical currents of the two JJs in the storage loop are assumed to be the same, i.e., I_C. The inductance of the storage loop L_S is large so that the loop can store the flux quantum. The bias current I_b is asymmetrically supplied to realize the bistable energy potential of the storage loop [16]. I_1 and I_2 are the currents flowing through J_1 and J_2, respectively, when the internal state of the storage loop is '1' where one flux quantum is stored in the storage loop. According to Kirchhoff's law, the following relationship is satisfied:

$$I_1 + I_b = I_2. \quad (2)$$

In the '1' state, as one flux quantum is stored in the storage loop, the phase difference across the path C shown in figure 1(a) is 2π. Therefore, the following equation should be satisfied:

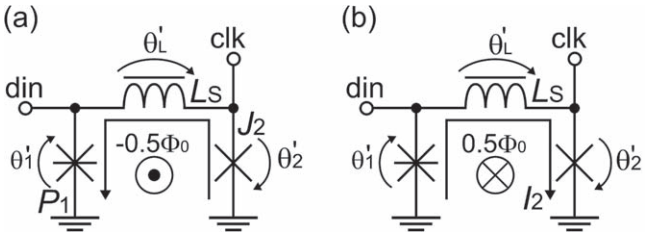

Figure 2. Simplified equivalent circuit of a π-storage loop composed of a π-JJ and a 0-JJ. (a) '0' and (b) '1' states of the π-storage loop are shown. The device symbol P_1 represents the π-JJ. The critical current of P_1 and J_2 is I_C.

$$\theta_1 + \theta_L + \theta_2 = 2\pi, \tag{3}$$

where θ_1, θ_L, and θ_2 are the phase differences across J_1, L_S, and J_2, respectively. The phase difference across each device is expressed as

$$\theta_1 = \sin^{-1}\left(\frac{I_1}{I_C}\right), \tag{4}$$

$$\theta_L = \frac{2\pi I_2}{\Phi_0} L_S, \tag{5}$$

and

$$\theta_2 = \sin^{-1}\left(\frac{I_2}{I_C}\right), \tag{6}$$

where Φ_0 is the flux quantum. It should be noted that this discussion is valid only for the steady state analysis because junctions' capacitances are not considered. By substituting equations (4), (5) and (6) into (3), the relationship between the inductance of the storage loop L_S and the current flowing through the storage loop can be obtained as

$$L_S = \frac{1}{I}\{2\pi - \sin^{-1}(I - i) - \sin^{-1}(I)\} \cdot \frac{\Phi_0}{2\pi I_C}, \tag{7}$$

where $I = I_2/I_C$ and $i = I_b/I_C$. To store the flux quantum in the storage loop, I should be less than 1. Equation (7) expresses the relationship between the inductance required to implement the storage loop and the current flowing through J_2 when the internal state of the storage loop is '1'.

Figure 2 shows the simplified equivalent circuits of a storage loop composed of a π-JJ, P_1, and a 0-JJ, J_2 (π-storage loop). P_1 and J_2 have the same critical current I_C. In the π-storage loop, the binary states are represented by the direction of half-flux quantum ($0.5\Phi_0$) threading the π-storage loop. The bias injection is removed because the bistable potential can be achieved without the current bias [16]. Therefore, the current flowing through both P_1 and J_2 has the same value I_2. Owing to the intrinsic π-phase shift in π-JJ P_1, the phase difference along the π-storage loop in its '1' state is expressed as

$$(\theta_1' + \pi) + \theta_L' + \theta_2' = 2\pi, \tag{8}$$

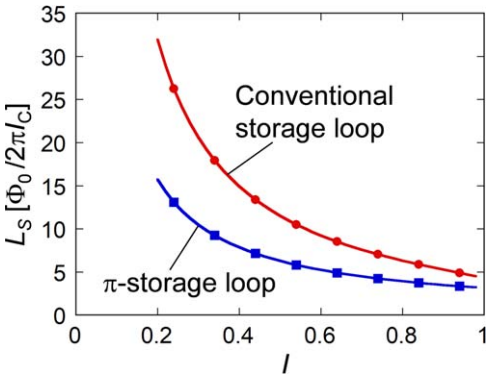

Figure 3. Dependences of the inductances required to implement the storage loop of the conventional SFQ circuits and the π-storage loop on the current flowing through J_2. I is the current flowing through J_2 normalized by I_C. L_S is normalized by $\Phi_0/2\pi I_C$.

where θ_1', θ_L', and θ_2' are the phase differences across P_1, L_S, and J_2, respectively. As the current flowing through both P_1 and J_2 is the same,

$$I_2 = I_C \sin(\theta_1' + \pi) = -I_C \sin\theta_2' \tag{9}$$

is satisfied. The phase differences across P_1 and J_2 are expressed as

$$\theta_1' = -\sin^{-1}\left(\frac{I_2}{I_C}\right) \tag{10}$$

and

$$\theta_2' = \sin^{-1}\left(\frac{I_2}{I_C}\right), \tag{11}$$

respectively. By substituting equations (9), (10) and (11) into (8), we obtain the following relationship:

$$L_S = \frac{\pi}{I} \cdot \frac{\Phi_0}{2\pi I_C}, \tag{12}$$

where $I = I_2/I_C$. '0' and '1' sates of the π-storage loop correspond to states where the normalized circulating current $\pm I$ is flowing in the loop. Equation (12) shows the relationship between the inductance required for the implementation of the π-storage loop and the current flowing through J_2 when one flux quantum is stored in the storage loop.

By using equations (7) and (12) we can derive the inductance required to implement the storage loop and π-storage loop as a function of I. In order to hold one flux quantum in the storage loop, I should be less than 1. Figure 3 shows the dependence of the required storage loop inductance on the current flowing through J_2 for both the conventional SFQ circuit implementation (assuming $i = 0.5$) and the π-JJ implementation. As shown in figure 3, the inductance of the π-storage loop is approximately half that of the conventional storage loop. Therefore, the circuit area required for implementing the storage loop is expected to be reduced by introducing π-JJs. As the π-storage loop does not require the injection of bias current, it consumes no static power.

However, assuming that the π-storage loop is directly connected to the conventional SFQ circuit, the intrinsic phase

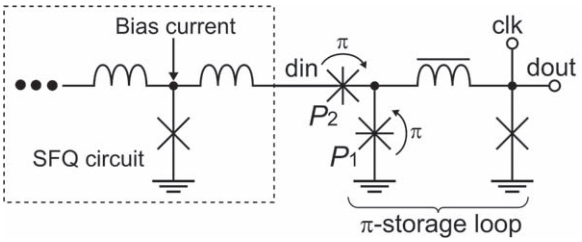

Figure 4. Interface between the π-storage loop and SFQ circuit.

shift of the π-JJ affects the operation of the SFQ circuit. To connect the SFQ circuit and π-storage loop without modifying the former, we devised the insertion of an additional π-JJ between them. Figure 4 shows the devised interface part between the SFQ circuit and the π-storage loop. An additional π-JJ P_2 is inserted to cancel the phase shift by P_1, and thus, the SFQ circuit can be directly connected to the π-storage loop. P_2 can also be used as an escape junction that cancels the successive data input. By using the devised interface, we can build SFQ flip-flops by replacing the storage loop with the π-storage loop, inserting the π-JJ, and removing the bias current injected to the storage loop.

As superconducting circuits other than the SFQ circuit require superconducting loops to store flux quantum, the investigated π-storage loop and its interface with the conventional superconducting circuit are expected to be applied to other superconducting circuits.

3. Development of simulator for circuits containing π-JJs

To evaluate the characteristics of the superconducting circuits composed of 0-JJs and π-JJs, we developed an analog circuit simulator by modifying JSIM [31], which was developed in 1989 and has been widely used [32]. The JSIM employs the modified nodal analysis (MNA) method to represent the circuit equation including characteristics of 0-JJs in matrix form [31]. We added a new function that builds the matrix (called MNA stamp) in the circuit equation of the π-JJ, the characteristic of which obeys the current–phase relationship represented by equation (1). The matrix size of the MNA stamp of the π-JJ is 3×3, which is the same as that of the 0-JJ. Therefore, the calculation time and the computation resources required for the simulation of the π-JJ are the same as those of the 0-JJ. The MNA stamp of the circuit under simulation, the connection and circuit parameters of which are described in the netlist, is updated by the functions corresponding to each circuit component including the π-JJ. Calculation results are obtained by numerically solving the differential equations of the MNA and are output every calculation step. We added and modified functions for netlist input, updating the MNA stamp, and calculation result output. In total, we added 10 functions and modified 21 functions. The developed circuit simulator can also perform a transient analysis taking thermal noises at the finite temperature into account by employing the noise model implementation by Satchell [33].

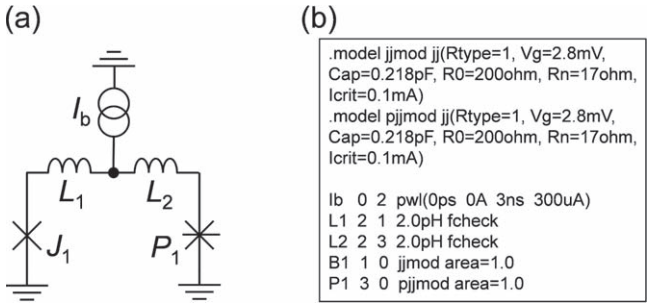

Figure 5. (a) Equivalent circuit and (b) an example of the netlist of a dc-SQUID composed of a 0-JJ and a π-JJ. The circuit symbol of P_1 corresponds to the π-JJ [36]. J_1 and P_1 are device names of the 0-JJ and the π-JJ, respectively. The critical current of J_1 and P_1 is 100 μA. 'fcheck' is needed to describe inductors in the netlist [37].

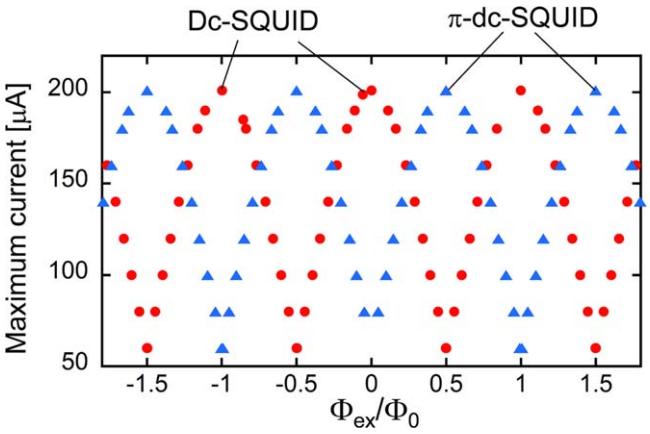

Figure 6. Simulated dependences of maximum currents of the π-dc-SQUID and the dc-SQUID on external magnetic flux Φ_{ex} normalized by the magnetic flux quantum in the superconductor Φ_0 [36].

In order to confirm validity of the simulation results by the developed analog circuit simulator, we calculated the maximum current characteristic of a dc-SQUID composed of a 0-JJ and a π-JJ (π-dc-SQUID) and compared it to that of a dc-SQUID composed of two 0-JJs. Figure 5 shows the equivalent circuit of the π-dc-SQUID and an example of the corresponding netlist. As shown in figure 5(b), if the case that the initial character of the device name is 'P' or 'p', the simulator recognizes the corresponding device as the π-JJ. In this simulation, the junction characteristics of both the 0-JJ and the π-JJ, which are described in the netlist, are assumed to be the same as that of the junction fabricated by the National Institute of Advanced Industrial Science and Technology (AIST) 2.5 kA cm^{-2} Nb standard process 2 (AIST-STP2) [34, 35]. In the simulation, the ramped current I_b with the rise rate of 100 μA ns^{-1} was applied to the π-dc-SQUID. The maximum current was obtained by measuring the applied current value when the π-dc-SQUID switches to the finite voltage state. The magnetic flux was applied to the π-dc-SQUID by applying the dc-current to the inductors L_1 and L_2 shown in figure 5. Figure 6 shows the calculated dependence

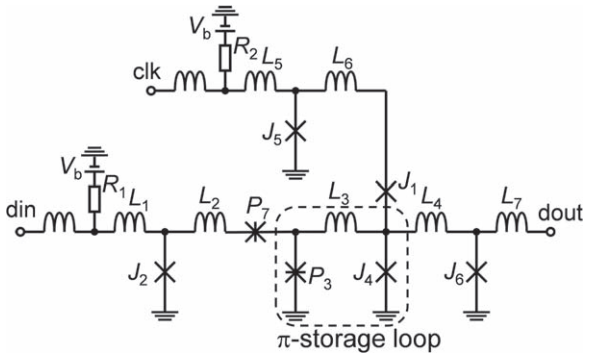

Figure 7. Equivalent circuit of the π-DFFE. 'din', 'clk', and 'dout' correspond to data input, clock, data output ports, respectively. The critical current values of the 0-JJs and π-JJs are as follows: $J_1 = 230\ \mu$A, $J_2 = 216\ \mu$A, $P_3 = 140\ \mu$A, $J_4 = 150\ \mu$A, $J_5 = 216\ \mu$A, $J_6 = 228\ \mu$A, and $P_7 = 170\ \mu$A. $L_1 = 2.457$ pH, $L_2 = 2.500$ pH, $L_3 = 5.500$ pH, $L_4 = 4.690$ pH, $L_5 = 2.457$ pH, $L_6 = 3.400$ pH, $L_7 = 2.421$ pH, and $R_1 = R_2 = 8.34\ \Omega$. The bias voltage V_b is 2.5 mV.

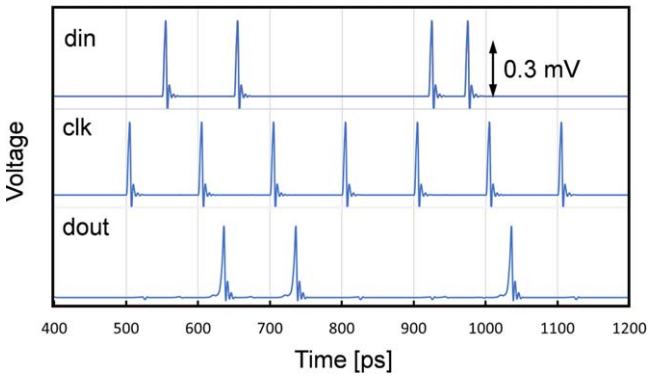

Figure 8. Example of transient analysis result of the π-DFFE.

of the maximum current on the externally applied magnetic flux. The threshold characteristic of the dc-SQUID, composed of two 0-JJs, is also shown in figure 6. The threshold characteristic of the π-dc-SQUID shows the periodicity shifted by half a period compared to that of the dc-SQUID. This result indicates that the characteristic of the superconducting circuit containing π-JJ can be precisely simulated by the analog circuit simulator we developed.

The developed analog circuit simulator, which we call PJSIM, is advantageous to design and analyze large-scale superconducting circuit composed of both 0-JJs and π-JJs compared to the conventional simulation method that uses an equivalent circuit model, which is composed of an inductance and a current source, and can imitate π-phase shift in the superconducting circuit [38]. We used the analog circuit PJSIM to quantitatively evaluate the characteristics of the superconducting circuits composed of both 0-JJs and π-JJs mentioned in the following section. We are planning to make PJSIM available for the public in the near future.

4. SFQ flip-flops containing π-JJs

We designed several SFQ flip-flops based on the design methodology discussed in section 2. Figure 7 shows the equivalent circuit of a delay flip-flop with an escape junction (DFFE) implemented by using a π-storage loop (π-DFFE). The π-DFFE was designed by modifying the DFFE cell in the CONNECT cell library [39]. The storage loop of the DFFE cell with an asymmetric bias supply is replaced by the π-storage loop and the escape junction for data input (din) is replaced by P_7. At the standard bias voltage of 2.5 mV, the static power consumption of the π-DFFE is 1.50 μW, whereas the original DFFE cell from the CONNECT cell library has a static power consumption of 1.72 μW. The inductance in the π-storage loop (L_3) is 5.500 pH, which is much smaller than the typical inductance of a conventional storage loop.

As the conventional SFQ circuits can be directly connected to the π-storage loop owing to P_7, the π-DFFE is compatible with any cells in the CONNECT cell library. We simulated the π-DFFE by connecting three Josephson transmission line cells in the CONNECT cell library in front of and behind the π-DFFE. Figure 8 shows an example of the result of simulated transient analysis of the π-DFFE by using the PJSIM discussed in section 3. In this simulation, the junction characteristics of both the 0-JJ and the π-JJ, critical current density, normal and sub-gap resistances, and junction capacitance are assumed to be the same as those of the 0-JJ fabricated by the AIST-STP2 [34, 35]. Because the current flowing in P_7 is larger than that in P_3 when the π-DFFE is in '1' state, P_7 acts as the escape junction for data input (din), and thus, the successive 'din' input is canceled. The simulated dc bias margin of the π-DFFE is -31.6% to 45.2%. Although the circuit parameters of the π-DFFE were not optimized well, a wide bias margin of $\pm 30\%$ could be obtained. We also evaluated the circuit parameter margin of all circuit elements of π-DFFE using PJSIM. The critical device, which has the narrowest parameter margin, is J_1 and the margin is -23.0% to 23.5%. Similarly, we designed the AND gate and the nondestructive read-out flip-flop (NDRO) and confirmed the correct operation of the circuits with dc bias margins of more than $\pm 25\%$.

The π-storage loop has a symmetric circuit structure and logic representation according to the direction of half-flux quantum. By using the symmetry of the π-storage loop, SFQ flip-flops with complementary outputs, such as the NDRO with complementary output (NDROC), can be designed efficiently. The NDROC is widely used in a binary decoder [40–42], dual-rail SFQ circuits [43–46], etc. However, the NDROC with a complex complementary function is one of the largest SFQ flip-flops and the delay of the NDROC is larger than that of other flip-flops. In the conventional NDROC, two storage loops are used to realize the complementary output function. The number of 0-JJs of the NDROC cell in the CONNECT cell library is 33.

Figure 9 shows the equivalent circuit of the NDROC implemented by using π-JJs (π-NDROC). The loop composed of P_8, L_9, L_{12}, L_{10}, and J_9 in figure 9 is the π-storage loop. The π-NDROC is designed using only one π-storage loop and has a symmetric circuit structure with an axis of

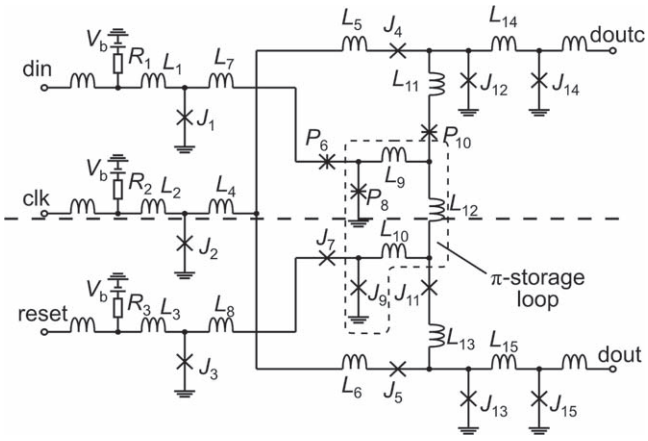

Figure 9. Equivalent circuit of the π-NDROC. The critical current values of the 0-JJs and π-JJs are as follows: $J_1 = J_2 = J_3 = 215\ \mu$A, $J_4 = J_5 = 205\ \mu$A, $P_6 = J_7 = 230\ \mu$A, $P_8 = J_9 = 140\ \mu$A, $P_{10} = J_{11} = 120\ \mu$A, $J_{12} = J_{13} = 100\ \mu$A, and $J_{14} = J_{15} = 203\ \mu$A. $L_1 = L_2 = L_3 = 2.457$ pH. $L_4 = 1.500$ pH, $L_5 = 5.500$ pH, $L_6 = L_{11} = L_{13} = 0.500$ pH, $L_7\ L_8 = L_9 = L_{10} = 0.500$ pH, $L_{14} = L_{15} = 5.486$ pH. $R_1 = R_2 = R_3 = 8.34\ \Omega$. The bias voltage V_b is 2.5 mV.

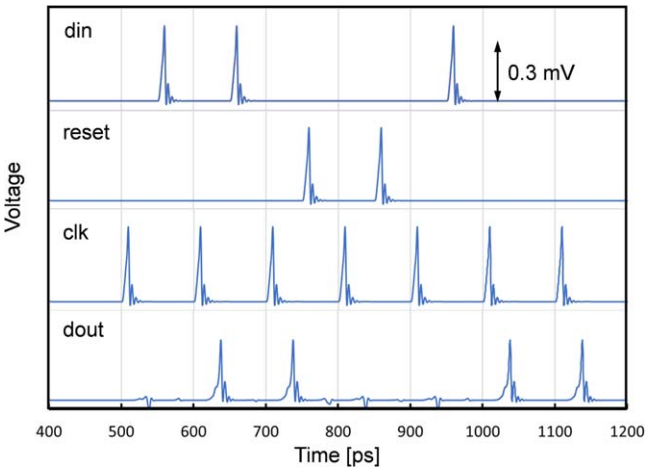

Figure 10. Example of transient analysis result of the π-NDROC.

symmetry expressed by the horizontal dashed line in figure 9. This π-storage loop is not only structurally but also logically symmetric because P_6 and P_8 are π-JJs whereas J_7 and J_9 are 0-JJ. When the clock (clk) signal is supplied to the π-storage loop, the output is obtained from either 'dout' or 'doutc' ports according to the direction of the half-flux quantum in the π-storage loop. As the internal logic state of the π-storage loop, which corresponds to the direction of half-flux quantum in the π-storage loop, can be changed by applying 'din' and 'reset' signals, the function of NDROC can be obtained. The number of JJs, including π-JJ, used in the π-NDROC is 15. The static power consumption of the π-NDROC is 2.25 μW, whereas that of the NDROC cell in the CONNECT cell library is 8.56 μW.

Figure 10 shows the simulation result of the π-NDROC. The correct complementary output signals are obtained from the 'dout' and 'douc' ports. The simulated dc bias margin of the π-NDROC is -18.4% to 42.4%. The critical devices are J_4 and J_5 and the parameter margin is -20.5% to 21.5%. The latency of the π-NDROC is also reduced compared with that of the NDROC cell.

5. Conclusion

We investigated a design methodology of SFQ flip-flops composed of both 0-JJs and π-shifted JJs. The investigated design method enables us to design SFQ flip-flops by using a storage loop containing π-JJs. Moreover, the design methodology is suitable for implementing SFQ logic gates with complementary outputs owing to the symmetric circuit structure and logic state representation. We could drastically reduce the number of JJs and the power consumption of the flip-flops with complementary outputs by introducing π-JJs. We developed an analog circuit simulator for the superconducting circuits containing π-JJs. We confirmed the correct operation of SFQ flip-flops composed of 0-JJs and π-JJs with wide operation margins. The developed design methodology and analog circuit simulators are helpful for designing future large-scale superconducting circuits containing π-JJs and reconfigurable logic circuits composed of programmable 0-π JJs.

Acknowledgments

This work was supported by JSPS KAKENHI Grant Number JP18K04280. The authors would like to thank Akira Fujimaki and Masamitsu Tanaka for fruitful discussions. The authors are also grateful to Christopher Ayala for proofreading the manuscript.

ORCID iDs

Yuki Yamanashi https://orcid.org/0000-0003-4840-7611
Nobuyuki Yoshikawa https://orcid.org/0000-0001-6191-6715

References

[1] Theis T N and Wong H S P 2017 The end of Moore's law: a new beginning for information technology *Comput. Sci. Eng.* **19** 41–50
[2] Khan H N, Hounshell D A and Fuchs E R H 2018 Science and research policy at the end of Moore's law *Nat. Electron.* **1** 14–21
[3] Mukhanov O A 2011 Energy-efficient single flux quantum technology *IEEE Trans. Appl. Supercond.* **21** 760–9
[4] Holmes D S, Ripple A L and Manheimer M A 2013 Energy-efficient superconducting computing-power budgets and requirements *IEEE Trans. Appl. Supercond.* **23** 1701610
[5] Takeuchi N, Yamanashi Y and Yoshikawa N 2015 Energy efficiency of adiabatic superconductor logic *Supercond. Sci. Technol* **28** 015003
[6] Soloviev I I, Klenov N V, Bakurskiy S V, Kupriyanov M Y, Gudkov A L and Sidorenko A S 2017 Beyond Moore's

technologies: operation principles of a superconductor alternative *Beilstein J. Nanotechnol.* **8** 2689–710
[7] Josephson B D 1962 Possible new effects in superconductive tunneling *Phys. Lett.* **1** 251–3
[8] Anderson P W and Rowell J M 1963 Probable observation of the Josephson superconducting tunneling effect *Phys. Rev. Lett.* **10** 230–2
[9] Nakajima K, Mizusawa H, Sugahara H and Sawada Y 1991 Phase mode Josephson computer system *IEEE Trans. Appl. Supercond.* **1** 29–36
[10] Likharev K K and Semenov V K 1991 RSFQ logic/memory family: a new Josephson-junction technology for sub-terahertz-clock-digital systems *IEEE Trans. Appl. Supercond.* **1** 3–28
[11] Hosoya M, Hioe W, Casas J, Kamikawai R, Harada Y, Wada Y, Nakane H, Suda R and Goto E 1991 Quantum flux parametron: a single quantum flux device for Josephson supercomputer *IEEE Trans. Appl. Supercond.* **1** 77–89
[12] Takeuchi N, Ozawa D, Yamanashi Y and Yoshikawa N 2013 An adiabatic quantum flux parametron as an ultra-low power logic device *Supercond. Sci. Technol.* **26** 035010
[13] Herr Q P, Herr A Y, Oberg O T and Ioannidis A G 2011 Ultra-low-power superconductor logic *J. Appl. Phys.* **109** 103903
[14] Terzioglu E and Beasley M R 1998 Complementary Josephson junction devices and circuits: a possible new approach to superconducting electronics *IEEE Trans. Appl. Supercond.* **8** 48–53
[15] Ustinov A V and Kaplunenko V K 2003 Rapid single-flux quantum logic using π-shifters *J. Appl. Phys.* **94** 5405–7
[16] Ortlepp T, Ariando A, Mielke O, Verwijs C J M, Foo K F K, Rogalla H, Uhlmann F H and Hilgenkamp H 2006 Flip-flopping fractional flux quanta *Science* **312** 1495–7
[17] Ortlepp T, Ariando A, Mielke O, Verwijs C J M, Foo K F K, Andreski A, Rogalla H, Uhlmann F H and Hilgenkamp H 2007 RSFQ circuitry using intrinsic π-phase shifts *IEEE Trans. Appl. Supercond.* **17** 659–64
[18] Khabipov M I, Balashov D V, Maibaum F, Zorin A B, Oboznov V A, Bolginov V V, Rossolenko A N and Ryazanov V V 2010 A single flux quantum circuit with a ferromagnet-based Josephson π-junction *Supercond. Sci. Technol.* **23** 045032
[19] Kamiya T, Tanaka M, Sano K and Fujimaki A 2018 Energy/space-efficient rapid single-flux-quantum circuits by using π-shifted Josephson junctions *IEICE Trans. Electron.* **E101-C** 385–90
[20] Ioffe L B, Geshkenbein V B, Feigel'man M V, Fauchere A L and Blatter G 1999 Environmentally decoupled sds-wave Josephson junctions for quantum computing *Nature* **398** 679–81
[21] Yamashita T, Tanikawa K, Takahashi S and Maekawa S 2005 Superconducting π qubit with a ferromagnetic Josephson junction *Phys. Rev. Lett.* **95** 097001
[22] Yamashita T, Takahashi S and Maekawa S 2006 Superconducting π qubit with three Josephson junctions *Appl. Phys. Lett.* **88** 132501
[23] Buzdin A I 2005 Proximity effects in superconductor-ferromagnet heterostructures *Rev. Mod. Phys.* **77** 935–76
[24] Weidesa M, Kemmler M, Goldobin E, Koelle E, Kleiner R, Kohlstedt H and Buzdin A 2006 High quality ferromagnetic 0 and π Josephson tunnel junctions *Appl. Phys. Lett.* **89** 122511
[25] Khaire T S, Pratt W P Jr and Birge N O 2009 Critical current behavior in Josephson junctions with the weak ferromagnet PdNi *Phys. Rev.* B **79** 094523
[26] Feofanov A K *et al* 2010 Implementation of superconductor/ferromagnet/superconductor π-shifters in superconducting digital and quantum circuits *Nat. Phys.* **6** 593–7
[27] Niedzielski B M, Gingrich E C, Loloee R, Pratt W P and Birge N O 2015 S/F/S Josephson junctions with single-domain ferromagnets for memory applications *Supercond. Sci. Technol.* **28** 085012
[28] Ito H, Taniguchi S, Ishikawa K, Akaike H and Fujimaki A 2017 Fabrication of superconductor-ferromagnet-insulator-superconductor Josephson junctions with critical current uniformity applicable to integrated circuits *Appl. Phys. Express* **10** 033101
[29] Gingrich E C, Niedzielski B M, Glick J A, Wang Y, Miller D L, Loloee R, Pratt W P Jr and Birge N O 2016 Controllable 0-π Josephson junctions containing a ferromagnetic spin valve *Nat. Phys.* **12** 564–7
[30] Dayton I M *et al* 2018 Experimental demonstration of a Josephson magnetic memory cell with a programmable π-junction *IEEE Magn. Lett.* **9** 3301905
[31] Fang E S and Van Duzer T 1989 A Josephson integrated circuit simulator (JSIM) for superconductive electronics application *Extended Abstracts of Int. Supercond. Electron. Conf.* pp 407–10
[32] Fourie C J and Volkmann M H 2013 Status of superconductor electronic circuit design software *IEEE Trans. Appl. Supercond.* **23** 1300205
[33] Satchell J 1999 Limitations on HTS single flux quantum logic *IEEE Trans. Appl. Supercond.* **9** 3841–4
[34] Nagasawa S, Hashimoto Y, Numata H and Tahara S 1995 A 380 ps, 9.5 mW Josephson 4 kbit RAM operated at a high bit yield *IEEE Trans. Appl. Supercond.* **5** 2447–52
[35] Hidaka M, Nagasawa S, Satoh T, Hinode K and Kitagawa Y 2006 Current status and future prospect of the Nb-based fabrication process for single flux quantum circuits *Supercond. Sci. Technol.* **19** S138–42
[36] Yamanashi Y, Sugiyama A, Imagawa S and Yoshikawa N 2017 Simulation of superconducting circuits composed of Josephson junctions and π-junctions *IEICE Tech. Rep.* **117** 13–6
[37] Febvre P 2011 Manual to handle JSIM and optimizer program AUTO5 from University of Technology Ilmenau (version 7.0) http://sun.ac.za/ix/?q=tools_jsim
[38] Mielke O, Ortlepp T, Febvre P and Uhlmann F H 2009 Reduced probability of noise introduced malfunction in RSFQ circuits by implementing intrinsic π-phaseshifter *IEEE Trans. Appl. Supercond.* **19** 621–5
[39] Yorozu S, Kameda Y, Terai H, Fujimaki A, Yamada T and Tahara S 2002 A single flux quantum standard logic cell library *Physica* C **378–381** 1471–4
[40] Takahashi T, Numaguchi R, Yamanashi Y and Yoshikawa N 2016 High-speed demonstration of low-power 1k-bit shift-register memories using LR-biasing SFQ circuits *IEICE Electron. Express* **13** 1–6
[41] Tanaka M, Sato R, Hatanaka Y and Fujimaki A 2016 High-density shift-register-based rapid single-flux-quantum memory system for bit-serial microprocessors *IEEE Trans. Appl. Supercond.* **26** 1301005
[42] Ando Y, Sato R, Tanaka M, Takagi K, Takagi N and Fujimaki A 2016 Design and demonstration of an 8 bit bit-serial RSFQ microprocessor: CORE e4 *IEEE Trans. Appl. Supercond.* **26** 1301205
[43] Deng Z J, N Yoshikawa N, Whiteley S R and Van Duzer T 1997 Data-driven self-timed RSFQ digital integrated circuit and system *IEEE Trans. Appl. Supercond.* **7** 3634–7
[44] Maezawa M, Kurosawa I, Aoyagi M, Nakagawa H, Kameda Y and Nanya T 1997 Rapid single-flux-quantum dual-rail logic for asynchronous circuits *IEEE Trans. Appl. Supercond.* **7** 2705–8
[45] Polonsky S 1999 Delay insensitive RSFQ circuits with zero static power dissipation *IEEE Trans. Appl. Supercond.* **9** 3535–8
[46] Obata K, Takagi K and Takagi N 2007 Logic synthesis method for dual-rail RSFQ digital circuits using root-shared binary decision diagrams *IEICE Trans. Fundam.* **E90-A** 257–66