

A superconducting nanowire can be modeled by using SPICE

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Abstract

Modeling of superconducting nanowire single-photon detectors typically requires custom simulations or finite-element analysis in one or two dimensions. Here, we demonstrate two simplified one-dimensional SPICE models of a superconducting nanowire that can quickly and efficiently describe the electrical characteristics of a superconducting nanowire. These models may be of particular use in understanding alternative architectures for nanowire detectors and readouts.

Supplementary material for this article is available [online](#)

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(Some figures may appear in colour only in the online journal)

1. Introduction

Superconducting nanowire single-photon detectors (SNSPDs) are becoming increasingly used for applications as wide ranging as integrated-circuit debugging [1] and space communications [2, 3]. As a result, device architectures have proliferated in recent years, including the superconducting nanowire avalanche photodetector (SNAP), the multi-element superconducting nanowire single-photon detector [4], and a variety of alternative array architectures [5–7]. Currently, simulation of these new architectures is used extensively for optimization and verification prior to fabrication, but this approach relies on slow electrothermal physical modeling outside of a typical circuit-design environment [8]. Furthermore, new nanowire-based electronic devices have been recently demonstrated that require convenient methods of electrical simulation [9, 10]. These devices could factor into designs for large-scale power-efficient computing systems based on superconductors, but existing models cannot be easily integrated with complex conventional or superconducting circuits

[11]. By describing a simple but accurate model of the nanowire element using the industry-standard Simulation Program with Integrated Circuit Emphasis (SPICE) circuit-modeling software [12], this report provides a quick and conceptually simple alternative to custom electrothermal numerical models, and thus enables broader application of these and similar devices.

Various SPICE implementations exist, all consisting of a core engine for circuit simulation, along with a library of basic components. In this work, we used both the LTspice implementation of SPICE [13], which is a freely available electrical-circuit modeling software closely based on SPICE, and the WRspice [14] implementation, which is an implementation devised specifically for Josephson-junction-based circuits [15–17]. Adaptation of this model to additional SPICE implementations should be straightforward. SPICE was recently adapted for use in modeling macroscopic high-critical-temperature superconducting wires [18]. However, until now, the component list in SPICE has not included superconducting nanowires, thus it has been impossible to quickly and easily model complex superconducting nanowire detector architectures using SPICE.

In this paper, we present three circuit models of the hotspot creation and annihilation process: (1) a curve-fitting model; (2) a more complete dynamic model; and (3) a thermal device

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model (see appendix A in the online supplementary material available online at stacks.iop.org/SUST/31/055010/mmedia). The curve-fitting model is based on replicating the i - v relation of the nanowire, as well as the switching behavior into and out of the superconducting state. This model is accurate as long as the timescales over which the external circuit can evolve and respond (typically hundreds of picoseconds to nanoseconds) are long relative to the timescales over which the hot-spot and switching dynamics occur within the nanowire (typically tens of picoseconds). The dynamic model includes the electrothermal dynamics of the nanowire (with the exceptions noted in section 2.1 below) and is necessary when the nanowire dynamics interact with the dynamics of the external circuit. The dynamic model is thus more complete, but may be computationally slower than the curve-fitting model. Neither of these models adequately treat fluxoid quantization in superconducting loops, although incorporation of this model in WRspice should be able to address this issue. These models also cannot adequately treat coherent flux tunneling, as might occur in quantum-coherent superconducting electronics. Such treatments are beyond the scope of the work presented here.

For situations in which large-scale architectural considerations are at play (e.g. system power assessments, or when dealing with long operations), the curve-fit model may be preferred. In device simulations, when attempting to understand the physics at play, simplified simulations might also be preferred. Normally, however, we expect the full dynamic model to be preferred due to its improved accuracy and completeness. In situations where rapid counting rates are required, we expect the thermal device model to be required.

Our goal in this paper is to provide the required understanding to implement a SPICE model of superconducting nanowires in LTspice or similar SPICE software, and a framework for implementation in other contexts. The paper proceeds first by describing the underlying physics, then discussing how the physical model is implemented in SPICE, first by a simpler curve-fit model, and second by the complete dynamic model. The paper then discusses parameter extraction and goes through a number of examples where the SPICE models reproduce well-known results from the SNSPD literature. Finally, we discuss some of the issues with and advantages of our approach, and conclude with a description of some of the future work that might be enabled.

2. Physical model of nanowire electrical behavior following photon-arrival events

The circuit model of a superconducting nanowire and a photon-arrival event must contain the relevant device physics, thus understanding the physical model is key to understanding the circuit model. In this section, we describe the physical model of a superconducting nanowire following a photon-arrival event in a way that simplifies adaptation to a circuit model. We do not attempt to treat the physics of jitter, ignoring the microscopic physics of hot-spot creation and post-photon-arrival signal-propagation delay in the nanowire [19–23].

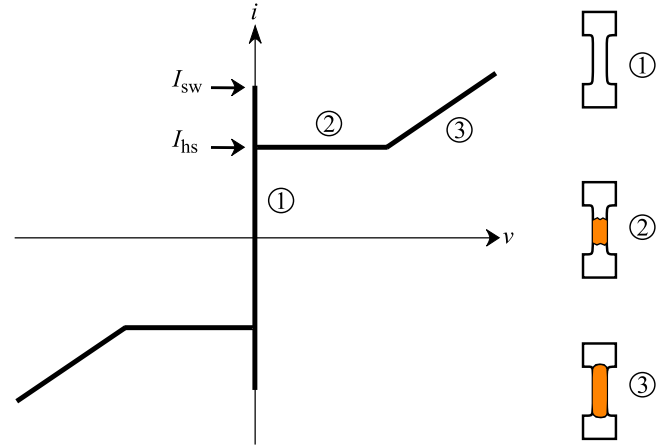


Figure 1. Schematic i - v curve for a superconducting nanowire illustrating showing important regions: ① superconducting state; ② hot-spot plateau; and ③ normal state.

2.1. Physical model of a nanowire

Figure 1 displays a schematic i - v curve illustrating the most basic direct-current electrical characteristic of an idealized superconducting nanowire. The corresponding physical model depends on which of two relevant states the detector is in: ① the superconducting state; or ② the hot-spot state. A third state ③ exists, the normal state, in which the entire wire is in a resistive state, but this state is not realized in typical operation of the device. The entire relevant physical model can thus be described by accurately modeling the two relevant states as well as dynamic transitions between these states.

The superconducting state occurs when the entire wire remains in the superconducting phase and thus the voltage v across the device is zero. We will refer to this state as the ‘zero-voltage state’ of the wire. The device can transition out of the superconducting state if its current i_D exceeds the switching current of the device I_{sw} ⁶. In the superconducting state, the wire behaves electrically as an inductor where the source of the inductance is almost entirely due to kinetic, rather than geometric inductance [24]. The density of Cooper pairs in the wire depends on the current in it, thus the wire inductance is also dependent on the current, resulting in an increased inductance relative to the zero-bias inductance (by $\sim 20\%$ as the current approaches the critical current of the nanowire) [25]. The dependence of kinetic inductivity on current density is known if the depairing current density is known [26] and vice versa. A fit to the current dependence of the kinetic inductance can thus be used to determine the depairing current density. By applying a visual fit to the data represented by the black circles in figure 3 of [25], we extracted a value for the depairing current of $1.67I_{sw}$ leading to the relation:

$$L_k(i_D) = \frac{L_0}{2 \cos(2 \arcsin(0.6 i_D / I_{sw}) / 3) - 1}, \quad (1)$$

⁶ We use I_{sw} rather than I_c to describe the current at which the device can no longer support a supercurrent to emphasize that the depairing current is not the limiting current in these devices, and that vortex crossings, noise, and other factors may contribute to the suppression of I_c .

where L_o is the zero-current inductance of the wire. Although a more careful fitting process could perhaps yield a more accurate estimate of the depairing current, one should keep in mind that material, processing, and testing apparatus differences between experiments are likely to dominate over any slight variations in fit. Thus, estimates for depairing current should be done for each experiment. Fortunately, the dependence of inductance on bias current only influences the hot-spot indirectly, via modification of external circuit parameters, and even then the full range of inductance variation is only $\sim 20\%$. Indeed, we verified that our results were little changed even when we neglected the dependence of L_k on current entirely. As such, the simple visual fitting process used was more than adequate for our purpose here.

The hot-spot state occurs when the device has an extended and sustained region in which the wire is in its non-superconducting (normal) phase, i.e. a region where the temperature T exceeds the critical temperature T_C across the wire⁷. In the hot-spot state, additional voltage simply results in an expansion of the hot-spot (i.e. increased resistance) but no change in the current. This situation is physically possible due to the balance between Joule heating and cooling through the device at the superconducting-normal phase boundary of the wire, a well-studied topic in the field [27].

Rather than explicitly model the thermal physics of the device, as is typically done, we will use a phenomenological model developed by Kerman *et al* [28] in which the velocity of the superconducting-/normal-phase boundary depends on the bias current. Figure 2 shows the dependence of hot-spot growth rate on the applied bias current. Multiplying this rate by R_{SH}/w , where R_{SH} is the sheet resistance (resistivity ρ divided by thickness d) of the superconducting film in the normal phase and w is the width of the nanowire, we obtain the time derivative of the hot-spot resistance:

$$\frac{dR_{HS}}{dt} = \frac{R_{SH}}{w} \frac{dl}{dt}, \quad (2)$$

where R_{HS} is the instantaneous hot-spot resistance, and l is the length of the hot-spot. The derivative on the right side of equation (2) captures the rate of hot-spot expansion, and is derived by balancing Joule heating with conductive cooling into the substrate. Following a standard treatment of normal-domains in superconducting films [29], Kerman *et al* provide an explicit expression for the dependence of the rate of hot-spot growth on bias current [28]:

$$v_{HS} = \frac{dl}{dt} = 2v_o \frac{\psi i^2 / I_{SW}^2 - 2}{\sqrt{\psi i^2 / I_{SW}^2 - 1}}, \quad (3)$$

where $v_o = \sqrt{h_c \kappa / d} / c$ is a characteristic velocity

⁷ The term hot-spot is a misnomer, as in fact it is neither necessarily hot nor a spot. Rather as we use it here it is a strip of material in the normal (non-superconducting) phase that spans the nanowire. This strip grows or shrinks according to the device geometry and the history of the bias current; 'normal domain' would be a more precise description. Nonetheless, hot-spot is the term used in the field, so we will continue with this term here.

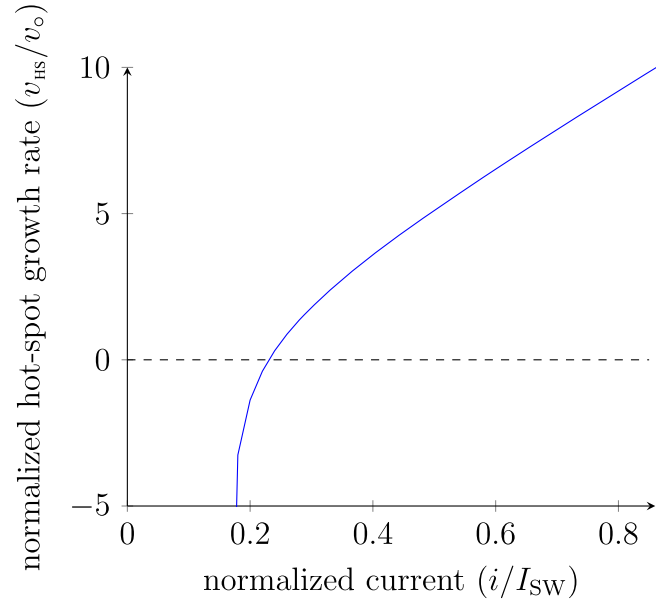


Figure 2. Hot-spot growth rate v_{HS} versus normalized bias current extracted from [28] and used in the models described. i' is the normalized bias current i/I_{SW} . At $v_{HS} = 0$, $i_D = I_{HS}/I_{SW}$ where I_{HS} is the current at the hot-spot plateau, where the hot-spot is stable. For currents i_D larger than I_{HS} , the hot-spot grows. For currents smaller than I_{HS} , the hot-spot shrinks. Numerical troubles with convergence induced by the pole in the denominator of equation (3) in the main text were addressed by using the modification of the expression (3) as provided in appendix B with $\delta = 0.01$.

($\sim 0.25 \text{ nm ps}^{-1}$ for 4 nm thick NbN),

$$\psi = \frac{\rho I_{SW}^2}{h_c w^2 d (T_C - T_S)} \quad (4)$$

is the Stekly parameter [29] (~ 38 for 4 nm thick NbN), $h_c = 50000 \text{ W m}^{-2} \text{ K}^{-1}$ is the thermal contact conductivity of the interface between the substrate (we use the value for sapphire) and the nanowire, $\kappa = 0.108 \text{ W m}^{-1} \text{ K}^{-1}$ is the thermal conductivity of the nanowire, $c = 4400 \text{ J m}^{-3} \text{ K}^{-1}$ is the specific heat per unit volume of the nanowire, T_S is the substrate temperature, and T_C is the critical temperature of the nanowire⁸. Values for h_c , κ , and c were taken from [28]. The factor of two in (3) arises because the hot-spot has two boundaries.

Figure 2 illustrates two interesting limiting behaviors of the expression presented in (3) above. First, it illustrates that for low currents, this simple model breaks down when the current becomes small enough, as is illustrated by the divergence in the hot-spot-growth rate at low currents. In this limit, cooling must exceed Joule heating and the device will switch back into the superconducting state suddenly. It also illustrates the apparent linearity of the expression for large currents. This linear region occurs because for NbN (where

⁸ To be more careful, one should consider the electron and phonon temperatures as separate quantities during the dynamic evolution of the superconductors—we obtain good agreement with experiment without taking this step, suggesting that this distinction is not relevant to the electrothermal device behavior.

$\psi \approx 38 \gg 1$) and currents approaching I_{SW} equation (3) can be linearized and approximated as

$$\frac{dI}{dt} = 2v_0(i/I_{SW})\sqrt{\psi}. \quad (5)$$

When in the hot-spot state described above, if the voltage across the device is increased, the length of the hot-spot will increase proportionately until eventually the hot-spot will extend along the full length of the device. At this point, the device resistance cannot increase further, even with increasing voltage, as its growth is limited by the large, thermally anchored contact pads found at the end of the wire. The full nanowire length is then in the normal state. At this point, the superconductor is in the normal phase throughout. In this situation, the device behaves like a simple resistor (ignoring the dependence of R_{SH} on temperature, which is a reasonable approximation for the temperature ranges we are dealing with). We call this state the normal state. In the normal state, the device impedance ($\sim 100 \text{ k}\Omega$) is enormous relative to other impedances in the circuit. As such, it is unlikely any signal present in a typical nanowire circuit would suffice to drive the system into this state, and thus one does not realize this state in conditions of typical device operation.

Dynamic transitional (non-equilibrium) states exists, not shown in figure 2, while the hot-spot is either growing or contracting. During the growth period, Joule heating in the nanowire exceeds cooling into the substrate. During the cooling period, the hotspot collapses as heat dissipates into the substrate. The result is a hot-spot that grows and shrinks over timescales set by the thermal physics of the system, much shorter than typical $> 1 \text{ ns}$ L/R time constants in the circuit. In this regime, the rate of change of the voltage across the wire is proportional to the current in the wire, as expressed mathematically in equation (3).

There is an additional dynamic state in which the equilibrium temperature of the nanowire exceeds the temperature of the surroundings, but is below T_C . In this state, the nanowire is more prone to switching than it would typically be, as I_{SW} is suppressed by the elevated wire temperature. This state leads to after-pulsing effects [30], but is short lived and can be safely ignored in many circuits. The details of this situation are somewhat complicated and a full explanation here would distract from the main goal of the paper. Thus, this treatment is discussed in appendix A in the online supplementary material.

2.2. Physical model of signal propagation on nanowire

Recent results have shown that the lumped-element model of a nanowire is inadequate to understanding the jitter characteristics of typical nanowires [19–21]. One might thus worry that the lumped-element model described above is insufficient, and indeed one would be correct when considering the impact of device geometry on device jitter. However, the characteristic velocity of hot-spot growth is set by $v_0 \sim 0.25 \text{ nm ps}^{-1}$ while the speed of signal propagation is much larger, having been estimated to be $v \sim 2\%c \approx 6 \text{ }\mu\text{m ps}^{-1}$ [20]. Therefore, from the point of view of the

dynamics involved in hot-spot growth, we can safely ignore the distributed-element picture.

For the signal-propagation to significantly impact calculations of the device reset and latching, the device dimension must be large enough so that the propagation delay ($\sim v/L$) approaches the hot-spot lifetime $\sim 200 \text{ ps}$. For typical device dimensions, this situation will start to become an issue for $L > 6 \text{ }\mu\text{m ps}^{-1} \times 200 \text{ ps} \sim 1.2 \text{ mm}$. While typical nanowire devices are currently smaller than this threshold, they are not a full order of magnitude smaller, so for certain larger devices, this situation should be considered. Such a consideration is complex, and outside the scope of a simple lumped-element SPICE-based treatment, thus we do not pursue it further here. By combining the lumped-element model provided here with standard SPICE transmission-line models, the SPICE model might be extended to accurately describe a distributed nanowire device (e.g. an imager [20]).

2.3. Physical model of a photon-arrival event

A photon will add some energy to the superconducting material. For visible photons, this energy is much larger than the superconducting gap energy Δ . The precise mechanism by which the photon absorption results in creation of a hot-spot in the wire remains a topic of interest [23, 31, 32], but is not relevant to us. The only topic of relevance here is that this added energy leads to a local suppression of I_{SW} of the nanowire by enough to promote a local transition to a non-superconducting normal phase. This phenomenological model of the photon-arrival is adequate for our purposes.

2.4. Circuit model of a nanowire, including photon arrival

While the physical model is informative at the device-design level, at the circuit level it can be a distraction. Therefore, a compact model in which we deliberately neglect the details of the device physics is helpful. In a compact model, the entire device behavior is contained in its terminal characteristics. While recognizing that such a treatment can only ever be approximate, applying the lumped-element abstraction in this way permits enormous simplification of the design process.

The portion of the wire in the superconducting phase behaves electrically like an inductor with inductance L_k from equation (1). In our SPICE implementation, this device was modeled as an inductor with a parametrically defined inductance by specifying the flux in the inductor to be $L_k i_D$ ⁹.

The circuit model also requires a mechanism by which a photon-detection event can be introduced. As discussed in section 2.3, a photon absorption results in a brief suppression of I_{SW} . To replicate this effect in SPICE, we momentarily injected an artificial current into the portion of the nanowire used by the model to sense the device state, which we call the gate. Effectively, rather than reduce I_{SW} , we created a region

⁹ In practice, the inductance will of course also be reduced by the formation of a hot-spot in the nanowire, but this reduction constitutes a trivial fraction of the total inductance during typical operation, so it can be ignored in most situations involving SNSPDs. In our model, we ignored this effect, and treated the device inductance as if it were independent of hot-spot length.

with an artificially enhanced i_D . If more current is inserted into the gate, the effect of the photon is larger. We can thus use a gain parameter to scale the impact of the photon on the nanowire device. The product of the gate current and the gain thus correspond to the degree of current suppression induced by the photon arrival event. We chose the gain parameter in these simulations to be 10 and the gate current to be $1\ \mu\text{A}$ to ensure that every incident photon would lead to a detection event. However, in the presence of current noise in i_D in the nanowire, events could occur when a photon is incident and the mean current i_D is large enough to ensure switching, but noise fluctuations nonetheless prevent switching. This feature could in principle be used to model qualitatively the influence of photon energy and noise on a circuit, but this topic would require an extensive analysis and discussion, and so is beyond the scope of this paper.

3. SPICE implementation of curve-fit circuit model

Now that we have explained the physical and circuit models, we will describe how these models are implemented computationally. In this section, we will describe how the basic curve-fitting model is developed in SPICE.

Figure 1 shows a sketch of a typical i - v curve for a nanowire [27], the curve we must replicate in our simplest device model. To translate this graphical model into a SPICE model of the device, we have to describe the constitutive relation of the device in each of the three states mentioned in section 2.1 above, as well as the ranges of current and voltage over which the device is in each of these states. We will treat each state in sequence.

State 1. In the ‘off’ state, the device is superconducting (region ① in figure 1). Thus the constitutive relation of the device is simply $v = 0$. The range over which this relation applies is $|i_D| < I_{SW}$, where I_{SW} is a device parameter. In practice, I_{SW} is a sensitive function of temperature and may depend on other parameters such as ambient magnetic field, but we will assume the temperature and magnetic field are constant, and so the parametric variation of I_{SW} can be ignored. This assumption is likely valid for magnetic field (where only field variations on the order of the critical fields of the material would be likely to have a measurable effect on I_{SW}), but not for temperature when the device is operated near its reset-time limit. Thus for operating reset times in the 100 MHz range and above, a more careful treatment is likely required.

State 2. In the hot-spot state (region ② in figure 1), sometimes referred to as the hot-spot plateau, the device acts as a constant-current source with $|i_D| = I_{HS}$ for $0 < |v| < I_{HS}R_{nw}$ where I_{HS} is a device parameter, typically a sizable fraction of I_{SW} and where R_{nw} is the resistance of the wire when it is entirely normal, i.e. $R_{nw} = R_{SH}\lambda/w$ where λ is the length of the nanowire.

State 3. In principle, when biased with a sufficiently high source impedance, the entire length of the wire could be put into the normal state (region ③ in figure 1). In this normal state, the i - v relation follows that of a simple resistor,

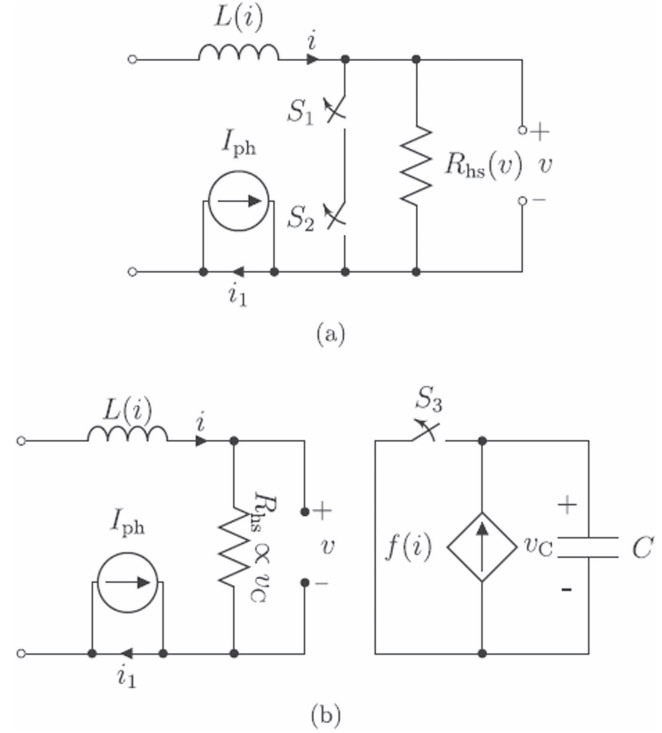


Figure 3. (a) Schematic circuit diagram of the basic-curve-fit SPICE circuit model. This model includes an inductor whose kinetic inductance depends on the current passing through it, and a curve-fit resistor whose resistance depends on the voltage across it. In addition, two switches in series ensure correct transitions into and out of the superconducting state. Finally, a current source with strength I_{ph} is used to trigger photon arrival events, where the current i_1 exceeding I_{SW} is used to trigger S_1 in the event of a photon arrival. (b) Full dynamic model of SNSPD implemented in LTspice showing nonlinear inductor $L(i)$, the ancillary capacitor circuit used to simulate the hot-spot resistance R_{hs} , and ancillary dependent voltage supply circuit that tracks wire state (normal or superconducting).

$v = i_D R_{nw}$. This state applies for $|v| > I_{HS}R_{nw}$. This state is unlikely to occur in a typical passively biased circuit, due to the implausibly large bias and load impedances that would be required (many 10s of $k\Omega$ for practical device parameter values).

In the SPICE implementation, the challenge of accurately modeling the nonlinear normal resistive region (region ② in figure 1), is addressed by having the device current flow through a nonlinear voltage-dependent resistor $R(v)$ that models the hot-spot plateau regime, in which $R(v) = |v|/I_{HS}$.

The SPICE model requires switches to deal with events in which the device transitions back and forth between the normal ② and superconducting ① state. These switches have two key roles to perform: (1) they must take the device out of the superconducting state when a photon is incident on it, or when $|i| > I_{SW}$; and (2) they must return the device to the superconducting state when the voltage drops below some threshold (equivalent to the voltage that would drop across a hot-spot region that is too small to sustain itself). The first condition is based on the device current, while the second is based on the device voltage, so two switches in series are required.

As shown in figure 3(a), the switch network consists of two elements, a current-controlled switch S_1 in series with a voltage-controlled switch S_2 . In the superconducting state, both switches must be closed. In the normal phase, either S_1 or S_2 or both must be open in order to sustain a non-zero voltage across the hotspot¹⁰. The current i_D upstream of the switching network (near the device inductor as shown in figure 3(a)) is used to set the state of S_1 , while the voltage v across the hot-spot resistor is used to set the state of S_2 .

The transition from the superconducting phase to the normal phase is precipitated by the device current exceeding the switching current (recall we simulate the photon arrival event by injecting extra current into a particular device region). S_1 is set to open when $i \geq I_{SW}$, thus when I_{SW} is reached, the switching network becomes an open circuit. S_2 is normally closed, but will open when $v > f I_{HS} R_{SH}$ where $f \ll 1$ is the minimum fraction of a square of resistance presumed to be required to sustain a hot-spot.

Because the current in the inductor cannot change instantaneously, upon S_1 opening, the current that was passing through the switching network is instantly diverted into R_{HS} . At this point, a finite voltage v will appear across the switching network and so the voltage switch S_2 will open and the current through the inductor will start to drop. Very shortly after S_2 opening, the current in the inductor will have dropped enough to permit S_1 to close but at this point S_2 is open and so the hot-spot state is maintained.

One possible practical limitation of the model is the possibility that S_1 might close before S_2 opens, thus preventing the device from ever switching into the hot-spot phase. As we have implemented the model, we have not observed this problem, but it should be considered carefully in future extensions of this work. This might occur if, for example, the device has very low inductance and is shunted by a low impedance externally, permitting the current diverted by S_1 opening to leave the device without developing a significant voltage across it. The simulation time step is relevant here, as an overly coarse time step in a marginal case could potentially lead to artifacts and errors.

Depending on the dynamics of the external circuit, the voltage v across the device can now move up or down (typically desired behavior in the device), or remain constant (typically undesired latching behavior). If v drops below $f I_{HS} R_{SH}$, S_2 will close and the device will return to the superconducting state (remember S_1 is already closed).

To summarize, the sequence of events initiated when a photon hits the nanowire or when i_D exceeds I_{SW} are: (0) prior to the incidence of the photon, S_1 and S_2 start closed; (1) once the current exceeds I_{SW} , S_1 opens, diverting current into the parallel resistive path R_{HS} ; (2) v exceeds the S_2 threshold and S_2 opens; (3) i_D drops due to diverted current into the external circuit and S_1 closes; (4) circuit dynamics then control the evolution of the wire voltage until (5) v drops below a threshold and so S_2 closes, returning the system to its initial state with $v = 0$.

¹⁰ Note that voltage can drop across the inductor even if there is no voltage drop across the hot-spot.

4. SPICE implementation of dynamic device model

Figure 3(b) shows a schematic of the dynamic device model that uses the nanowire electrothermal physics to model the evolution of the hot-spot resistance in time. In this model, the current i_D in the inductor is compared to $I_{SW} - i_{ph} \times g$ where g is a gain value that is set somewhat arbitrarily to 10, and is included so that in future implementations one can represent effects associated with photon energy. If the suppressed switching current is exceeded by i_D , a hot-spot is formed in the detector. This hot-spot is modeled as a resistor with a state variable, i.e. whose resistance R_{HS} depends on the history of the current through the device. This resistor is implemented in SPICE as a current-dependent voltage source. The normal/superconducting phase of the device is tracked by using a DC voltage source in parallel with a resistor as a memory element. This tracking is not absolutely necessary, but is convenient for debugging and enhances understandability of the circuit. We will explain each component of the device model in more detail here.

To model the hot-spot growth, we used the Kerman electrothermal model [28]. This model has been experimentally verified in the range $L = 6\text{--}605$ nH and with a load impedance of $20\ \Omega\text{--}1$ k Ω with device switching currents of $20\ \mu\text{A}$. Outside this range, verification should be performed before relying on this model. However, this range encompasses typical SNSPD device parameters.

The expression in equation (2) models the rate of change of the resistance of the nanowire with current. This expression goes to zero at $i_D = \sqrt{2/\psi} I_{SW} = I_{HS}$ and diverges at $i_D = \sqrt{1/\psi} I_{SW}$. The divergence originates because we fit to the phenomenological model in [28] and occurs beyond the range of experimental verification of that model. As a result, it is appropriate to simply eliminate the divergence mathematically, as described in appendix B of the online supplementary material.

In SPICE, the total device resistance can be calculated by integrating dR_{HS}/dt in time. We performed this integral in the simulator by integrating a current on a capacitor. To do this, we created an ancillary circuit, disconnected from the main circuit, consisting of a current source and a capacitor. The current value of the source as well as the capacitance were set so that the voltage on the capacitor would correspond to the hot-spot resistance, integrated from equation (2). The capacitance was $C = w/(2R_{SH}v_0)$ and the current source had value $f(i) = (\psi i^2/I_{SW}^2 - 2)/\sqrt{\psi i^2/I_{SW}^2 - 1}$. The voltage across the capacitor v_C was then used in the main circuit to set the instantaneous resistance of the nanowire. We assigned negative v_C values to correspond to zero hot-spot resistance, to ensure the hot-spot resistance could never be negative. The only purpose of the ancillary circuit was to perform this integral. This approach is common practice in SPICE modeling of thermal effects [33].

To complete the hot-spot model, a mechanism was required to permit hot-spot formation and the recovery of superconductivity in the primary circuit. To accomplish this set and reset function, a normally closed switch was used in

parallel with the ancillary capacitor, such that v_C was forced to zero except when a hot-spot was present. The state of the nanowire (superconducting or with a hot-spot) was tracked by the small secondary ancillary circuit mentioned earlier. The complete hot-spot model including both ancillary circuits is shown schematically in figure 3(b).

5. Parameter extraction

Understanding the physical model of a device and modeling its qualitative behavior is inadequate for the goal of designing complex circuits that include superconducting nanowires. Accurate extraction of device parameters for use in the model is a key additional task. The values required to accurately model the device include geometric and material parameters, most of which can be ascertained from electrical tests.

The first key parameter required in the model is the sheet resistance R_{SH} which can be estimated by a DC resistance measurement of a long nanowire at 20 K (two-point measurements are typically adequate because the sheet resistance is typically much larger than contact resistances in these materials). Room-temperature values differ from 20 K values by at most a factor of two, and thus room-temperature values can be used as approximate starting points, although low-temperature values might give more accurate results. Because the sheet resistance can vary with temperature at low temperatures for very thin films, an ideal measurement would suppress the superconductivity in the device with magnetic field and measure the resistance in the normal phase at the operating temperature. For nanowires with a high series inductance or large shunt impedance (or both), to first order the sheet resistance of the material only affects the slope of the rising edge, not the amplitude (the amplitude is simply $i_D R_L$, where R_L is the load impedance), as nearly all the bias current is ultimately diverted from the nanowire in a switching event. As such, great care in extraction of sheet resistance values need not be taken for modeling simple nanowire circuits.

The second key parameter required is the material inductivity. This value can be measured directly as described in [25], or calculated from T_C by using the expression for the kinetic inductivity per square of $\hbar R_{SH} / \pi \Delta$ where Δ is the superconducting gap which is related to T_C by the BCS relation $\Delta \approx 1.76 k_B T_C$ [27]. T_C is determined by measuring resistance versus T and recording the temperature at which the resistance drops to 10% of the pre-transition resistance.

The fractional error in the fabricated versus nominal nanowire length is typically negligible, but not so for the width, which depends on the lithographic and etch parameters used in the fabrication process. Thus it is preferable to estimate the nanowire width electrically, either by using the known sheet resistance in combination with a resistance measurement of the wire, or by measuring the width of a number of wires with various nominal widths and fitting their resistances to a model in which a fixed offset from nominal width is assumed.

Two important electrical and electrothermal parameters that must be determined are I_{SW} and I_{HS} . I_{SW} can be determined by increasing the bias current and measuring the current at which a voltage first appears across the device¹¹. I_{HS} can be measured by taking a complete $i-v$ curve of a nanowire (both while increasing and while decreasing i_D) and recording the level of the hot-spot plateau. I_{HS} and I_{SW} can then be used to calculate the Stekly parameter ψ by observing that at I_{HS} the hot-spot is stable, thus equation (3) has a zero at this current. This argument implies that $\psi = 2(I_{SW}/I_{HS})^2$.

The substrate temperature can be estimated by using a well-constructed and calibrated thermal sensor attached to the stage holding the nanowire chip while ensuring adequate thermal contact between the chip and the substrate.

The only parameter remaining to be extracted is the capacitance C in the ancillary circuit used to determine the hot-spot resistance. This capacitance can be expressed as:

$$C = w / (2R_{SH}v_0) = wc\sqrt{d} / (2R_{SH}\sqrt{h_c\kappa}) \quad (6)$$

which requires an estimate of the nanowire-to-substrate conductivity h_c , the nanowire thermal conductivity κ , and the volumetric heat capacity c .

The nanowire-to-substrate specific thermal conductivity h_c can be estimated from other known parameters by using the expression $h_c = I_{SW}^2 R_{SH}^2 / (\psi w^2 (T_C - T_s))$ which is readily derived from the expression for ψ given in equation (4).

The nanowire thermal conductivity κ and volumetric heat capacity c are difficult to determine experimentally. In this case, we settle for using the literature values summarized in [30]. It is somewhat reassuring that previous work [30] has successfully modeled devices electrothermally by using published values of these parameters, even though their accuracy across different materials, substrates, and measurement methodologies may be suspect. This circumstance is likely at least in part because of the relatively weak (square-root) dependence of v_0 on h_c and κ .

Quantitative fits to experimental results might be used to further refine the correct model parameters. Certain aspects of device behavior would be particularly sensitive to various fitting parameters, for example the slope of the rising edge of the detection signal, if measured with sufficient precision, would perhaps give a better and more relevant estimate of the ψ parameter than the method proposed above. Similar, fitting the model to observed latching thresholds might be an alternative approach to determining the thermal constants of the system. However, one would have to be careful not to include systematic errors in this process, as it would have a weaker connection to the underlying physics of the model. This approach could be pursued in future work.

¹¹ Because I_{SW} increases with the slew rate of i_D [34], the ramp slew rate should be specified with any careful I_{SW} measurement (but unfortunately rarely is). We typically use a longer-than-1 s slew time when measuring I_{SW} , and make several measurements, ignoring the occasional outlier value.

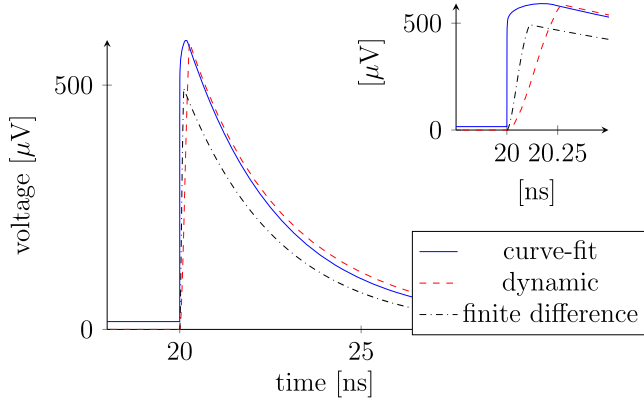


Figure 4. Comparison of voltage output pulses from basic curve-fit and full dynamic models. Inset illustrates the rising edge, where the difference is most noticeable. The curve-fit model assumed current-independent inductance of 130 nH, while the dynamic model assumed zero-current inductance of 130 nH. Both models were performed using a $50\ \Omega$ load, $15\ \mu\text{A}$ bias current, and a $20\ \mu\text{A}$ I_{sw} . All other parameters were as specified in the text.

6. Examples

To illustrate the power of these models, we tested them on a number of example circuits. The examples we describe in detail include the SNSPD, the SNAP, and a photon-number-resolving (PNR) detector. The SNSPD example is discussed in the main body of the paper, while the SNAP and PNR examples are discussed in the online supplementary material.

For all examples aside from the basic photodetection example, we used the dynamic device model. For the basic photodetection example, we compared the dynamic device model, the curve-fit model, and the more traditional full electrothermal device model [8] to experimental data.

There are a number of aspects of the devices that our simple SPICE model replicates, including latching, the influence of device inductance and load impedance on the electrical reset time, relaxation oscillations that result from driving the device above I_{sw} , and the excess bias current that is known to result when the device output is capacitively coupled to its output resistor [35]. We explore these aspects in the following subsections.

6.1. Basic photodetection by SNSPDs

Figures 4 and 5(b) shows the results of simulating a basic SNSPD with the models described here. We include a comparison of the basic curve-fit model, the dynamic device model in figure 4, and the traditional finite-difference-based model. A comparison of the dynamic device model and an experimental result is included in figure 5(b).

To verify the properties of the devices, we observed the characteristic rise and decay time of the edges of the photon pulses by using the basic-curve-fit model. In this model, the rising edges are very fast because the resistance of the device in the normal state is tens of $\text{k}\Omega$ at least. As a result the time constant over which the current changes after S_1 opening will be in the few-picosecond range. The falling edges follow the usual much-longer time constant set by the inductance of the

device and the input resistance of the readout circuit. We further observed the effect of blocking, in which closely-spaced photons result in fewer pulses, as subsequent photons are not detected because of suppressed current in the nanowire during the photon arrival event.

We used the electrical parameters estimated from experiments and the device presented in [7] for a large-area SNSPD. We additionally measured the scattering parameters of the amplifiers used to readout the device and built a simple LRC circuit model of the amplifier based on those parameters. The resulting filter model is shown in figure 5(a).

We inserted a pulse at the gate port to observe the basic switching and appropriate reset of the device. We point out that one could also use a script to generate photon-arrival events with appropriate Poisson statistics, and input these events into the gate to simulate random photon arrival processes from a laser source. This procedure could be useful to better understand the dynamic range and blocking loss associated with the device.

As shown in figure 4, the voltage across the load resistor shows the expected pulse shape with approximately exponential decay. In the inset, we compare the rising edge of the dynamic device model output with the curve-fit model output. The dynamic device model accounts for the finite rise time of the pulse. We also show the results of the traditional electrothermal finite-element-based model for this device. This model is substantially more complex, including temperature dependence of various parameters, and thus is not expected to agree perfectly with the model used here.

6.2. Relaxation oscillations in SNSPDs

As a confirmation that both of our models can reproduce relaxation oscillations known to occur in over-biased SNSPDs [36], we simulated an over-biased device with $i_D = 1.05I_{\text{sw}}$ and observed the expected oscillations. These oscillations occur when an overbiased detector forces current out of the nanowire long enough for the device to cool. Eventually, the current returns to the device, the device switches and the cycle repeats. Figure 6 shows relaxation oscillations occurring within an over-biased nanowire as simulated by our SPICE model.

6.3. AC-coupled readout of SNSPDs

One of our key purposes in creating this model was to enable study of the effect of the readout circuit on SNSPD performance. As an example of this influence, we simulated the effect of a capacitor in series with the output load. This effect leads to back-biasing: a count-rate-dependent bias-current variation in the device. This effect was first described in [35], and then described again in more detail in [37].

To replicate the back-biasing effect, we performed a simulation where we included a more realistic model of the output load. The full model is described in figure 5(a) and was extracted by fitting a simple band-pass design to the observed low- and high-frequency roll-off of our amplifiers. Performing a $\sim 1\ \mu\text{s}$ transient simulation, we observed a clear

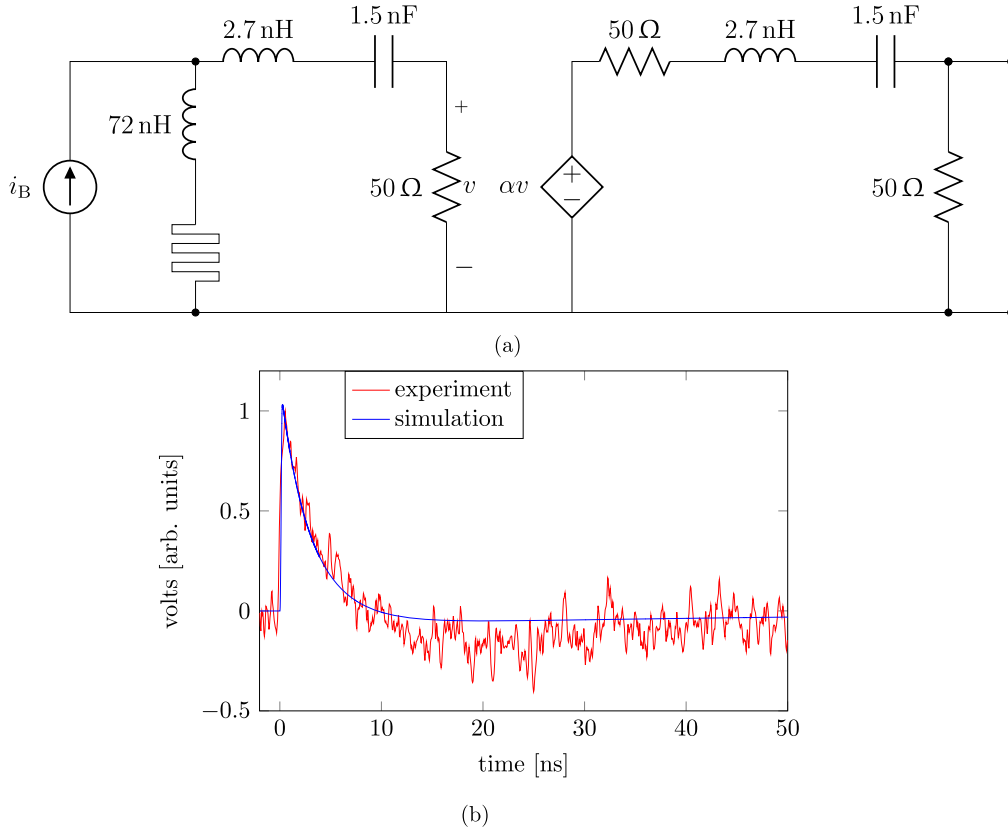


Figure 5. (a) Circuit including readout of SNSPD pulse. The output load was based on cascading two bandpass filters whose parameters were extracted from the measured transfer-function characteristics of amplifiers used in our experiments. A ~ 72 nH inductor was included in series with the SNSPD to control latching. α is a gain factor, and can be negative depending on the desired direction of the output signal. (b) Comparison of full dynamic model and experiment using $T_C = 11.4$ K, $T_s = 2.7$ K, $R_{SH} = 429 \Omega/\square$ at room temperature, $w = 50$ nm, nanowire length $\lambda = 128 \mu\text{m}$ giving an estimated inductance of 62.5 nH, $I_{SW} = 7.2 \mu\text{A}$, $i_B = 6 \mu\text{A}$. Inductances were calculated by using sheet resistance at room temperature, the measured critical temperature, and the nominal device dimensions rather than measured dimensions, and are thus not expected to be particularly accurate.

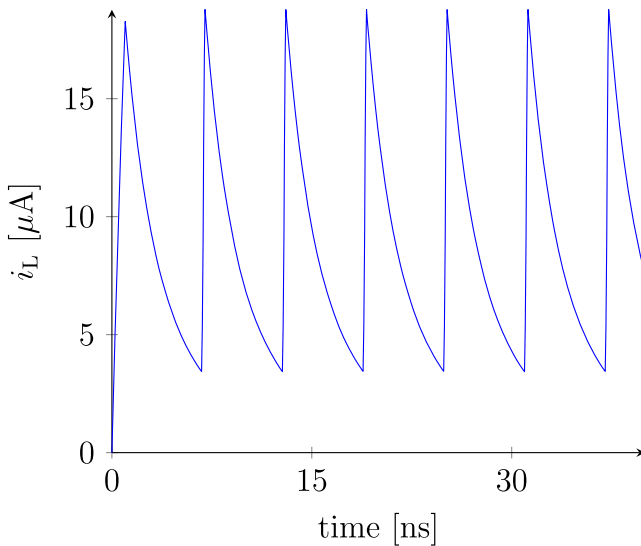


Figure 6. Current through load resistor i_L versus time for an over-biased nanowire, showing characteristic relaxation oscillations whose period depends on the device inductance and load impedance (in this case set to 25Ω). In this biasing condition, the input photon pulses have minimal effect.

transition from a pulsing regime to a relaxation-oscillation regime and then to a latching regime. We understand this transition as being the result of the bias current steadily rising as the capacitor started to discharge back into the SNSPD. An observed steady increase in pulse amplitude in the pulsing regime and a DC offset in the oscillating regime provided further confirmation of this understanding. These data are shown in the online supplementary material accompanying this paper.

6.4. Latching of SNSPDs

When SNSPDs are biased close to their critical current and connected to a load, the timescale of electrical restoration of their current can be so fast that the current bias can be restored before the device has cooled completely. In that case, the device can switch back into the normal phase and latch into a stable resistive state. In this state, the device is not sensitive to future photon-arrival events. We refer to this process as latching.

The device was simulated using parameters consistent with latching by using the full dynamic model. The

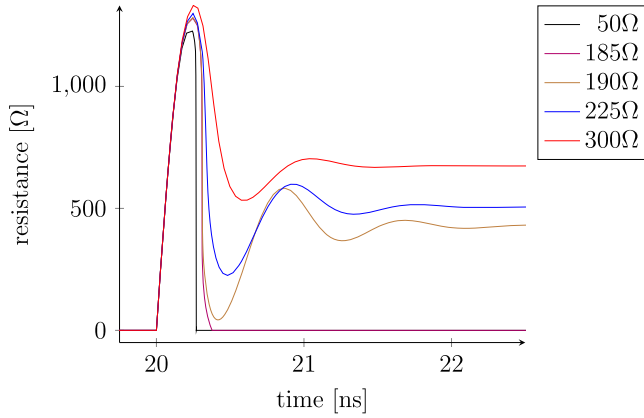


Figure 7. Nanowire hot-spot resistance as a function of time after a photon arrival event occurring at $t = 20$ ns. The simulation exhibits a transition from a non-latching (self-resetting) domain to a latching domain as the load resistor is increased, corresponding in a decrease in the electrical reset time. The following parameters were used for this simulation: $I_{SW} = 20 \mu\text{A}$; bias current $i = 15 \mu\text{A}$ via a voltage source in series with a $100 \text{ k}\Omega$ resistor. $L_o = 130 \text{ nH}$; $w = 100 \text{ nm}$; $d = 4 \text{ nm}$; $h_c = 50\,000 \text{ W m}^{-2} \text{ K}^{-1}$, $\kappa = 0.108 \text{ W m}^{-1} \text{ K}^{-1}$; $c = 4400 \text{ J K m}^{-3}$; $R_{SH} = 400 \Omega/\text{square}$, $T_s = 2 \text{ K}$; $T_C = 10.5 \text{ K}$.

simulation circuit along with simulation results appear in figure 7. The results showed that, as expected, latching occurred with increasing load resistance. The threshold for latching was between 185Ω and 190Ω . These results are consistent with previous electrothermal simulations [8] and experimental results [28].

7. Discussion

Of course it is not possible to model every aspect of the device physics in any circuit model. Here we discuss some of the advantages and known failings of our model, and suggest some approaches that might refine the model further.

First and foremost, the entire theoretical framework on which the model is phenomenological, as described in [28]. Thus, this model at best only approximates the device electrical characteristics.

Nonetheless, the model has two key advantages over other modeling options: (1) convenience, and (2) speed. Because free and simple implementations of SPICE exist (e.g. LTspice [13]), this model can be quickly and conveniently applied. This convenience may be particularly valuable when integrating nanowires with more complex semiconducting and superconducting readout circuitry.

In addition, while a typical electrothermal simulation of a multi-element device (e.g. a SNAP circuit) can take ~ 1 min per 100 ps, on typical laptop computers, the SPICE implementation takes only a fraction of a second.

With the convenience of SPICE implementation comes certain disadvantages in terms of accuracy and completeness of the model. One key factor that is missing from the model we have presented is a treatment of the temperature-dependence of the thermal device parameters, as well as the

possibility of multiple systems (e.g. electron, phonon) with various temperatures and couplings. These omissions can have important consequences for some designs, and for achieving consistent quantitative agreement with thermal effects such as latching and after-pulsing. Thus far, we have not needed to deal with these additional complications, but we expect ultimately it will be important to do so. The temperature dependence of the normal resistance and the thermal parameters is of particular concern at lower temperatures, where this dependence could slow down thermal equilibration. Extensive experimentation would be required to accurately determine the temperature dependence of these parameters.

In addition, the electrothermal physics that describes the device operation has only been rigorously tested for NbN-based devices. WSi [38] and NbTiN [39] devices have not yet been studied in detail in this regard, and the relevant physical parameters for these materials are not yet known, so one should approach modeling of these devices with caution.

Still one more important factor is the accurate treatment of the microscopic electrodynamics of the system. For small-area detectors, the lumped-element model that we use throughout may be accurate, but for longer nanowires it is possible that there are non-trivial dynamics introduced that are not accounted for in the lumped-element model. In particular, it would be interesting to examine whether parasitic capacitance plays an important role, particularly in limiting the initial rate of hot-spot expansion. This capacitance could provide an alternative path for current across the wire in the moments immediately after hot-spot formation. Thus, inclusion of parasitics in the model would be a valuable next step in refinement of the model.

As a final word of caution, SPICE as a framework for circuit modeling is somewhat limited. Indeed professional design efforts would more commonly use a higher-level design language such as Verilog A. Translation between SPICE and Verilog A is straightforward (indeed, parts of this model originated in Verilog A before being transferred to SPICE), and would be a worthwhile extension of this work.

8. Conclusions

The central result of this work is the demonstration of an accurate and convenient SPICE-based circuit model of a superconducting nanowire across a technologically useful range of materials and device dimensions.

It may be useful at this point to state concisely the scope and limitations of the model. The model correctly estimates nanowire-switching effects including: (1) rise time of the signal; (2) signal amplitude; (3) reset of the device (with the exception of afterpulsing); and (4) latching of the nanowire. It does not correctly model the electromagnetic propagation delay of the signal, nor does it model afterpulsing. Nonetheless, the aspects that it successfully models include the majority of important properties of the wires, and the model is thus of practical utility in designing future nanowire-based circuits.

The electrical [24] and electrothermal models [8, 28] of SNSPDs and their impact on device performance [30] were well-understood prior to our work here. Thus one might assume that there is little additional utility that we could hope to glean from a new implementation of these models. However, the convenience and accessibility of SPICE-based circuit modeling permits rapid design development, and thus serves to facilitate future nanowire device development.

In future work, various additional aspects of the device operation could be incorporated into the model. For example, it should be possible, by including electrical noise in the triggering sense current i_1 and varying the value of the photon-event current I_{ph} , to observe a dependence of device efficiency on bias current using this model. A comparison of this dependence to the experimentally observed dependence of efficiency on different photon energies would help illuminate the origin of the shape of that dependence which remains a topic of academic and practical interest to the field [31, 40, 41].

Electrical noise inclusion may also help in modeling jitter. A number of recent results suggest that jitter may in part be due to the presence of noise in the pulse amplitude accompanied by a finite pulse slew rate on its rising edge [19, 42, 43]. As a consequence, we expect that the dependence of device jitter on bias current and device architecture could be at least partially explained by this model given an accurate estimate of the circuit noise in the device.

The model also enables estimates of power dissipation in the device by considering the current and voltage at the device terminals (clearly current and power in the ancillary circuits should not be included in such a calculation). This treatment could be useful in the future in estimating thermal loads for systems using realistic multi-nanowire circuits (e.g. in detector arrays).

As a consequence of this model, we expect it will be possible to develop similar models for related electrical components such as the three-terminal superconducting nanowire amplifier [9], and the nanowire cryotron (or nTron) [10] circuits. We also expect further refinements of the model to be possible and indeed necessary as these devices develop in sophistication and the need for more accuracy follows.

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